

NBWAA

Low Cost Los Angeles 10L

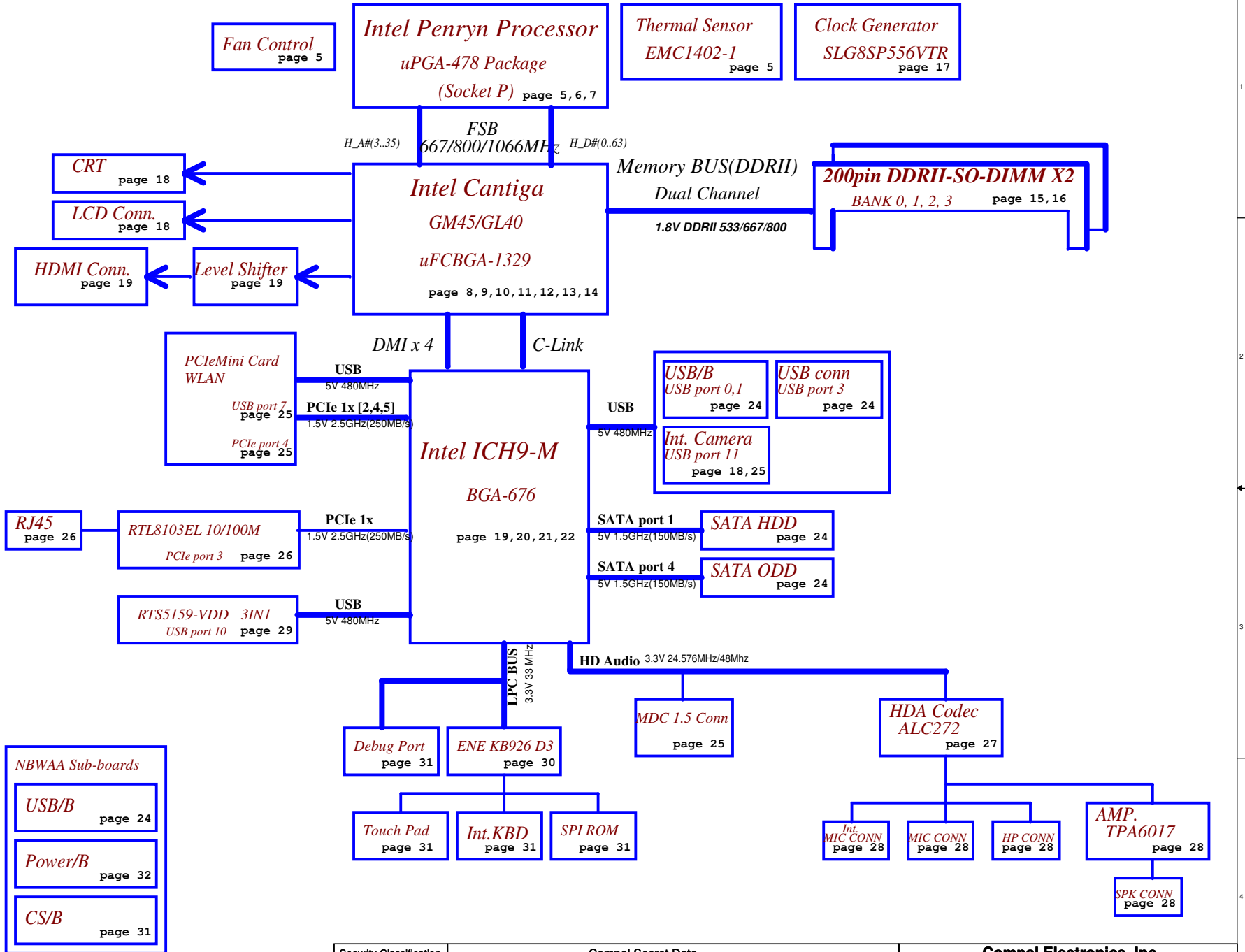
LA-5821P REV 1.0 Schematics

Intel Penryn/ Cantiga/ ICH9M
2008-08-10 Rev. 1.0

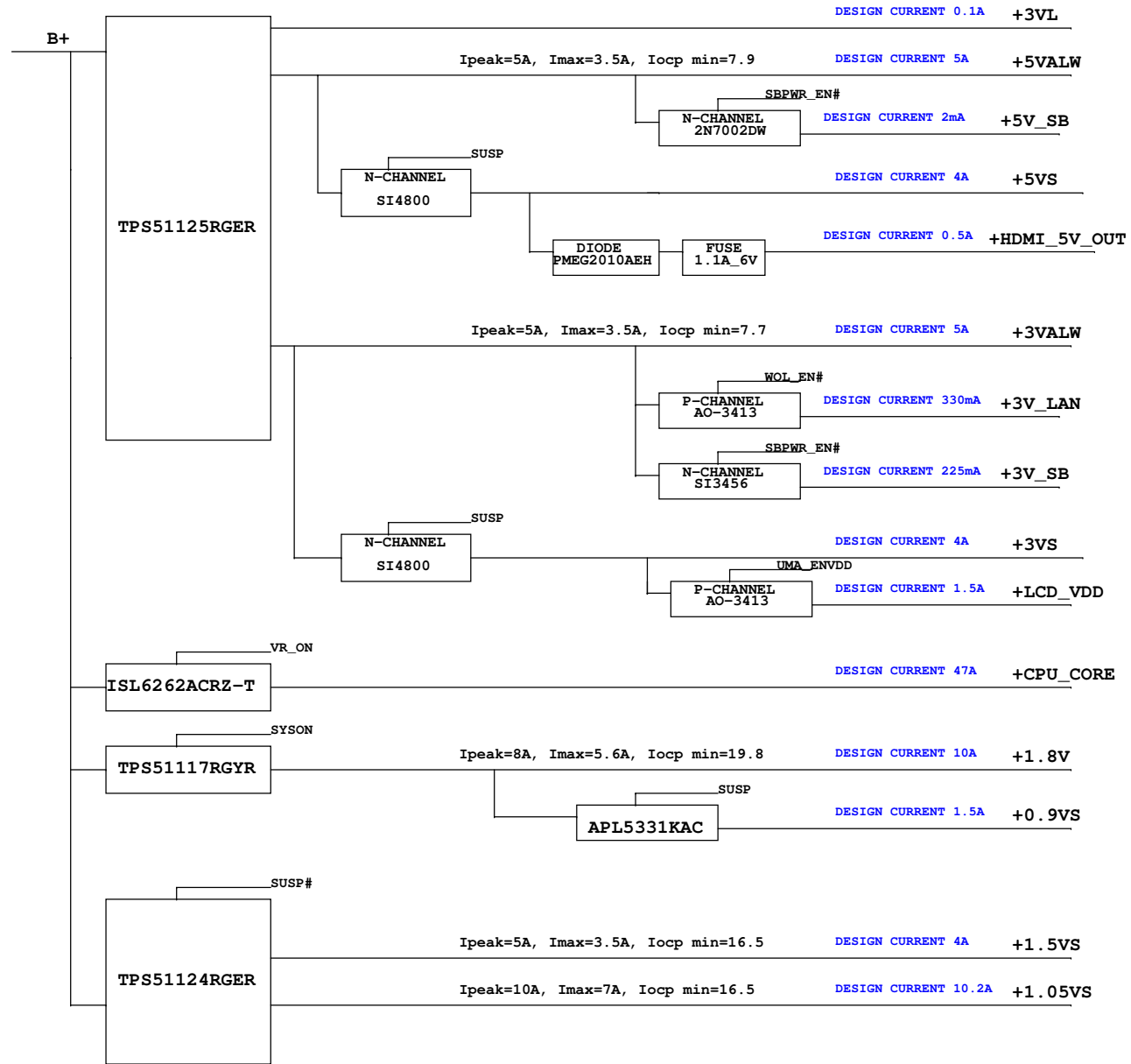
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Compal Confidential

Model Name : NBWAA
File Name : LA-5821P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON		HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH		
S5 (Soft OFF)		LOW	LOW	LOW	LOW		
G3		LOW	LOW	LOW	LOW		

BTO Option Table

Function	North Bridge		RJ11	CAMERA	MIC	HDMI	
description	GM	GL				Y	
explain	GM45	GL40	MODEM	CAMERA	MIC	HDMI	Non-HDMI
BTO	GM45R3@ GM45R1@	GL40R3@ GL40R1@	MDC@	CAM@	MIC@	IHDMI@	NIHDMI@

External PCI Devices

EC SM Bus1 address

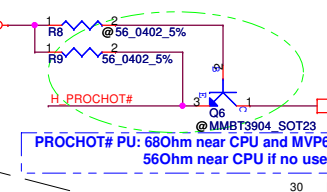
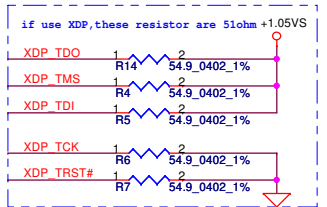
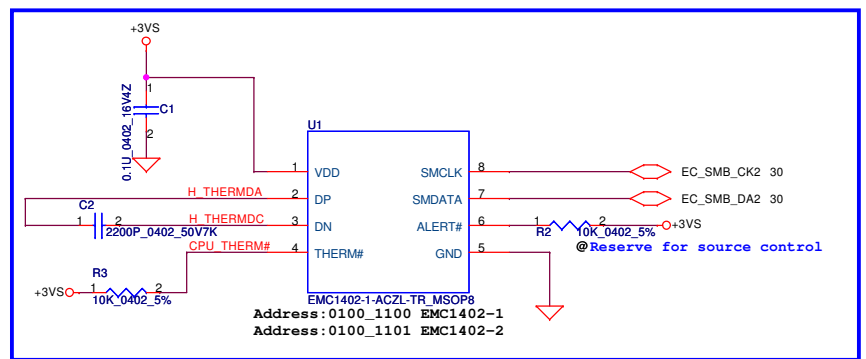
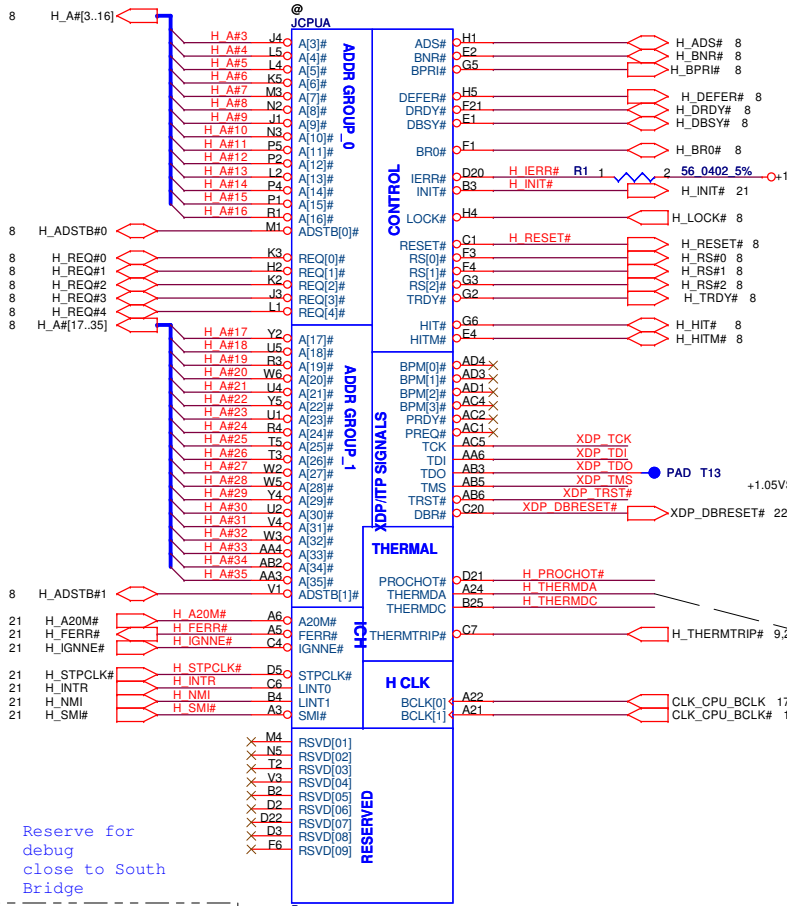
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 01X b	+3VS	CPU THM Sen	
+3VL	FUN/B (CAP Sensor)		+3VS	SMSC SMC1402	0100 110x b

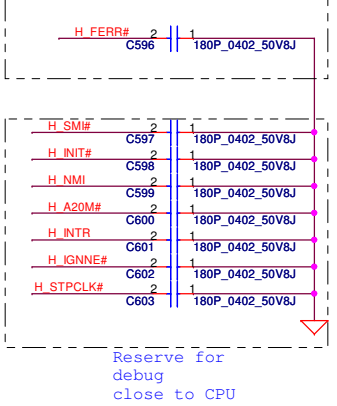
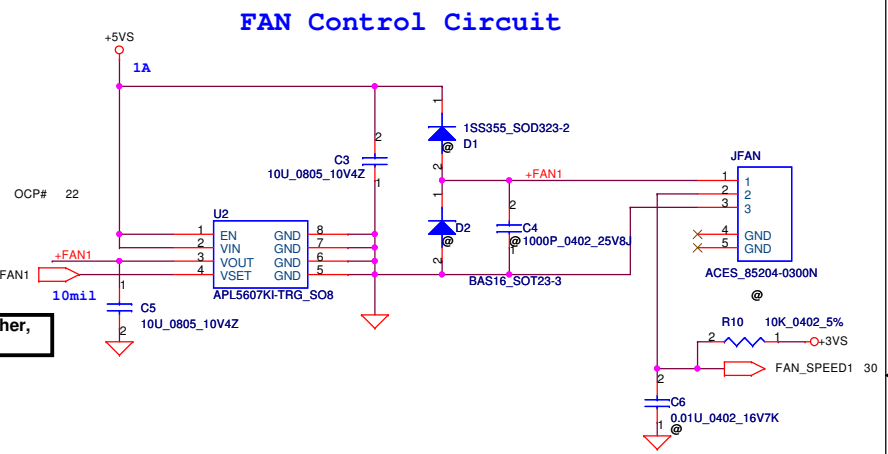
ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS		

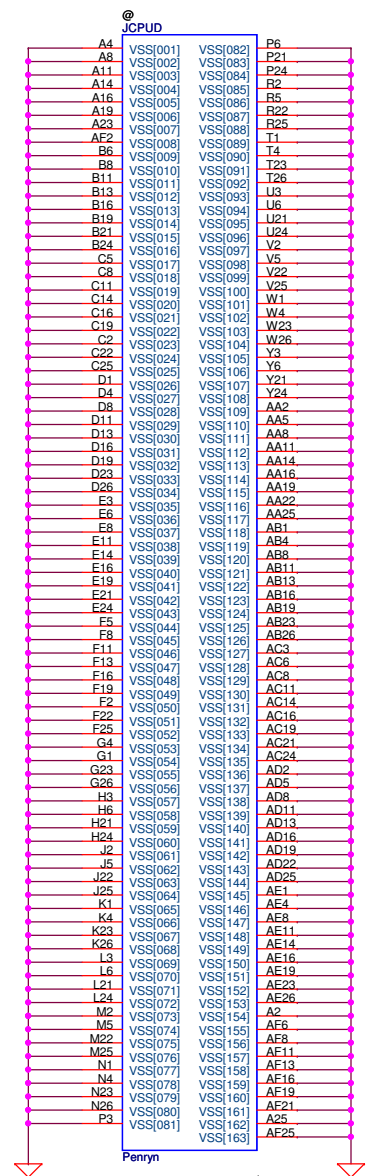
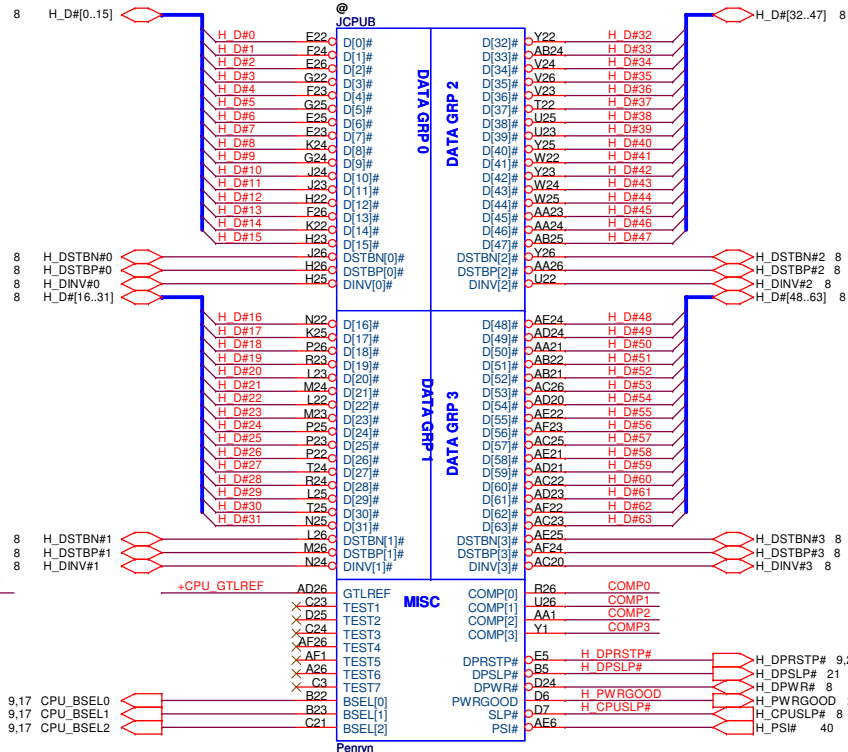
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				Notes List
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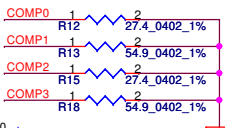
**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**



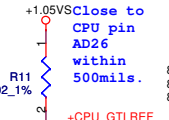
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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

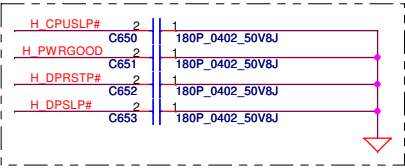


layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

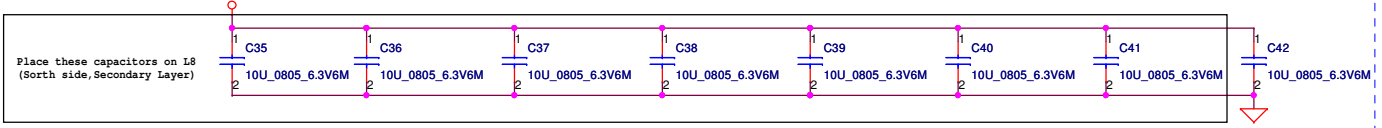
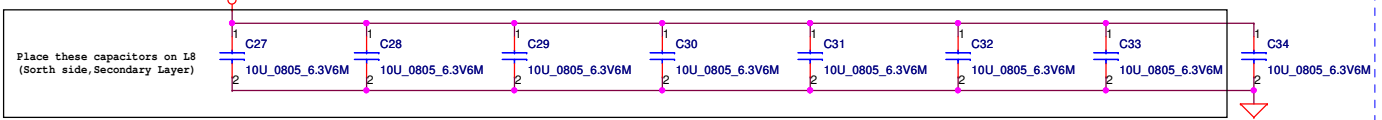
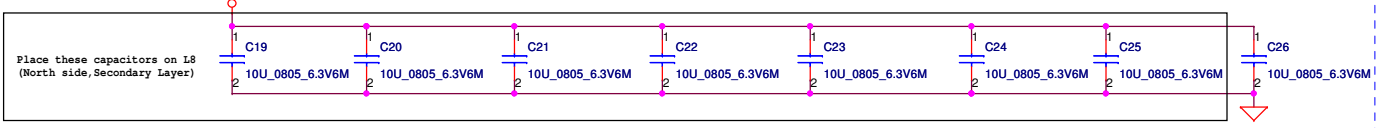
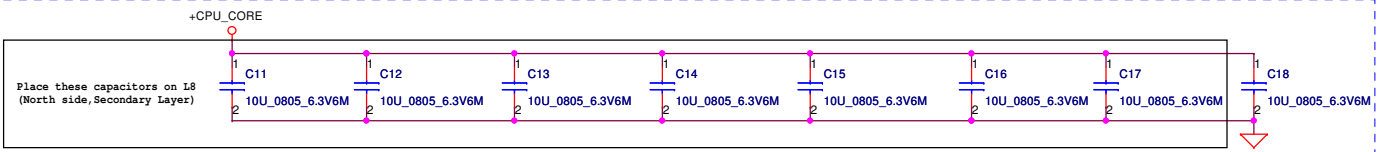
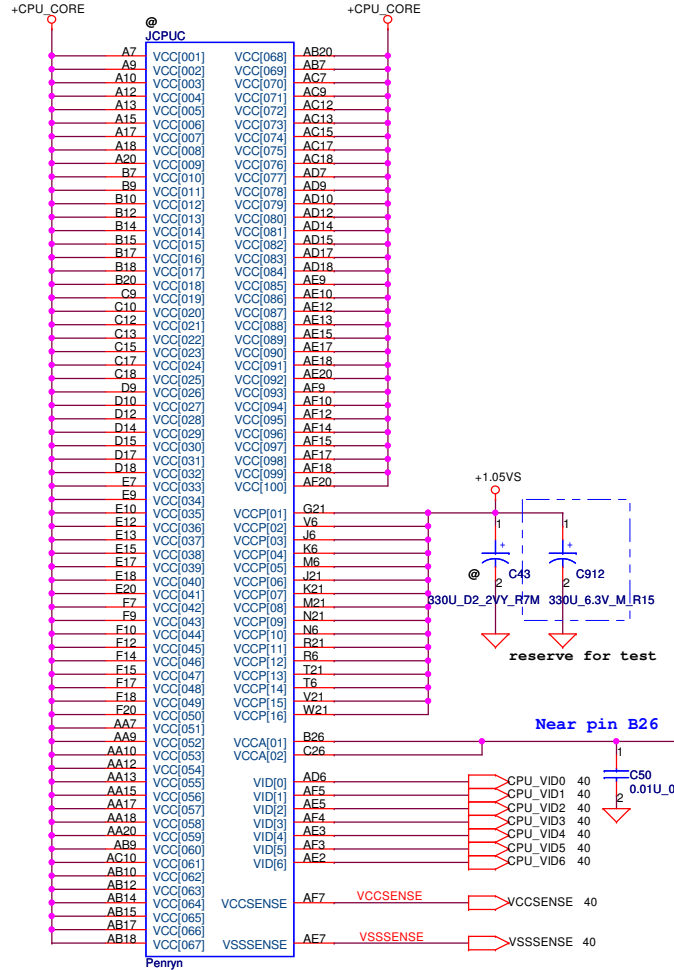
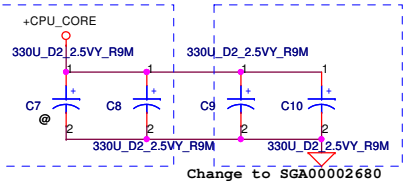
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



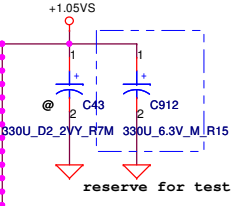
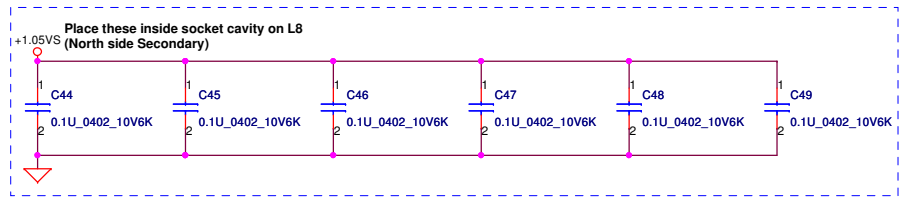
Reserve for debug close to CPU

Near CPU CORE regulator

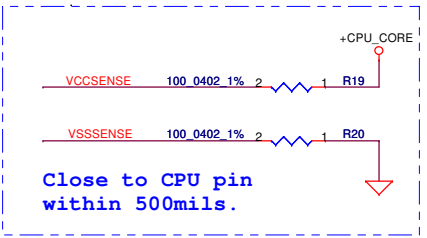
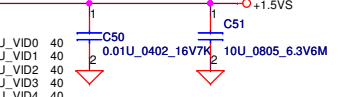
ESR <= 1.5m ohm
Capacitor > 1980uF



Mid Frequency Decoupling

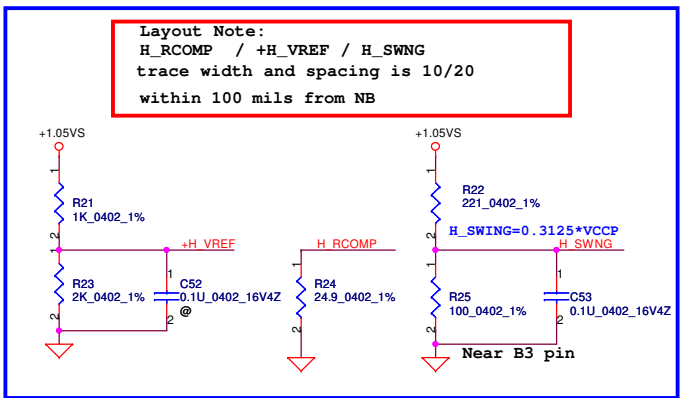
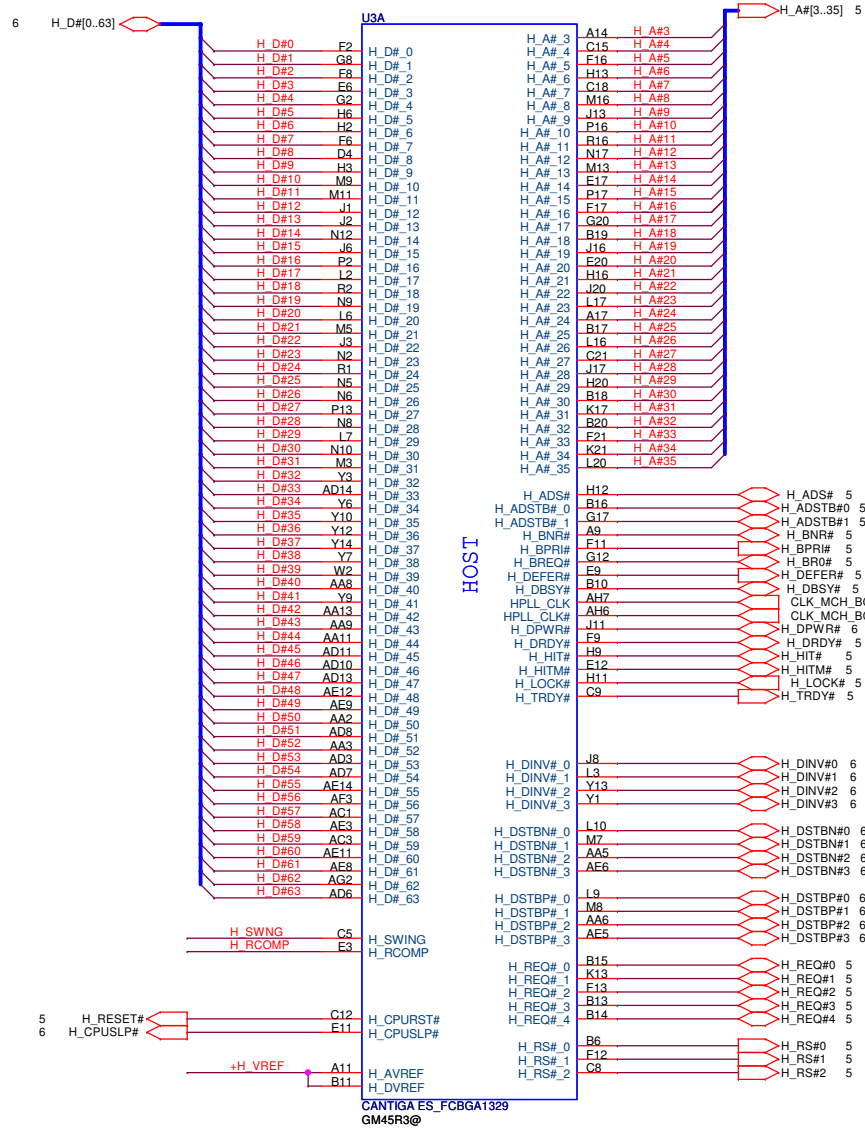


Near pin B26



Length match within 25 mils.
The trace width/space/other is 14/7/25.

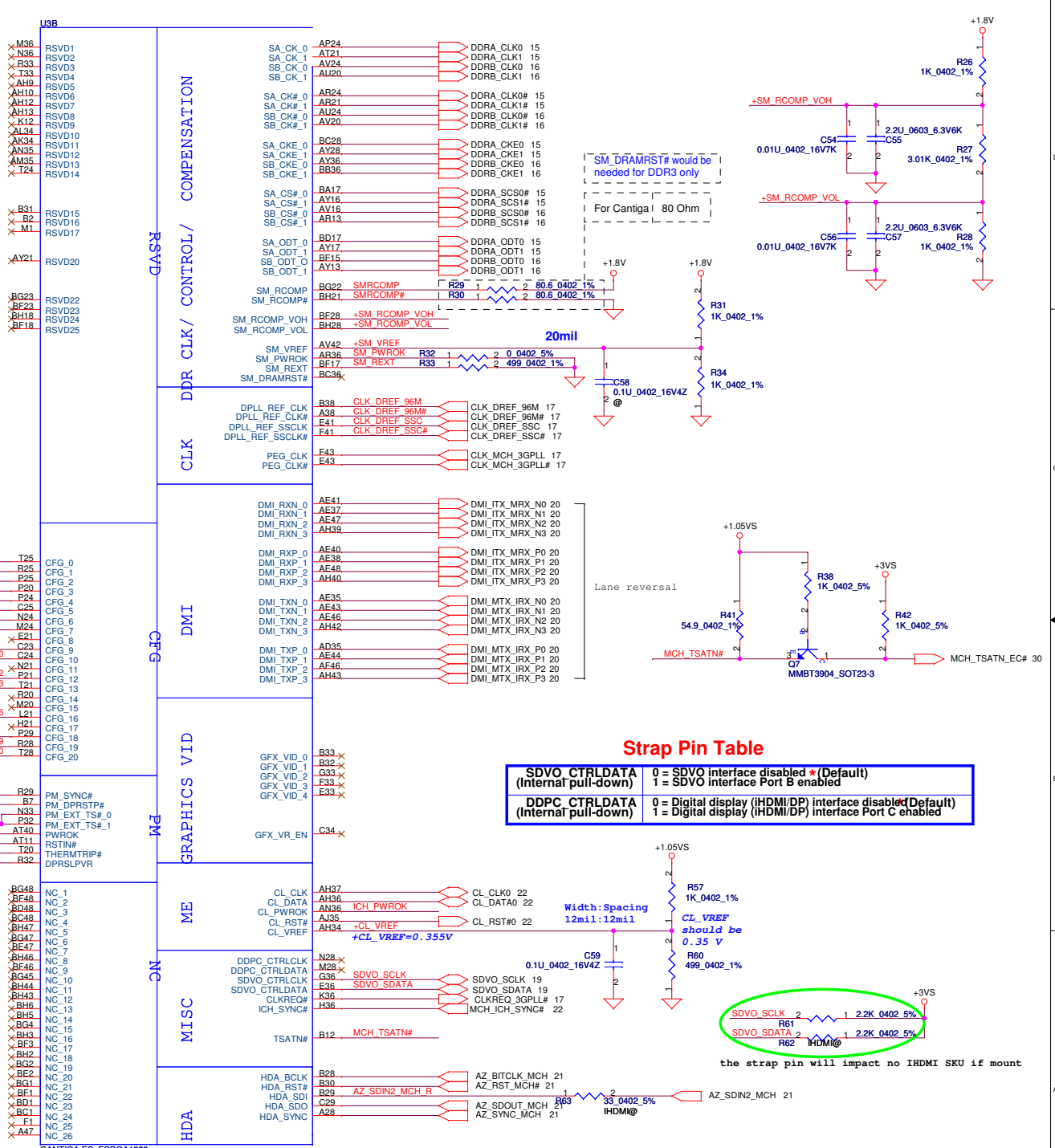
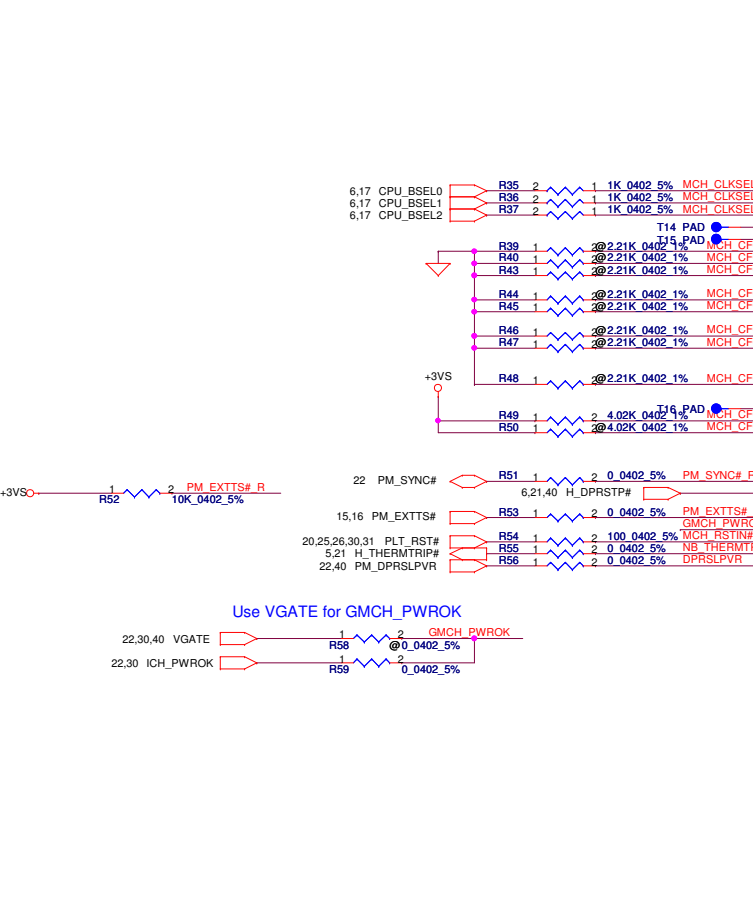
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				Penryn(3/3)-PWR/Bypass	
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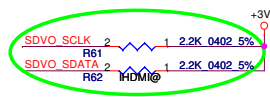
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = ITPM Host Interface is enabled can support disable by SW. 1 = ITPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. *(Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO Interface disabled *(Default) 1 = SDVO interface Port B enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (IHDMI/DP) interface disabled*(Default) 1 = Digital display (IHDMI/DP) interface Port C enabled

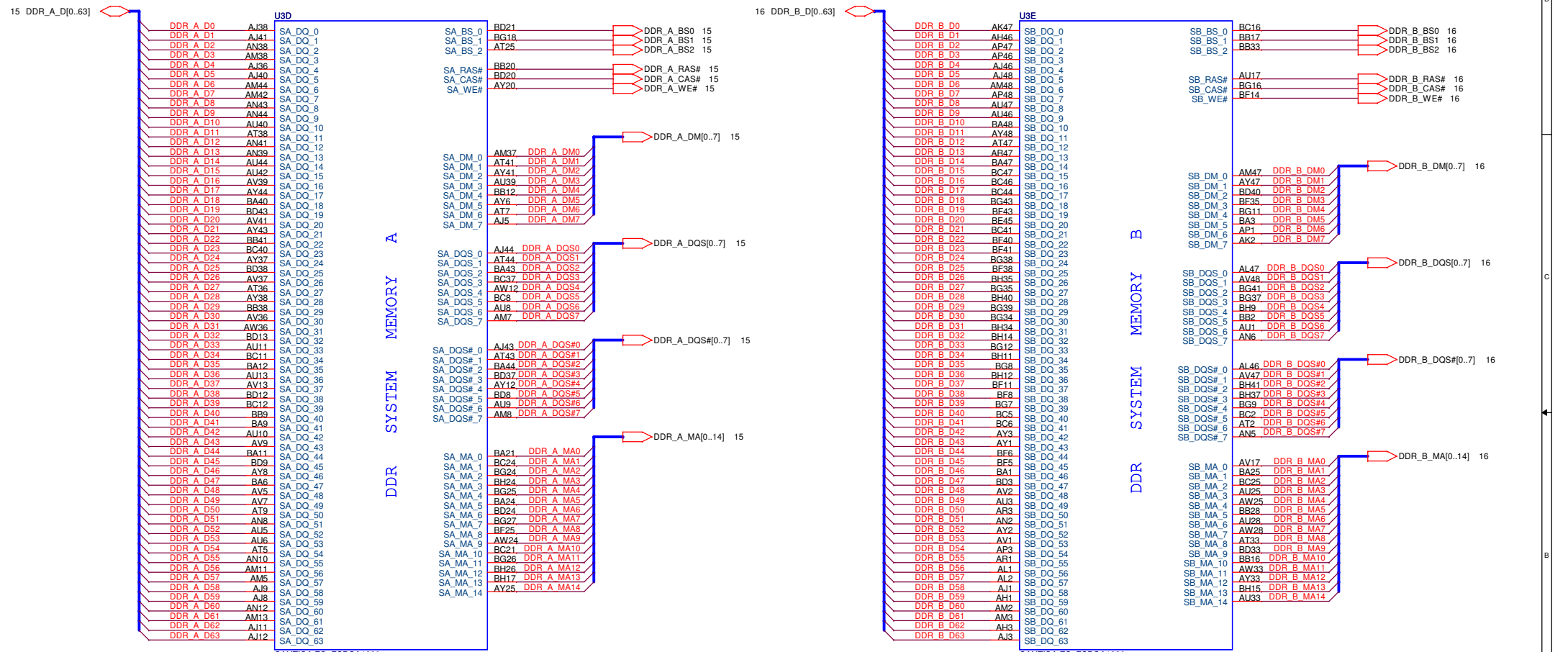


CANTIGA ES_FCBGA1329
GM45R3Q

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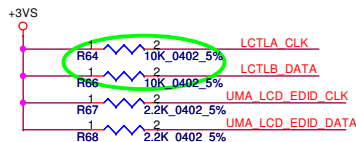
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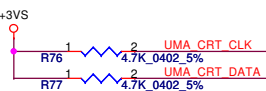
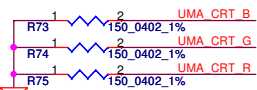
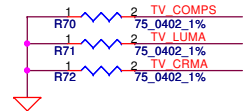
CANTIGA_ES_FCBGA1329
GM45R3@

CANTIGA_ES_FCBGA1329
GM45R3@

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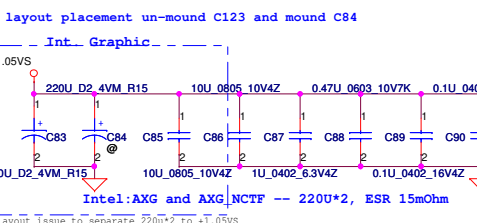
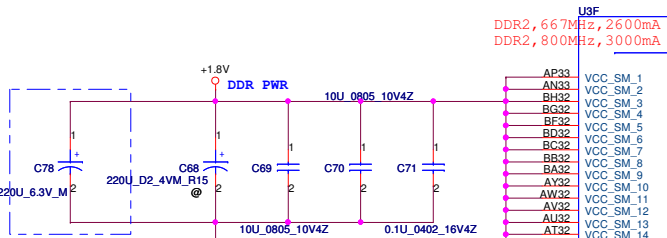


L_DDC_DATA
 0 = LFP Disable * (Default)
 1 = LFP Card Present; PCIe disable



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 GM45R3@

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DDR2, 667MHz, 2600mA
DDR2, 800MHz, 3000mA

Extnal Graphic: 1210.34mA
Integrated Graphic: 1930.4mA
Intel Management Engine Link:508.12mA

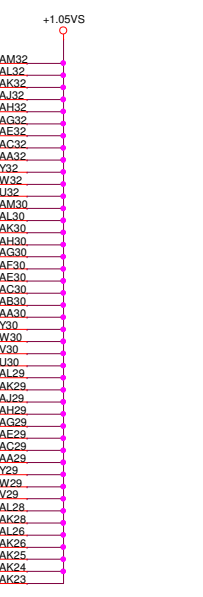
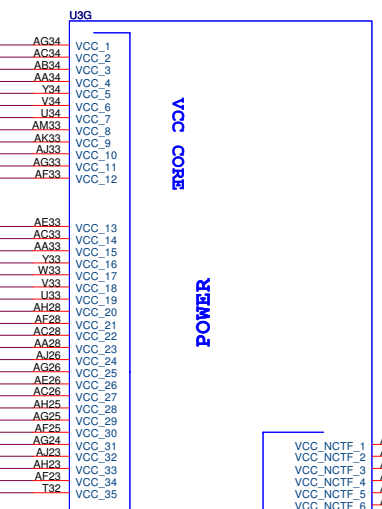
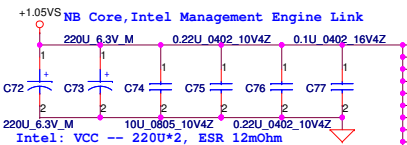
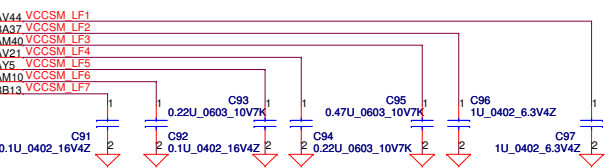
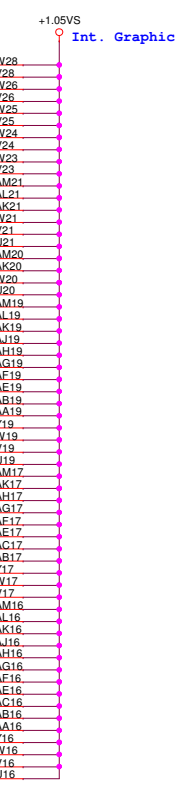
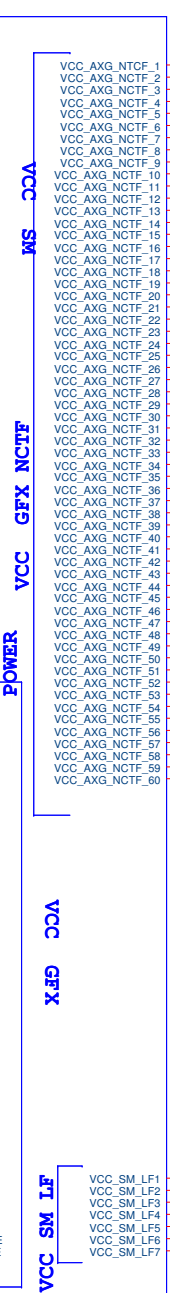
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- VCC_SM_2
- VCC_SM_3
- VCC_SM_4
- VCC_SM_5
- VCC_SM_6
- VCC_SM_7
- VCC_SM_8
- VCC_SM_9
- VCC_SM_10
- VCC_SM_11
- VCC_SM_12
- VCC_SM_13
- VCC_SM_14
- VCC_SM_15
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- VCC_SM_30
- VCC_SM_31
- VCC_SM_32
- VCC_SM_33
- VCC_SM_34
- VCC_SM_35

Could be NC for DDR2 Board.

- >BA36
- >BB24
- >BD16
- >BE24
- >BB21
- >AW16
- >AW15
- >AT18

- VCC_Axg_1
- VCC_Axg_2
- VCC_Axg_3
- VCC_Axg_4
- VCC_Axg_5
- VCC_Axg_6
- VCC_Axg_7
- VCC_Axg_8
- VCC_Axg_9
- VCC_Axg_10
- VCC_Axg_11
- VCC_Axg_12
- VCC_Axg_13
- VCC_Axg_14
- VCC_Axg_15
- VCC_Axg_16
- VCC_Axg_17
- VCC_Axg_18
- VCC_Axg_19
- VCC_Axg_20
- VCC_Axg_21
- VCC_Axg_22
- VCC_Axg_23
- VCC_Axg_24
- VCC_Axg_25
- VCC_Axg_26
- VCC_Axg_27
- VCC_Axg_28
- VCC_Axg_29
- VCC_Axg_30
- VCC_Axg_31
- VCC_Axg_32
- VCC_Axg_33
- VCC_Axg_34
- VCC_Axg_35
- VCC_Axg_36
- VCC_Axg_37
- VCC_Axg_38
- VCC_Axg_39
- VCC_Axg_41
- VCC_Axg_42

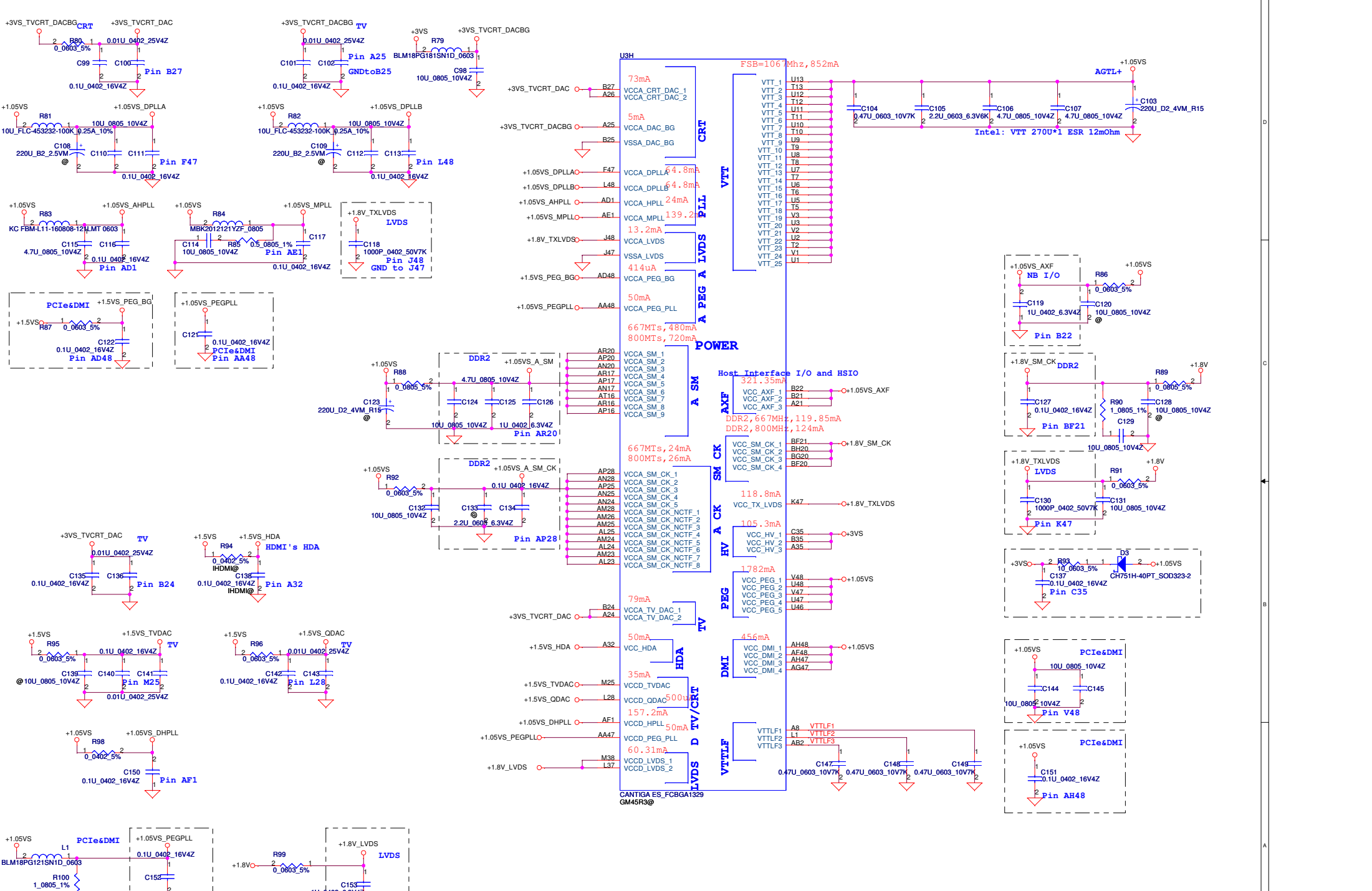
VCC_Axg_SENSE
VSS_Axg_SENSE



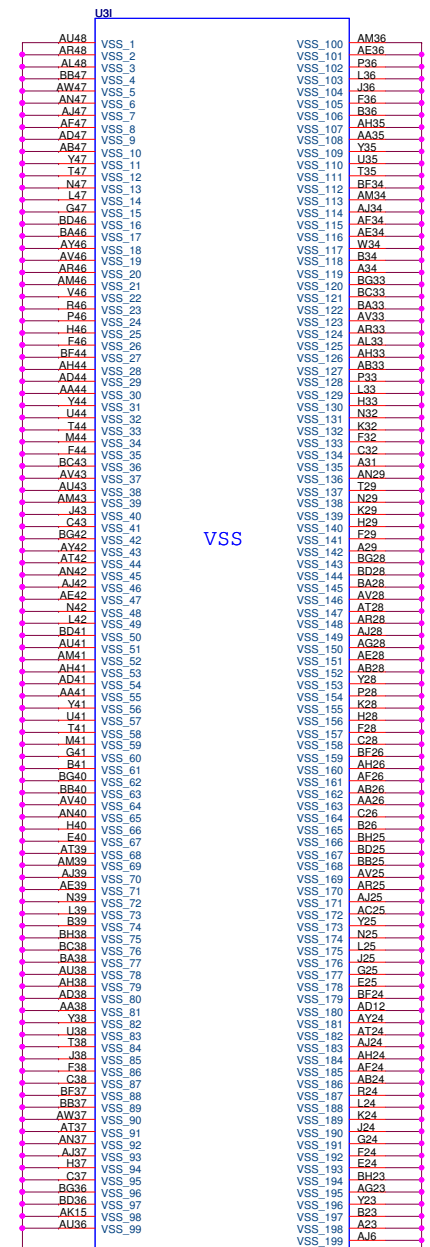
CANTIGA ES_FCBGA1329
GM45R3@

CANTIGA ES_FCBGA1329
GM45R3@

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Date: Monday, August 10, 2009				Sheet 12 of 41	

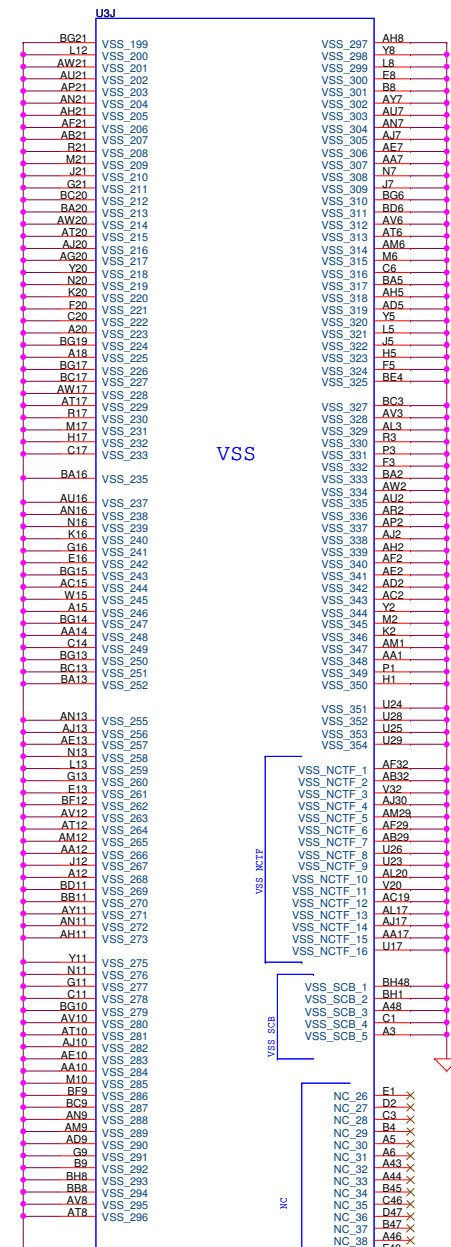


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Issued Date	2009/07/28	Deciphered Date	2010/07/28	Crestline GMCH (6/7)-VCC	
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Date:	Monday, August 10, 2009	Sheet:	13	of	41



VSS

CANTIGA ES_FCBGA1329
GM45R3@



VSS

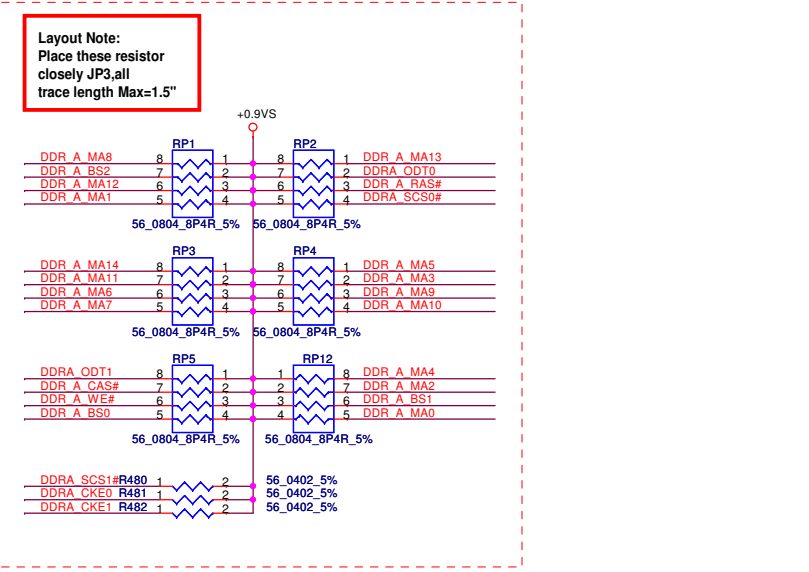
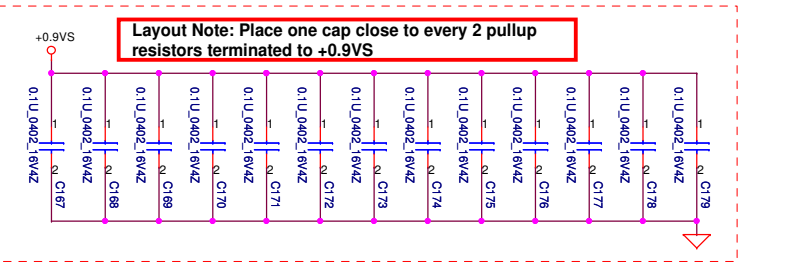
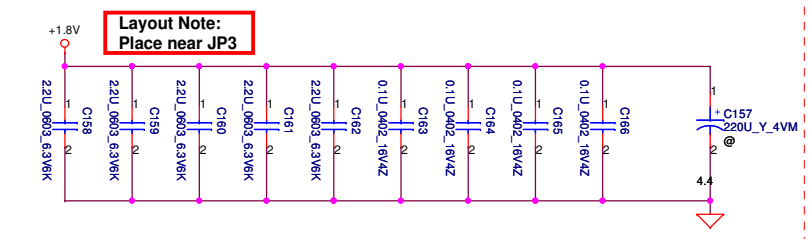
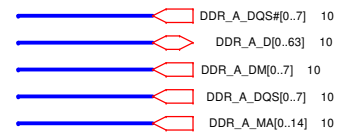
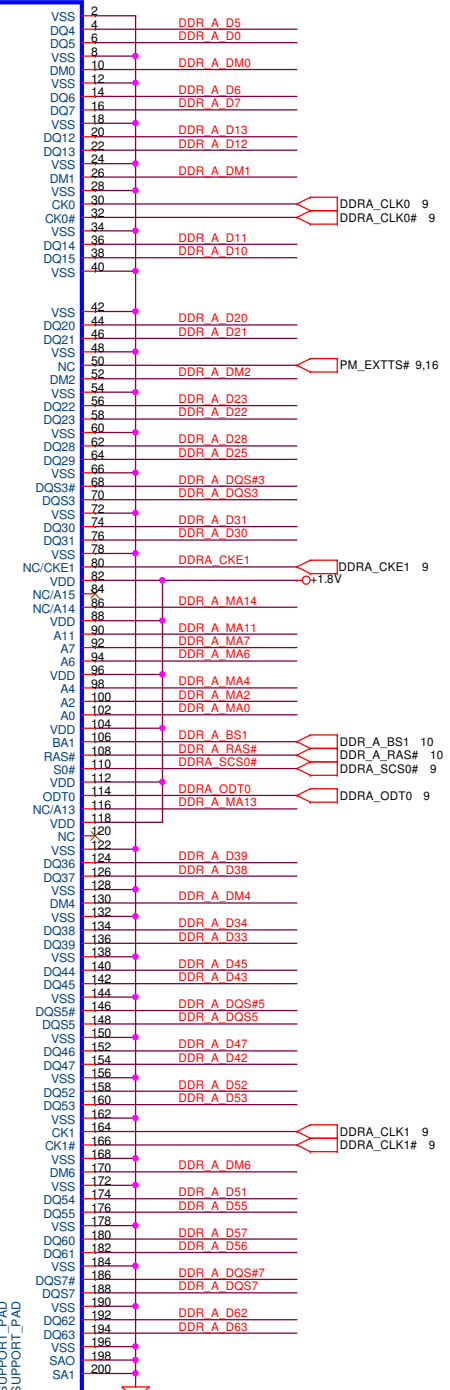
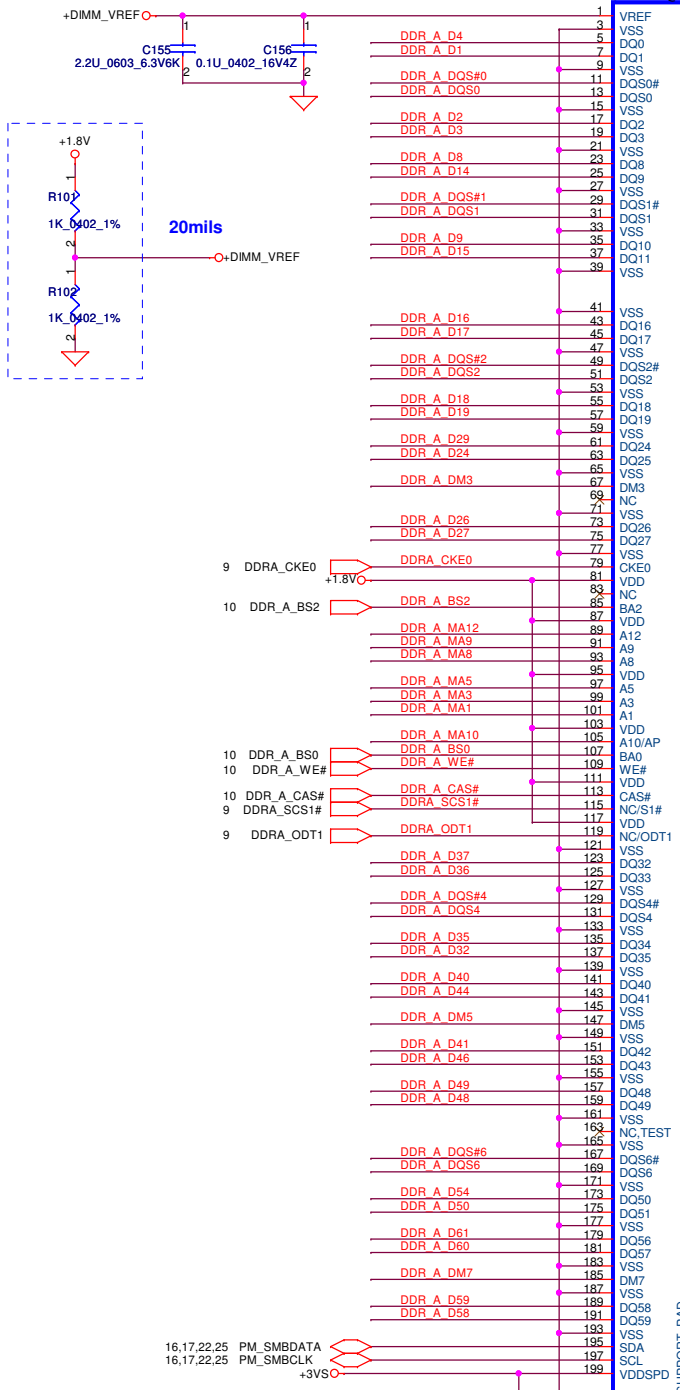
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VSS_SCB

NC

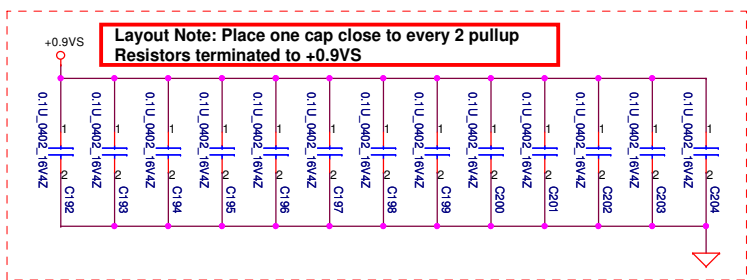
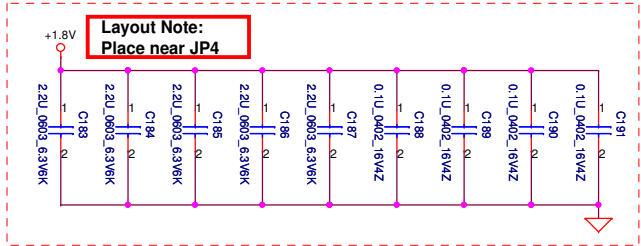
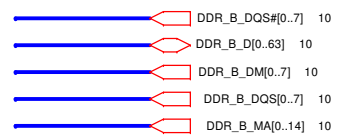
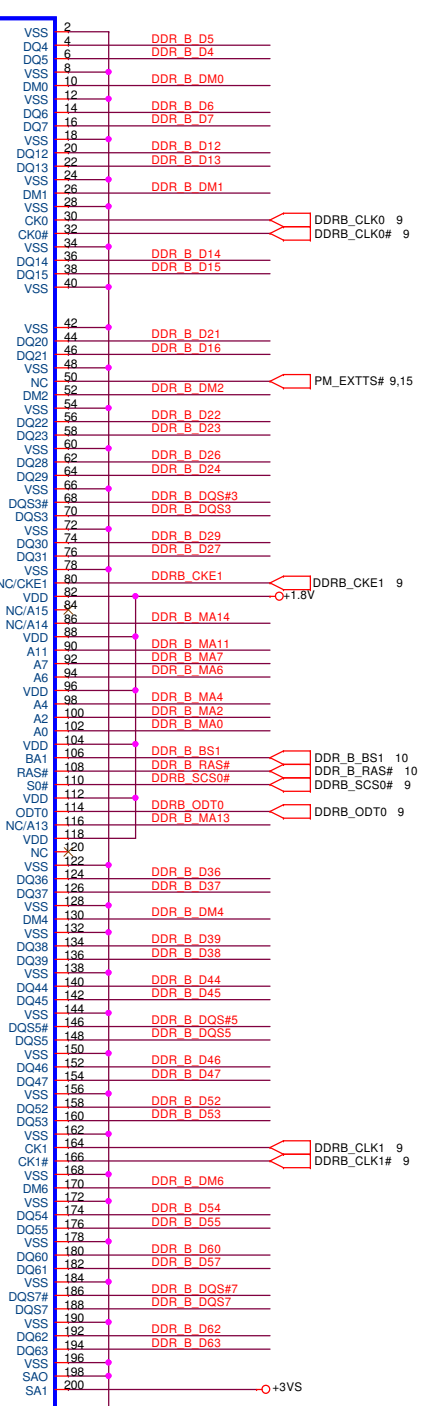
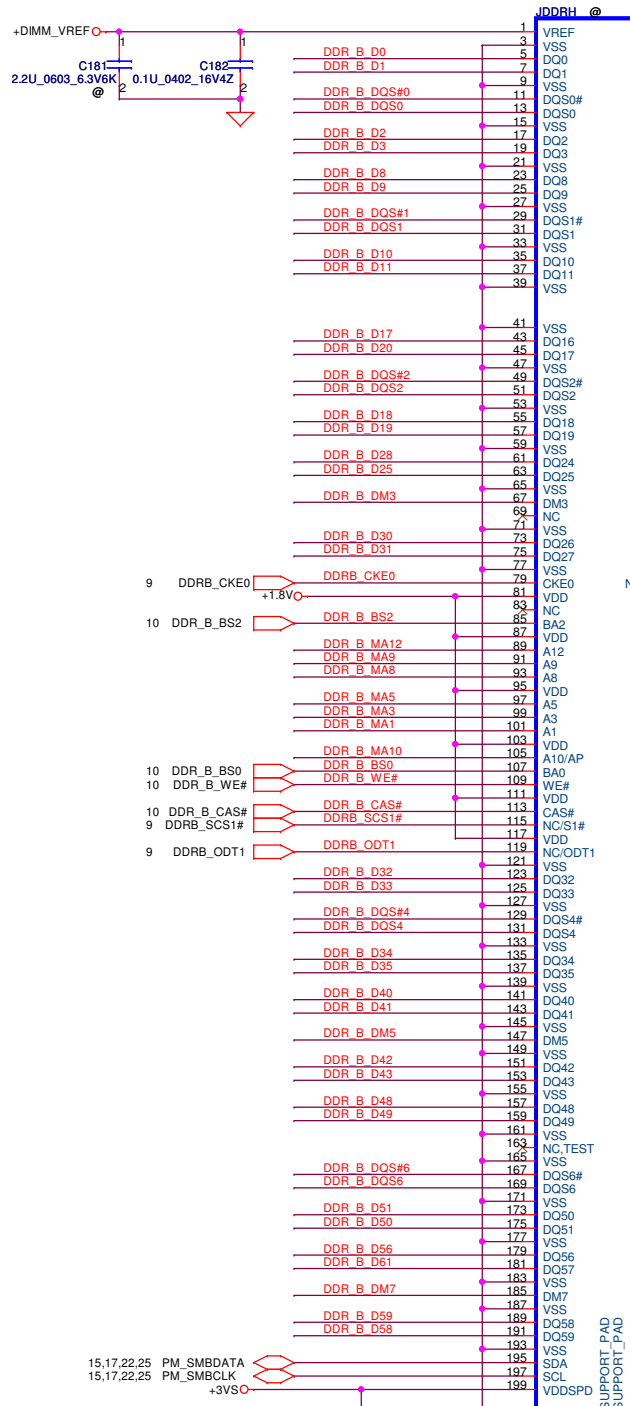
CANTIGA ES_FCBGA1329
GM45R3@

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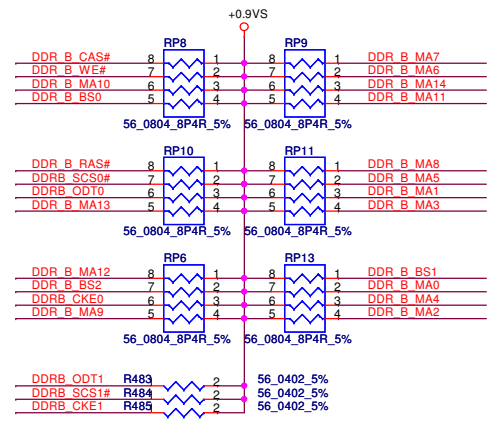


SO-DIMM A REVERSE Top side

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Issued Date	2009/07/28	Deciphered Date	2010/07/28	DDR II-SODIMMO	
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Layout Note:
Place these resistor closely JP4,all trace length Max=1.5"



**SO-DIMM B
STANDARD
Bottom side**

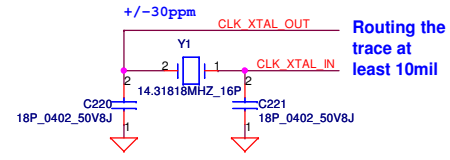
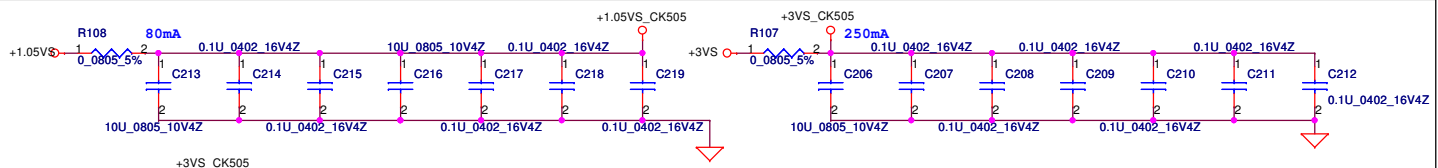


201_202
FOX_AS0A426-MAR02E

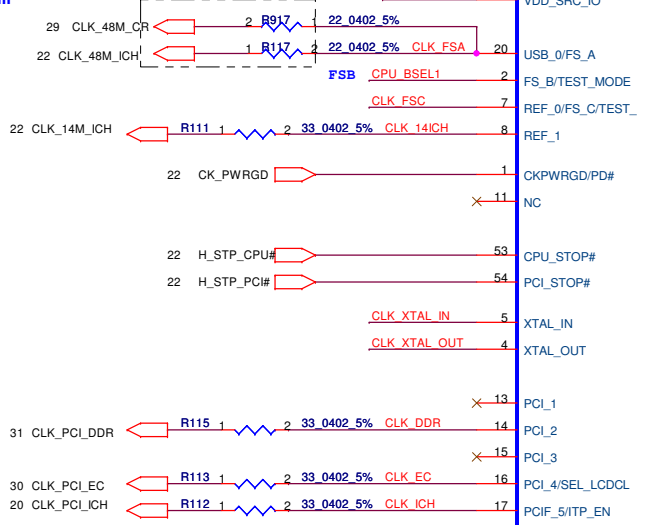
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Issued Date	2009/07/28	Deciphered Date	2010/07/28
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Compal Electronics, Inc.			
Title DDR II-SODIMM1			
Size	Document Number	Rev	
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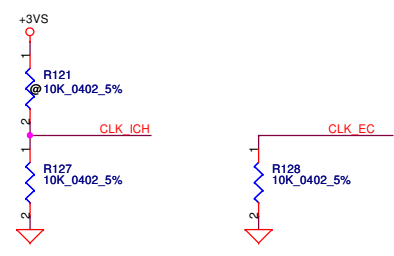
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						



place 22ohm for damping resistor when loading is two devices

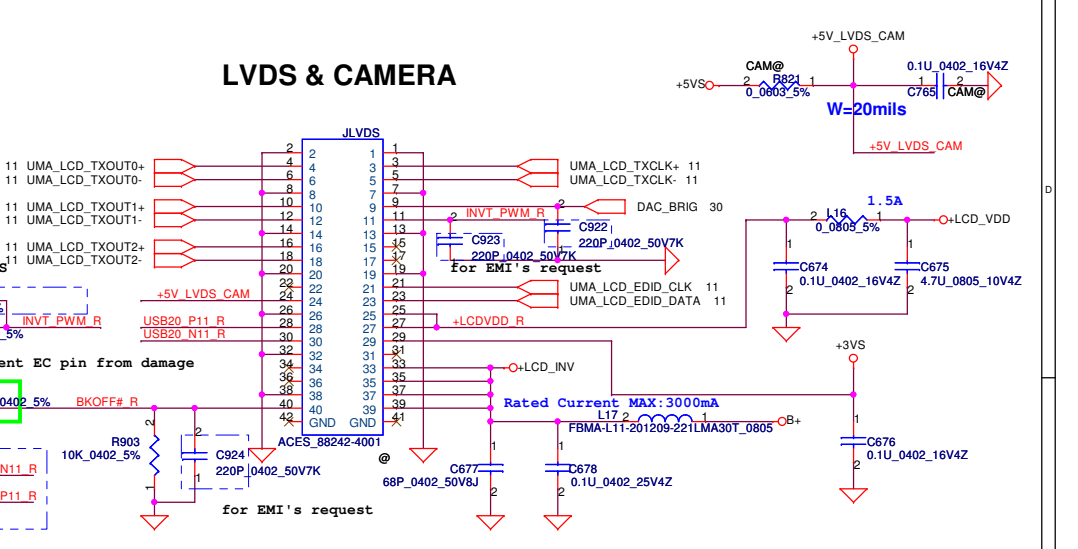
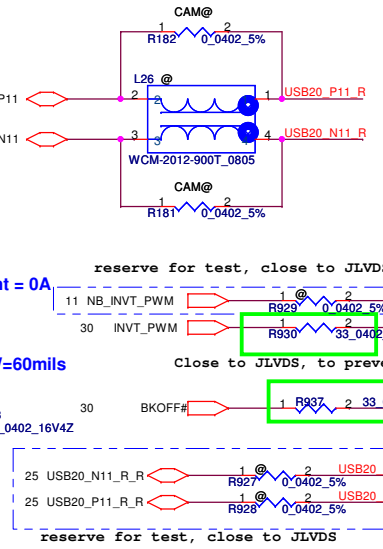
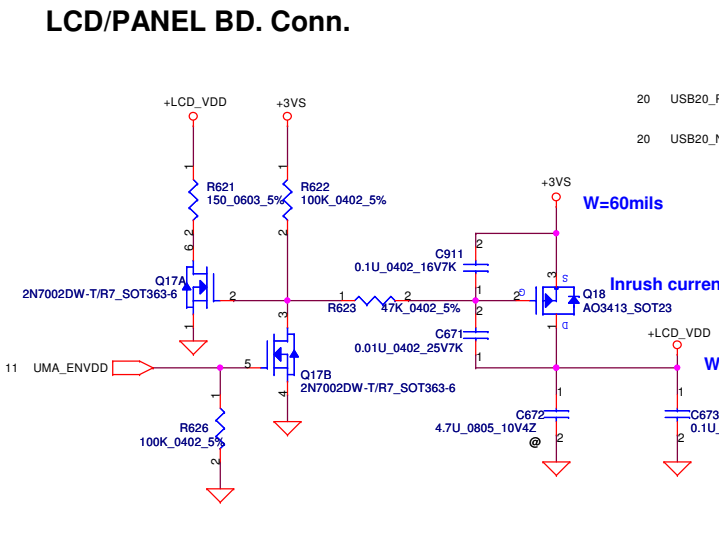


CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1 (UMA) 1 = Enable SRC0 & 27MHz (DIS)

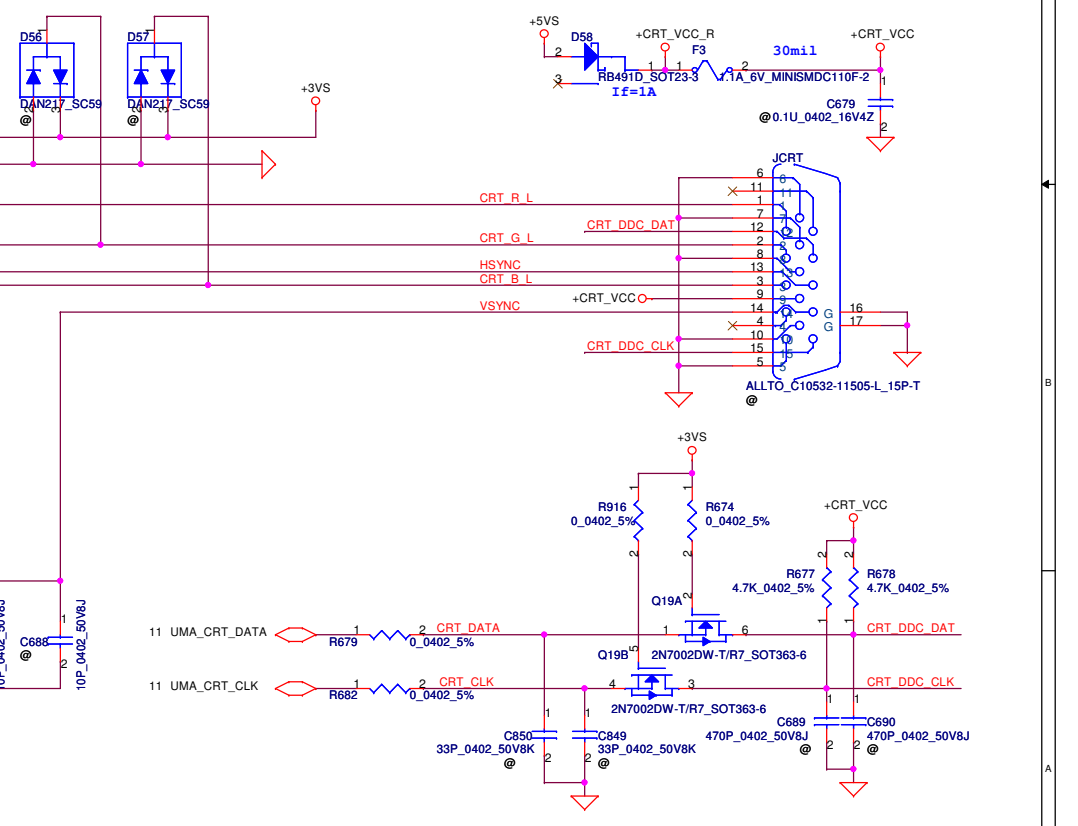
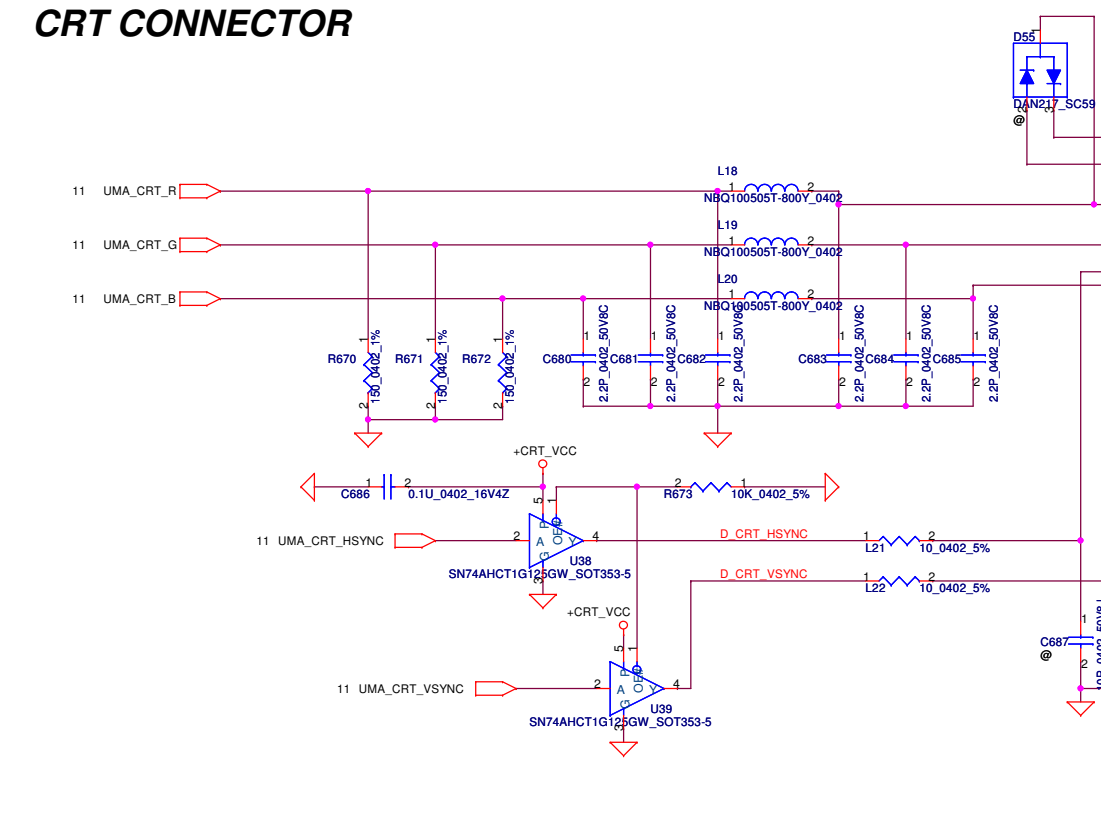


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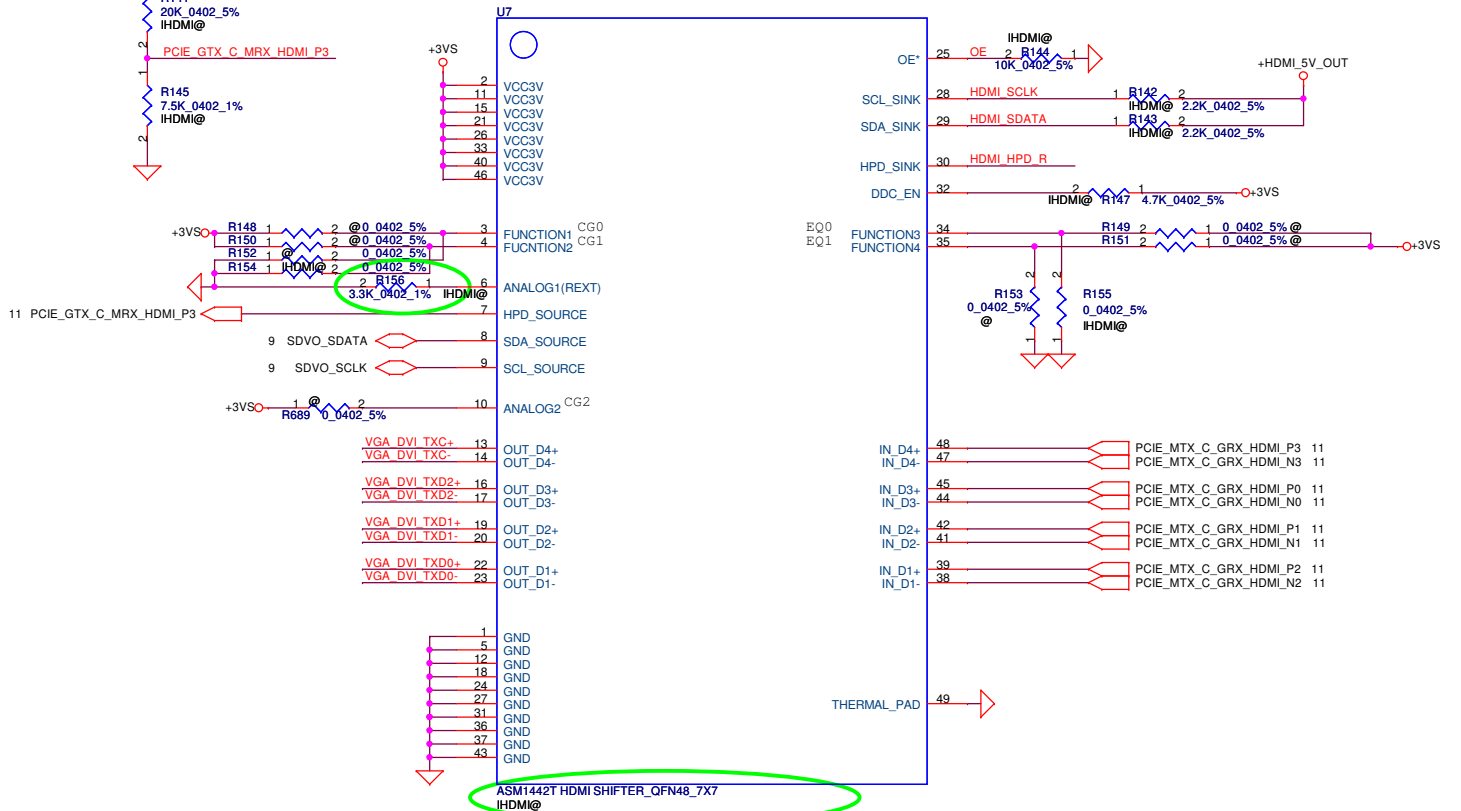
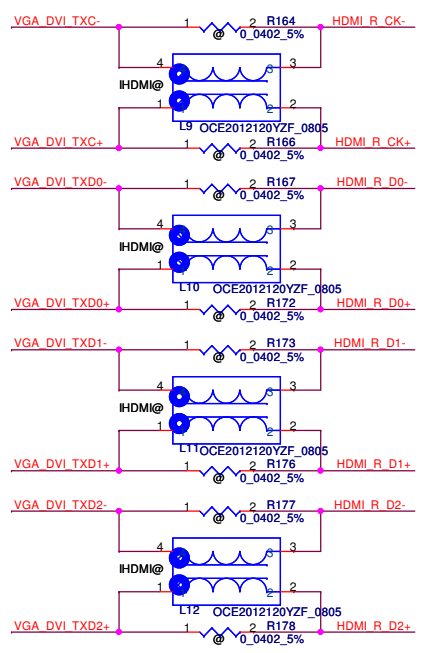
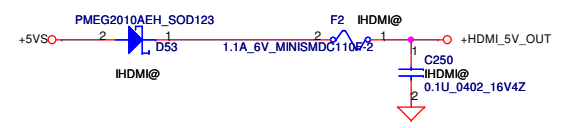
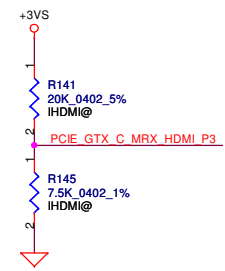
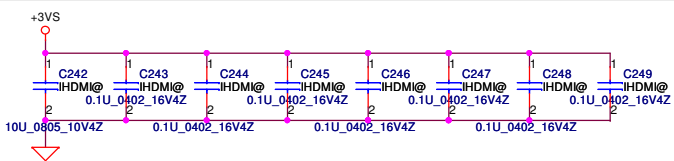
LCD/PANEL BD. Conn.



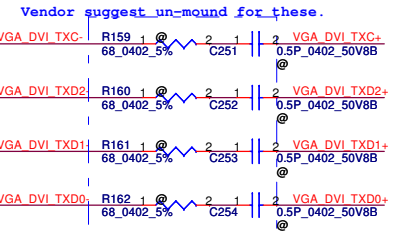
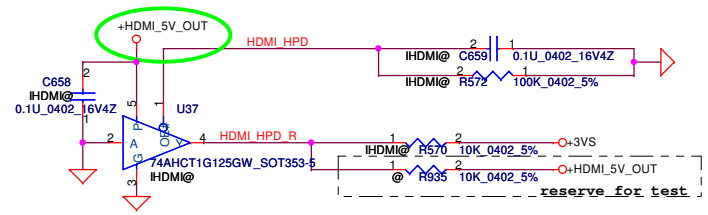
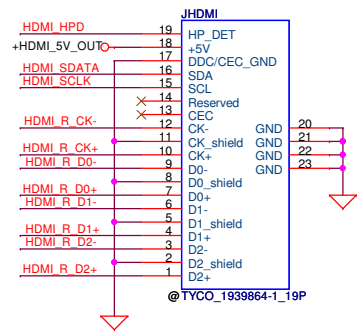
CRT CONNECTOR



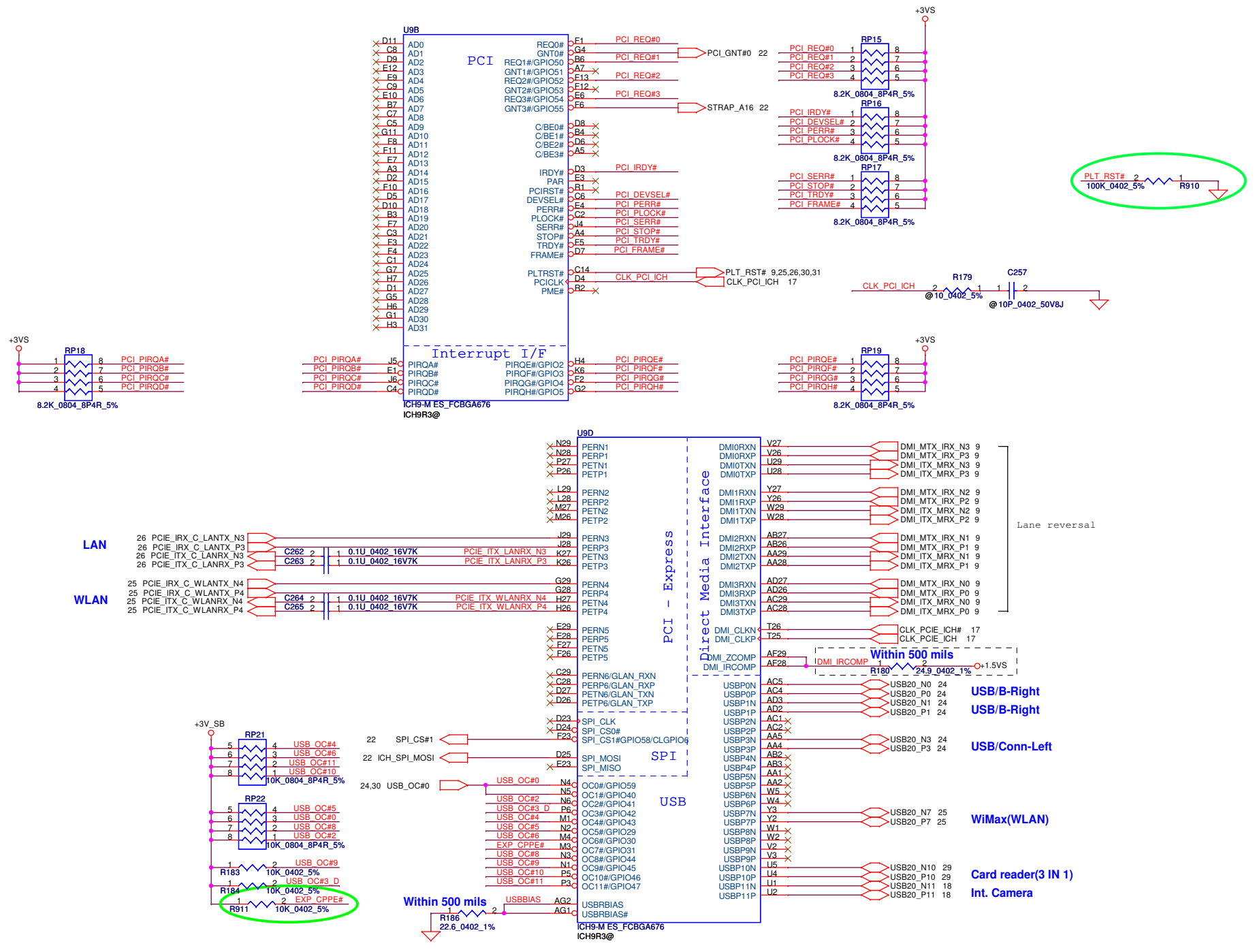
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Size	Document Number	Date		Sheet	Rev
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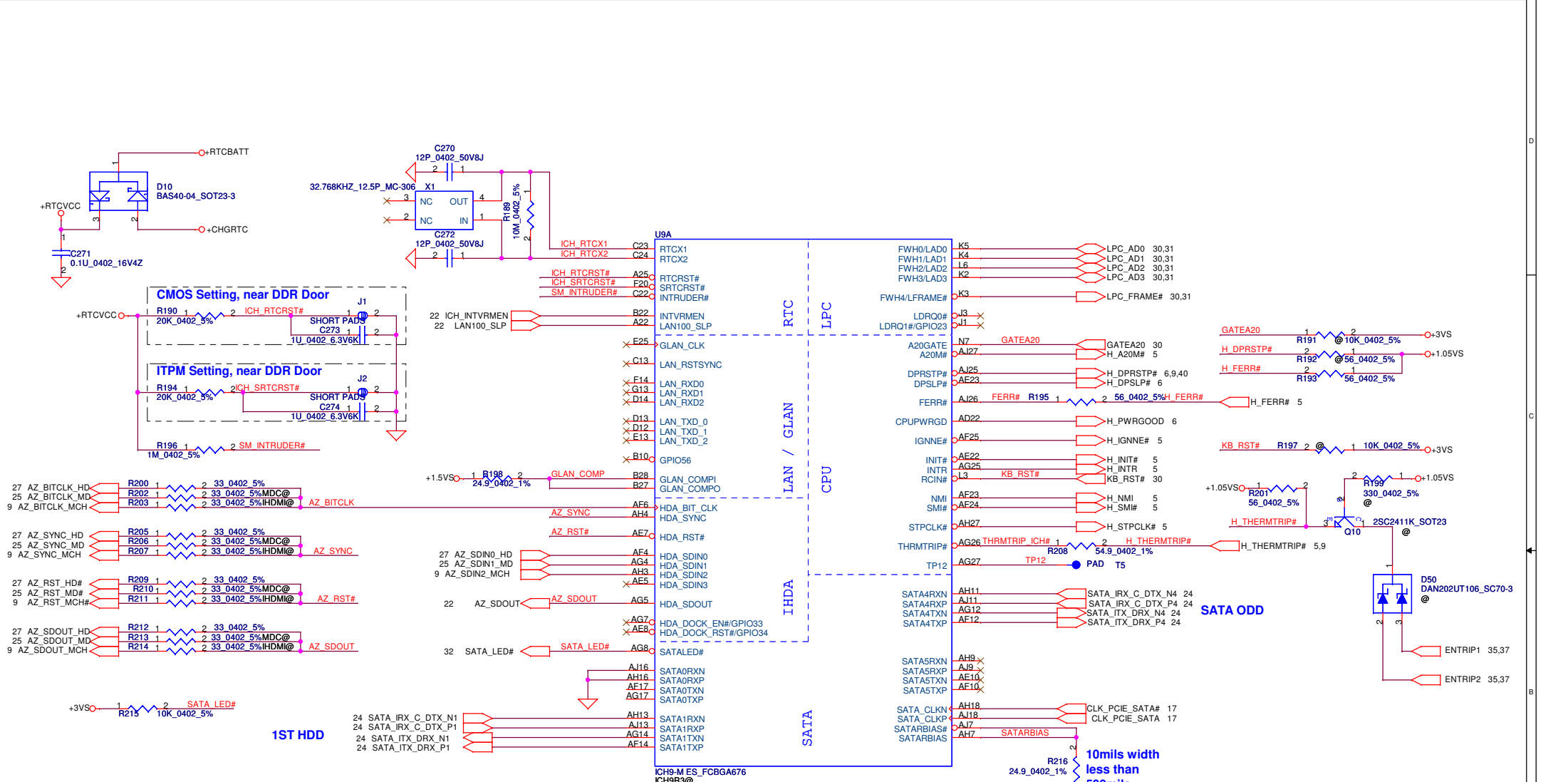
HDMI Connector



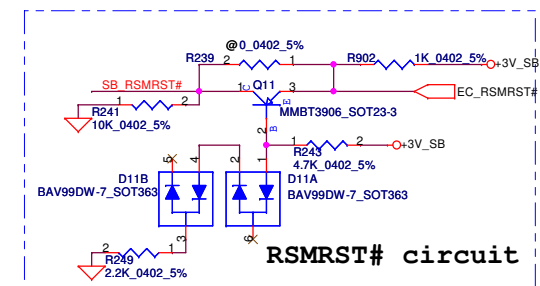
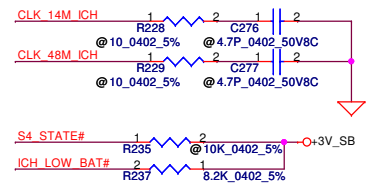
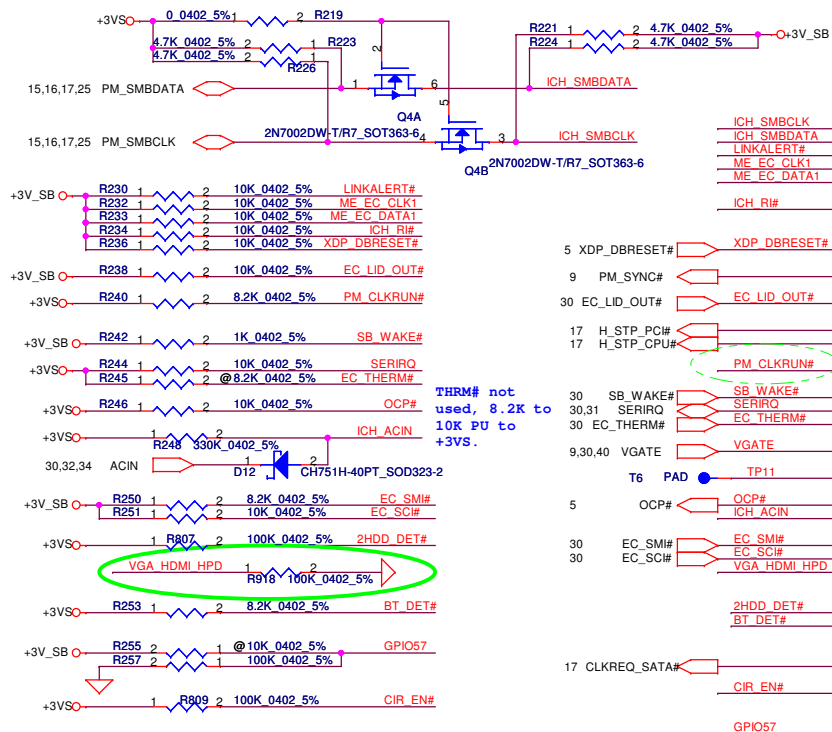
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				Document Number	
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				Title	
				ICH9M(1/4)-PCI	
				Size	
				NWAA LA5821P M/B	
				Rev	
				1.0	



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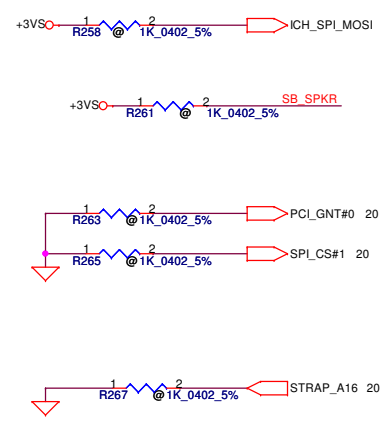


ITPM Physical Presence

CLGPI05	Assert = iTPM Physical Presence Enable De-assert = iTPM disable **Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin



Internal TPM Strap (Internal pull-down)

SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*
----------	---

No Reboot Strap (Internal pull-up)

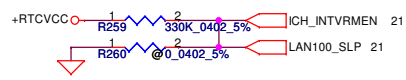
SB_SPKR	Low= "Default" High= "No Reboot"
---------	-------------------------------------

Boot BIOS Strap (Internal pull-up)

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)
-----------	--



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
--------------	---

Flash Descriptor Security Override Strap

GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)
--------	--

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
----------------	---

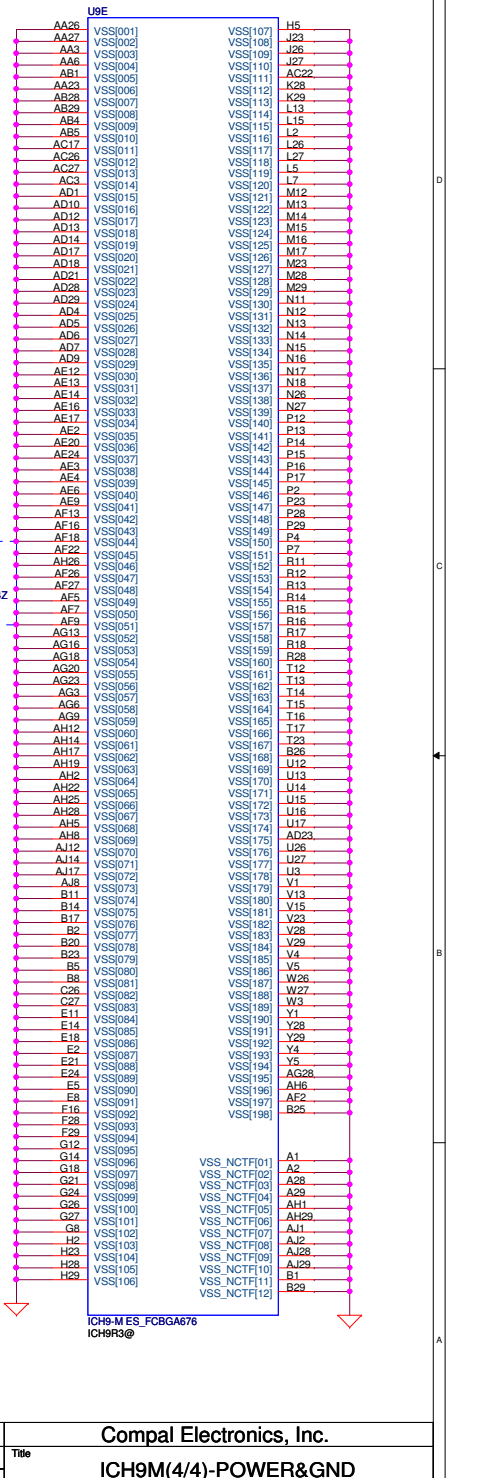
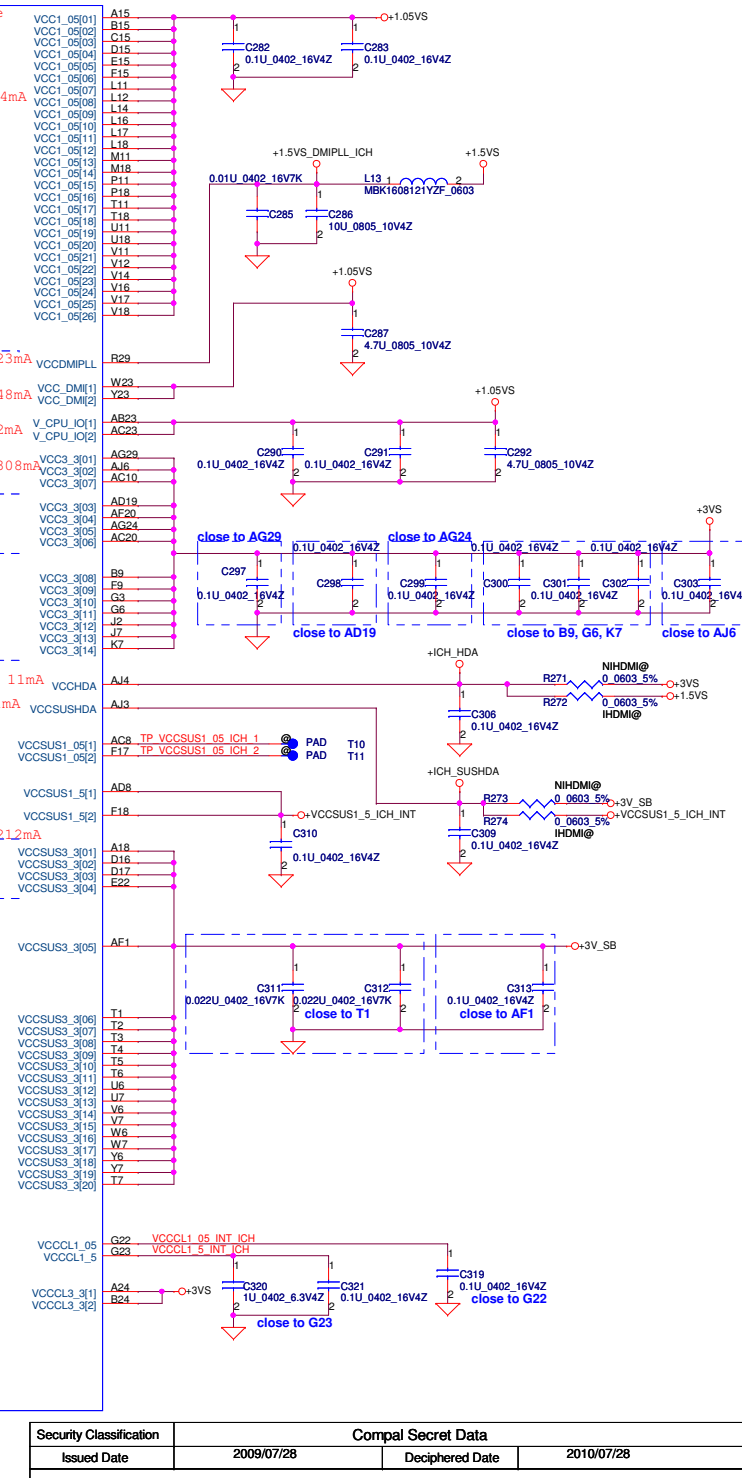
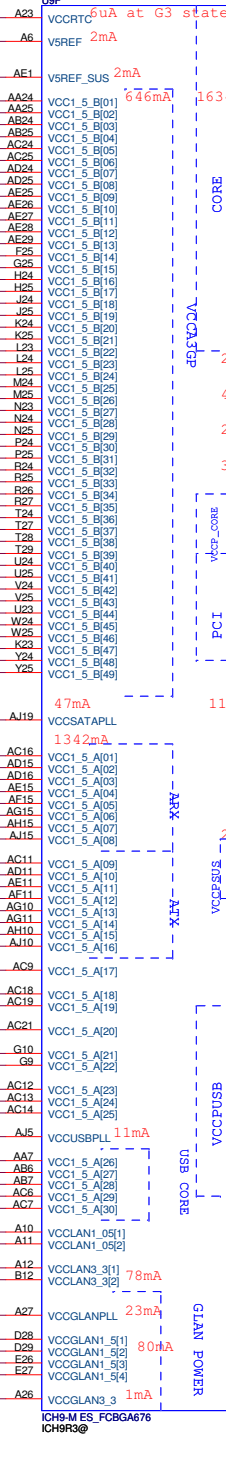
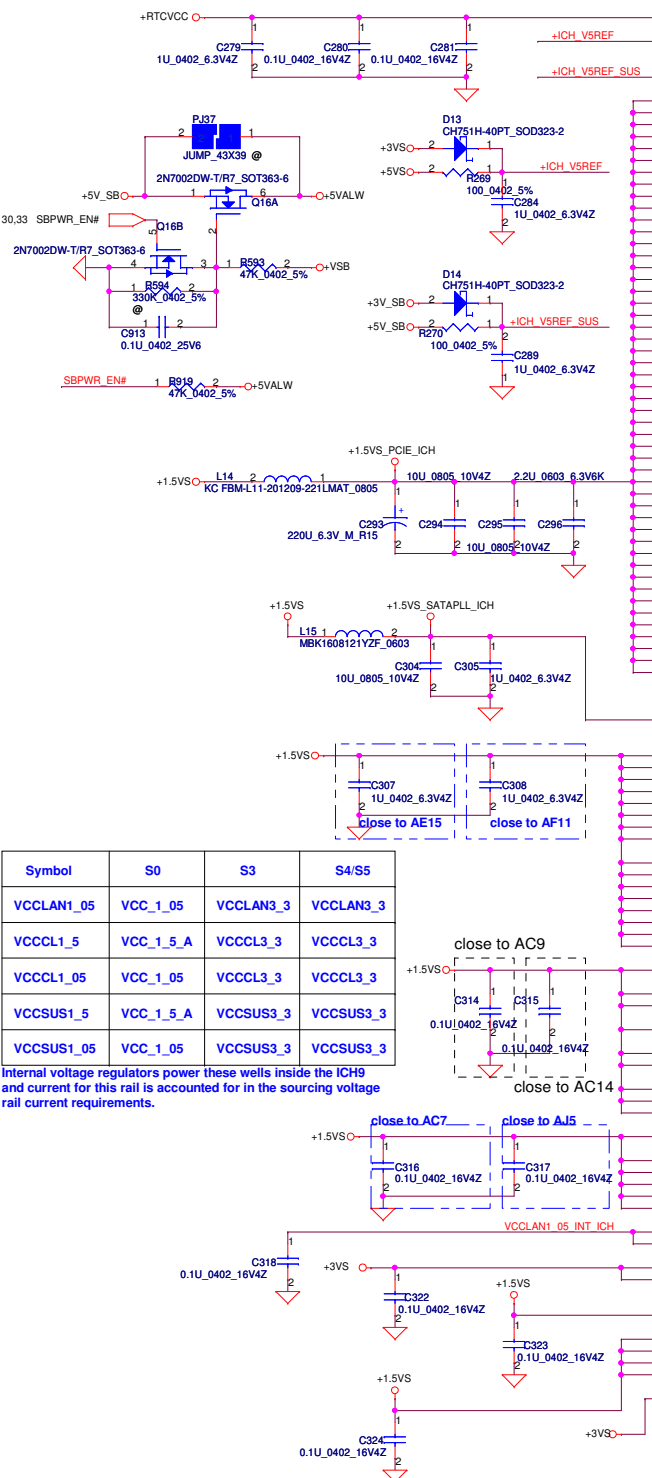
DMI Termination Voltage

GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)
--------	---

XOR Chain Entrance Strap

ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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Size	Document Number	Rev		1.0	
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				Title	
				ICH9M(3/4)-USB,GPIO,PCIE	
				NWAA LA5821P M/B	



Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

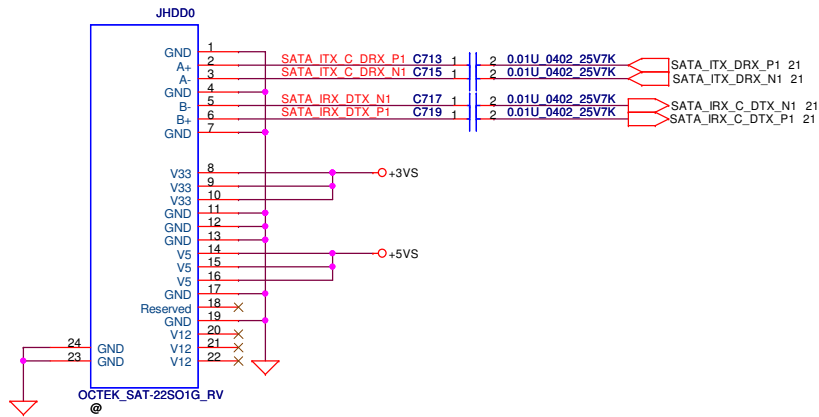
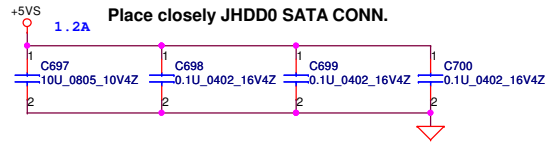
Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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Compal Secret Data			

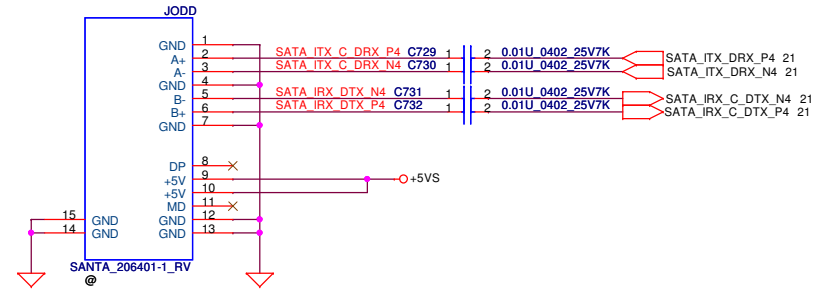
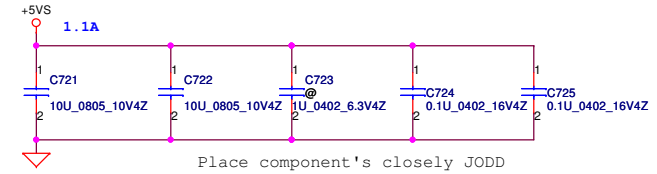
Compal Electronics, Inc.	
Title: ICH9M(4/4)-POWER&GND	
Size: Document Number	Rev: 1.0
Date: Monday, August 10, 2009 1:22:23 PM	
Sheet: 23 of 41	

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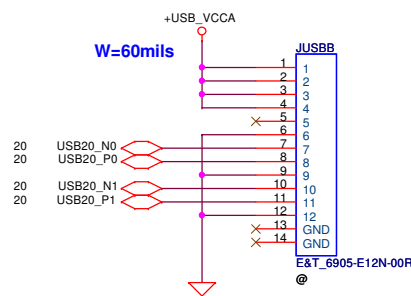
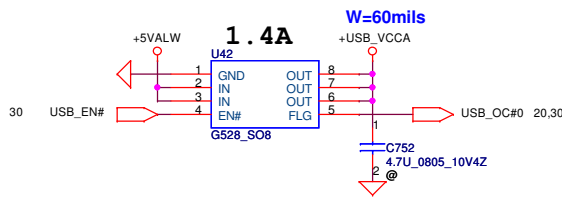
SATA HDD Conn.



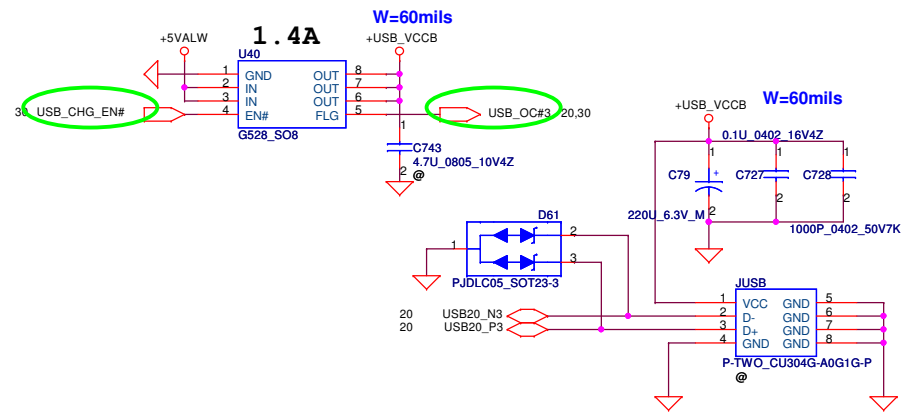
SATA ODD Conn



USB Board Conn

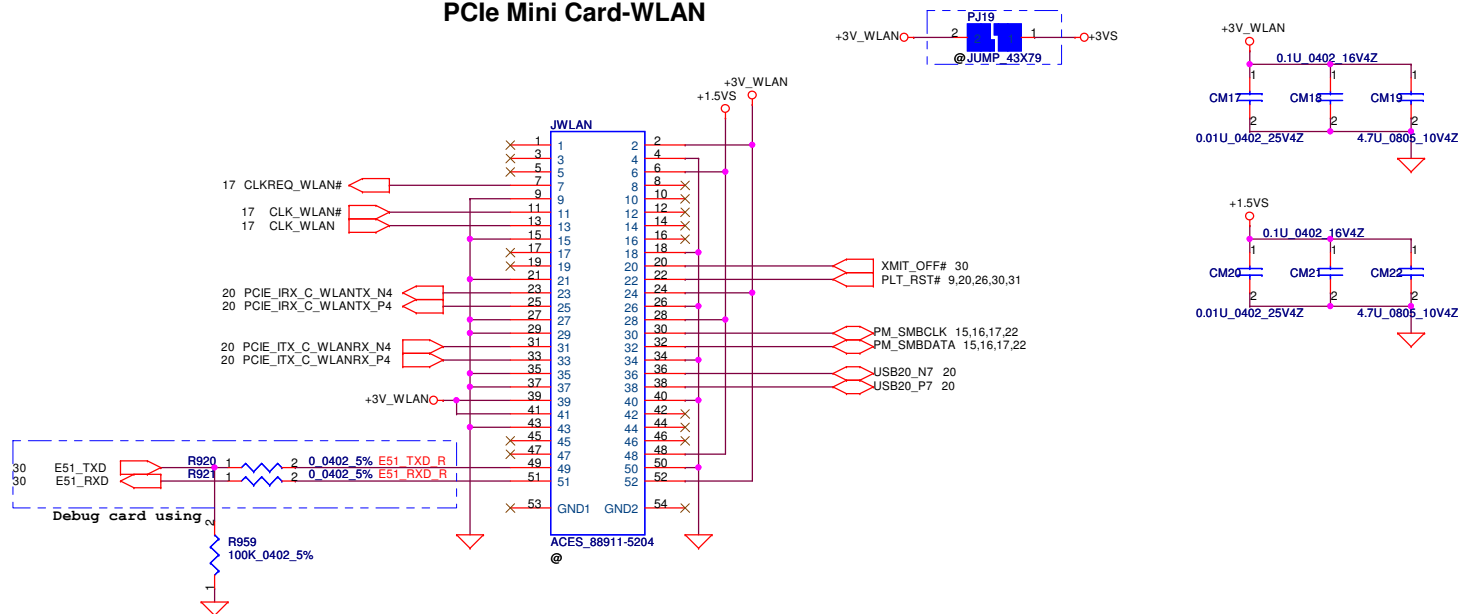


USB Left Conn

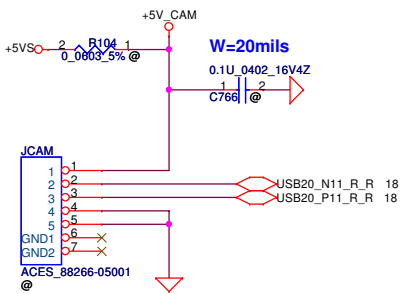


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Issued Date	2009/07/28	Deciphered Date	2010/07/28	SATA-HDD/ODD& USB	
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				NBWAA LA5821P M/B	
Date:	Thursday, August 06, 2009	Sheet	24	of	41

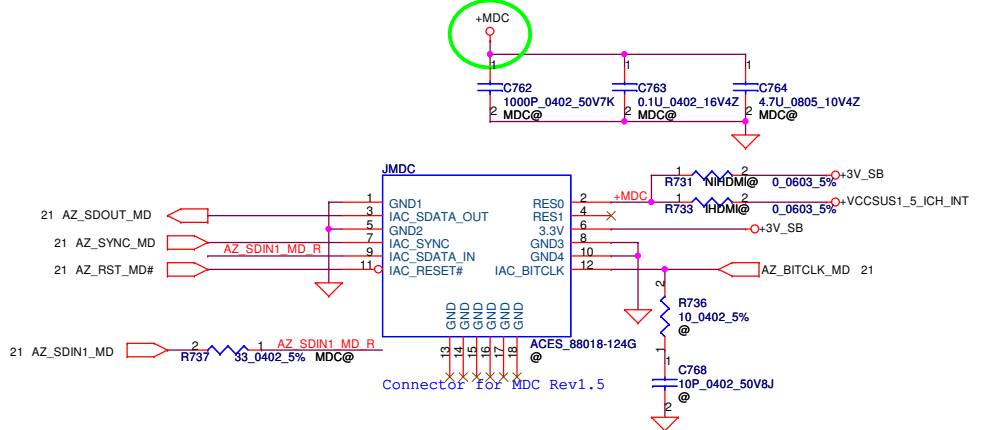
PCIe Mini Card-WLAN



Int. Camera

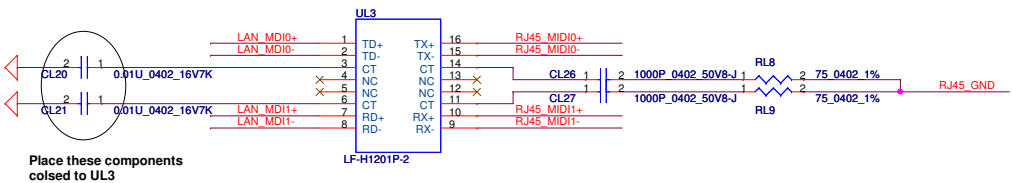
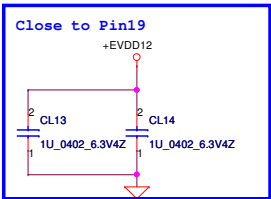
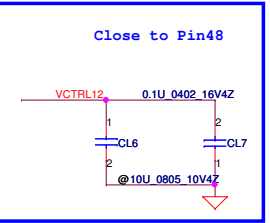
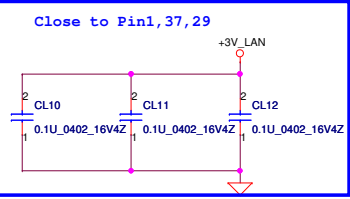
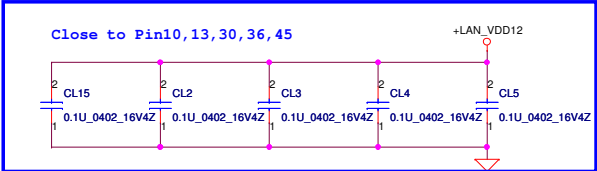
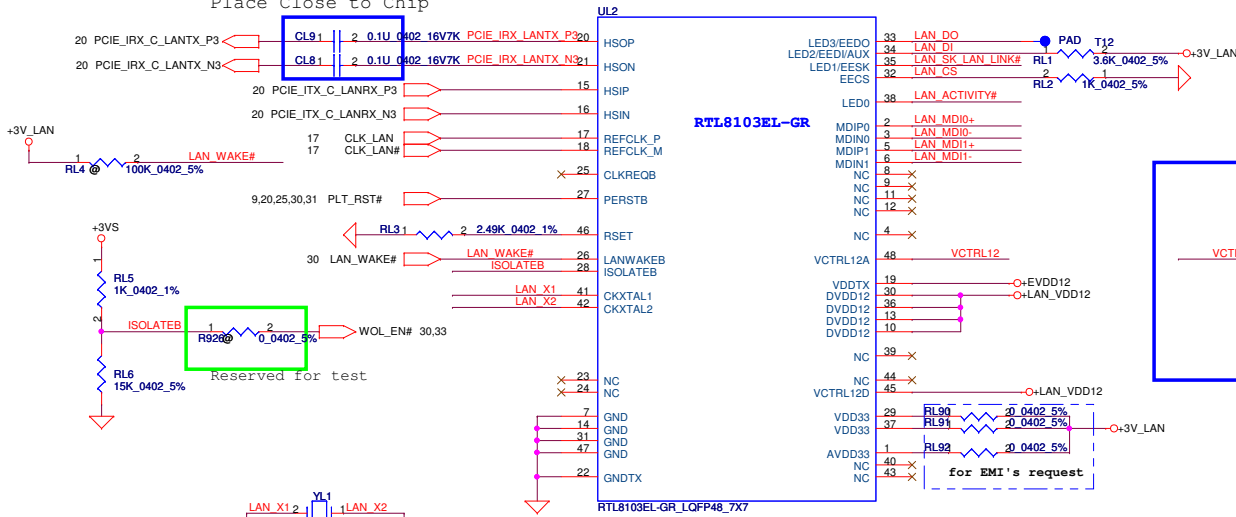


MDC 1.5 Conn.

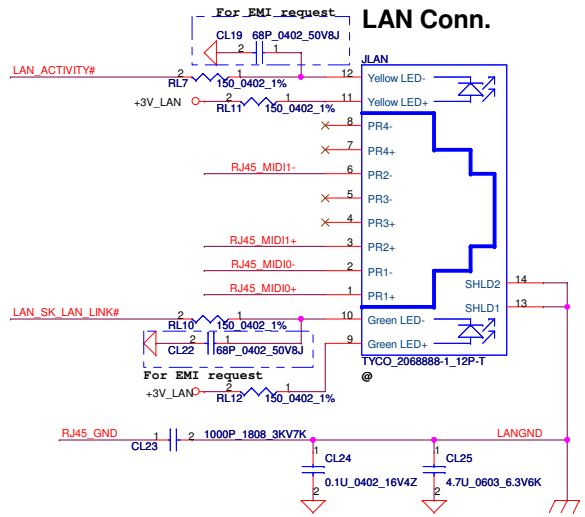


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				NBWAA LA5821P M/B	
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Place Close to Chip

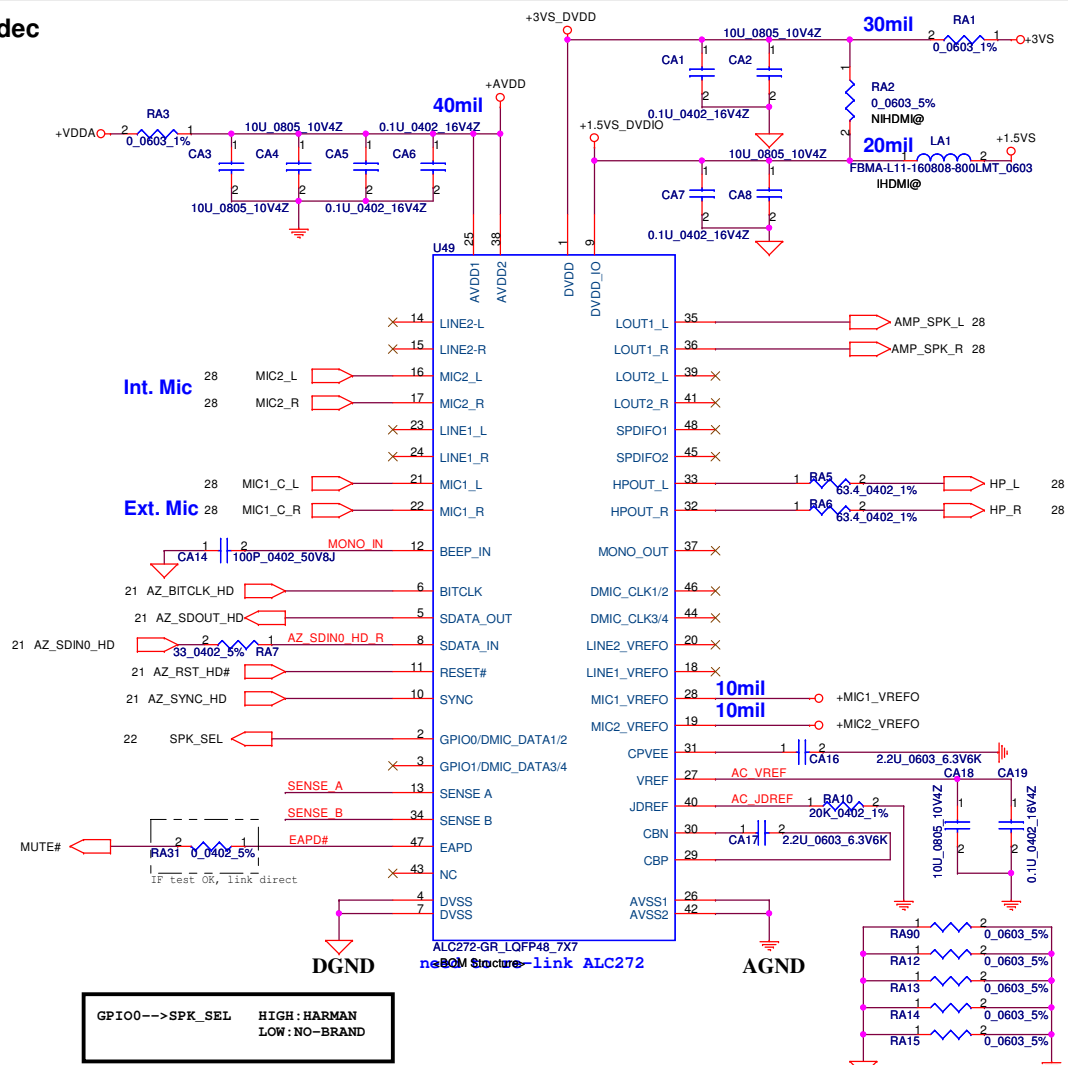


Place these components close to UL3

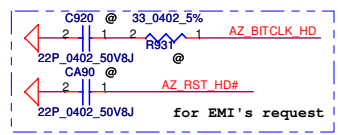
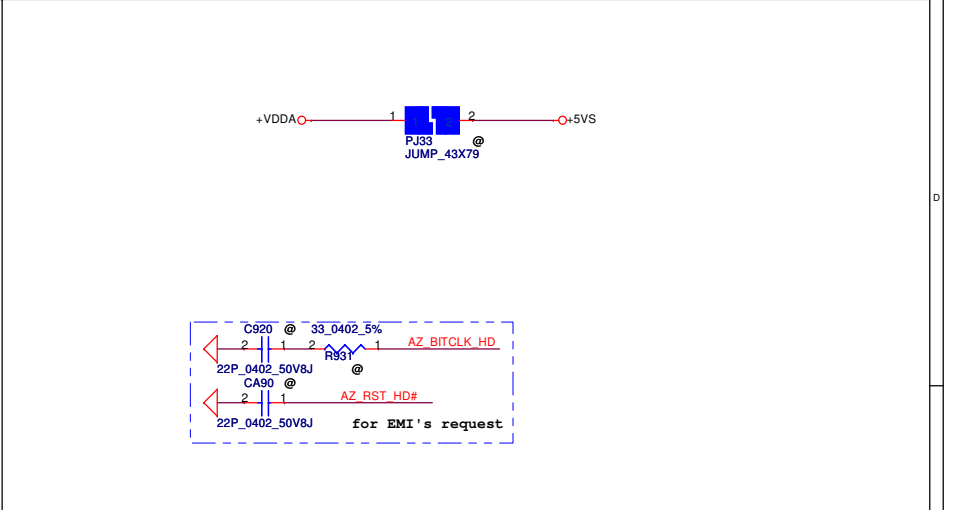


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Issued Date	2009/07/28	Deciphered Date	2010/07/28	RTL8103EL 10/100 LAN	
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				Custom	NBWAALAS821P M/B
				Date:	Thursday, August 06, 2009
				Sheet	26 of 41
				Rev	1.0

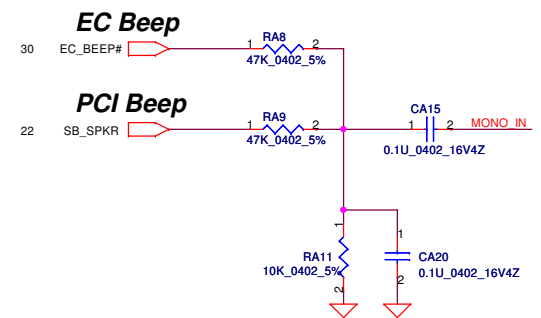
Codec



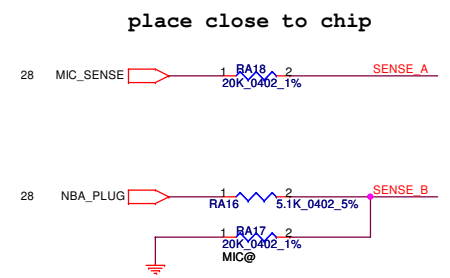
GPIO0-->SPK_SEL HIGH: HARMAN LOW: NO-BRAND



Beep sound

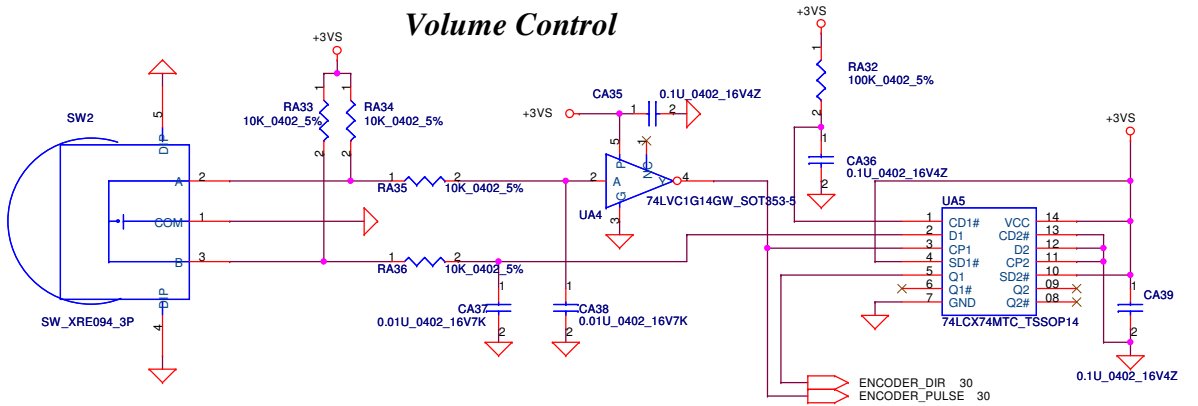
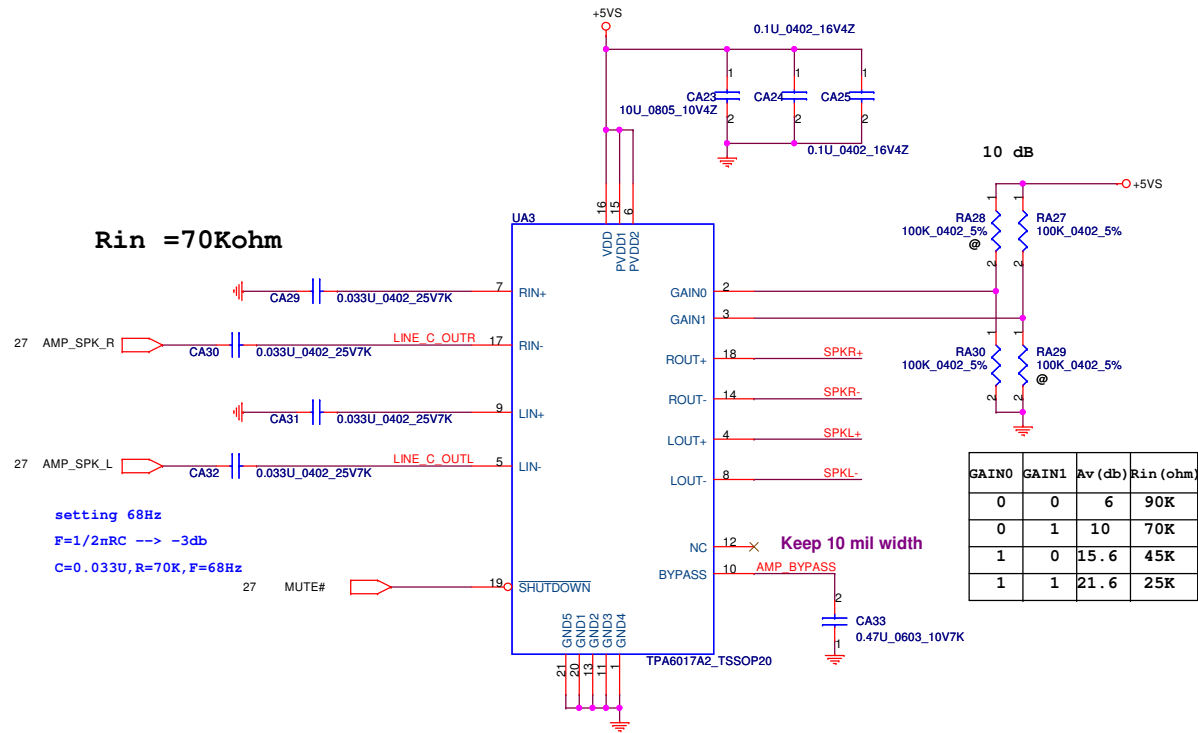


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	/
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	/
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	/
	5.1K	PORT-I (PIN 32, 33)	Headphone out

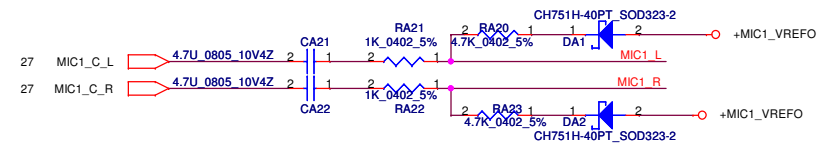


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Date:	Monday, August 10, 2009	Sheet	27	of	41

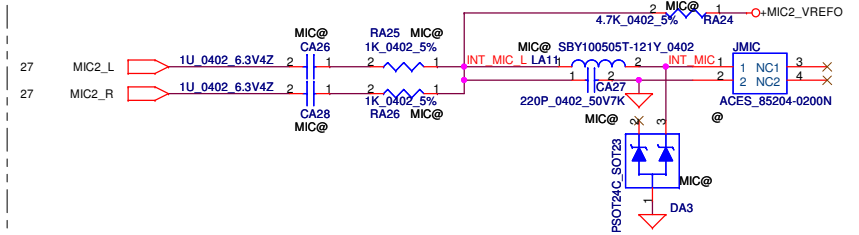
TPA6017 Medium Range Amplifier



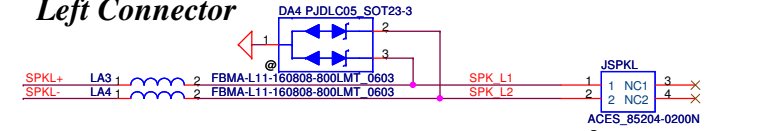
Ext. Mic



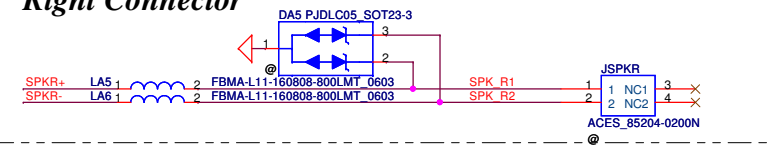
Int. Mic



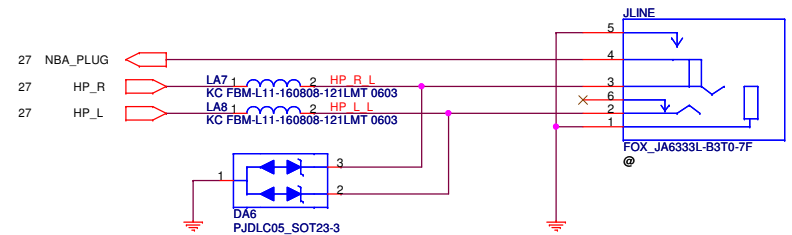
Left Connector



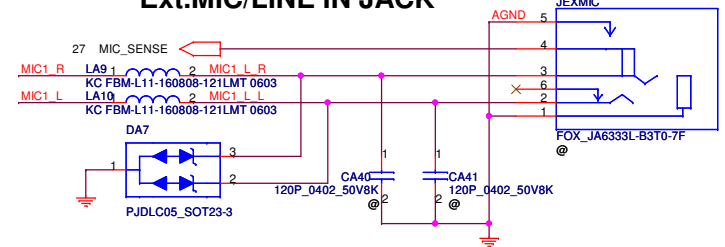
Right Connector



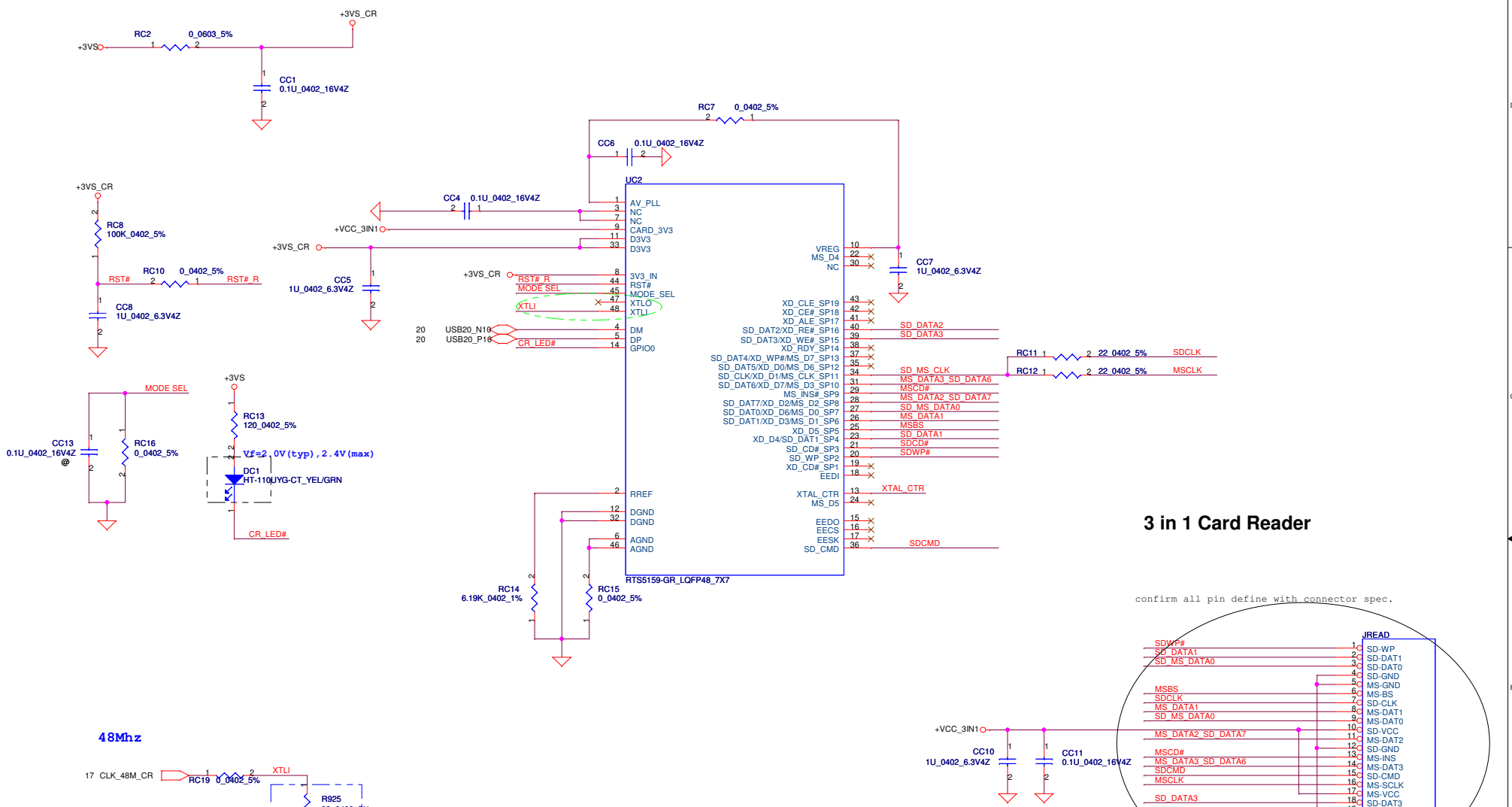
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

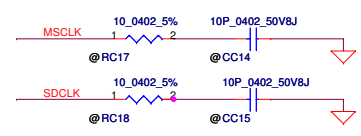
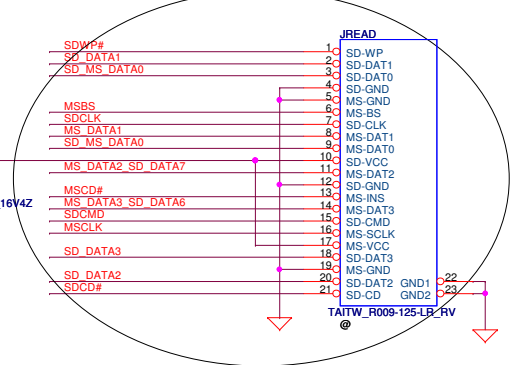


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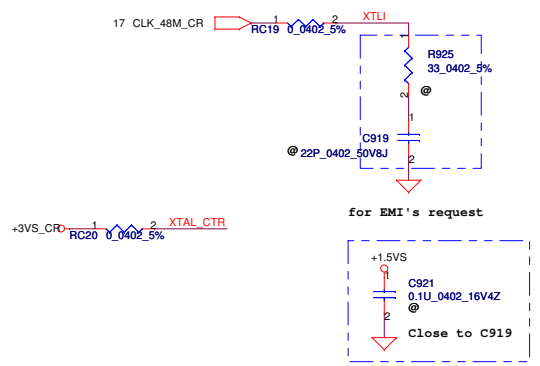


3 in 1 Card Reader

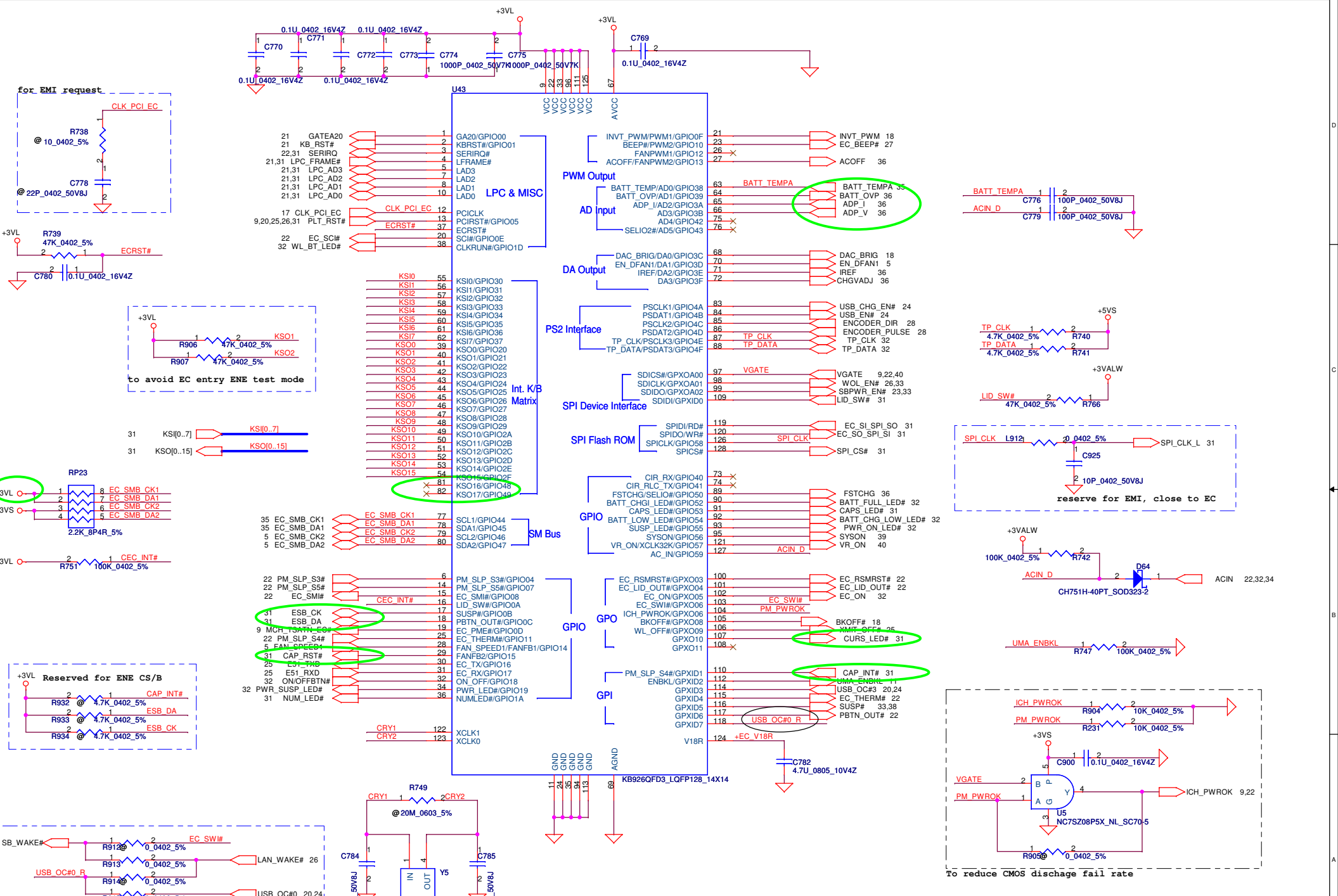
confirm all pin define with connector spec.



48Mhz



R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	



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				Document Number	1.0
				Date	Monday, August 10, 2009
				Sheet	30 of 41

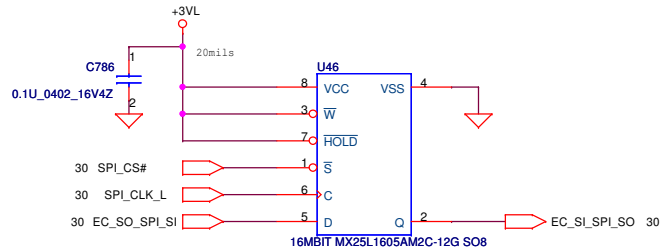
Compal Electronics, Inc.

ENE-KB926 RevD3

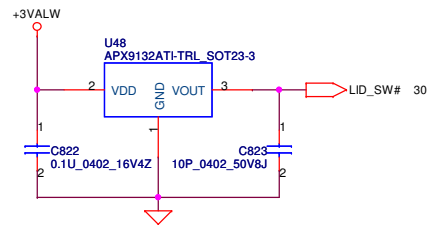
NBWAA LA5821P M/B

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SPI Flash (16Mb*1)

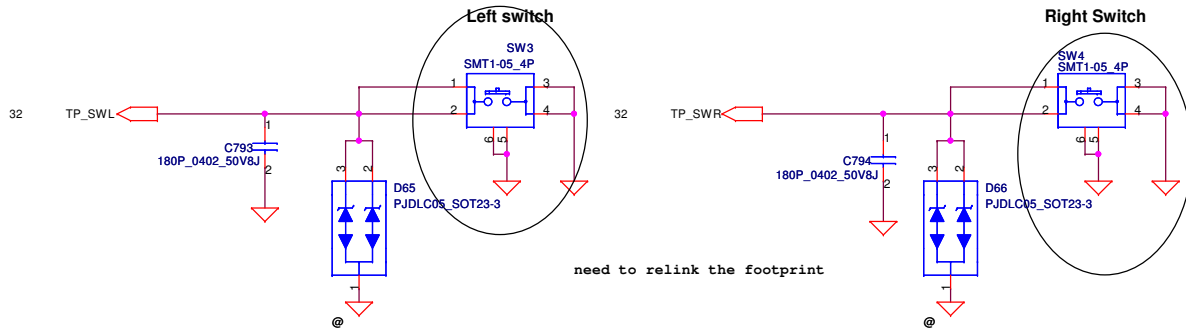
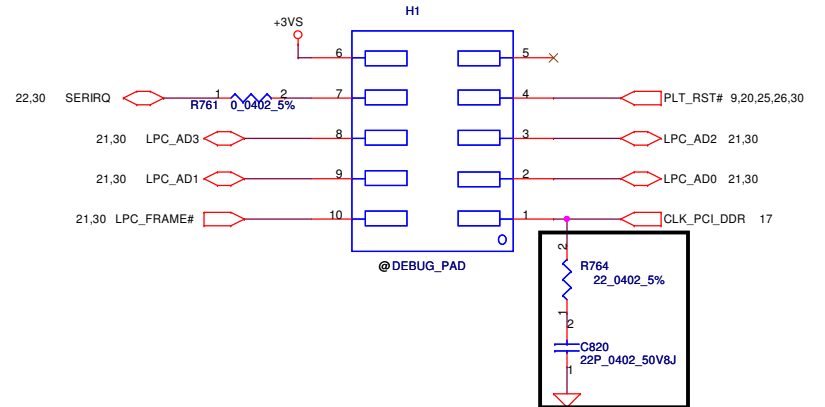


Lid SW



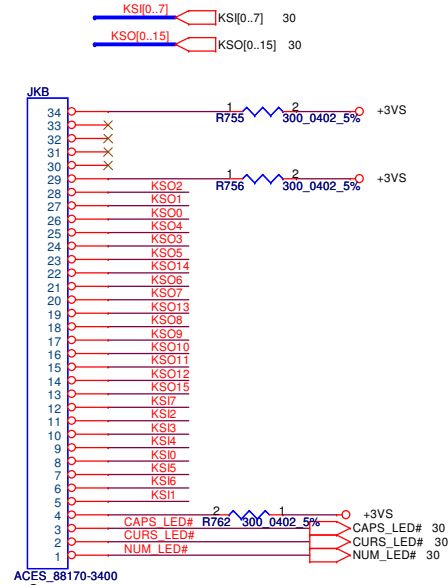
LPC Debug Port

Please place the PAD under DDR DIMM.



need to relink the footprint

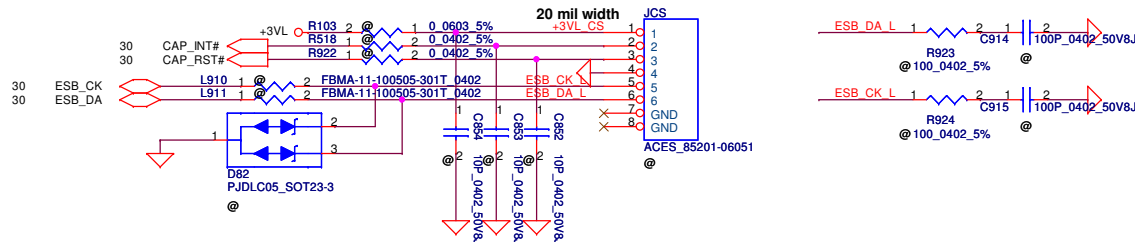
KEYBOARD CONN.



please close to JKB

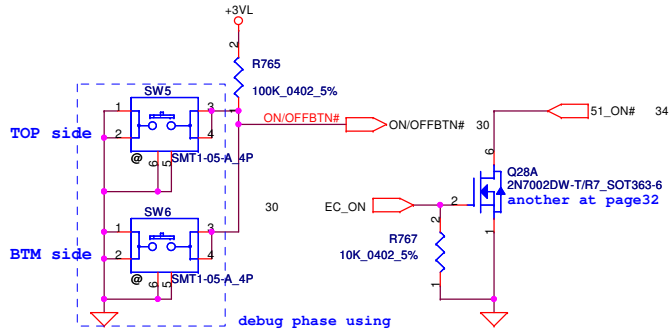
KSO2	C789	1	2	100P_0402_50V8J
KSO1	C790	1	2	100P_0402_50V8J
KSO0	C791	1	2	100P_0402_50V8J
KSO4	C792	1	2	100P_0402_50V8J
KSO3	C795	1	2	100P_0402_50V8J
KSO5	C796	1	2	100P_0402_50V8J
KSO14	C796	1	2	100P_0402_50V8J
KSO6	C797	1	2	100P_0402_50V8J
KSO8	C798	1	2	100P_0402_50V8J
KSO7	C799	1	2	100P_0402_50V8J
KSO13	C799	1	2	100P_0402_50V8J
KSO8	C800	1	2	100P_0402_50V8J
KSO8	C801	1	2	100P_0402_50V8J
KSO9	C802	1	2	100P_0402_50V8J
KSO10	C802	1	2	100P_0402_50V8J
KSO11	C803	1	2	100P_0402_50V8J
KSO11	C804	1	2	100P_0402_50V8J
KSO12	C805	1	2	100P_0402_50V8J
KSO15	C807	1	2	100P_0402_50V8J
KSO15	C807	1	2	100P_0402_50V8J
KSI7	C808	1	2	100P_0402_50V8J
KSI2	C810	1	2	100P_0402_50V8J
KSI3	C811	1	2	100P_0402_50V8J
KSI4	C812	1	2	100P_0402_50V8J
KSI0	C813	1	2	100P_0402_50V8J
KSI5	C814	1	2	100P_0402_50V8J
KSI6	C815	1	2	100P_0402_50V8J
KSI1	C816	1	2	100P_0402_50V8J
CAPS_LED#	C817	1	2	100P_0402_50V8J
CURS_LED#	C818	1	2	100P_0402_50V8J
NUM_LED#	C819	1	2	100P_0402_50V8J

CS/B Connector

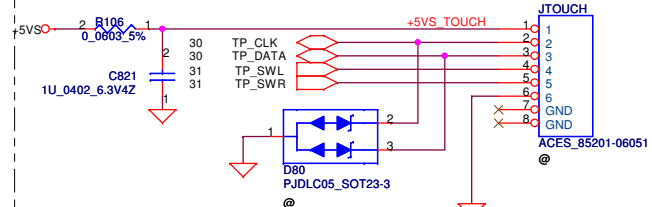


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				Document Number
				Rev
				1.0
Date:	Monday, August 10, 2009	Sheet	31	of 41

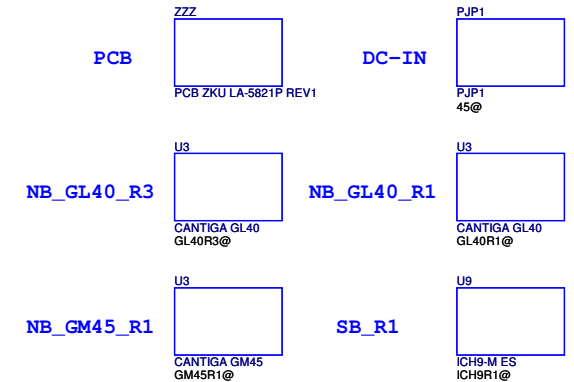
Power Button



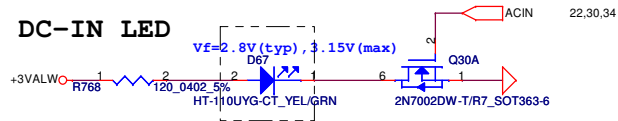
Touch Pad Connector



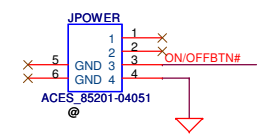
ISPD



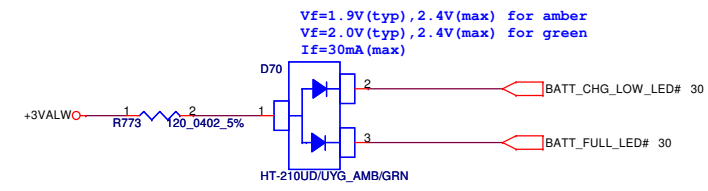
DC-IN LED



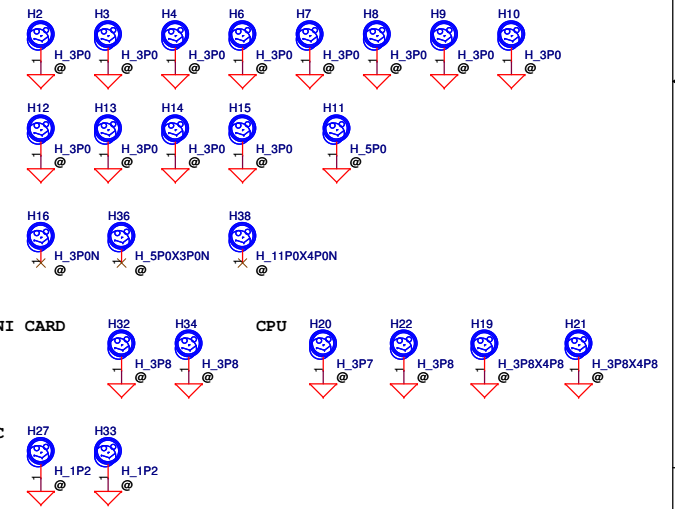
PWR/B



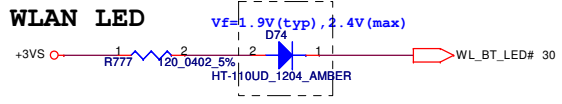
BATT CHARGE/FULL LED



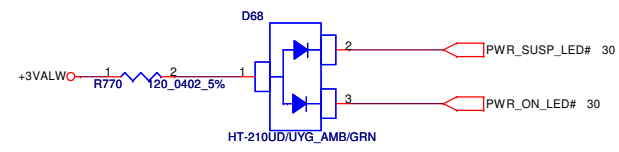
Screw Hole



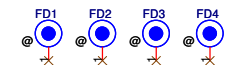
WLAN LED



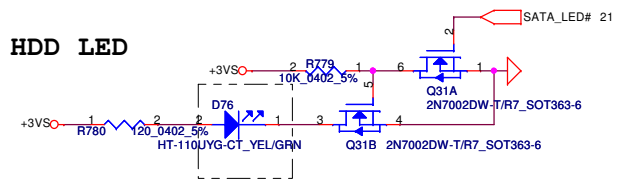
POWER/SUSPEND LED



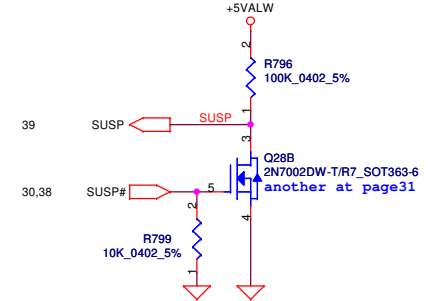
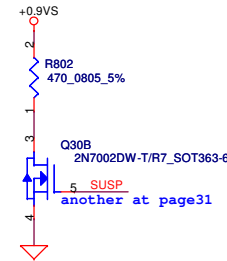
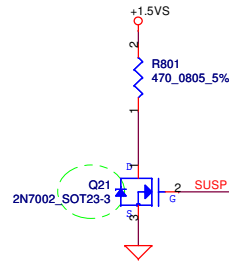
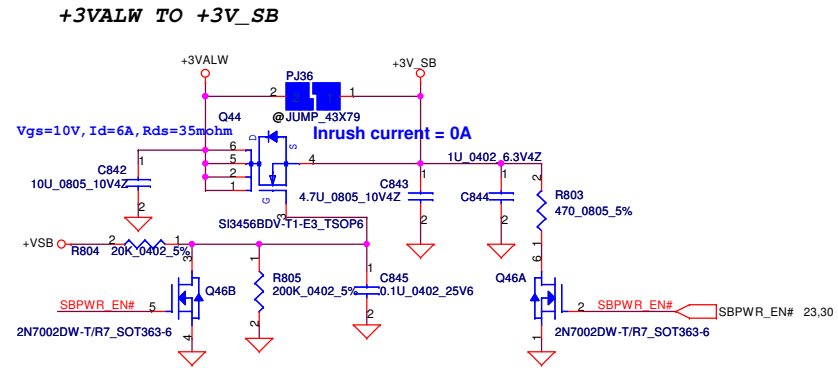
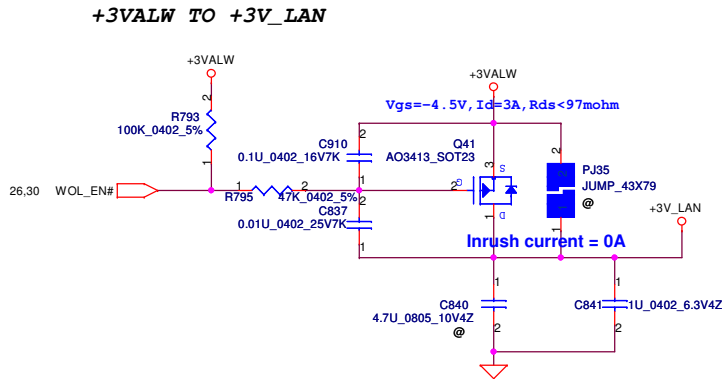
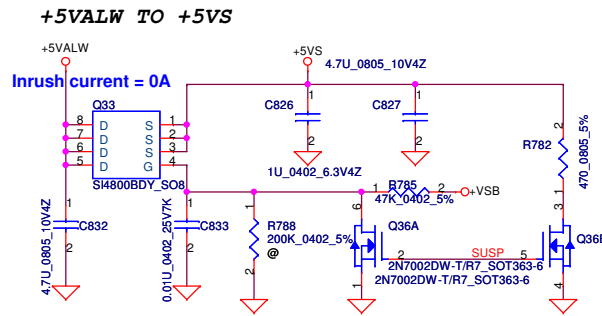
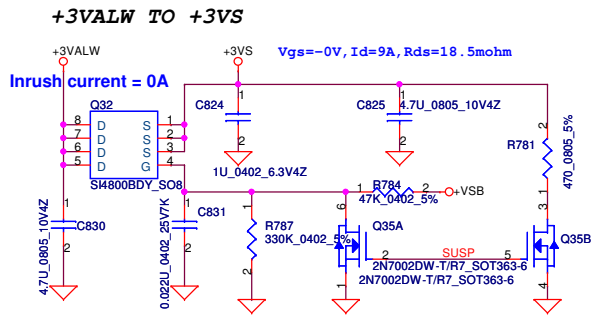
PCB Federal Mark PAD



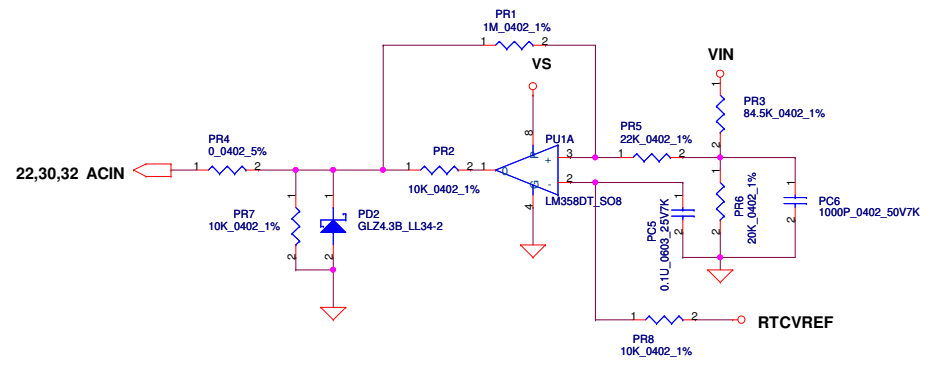
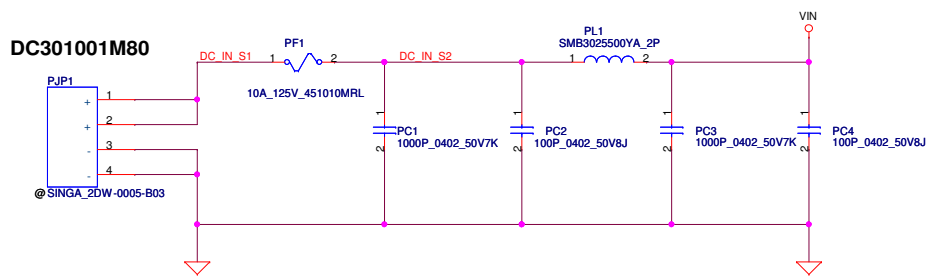
HDD LED



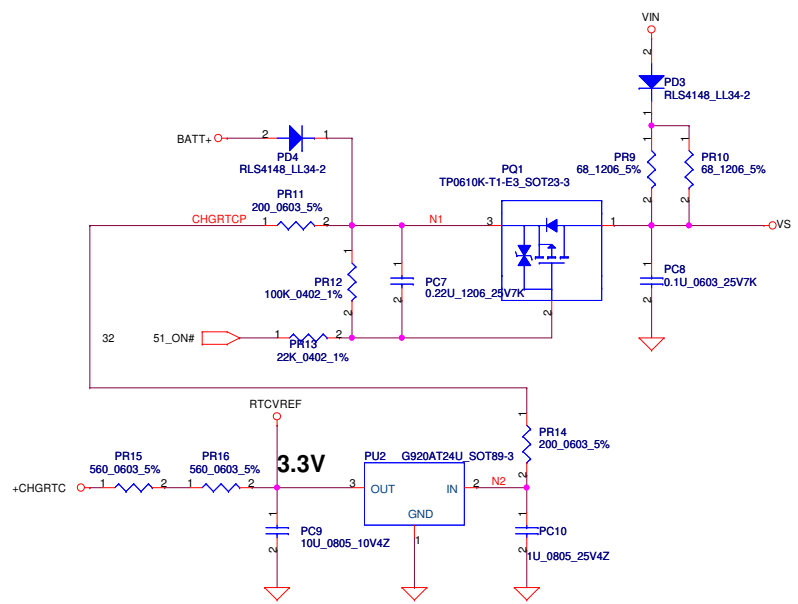
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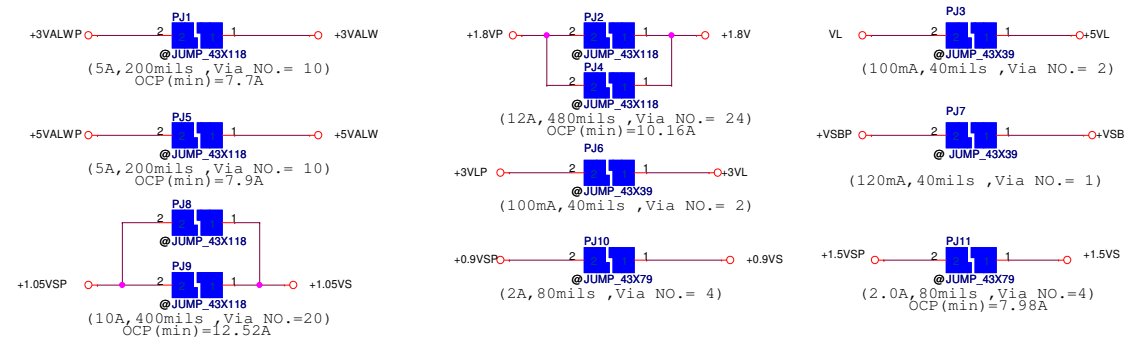
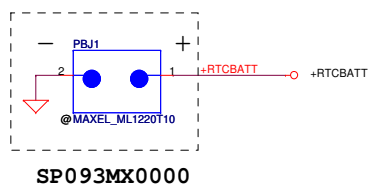
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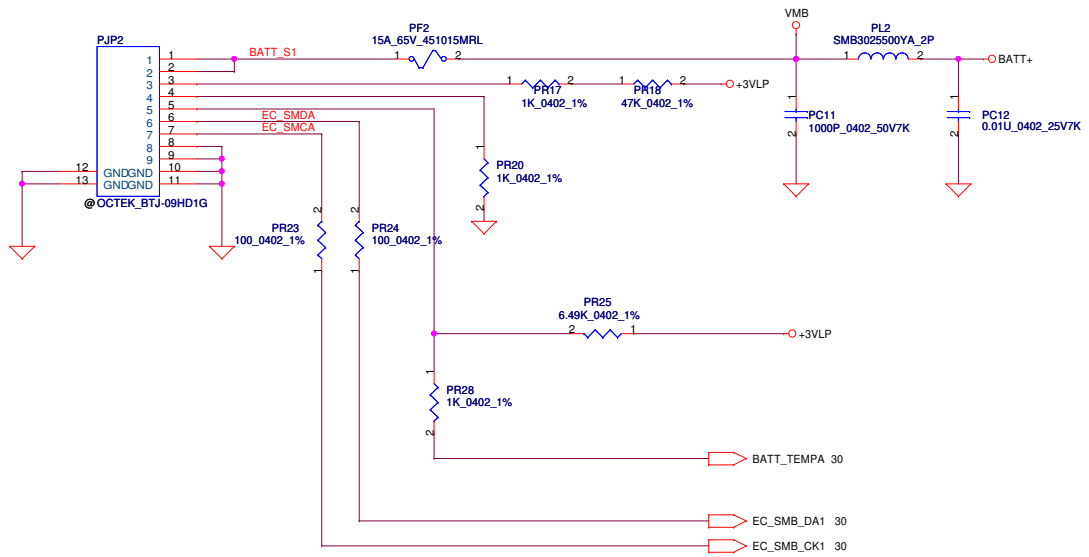
Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



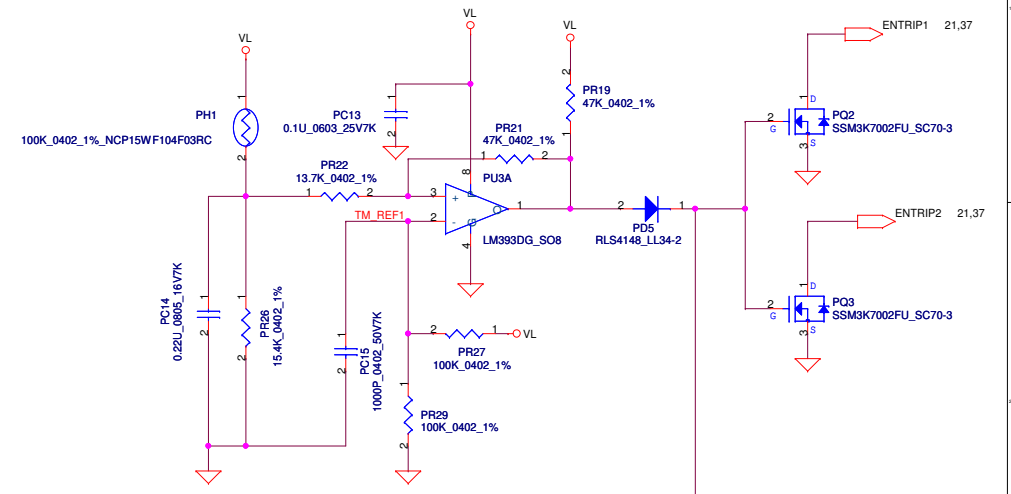
RTC Battery



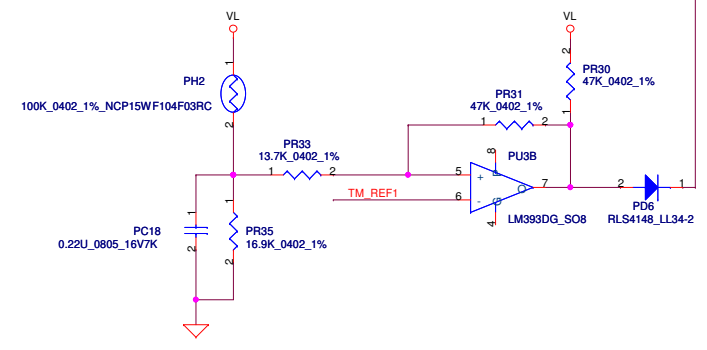
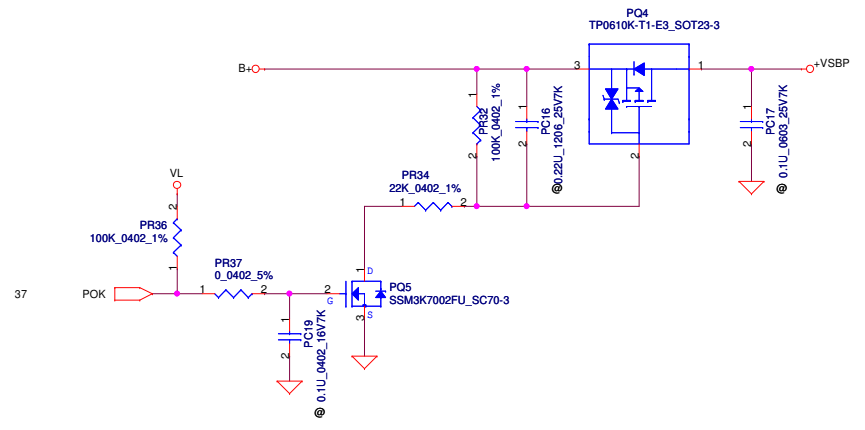
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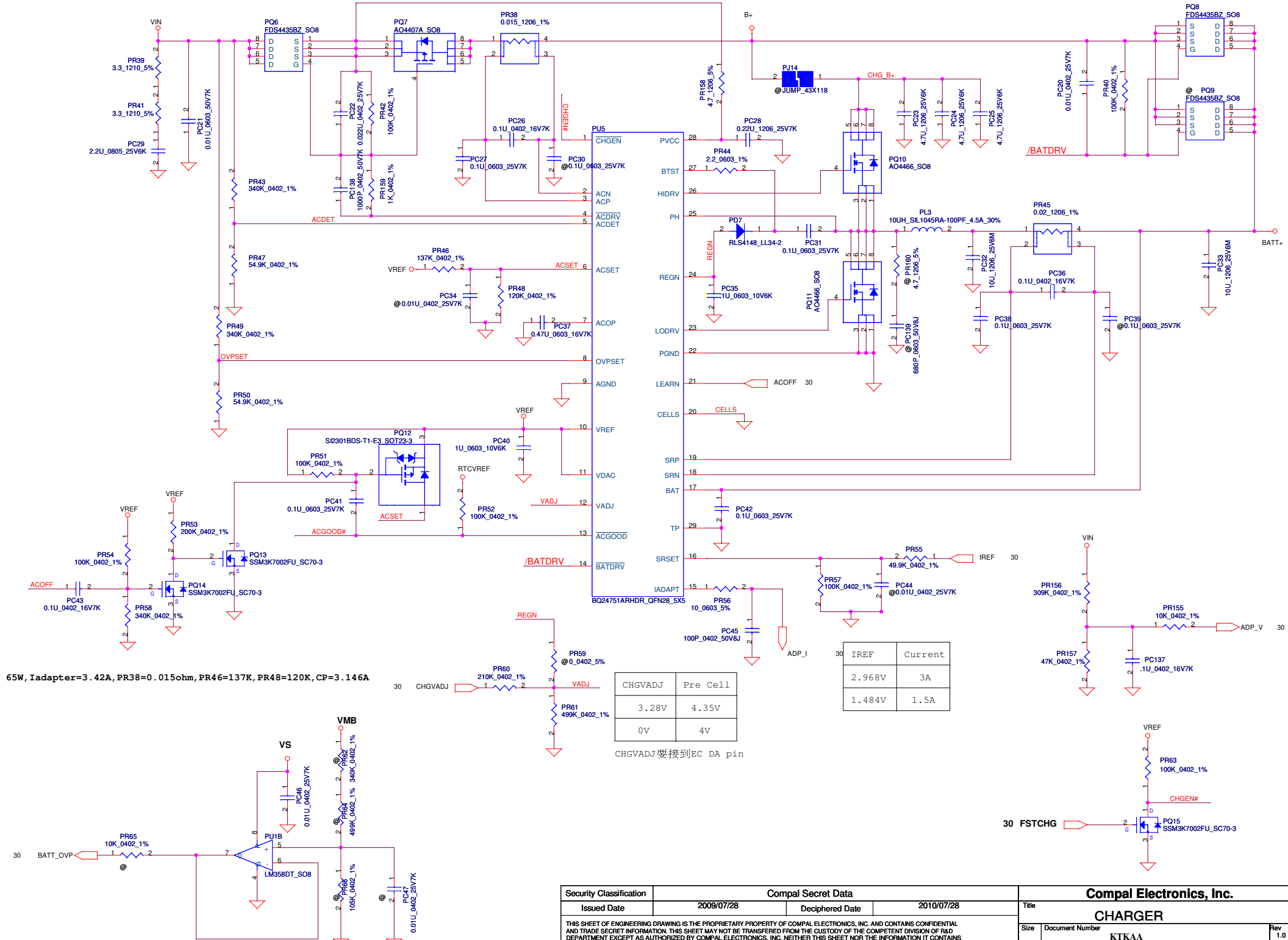


PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 90 degree C
 Recovery at 53 degree C





65W, Iadapter=3.42A, PR38=0.015ohm, PR46=137K, PR48=120K, CP=3.146A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

CHGVADJ要接到EC DA pin

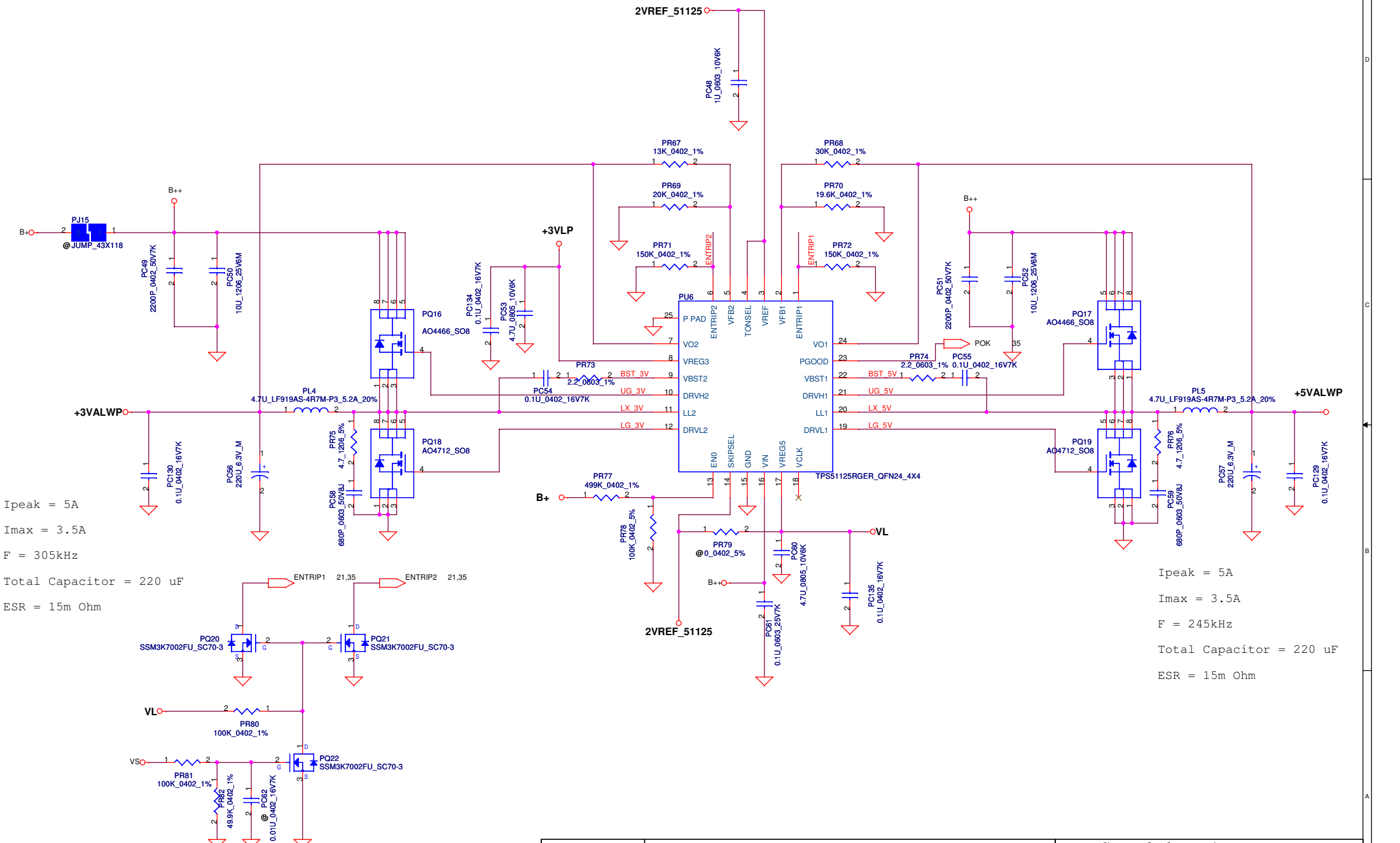
IREF	Current
2.968V	3A
1.484V	1.5A

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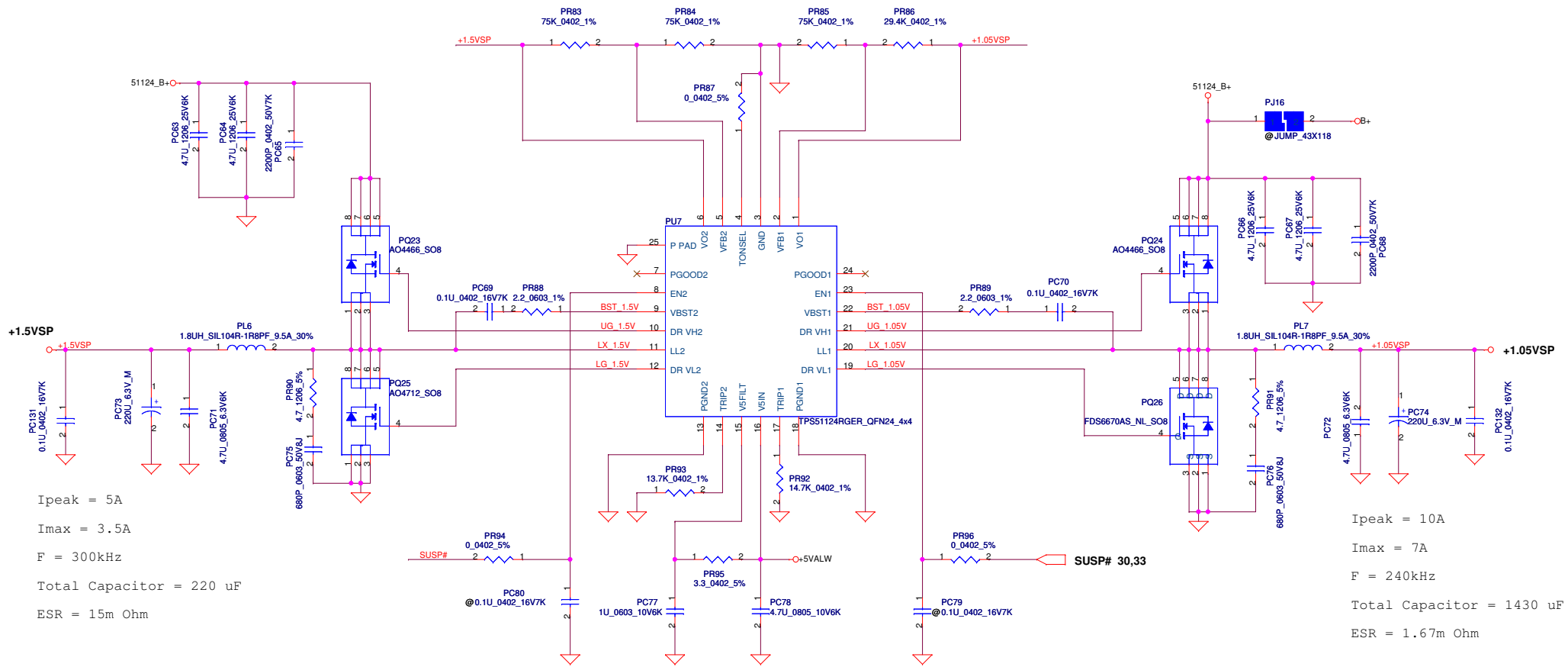
Compal Electronics, Inc.			
CHARGER			
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$I_{peak} = 5A$
 $I_{max} = 3.5A$
 $F = 305kHz$
 Total Capacitor = 220 μF
 ESR = 15m Ohm

$I_{peak} = 5A$
 $I_{max} = 3.5A$
 $F = 245kHz$
 Total Capacitor = 220 μF
 ESR = 15m Ohm



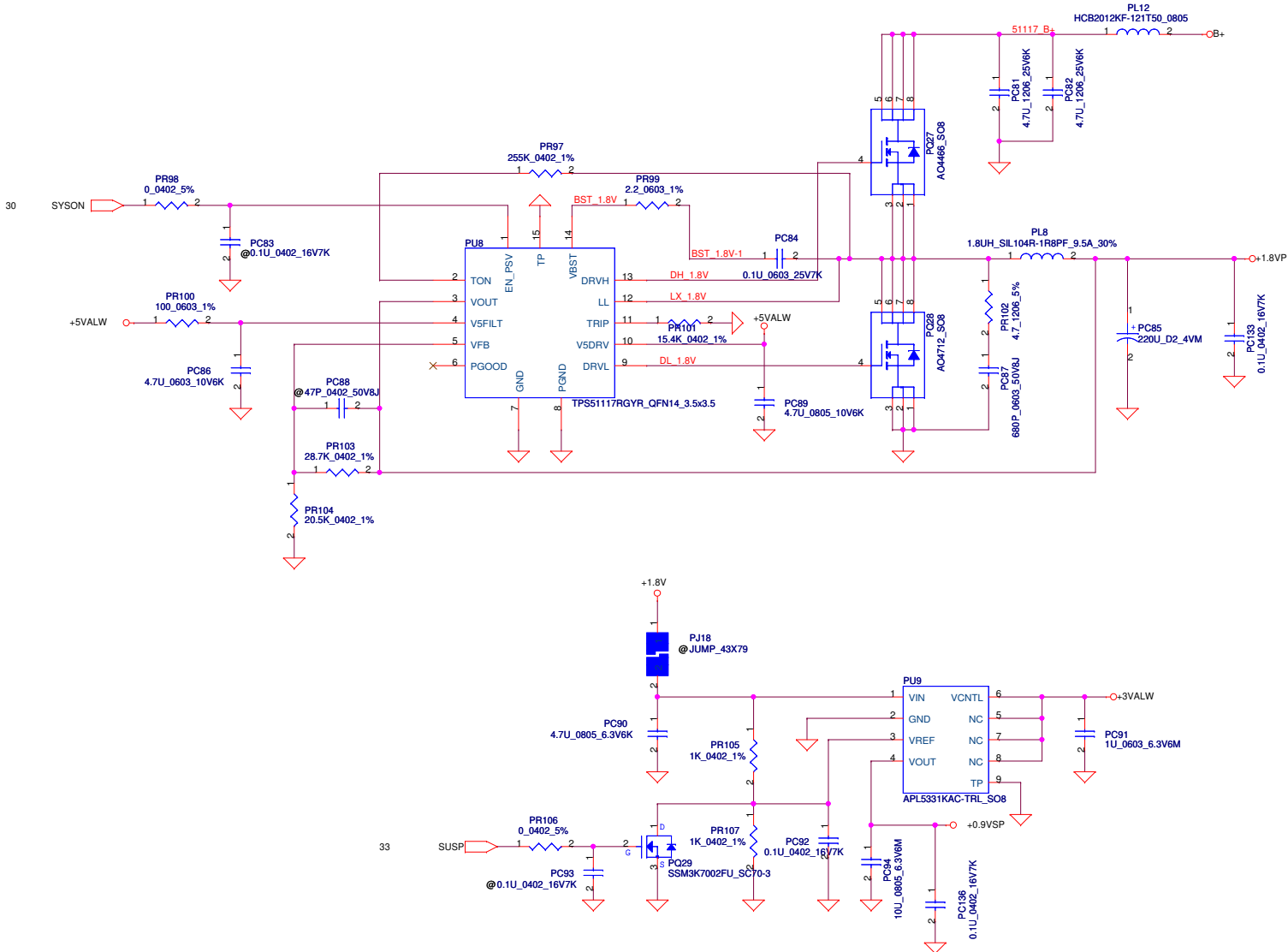
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Ipeak = 5A
 Imax = 3.5A
 F = 300kHz
 Total Capacitor = 220 uF
 ESR = 15m Ohm

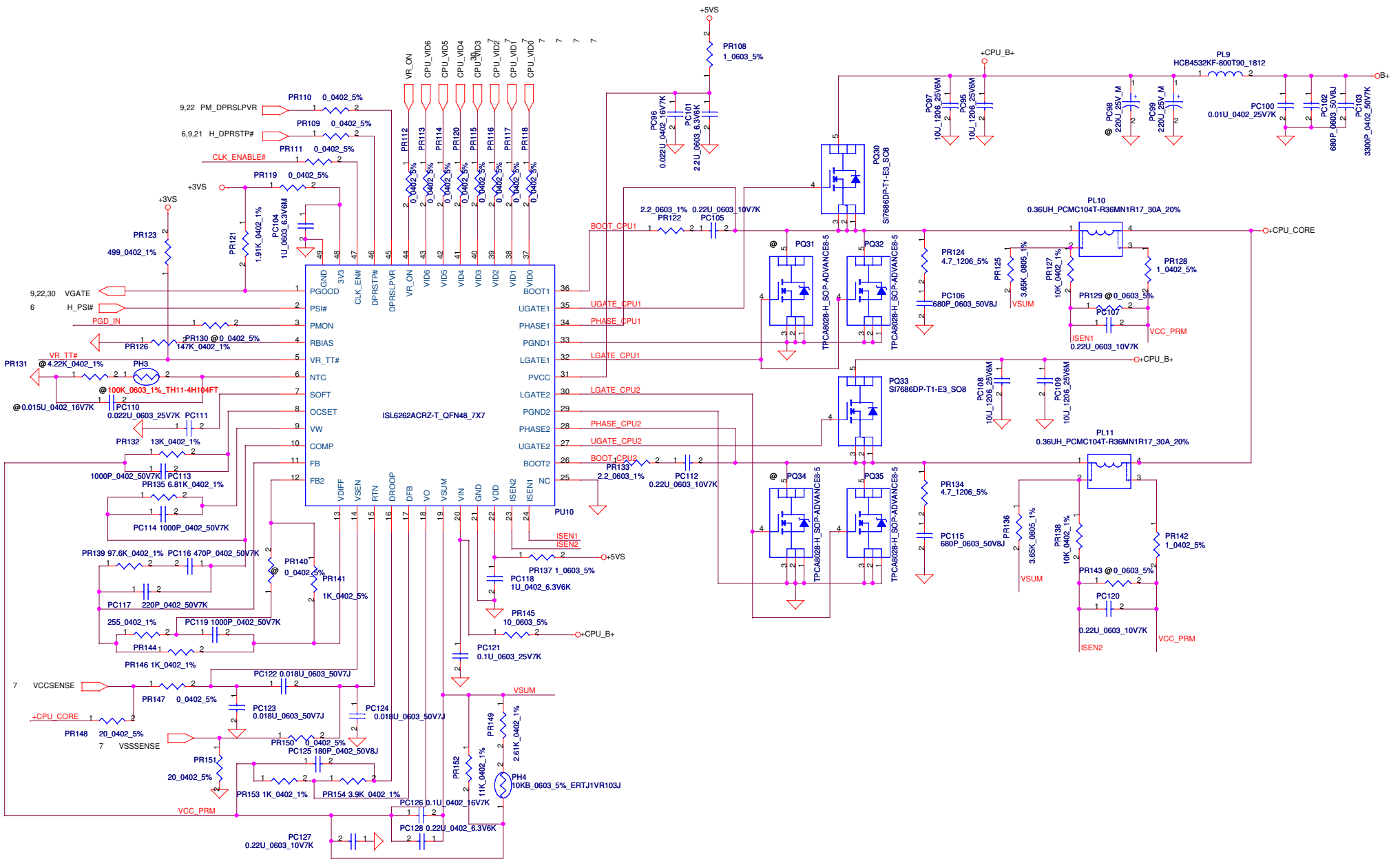
Ipeak = 10A
 Imax = 7A
 F = 240kHz
 Total Capacitor = 1430 uF
 ESR = 1.67m Ohm

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$I_{peak} = 8A$
 $I_{max} = 5.6A$
 $F = 312kHz$
 Total Capacitor = 440 uF
 ESR = 7.5m Ohm

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PIR (Product Improve Record)

NBWAA LA-5821P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	08/06	18	Add R936 on BKOFF#; R937 on INVT_PWM	To prevent EC pin damage
2.	08/06	26	Add RL90, RL91, RL91 on +3V_LAN	For EMI's request
3.	08/06	18	Add C922, C923, C924 220pF on DAC_BRIG, INVT_PWM_R, BKOFF#_R	For EMI's request
4.	08/06	31	Delete R752, C787 on SPI_CLK; Add L912, C925 on SPI_CLK_L	For EMI's request
5.	08/06	28	Add LA11 on INT_MIC_L	For EMI's request
6.	08/06	28	Mount D61, DA3, DA6, DA7	For ESD's request
7.	08/06	32	Un-mount SW5, SW6	Power button, no need after pre-MP

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