

Compal Confidential

NEWX5 / PEW56 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

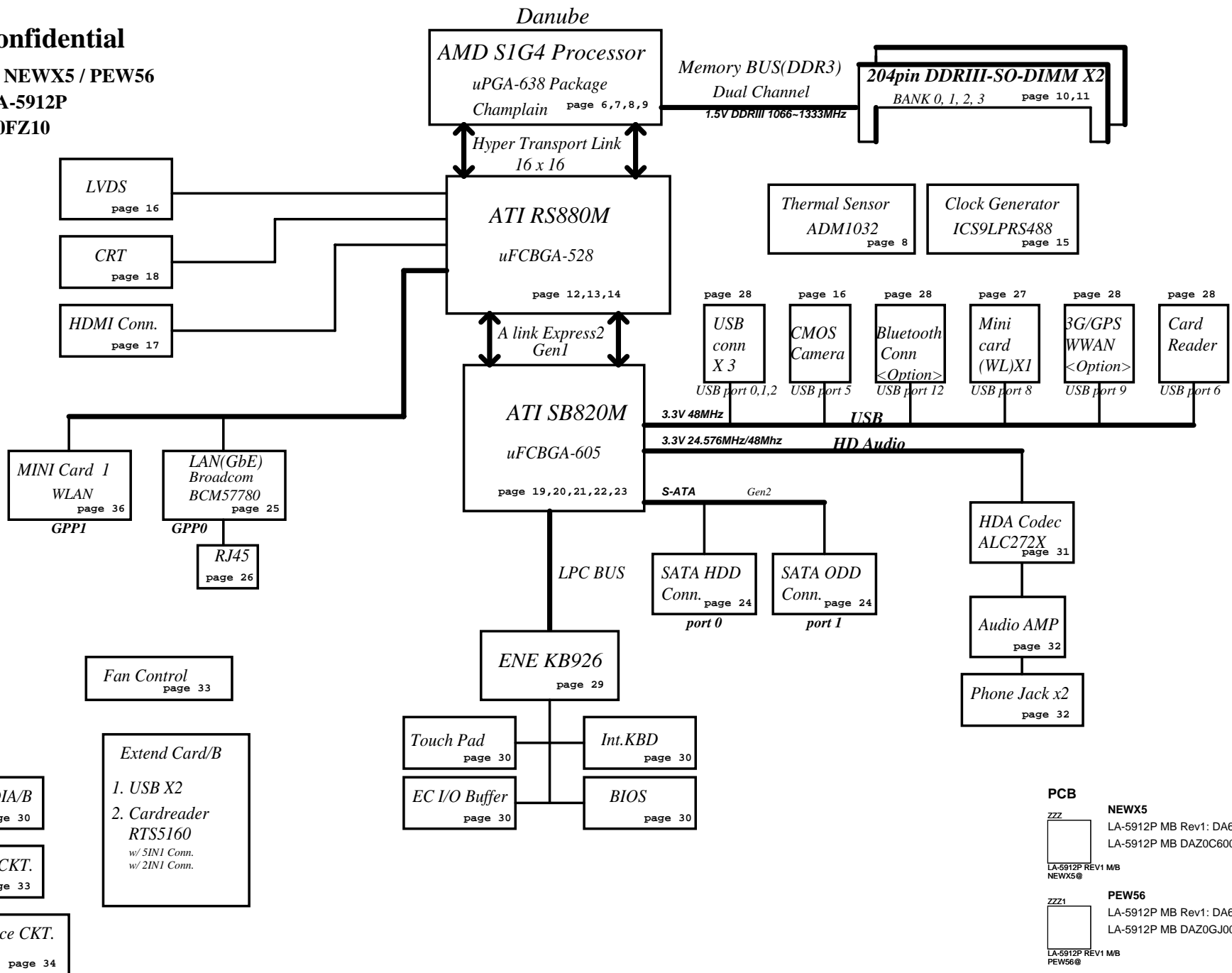
2010-06-17

LA5912P REV: 1.0

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				Date:	Wednesday, June 30, 2010	Sheet 1 of 45

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Model Name : NEWX5 / PEW56
 File Name : LA-5912P
 P/N : DA6000FZ10

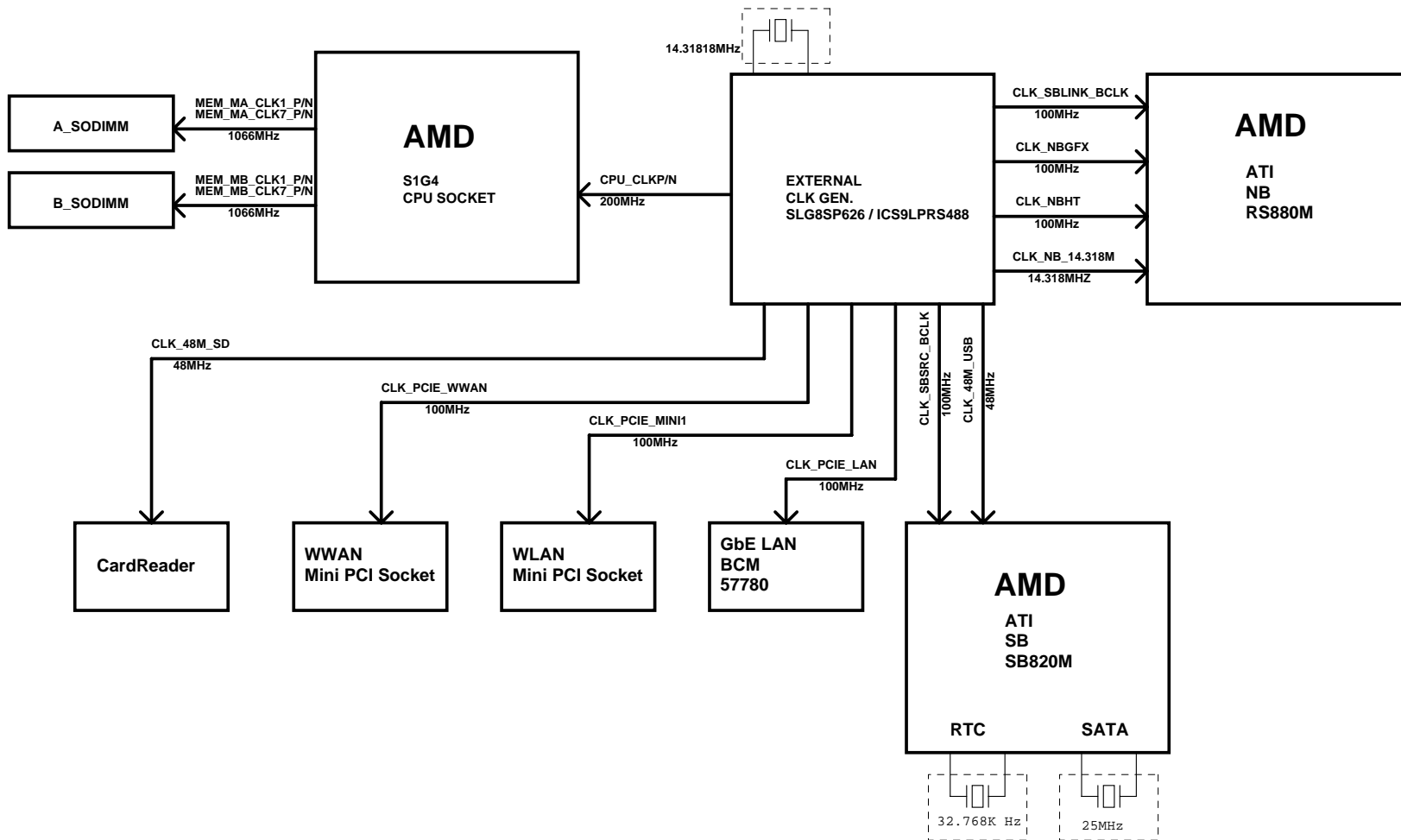


PCB

ZZZ NEWX5
 LA-5912P MB Rev1: DA6000FZ10
 LA-5912P MB DAZ0G600100
 LA-5912P REV1 MB NEWX5®

ZZZ1 PEW56
 LA-5912P MB Rev1: DA6000FZ10
 LA-5912P MB DAZ0GJ00100
 LA-5912P REV1 MB PEW56®

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (1.375-1.5V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+CPU_VDDR	1.05V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V power rail for MINI Card	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			SB-Temp Sensor		98H

EC SM Bus2 address

SB820 SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2		
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

SB820 SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	NEWX5 / PEW56 PVT stage (w/ pach code)
2	
3	
4	
5	
6	
7	

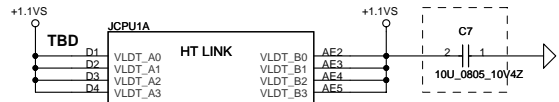
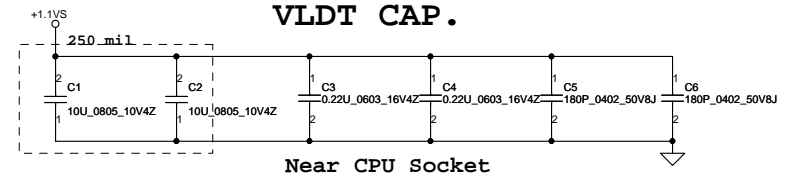
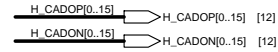
BTO Option Table

BTO Item	BOM Structure
Internal CLK	INT@
External CLK	EXT@
Vari-Bright	VB@
No Vari-Bright	UNVB@
HDMI	HDMI@
NEWX5	NEWX5@
PEW56	PEW56@
NEW75/85 LED	7585@
NEW95/PEW56 LED	9556@
Bluetooth	BT@
3G	3G@

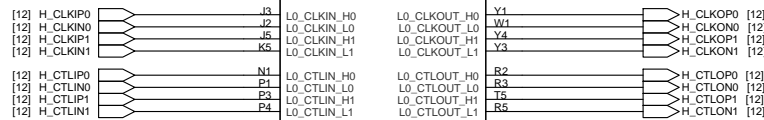
Project ID Table

Board ID	PCB Revision
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1	PEW56
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3	
4	
5	
6	
7	

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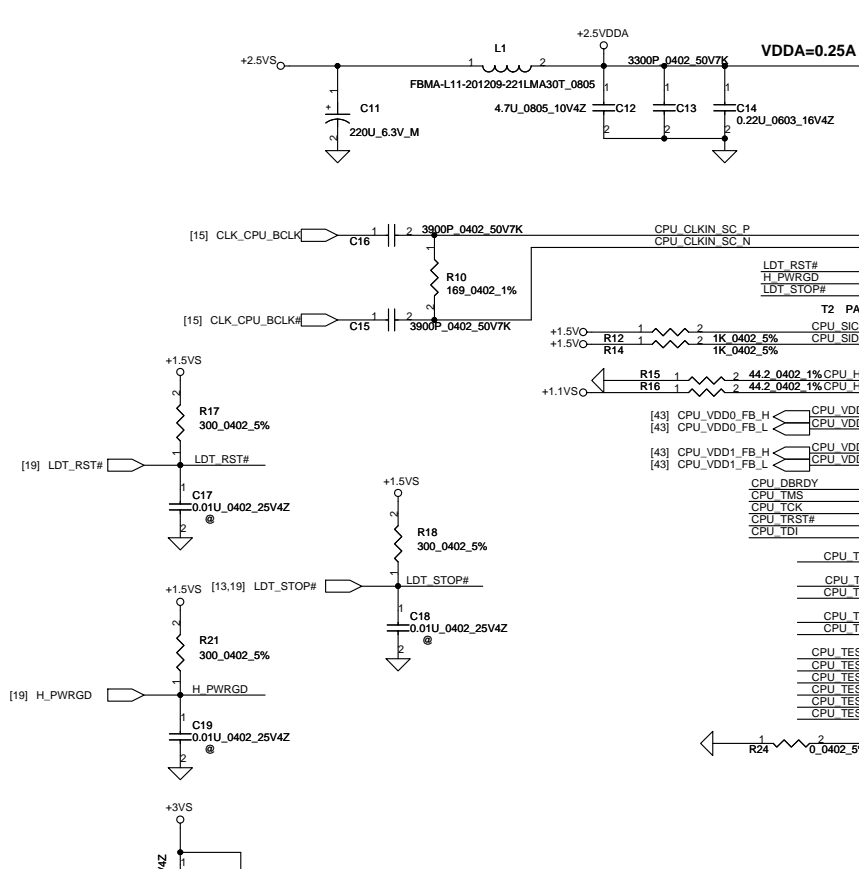


H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	H1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	L11	H_CADON5
H_CADIP6	L4	L0_CADIN_H6	L0_CADOUT_H6	L12	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	L13	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
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H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	Y5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	W5	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V4	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V3	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	V5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	U5	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T4	H_CADON15
				T3	H_CADON15

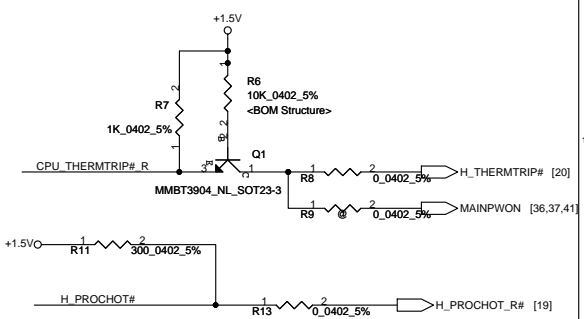
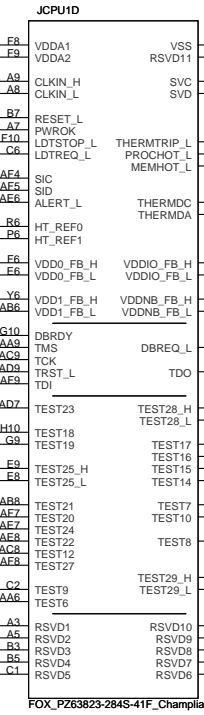


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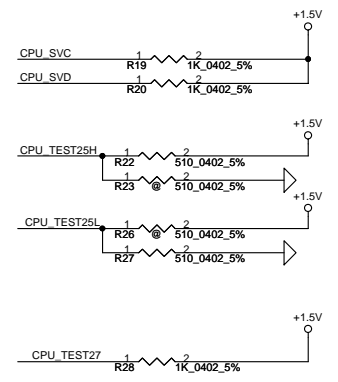
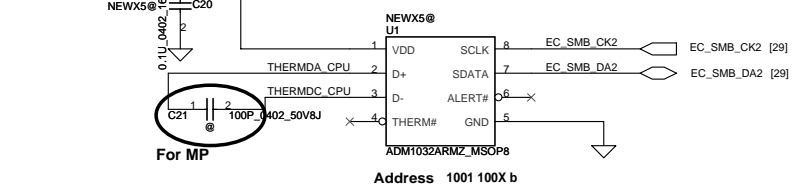
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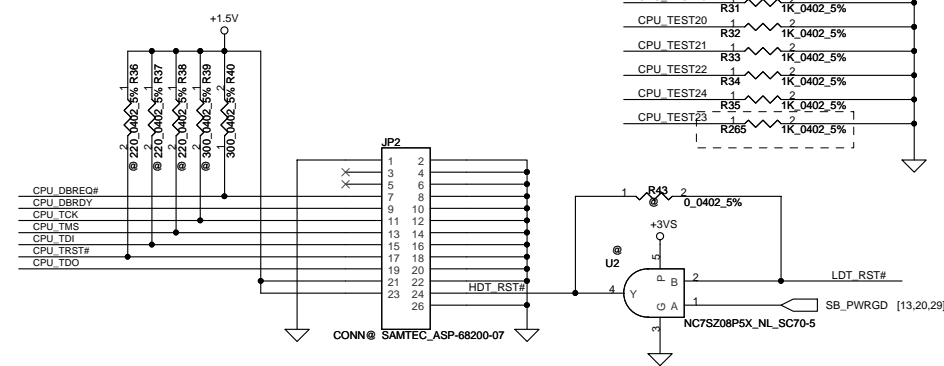
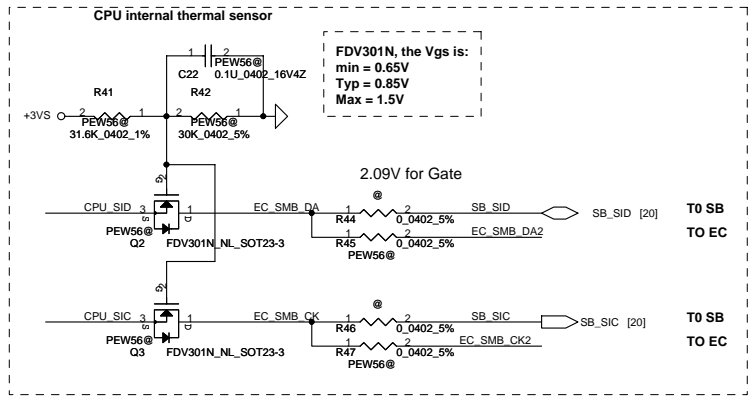
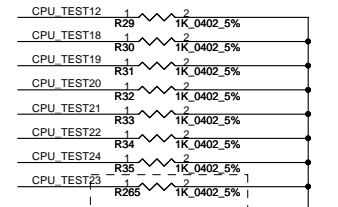
Champlain: C1E
 C1E: LDT_REQ# no connect
 CLMC: LDT_REQ# connect to NB
 LDT_RES# / MEMHOT#
 no support in S1g4



PROCHOT:
 Input: For HTC Function
 Output: Over Temperature Condition

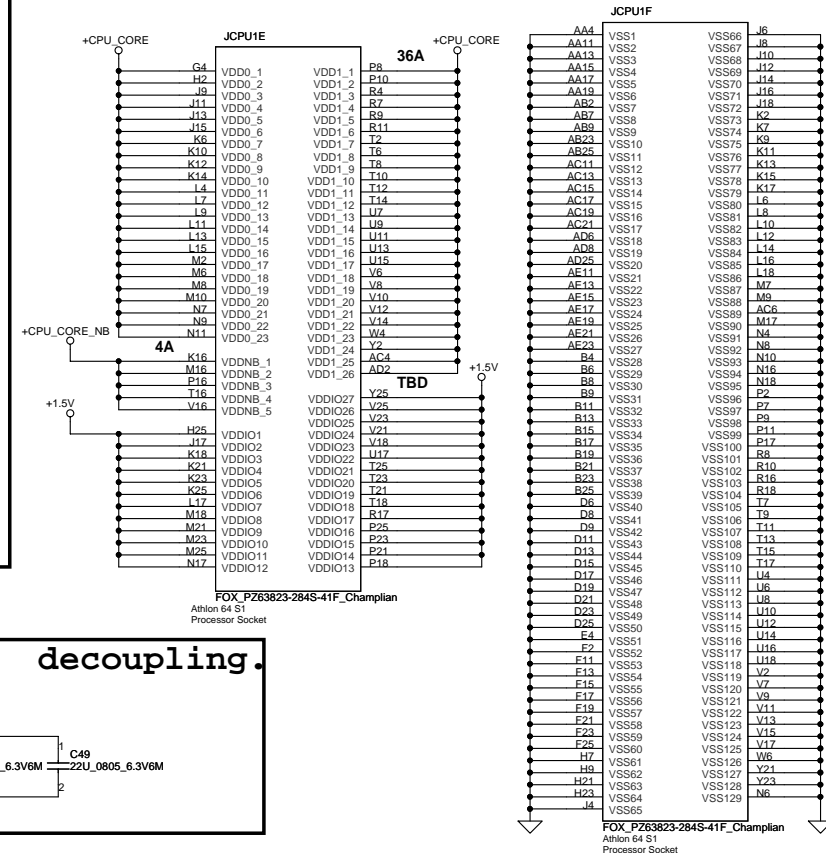
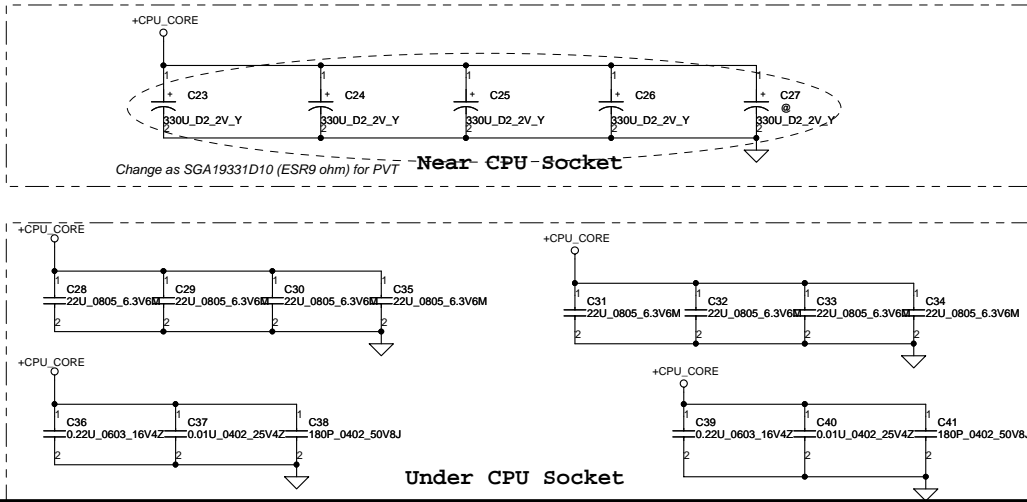


For SCAN connect use

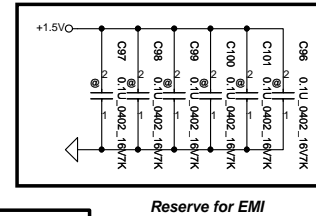
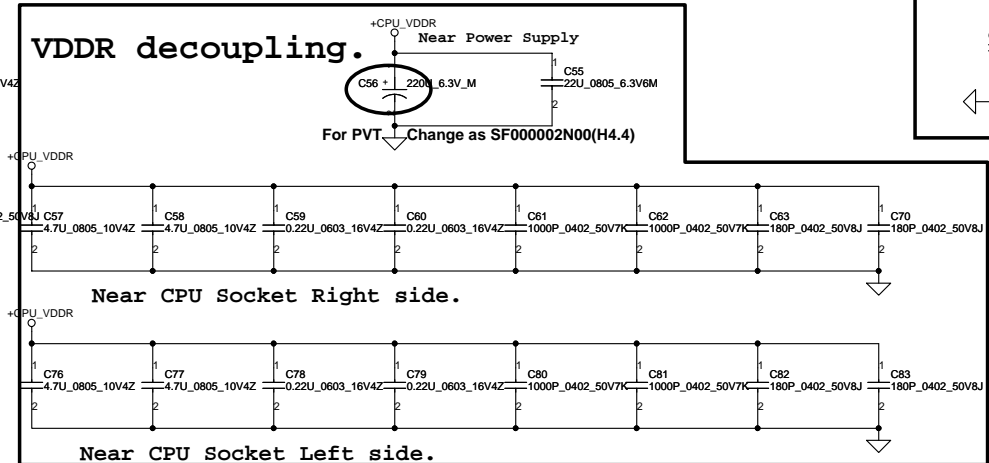
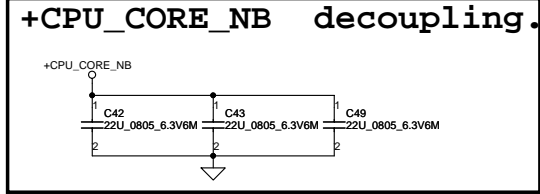
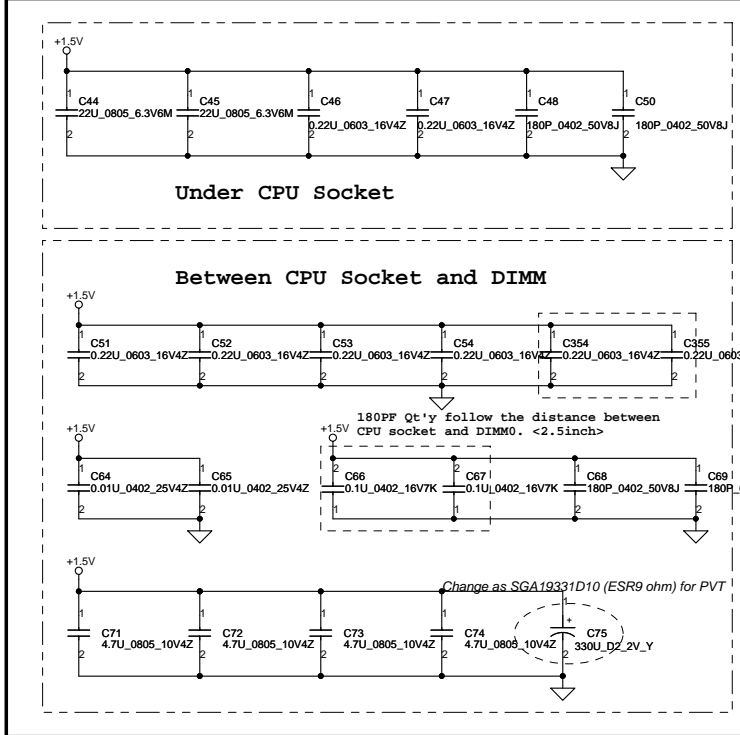


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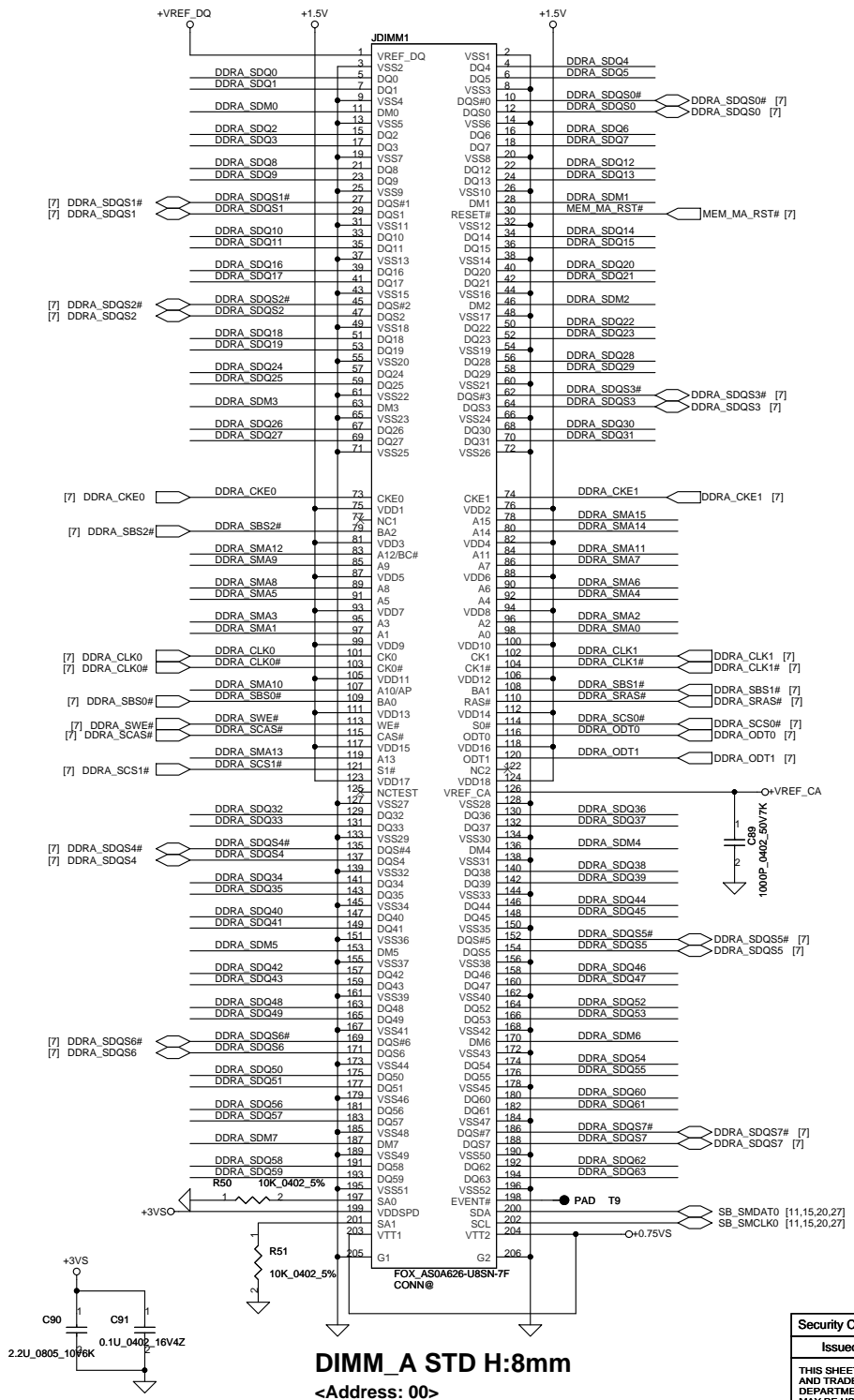
VDD(+CPU_CORE) decoupling.



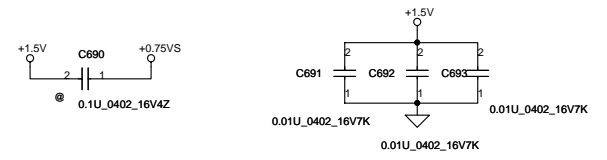
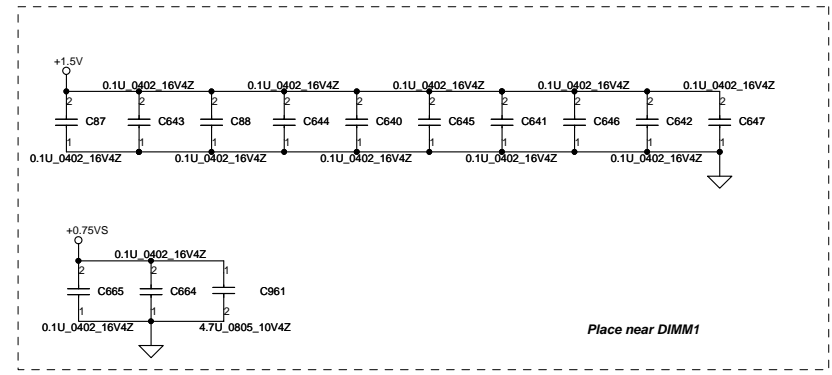
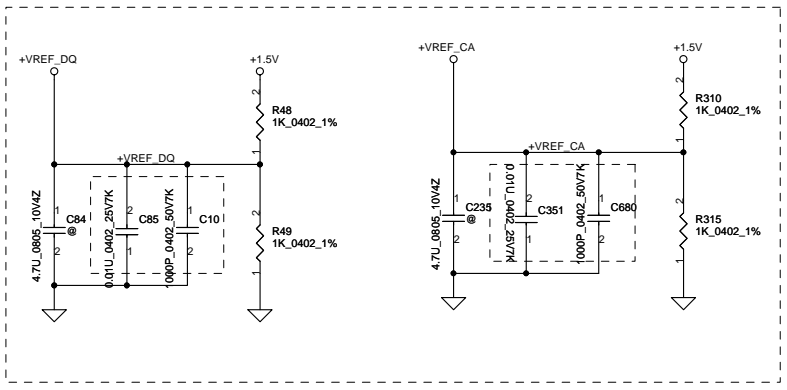
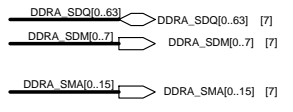
VDDIO decoupling.



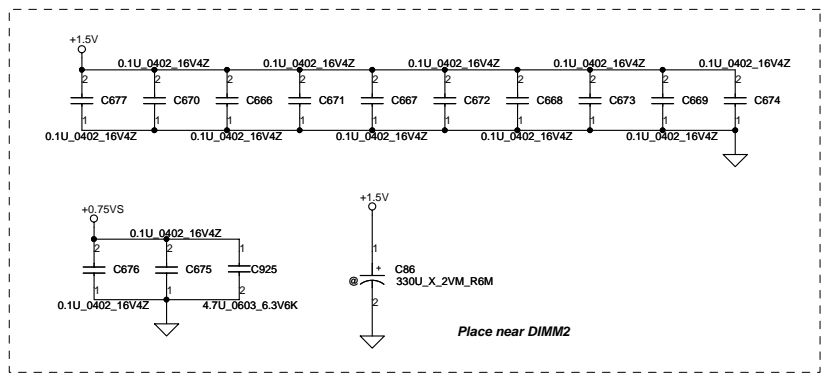
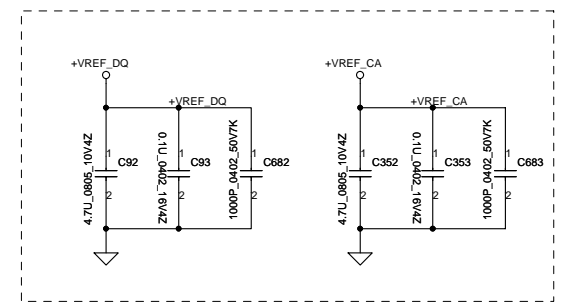
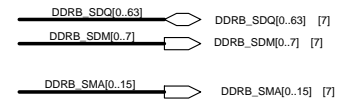
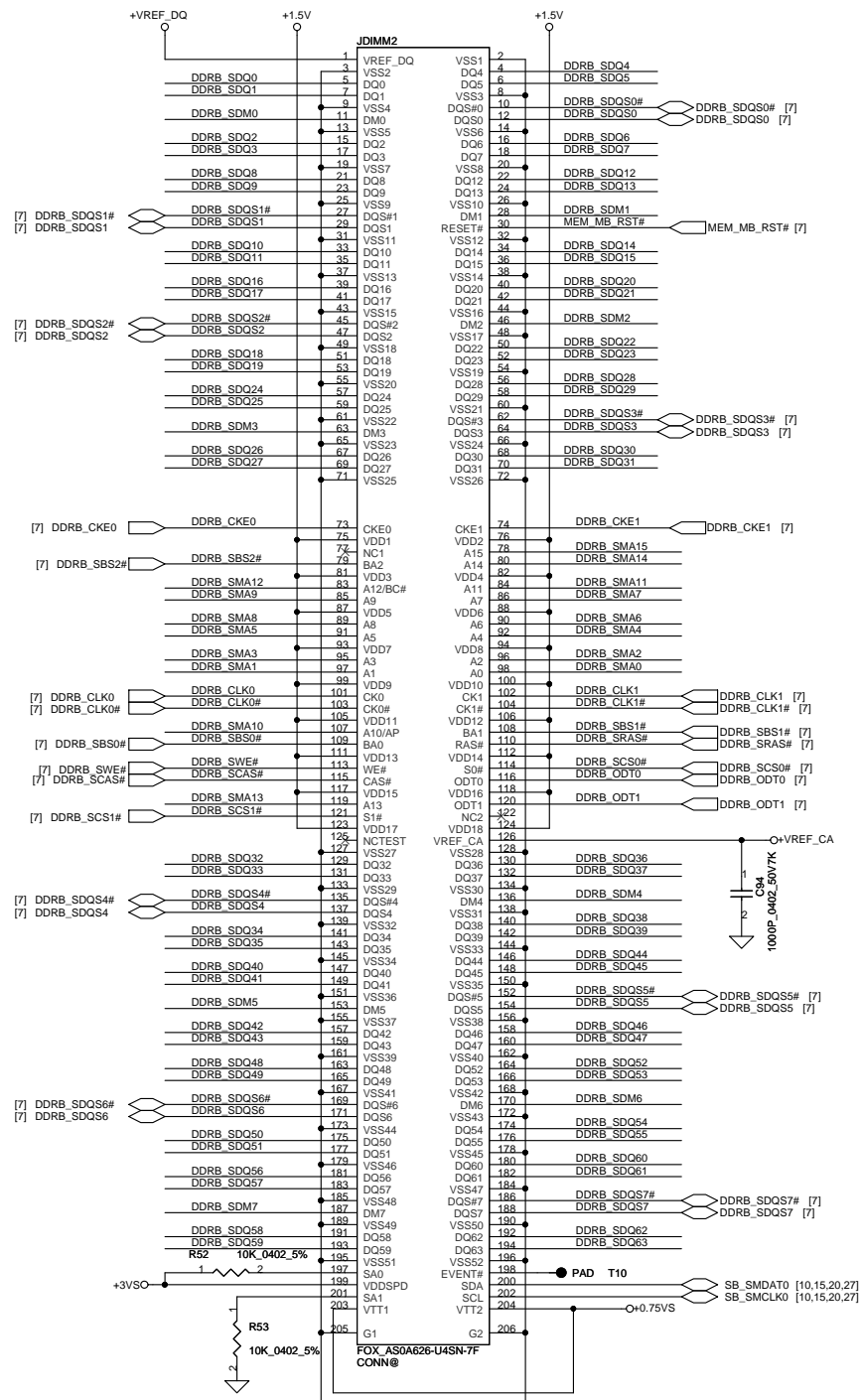
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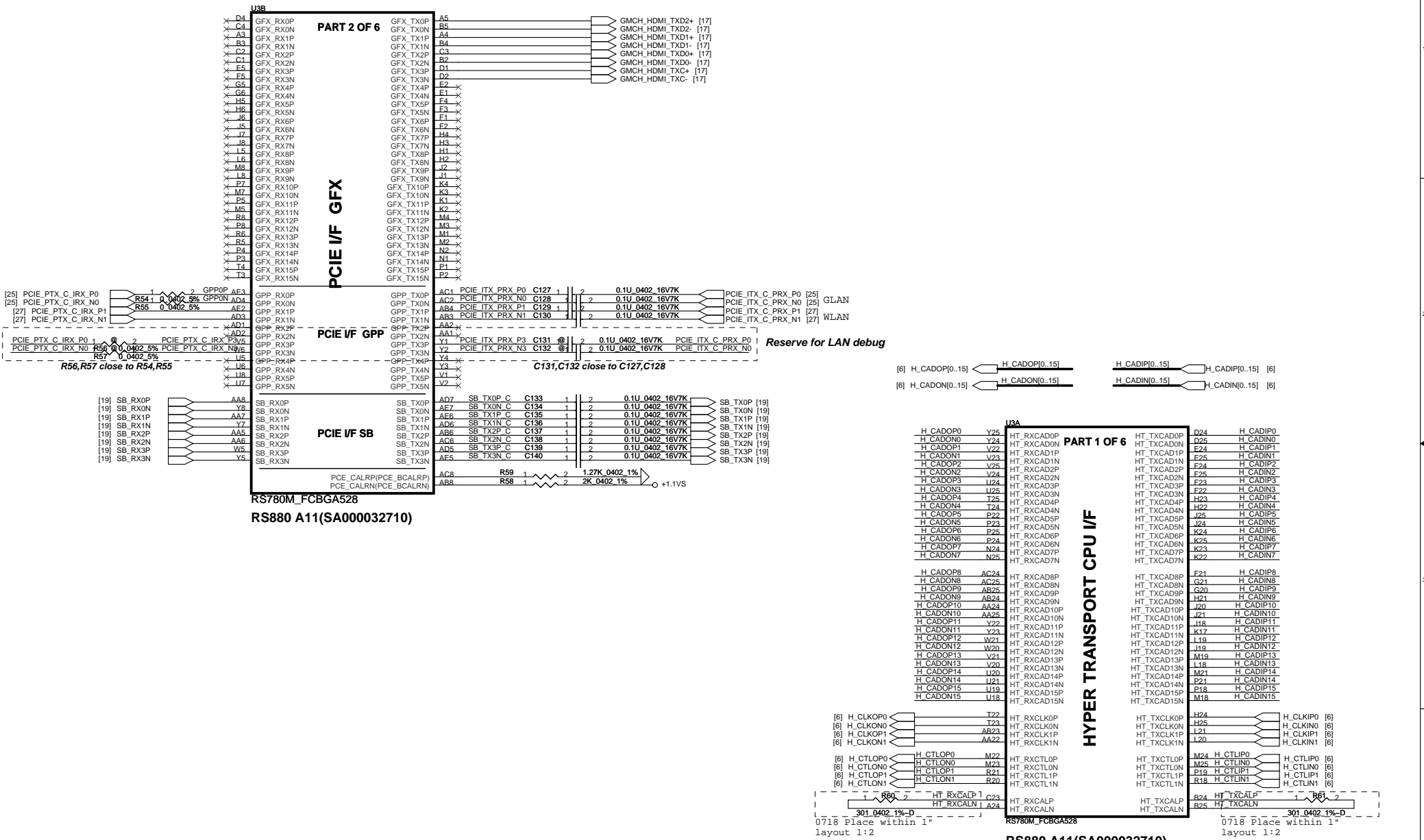


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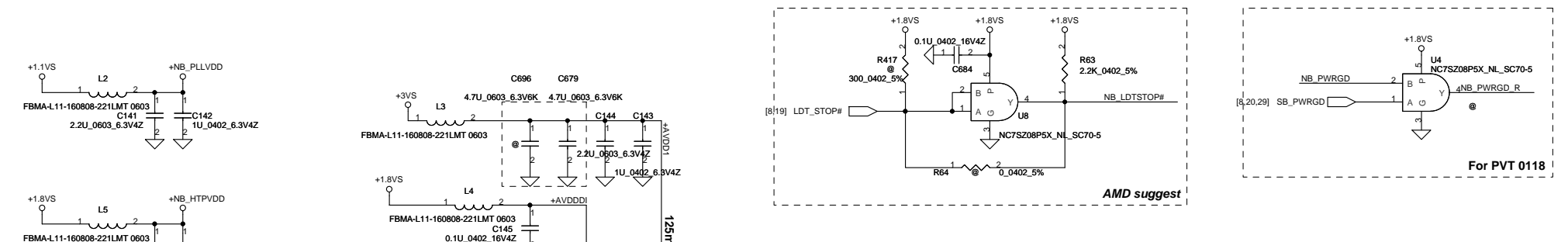


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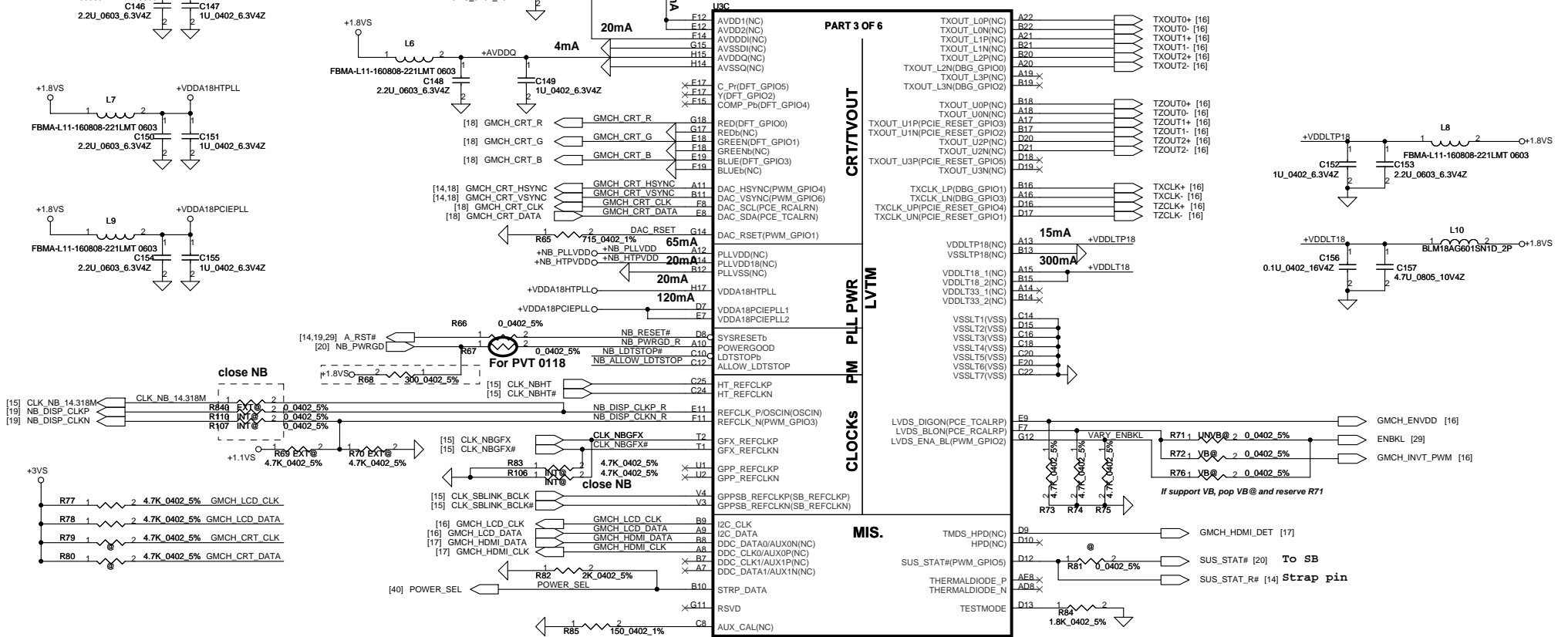
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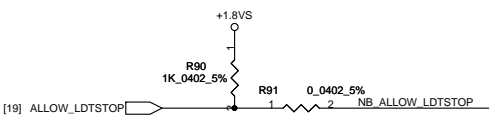
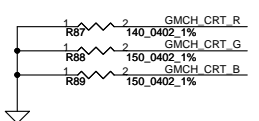
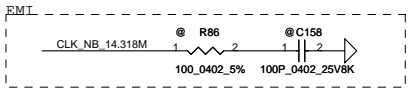
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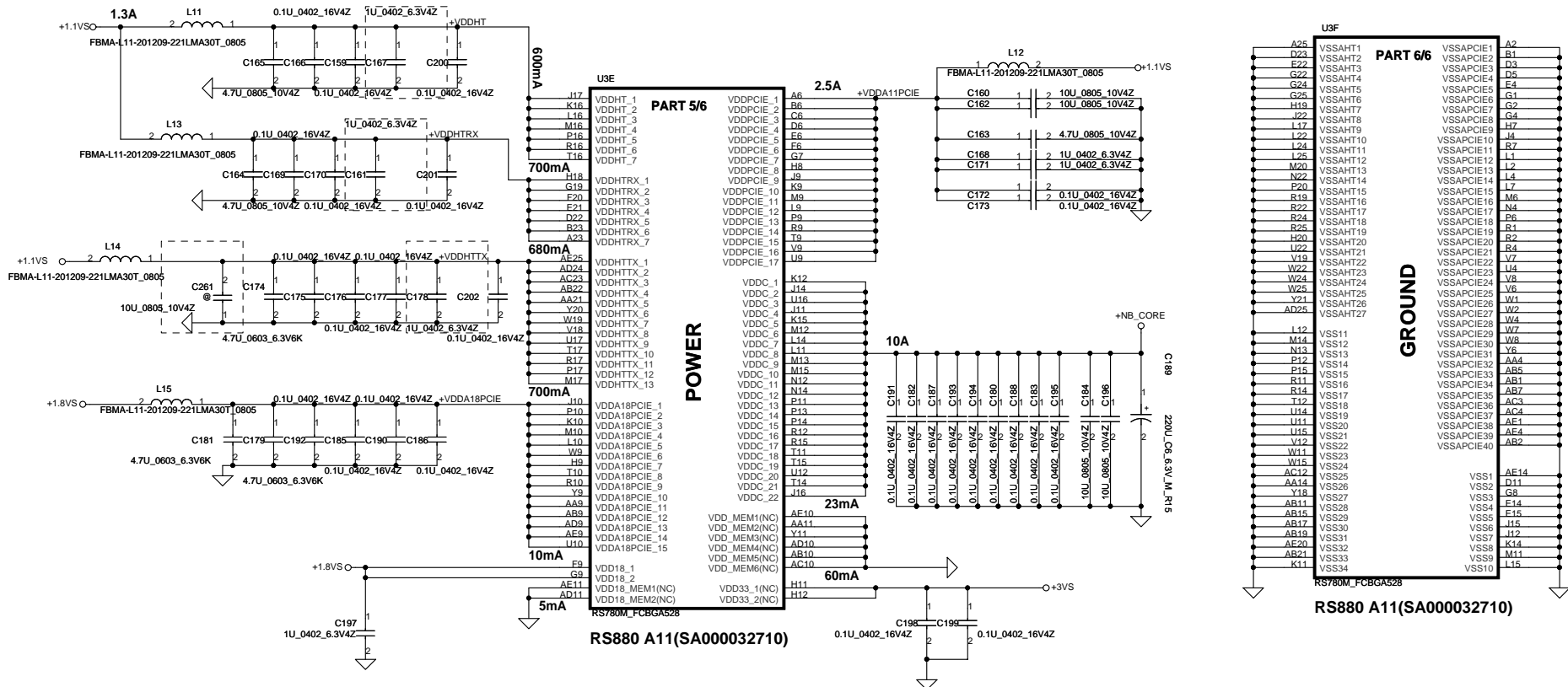
For PVT 0118



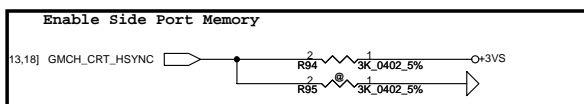
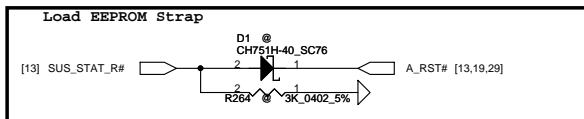
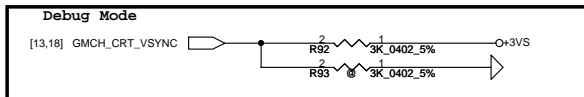
RS880	POWER_SEL
HIGH	0.95V
LOW	1.1V



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Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLE#

Enables the Test Debug Bus using GPIO. (VSYNC)

1 : Disable
0 : Enable

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

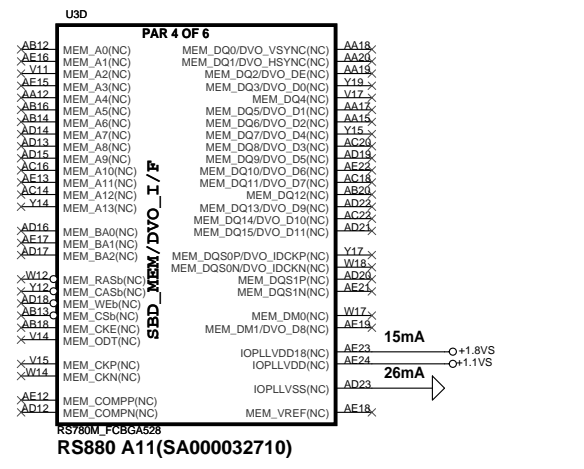
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Enable Side Port Memory

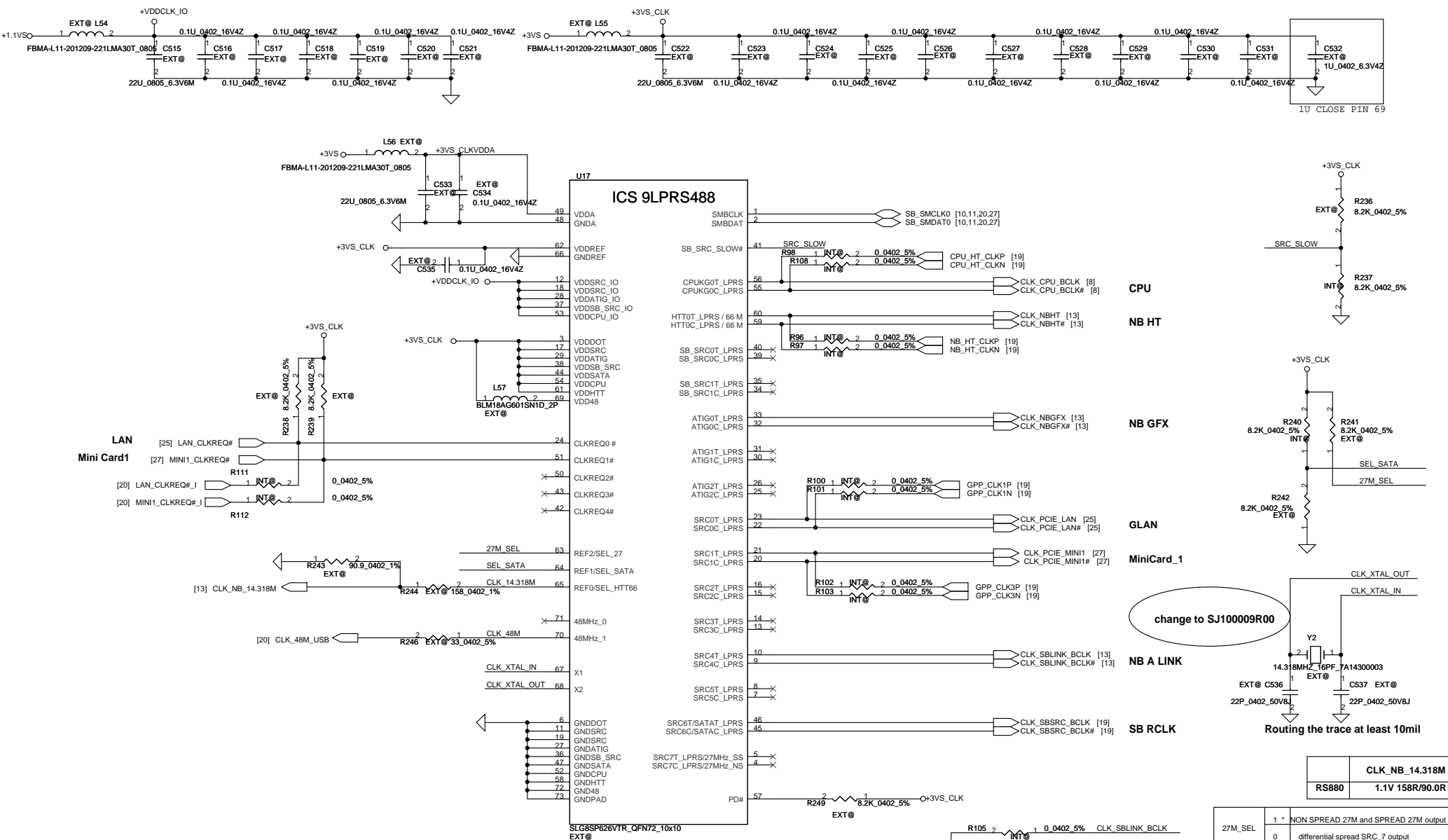
RS880: HSYNC# Register Readback of strap:

0: Enable
1: Disable

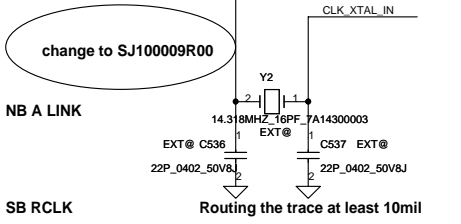
NB_CLKCFG:CLK_TOP_SPARE[D1]



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1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN



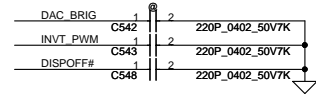
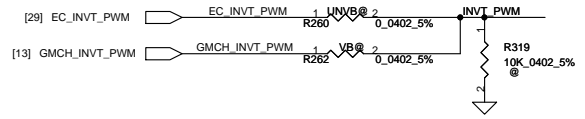
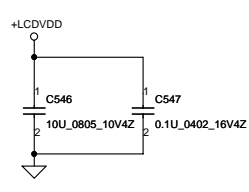
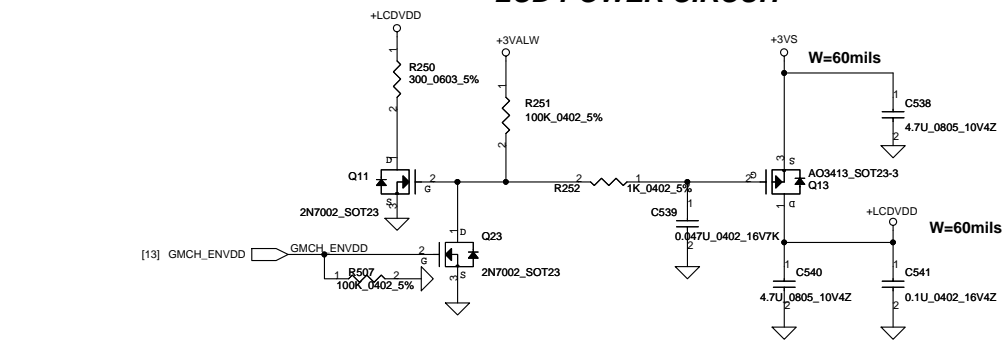
	CLK_NB 14.318M
RS880	1.1V 158R/90.0R

27M_SEL	1*	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

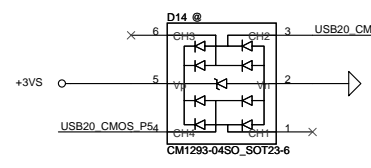
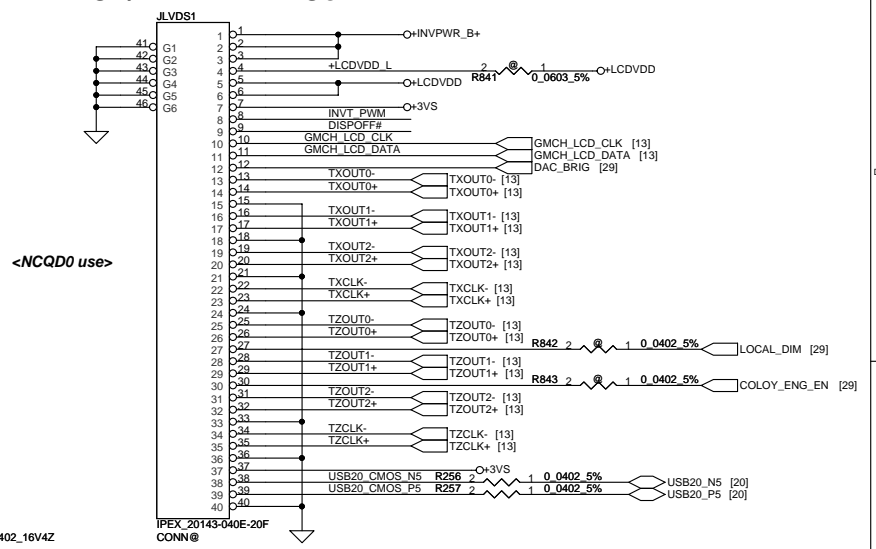
* default

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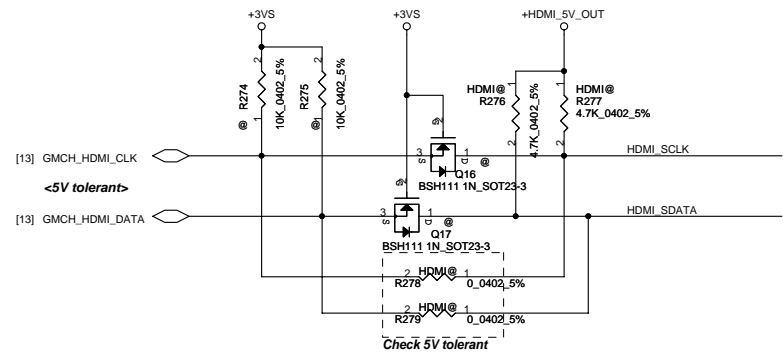
LCD POWER CIRCUIT



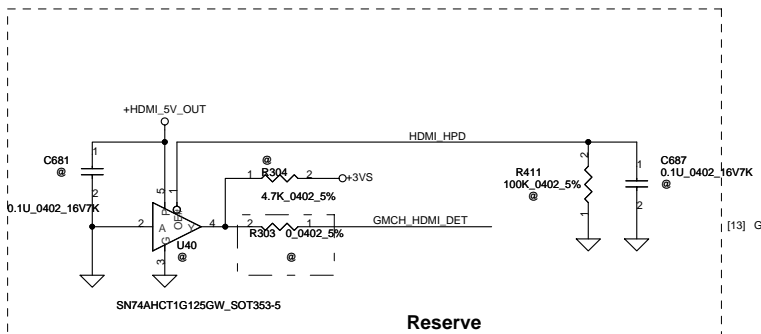
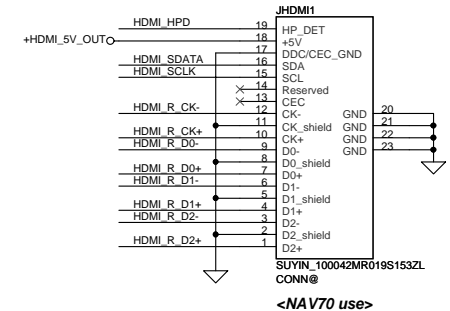
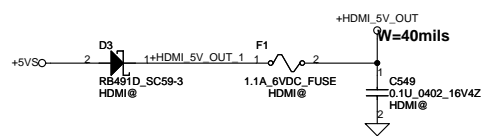
LCD/LED PANEL Conn.



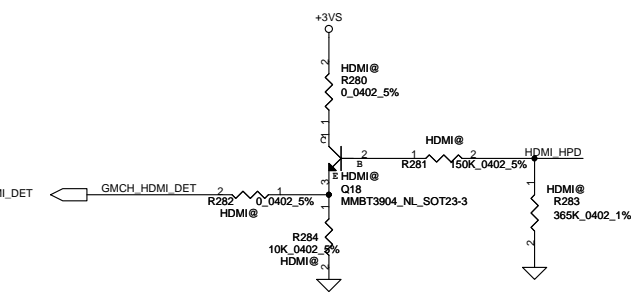
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Place closed to JHDMI1

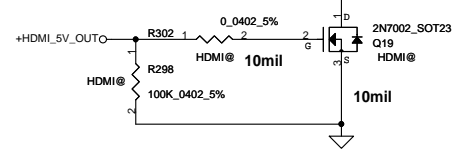


Reserve

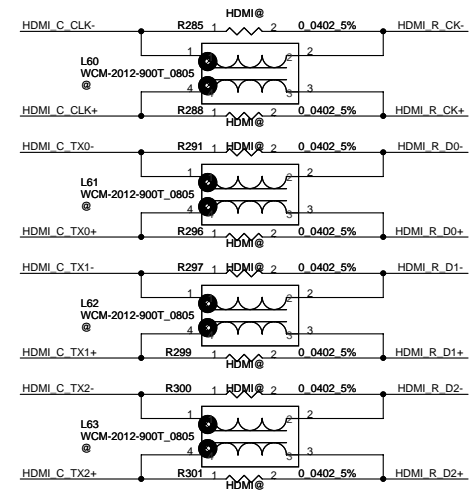


[12] GMCH_HDMI_TXD2-	C550	HDMI@	1	0.1U_0402_16V7K	HDMI C TX2-	R286	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXD2+	C551	HDMI@	1	0.1U_0402_16V7K	HDMI C TX2+	R287	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXD1-	C552	HDMI@	1	0.1U_0402_16V7K	HDMI C TX1-	R289	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXD1+	C553	HDMI@	1	0.1U_0402_16V7K	HDMI C TX1+	R290	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXD0-	C554	HDMI@	1	0.1U_0402_16V7K	HDMI C TX0-	R292	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXD0+	C555	HDMI@	1	0.1U_0402_16V7K	HDMI C TX0+	R293	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXC-	C556	HDMI@	1	0.1U_0402_16V7K	HDMI C CLK-	R294	1	HDMI@	2	715_0402_1%
[12] GMCH_HDMI_TXC+	C557	HDMI@	1	0.1U_0402_16V7K	HDMI C CLK+	R295	1	HDMI@	2	715_0402_1%

UMA 715 ohm

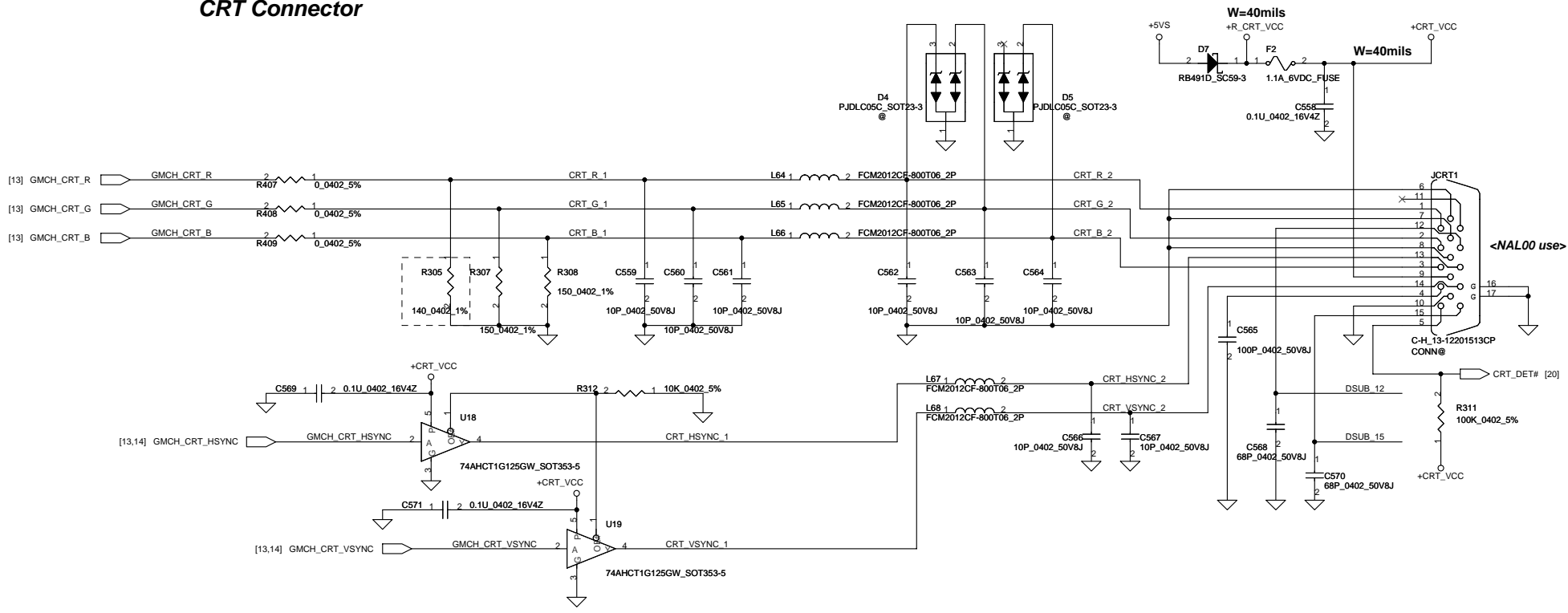


Place closed to JHDMI1

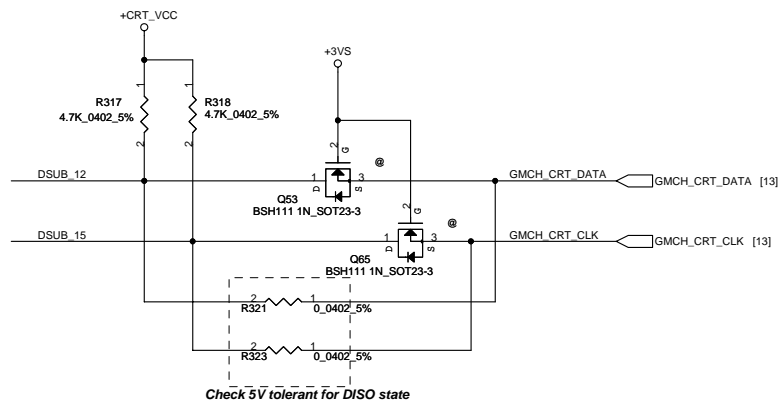


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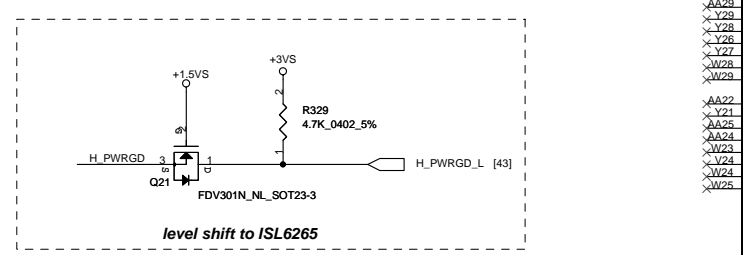
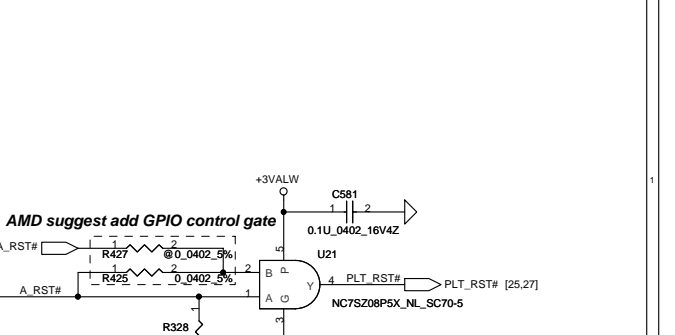
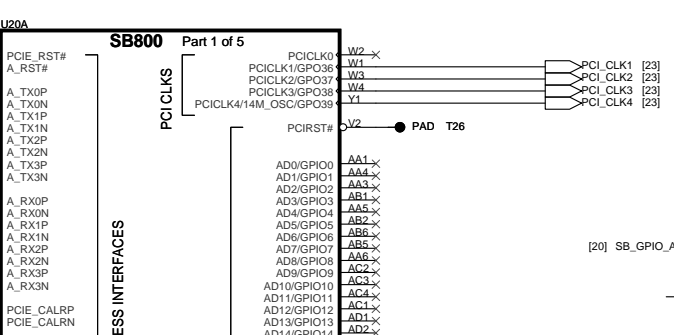
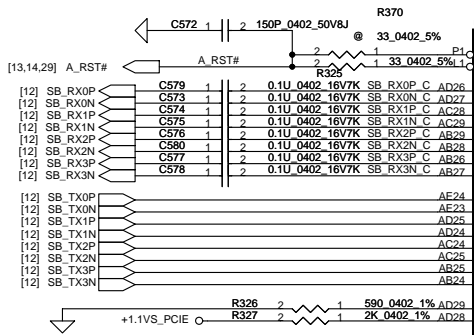
CRT Connector



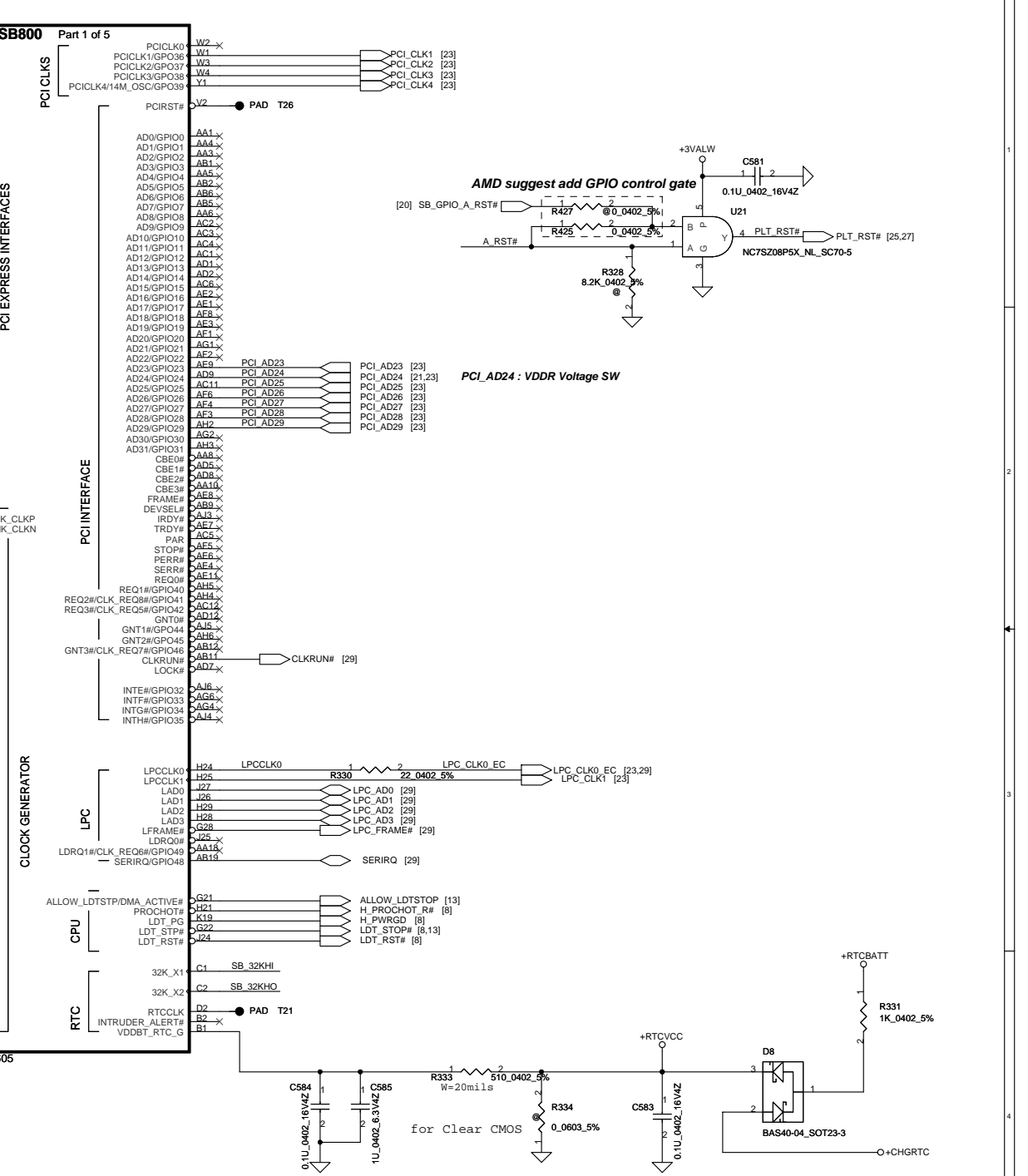
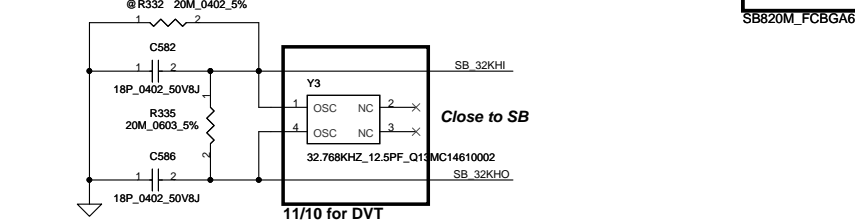
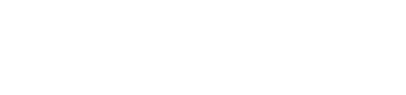
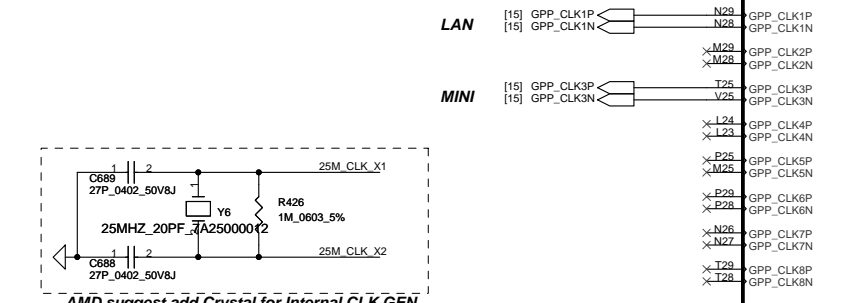
Close to Conn side



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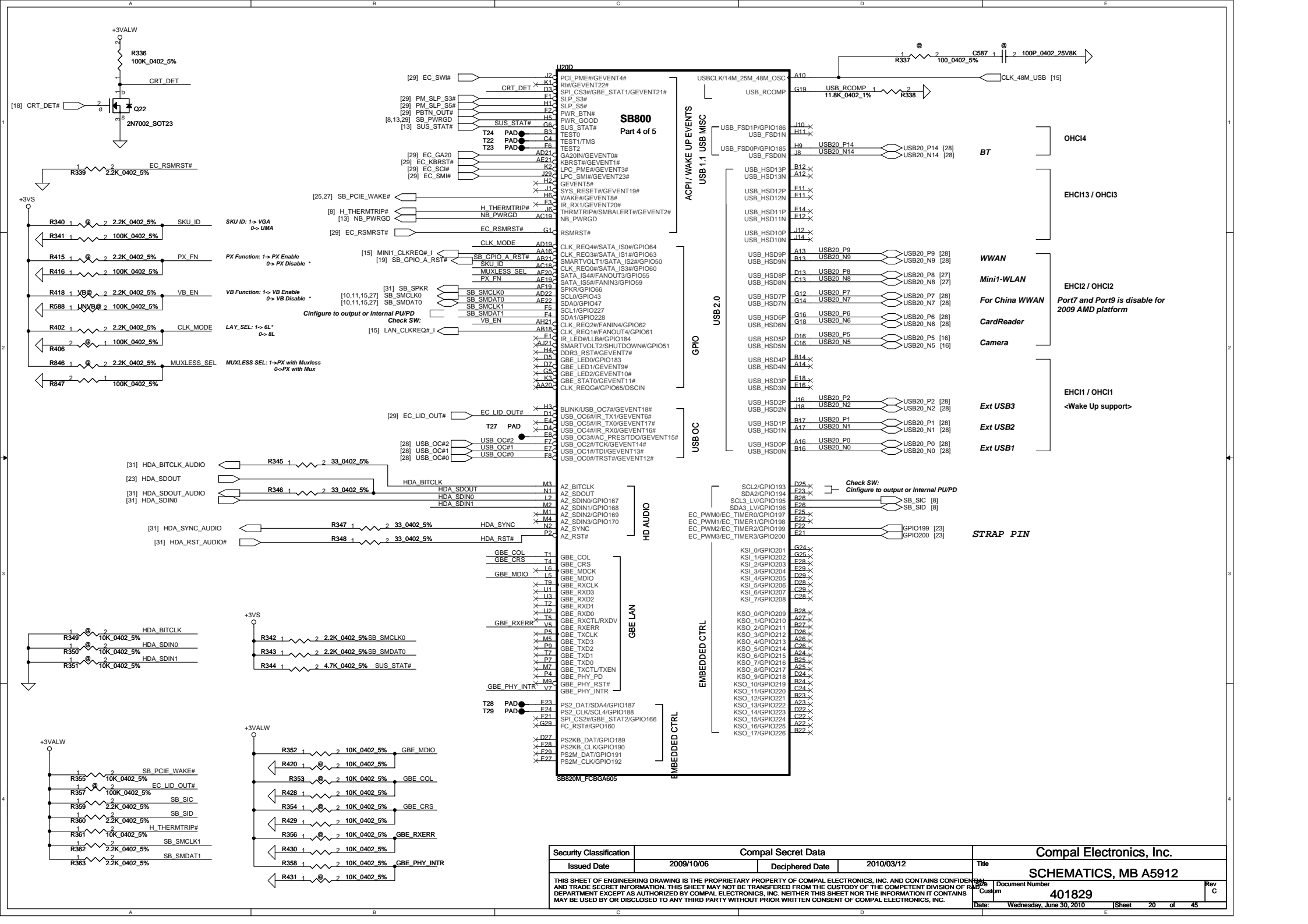
ISL6265 PWROK input, TTL level: 0.8V-2.0V
 When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high



AMD suggest add GPIO control gate

PCI AD24 : VDDR Voltage SW

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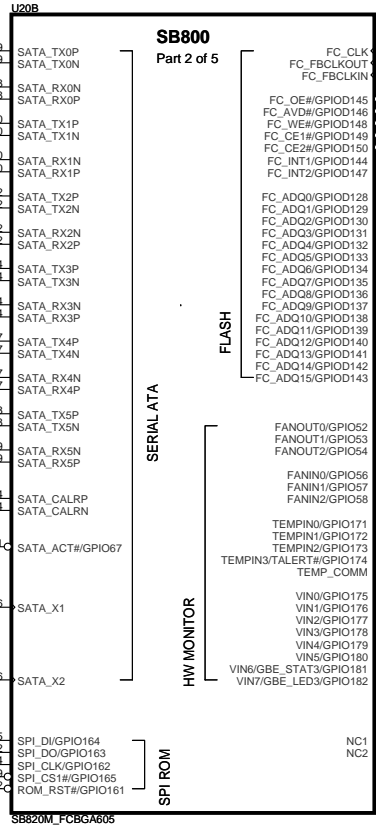
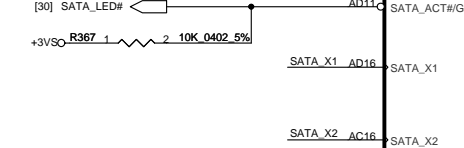
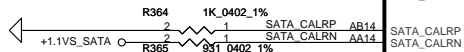
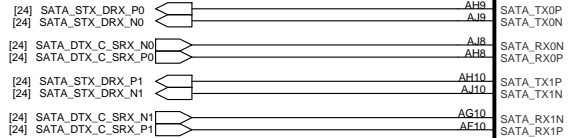


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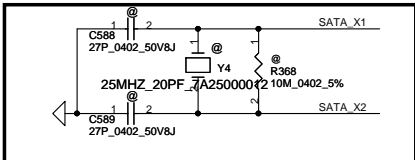
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HDD

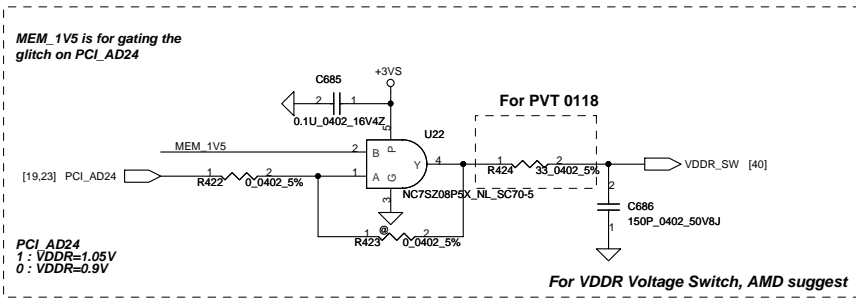
ODD



SB820 A12(SA000031W10)



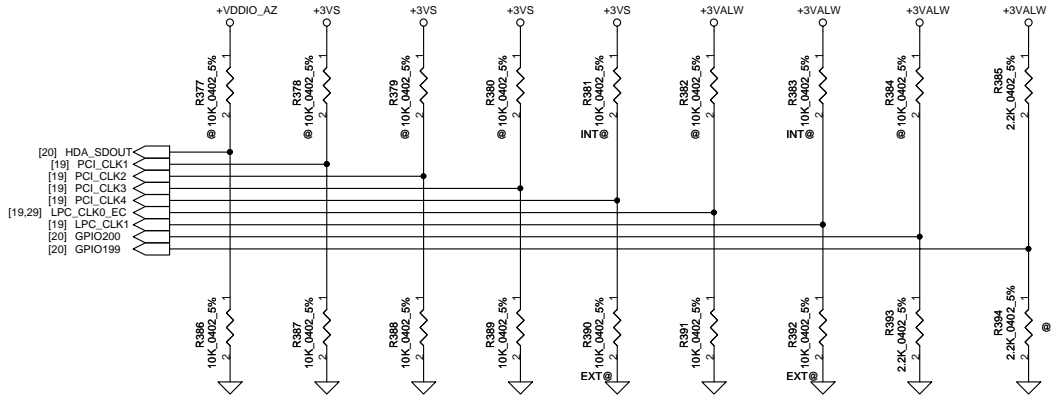
AMD Suggest Unpop Y4 For DVT 11/17



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REQUIRED STRAPS

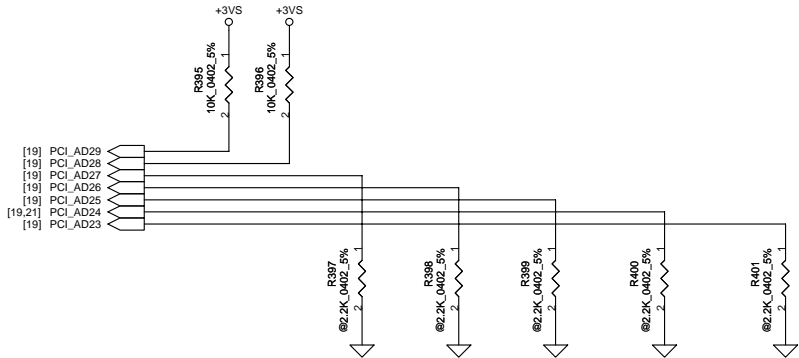
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1		GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved H,L = SPI ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Disable	EC DISABLE	CLOCKGEN DISABLE		L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT			



DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

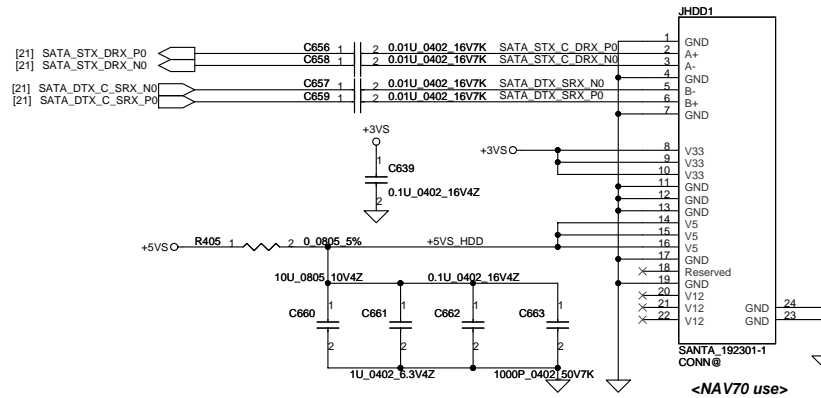
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT



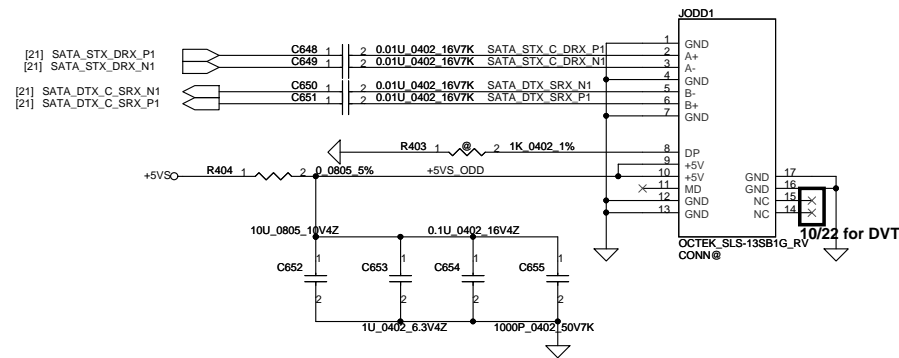
Check AD29,AD28 strap function

check default

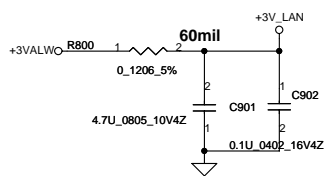
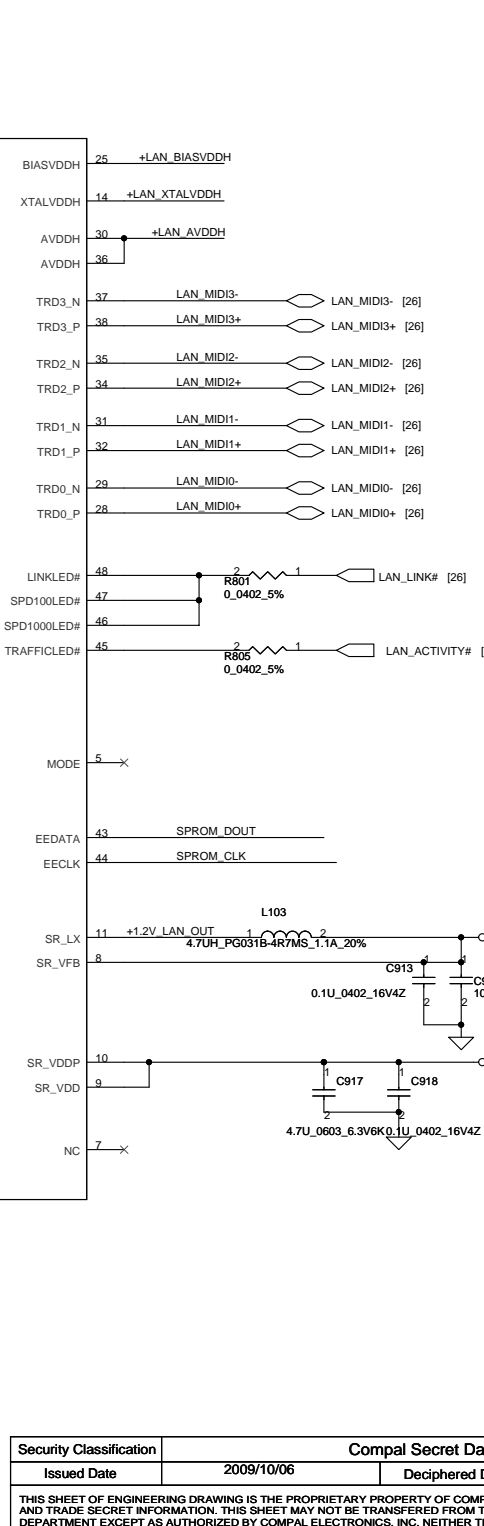
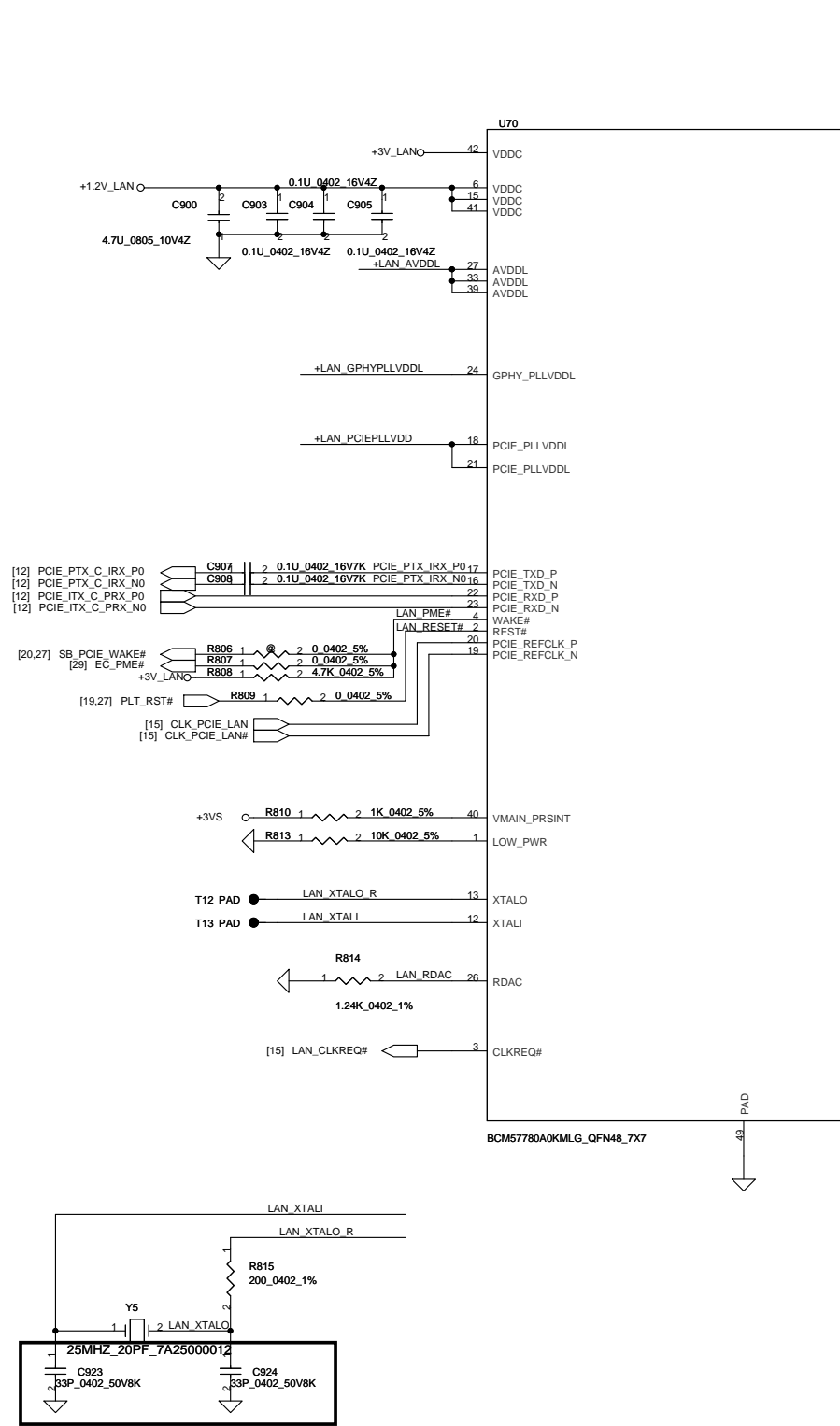
SATA HDD Conn.



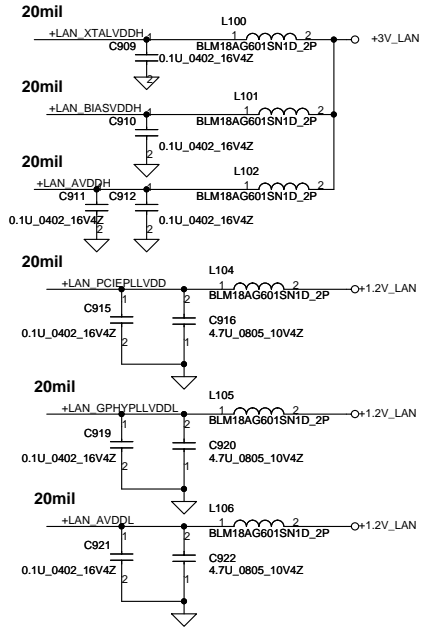
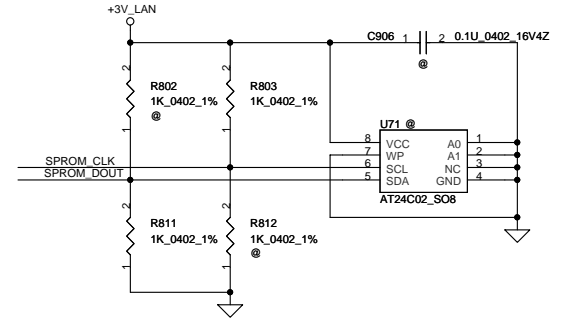
SATA ODD Conn.



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	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
on chip	1	0
AT24C02	1	1



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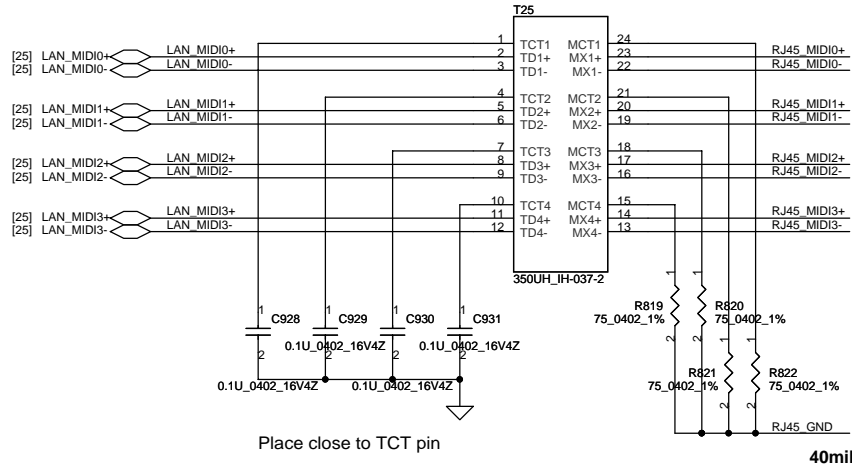
SHEMATICS, MB A5912

Document Number: 401829

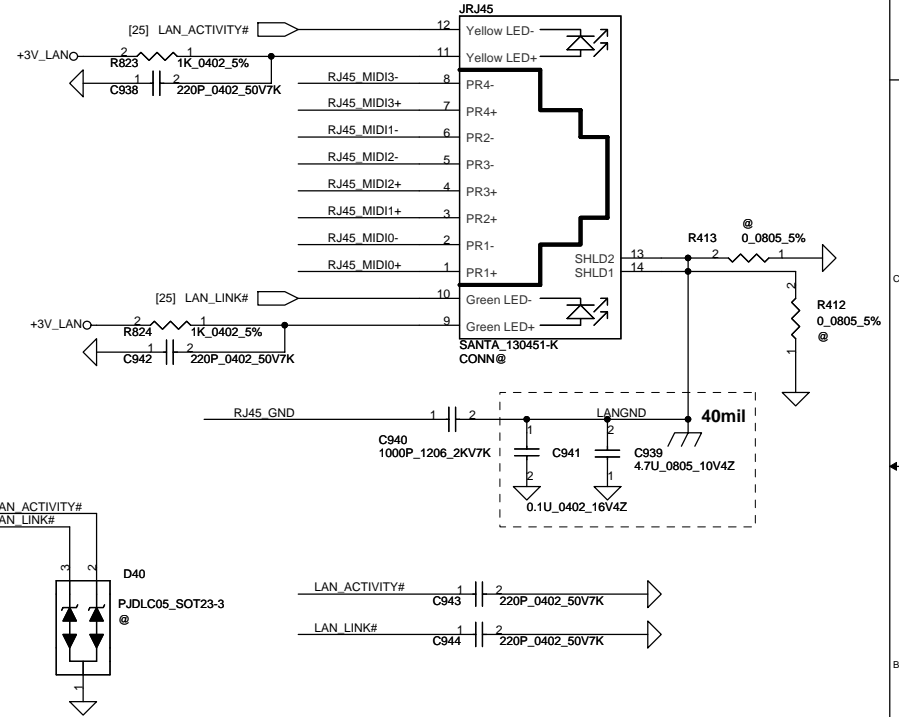
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BH GS5009-D <SP050006B00>

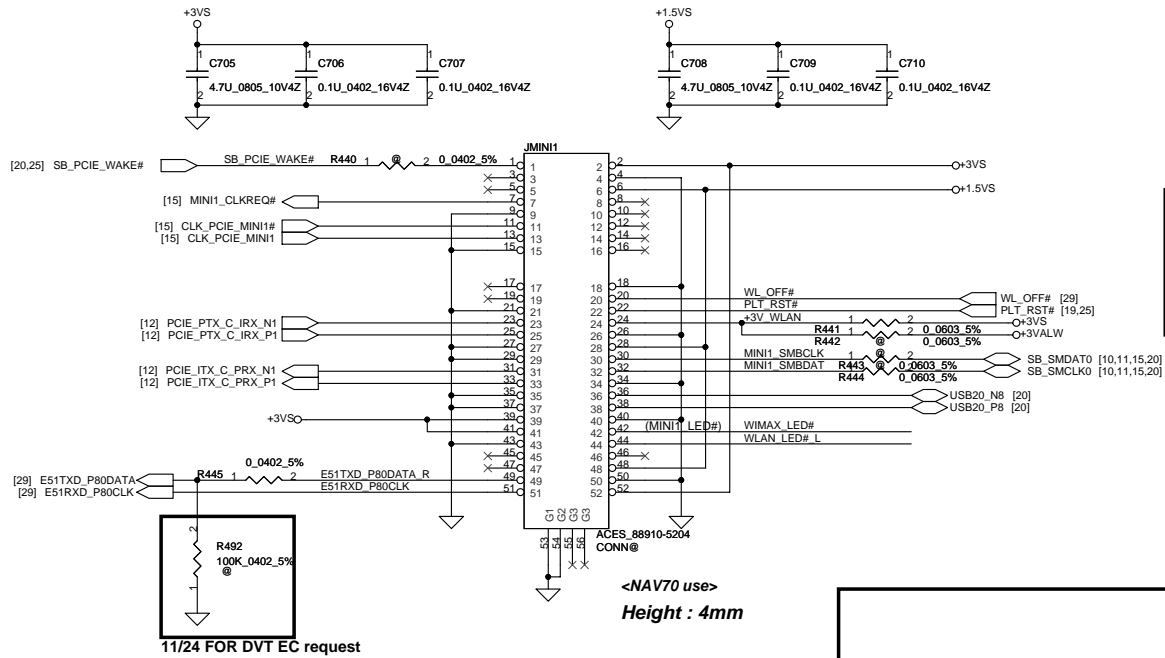


LAN Connector



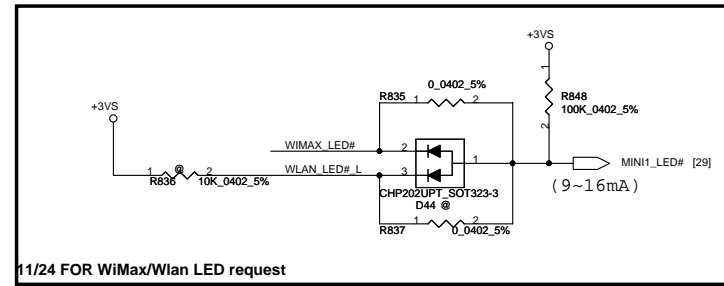
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Mini-Express Card for WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

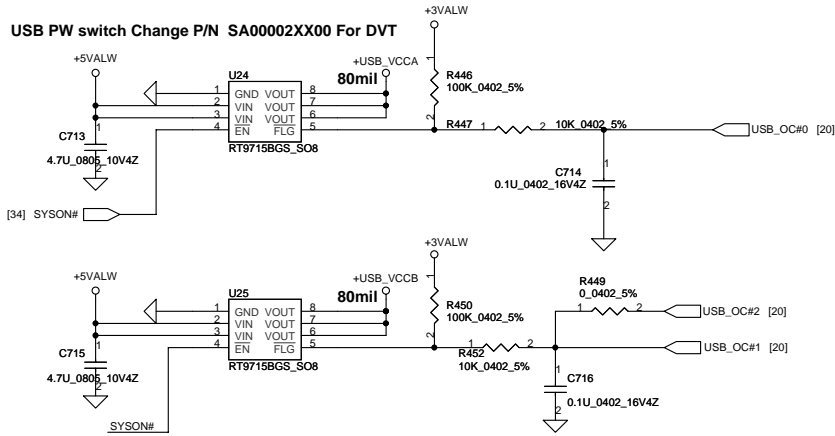
11/24 FOR DVT EC request



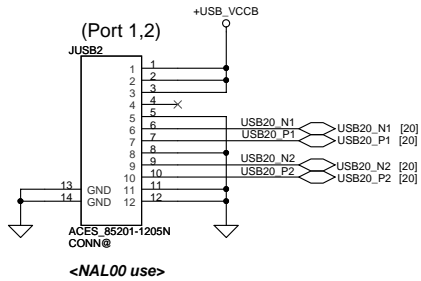
11/24 FOR WiMax/Wlan LED request

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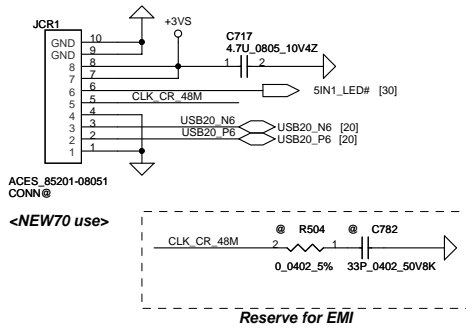
USB PW switch Change P/N SA00002XX00 For DVT



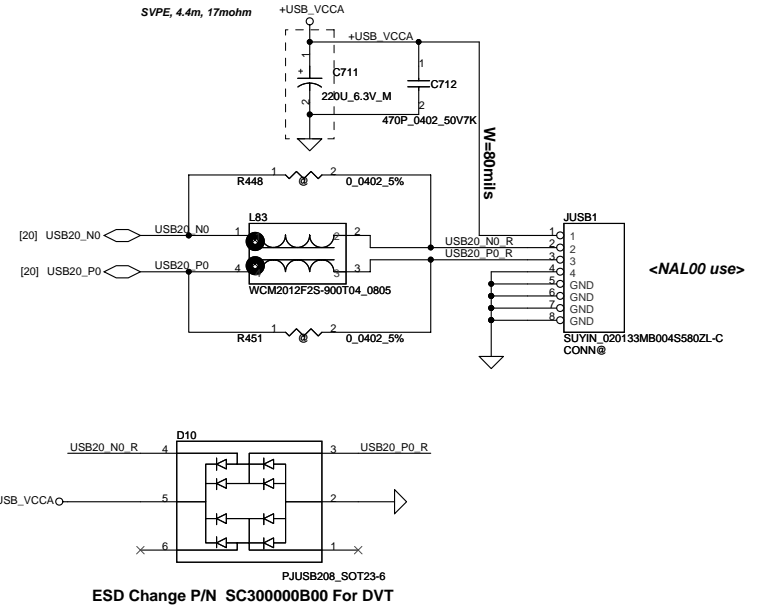
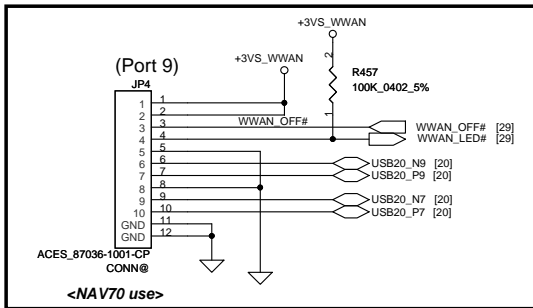
To USB/B Connector



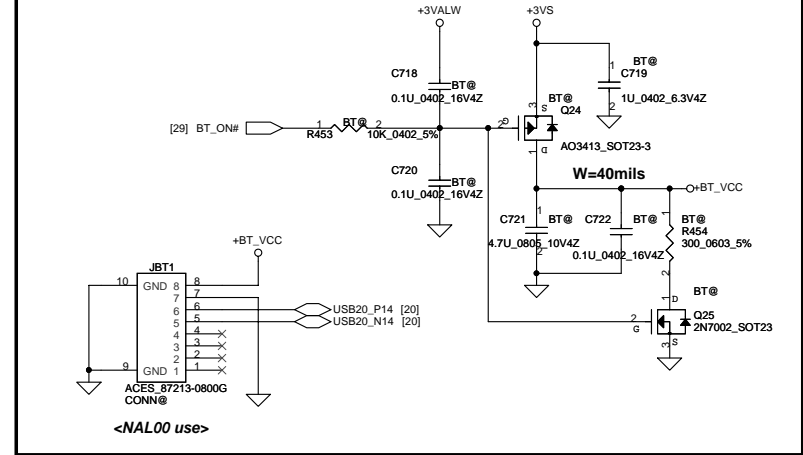
To CardReader/B Connector



To 3G Module Connect

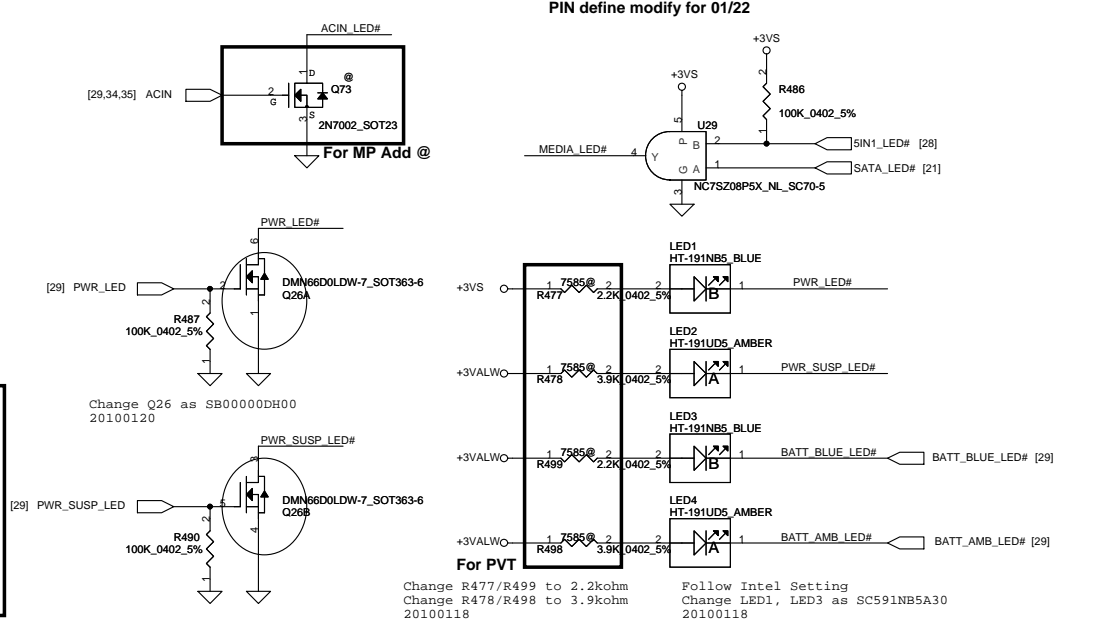
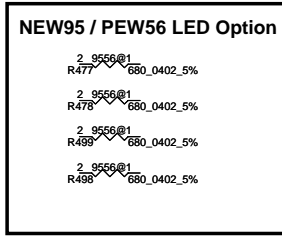
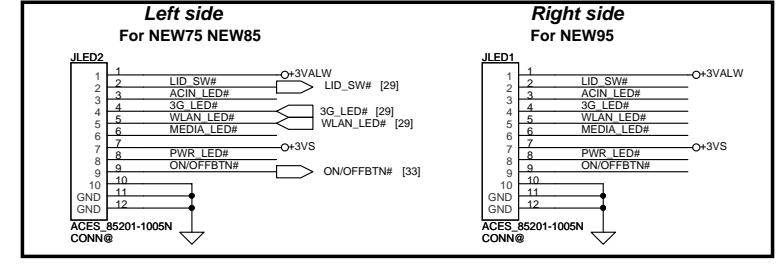
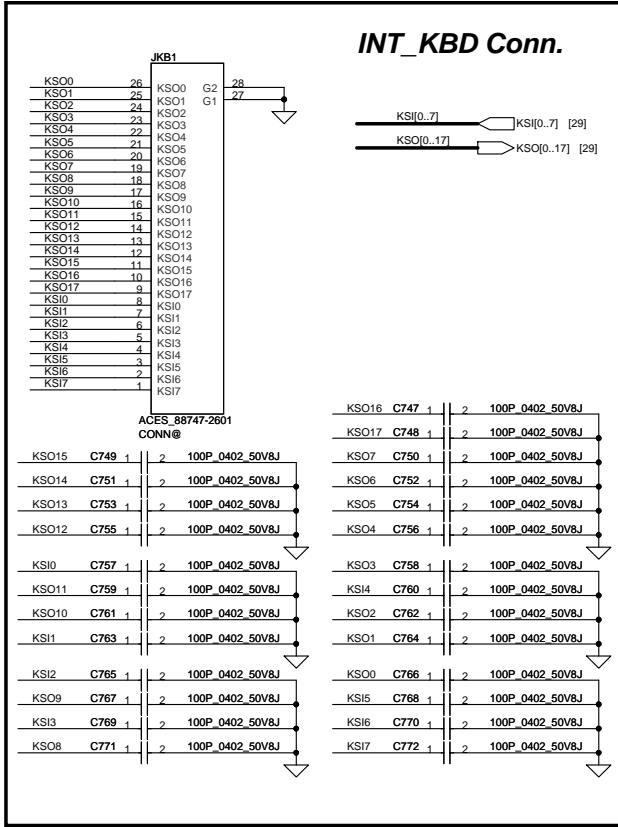
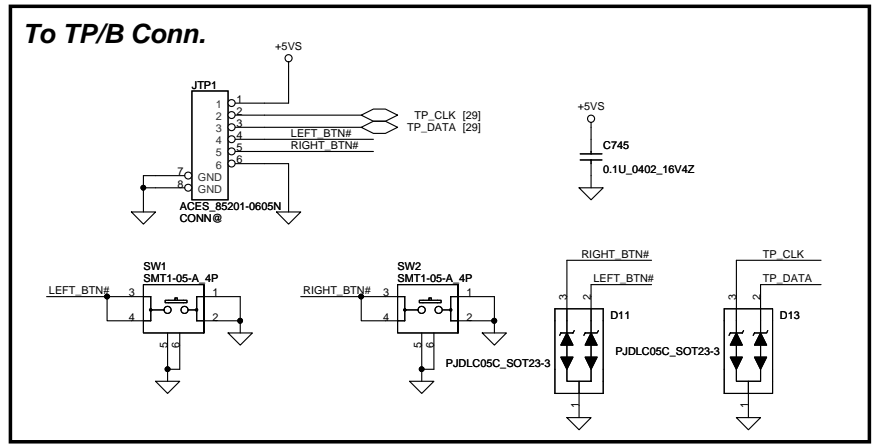
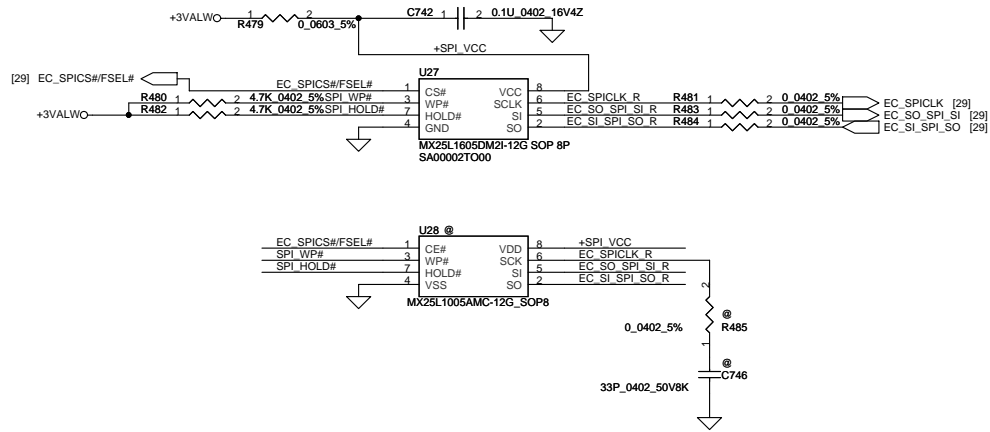


Bluetooth Conn.

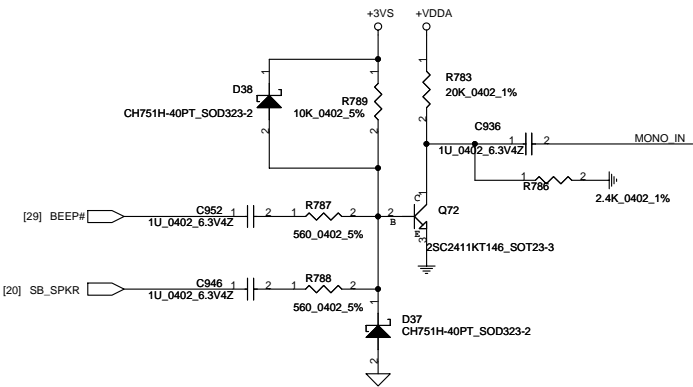


11/25 for DVT

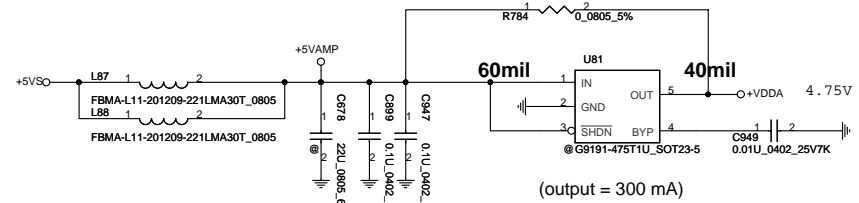
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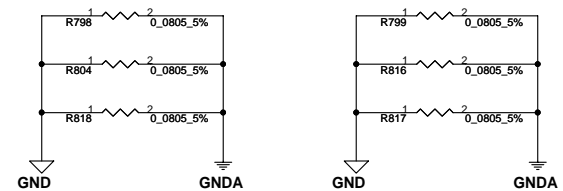
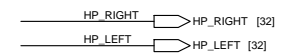
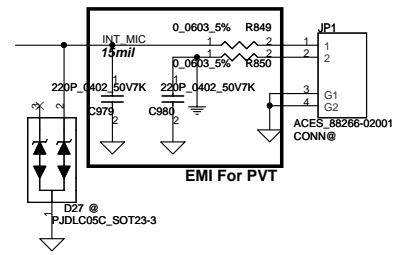
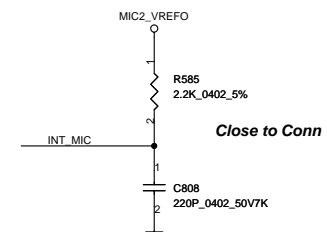
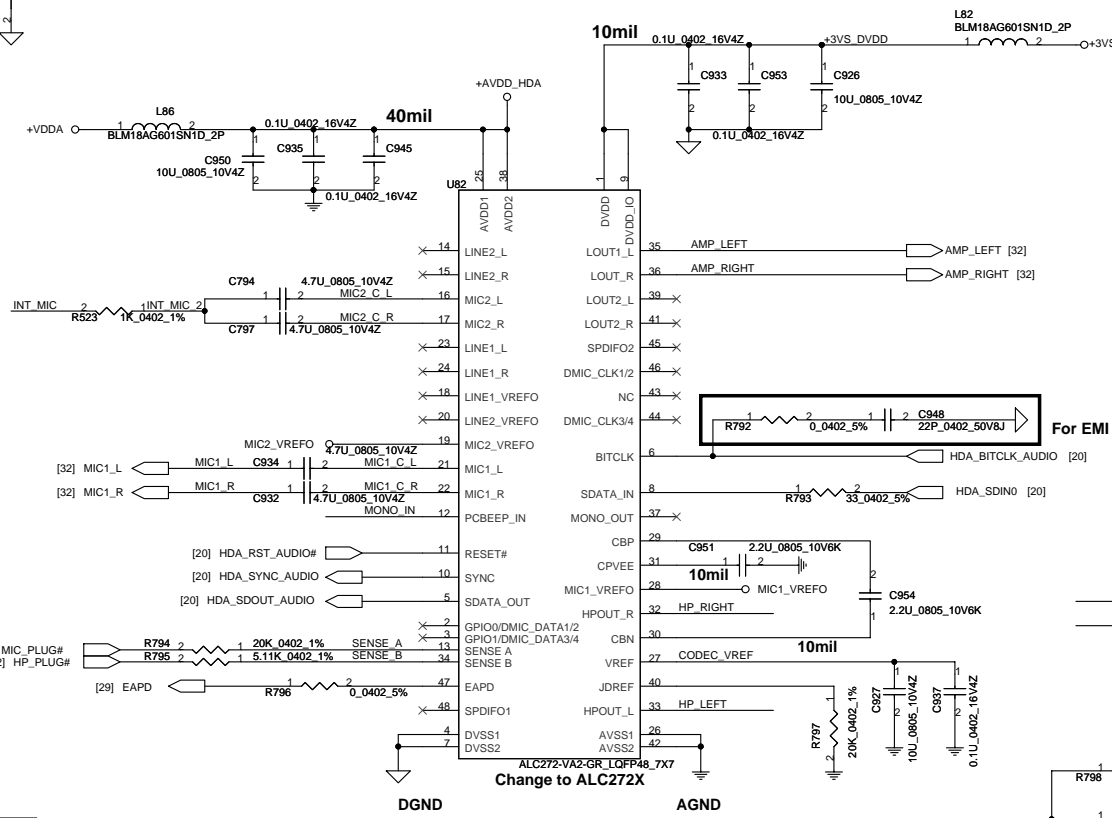
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HD Audio Codec



(output = 300 mA)

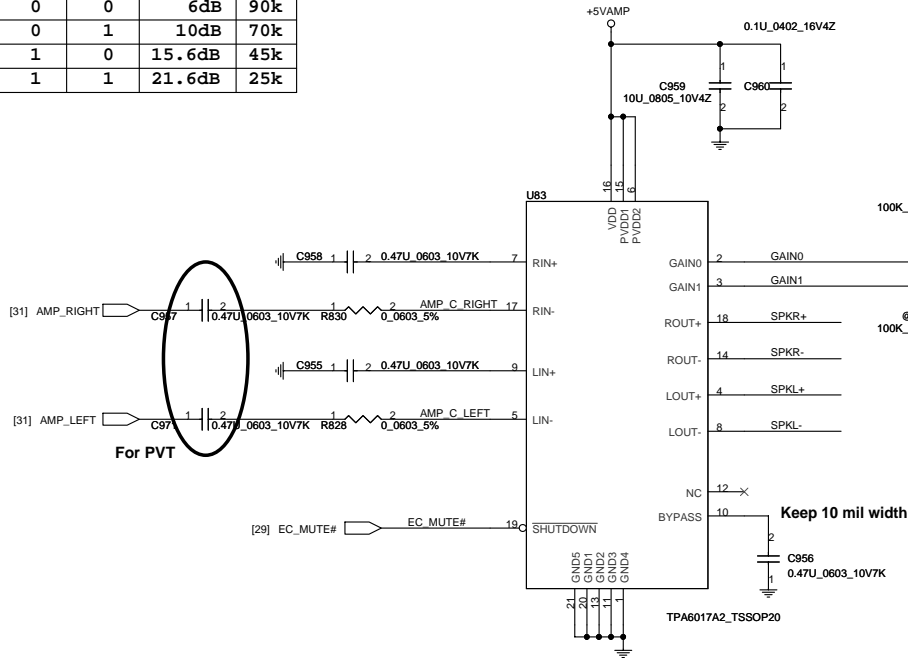


ALC272X			
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K	PORT-I (PIN 32, 33)	HP

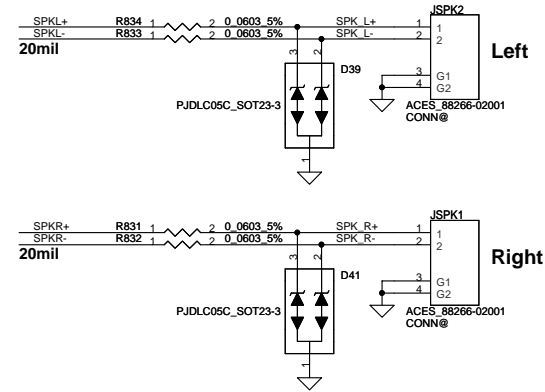
Change to ALC272X

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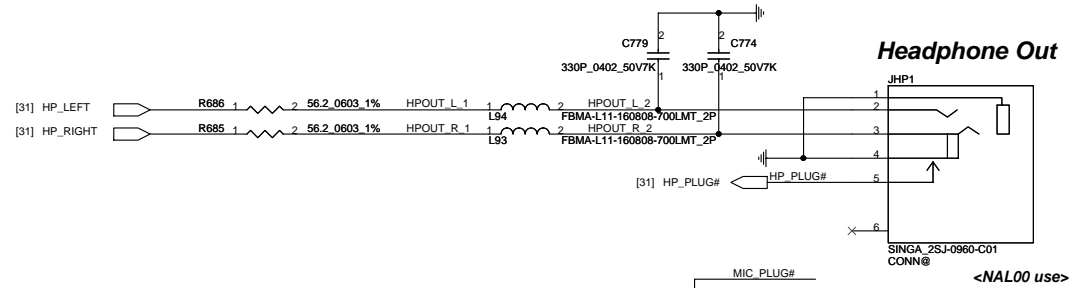
GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



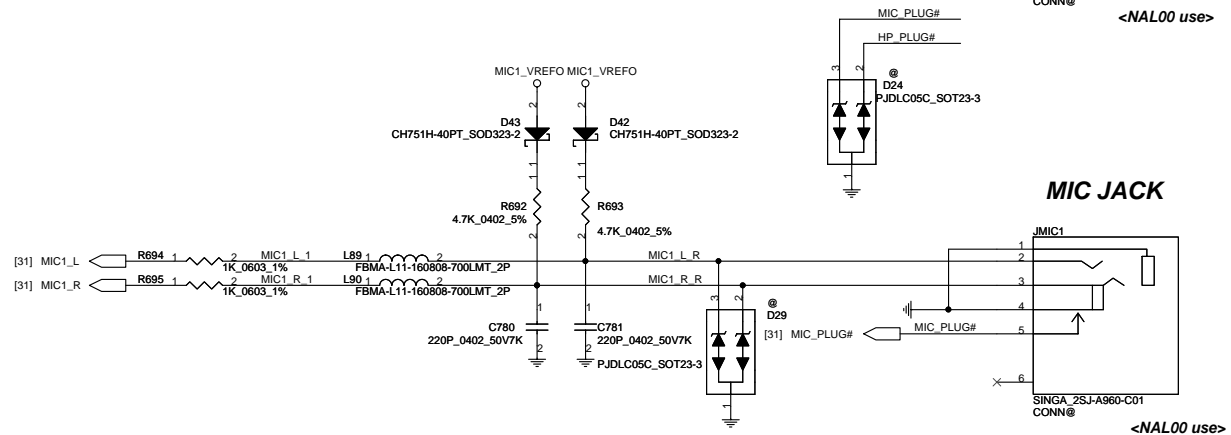
Int. Speaker Conn.



Headphone Out



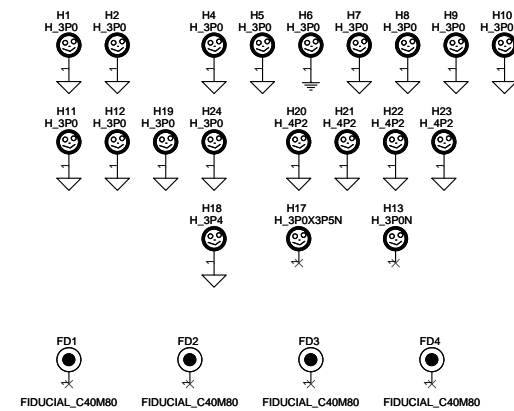
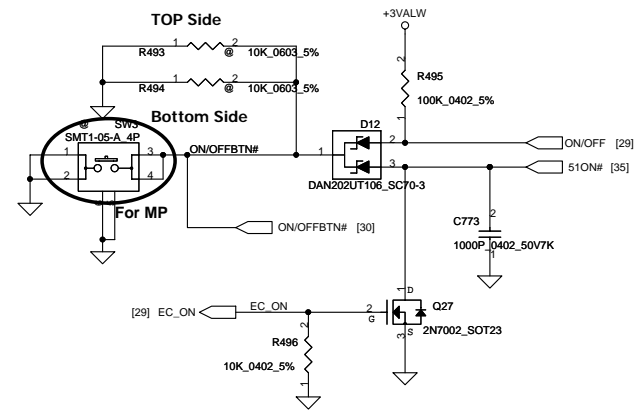
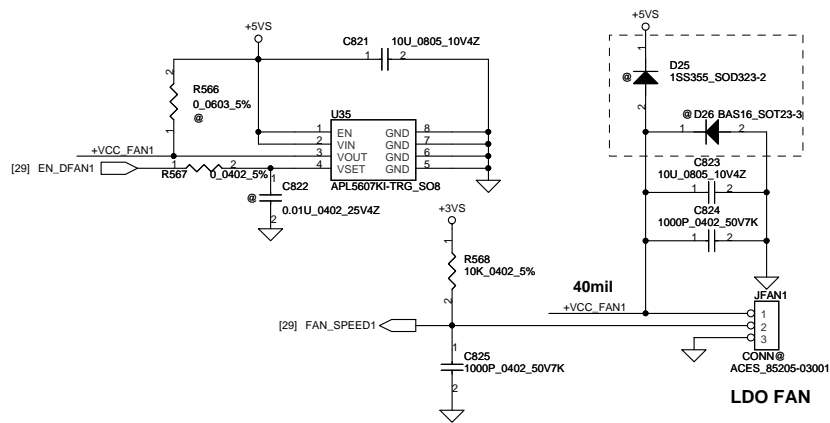
MIC JACK



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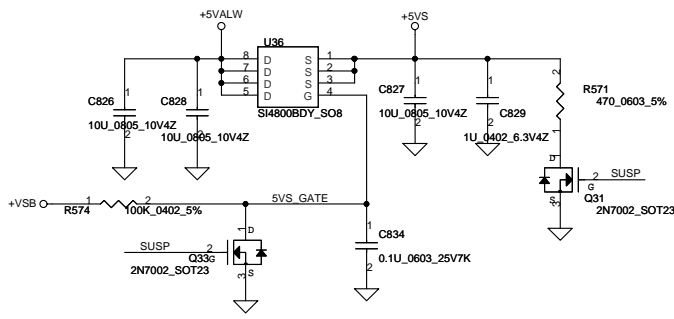
ON/OFF switch **Power Button**

FAN1 Conn

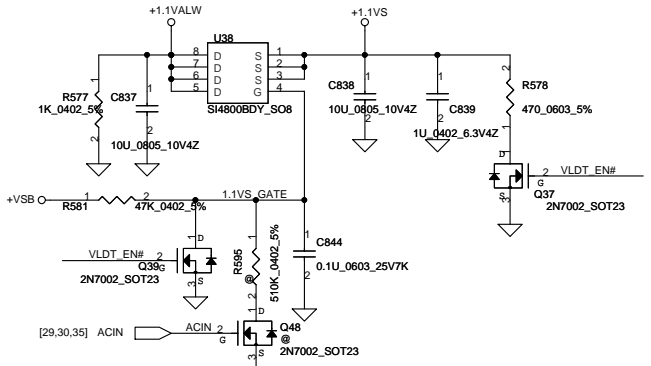


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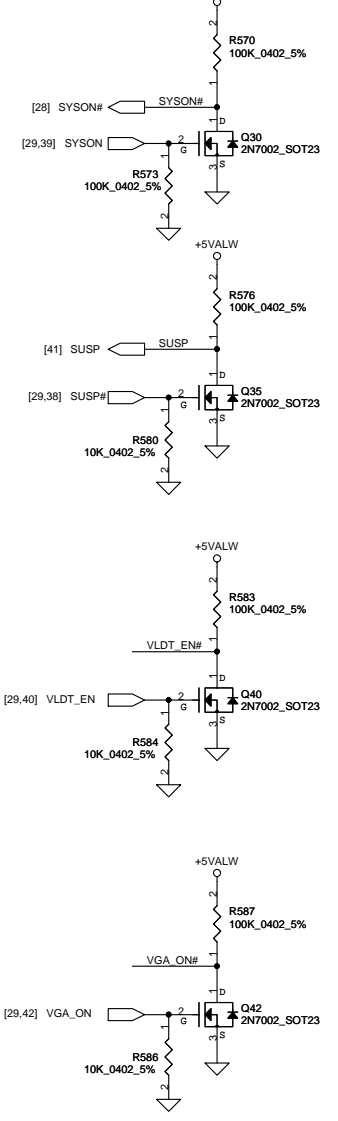
+5VALW TO +5VS



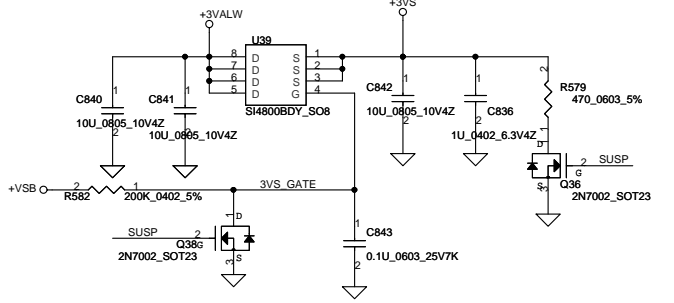
+1.1VALW TO +1.1VS



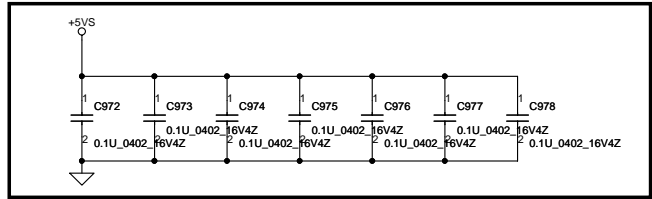
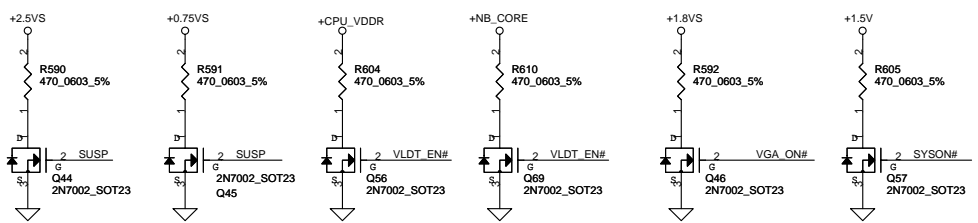
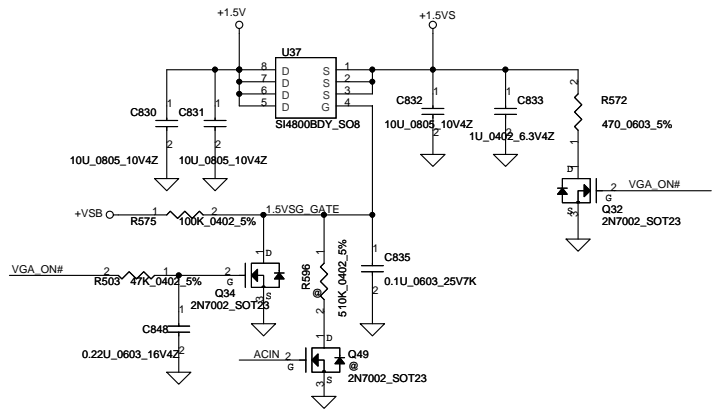
+5VALW



+3VALW TO +3VS



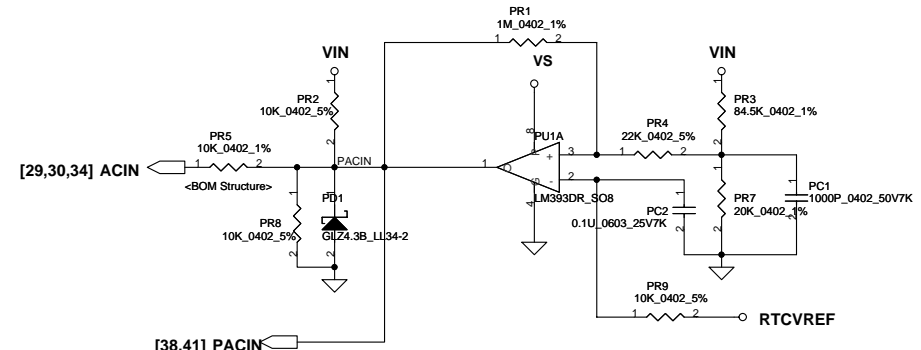
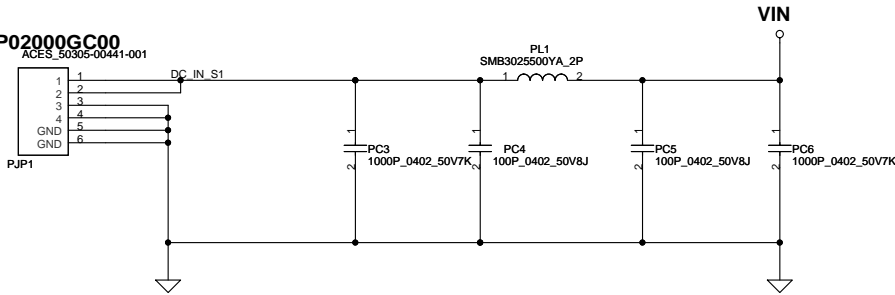
+1.5V to +1.5VS



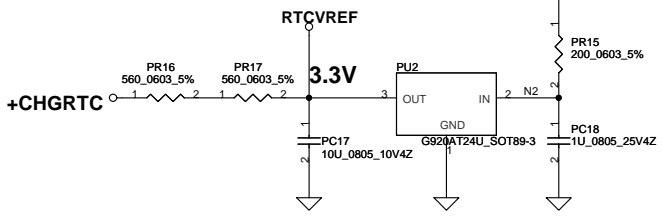
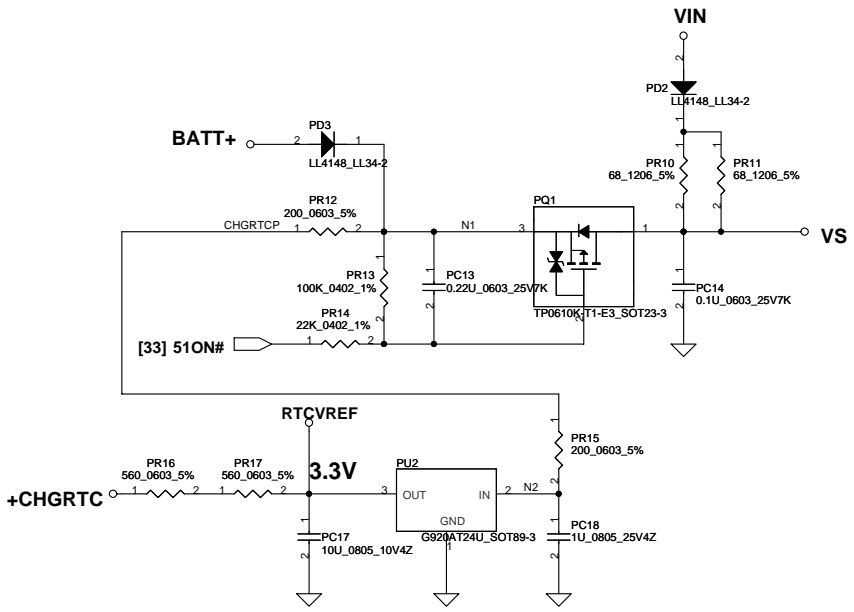
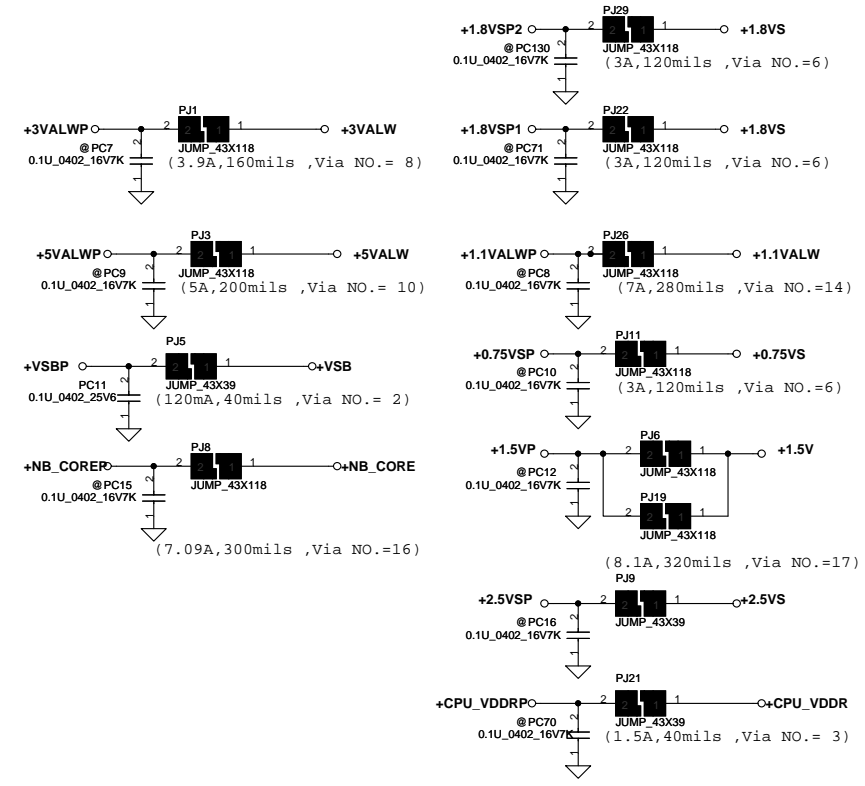
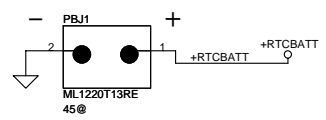
11/26 DVT for EMI request

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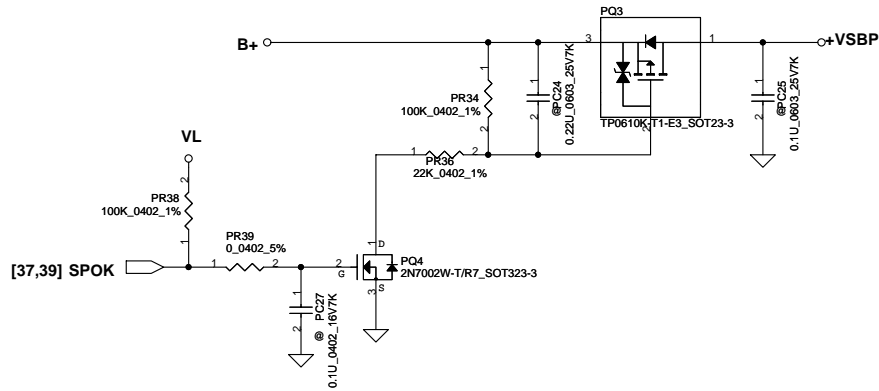
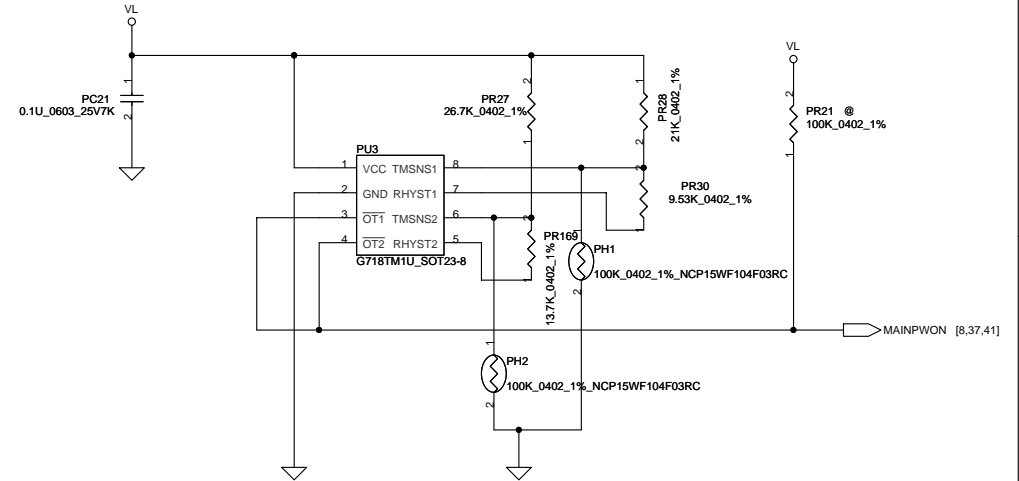
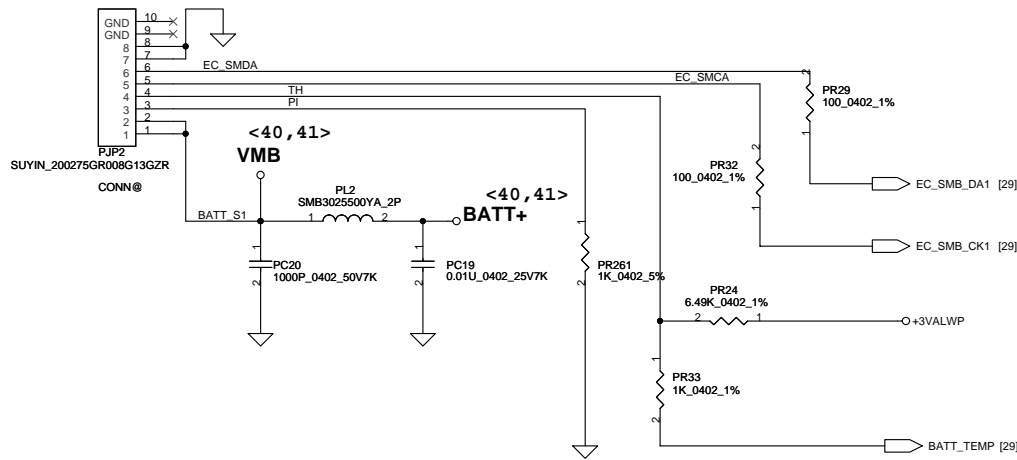


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

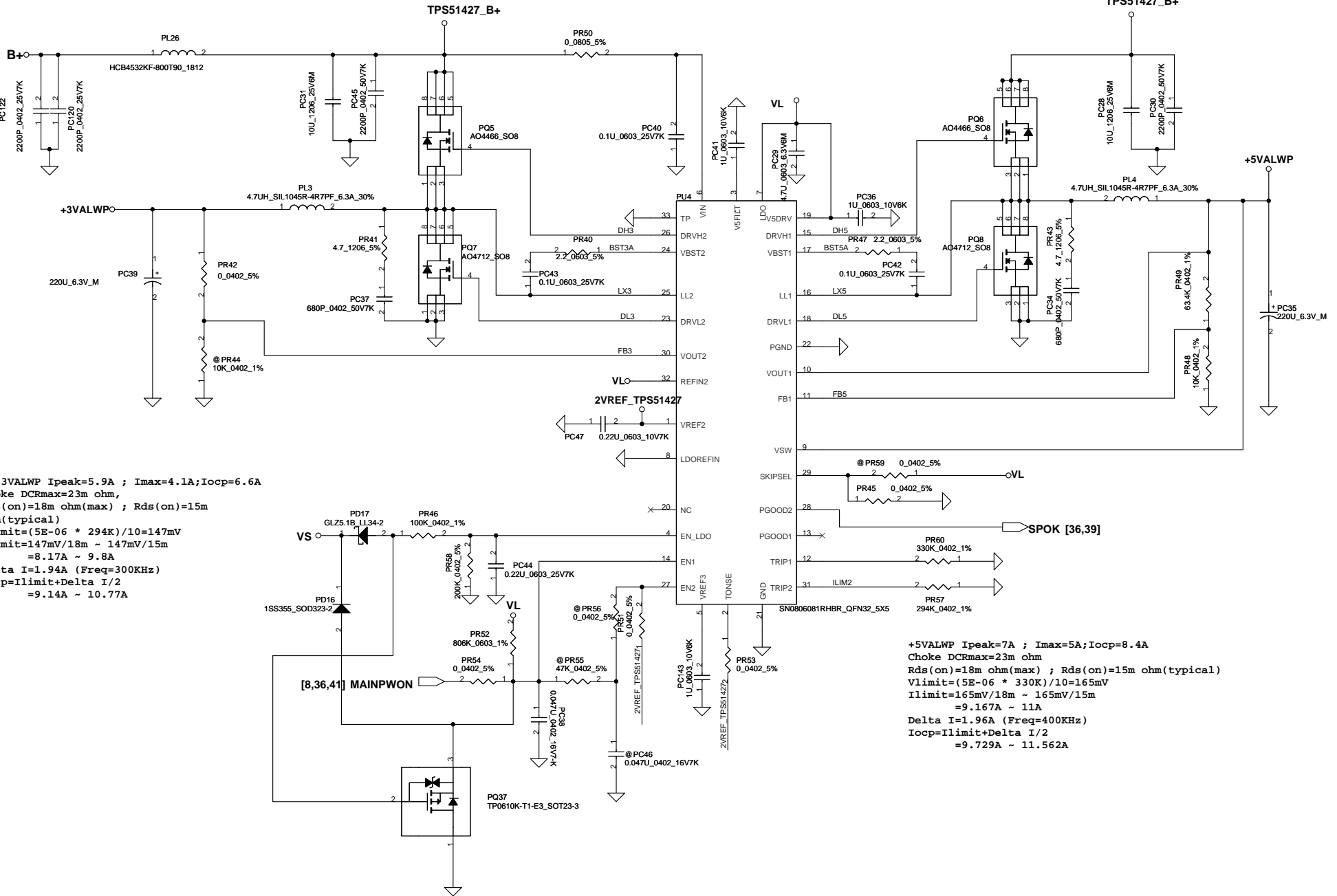


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PH1 thermal protection at 92 degree C Recovery at 56 degree C
 PH2 thermal protection at 85 degree C Recovery at 56 degree C



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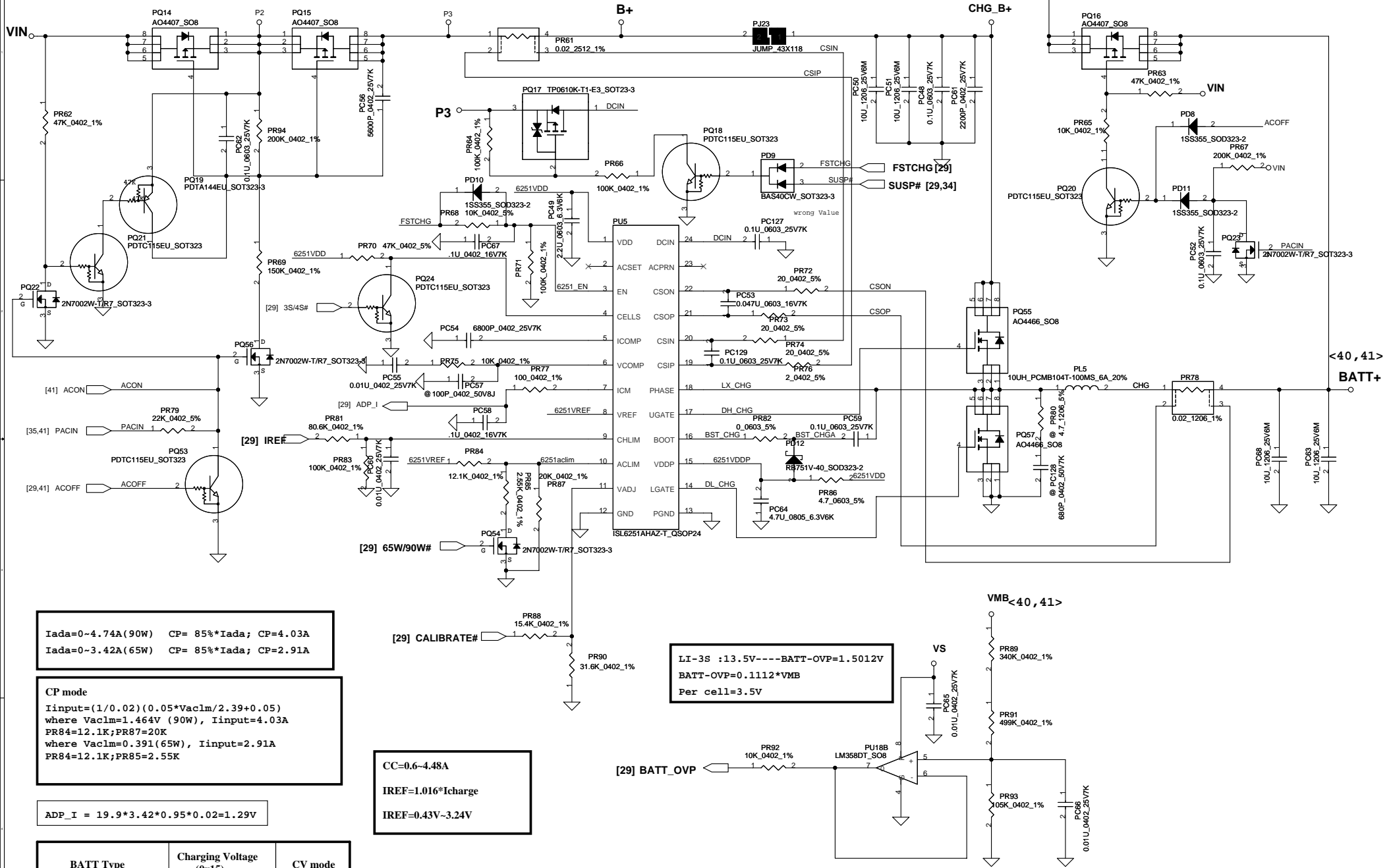
+3.3VALWP Ipeak=5.9A ; Imax=4.1A;Iocp=6.6A
 Choke DCRmax=23m ohm,
 Rds(on)=18m ohm(max) ; Rds(on)=15m
 ohm(typical)
 $V_{limit} = (5E-06 * 294K) / 10 = 147mV$
 $I_{limit} = 147mV / 18m \sim 147mV / 15m$
 $= 8.17A \sim 9.8A$
 $\Delta I = 1.94A$ (Freq=300KHz)
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 9.14A \sim 10.77A$

+5VALWP Ipeak=7A ; Imax=5A;Iocp=8.4A
 Choke DCRmax=23m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$
 $\Delta I = 1.96A$ (Freq=400KHz)
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 9.729A \sim 11.562A$

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Iada=0-4.74A(90W/19V=4.736A)

$CP = 85\% * Iada ; CP = 4.03A$



Iada=0-4.74A(90W) CP= 85%*Iada; CP=4.03A
 Iada=0-3.42A(65W) CP= 85%*Iada; CP=2.91A

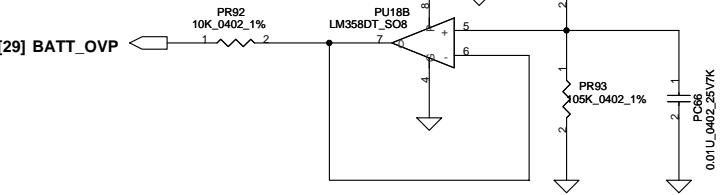
CP mode
 $I_{input} = (1/0.02) * (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.464V$ (90W), $I_{input} = 4.03A$
 $PR84 = 12.1K; PR87 = 20K$
 where $V_{ac1m} = 0.391V$ (65W), $I_{input} = 2.91A$
 $PR84 = 12.1K; PR85 = 2.55K$

$ADP_I = 19.9 * 3.42 * 0.95 * 0.02 = 1.29V$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6-4.48A
 IREF=1.016*Icharge
 IREF=0.43V-3.24V

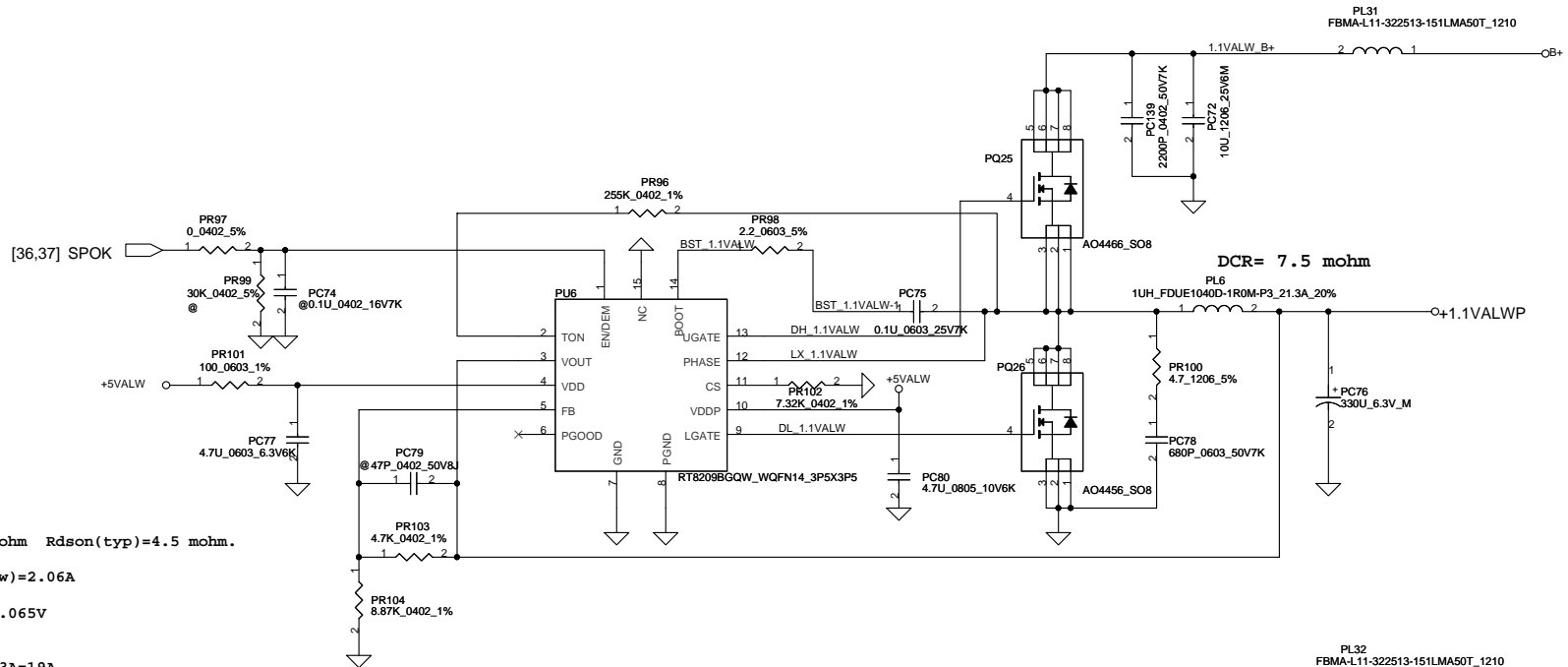
LI-3S :13.5V---BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=3.5V



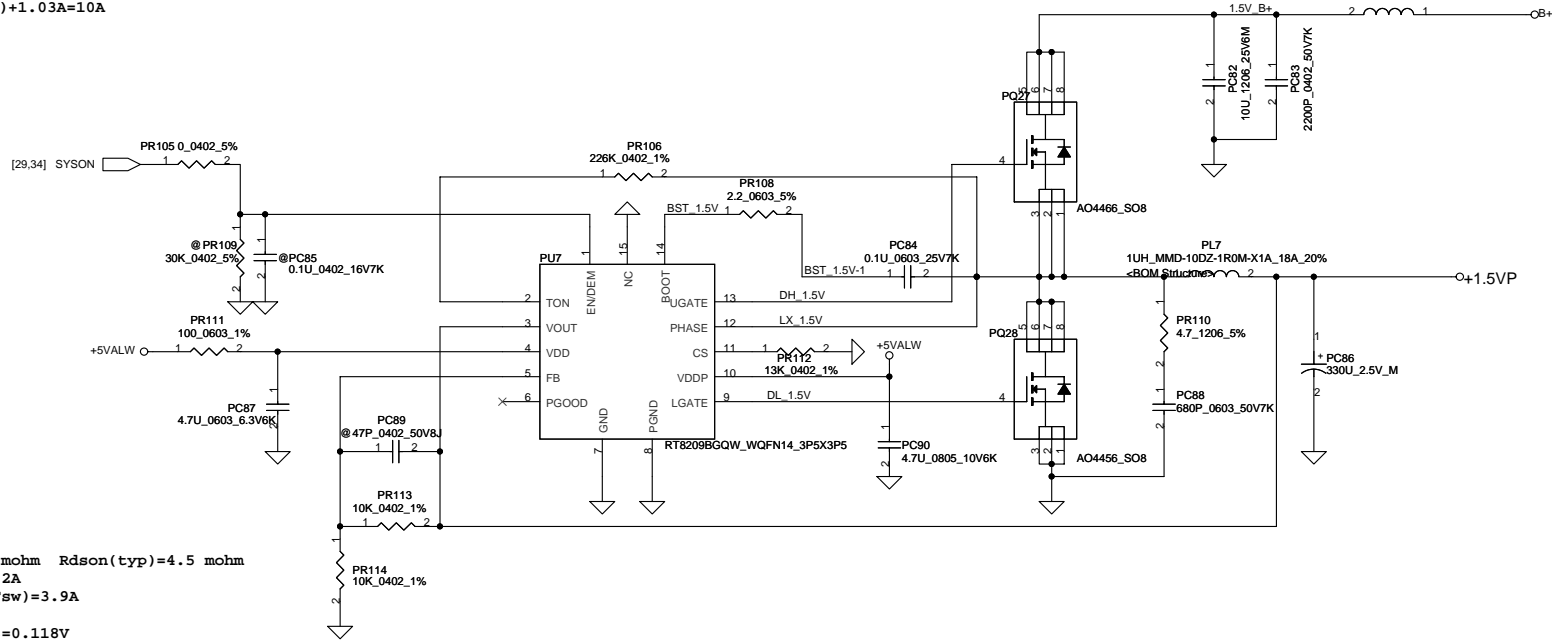
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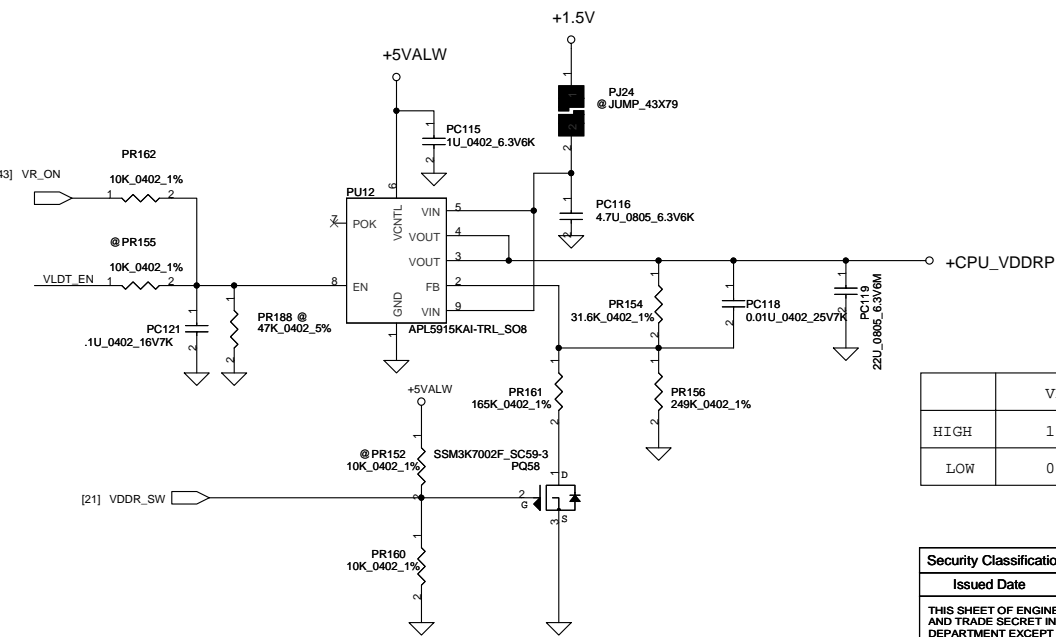
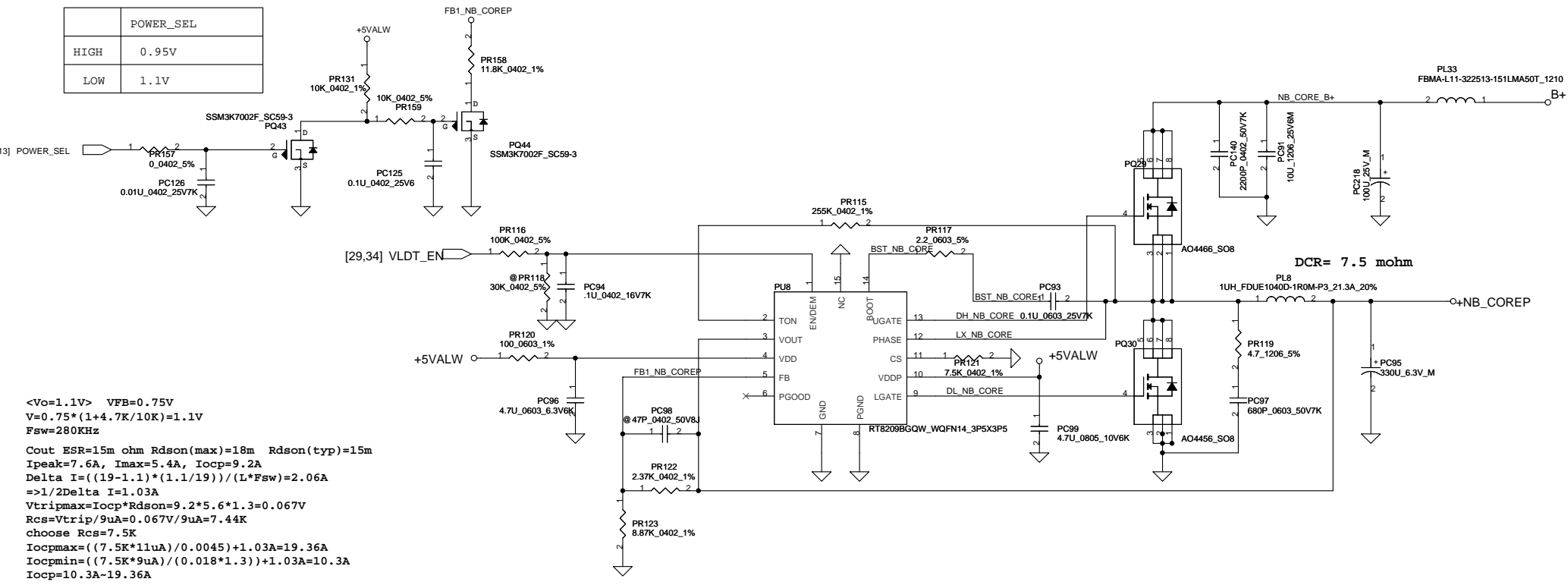
<Vo=1.1V> VFB=0.75V
 V=0.75*(1+4.7K/10K)=1.1V
 Fsw=280KHz
 Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
 Ipeak=7.42A, Imax=5.2A, Iocp=8.9A
 Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
 =>1/2Delta I=1.03A
 Vtripmax=Iocp*Rdson=8.9*5.6*1.3=0.065V
 Rcs=Vtrip/9uA=0.065V/9uA=7.2K
 choose Rcs=7.32K
 Iocpmax=((7.32K*11uA)/0.0045)+1.03A=19A
 Iocpmin=((7.32K*9uA)/(0.0056*1.3))+1.03A=10A
 Iocp=10A-19A



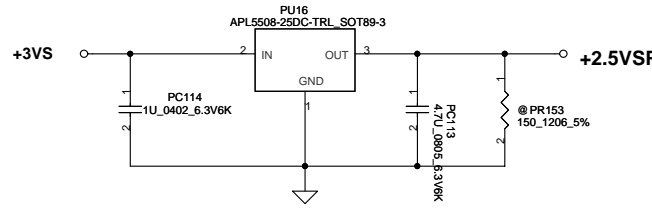
<Vo=1.5V> VFB=0.75V
 Vo=0.75*(1+10K/10K)=1.5V
 Fsw=335KHz
 Cout ESR=17 mohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm
 Ipeak=13.5A, Imax=9.5A, Iocp=16.2A
 Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
 =>1/2Delta I=1.95A
 Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
 Rcs=Vtrip/9uA=0.118V/9uA=13.1K
 choose Rcs=13K
 Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
 Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
 Iocp=18A-32A

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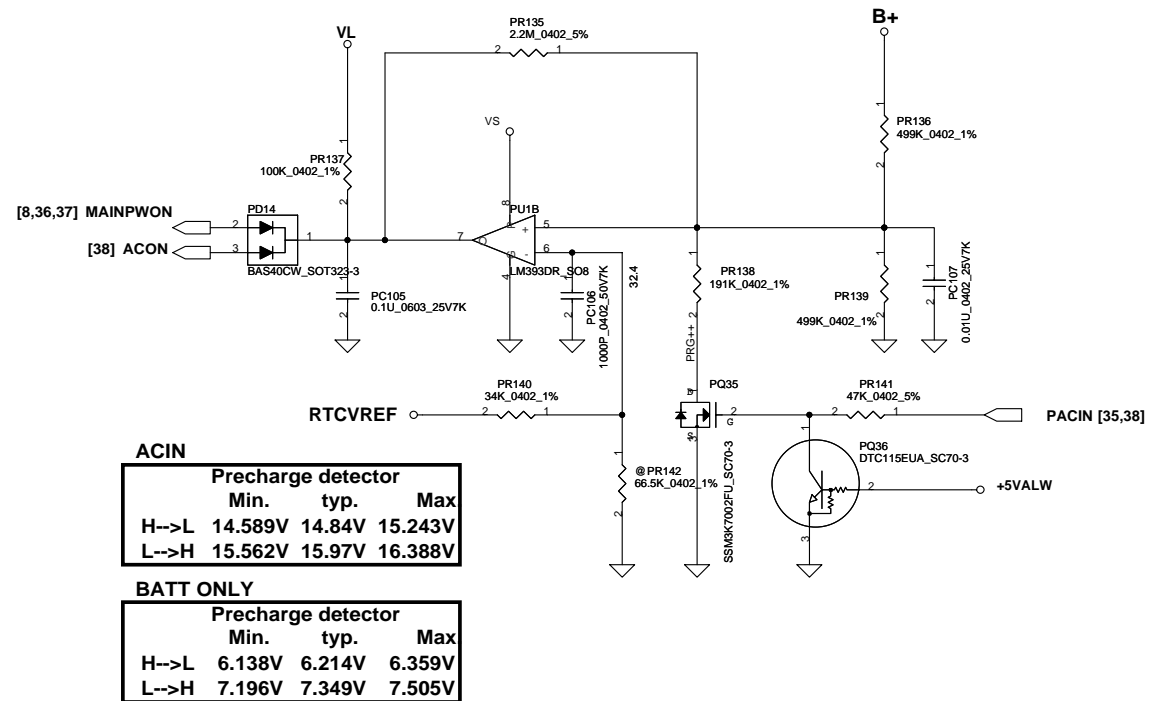
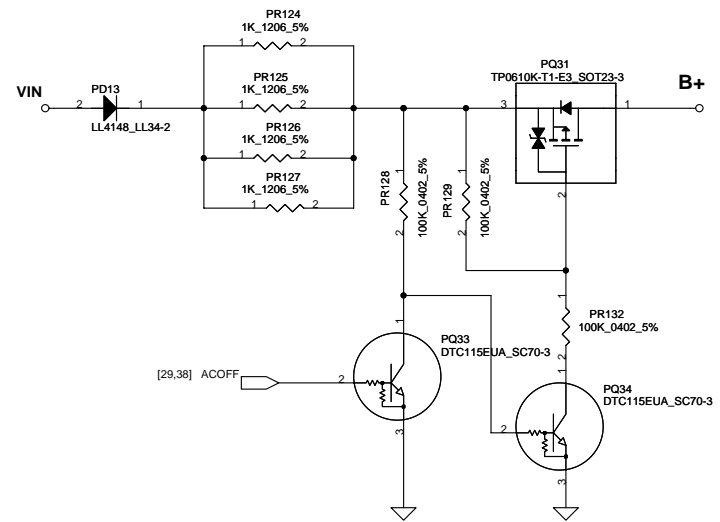
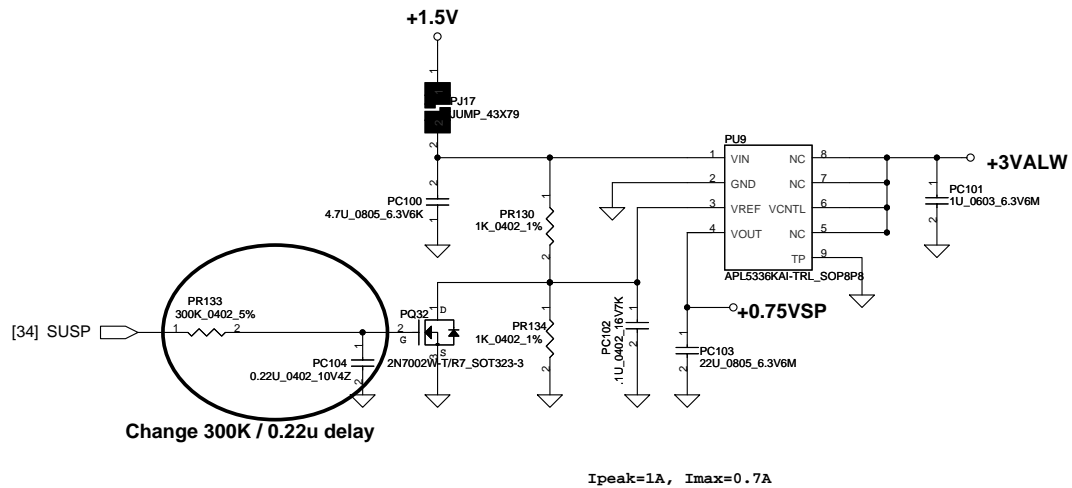
	POWER_SEL
HIGH	0.95V
LOW	1.1V



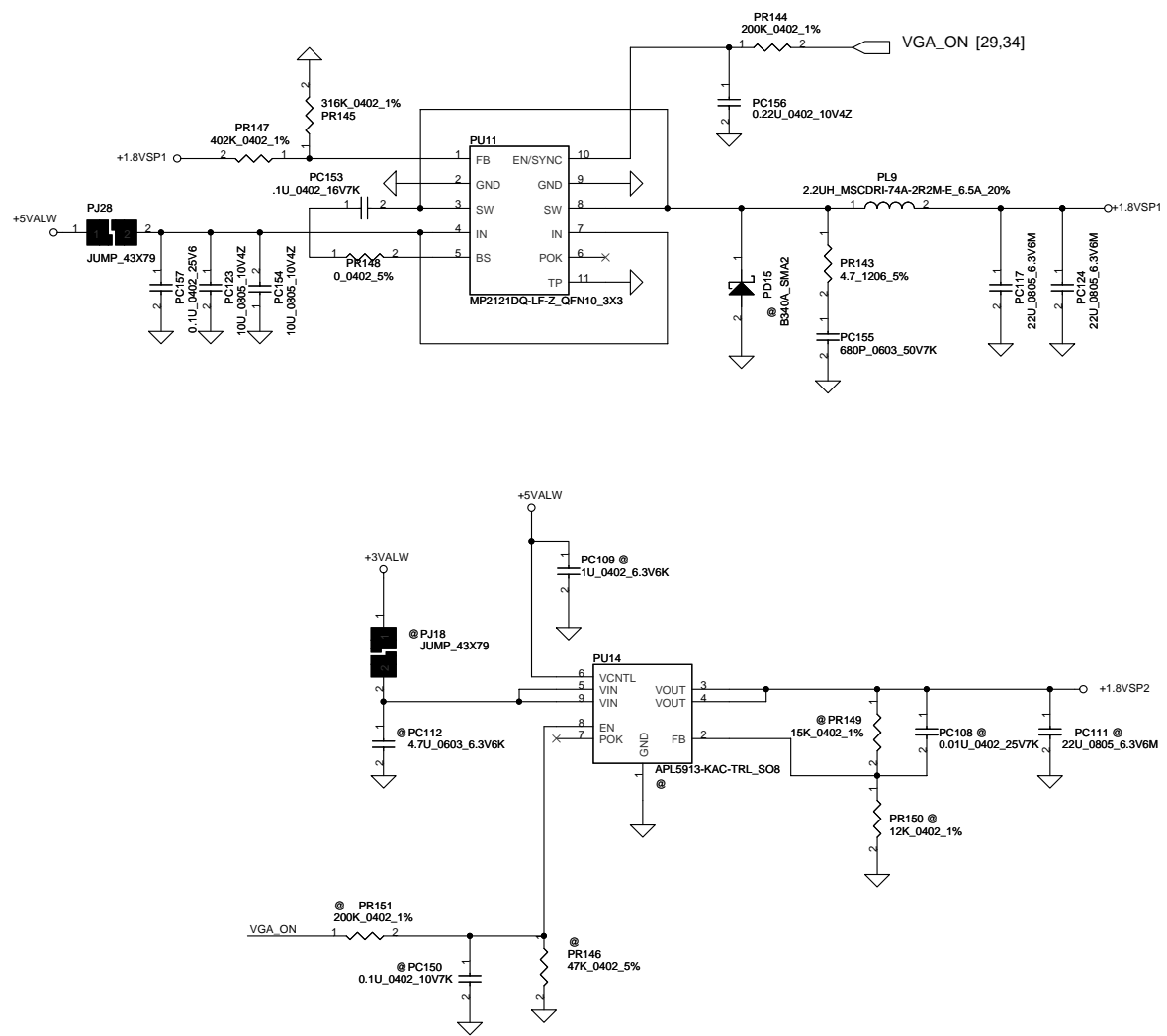
	VDDR_SW
HIGH	1.05V
LOW	0.9V



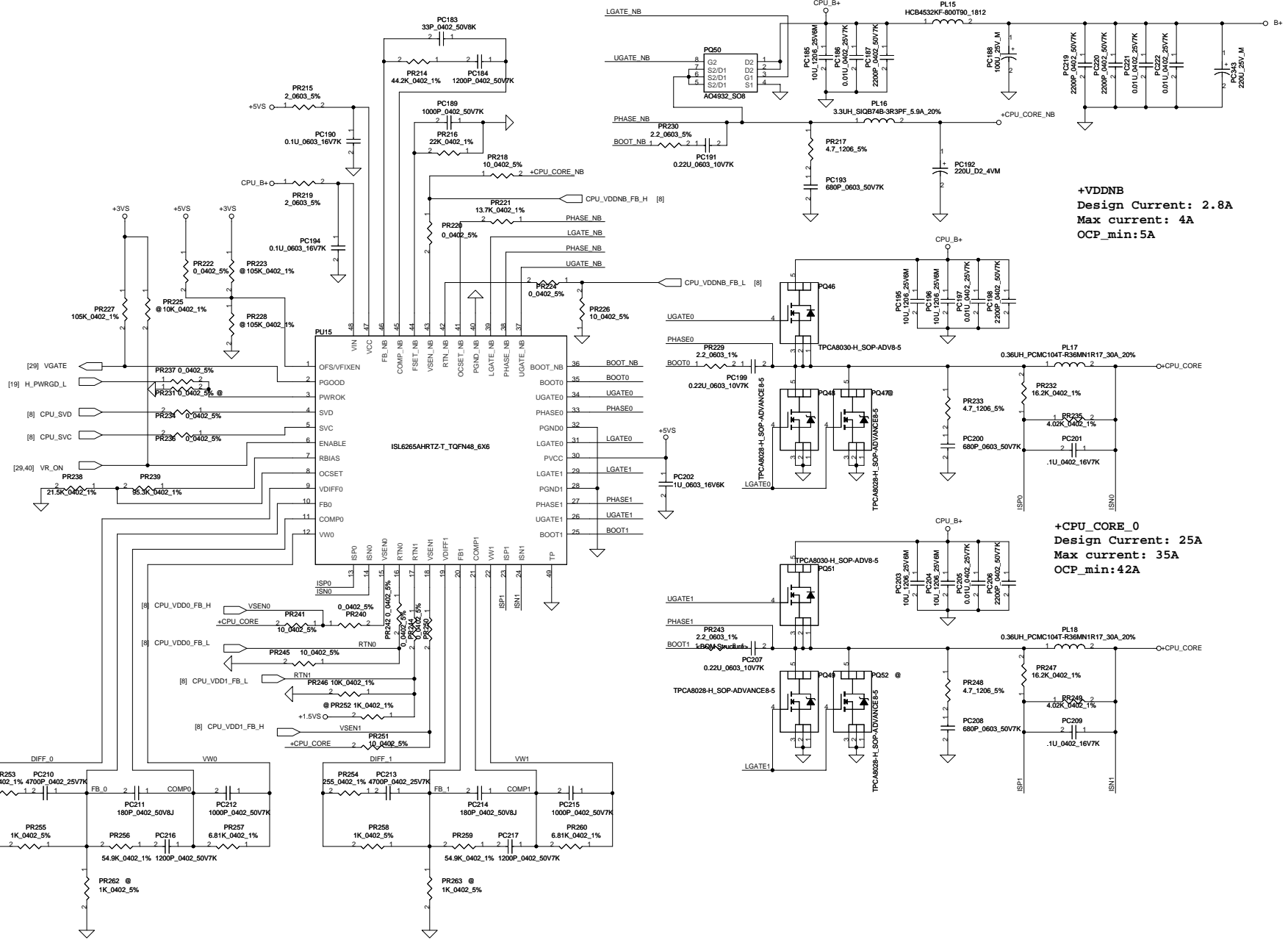
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD 2 switch mos and remove 2 pull high resistance to modify VGA_CORE switch level	Before modify to fault, we recognize that VGAPWRSEL pin is open drain state. But after check with AMD AE regoer to clear the foul that VGAPWRSEL pin has driving ability,so i take away 2 pull high resistance and add 2 switch mos to modify the switch level.	0.1	52	ADD PQ60 and PQ61 remove PR212(10K,0402) and PR213(10K.0402)	2009/08/21	EVT_NAV71
2	change thermister , tune PH1 protection and recovery set point	change thermister from 150K to 100K	0.1	44	thermister part number SL200000V00 and PR28 change to 21K, PR30 change to 9.53K	2009/08/27	EVT_NEW75
3	Add GPU voltagr sence net	Cause GPU have GCORE_SEN and FB_GND pin so power add receive net.	0.1	51	ADD GCORE_SEN and FB_GND net, also add PR296(0_0402_1%), PR297(10_0402_5%) and PR298(0_0402_5%)	2009/09/04	EVT_NEW75
4	change DC-IN connector part number	to meet pin definition	0.1	43	change part number is SP020908120	2009/09/10	EVT_NEW75
5	change reistance PR81 value	Cause meet battery Ki value setting from 1.106 to 0.7224. change PR81 from 154K(0402_1%) to 80.6K(0402_1%)	0.1	46	change resistance PR81 value from 154K to 80.6K	2009/09/22	EVT_NEW75
6	ADD switch circuit for 1.05V	Cause follow AMD electrclal sheet, VDDIO/ VDDR voltage setting procedure. AMD processor will switch between 1.05V and 0.9V by VDDIO and VDDR	0.1	48	ADD PR161 (165K_0402_1%), PQ58,PR152(10K_0402_5%),PR160(10K_0402_5%), PC131(0.1U_25V6) , change PR161 value from 100K to 249K, and ADD enable net name -VDDR_SW	2009/09/22	EVT_NEW75
7	Change enable signal of +CPU_VDDRP	Cause follow HW demand	0.1	41	change +CPU_VDDR enable signal from VLDT_EN to VR_ON	2009/10/02	EVT_NEW75_6L
8	change resistance size	cause for component de-rating . Prevent the component break down when inrush current happen.	0.1	39	change PR61 from (0.02_1206_1%) to (0.02_2512_1%)	2009/10/06	EVT_NEW75
9	change capacitor value for 0.75VSP request	Cause follow HW request	0.1	41	Change PC103 value from 10u to 22u	2009/10/15	EVT_NEW75_6L
10	Add snubber and boost resistance of 1.1Valw and 1.5V	Cause follow EMI request	0.2	39	Add 4.7 ohm to PR100, add cap. 680p to PC78 and add 2.2 ohm toPR98. Add 4.7 ohm to PR110, add cap. 680p to PC88 and add 2.2 ohm toPR108	2009/11/23	EVT_NEW75_6L
11	Add bead	For reduce B+ noise	0.2	37,39,40	Add PL31,PL32,PL33(SM010020720) and PL26(SM010018210)	2009/11/23	EVT_NEW75_6L
12	Change chock	Cause A phase put wrong chock	0.2	37,39,40	Change PL9 from SH00000FK00 to SH000009Q00	2009/11/23	EVT_NEW75_6L
13	Change resistance value	Cause Hw request 1.1Valw need to set to 1.15V, so change divider resistance PR104	0.2	39	Change PR104 from SD000000680 (S RES 1/16W 8.45K +-1% 0402) to SD034887180 (S RES 1/16W 8.87K +-1% 0402)	2009/12/01	EVT_NEW75_6L
14	ADD capacitance	Cause EMI request	0.2	43	ADD PC219 PC220 SE074222K80 (S CER CAP 2200P 50V K X7R 0402) and PC221 PC222 SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402)	2009/12/01	EVT_NEW75_6L
15	change resistance value	Cause NB_CORE need to switch	0.2	40	change PR158 from SD034232280 (S RES 1/16W 23.2K +-1% 0402) to SD034118280 (S RES 1/16W 11.8K +-1% 0402)	2009/12/01	EVT_NEW75_6L
16	ADD Boost resistance	Cause EMI request	0.2	37-43	ADD PR40, PR47,PR117 and PR230 from SD013000080 (S RES 1/10W 0 +-5% 0603) to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2009/12/01	EVT_NEW75_6L

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11/20

- 1. P.21 unstuff Y4, C588, C589, R368 for AMD suggest
- 2. P.19 Modify Y3 net connect
- 3. P.25 Change C923, C924 as 33pF for Y5

11/24

- 1. P.13, P.15, P.20, P.23 Add Ext@ & Int@ option ; Modify CLK_SBLINK_BCLK net connect
- 2. P.13, P.16, P.20 Add VB@ & UNVB@ option
- 3. P.34 Change U38 as 4430(SB000007010)
- 4. P.27 Add R835, R837 unstuff D44, R836 for WiMax/Wlan LED request ; change R492 as 100Kohm for EC request
- 5. P.30 Change R477, R499 as 680ohm ; R478, R498 as 3.9kohm for LED brightness

11/25

- 1. P.19, P20 update SB GPIO PIN
- 2. P.29 Add R838, R839 for EC RevD3, E0
- 3. P.34 Add C972, C973, C974, C975, C976, C977, C978 for EMI Request
- 4. P.15 Remove R245, R247 for unSD CLK
- 5. P.13 Add R840 for CLK_NB_14.318

11/28

- 1. P.30 JLED1, JLED2 Pin define modify; Add Q73
- 2. P.23 Add R841, R842, R843 ; P.29 Add R844, R845 for Panel Low Power
- 3. P.28 Change D10 P/N as SC300000B00 ; Stuff D41, D27, D39, D11, D13, D29, D24 For ESD Request

PVT

01/18

- 1. P.17 Add HDMI@
- 2. P.19 Change C56 as SF000002N00(H4.4)
- 3. P.13 stuff R67, unstuff U4 for NB_PWRGD
- 4. P.21 stuff R424 for +CPU_VDDR
- 5. P.30 Change LED1, LED3 as SC591NB5A30 ; Change Resistance value for NEW75/85/95
- 6. P.32 Change C957, C971 as 0.47UF
- 7. P.20 Unstuff R359, R360 for SB_SIC, SB_SID

01/25

- 1. P.30 Change Q26 as SB00000DH00
- 2. P.29 Define U26 Pin 36, Pin 17, Pin 85, Pin86 for WWAN & WLAN
- 3. P.31 Reserve C979, C980, R849, R850 for EMI solution
- 4. P.9 Change C23, C24, C25, C26, C75 as SGA19331D10 (ESR 9 ohm)

03/02

- 1. P.29 Add R851, unstuff R852

03/30 For MP

- 1. P.8, P33 unstuff C21, SW3 for MP

05/18 For Cost down

- 1. P.8, P.29, P.31, P.32 unstuff Q73, D24, D27, D29, U2, U40, C681, R304 ,C687, R411 stuff R283

05/18 For PEW56

- 1. Modify SB GPIO64, B_ID, P_ID, LED, TSI BOM option

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