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Compal Confidential

IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M
(With nVIDIA MXM/B)

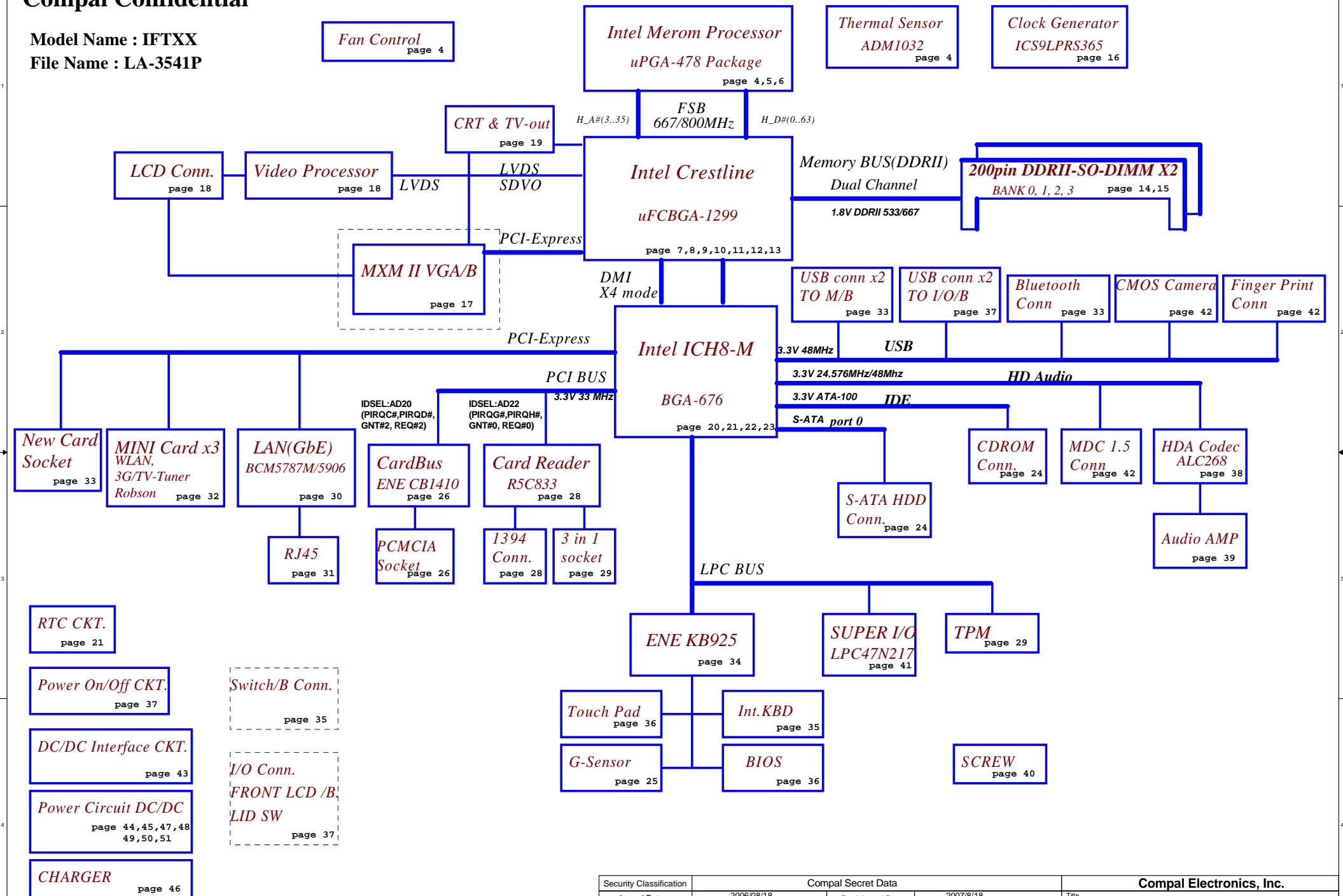
2006-11-01

REV: 0.1

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title Cover Page		
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				Date:	Wednesday, November 01, 2006	Sheet 1 of 52

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Model Name : IFTXX
File Name : LA-3541P



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				IFTXX M/B LA-3541P Schematic	
				Date:	Wednesday, November 01, 2006
				Sheet	2 of 52

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
NVIDIA NB8X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

BOARD ID Table

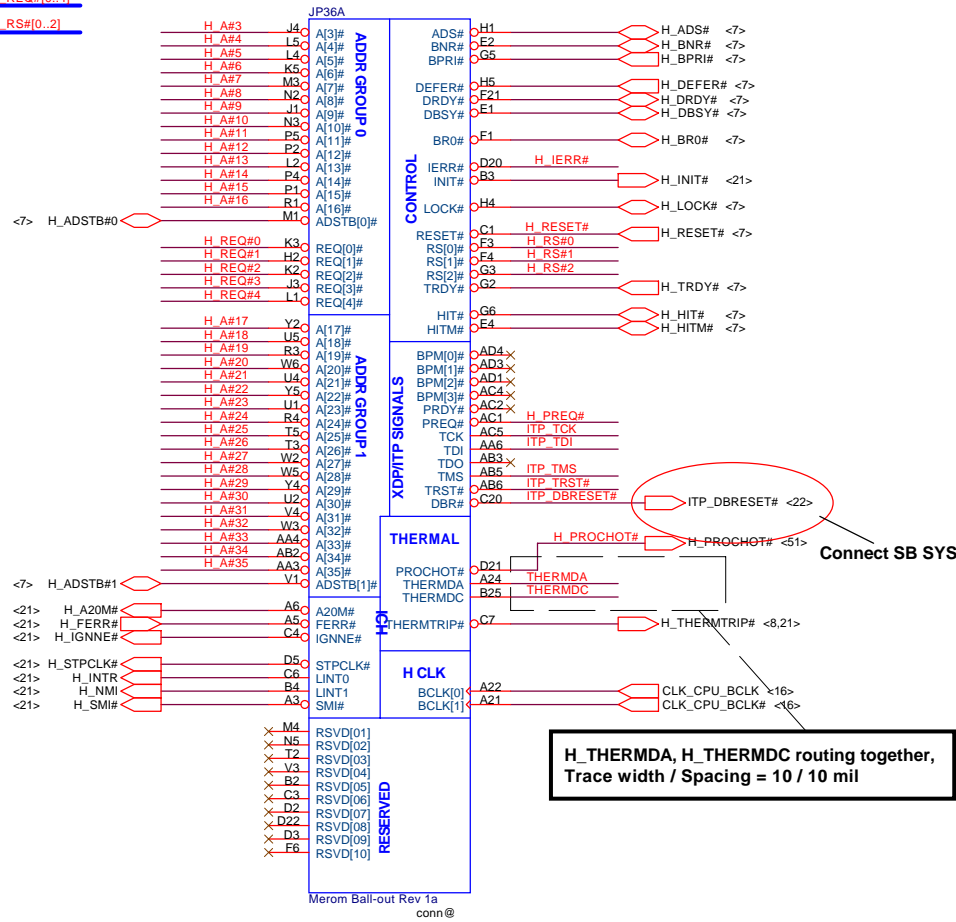
ID1	ID0	TEST
0 (R744)	0 (R745)	A-TEST
0 (R744)	1 (R742)	B-TEST
1 (R741)	0 (R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

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Size B	Document Number	Rev 0		
	IFTXX M/B LA-3541P Schematic			
Date:	Wednesday, November 01, 2006	Sheet	3	of 52

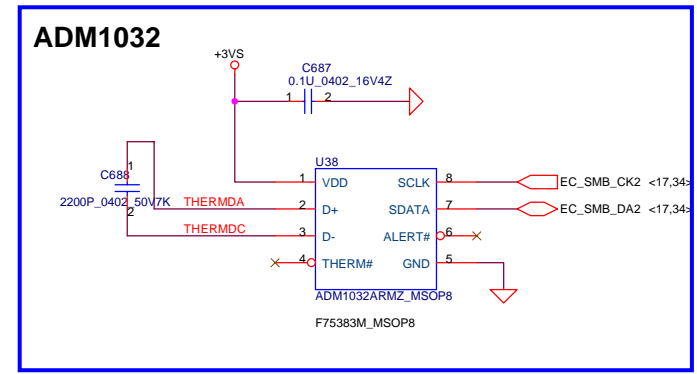
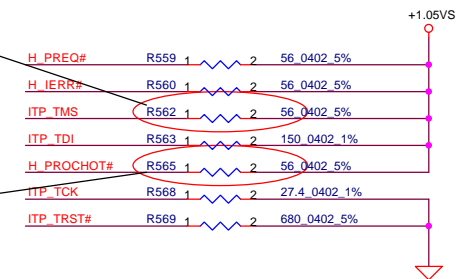
<7> H_A#[3..35] \rightarrow H_A#[3..35]
 <7> H_REQ#[0..4] \rightarrow H_REQ#[0..4]
 <7> H_RS#[0..2] \rightarrow H_RS#[0..2]



Place close to CPU within 500mil

Checklist recommend 39 Ohm

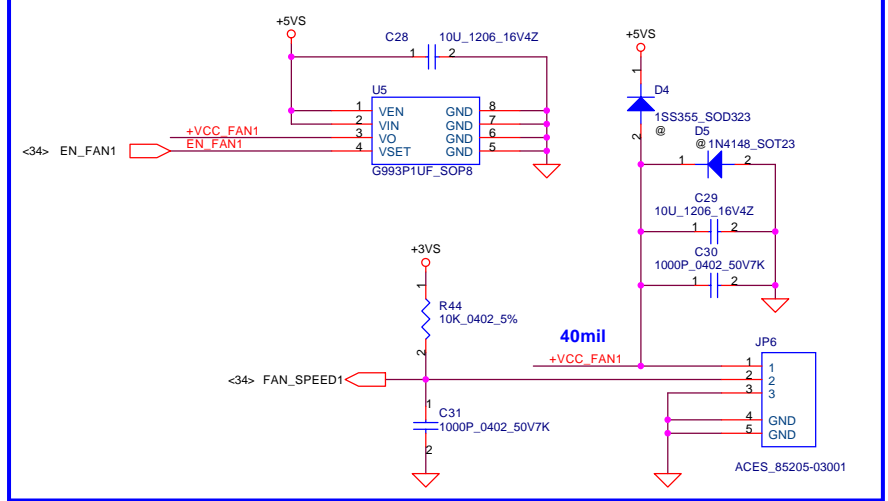
CRB pull 75 Ohm



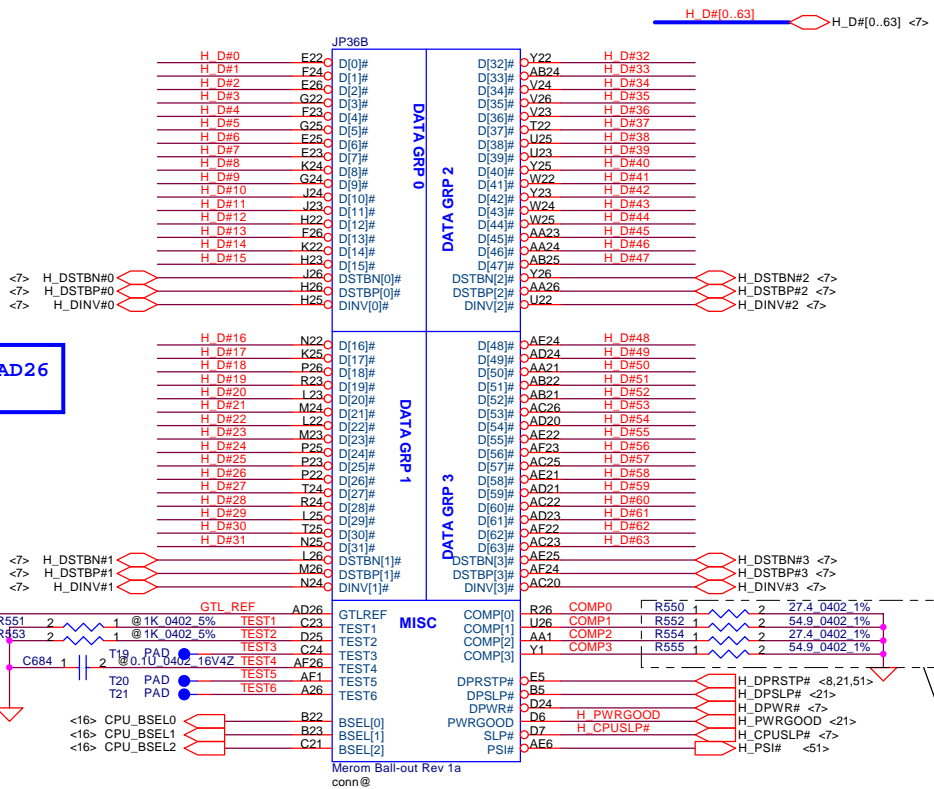
Connect SB_SYS_RESET# or just left NC

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

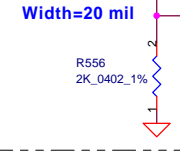
FAN1 Conn



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Size	Document Number	Date:	Wednesday, November 01, 2006	Rev 0
B	IFTXX/MB LA-3541P Schematic	Sheet	4	of 52



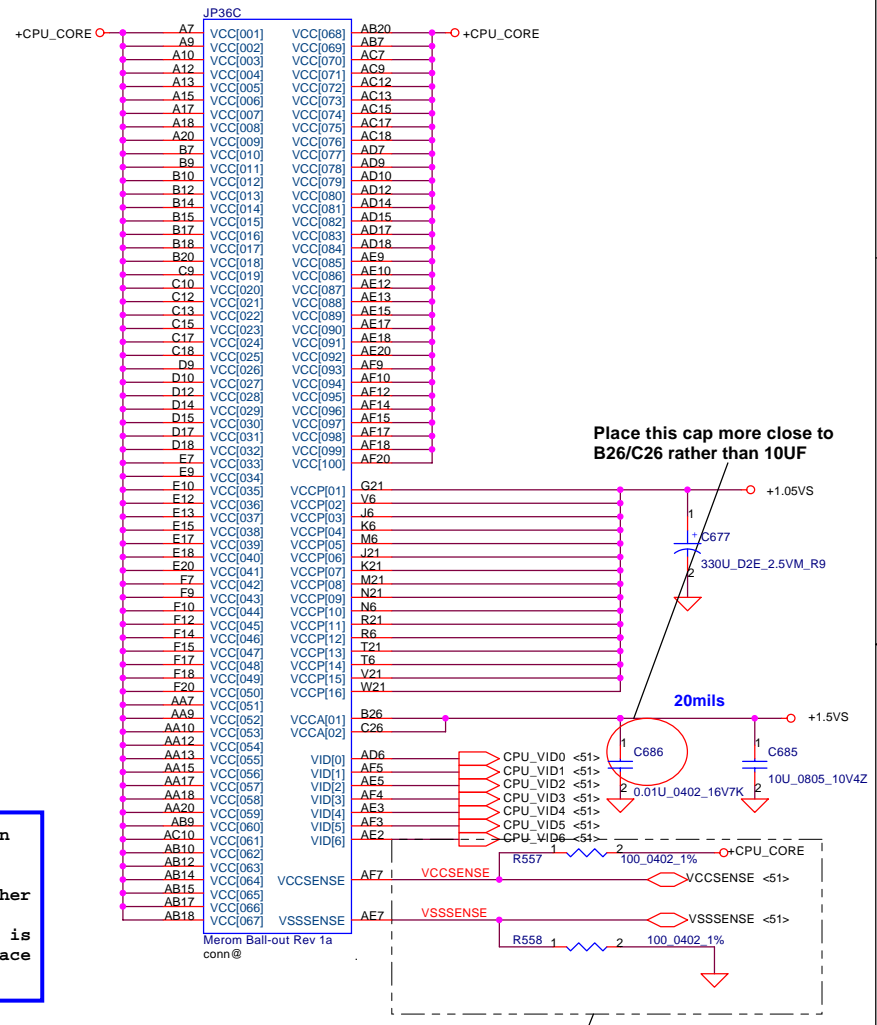
Close to CPU pin AD26 within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



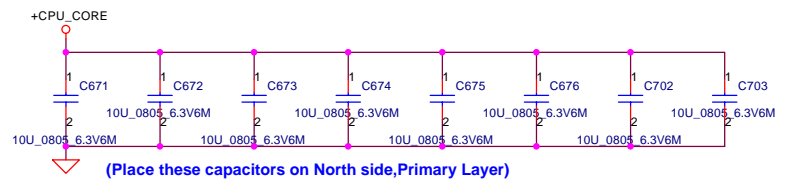
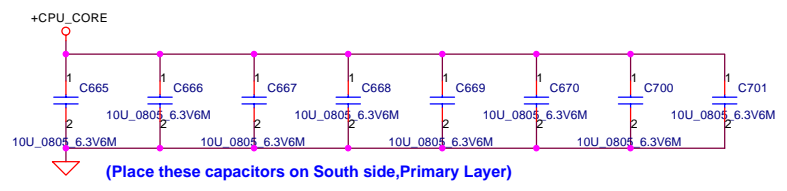
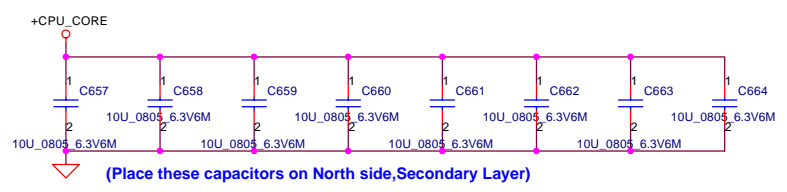
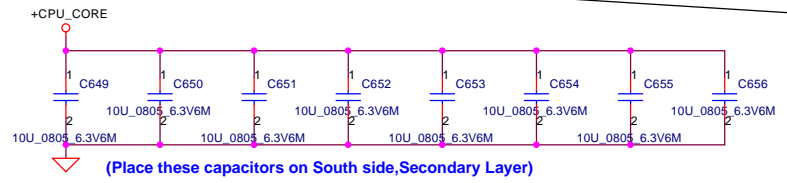
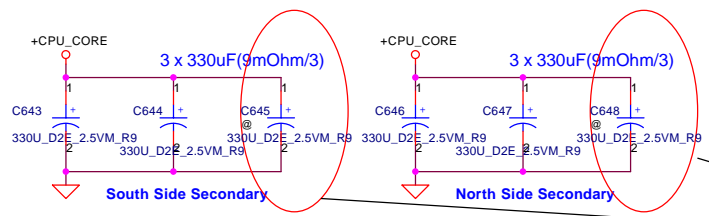
Place this cap more close to B26/C26 rather than 10UF

Length match within 25 mils. The trace width/space/other is 20/7/25.

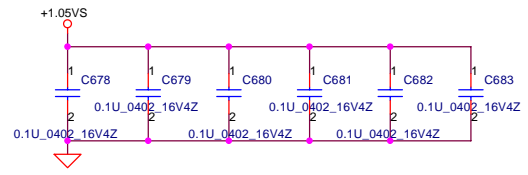
Close to CPU pin within 500mils.

JP36D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A27	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
F24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

Merom Ball-out Rev 1a
conn@



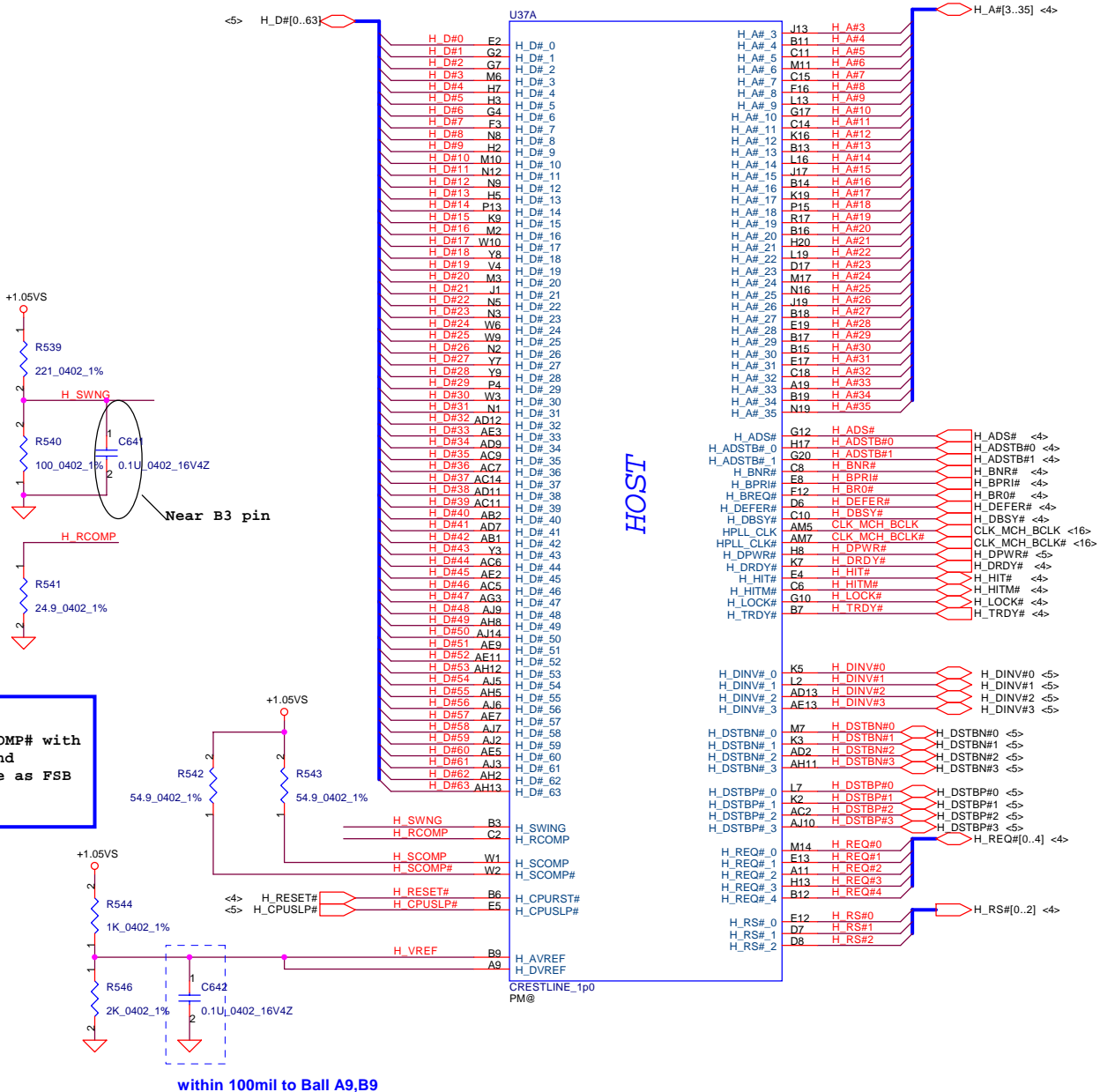
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



CRB no stuff. Reserved!

9/25 10U checked. OK for use!

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Size B	Document Number	Rev 0		
	IFTXX M/B LA-3541P Schematic			
Date:	Wednesday, November 01, 2006	Sheet	6 of 52	



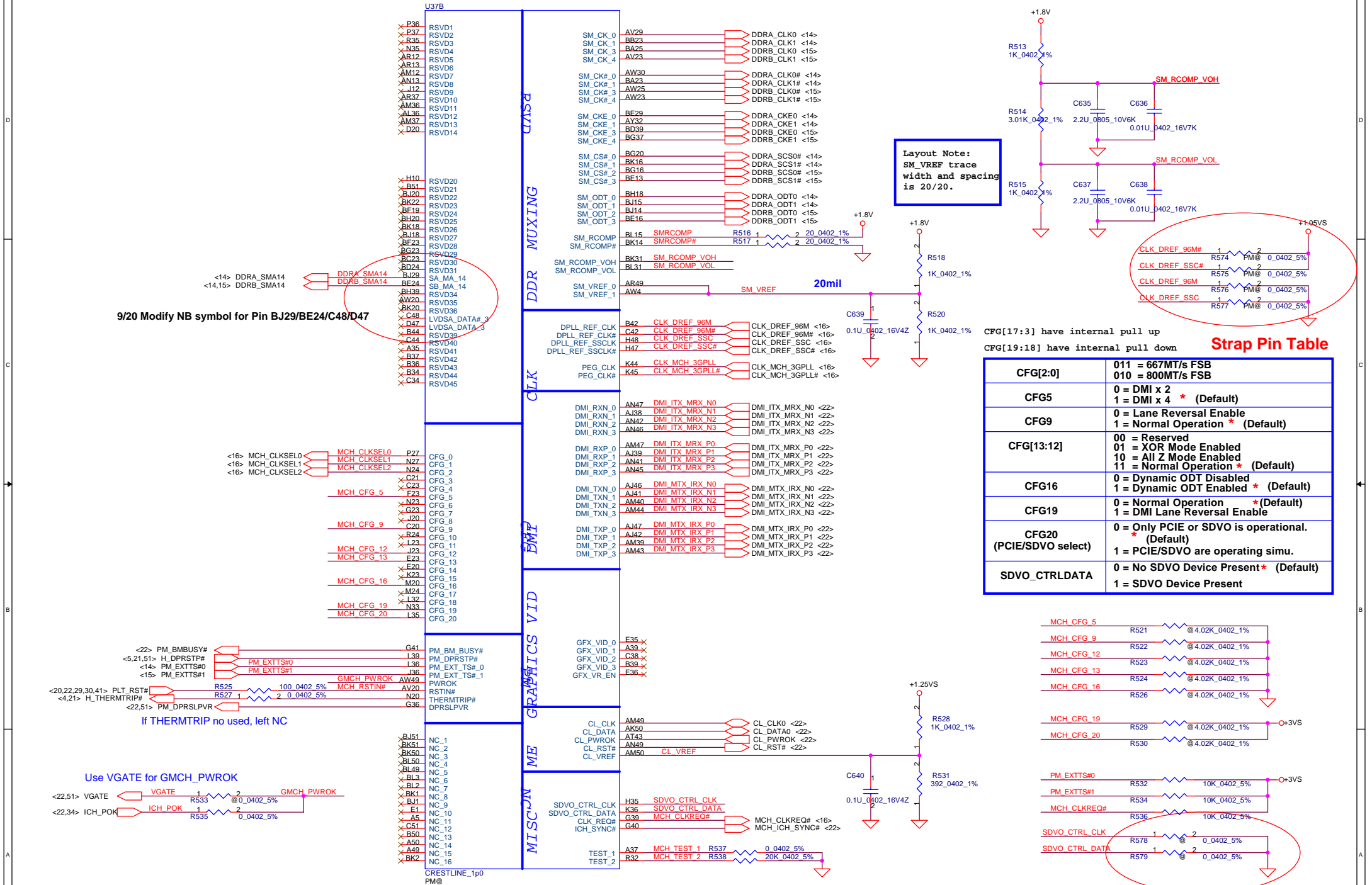
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

within 100mil to Ball A9,B9

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

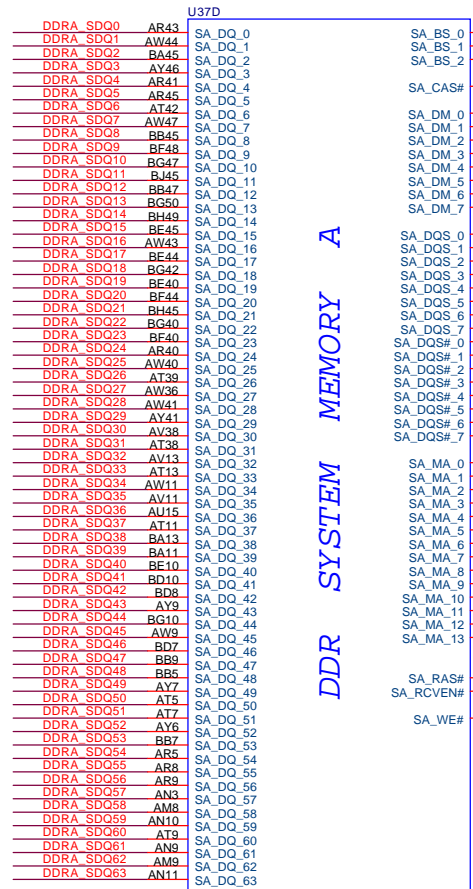
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Date:	Wednesday, November 01, 2006	Sheet	7	of 52

Crestline (1/7)-GTL		Rev	0
Size B	Document Number	IFTXX M/B LA-3541P Schematic	

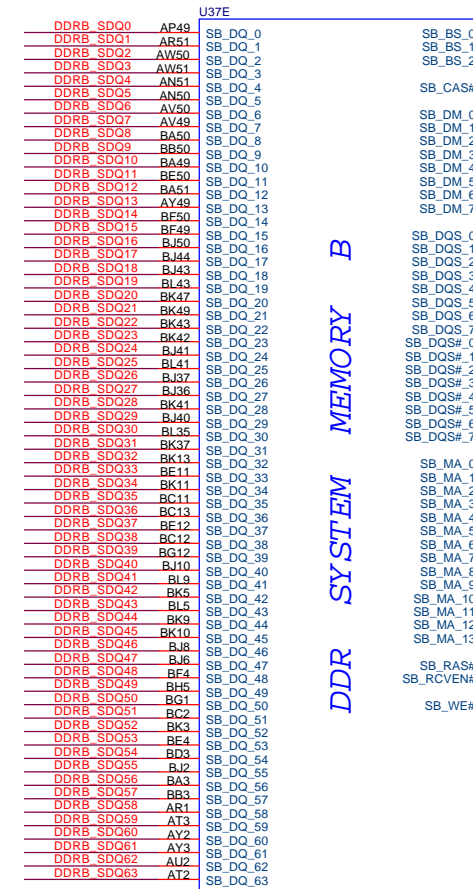
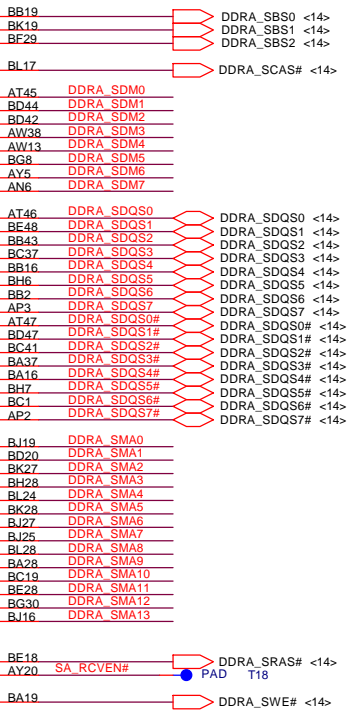


<14> DDRA_SDQ[0..63] DDRA_SDQ[0..63]
 <14> DDRA_SDM[0..7] DDRA_SDM[0..7]
 <14> DDRA_SMA[0..13] DDRA_SMA[0..13]

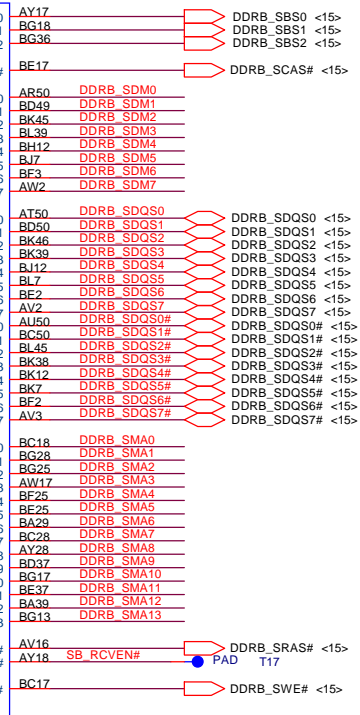
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 <15> DDRB_SDM[0..7] DDRB_SDM[0..7]
 <15> DDRB_SMA[0..13] DDRB_SMA[0..13]



DDR SYSTEM MEMORY A

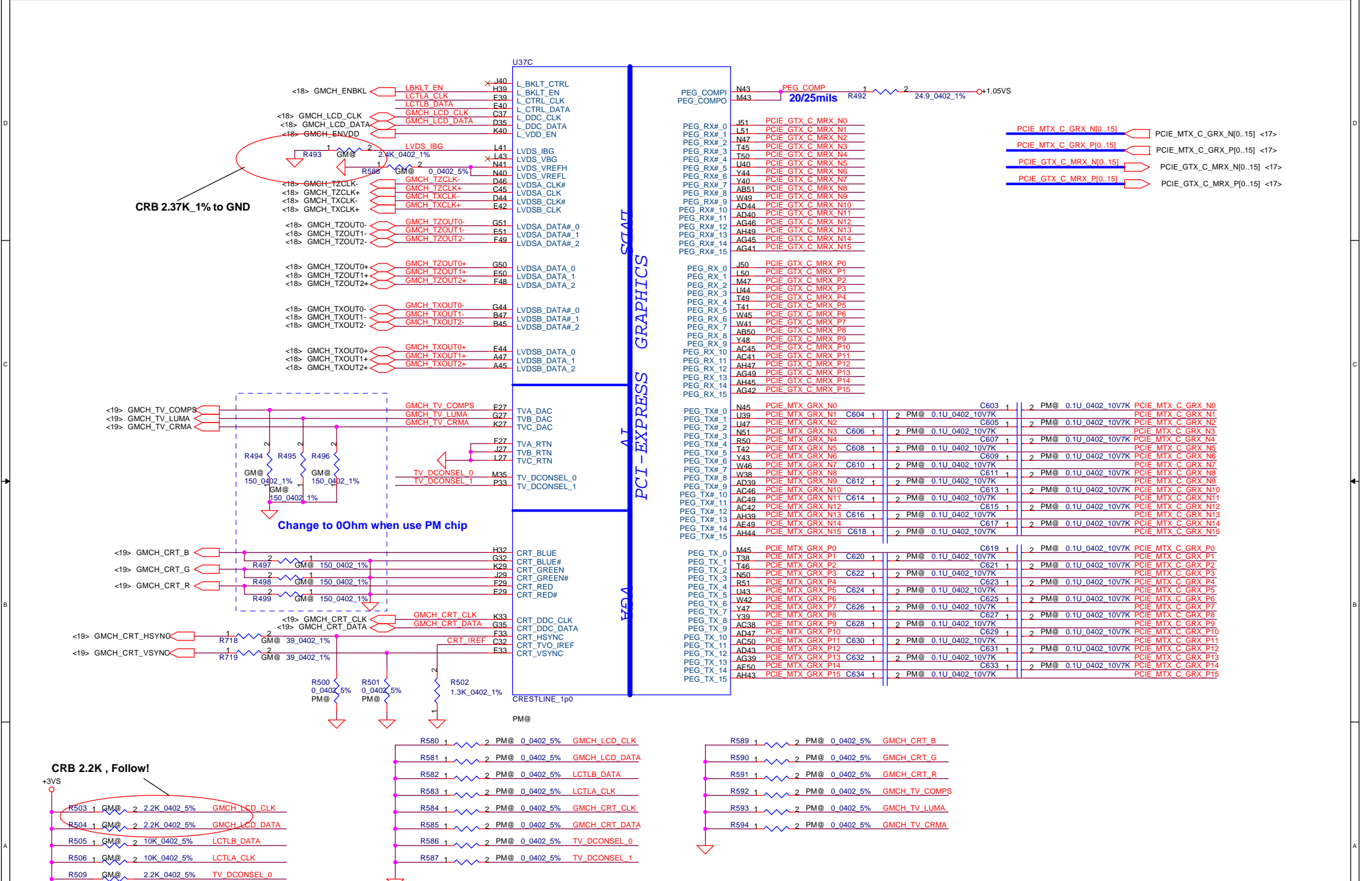


DDR SYSTEM MEMORY B



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Size B	Document Number	Date:		Sheet	Rev 0
	IFTXX M/B LA-3541P Schematic	Wednesday, November 01, 2006		9	52

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Size B	Document Number	Date:		Sheet	Rev 0
	IFTXX M/B LA-3541P Schematic	Wednesday, November 01, 2006		9	52



PEG_COMP1 N43 PEG COMP 1 24.9_0402_1% +1.05VS

- PCIE_MTX_C_GRX_N0[.15] <17>
- PCIE_MTX_C_GRX_P0[.15] <17>
- PCIE GTX C_MRX_N0[.15] <17>
- PCIE GTX_C_MRX_P0[.15] <17>

- J51 PCIE GTX C_MRX_N0
- L51 PCIE GTX C_MRX_N1
- M47 PCIE GTX C_MRX_N2
- T45 PCIE GTX C_MRX_N3
- T50 PCIE GTX C_MRX_N4
- U40 PCIE GTX C_MRX_N5
- Y44 PCIE GTX C_MRX_N6
- Y40 PCIE GTX C_MRX_N7
- Y40 PCIE GTX C_MRX_N8
- AB51 PCIE GTX C_MRX_N9
- W49 PCIE GTX C_MRX_N10
- AD44 PCIE GTX C_MRX_N11
- AD40 PCIE GTX C_MRX_N12
- AG46 PCIE GTX C_MRX_N13
- AH49 PCIE GTX C_MRX_N14
- AG45 PCIE GTX C_MRX_N15

- J50 PCIE GTX C_MRX_P0
- L50 PCIE GTX C_MRX_P1
- M47 PCIE GTX C_MRX_P2
- U44 PCIE GTX C_MRX_P3
- T49 PCIE GTX C_MRX_P4
- T41 PCIE GTX C_MRX_P5
- W45 PCIE GTX C_MRX_P6
- W41 PCIE GTX C_MRX_P7
- AB50 PCIE GTX C_MRX_P8
- Y48 PCIE GTX C_MRX_P9
- AC45 PCIE GTX C_MRX_P10
- AC41 PCIE GTX C_MRX_P11
- AH47 PCIE GTX C_MRX_P12
- AG49 PCIE GTX C_MRX_P13
- AH45 PCIE GTX C_MRX_P14
- AG42 PCIE GTX C_MRX_P15

- N45 PCIE MTX GRX N0 C603 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N0
- L39 PCIE MTX GRX N1 C604 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N1
- L47 PCIE MTX GRX N2 C605 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N2
- N51 PCIE MTX GRX N3 C606 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N3
- R50 PCIE MTX GRX N4 C607 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N4
- T42 PCIE MTX GRX N5 C608 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N5
- W43 PCIE MTX GRX N6 C609 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N6
- W46 PCIE MTX GRX N7 C610 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N7
- W38 PCIE MTX GRX N8 C611 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N8
- AD39 PCIE MTX GRX N9 C612 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N9
- AC46 PCIE MTX GRX N10 C613 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N10
- AC49 PCIE MTX GRX N11 C614 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N11
- AC42 PCIE MTX GRX N12 C615 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N12
- AH39 PCIE MTX GRX N13 C616 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N13
- AE49 PCIE MTX GRX N14 C617 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N14
- AH44 PCIE MTX GRX N15 C618 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_N15

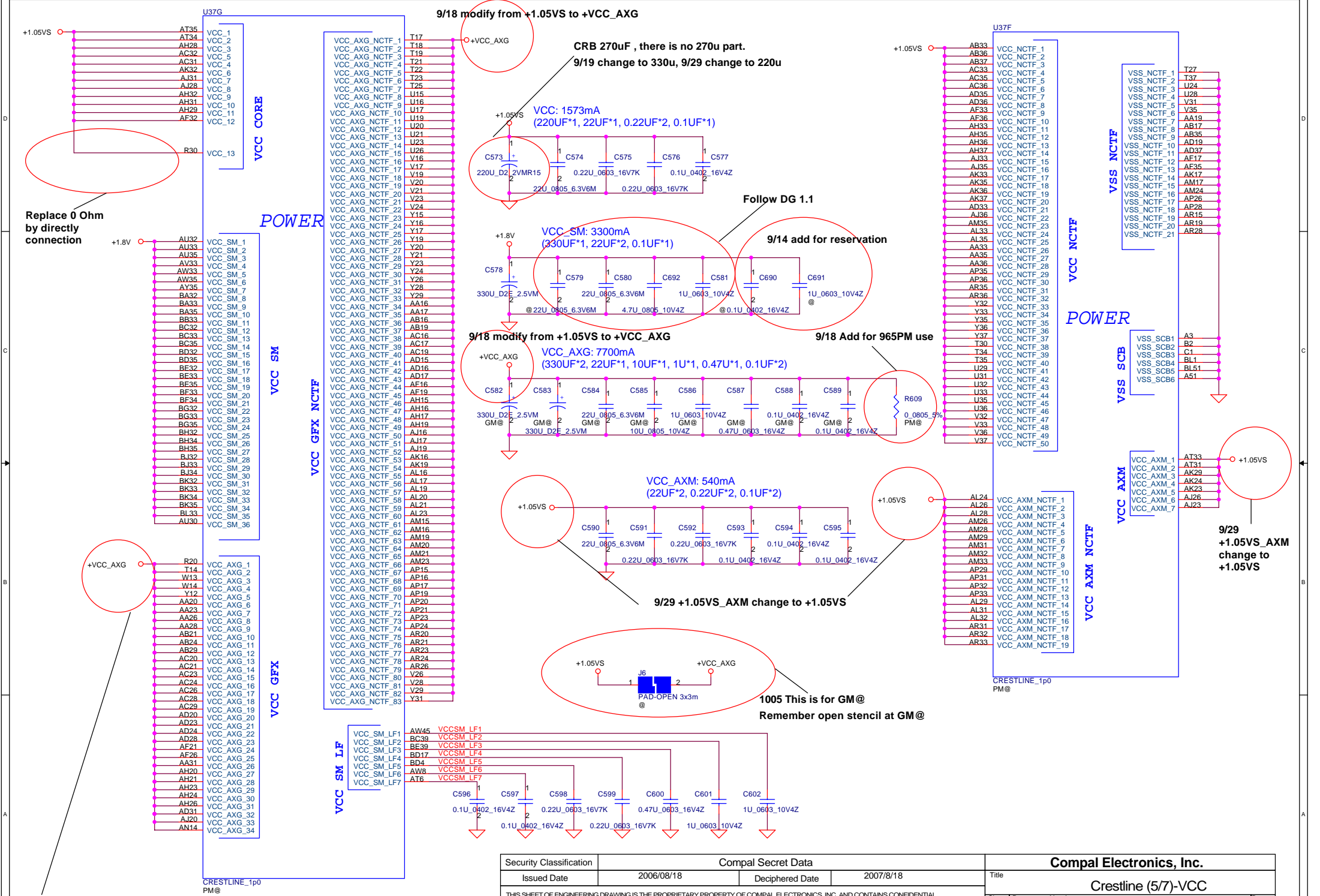
- M45 PCIE MTX GRX P0 C619 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P0
- T38 PCIE MTX GRX P1 C620 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P1
- T46 PCIE MTX GRX P2 C621 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P2
- N50 PCIE MTX GRX P3 C622 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P3
- R51 PCIE MTX GRX P4 C623 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P4
- U43 PCIE MTX GRX P5 C624 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P5
- W42 PCIE MTX GRX P6 C625 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P6
- Y47 PCIE MTX GRX P7 C626 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P7
- Y39 PCIE MTX GRX P8 C627 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P8
- AD38 PCIE MTX GRX P9 C628 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P9
- AD47 PCIE MTX GRX P10 C629 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P10
- AC50 PCIE MTX GRX P11 C630 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P11
- AD43 PCIE MTX GRX P12 C631 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P12
- AG39 PCIE MTX GRX P13 C632 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P13
- AE50 PCIE MTX GRX P14 C633 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P14
- AH43 PCIE MTX GRX P15 C634 1 2 PM@ 0.1U_0402_10V7K PCIE_MTX_C_GRX_P15

- CRB 2.2K , Follow!**
- K503 1 GM@ 2 2.2K 0402 5% GMCH_LCD_CLK
 - R504 1 GM@ 2 2.2K 0402 5% GMCH_LCD_DATA
 - R505 1 GM@ 2 10K 0402 5% LCTLB_DATA
 - R506 1 GM@ 2 10K 0402 5% LCTLA_CLK
 - R509 GM@ 2.2K 0402 5% TV_DCONSEL_0
 - R510 GM@ 2.2K 0402 5% TV_DCONSEL_1

- R580 1 2 PM@ 0.0402 5% GMCH_LCD_CLK
- R581 1 2 PM@ 0.0402 5% GMCH_LCD_DATA
- R582 1 2 PM@ 0.0402 5% LCTLB_DATA
- R583 1 2 PM@ 0.0402 5% LCTLA_CLK
- R584 1 2 PM@ 0.0402 5% GMCH_CRT_CLK
- R585 1 2 PM@ 0.0402 5% GMCH_CRT_DATA
- R586 1 2 PM@ 0.0402 5% TV_DCONSEL_0
- R587 1 2 PM@ 0.0402 5% TV_DCONSEL_1

- R589 1 2 PM@ 0.0402 5% GMCH_CRT_B
- R590 1 2 PM@ 0.0402 5% GMCH_CRT_G
- R591 1 2 PM@ 0.0402 5% GMCH_CRT_R
- R592 1 2 PM@ 0.0402 5% GMCH_TV_COMPS
- R593 1 2 PM@ 0.0402 5% GMCH_TV_LUMA
- R594 1 2 PM@ 0.0402 5% GMCH_TV_CRMA

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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Size B	Document Number	IFTXX M/B LA-3541P Schematic		Rev 0
Date:	Wednesday, November 01, 2006	Sheet	10	of 52



Replace 0 Ohm by directly connection

9/18 modify from +1.05VS to +VCC_AXG

CRB 270uF , there is no 270u part.

9/19 change to 330u, 9/29 change to 220u

VCC: 1573mA
(220UF*1, 22UF*1, 0.22UF*2, 0.1UF*1)

Follow DG 1.1

VCC_SM: 3300mA
(330UF*1, 22UF*2, 0.1UF*1)

9/14 add for reservation

9/18 modify from +1.05VS to +VCC_AXG

VCC_AXG: 7700mA
(330UF*2, 22UF*1, 10UF*1, 1U*1, 0.47U*1, 0.1UF*2)

9/18 Add for 965PM use

VCC_AXM: 540mA
(22UF*2, 0.22UF*2, 0.1UF*2)

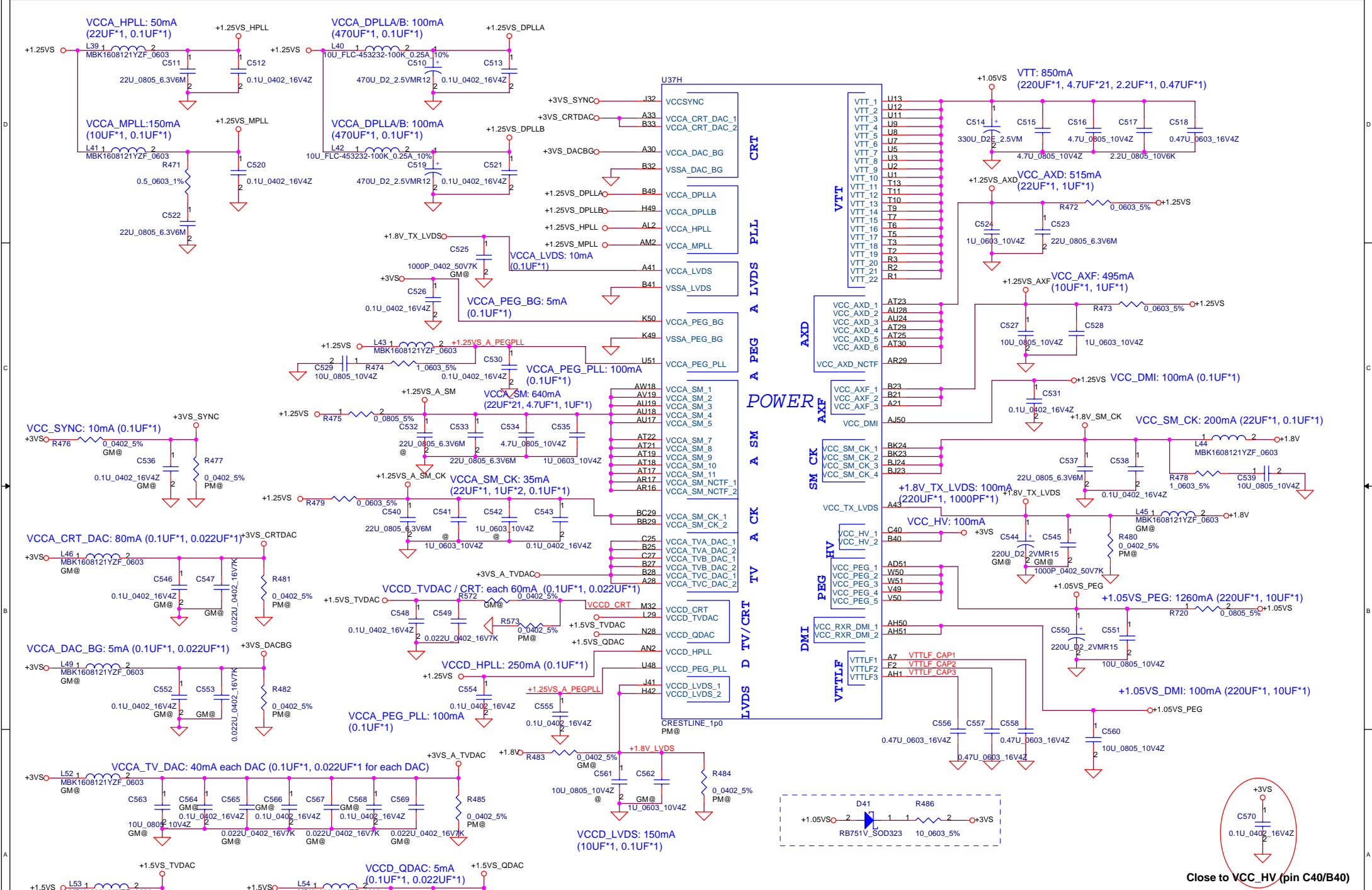
9/29 +1.05VS_AXM change to +1.05VS

1005 This is for GM@
Remember open stencil at GM@

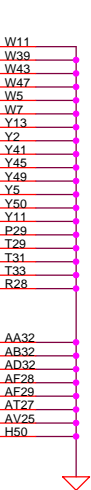
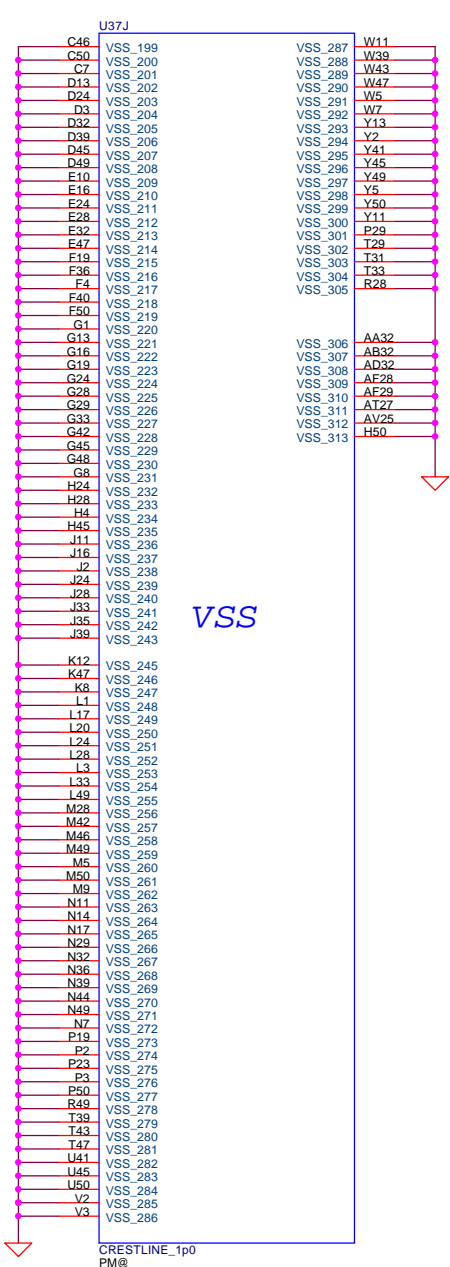
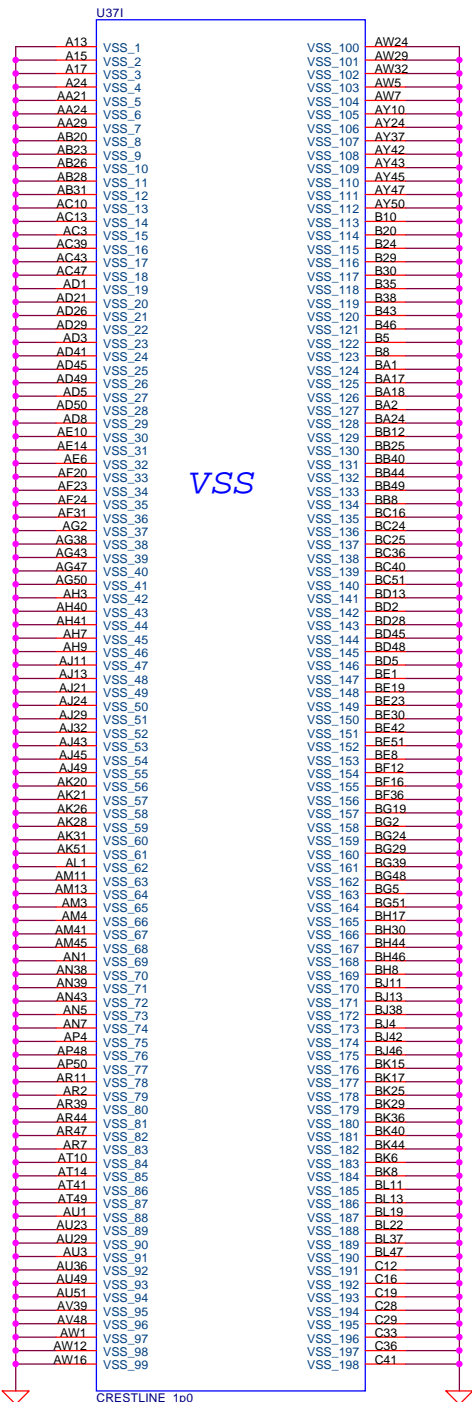
9/18 modify from +1.05VS to +VCC_AXG

9/29 +1.05VS_AXM change to +1.05VS

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Title	Crestline (5/7)-VCC			
Size	Document Number	IFTXX MB LA-3541P Schematic		Rev
B				0
Date:	Wednesday, November 01, 2006	Sheet	11	of 52

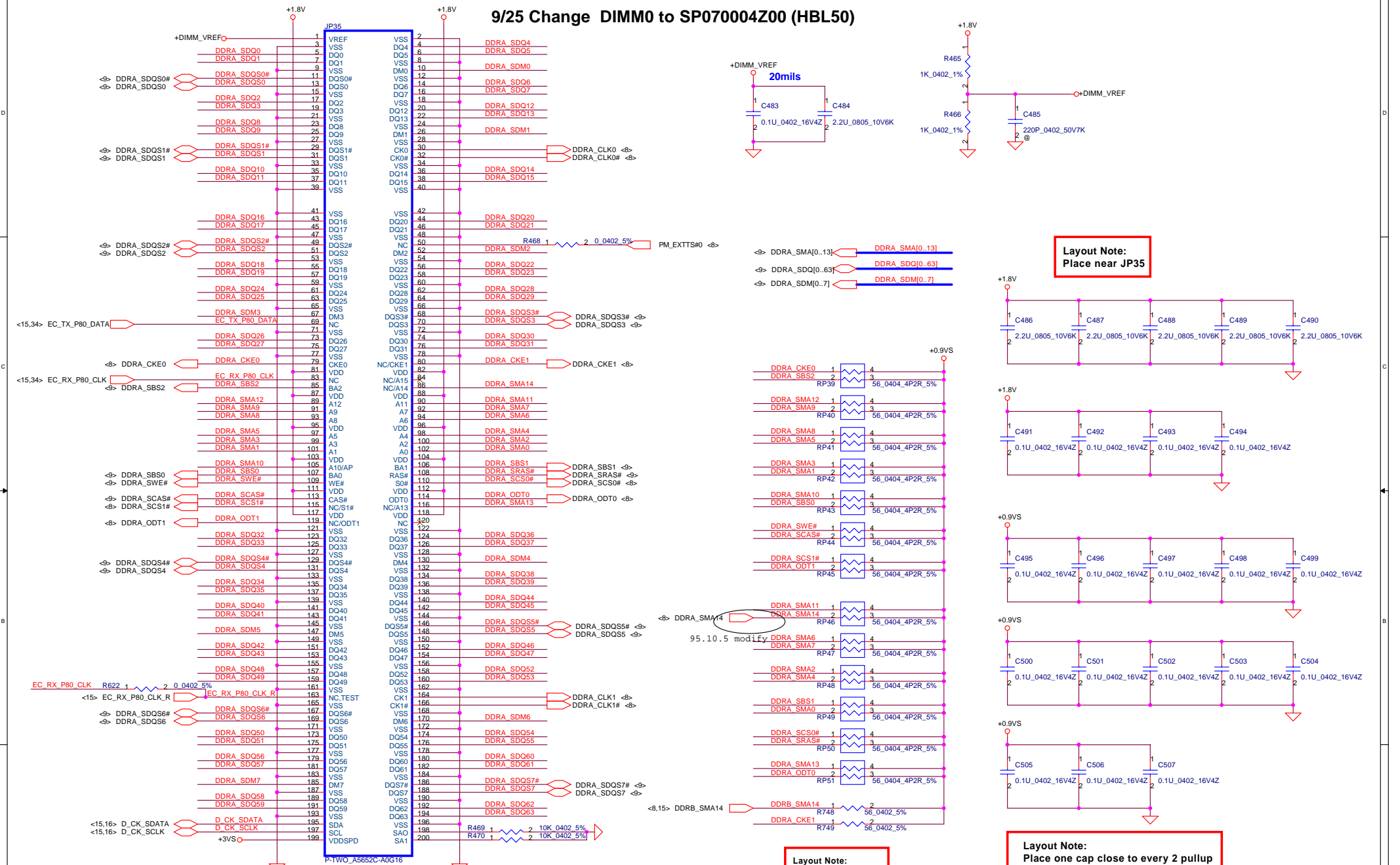


Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Crestline (6/7)-VCC	
2006/08/18		2007/8/18		IFTXX/MB LA-3541P Schematic	
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Size B	Document Number	Date:	Wednesday, November 01, 2006	Sheet	12 of 52

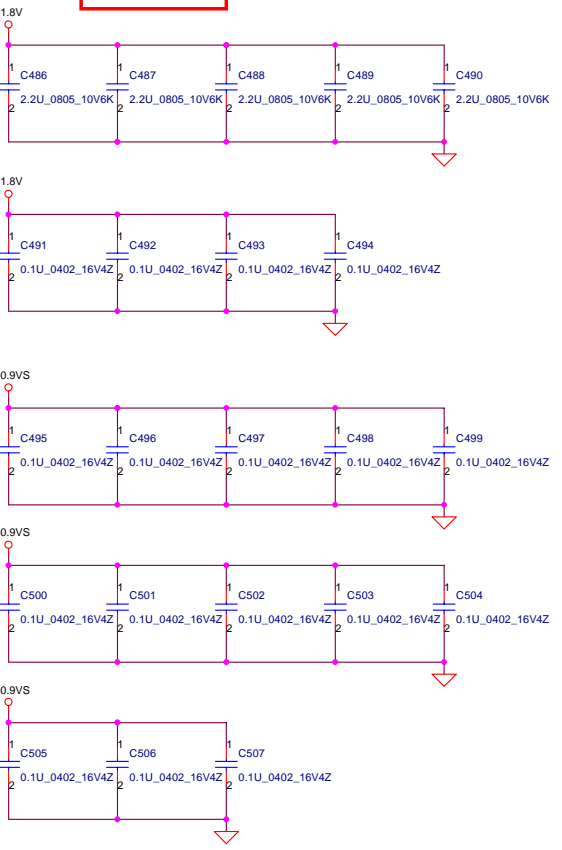


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Size B	Document Number	Rev 0		Date: Wednesday, November 01, 2006	
IFTXX M/B LA-3541P Schematic		Sheet 13 of 52		Date: Wednesday, November 01, 2006	

9/25 Change DIMM0 to SP070004Z00 (HBL50)



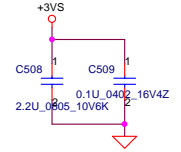
Layout Note:
Place near JP35



Layout Note:
Place these resistor closely JP35, all trace length Max=1.5"

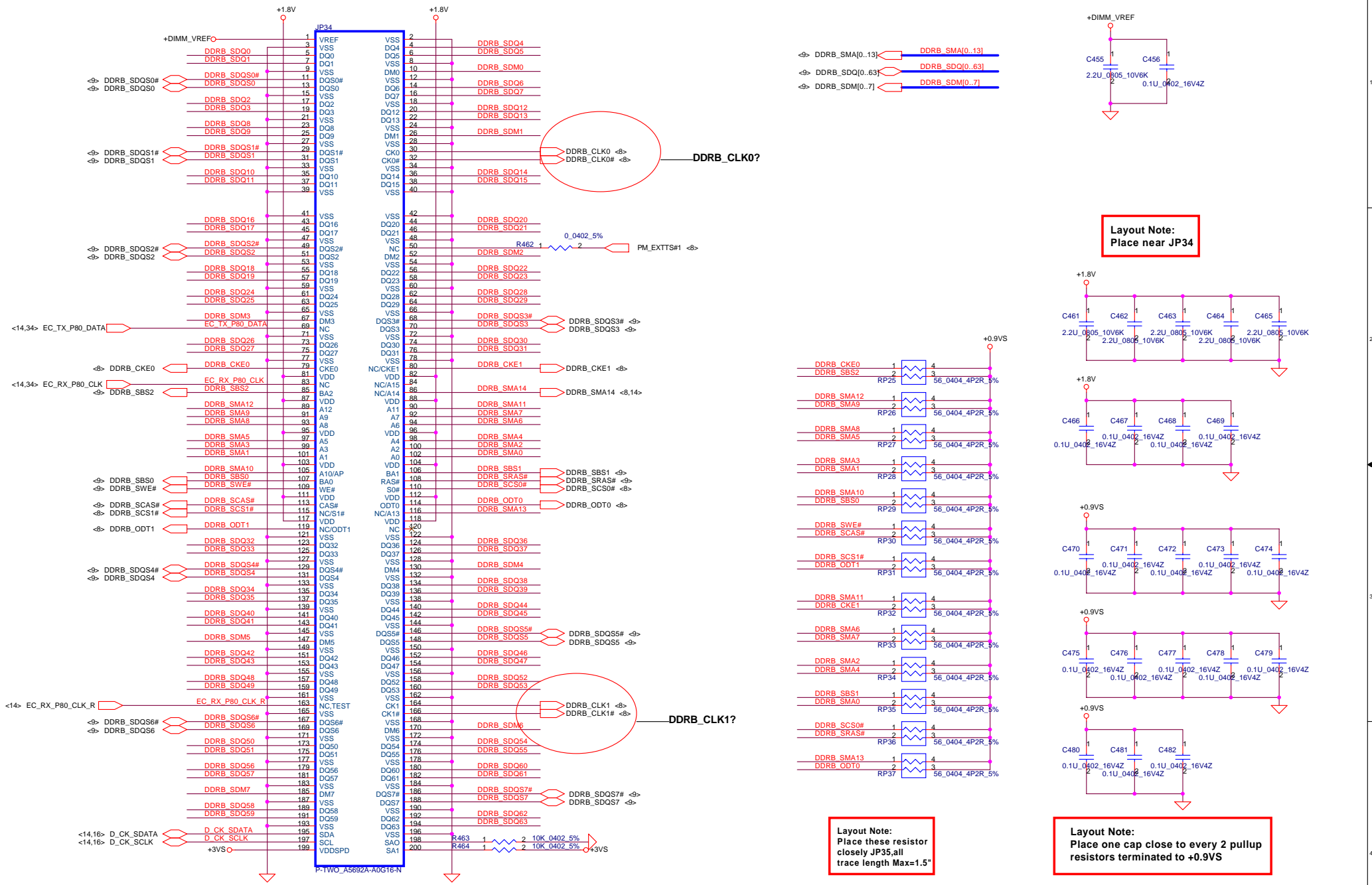
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DIMM0 STD H:5.2mm (BOT)
Change PCB Footprint



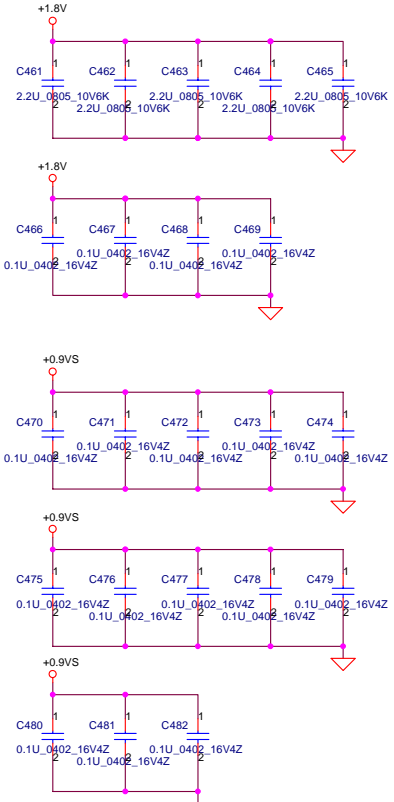
Security Classification		Compal Secret Data		Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	DDRII-SODIMMO
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Size B	Document Number	Date: Wednesday, November 01, 2006		Sheet	14 of 52
				IFTXX M/B LA-3541P Schematic	

9/25 Change DIMM1 to SP070006F00



DIMM1 STD H:9.2mm (BOT)

Layout Note:
Place near JP34



Layout Note:
Place these resistor closely JP35, all trace length Max=1.5"

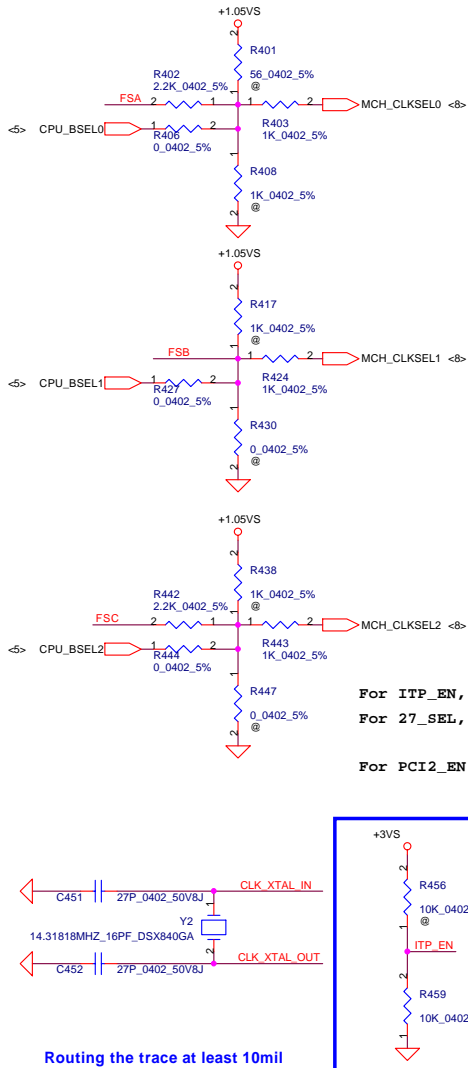
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

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				IFTX MB LA-3541P Schematic
Date: Wednesday, November 01, 2006				Sheet 15 of 52

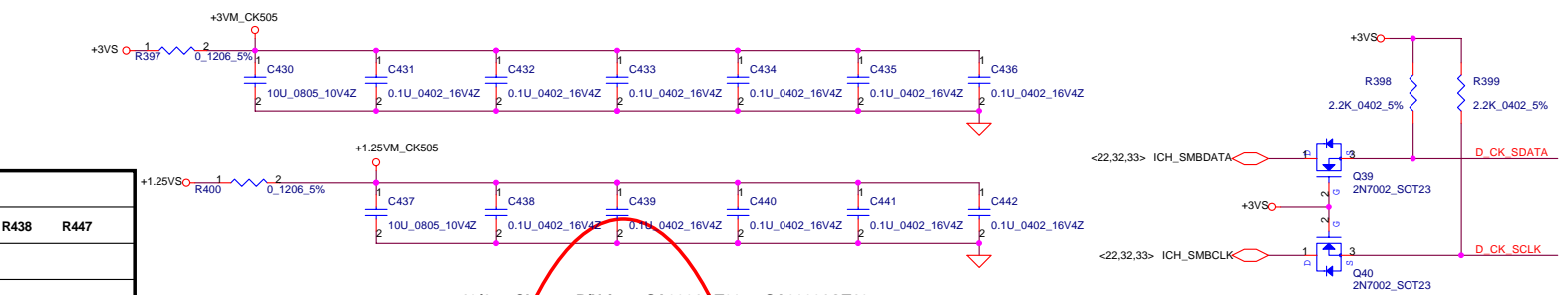
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R401	R408	R417	R430	R438	R447
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447
	Stuff	R401	R417	R447			
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			

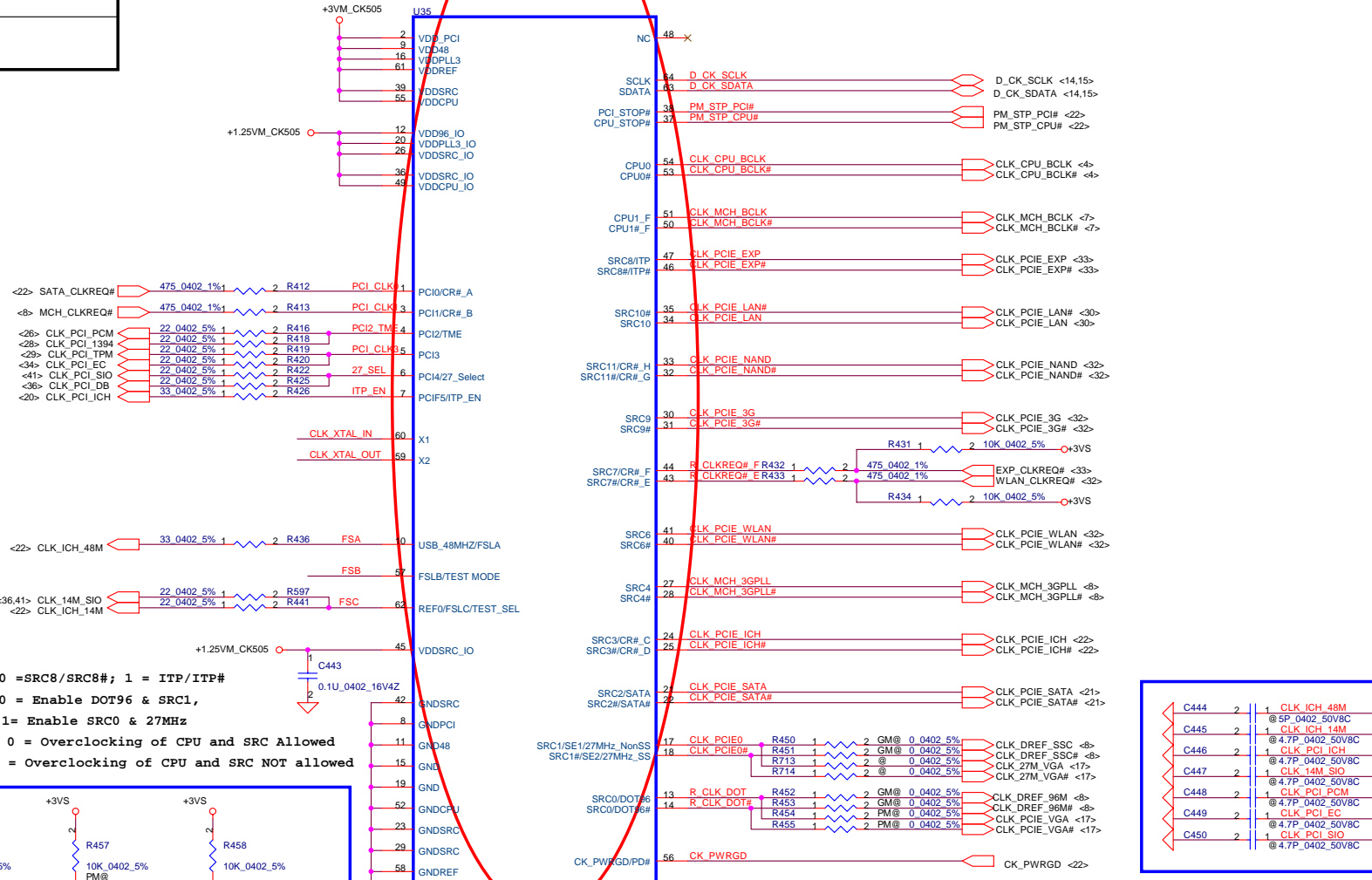


Routing the trace at least 10mil



10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol



C444	2	1	CLK_ICH_48M	@ 5P_0402_50V8C
C445	2	1	CLK_ICH_14M	@ 4.7P_0402_50V8C
C446	2	1	CLK_PCI_ICH	@ 4.7P_0402_50V8C
C447	2	1	CLK_14M_SIO	@ 4.7P_0402_50V8C
C448	2	1	CLK_PCI_PCM	@ 4.7P_0402_50V8C
C449	2	1	CLK_PCI_EC	@ 4.7P_0402_50V8C
C450	2	1	CLK_PCI_SIO	@ 4.7P_0402_50V8C

Place close to U35

Security Classification	Compal Secret Data		Title	
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Date:	Wednesday, November 01, 2006	Sheet	16	of 52

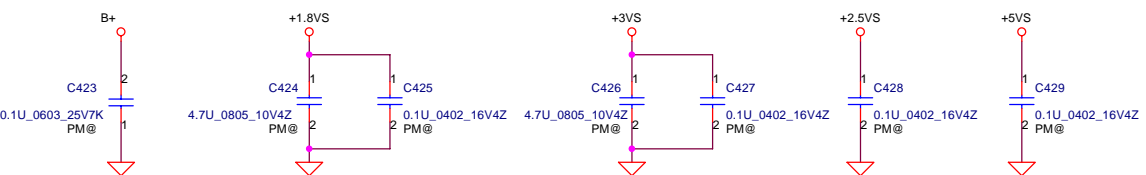
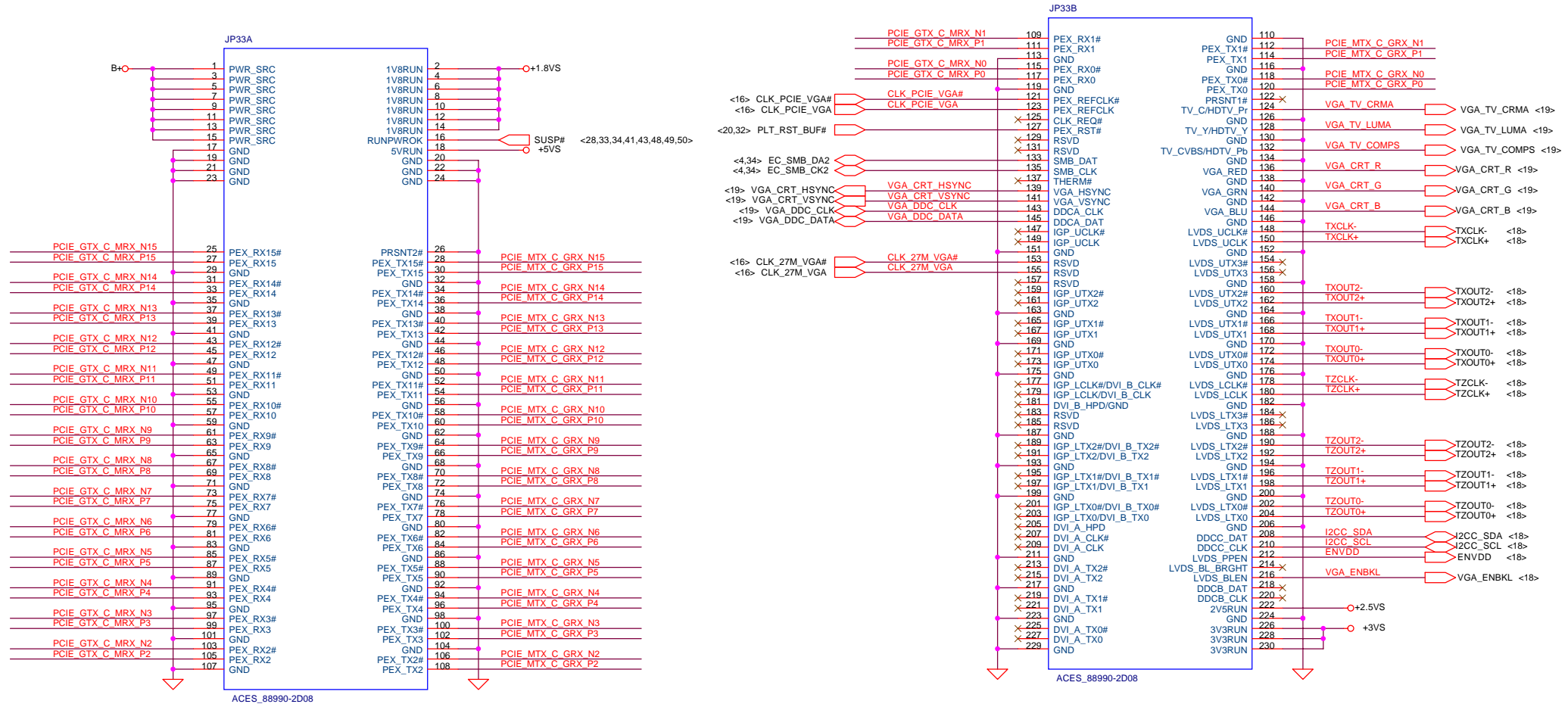
Compal Electronics, Inc.

Clock generator

Rev 0.1

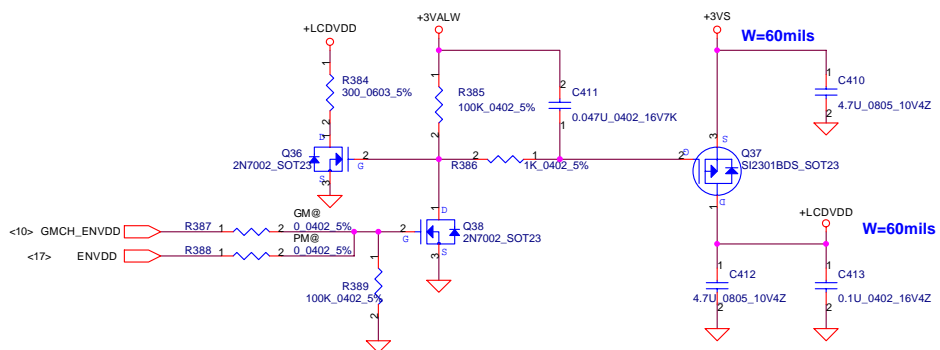
9/13 modify this footprint from ACES_88990-2D08_230P to ACES_88990-2D28_230P

- <10> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
- <10> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
- <10> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
- <10> PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

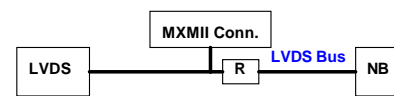


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				Date:	Wednesday, November 01, 2006	Sheet 17 of 52

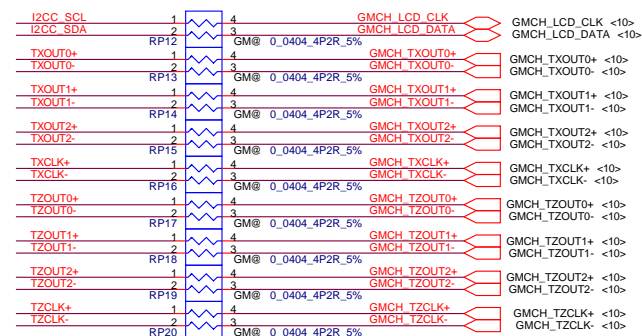
LCD POWER CIRCUIT



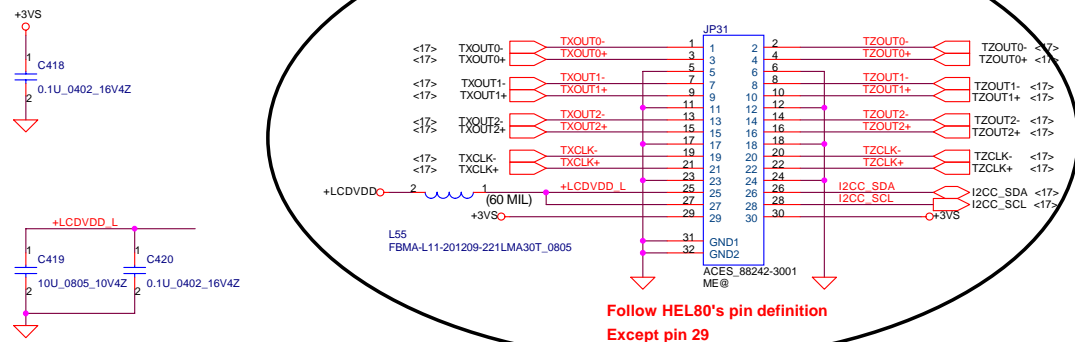
Routing Diagram



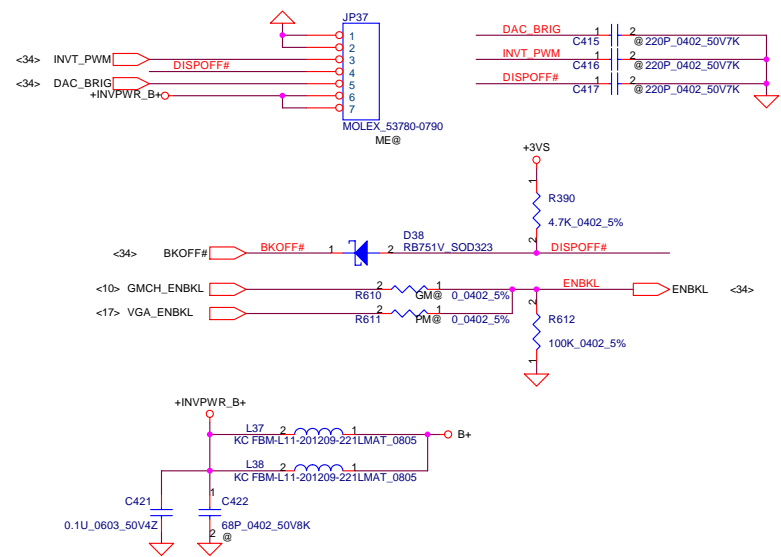
Use Daisy chain to route



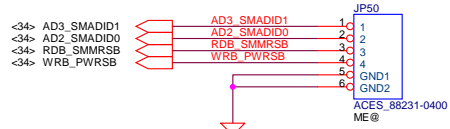
LCD/PANEL BD. Conn.



INVERTER Conn.

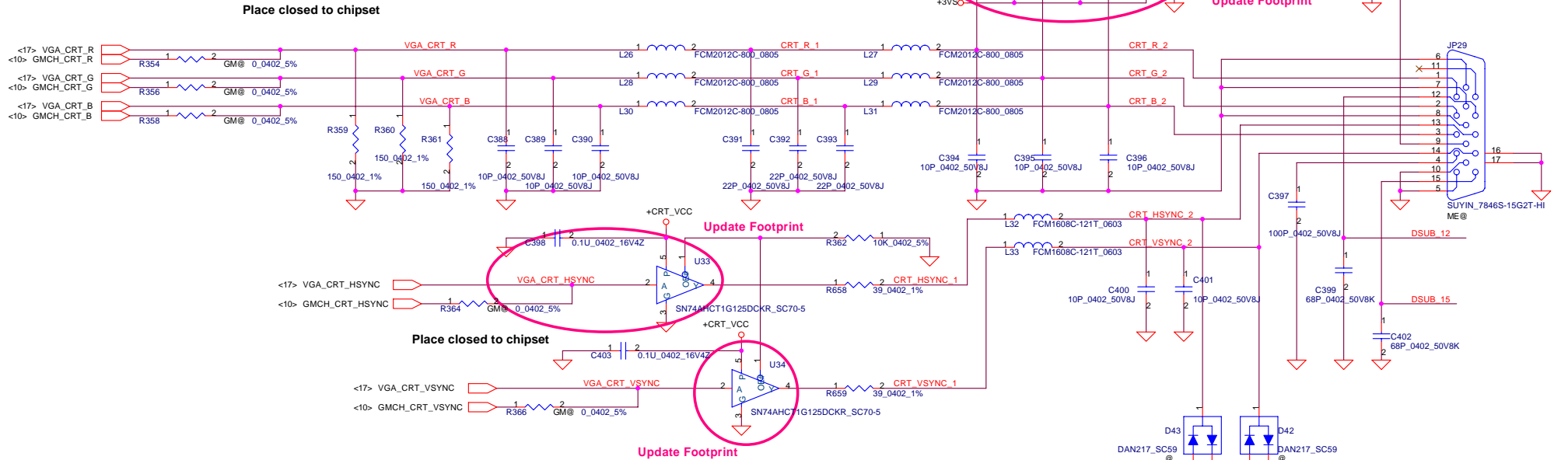


JEPICO Conn.

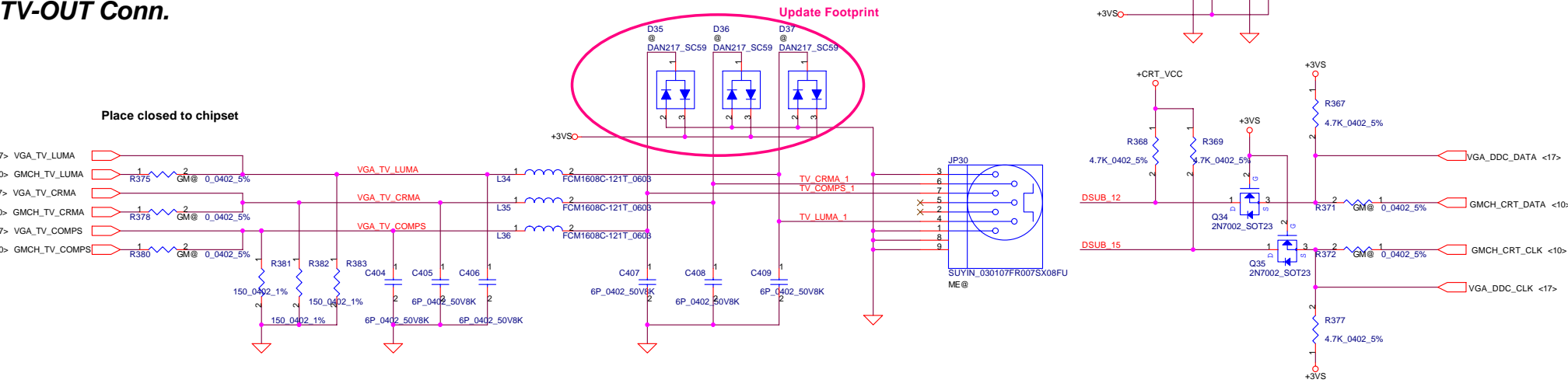


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	LVDS & DVI Connector	
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			B	IFTXX/MB LA-3541P Schematic	0
			Date:	Wednesday, November 01, 2006	Sheet 18 of 52

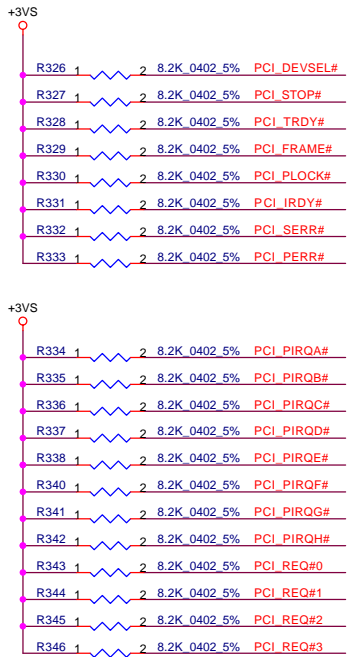
CRT Connector



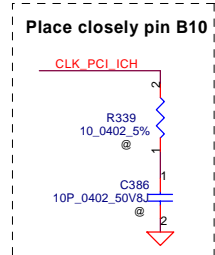
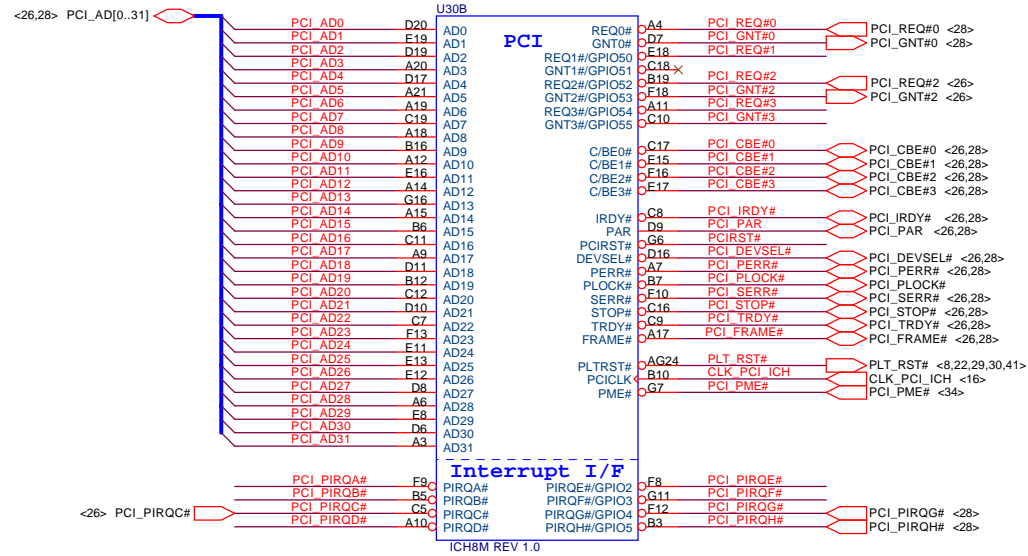
TV-OUT Conn.



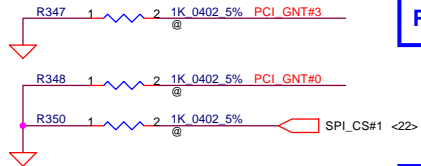
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	
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Size	Document Number	Rev		0
B	IFTXX/MB LA-3541P Schematic			
Date:	Wednesday, November 01, 2006		Sheet	19 of 52



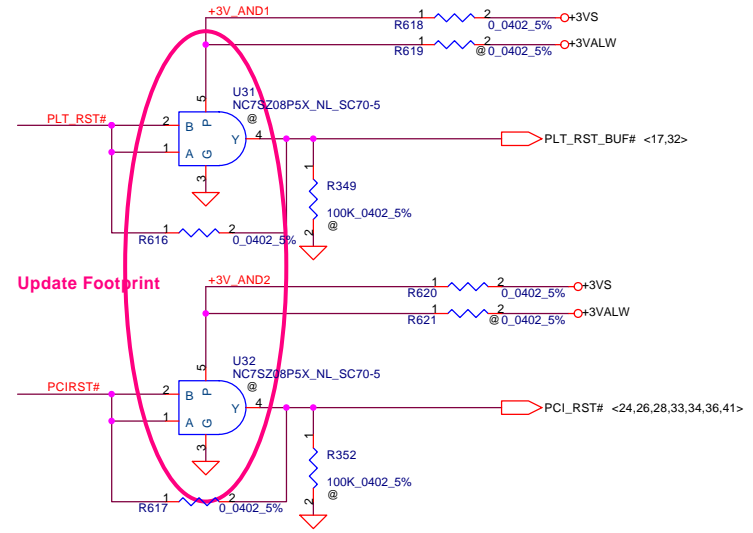
10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10

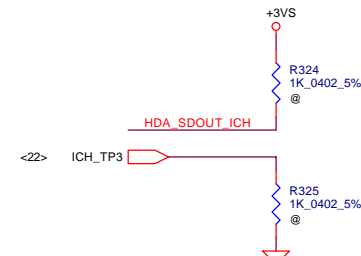
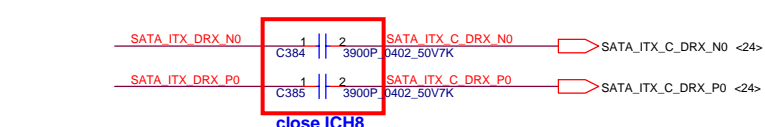
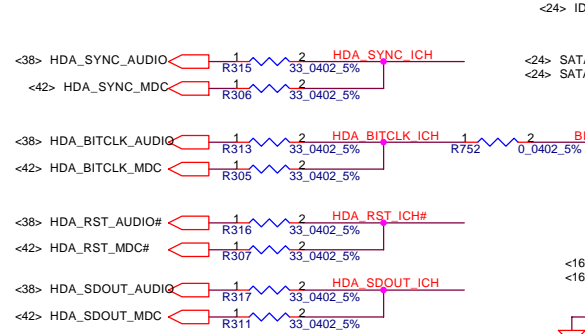
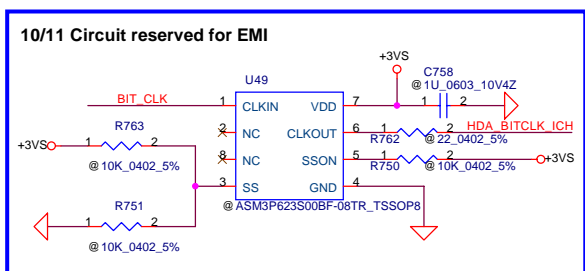
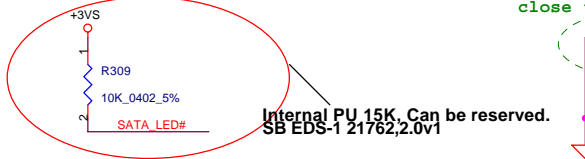
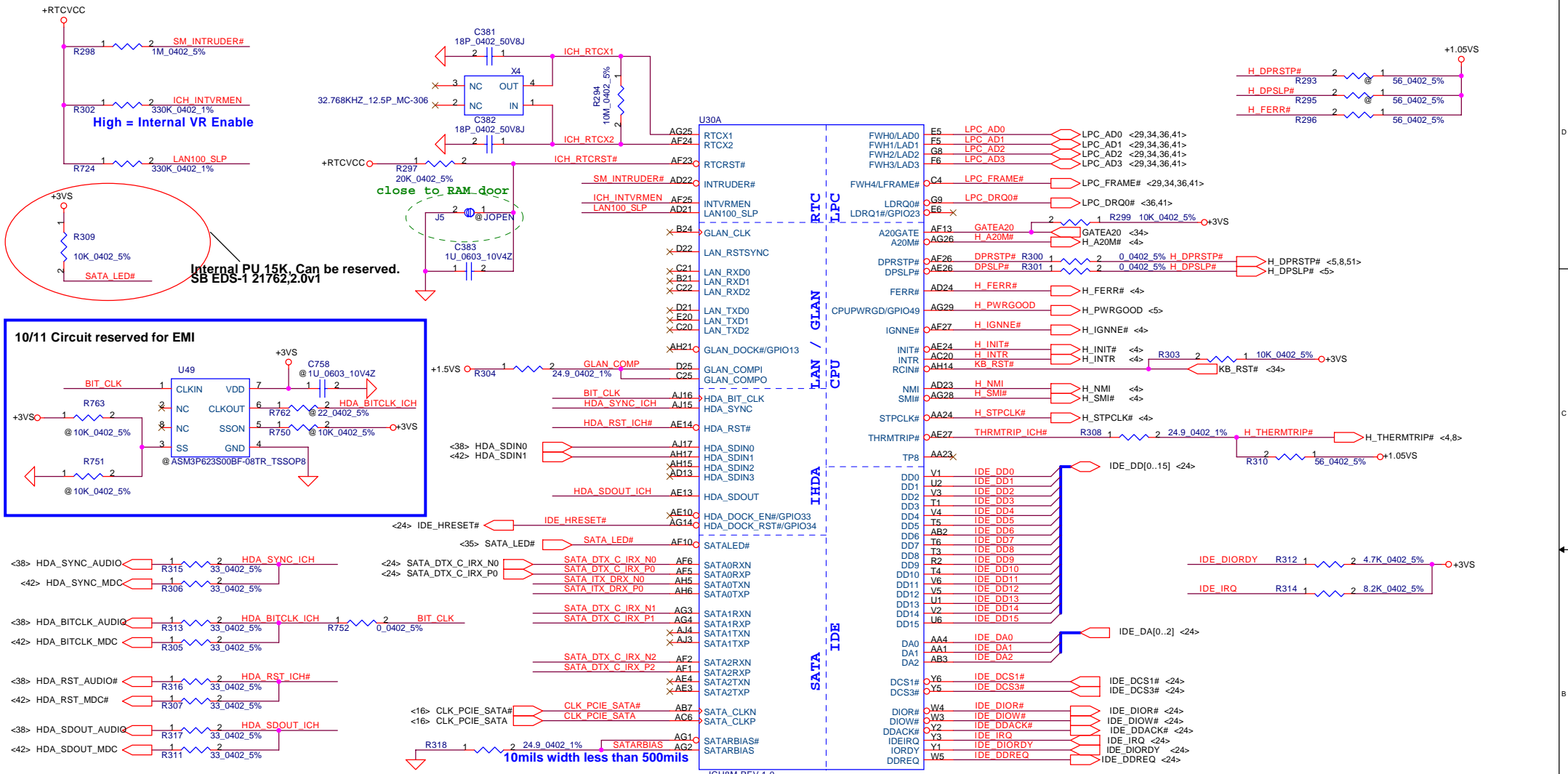


A16 Swap Override Strap
 PCI_GNT#3 Low= A16 swap override Enable
 High= Default*

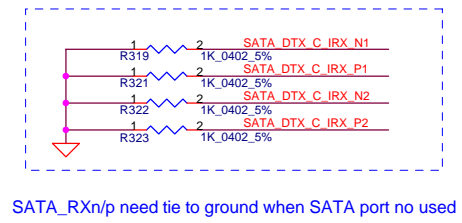


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

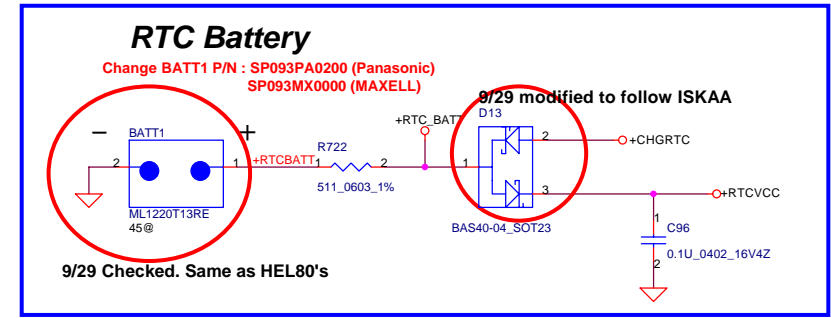




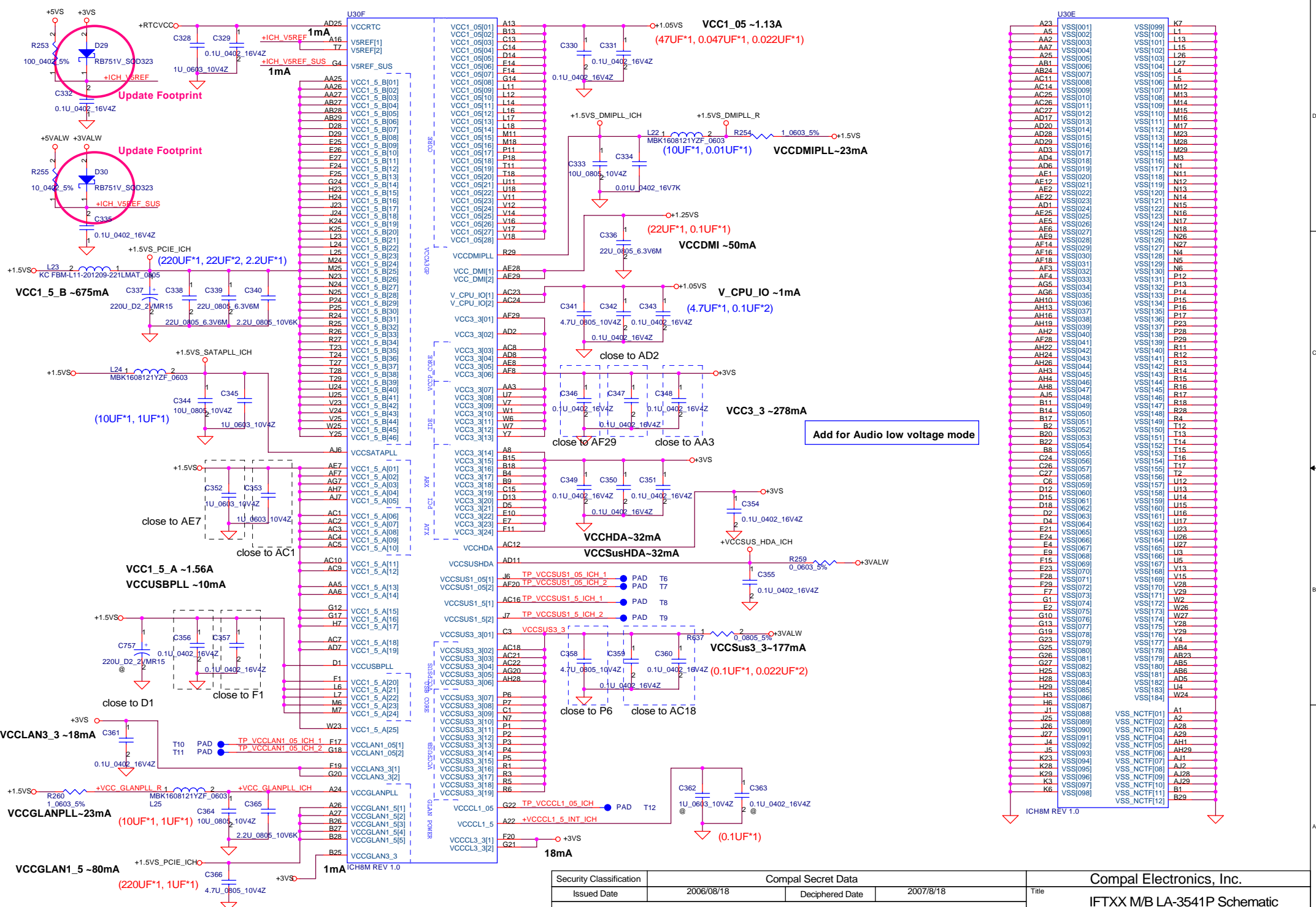
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1



SATA_RXn/p need tie to ground when SATA port not used



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Size	Document Number	Date		Rev
B	IFTXX M/B LA-3541P Schematic	Wednesday, November 01, 2006		0
		Sheet	21	of 52

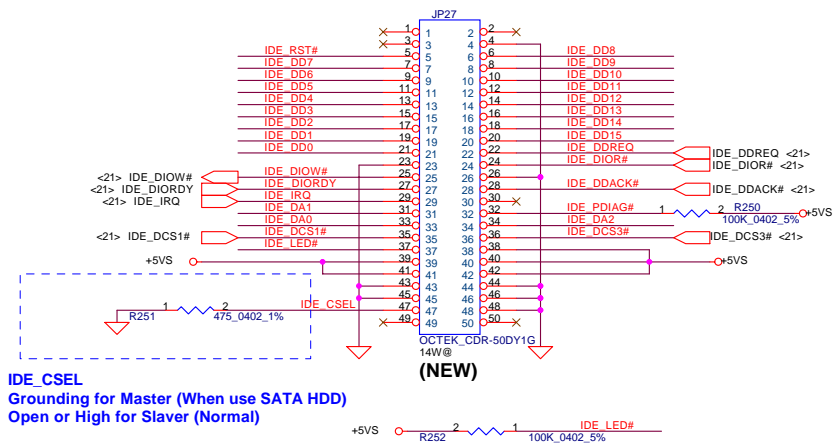
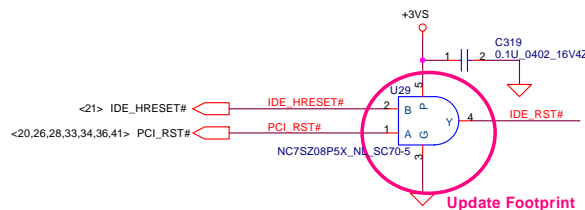
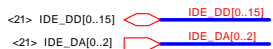
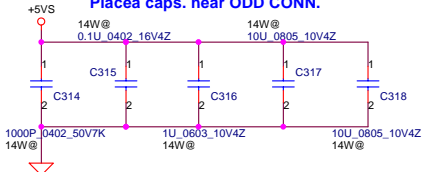


Security Classification		Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date	2007/8/18
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Compal Electronics, Inc.			
Title IFTXX MB LA-3541P Schematic			
Size	Document Number	Rev	
Custom	ICL50/ICK70 MB LA-3551P Schematic	0	
Date:	Wednesday, November 01, 2006	Sheet	23 of 52

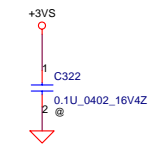
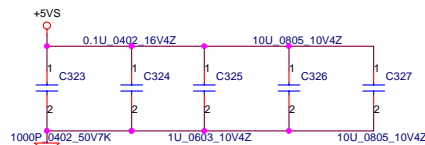
14W ODD Conn.

Place caps. near ODD CONN.



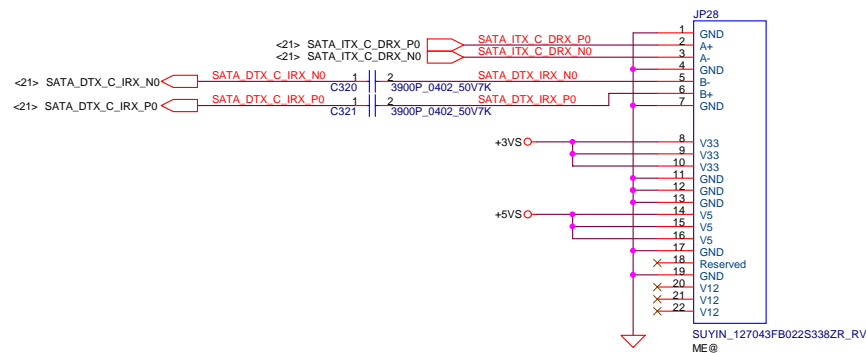
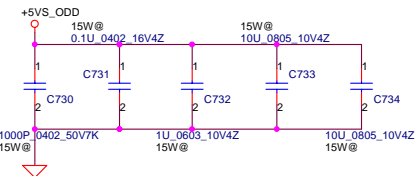
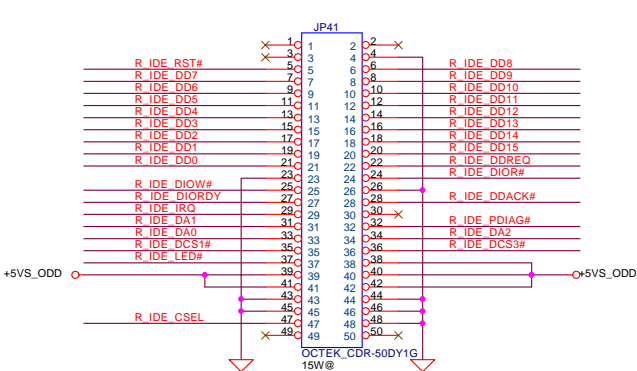
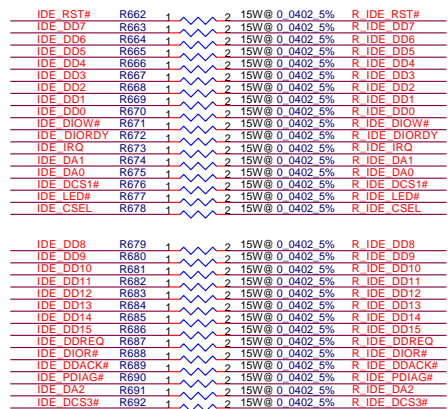
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

SATA HDD Conn.



15W ODD Conn.

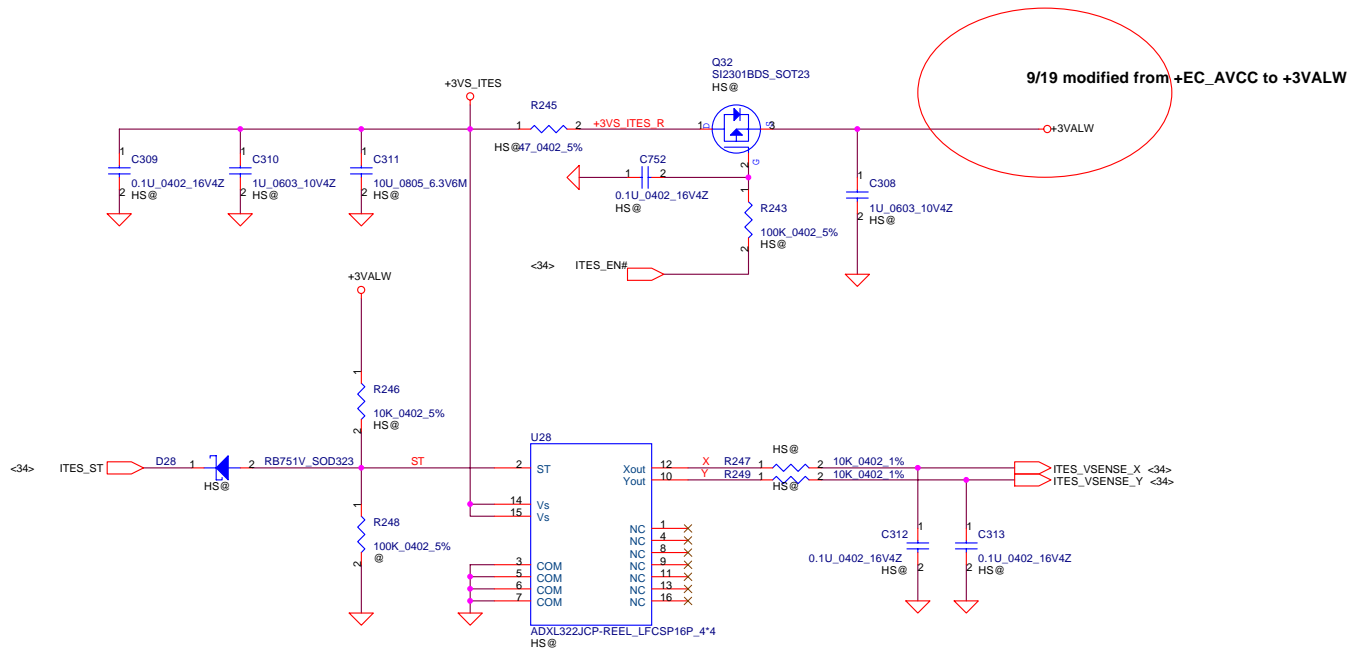
Remember Short at 15W@
PAD-OPEN 3x3m @

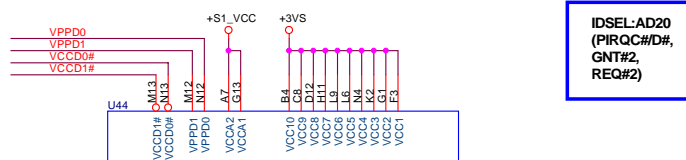


(NEW)
Change Library

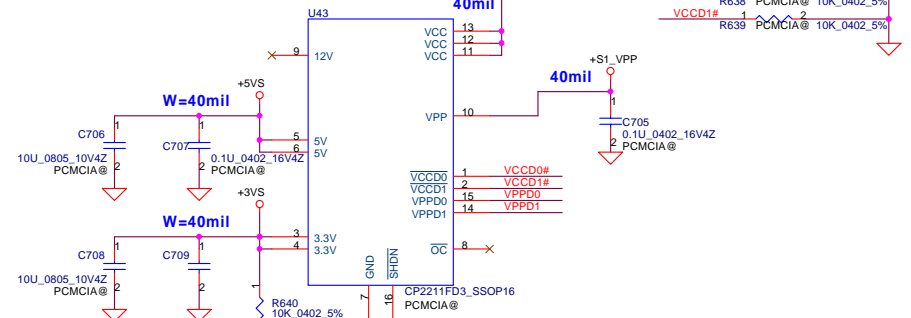
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	HDD & ODD Connector	
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				B	IFTXX/MB LA-3541P Schematic
				Date:	Rev 0
				Wednesday, November 01, 2006	Sheet 24 of 52

Note : BOM structure HS@ is for Heng shan IFT10/11 this model

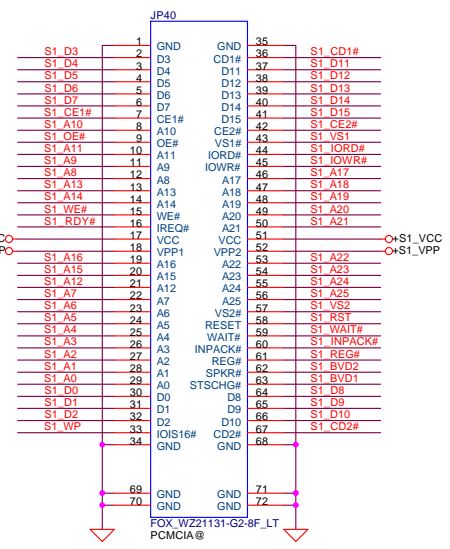




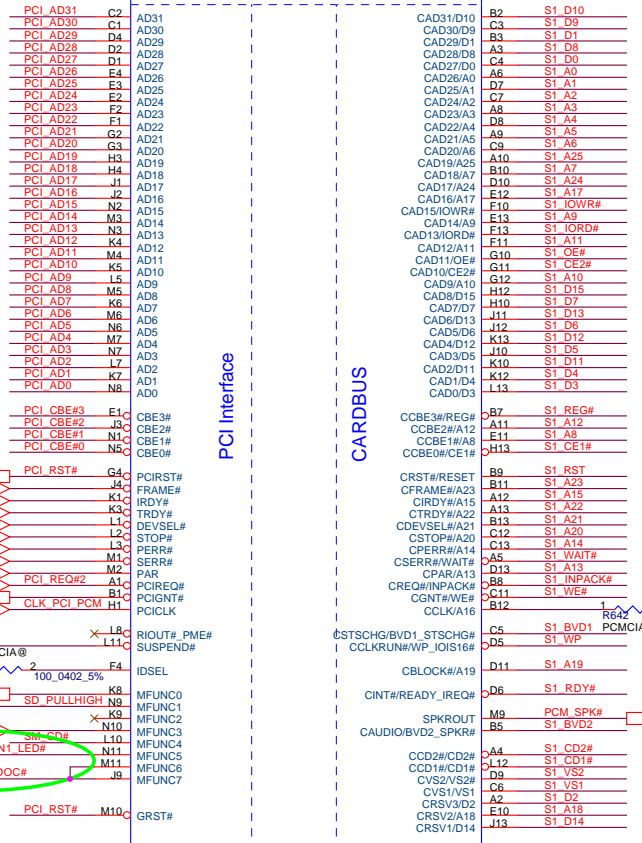
PCMCIA Power Control



PCMCIA Socket



ISEL:AD20
(PIRQC#D#,
GNT#2,
REQ#2)



PCI Interface

CARBUS

SD/MMC/MS/SM

NEED CHECK

10/17 : FootPrint : SA007140B10
BOM : SA014100310

CB1410 P/N: SA014100310

Security Classification		Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date	2006/10/06
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Compal Electronics, Inc.		
PCMCIA ENE CB1410		
Size	Document Number	Rev
Custom	IFTXX LA-3541P	0.1
Date	Wednesday, November 01, 2006	Sheet 26 of 52

5

4

3

2

1

D

D

C

C

B

B

A

A



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Wednesday, November 01, 2006	Sheet 27 of 52

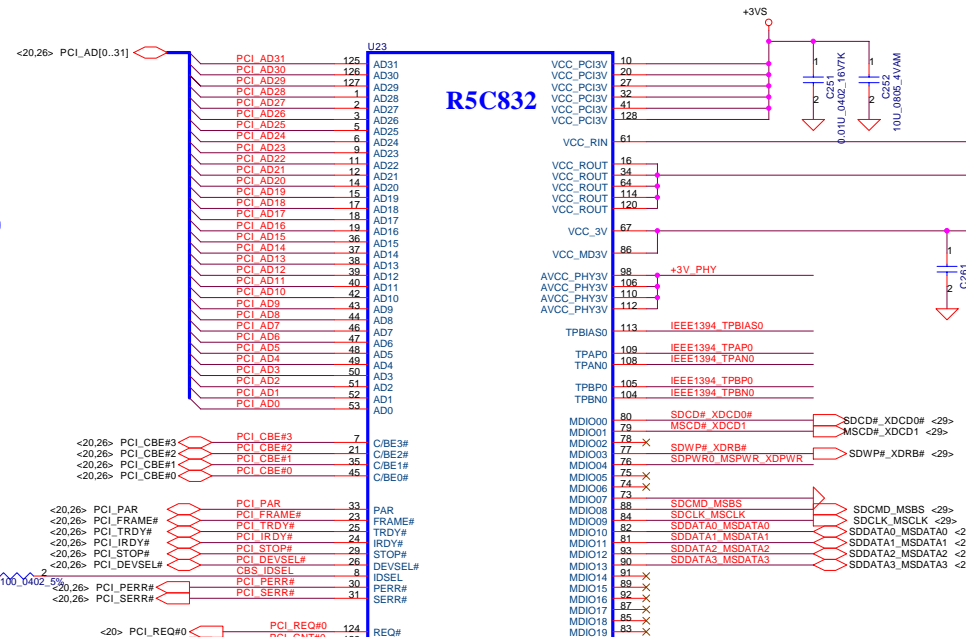
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4

3

2

1

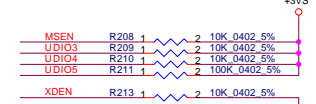


SD,MMC,MS multi-function pin define

MDIO	SD Card	MMC Card	MS Card
PIN Name	PIN Name	PIN Name	PIN Name
MDIO00	SDCD#	MMCCD#	
MDIO01			MSCD#
MDIO02			
MDIO03	SDWPH		
MDIO04	SDPWR0	MMCPWR	MSWR
MDIO05	SDPWR1		
MDIO06	SDLED#	MMCLED#	MSLED#
MDIO07			MSEXTC#
MDIO08	SDCCMD	MMCCMD	MSBS
MDIO09	SDCLK	MMCLK	MSCCLK
MDIO10	SDCDAT0	MMCDAT	MSCDAT0
MDIO11	SDCDAT1		MSCDAT1
MDIO12	SDCDAT2		MSCDAT2
MDIO13	SDCDAT3		MSCDAT3
MDIO14			
MDIO15			
MDIO16			
MDIO17			
MDIO18			
MDIO19			

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-low	Enable SD, MS, MMC Card



Layout Note: Shield GND for CLK_PCI_1394

Layout Note: C268, C270, R125 Place close to R5C832 and Shield GND for FILO,REXT,VREF

Layout Note: Place close to R5C832 and Shield GND for SDCLK_MSCLK

Layout Note: Place close to R5C832 and Shield GND for SD_CLK

Solve MS Duo Adaptor short problem

Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK

Layout Note: Place close to R5C832

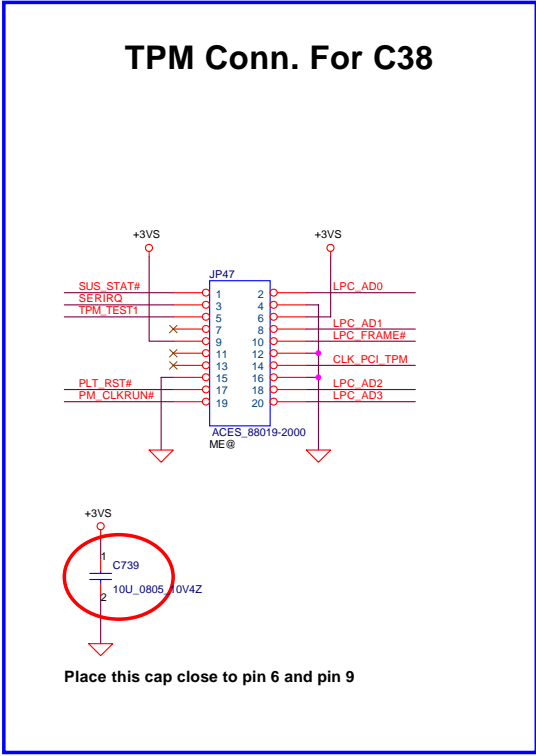
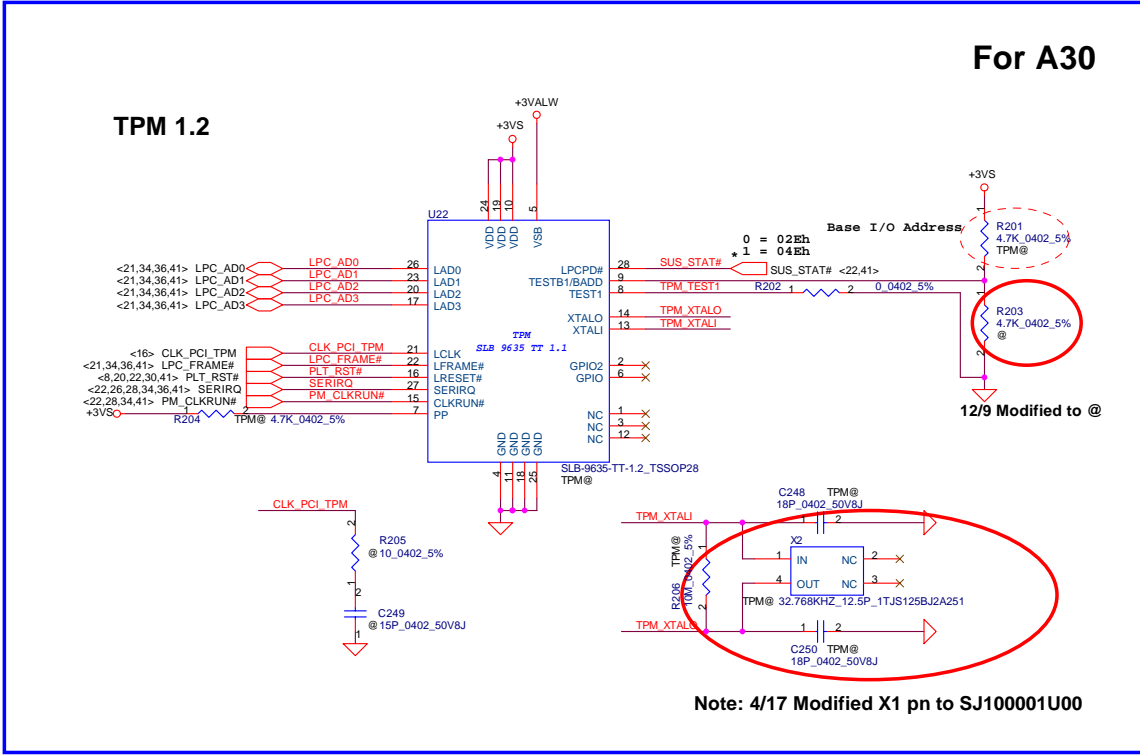
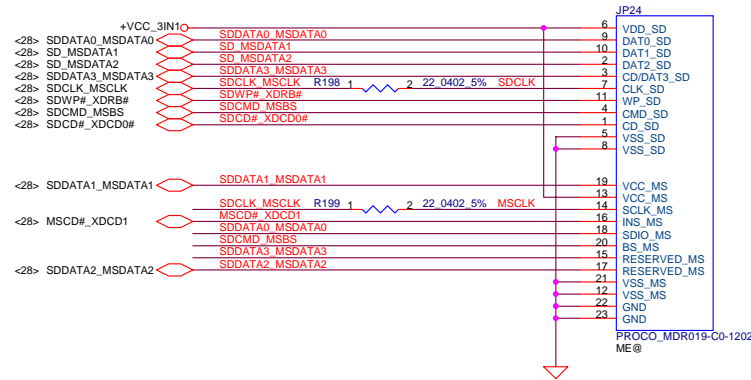
IEEE1394TPA+/- and IEEE1394TPB+/- Same Wire Length

Layout Note: Shield GND for IEEE1394_TPA and TPB

Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date 2006/10/06

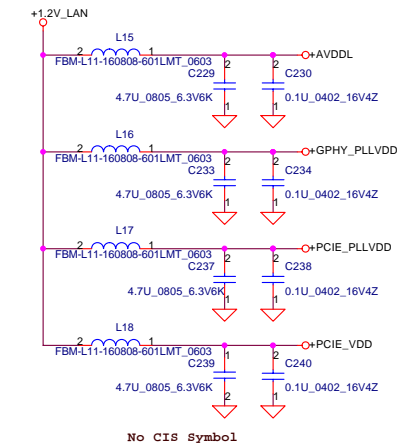
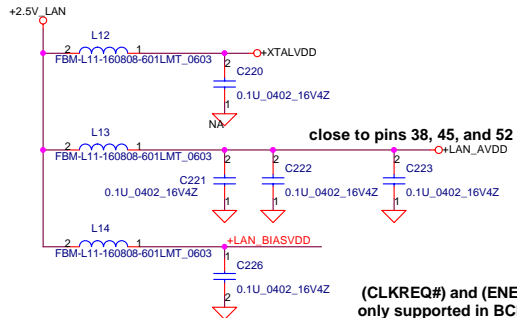
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3 in 1 Card Reader

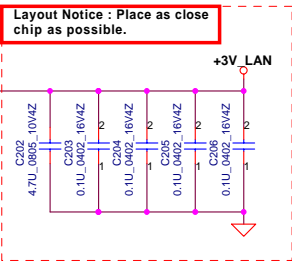
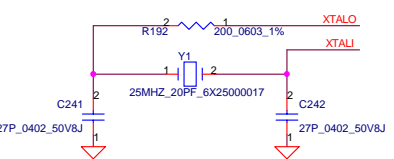


Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	INDICATE LED
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				Document Number XXXXX LA-3541P
				Rev 0.1
				Date: Wednesday, November 01, 2006
				Sheet 29 of 52

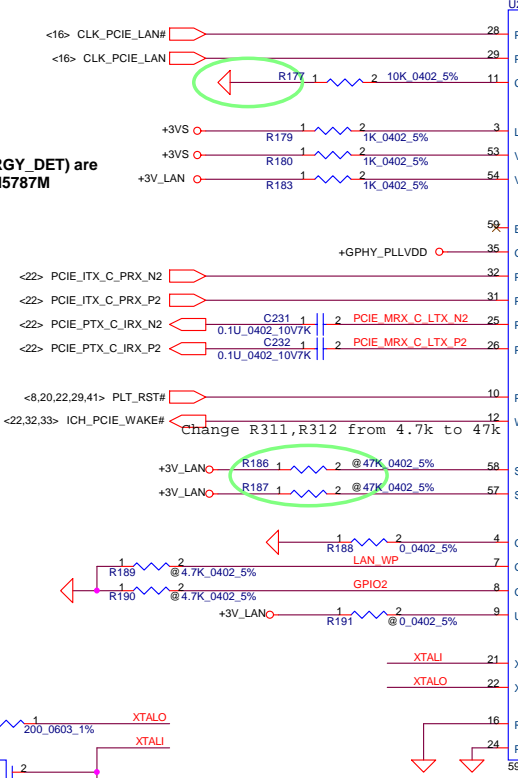
Layout Notice : Filter place as close chip as possible.



No CIS Symbol



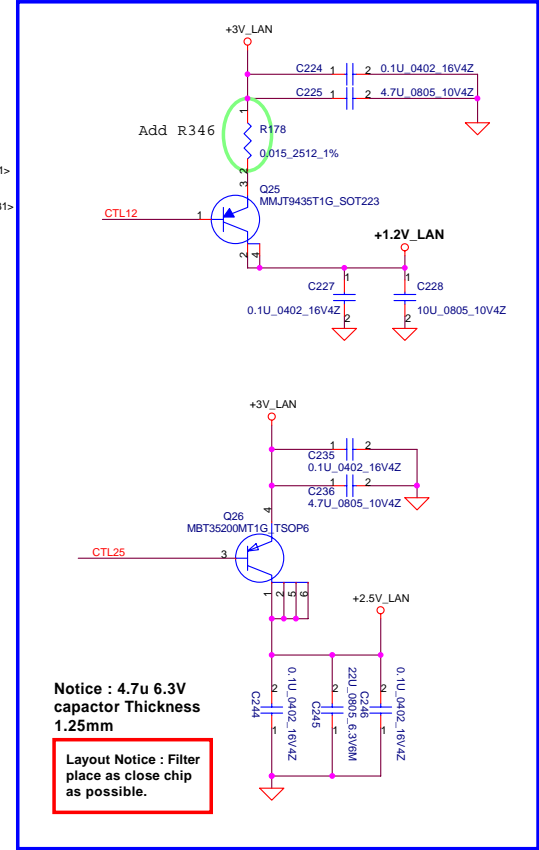
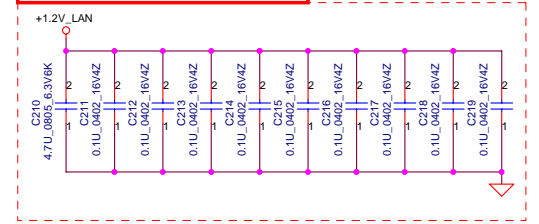
Layout Notice : Place as close chip as possible.



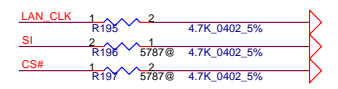
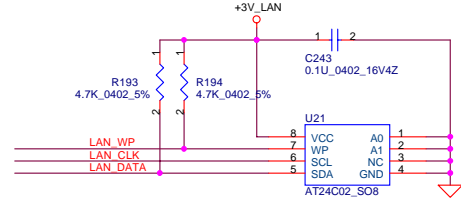
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

9/14 change from 1.24K to 1K (By broadcom James)

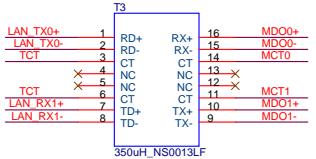
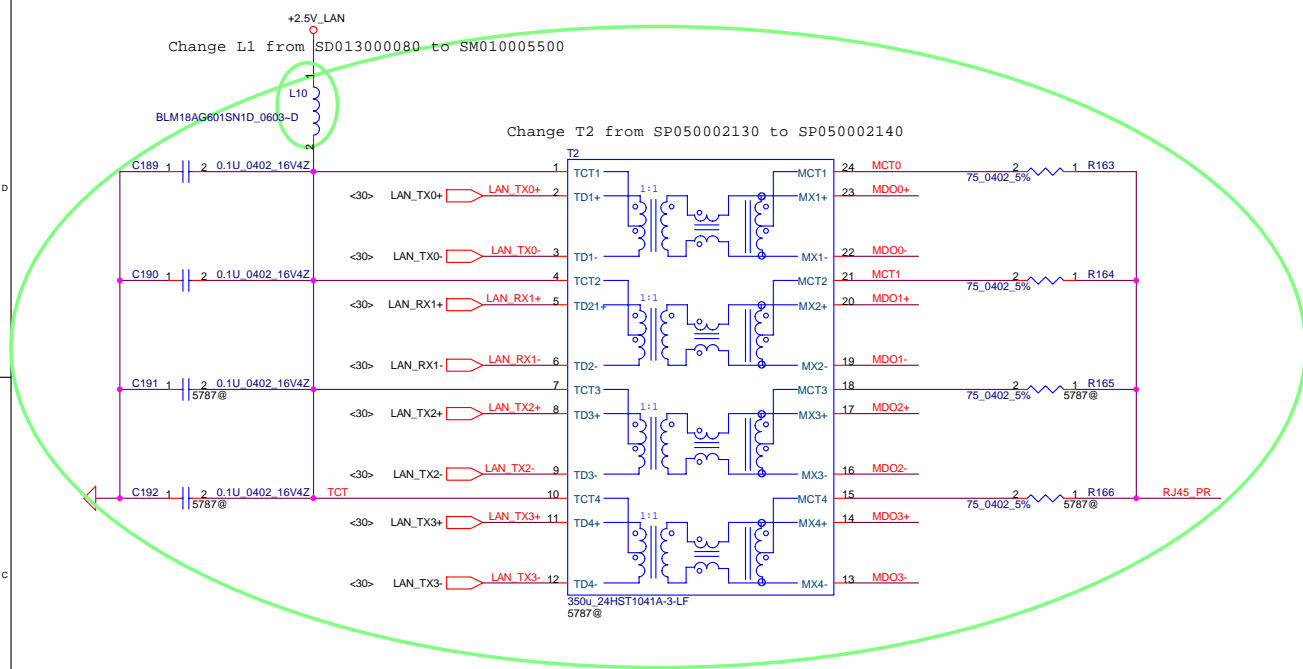
Layout Notice : 1.2V filter. Place as close chip as possible.



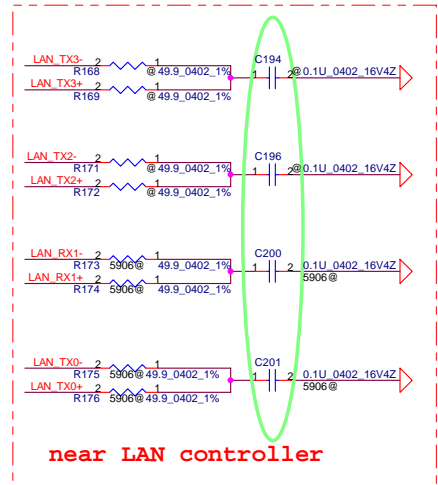
Layout Notice : Filter place as close chip as possible.



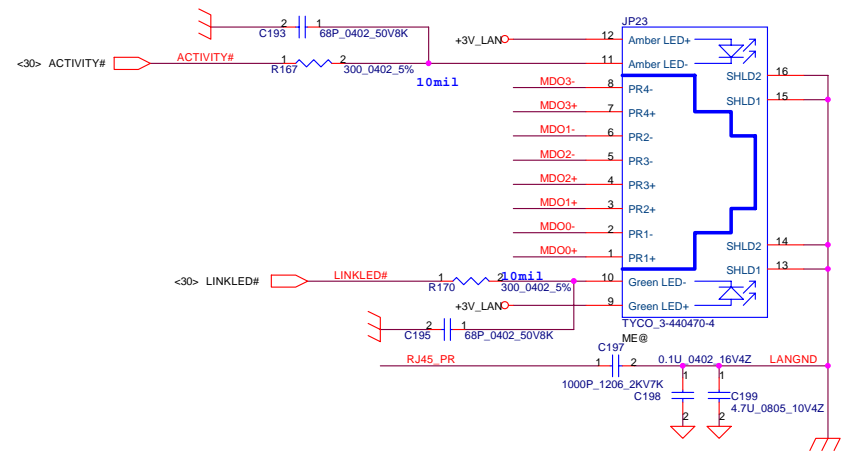
Security Classification				Compal Secret Data				Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	BCM5787MKML				Size	Document Number
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				Date: Wednesday, November 01, 2006				Sheet	30 of 52



Change T1 from SP050001210 to SP050001210
 Change C468, C470, C473, C474, C475, C476 from 0.01uF to 0.1uF

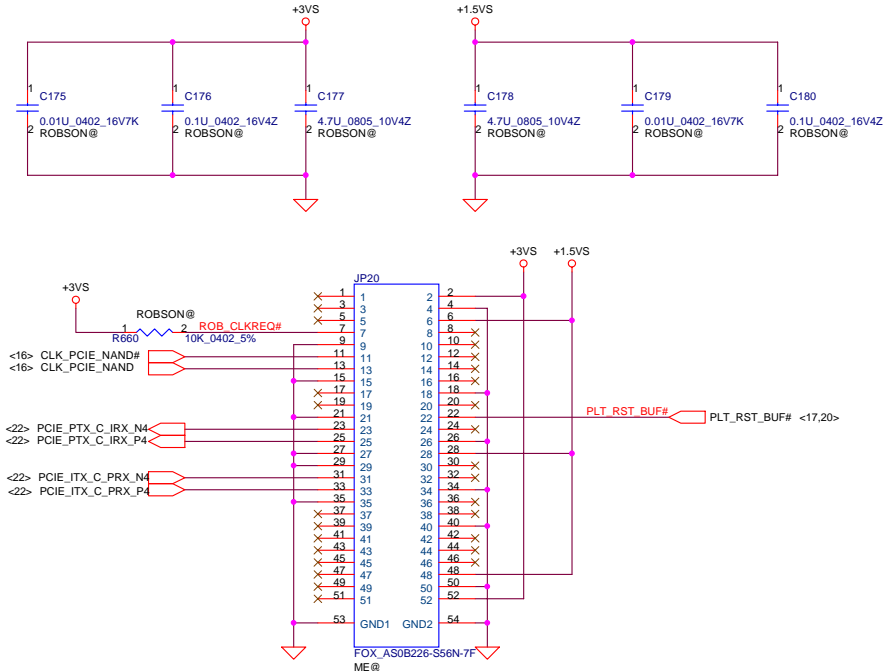


Lan Conn.

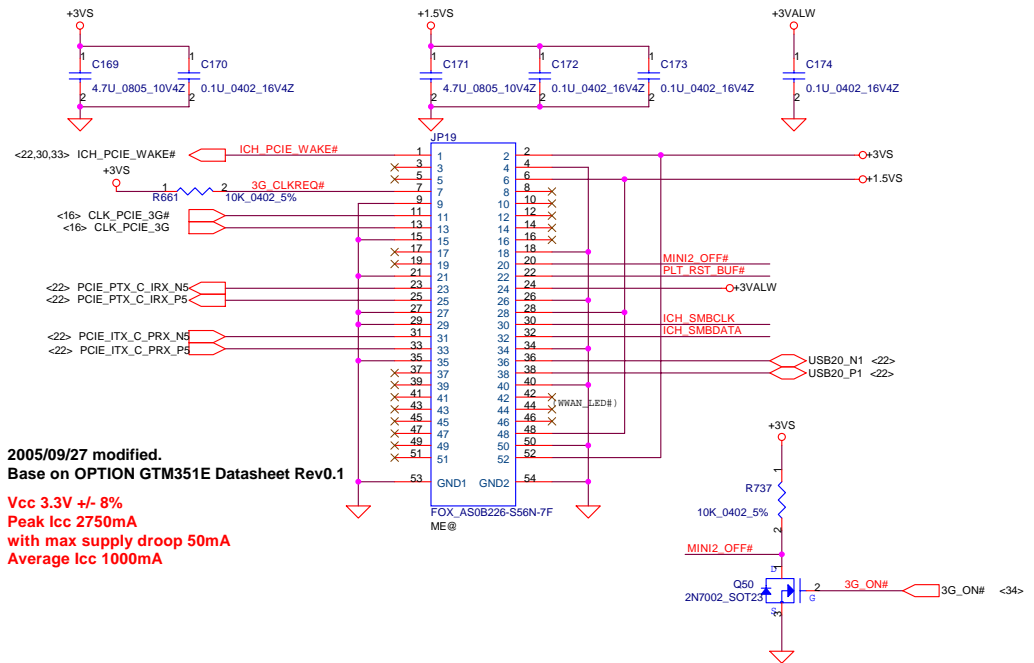


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Date:	Wednesday, November 01, 2006	Sheet	31	of	52	Rev 0.1

NAND mini Card(Robson support)

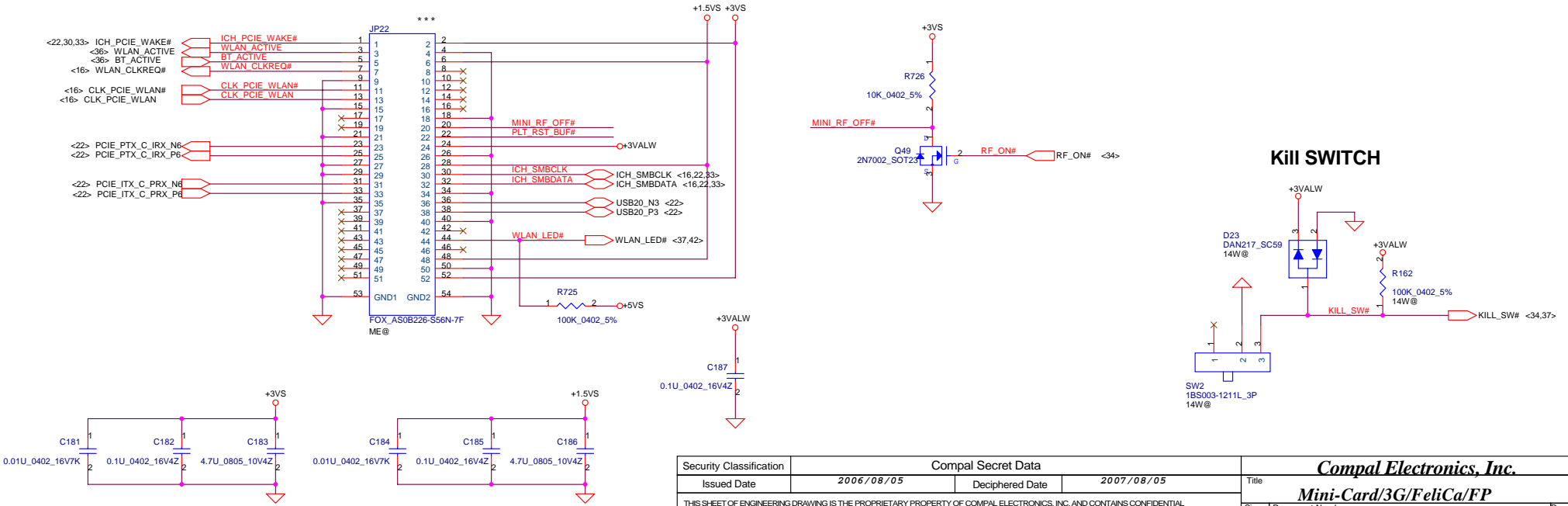


Mini-Express Card for 3G Or TV Tuner



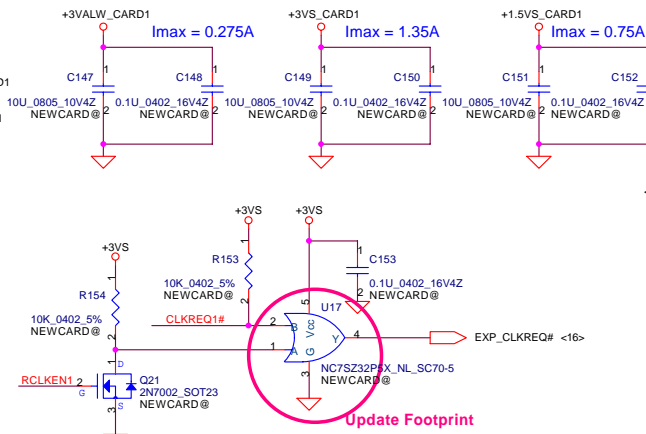
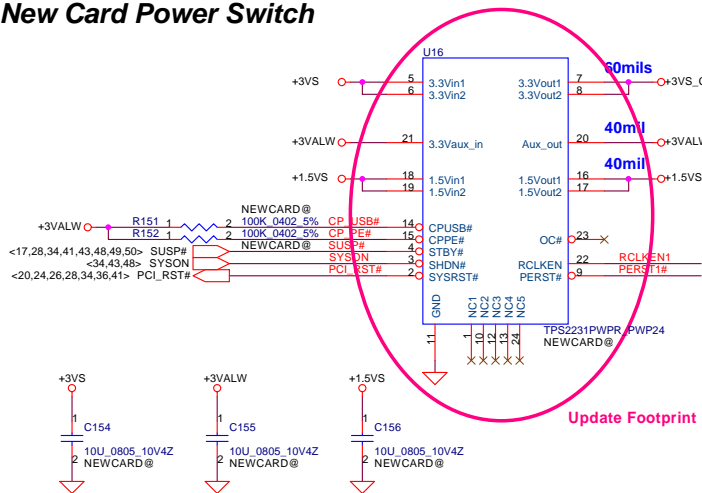
2005/09/27 modified.
 Base on OPTION GTM351E Datasheet Rev.0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Mini-Express Card for WLAN

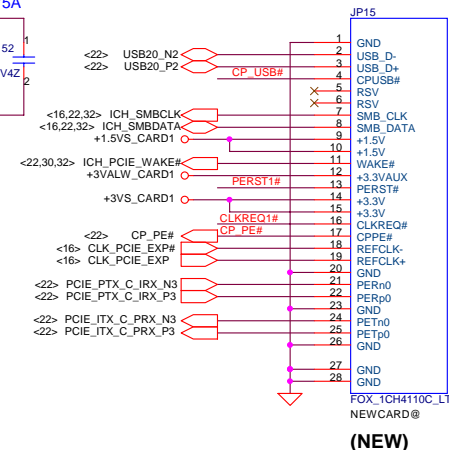


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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Compal Electronics, Inc.	
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Size	Document Number	LA-3541P		Rev	0.1
Date:	Wednesday, November 01, 2006	Sheet	32	of	52

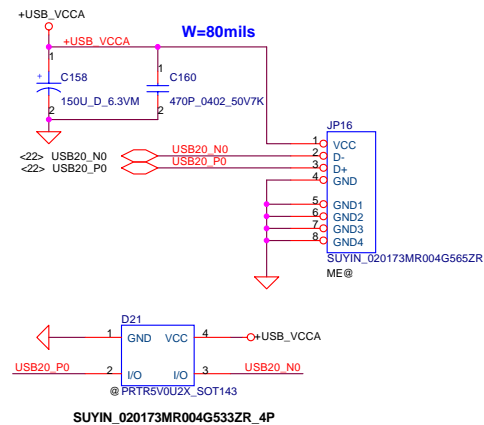
New Card Power Switch



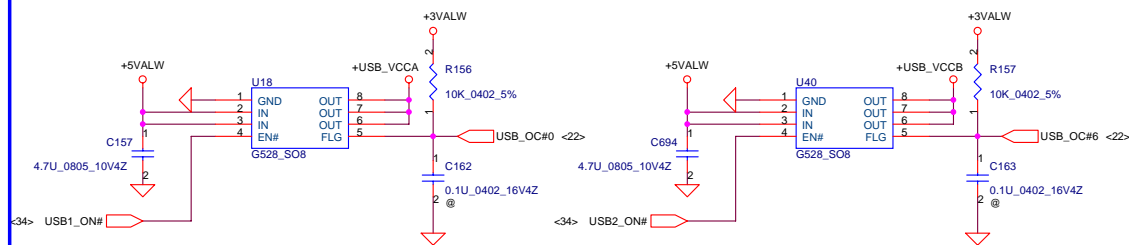
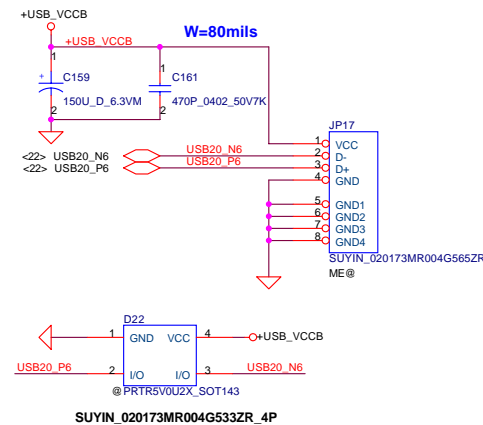
New Card Socket (Left/TOP)



USB CONN. 1

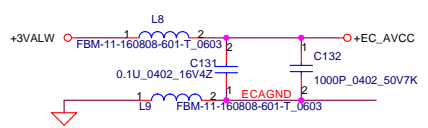


USB CONN. 2

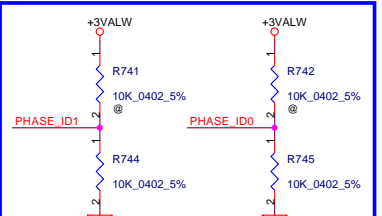
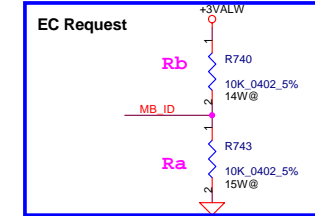
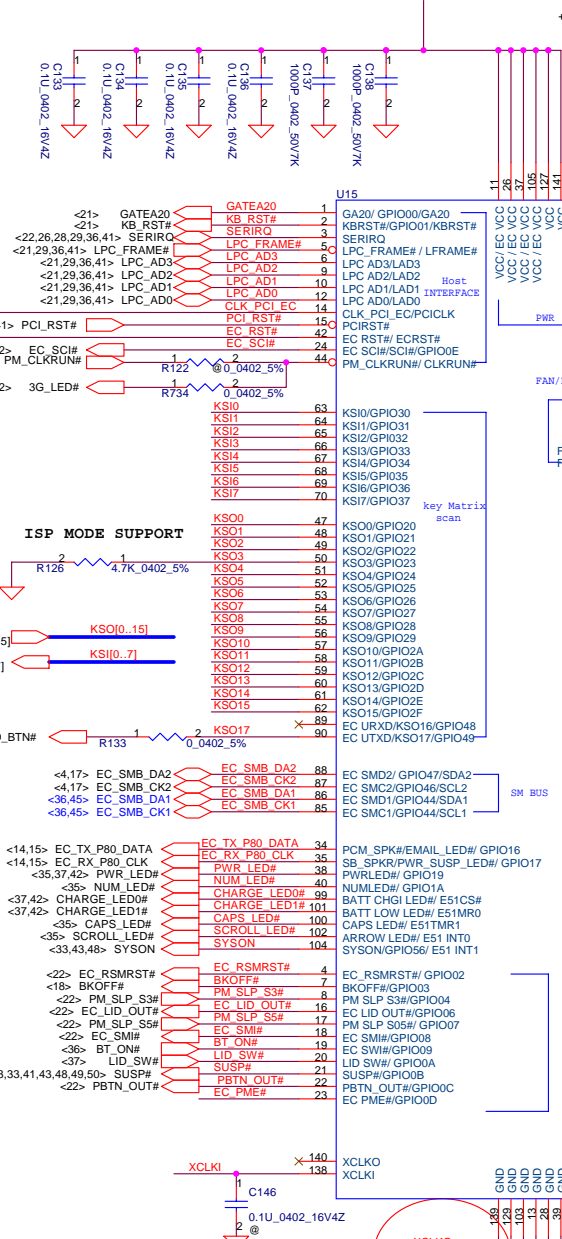
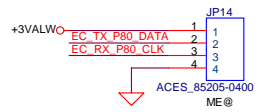


9/17 modified this block

Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	NEW CARD & USB Connector
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Date:	Wednesday, November 01, 2006	Sheet	33	of 52

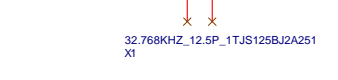
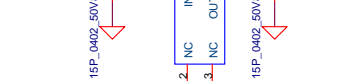
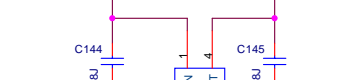
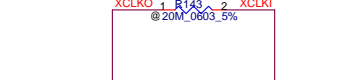
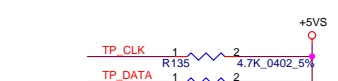
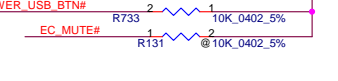
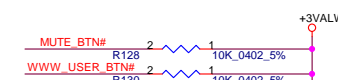
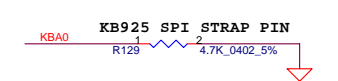


EC DEBUB PORT



ID1	ID0	Test Mode
0	0	A-Test
0	1	B-Test
1	0	C-Test

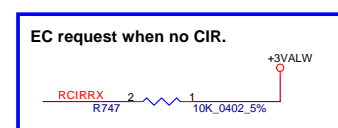
EC Request



10/17 : Change P/N from SA009100120 to SA00001HZ00

10/17 : FootPrint : SA009100120 BOM : SA00001HZ00

KB925 should use Data code 06361 which has fixed bonding issue
KB925 pin 139 is used for XCLKO, Pin 140 NC



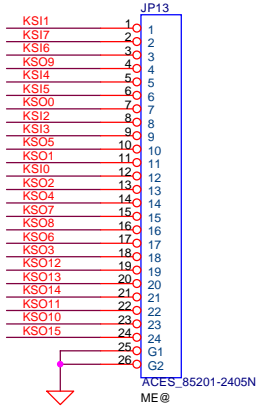
Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date
		2006/10/06

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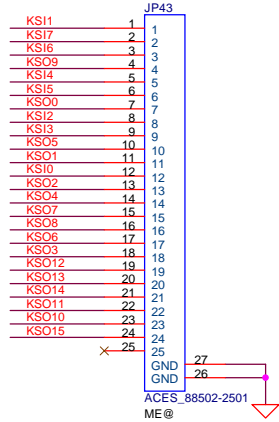
Title		Compal Electronics, Inc.	
ENE-KB925		Size	Document Number
Customer	IEL10 LA-3451P	Rev	0.1
Date:	Wednesday, 01/20/06	Sheet	34 of 52

INT_KBD Conn.

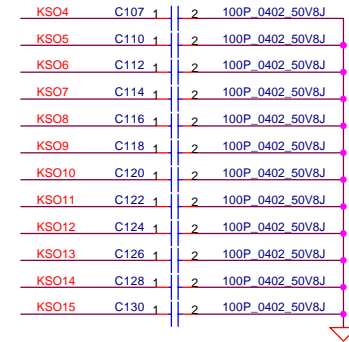
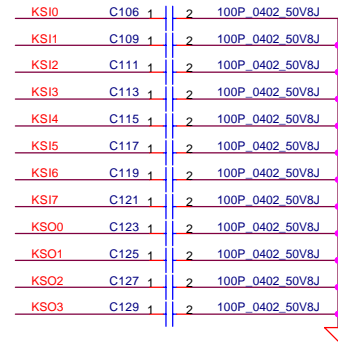
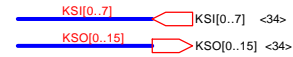
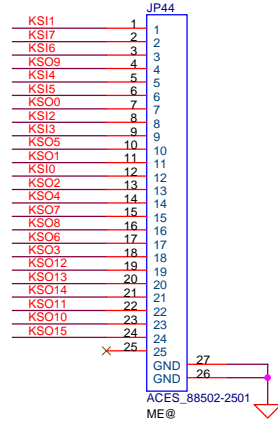
For IFT10



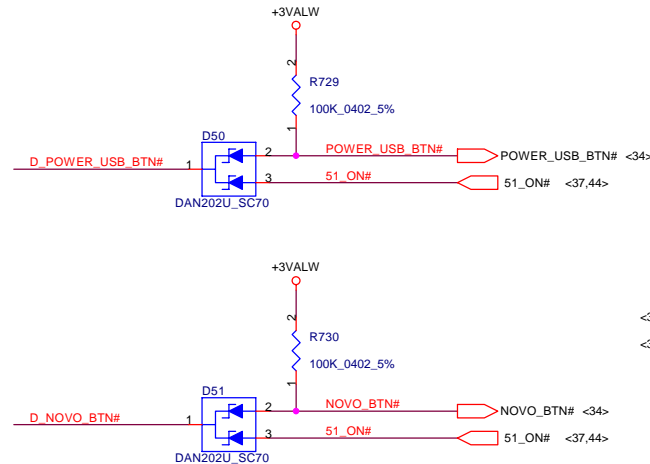
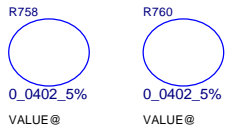
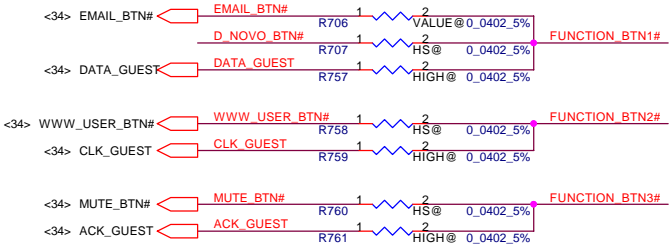
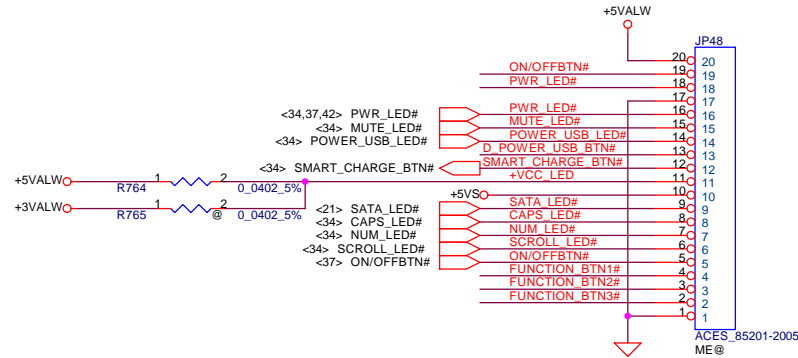
For IFL90



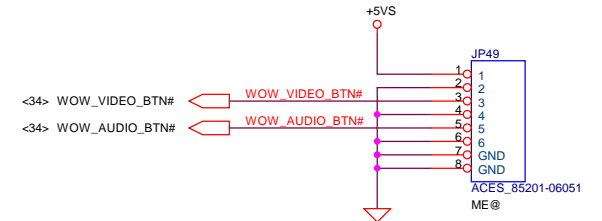
For IFT00



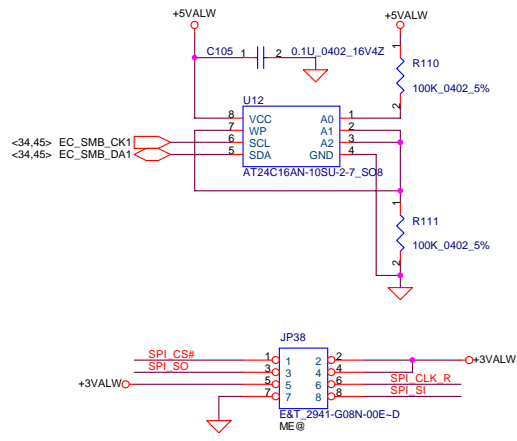
Switch Board Conn.



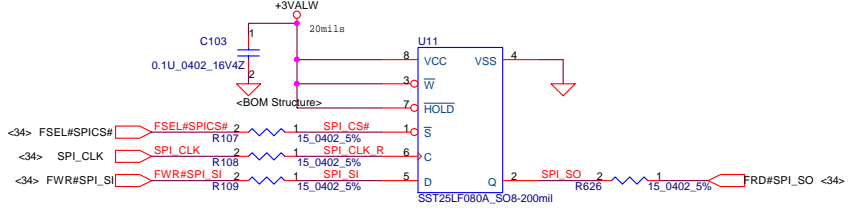
Video Switch Board Conn.



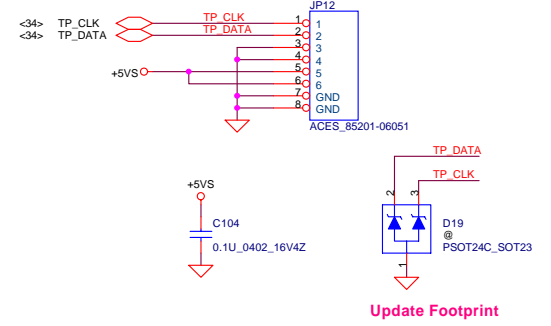
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	EC ENE KB910L(Reserved)
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			Document Number	Rev
			IFTXX M/B LA-3541P Schematic	0
Date:		Wednesday, November 01, 2006		Sheet
				35 of 52



8M SPI ROM

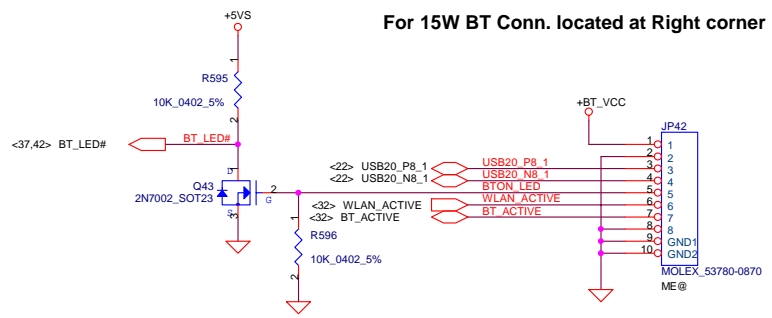


To TP/B Conn.

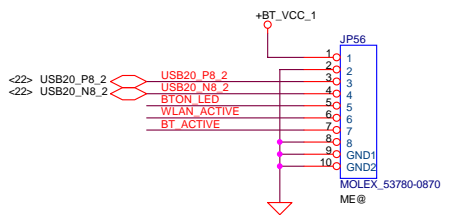


Bluetooth Conn.

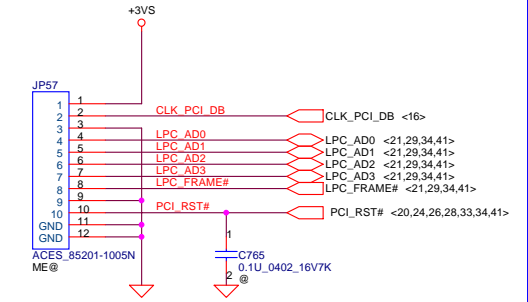
Need to check BT pin definition again!
9/20 modified this block



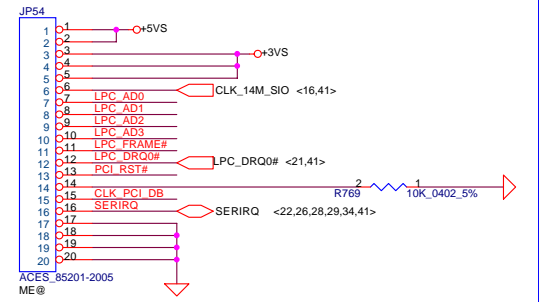
For 14W BT Conn. located at Left corner



FOR LPC DEBUG PORT

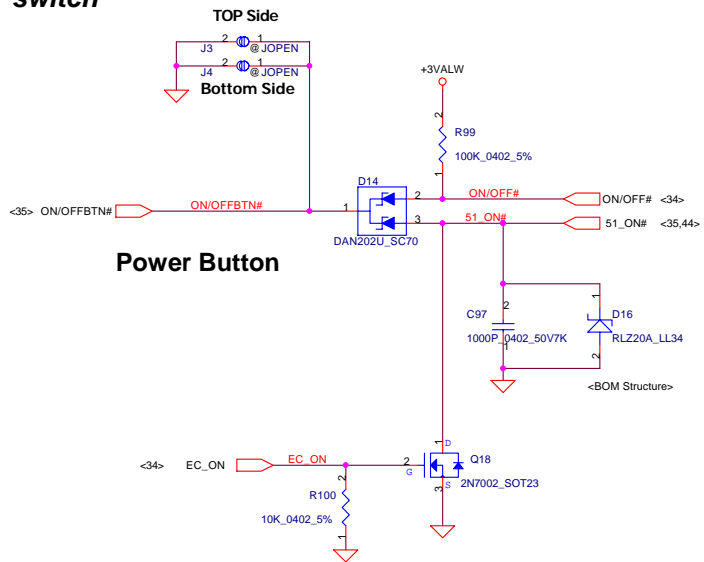


FOR LPC SIO DEBUG PORT

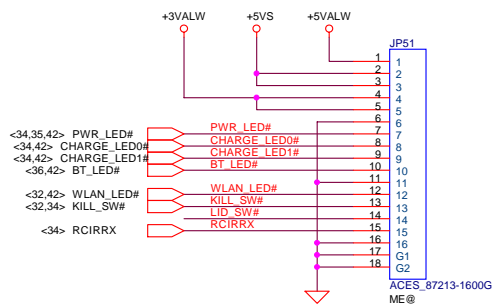


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Size	Document Number	Rev		
B	IFTXX M/B LA-3541P Schematic	0		
Date:	Wednesday, November 01, 2006	Sheet	36 of 52	

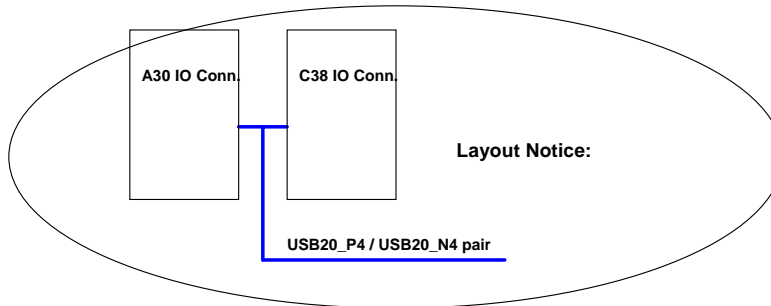
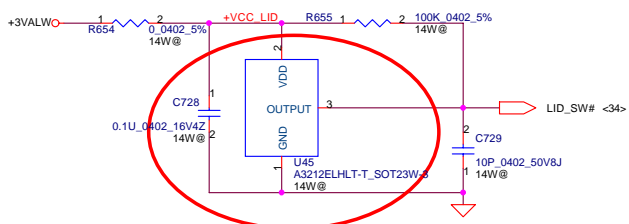
ON/OFF switch



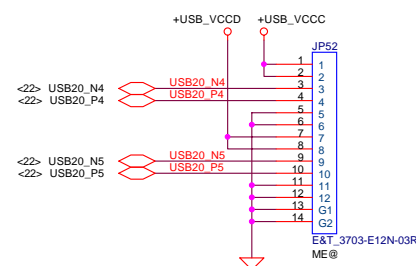
Front LED Board



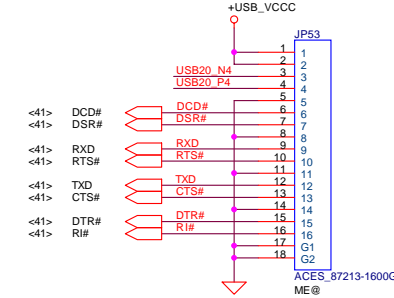
Lid Switch



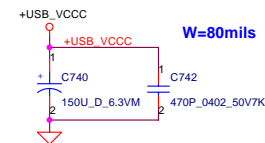
For A30 IO Conn.



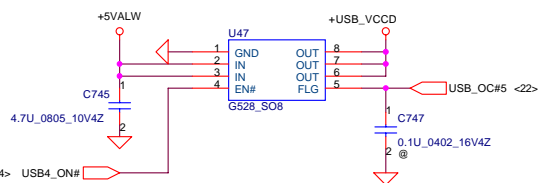
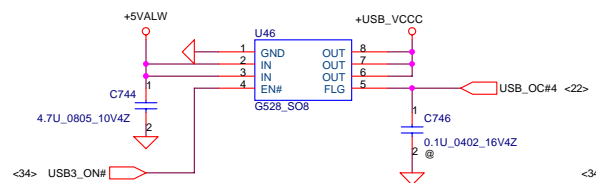
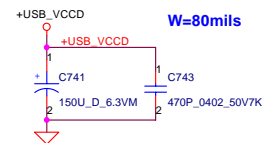
For C38 IO Conn.



To USB CONN. 3

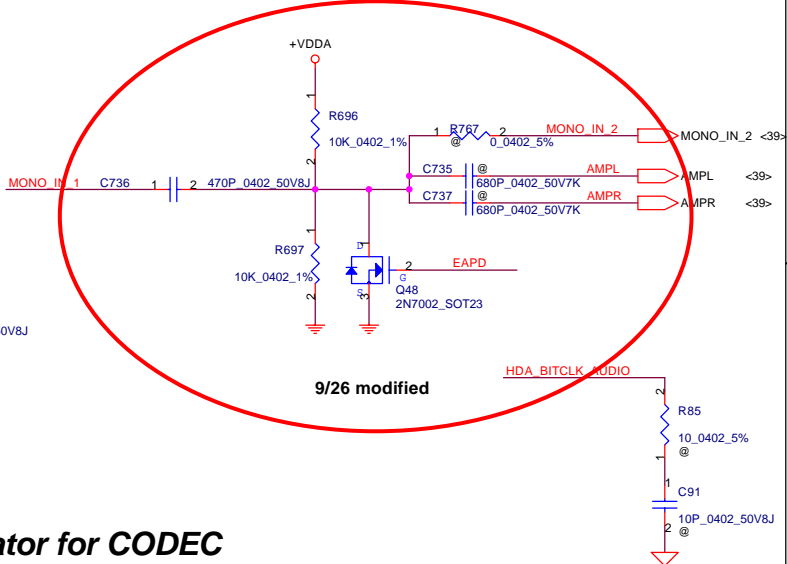
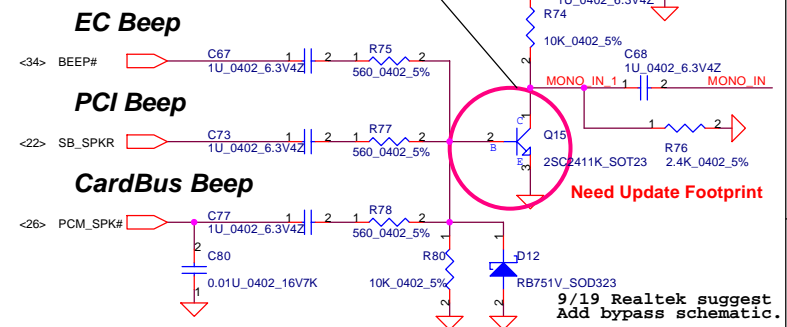
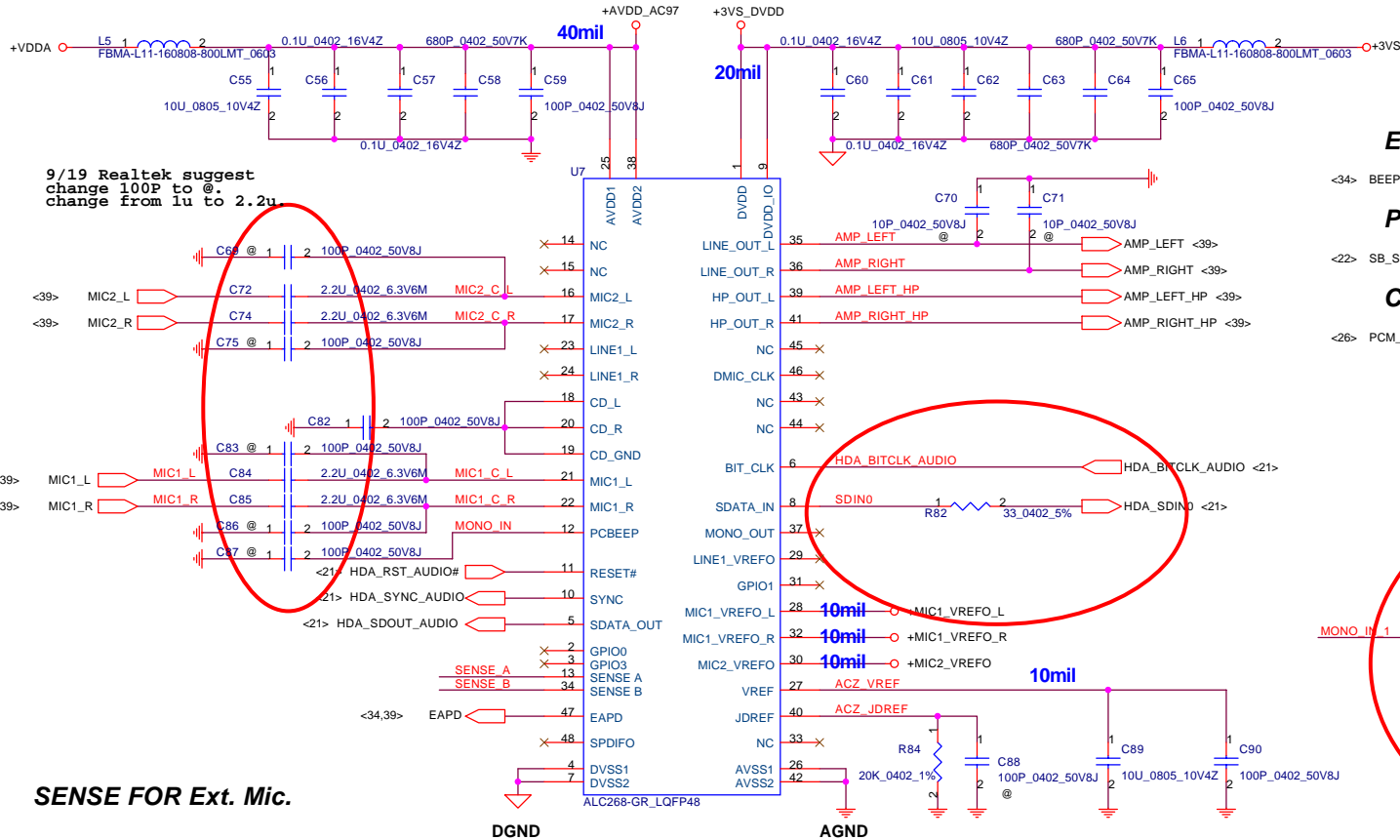


To USB CONN. 4



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				IFTXX MB LA-3541P Schematic	
Date:	Wednesday, November 01, 2006	Sheet	37	of	52

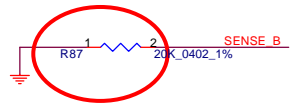
HD Audio Codec



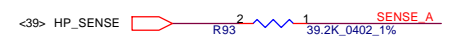
SENSE FOR Ext. Mic.



SENSE FOR Solo Int. Mic.

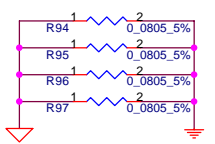


SENSE FOR HP

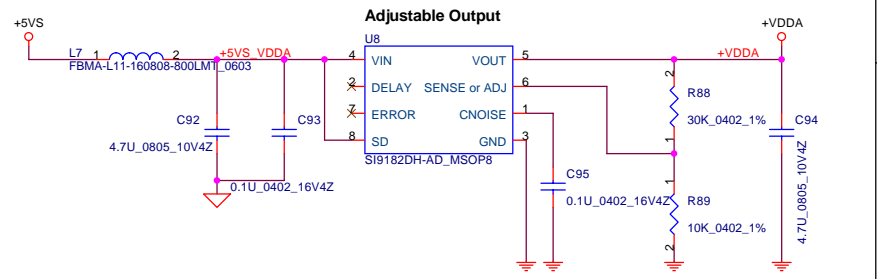


Sense Pin	Impedance	Codec Signals	Function
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
SENSE B	5.1K	PORT-D (PIN 35, 36)	LINE Out
	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Moat Bridge



Regulator for CODEC



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Compal Electronics, Inc.

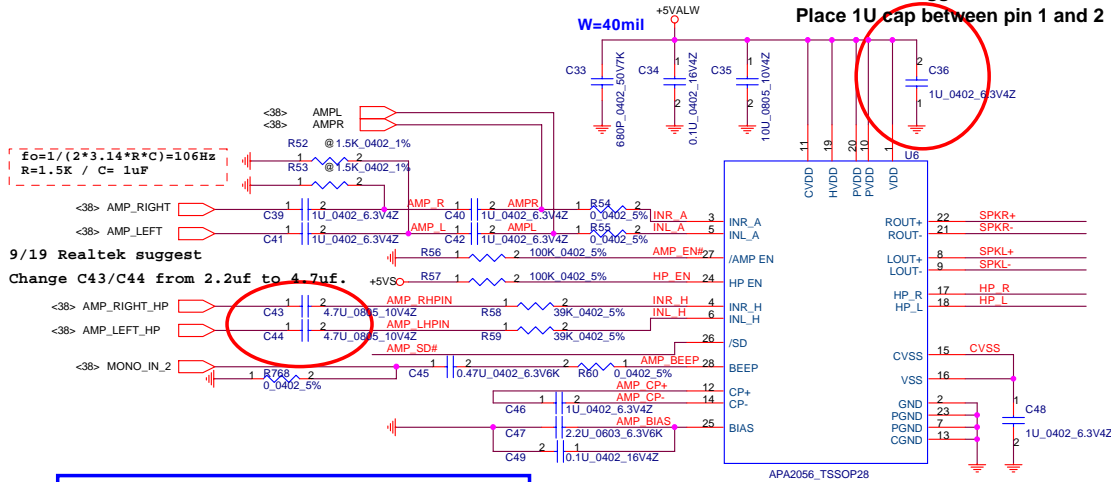
HD Audio Codec ALC268

Document Number: **LA-3541P**

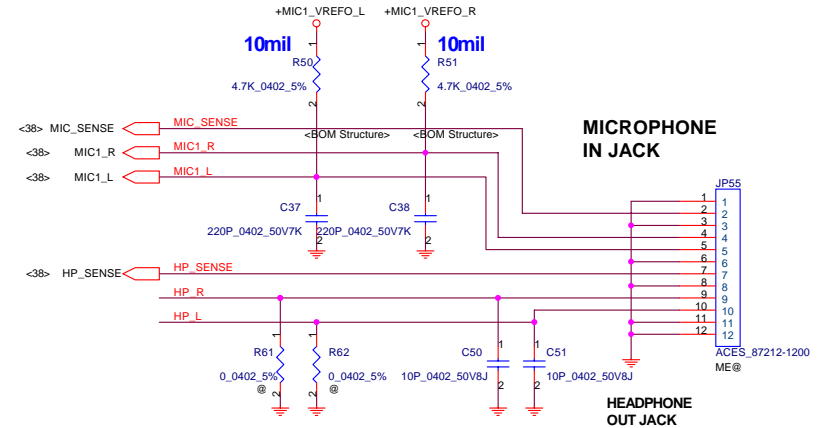
Rev: 0.1

APA2056 SPK/HP Amplifier

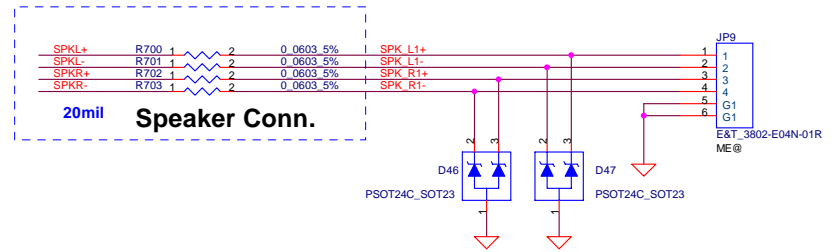
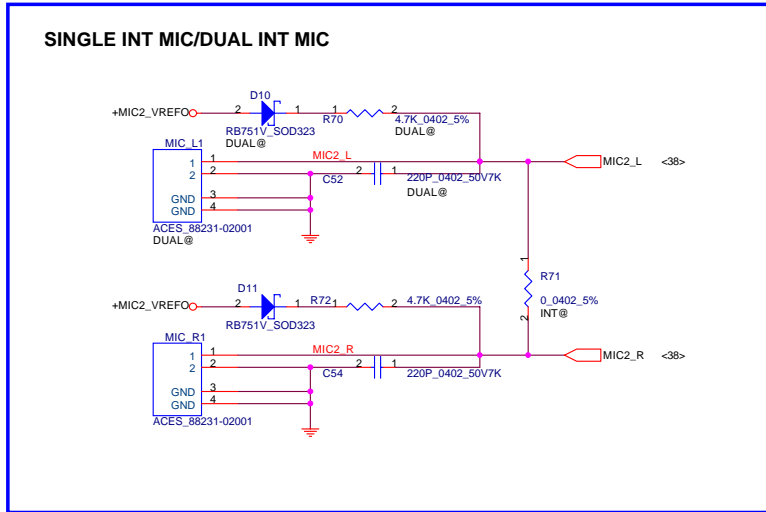
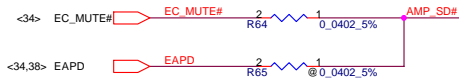
9/5 ANPEC Suggest
Place 1U cap between pin 1 and 2



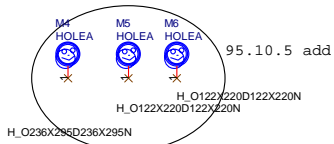
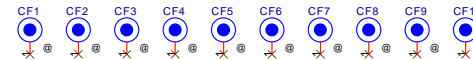
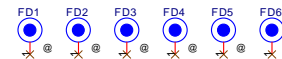
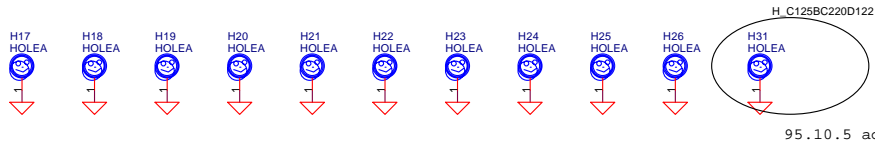
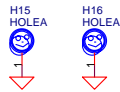
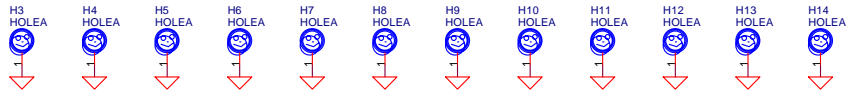
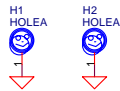
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



9/5 If implement AMP BEEP, Swap C155 and R79.
R79 change from 0 Ohm to 47K



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Custom	LA-3541P	0.1		
Date:	Wednesday, November 01, 2006	Sheet	39	of 52

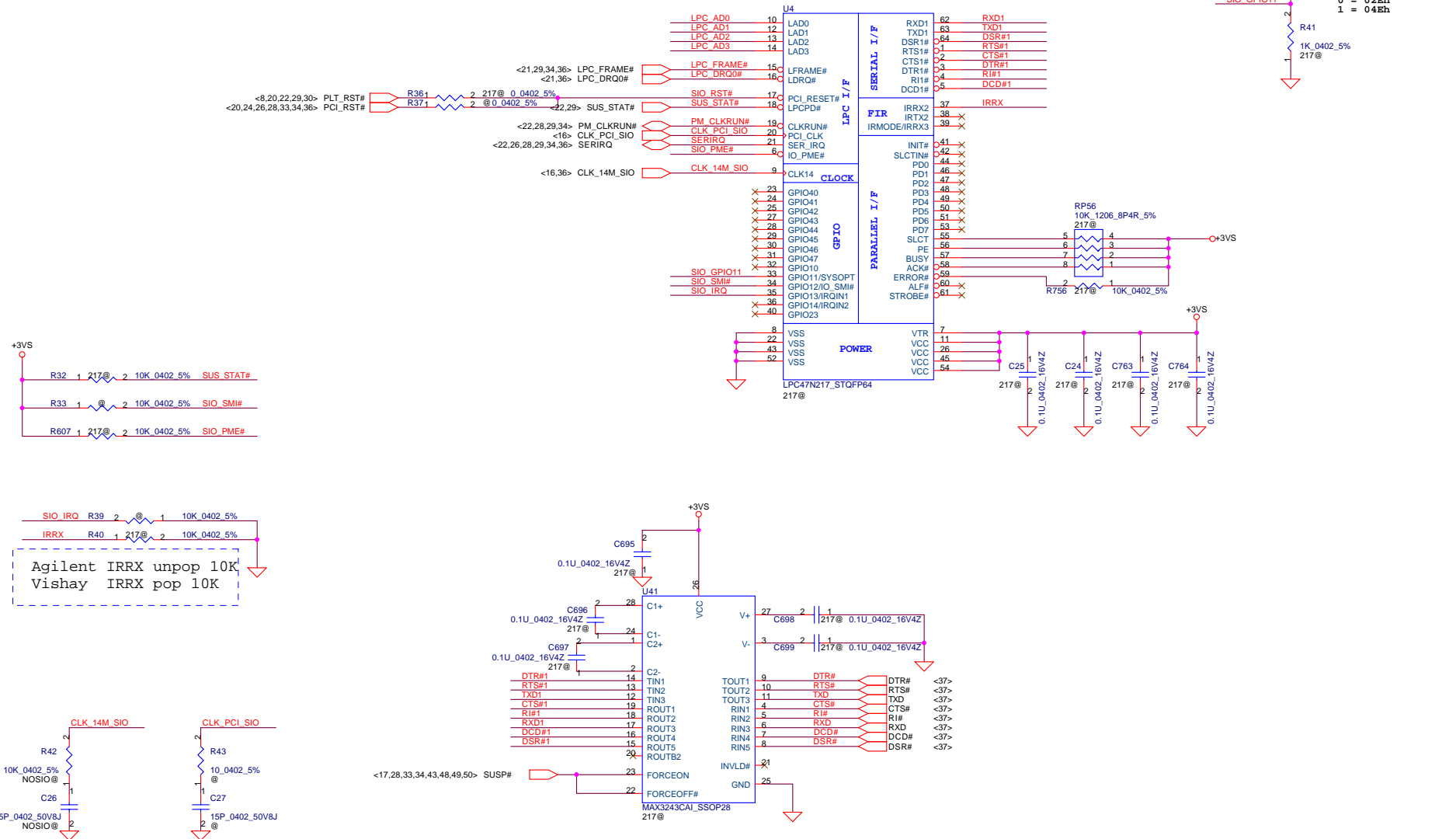


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Date: Wednesday, November 01, 2006				Sheet	40 of 52

SUPER I/O SMsC LPC47N217

<21,29,34,36> LPC_AD[0..3] \diamond LPC AD[0..3]

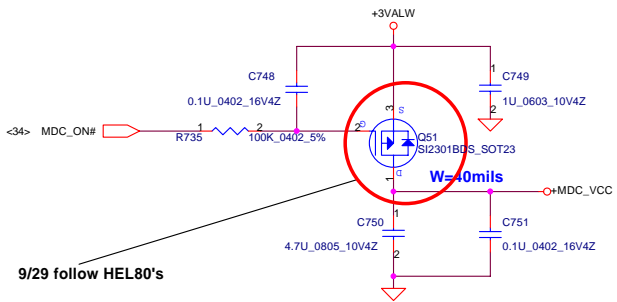
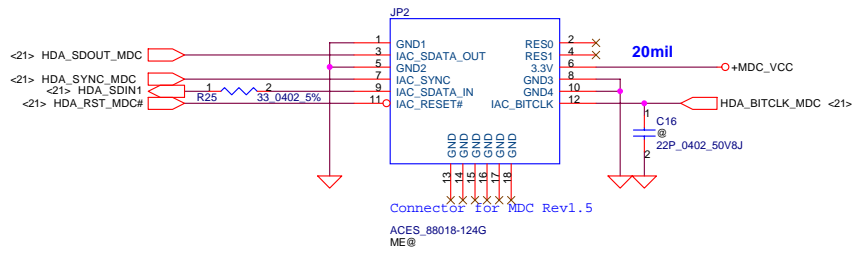
10/19 : Change P/N from SA472170000 to SA472170010



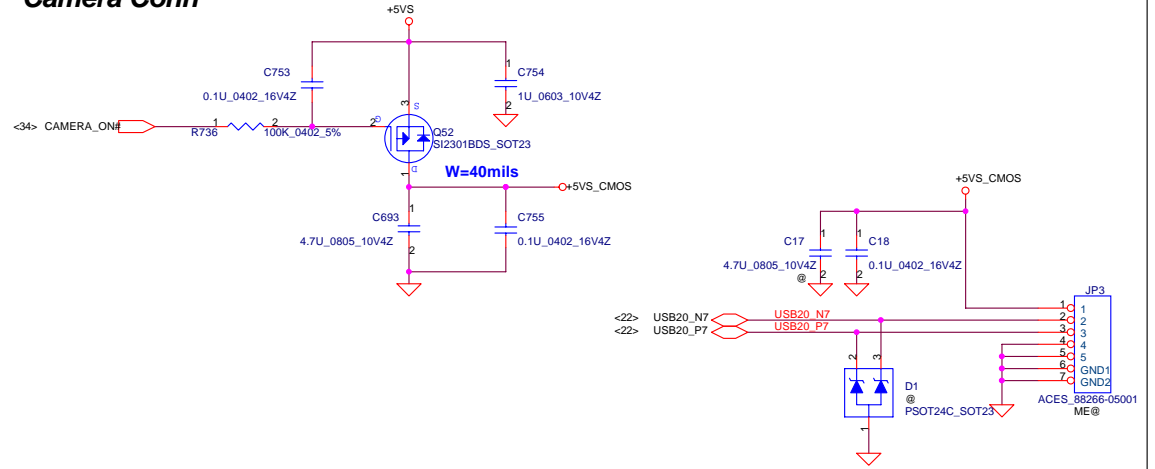
9/18 modify this page following IGT1x

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Size	Document Number	Rev		0.2	
Date: Wednesday, November 01, 2006				Sheet	41 of 52

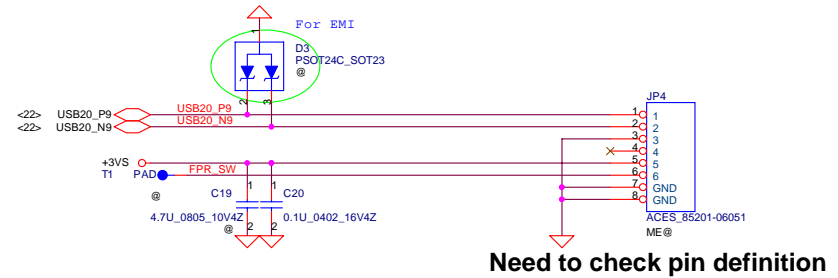
MDC Conn.



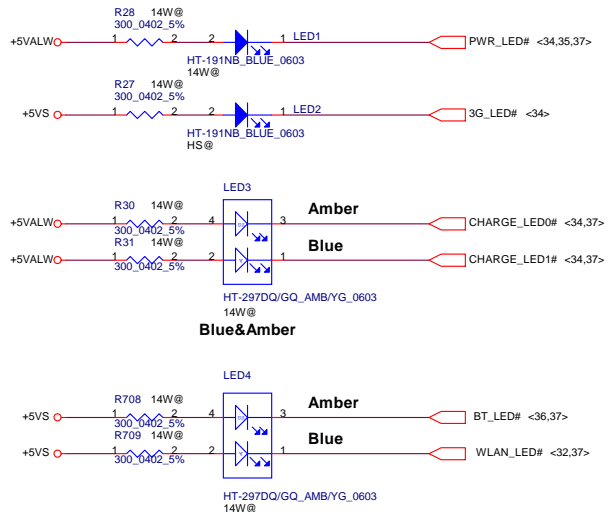
Camera Conn



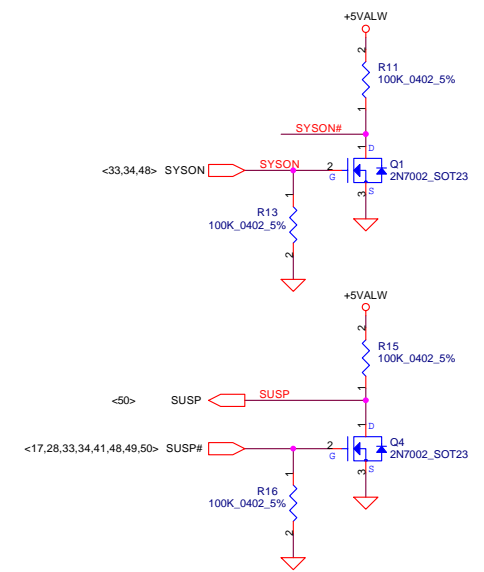
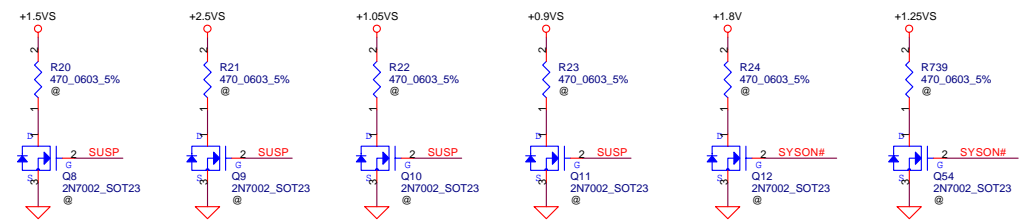
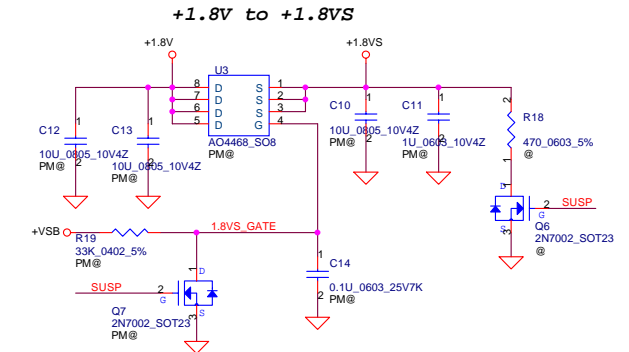
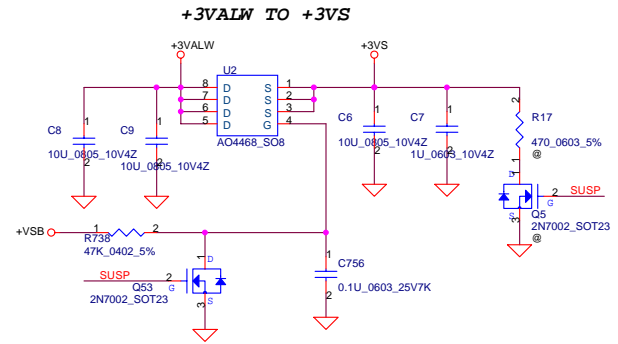
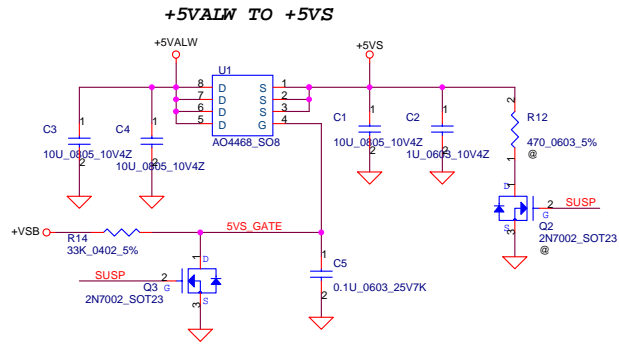
Finger Print board



LED



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Date:	Wednesday, November 01, 2006	Sheet	42	of	52	



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC Interface	
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				Date:	Wednesday, November 01, 2006
				Sheet	43 of 52

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