Compal Confidential

PAWGE Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M3L + GPU RobsonXT

2011-11-21

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Title: Cover Page

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B	LA8681P	1.0

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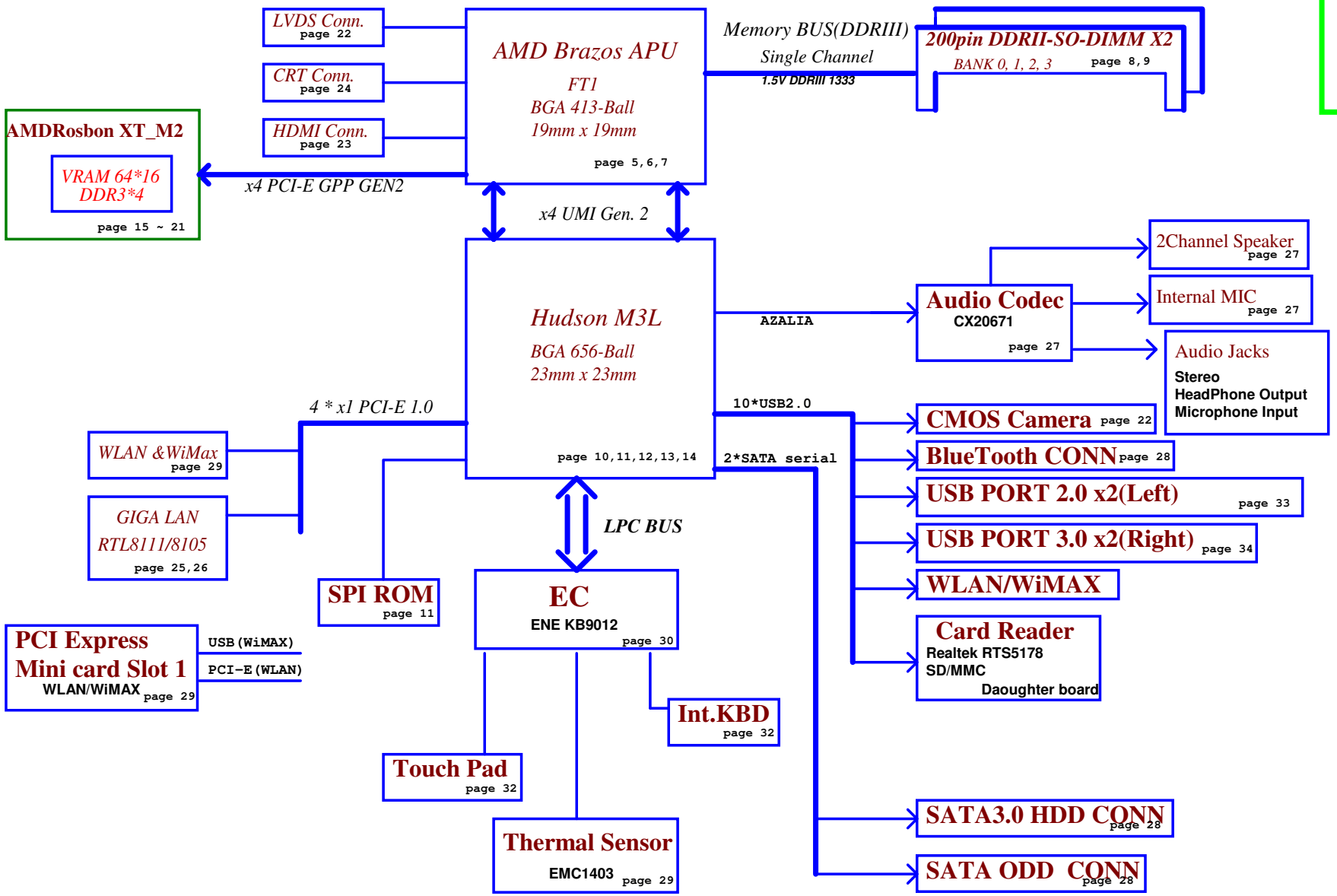
Compal confidential
File Name : PAWGE

QIWG5
LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B

QIWG6
LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B
LS7984P LED/B
LS7985P ODD/B



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
EMC1412-2 (dGPU)	1111-100xb	F8H
EMC1403-2(DDR,WLAN)	1001-101xb	9AH
SB-TSI	1001-100xb	98H

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M3L USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB
Port1	Right USB
Port2	Mini-PCIE
Port3	USB Camera
Port4	NC
Port5	CardReader
Port6	BT
Port7	NC
Port8	NC
Port9	NC
Port10	Left USB1
Port11	Left USB2
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M3L SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

```
UMA@   : UMA only
PX@    : DIS muxluss PX 4.0
Robson@ : Robson GPU
GIGA@ : RTL8111 1000
8105@ : RTL8105 10/100
DIMM@ : DIMM select
CMOS@ : USB camera
BT@    : BT function
ME@    : ME components
X76@, H1G@, H512@, S1G@, S512@  : VRAM
45@    : 45 Level
HDMI@    : HDMI function
 non HDMI@    : HDMI function

AN@    : Apple + Nokia ear phone combo
A@    : Apple ear phone
PCB@    : PCB PN
14@    : 14"
15@    : 15"
BBH@    : BBH
nonBBH@@    : nonBBH@
```

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Title: Notes List

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Power-Up/Down Sequence

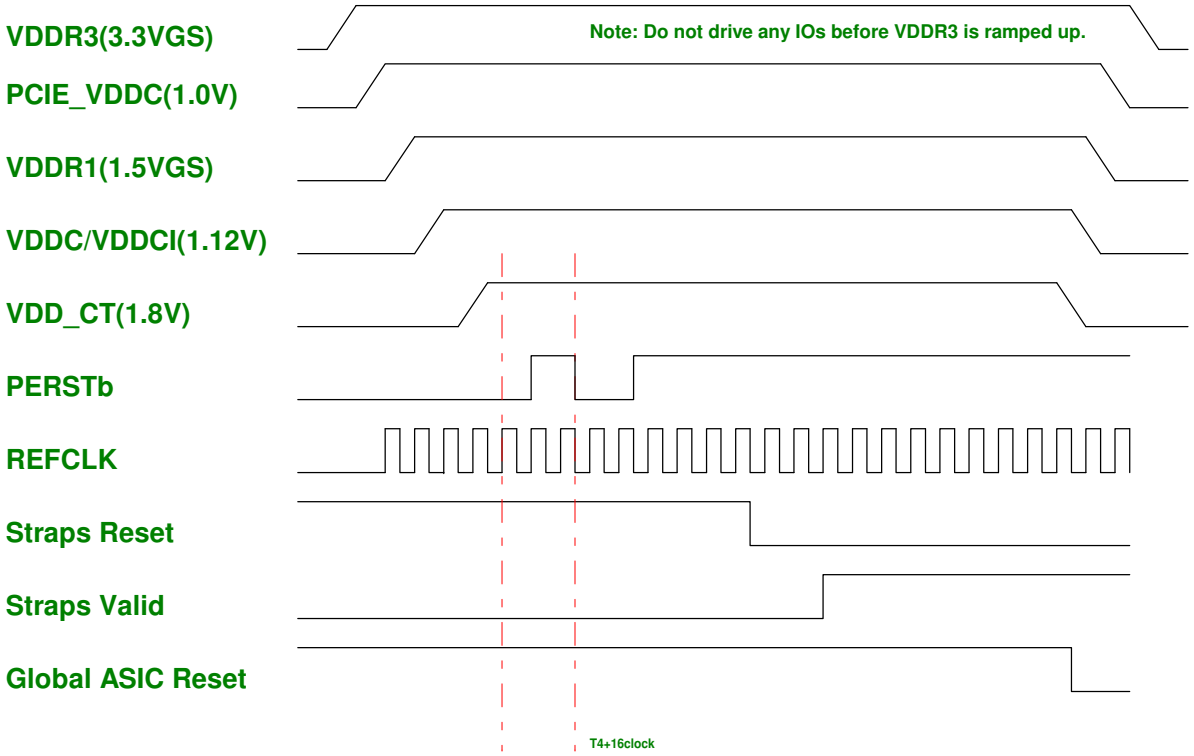
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



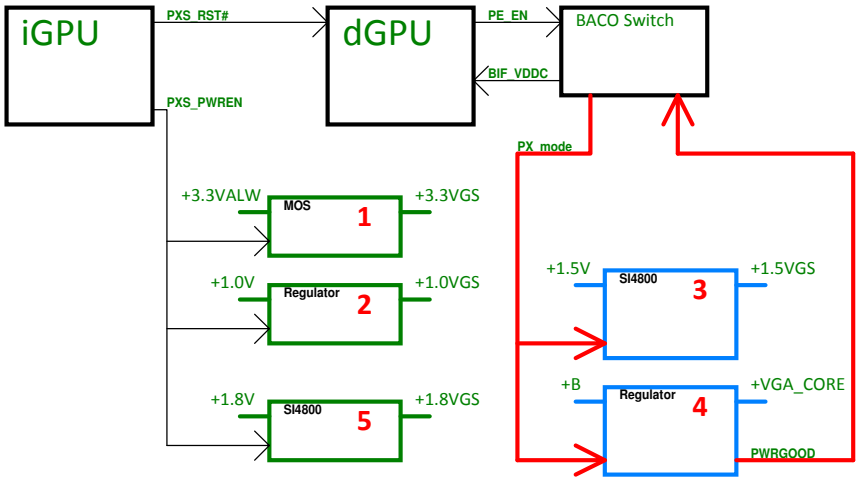
Without BACO option :

PXS_RST# : Low -> Reset dGPU ; High ->Normal operation
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PXS_RST# : High ->Normal operation (dGPU is not reset on BACO mode)
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

Size	Document Number	Rev
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AAAU6 PCB@
PCB 0R3 LA-8681P REV0 M/B

AAAU22 E1200@
EM1200GBB22GV

BBBU22 E1800@
EM1800GBB22GV

+1.8VS
R404 1 2 1K 0402 5% APU_DBREQ#
R399 1 2 1K 0402 5% APU_SVC
R400 1 2 1K 0402 5% APU_SVD
R405 2 1 300 0402 5% APU_RST#
R401 2 1 300 0402 5% APU_PWRGD
R402 1 2 510 0402 1% TEST_25_L
R403 1 2 1K 0402 5% TEST36

+3VS
R510 1 2 4.7K 0402 5% EDID_CLK
R511 1 2 4.7K 0402 5% EDID_DATA
R410 1 2 1K 0402 5% APU_PROCHOT#
R411 1 2 1K 0402 5% APU_ALERT#_R

U22B

DISPLAYPORT 1
<23> HDMI_TX2P C508 HDMI@ 0.1U 0402 16V7K HDMI_TX2P_C A8 TDP1_TXP0
<23> HDMI_TX2N C509 HDMI@ 0.1U 0402 16V7K HDMI_TX2N_C B8 TDP1_TXN0
<23> HDMI_TX1P C510 HDMI@ 0.1U 0402 16V7K HDMI_TX1P_C B9 TDP1_TXP1
<23> HDMI_TX1N C511 HDMI@ 0.1U 0402 16V7K HDMI_TX1N_C A9 TDP1_TXN1
<23> HDMI_TX0P C512 HDMI@ 0.1U 0402 16V7K HDMI_TX0P_C D10 TDP1_TXP2
<23> HDMI_TX0N C513 HDMI@ 0.1U 0402 16V7K HDMI_TX0N_C C10 TDP1_TXN2
<23> HDMI_CLKP C514 HDMI@ 0.1U 0402 16V7K HDMI_CLKP_C A10 TDP1_TXP3
<23> HDMI_CLKN C515 HDMI@ 0.1U 0402 16V7K HDMI_CLKN_C B10 TDP1_TXN3
TDP1_AUXP B2
TDP1_AUXN C2
TDP1_HPD C1

DP MISC
DP_ZVSS H3 DP_ZVSS R398 1 2 150 0402 1%
DP_BLON G2 APU_ENBKL <22>
DP_DIGON H2 APU_ENVDD <22>
DP_VARY_BL H1 APU_BLPWM <22>

HDMI_CLK <23>
HDMI_DATA <23>
HDMI_DET <23>

DISPLAYPORT 0
<22> LVDS_A2 B5 LTDP0_TXP0
<22> LVDS_A2# A5 LTDP0_TXN0
<22> LVDS_A1 D6 LTDP0_TXP1
<22> LVDS_A1# C6 LTDP0_TXN1
<22> LVDS_A0 A6 LTDP0_TXP2
<22> LVDS_A0# B6 LTDP0_TXN2
<22> LVDS_ACLK D8 LTDP0_TXP3
<22> LVDS_ACLK# C8 LTDP0_TXN3
LTDP0_AUXP A3 EDID_CLK
LTDP0_AUXN B3 EDID_DATA
LTDP0_HPD D3 LTDP0_HPD R406 1 2 100K 0402 5%

EDID_CLK <22>
EDID_DATA <22>

VGA DAC
DAC_RED C12
DAC_REDB D13 R407 1 2 150 0402 1% DAC_RED <24>
DAC_GREEN A12
DAC_GREENB B12 R408 1 2 150 0402 1% DAC_GRN <24>
DAC_BLUE A13
DAC_BLUEB B13 R409 1 2 150 0402 1% DAC_BLU <24>
DAC_HSYNC E1 CRT_HSYNC <24>
DAC_VSYNC E2 CRT_VSYNC <24>
DAC_SCL F2 CRT_DDC_CLK <24>
DAC_SDA D4 CRT_DDC_DATA <24>
DAC_ZVSS D12 DAC_ZVSS R413 1 2 499 0402 1%

CLK
<10> APU_CLK V2 CLKIN_H
<10> APU_CLK# V1 CLKIN_L
<10> APU_DISP_CLK D2 DISP_CLKIN_H
<10> APU_DISP_CLK# D1 DISP_CLKIN_L

SER
<44> APU_SVC J1 SVC
<44> APU_SVD J2 SVD
TO EC <16,29,30> EC_SMB_CK2 R809 1 2 0 0402 5% EC_SMB_CK2_R P3 SIC
<16,29,30> EC_SMB_DA2 R810 1 2 0 0402 5% EC_SMB_DA2_R P4 SID

CTRL
<10> APU_RST# T3 RESET_L
T4 PWROK
<10,44> APU_PWRGD
@C1022 1 2 100P 0402 50V8J
<10,30,37> H_PROCHOT# R808 1 2 0 0402 5% APU_PROCHOT# U1 PROCHOT_L
APU_THERMTRIP# U2 THERMTRIP_L
APU_ALERT#_R T2 ALERT_L

JTAG
APU_TDI N2 TDI
APU_TDO N1 TDO
APU_TCK P1 TCK
APU_TMS P2 TMS
APU_TRST# M4 TRST_L
APU_DBRDY M3 DBRDY
APU_DBREQ# M1 DBREQ_L

<44> APU_VDDNB_RUN_FB_H F4 VDDCR_NB_SENSE
<44> APU_VDD0_RUN_FB_H G1 VDDCR_CPU_SENSE
T77PAD F3 VDDIO_MEM_S_SENSE
<44> APU_VDD0_RUN_FB_L F1 VSS_SENSE
B4 RSVD_1
W11 RSVD_2
V5 RSVD_3

TEST
TEST4 R1 PAD T66
TEST5 R2 PAD T67
TEST6 R6
TEST14 T5 PAD T68
TEST15 E4 TEST15 R415 1 @ 2 1K 0402 5%
TEST16 K4 PAD T69
TEST17 L1 PAD T95
TEST18 L2 TEST18 R416 1 2 1K 0402 5%
TEST19 M2 TEST19 R417 1 2 1K 0402 5%
TEST25_H K1 TEST25_H R419 1 2 510 0402 1%
TEST25_L K2 TEST_25_L
TEST28_H L5 TEST28_H PAD T71
TEST28_L M5 TEST28_L PAD T72
TEST31 M21 TEST31 PAD T73
TEST33_H J18 TEST33_H C516 1 2 0.1U 0402 16V4Z R420 1 2 51 0402 1%
TEST33_L J19 TEST33_L C517 1 2 0.1U 0402 16V4Z R421 1 2 51 0402 1%
TEST34_H U15
TEST34_L T15
TEST35 H4 TEST35 R422 1 2 1K 0402 5%
TEST36 N5 TEST36
TEST37 R5 TEST37 PAD T76 R958 1 HDMI@ 2 1K 0402 5% +1.8VS
TEST38 K3
DMAACTIVE_L T1 ALLOW_STOP# <10>
R423 1 2 1K 0402 5% +1.8VS

AMD check list update 20101110
Delete Test point for layout limitation 20100818
non HDMI@
HDMI function enable R958 mount
disable R422 mount

S IC E SERIES EME450GBB22GVA 1.65G BGA

+3VS
R424 10K 0402 5%
R425 1K 0402 5%
Q79
APU_THERMTRIP# H_THERMTRIP# <12>
MMBT3904_NL_SOT23-3
R427 @ 0 0402 5%

If FCH internal pull-up disabled, level-shifter could be deleted.
Need BIOS to disable internal pull-up!!

AMD Debug
check the connect need or not

+1.8VS
R842 1K 0402 5%
APU_TRST# R846 0 0402 5% APU_TRST#_R
need to pop for HDT debug 20101012
R847 @ 10K 0402 5%
R848 @ 10K 0402 5%
R849 @ 10K 0402 5%

JHDT1
APU_TCK R843 1K 0402 5%
APU_TMS R844 1K 0402 5%
APU_TDI R845 1K 0402 5%
APU_TDO
APU_PWRGD
APU_RST#
APU_DBRDY
APU_DBREQ#
J108_PLLTST0 R851 @ 0 0402 5% TEST19
J108_PLLTST1 R852 @ 0 0402 5% TEST18
SAMTE_ASP-136446-07-B
@

Please be noted about TEST_18 and TEST_19
need to pop for HDT debug 20101012

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Title: FT1 CTRL/DP/CRT

Size	Document Number	Rev
Custom	LA8681P	1.0

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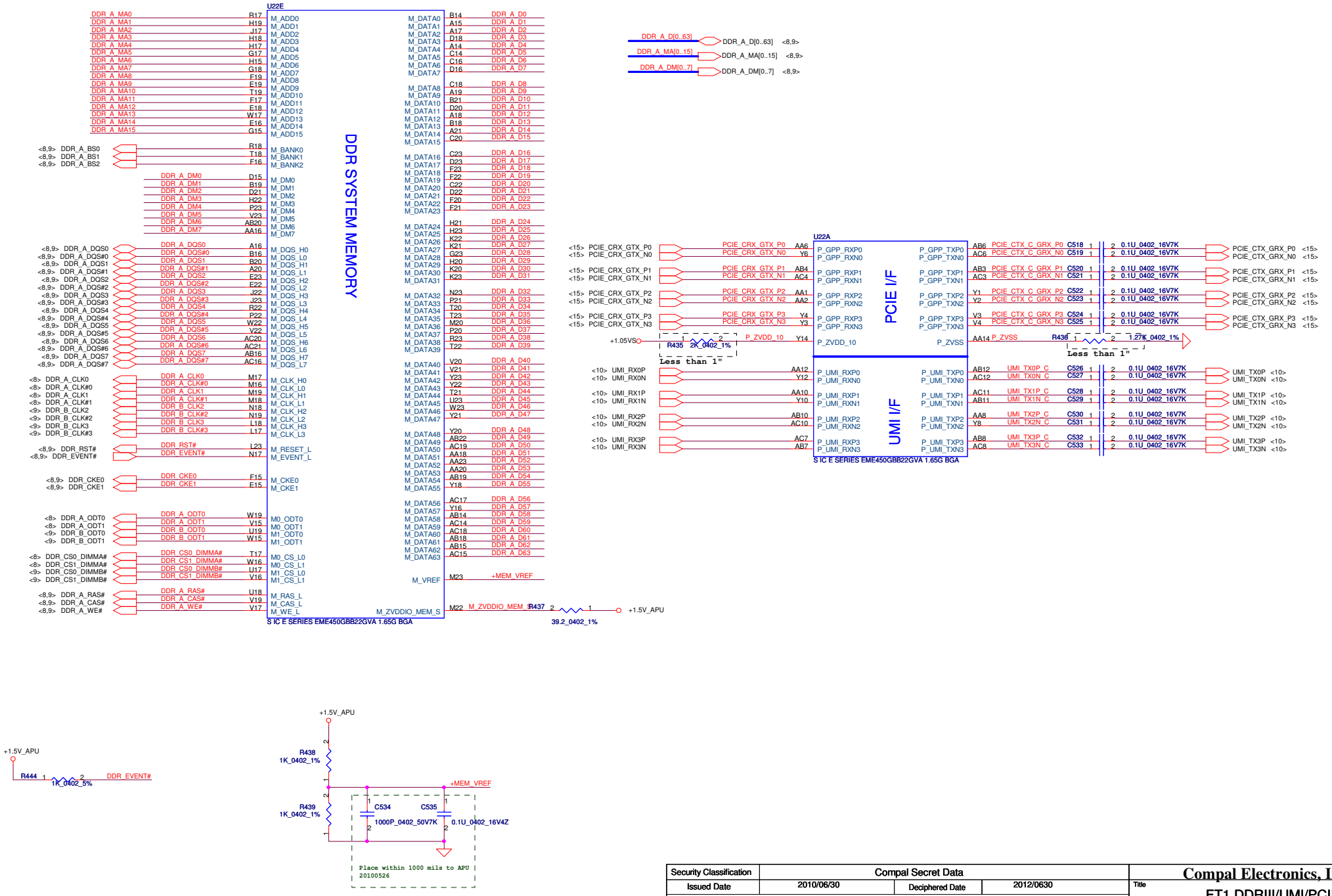

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: FT1 DDRIII/UMI/PCIE

Size	Document Number	Rev
Custom	LA8681P	1.0

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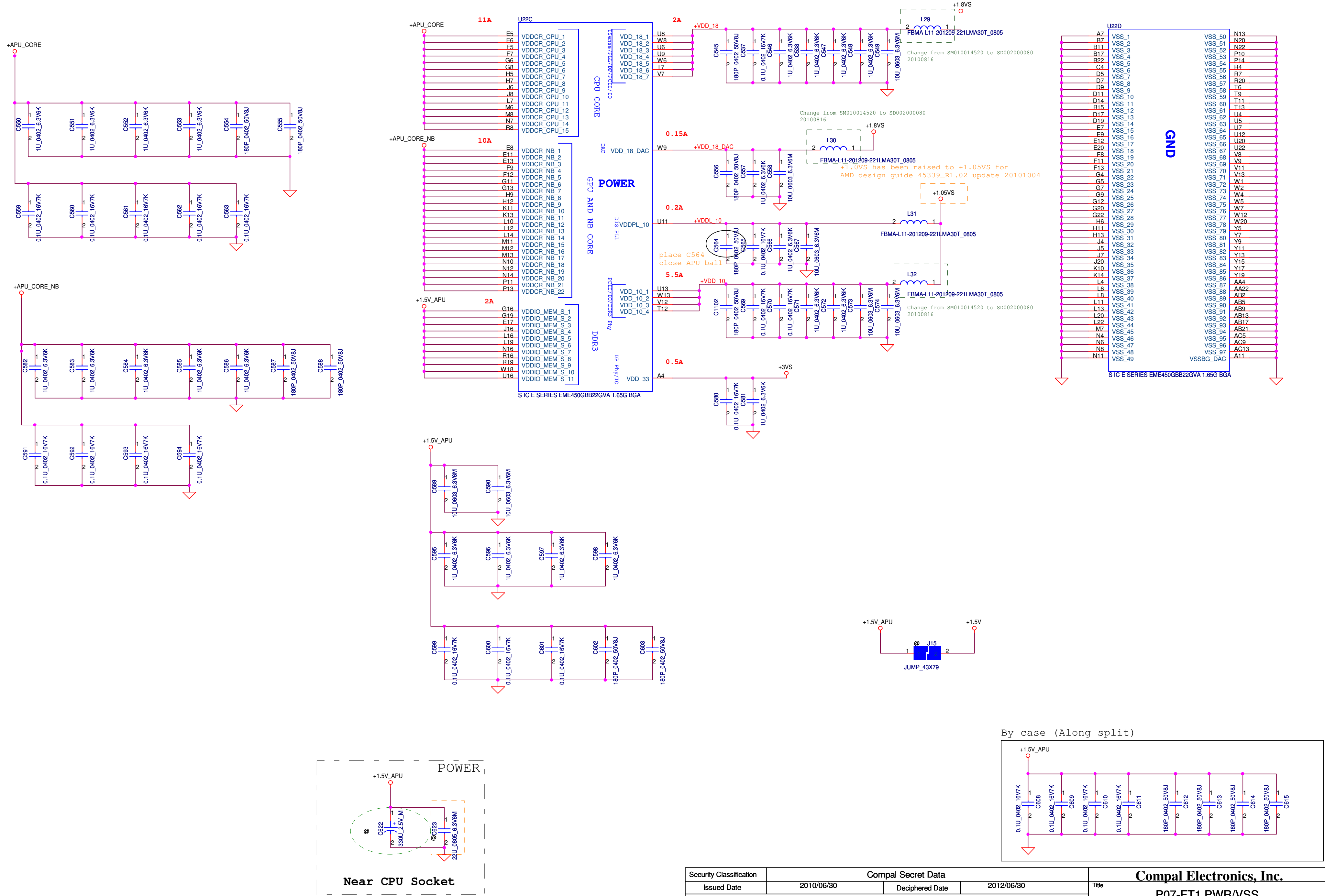

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Title	P07-FT1 PWR/VSS	
Size C	Document Number LA8681P	Rev 1.0
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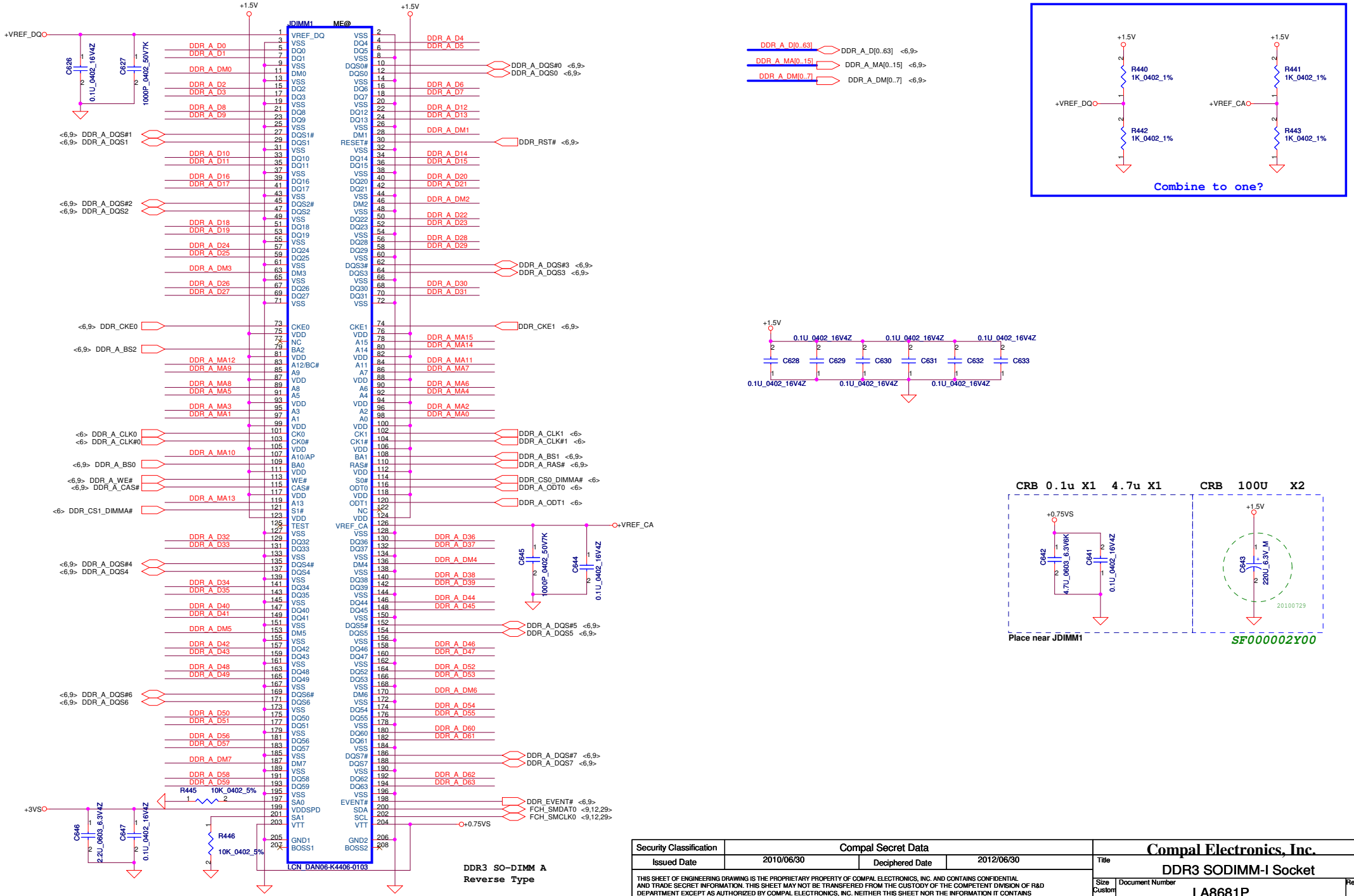

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: DDR3 SODIMM-I Socket

Size	Document Number	Rev
Custom	LA8681P	1.0

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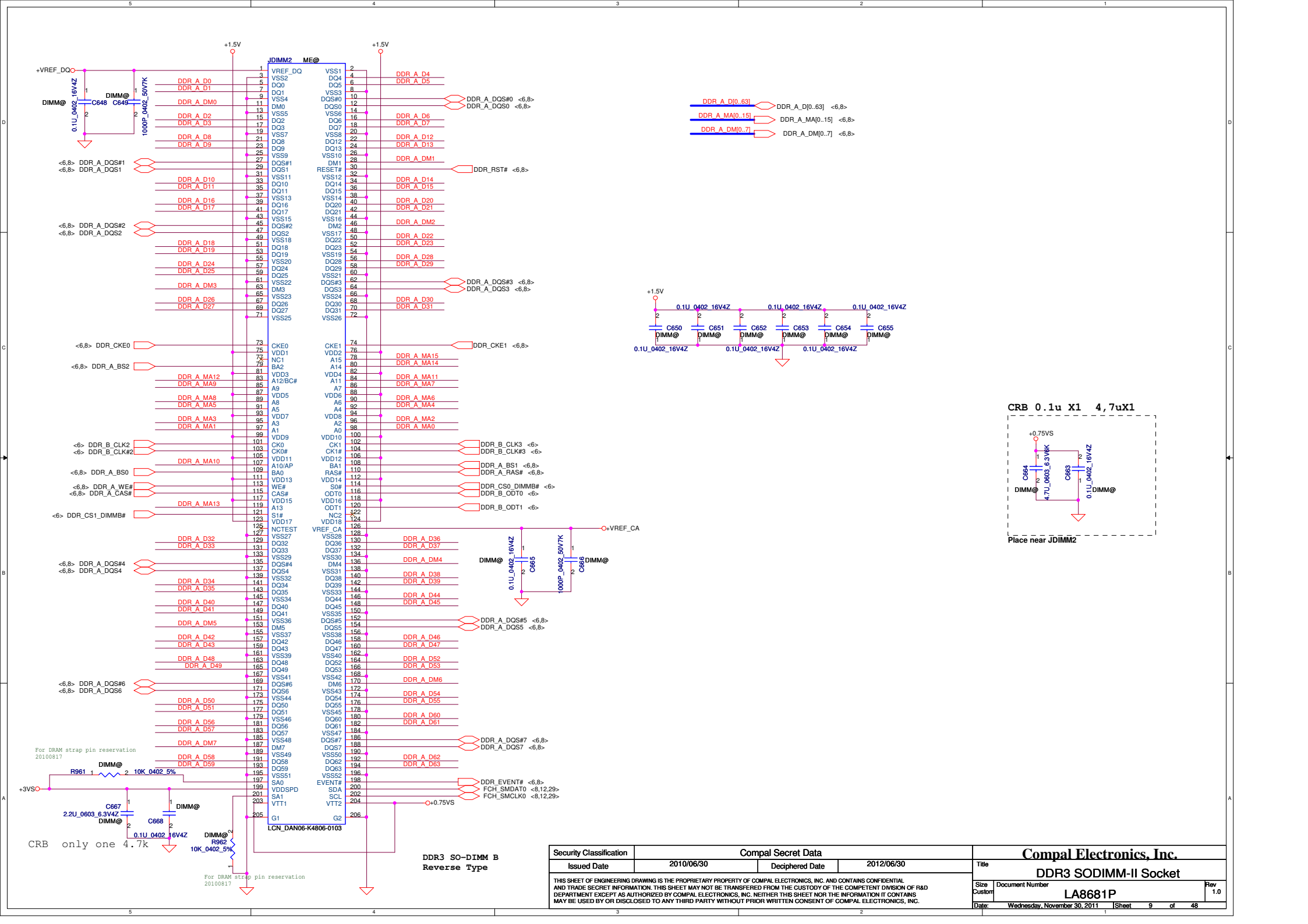

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Title: DDR3 SODIMM-II Socket

Size	Document Number	Rev
Custom	LA8681P	1.0

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C146 place close to FCH

C146 1 2 150P_0402_50V8J

U2A

HUDSON-2

PLT_RST# 1 R557 2 33_0402_5% APU_PCIE_RST#_C A_RST# AD5

PCIE_RST# AE2

<6> UMI_RX0P C147 2 0.1U_0402_16V7K UMI_RXP0_C AE30
<6> UMI_RX0N C148 2 0.1U_0402_16V7K UMI_RXN0_C AE32
<6> UMI_RX1P C149 2 0.1U_0402_16V7K UMI_RXP1_C AD33
<6> UMI_RX1N C150 2 0.1U_0402_16V7K UMI_RXN1_C AD31
<6> UMI_RX2P C151 2 0.1U_0402_16V7K UMI_RXP2_C AD28
<6> UMI_RX2N C152 2 0.1U_0402_16V7K UMI_RXN2_C AD29
<6> UMI_RX3P C153 2 0.1U_0402_16V7K UMI_RXP3_C AC30
<6> UMI_RX3N C154 2 0.1U_0402_16V7K UMI_RXN3_C AC32

UMI_TX0P
UMI_TX0N
UMI_TX1P
UMI_TX1N
UMI_TX2P
UMI_TX2N
UMI_TX3P
UMI_TX3N

<6> UMI_TX0P AB33
<6> UMI_TX0N AB31
<6> UMI_TX1P AB28
<6> UMI_TX1N AB29
<6> UMI_TX2P Y33
<6> UMI_TX2N Y31
<6> UMI_TX3P Y28
<6> UMI_TX3N Y29

UMI_RX0P
UMI_RX0N
UMI_RX1P
UMI_RX1N
UMI_RX2P
UMI_RX2N
UMI_RX3P
UMI_RX3N

+VDDAN_11_PCIE

R94 1 2 590_0402_1% PCIE_CALRP AE29
R88 1 2 2K_0402_1% PCIE_CALRN AF31

PCIE_CALRP
PCIE_CALRN

PCI EXPRESS INTERFACES

LAN
<25> PCIE_FTX_C_DRX_P0 C718 2 0.1U_0402_16V7K PCIE_FTX_DRX_P0 V33
<25> PCIE_FTX_C_DRX_N0 C720 2 0.1U_0402_16V7K PCIE_FTX_DRX_N0 V31
WLAN
<29> PCIE_FTX_C_DRX_P1 C721 2 0.1U_0402_16V7K PCIE_FTX_DRX_P1 W30
<29> PCIE_FTX_C_DRX_N1 C719 2 0.1U_0402_16V7K PCIE_FTX_DRX_N1 W32

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N

AB26
AB27
AA24
AA23

<25> PCIE_FRX_DTX_P0 AA27
<25> PCIE_FRX_DTX_N0 AA26
<29> PCIE_FRX_DTX_P1 W27
<29> PCIE_FRX_DTX_N1 V27

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N

V26
W26
W24
W23

+1.1VS_CKVDD

R95 1 2 2K_0402_1% CLK_CALRN F27

CLK_CALRN

G30 PCIE_RCLKP
G28 PCIE_RCLKN

<5> APU_DISP_CLK R26 DISP_CLKP
<5> APU_DISP_CLK# T26 DISP_CLKN

H33 DISP2_CLKP
H31 DISP2_CLKN

<5> APU_CLK T24 APU_CLKP
<5> APU_CLK# T23 APU_CLKN

VGA
<15> CLK_PCIE_VGA R98 1 2 0_0402_5% CLK_PCIE_VGA_R J30 SLT_GFX_CLKP
<15> CLK_PCIE_VGA# R99 1 2 0_0402_5% CLK_PCIE_VGA#_R K29 SLT_GFX_CLKN

H27 GPP_CLK0P
H28 GPP_CLK0N

J27 GPP_CLK1P
K26 GPP_CLK1N

WLAN
<29> CLK_PCIE_WLAN R102 1 2 0_0402_5% CLK_PCIE_WLAN_R F33 GPP_CLK2P
<29> CLK_PCIE_WLAN# R103 1 2 0_0402_5% CLK_PCIE_WLAN#_R F31 GPP_CLK2N

LAN
<25> CLK_PCIE_LAN R100 1 2 0_0402_5% CLK_PCIE_LAN_R E33 GPP_CLK3P
<25> CLK_PCIE_LAN# R101 1 2 0_0402_5% CLK_PCIE_LAN#_R E31 GPP_CLK3N

M23 GPP_CLK4P
M24 GPP_CLK4N

M27 GPP_CLK5P
M26 GPP_CLK5N

N25 GPP_CLK6P
N26 GPP_CLK6N

R23 GPP_CLK7P
R24 GPP_CLK7N

N27 GPP_CLK8P
R27 GPP_CLK8N

CLOCK GENERATOR

T101 @ R559 1 22_0402_5% 2 J26 14M_25M_48M_OSC

25M_X1 C31 25M_X1

25M_X2 C33 25M_X2

S IC 218-0755091 A13 HUDSON-M3L FCBGA 656P C38

PCI CLKS

PCICLK0 AF3
PCICLK1/GPO36 AF1 PCI_CLK1 <14>
PCICLK2/GPO37 AF5
PCICLK3/GPO38 AG2 PCI_CLK3 <14>
PCICLK4/14M_OSC/GPO39 AF6 PCI_CLK4 <14>

PCIRST# AB5

PCI INTERFACE

AD0/GPIO0 AJ3
AD1/GPIO1 AL5
AD2/GPIO2 AG4
AD3/GPIO3 AL6
AD4/GPIO4 AH3
AD5/GPIO5 AJ5
AD6/GPIO6 AL1
AD7/GPIO7 AN5
AD8/GPIO8 AN6
AD9/GPIO9 AJ1
AD10/GPIO10 AL8
AD11/GPIO11 AL3
AD12/GPIO12 AM7
AD13/GPIO13 AJ6
AD14/GPIO14 AK7
AD15/GPIO15 AN8
AD16/GPIO16 AG9
AD17/GPIO17 AM11
AD18/GPIO18 AJ10
AD19/GPIO19 AL12
AD20/GPIO20 AK11
AD21/GPIO21 AN12
AD22/GPIO22 AG12
AD23/GPIO23 AE12 PCI_AD23 <14>
AD24/GPIO24 AC12 PCI_AD24 <14>
AD25/GPIO25 AE13 PCI_AD25 <14>
AD26/GPIO26 AF13 PCI_AD26 <14>
AD27/GPIO27 AH13 PCI_AD27 <14>
AD28/GPIO28 AH14
AD29/GPIO29 AD15
AD30/GPIO30 AC15
AD31/GPIO31 AE16
CBE0# AE15
CBE1# AJ8
CBE2# AN10
CBE3# AD12
FRAME# AG10
DEVSEL# AK9
IRDY# AL10
TRDY# AF10
PAR AE10
STOP# AH1
PERR# AM9
SERR# AH8
REQ0# AG15
REQ1#/GPIO40 AG13
REQ2#/CLK_REQ8#/GPIO41 AF15
REQ3#/CLK_REQ5#/GPIO42 AM17 T14
GNT0# AD16
GNT1#/GPO44 AD13
GNT2#/SD_LED/GPO45 AD21
GNT3#/CLK_REQ7#/GPIO46 AK17 T99
CLKRUN# AD19
LOCK# AH9

INTE#/GPIO32 AF18
INTF#/GPIO33 AE18
INTG#/GPIO34 AC16
INTH#/GPIO35 AD18

Module design have reserve GPIO44,45 for VGA power enable and reset

LPC

LPCCLK0 B25 R558 1 22_0402_5% CLK_PCI_EC <14,30>
LPCCLK1 D25 @ R670 0_0402_5% CLK_PCI_DB <29>
LAD0 D27 LPC_CLK1 <14>
LAD1 C28 LPC_AD0 <29,30>
LAD2 A26 LPC_AD1 <29,30>
LAD3 A29 LPC_AD2 <29,30>
LFRAME# A31 LPC_AD3 <29,30>
LDRQ0# B27 LPC_FRAME# <29,30>
LDRQ1#/CLK_REQ6#/GPIO49 AE27
SERIRQ/GPIO48 AE19 SERIRQ <30>

APU

DMA_ACTIVE# G25
PROCHOT# E28 APU_PROCHOT#_R R15 1 @ 2 0_0402_5% ALLOW_STOP# <5>
APU_PG F26 H_PROCHOT# <5,30,37>
LDT_STP# G26 APU_PWRGD <5,44>
APU_RST# F25 APU_RST# <5>

S5 PLUS

S5_CORE_EN H7 T100
RTCCLK F1 RTC_CLK <14,30>
INTRUDER_ALERT# F3
VDDBT_RTC_G E6 W=20mils R105 1 2 510_0402_5% +RTCBATT
32K_X1 G2 32K_X1
32K_X2 G4 32K_X2

change to 510 Ohm

C156 1U_0402_6.3V6K

CLRP1 @ SHORT PADS

for Clear CMOS

APU_PCIE_RST#: Reset PCIE device on APU

+3VALW
C789 @ 0.1U_0402_16V4Z
MC74VHC1G08DFT2G SC70 5P
U43
APU_PCIE_RST# C
@R692 33_0402_5%
@ C790 150P_0402_50V8J
@ R693 8.2K_0402_5%
@R695 0_0402_5%
R866 0_0402_5%
APU_PCIE_RST# <15,29>
PLT_RST# <25,30>

R692/ C790 close to FCH

25M_X1
25M_X2
R106 1M_0402_5%
OSC NC NC OSC
Y4 25MHZ_20PF_FSX3M-25.M20FDO
C157 22P_0402_50V8J
C155 22P_0402_50V8J

C158 22P_0402_50V8J 32K_X1
R107 20M_0402_5% Y1 32.768KHZ_12.5PF_CM31532768DZFT
C159 22P_0402_50V8J 32K_X2

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

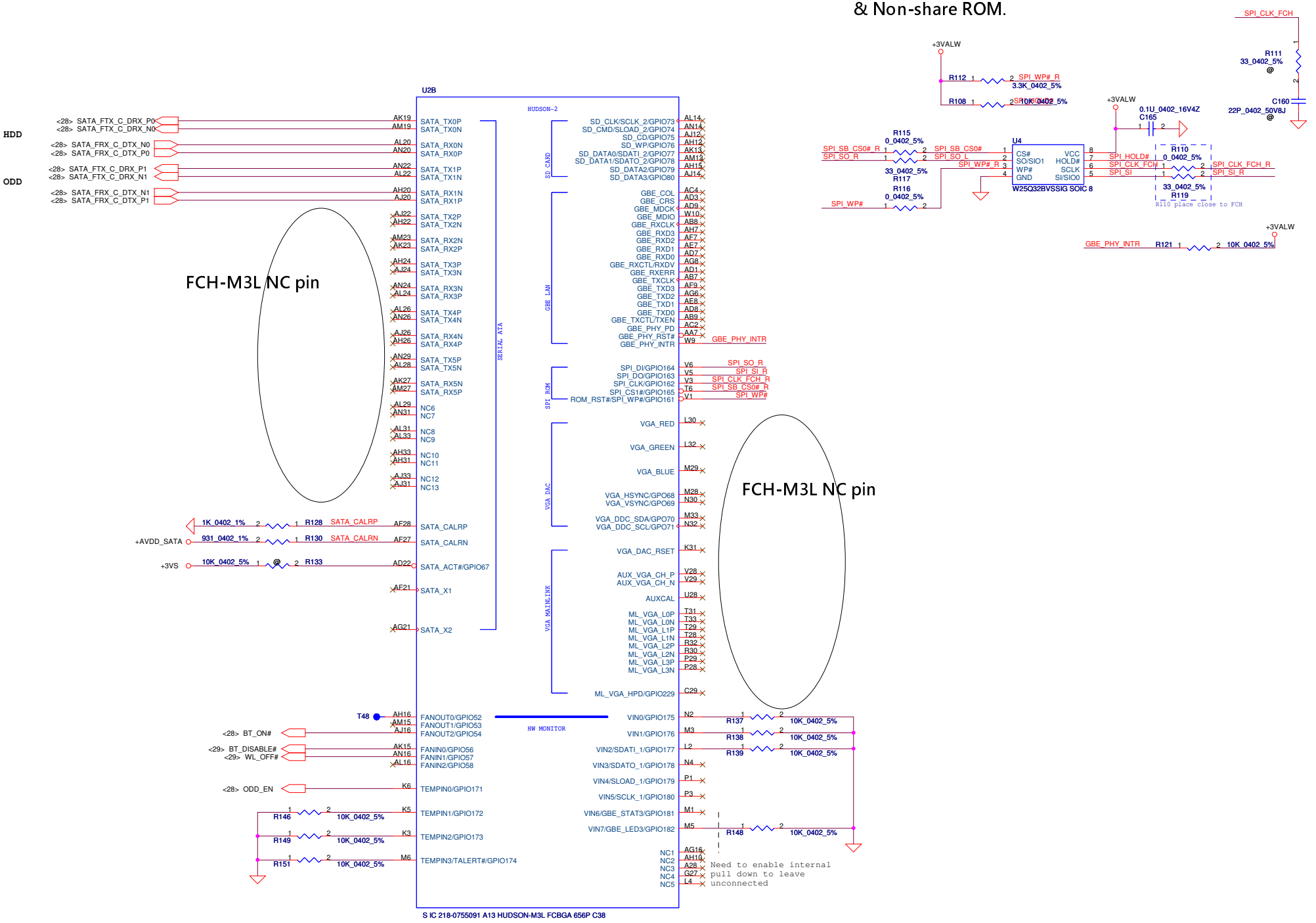
Compal Electronics, Inc.

Title: FCH PCIE/CLK/PCI/LPC/RTC

Size	Document Number	Rev
Custom	LA8681P	0.1

Date: Wednesday, November 30, 2011 Sheet 10 of 48

4MB SPI ROM
& Non-share ROM.



S IC 218-0755091 A13 HUDSON-M3L FCBGA 656P C38

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FCH SATA/SPI/VGA/HWM/SD

Size	Document Number	Rev
Custom	LA8681P	0.1

Date: Wednesday, November 30, 2011 | Sheet 11 of 48

PCIE_RST2 : Reset PCIE device on Hudson 3

U2D

HUDSON-2

T17 → PCIE_RST2#/PCI_PME#/GEVENT4#

<30> EC_LID_OUT# → RI#/GEVENT22#

SPI_CS3#/GBE_STAT1/GEVENT21#

<30> PM_SLP_S3# → SLP_S3#

<30> PM_SLP_S5# → SLP_S5#

<30> PBTN_OUT# → PWR_BTN#

<30,44> FCH_PWRGD → PWR_GOOD

TEST0 → TEST0

TEST1 → TEST1/TMS

TEST2 → TEST2

<30> GATEA20 → GA20IN/GEVENT0#

<30> KBRST# → KBRST#/GEVENT1#

<30> EC_SCI# → LPC_PME#/GEVENT3#

<30> EC_SMI# → LPC_SMI#/GEVENT23#

+3VALW — R155 1 @ 2 10K 0402 5% — SYS_RESET# → LPC_PD#/GEVENT5#

<25,29> FCH_PCIE_WAKE# → SYS_RESET#/GEVENT19#

WAKE#/GEVENT8#

<5> H_THERMTRIP# → IR_RX1/GEVENT20#

WD_PWRGD → THRMTRIP#/SMBALERT#/GEVENT2#

WD_PWRGD

<30> EC_RSMRST# → RSMRST#

<25> LAN_CLKREQ# → CLK_REQ4#/SATA_IS0#/GPIO64

CLK_REQ3#/SATA_IS1#/GPIO63

SMARTVOLT1/SATA_IS2#/GPIO50

CLK_REQ0#/SATA_IS3#/GPIO60

SATA_IS4#/FANOUT3/GPIO55

SATA_IS5#/FANIN3/GPIO59

<27> FCH_SPKR → SPKR/GPIO66

<8,9,29> FCH_SMCLK0 → FCH_SMCLK0 → SCL0/GPIO43

<8,9,29> FCH_SMDAT0 → FCH_SMDAT0 → SDA0/GPIO47

FCH_SMCLK1 → SCL1/GPIO227

FCH_SMDATA1 → SDA1/GPIO228

<29> WLAN_CLKREQ# → CLK_REQ2#/FANIN4/GPIO62

CLK_REQ1#/FANOUT4/GPIO61

IR_LED#/LLB#/GPIO184

<15,17,43> VGA_PWRGD → SMARTVOLT2/SHUTDOWN#/GPIO51

DDR3_RST#/GEVENT7#/VGA_PD

GBE_LED0/GPIO183

SPI_HOLD#/GBE_LED1/GEVENT9#

GBE_LED2/GEVENT10#

GBE_STAT0/GEVENT11#

<16> PEG_CLKREQ# — R156 2 @ 1 0 0402 5% — PEG_CLKREQ#_R → CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#

USB_OC7# → BLINK/USB_OC7#/GEVENT18#

<28> ODD_DA#_FCH → USB_OC5# → USB_OC6#/IR_TX1/GEVENT6#

<28> ODD_DETECT# → USB_OC3# → USB_OC5#/IR_TX0/GEVENT17#

USB_OC2# → USB_OC4#/IR_RX0/GEVENT16#

<32> USB_OC2# → USB_OC1# → USB_OC3#/AC_PRES/TDO/GEVENT15#

<33> USB_OC1# → USB_OC2#/TCK/GEVENT14#

<34> USB_OC0# → USB_OC1#/TDI/GEVENT13#

USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#

<27> HDA_BITCLK_AUDIO — R159 1 2 33 0402 5% — HDA_BITCLK → AZ_BITCLK

<27> HDA_SDOUT_AUDIO — R160 1 2 33 0402 5% — HDA_SDOUT → AZ_SDOUT

<27> HDA_SDIN0 → HDA_SDIN0 → AZ_SDIN0/GPIO167

AZ_SDIN1/GPIO168

AZ_SDIN2/GPIO169

AZ_SDIN3/GPIO170

<27> HDA_SYNC_AUDIO — R161 1 2 33 0402 5% — HDA_SYNC → AZ_SYNC

<27> HDA_RST_AUDIO# — R162 1 2 33 0402 5% — HDA_RST# → AZ_RST#

T61 → PS2_DAT/SDA4/GPIO187

T19 → PS2_CLK/CEC/SCL4/GPIO188

SPI_CS2#/GBE_STAT2/GPIO166

GPIO189 → PS2KB_DAT/GPIO189

GPIO190 → PS2KB_CLK/GPIO190

<15> PXS_RST# — 0 0402 5% 2 PX@ 1 R96 → PS2M_DAT/GPIO191

<17,43> PXS_PWREN — 0 0402 5% 2 PX@ 1 R97 → PS2M_CLK/GPIO192

<30> VGA_GATE# → Q112 PX@ 2N7002K_SOT23-3

KSO_0/GPIO209

KSO_1/GPIO210

KSO_2/GPIO211

KSO_3/GPIO212

KSO_4/GPIO213

KSO_5/GPIO214

KSO_6/GPIO215

KSO_7/GPIO216

KSO_8/GPIO217

KSO_9/GPIO218

KSO_10/GPIO219

KSO_11/GPIO220

KSO_12/GPIO221

KSO_13/GPIO222

KSO_14/GPIO223

KSO_15/GPIO224

KSO_16/GPIO225

KSO_17/GPIO226

S IC 218-0755091 A13 HUDSON-M3L FCBGA 656P C38

USB MISC

USB 1.1

ACPI / WAKE UP EVENTS

GPIO

USB 2.0

USB OC

HD AUDIO

USB 3.0

EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC

USB_RCOMP — R154 1 2 11.8K 0402 1%

USB_FSD1P/GPIO186

USB_FSD1N

USB_FSD0P/GPIO185

USB_FSD0N

USB_HSD13P — USB30_P11 <34>

USB_HSD13N — USB30_N11 <34>

USB_HSD12P

USB_HSD12N

USB_HSD11P — USB30_P10 <34>

USB_HSD11N — USB30_N10 <34>

USB_HSD10P

USB_HSD10N

USB_HSD9P

USB_HSD9N

USB_HSD8P — USB20_P6 <28>

USB_HSD8N — USB20_N6 <28>

USB_HSD7P — USB20_P5 <32>

USB_HSD7N — USB20_N5 <32>

USB_HSD6P

USB_HSD6N

USB_HSD5P — USB20_P3 <22>

USB_HSD5N — USB20_N3 <22>

USB_HSD4P — USB20_P2 <29>

USB_HSD4N — USB20_N2 <29>

USB_HSD3P — USB20_P1 <32>

USB_HSD3N — USB20_N1 <32>

USB_HSD2P — USB20_P0 <33>

USB_HSD2N — USB20_N0 <33>

USB_HSD1P

USB_HSD1N

USB_HSD0P

USB_HSD0N

USBSS_CALRP — USBSS_CALRP — R864 1 2 1K 0402 1%

USBSS_CALRN — USBSS_CALRN — R865 1 2 1K 0402 1% → +FCH_VDD_11_SSUSB_S

USB_SS_TX3P

USB_SS_TX3N

USB_SS_RX3P

USB_SS_RX3N

USB_SS_TX2P

USB_SS_TX2N

USB_SS_RX2P

USB_SS_RX2N

USB_SS_TX1P — USB30_FTX_DRX_P1 — USB30_FTX_DRX_P1 <34>

USB_SS_TX1N — USB30_FTX_DRX_N1 — USB30_FTX_DRX_N1 <34>

USB_SS_RX1P — USB30_FRX_DTX_P1 — USB30_FRX_DTX_P1 <34>

USB_SS_RX1N — USB30_FRX_DTX_N1 — USB30_FRX_DTX_N1 <34>

USB_SS_TX0P — USB30_FTX_DRX_P0 — USB30_FTX_DRX_P0 <34>

USB_SS_TX0N — USB30_FTX_DRX_N0 — USB30_FTX_DRX_N0 <34>

USB_SS_RX0P — USB30_FRX_DTX_P0 — USB30_FRX_DTX_P0 <34>

USB_SS_RX0N — USB30_FRX_DTX_N0 — USB30_FRX_DTX_N0 <34>

SCL2/GPIO193 — R165 1 2 10K 0402 5%

SDA2/GPIO194 — R167 1 2 10K 0402 5%

SCL3_LV/GPIO195 — R227 1 2 10K 0402 5%

SDA3_LV/GPIO196 — R228 1 2 10K 0402 5%

EC_PWM0/EC_TIMER0/GPIO197

EC_PWM1/EC_TIMER1/GPIO198

EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 — EC_PWM2 — EC_PWM2 <14>

EC_PWM3/EC_TIMER3/GPIO200

KSI_0/GPIO201

KSI_1/GPIO202

KSI_2/GPIO203

KSI_3/GPIO204

KSI_4/GPIO205

KSI_5/GPIO206

KSI_6/GPIO207

KSI_7/GPIO208

FCH-M3L NC pin

FCH-M3L NC pin

FCH-M3L NC pin

FCH-M3L NC pin

LP2 Root

LP1

BT Root

CR

CMOS Root

WLAN

RP2

RP1

LP2

LP1

strap pin

For FCH internal debug use

+3VALW

R179 1 @ 2 2.2K 0402 5% TEST0

R181 1 @ 2 2.2K 0402 5% TEST1

R183 1 @ 2 2.2K 0402 5% TEST2

+3VALW

R883 1 @ 2 10K 0402 5% USB_OC7#

R624 1 2 10K 0402 5% USB_OC2#

R625 1 2 10K 0402 5% USB_OC1#

R174 1 2 10K 0402 5% USB_OC0#

R618 1 @ 2 10K 0402 5% ODD_DA#_FCH

R649 1 @ 2 10K 0402 5% ODD_DETECT#

R620 1 @ 2 10K 0402 5% USB_OC5#

R163 1 @ 2 10K 0402 5% USB_OC3#

R164 1 @ 2 10K 0402 5% H_THERMTRIP#

R169 1 @ 2 100K 0402 5% EC_LID_OUT#

R170 1 @ 2 10K 0402 5% FCH_PCIE_WAKE#

+3VS

R171 1 2 2.2K 0402 5% FCH_SMCLK0

R172 1 2 2.2K 0402 5% FCH_SMDAT0

R175 1 2 10K 0402 5% WD_PWRGD

R173 1 2 8.2K 0402 5% WLAN_CLKREQ#

R176 1 2 8.2K 0402 5% LAN_CLKREQ#

+3VALW +3VALW

R685 1 UMA@ 2 10K 0402 5%

R684 1 UMA@ 2 10K 0402 5%

R166 1 2 10K 0402 5% FCH_SMCLK1

R168 1 2 10K 0402 5% FCH_SMDATA1

R177 1 2 2.2K 0402 5% EC_RSMRST#

R178 1 @ 2 10K 0402 5% HDA_BITCLK

R180 1 @ 2 10K 0402 5% HDA_SDIN0

R182 1 PX@ 2 10K 0402 5% PEG_CLKREQ#_R

GPIO189

GPIO190

R682 1 PX@ 2 10K 0402 5%

R683 1 PX@ 2 10K 0402 5%

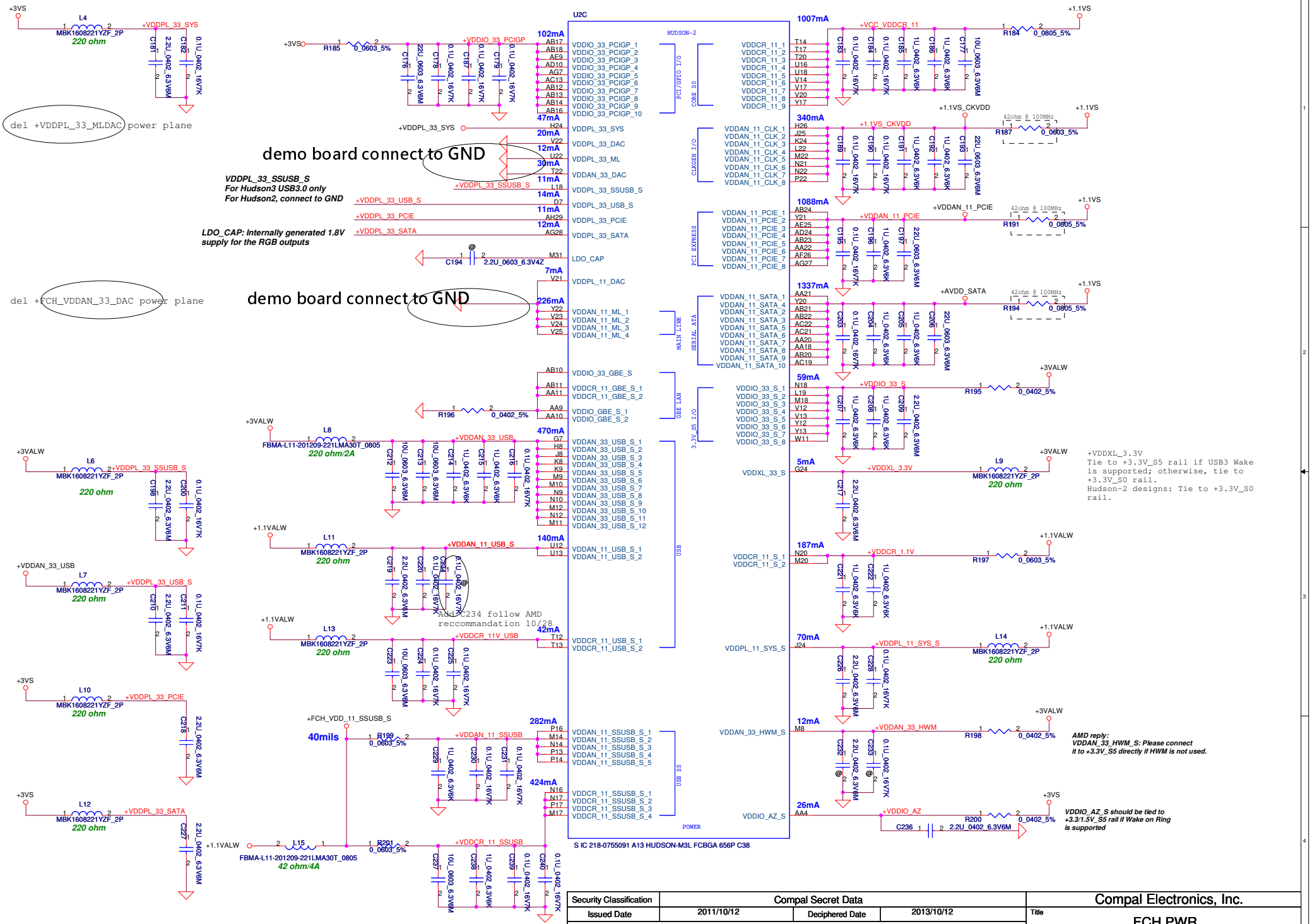
BOARD Config.	GPIO189	GPIO190	Function
	0	0	PX4 Full
	0	1	PX4 low
	1	0	UMA Low
	1	1	UMA Full

Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size: Custom — Document Number: LA8681P — Rev: 0.1

Date: Wednesday, November 30, 2011 — Sheet 12 of 48



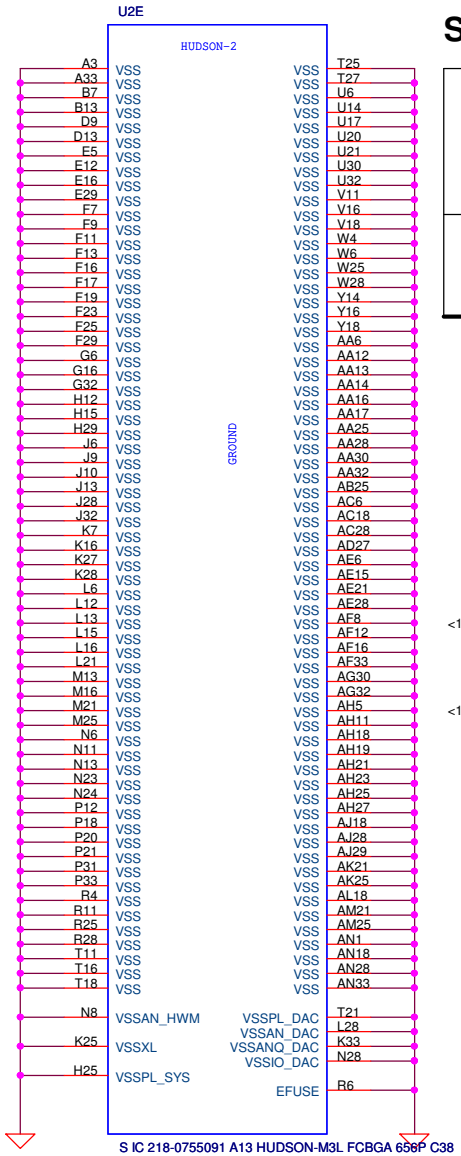
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: LA8681P | Rev: 0.1

Date: Tuesday, November 29, 2011 | Sheet 13 of 48



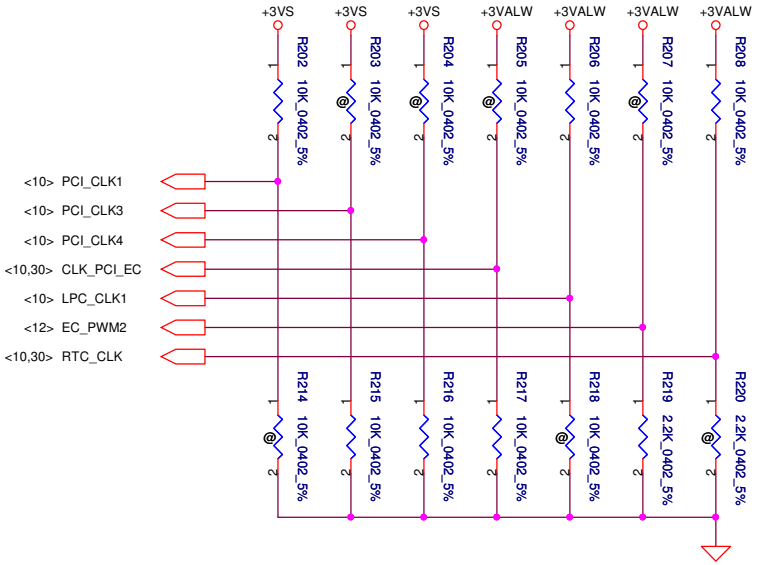
STRAP PINS

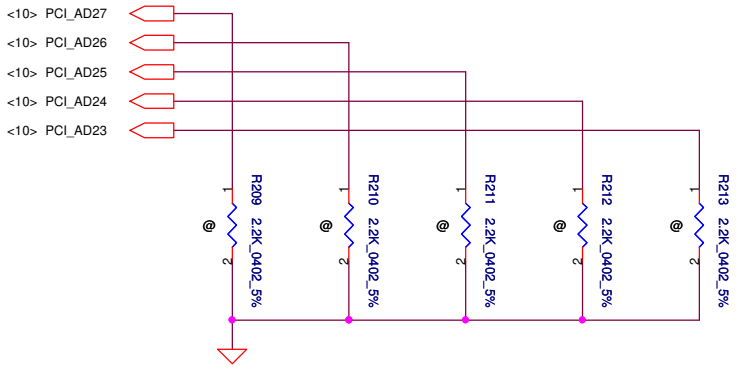
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





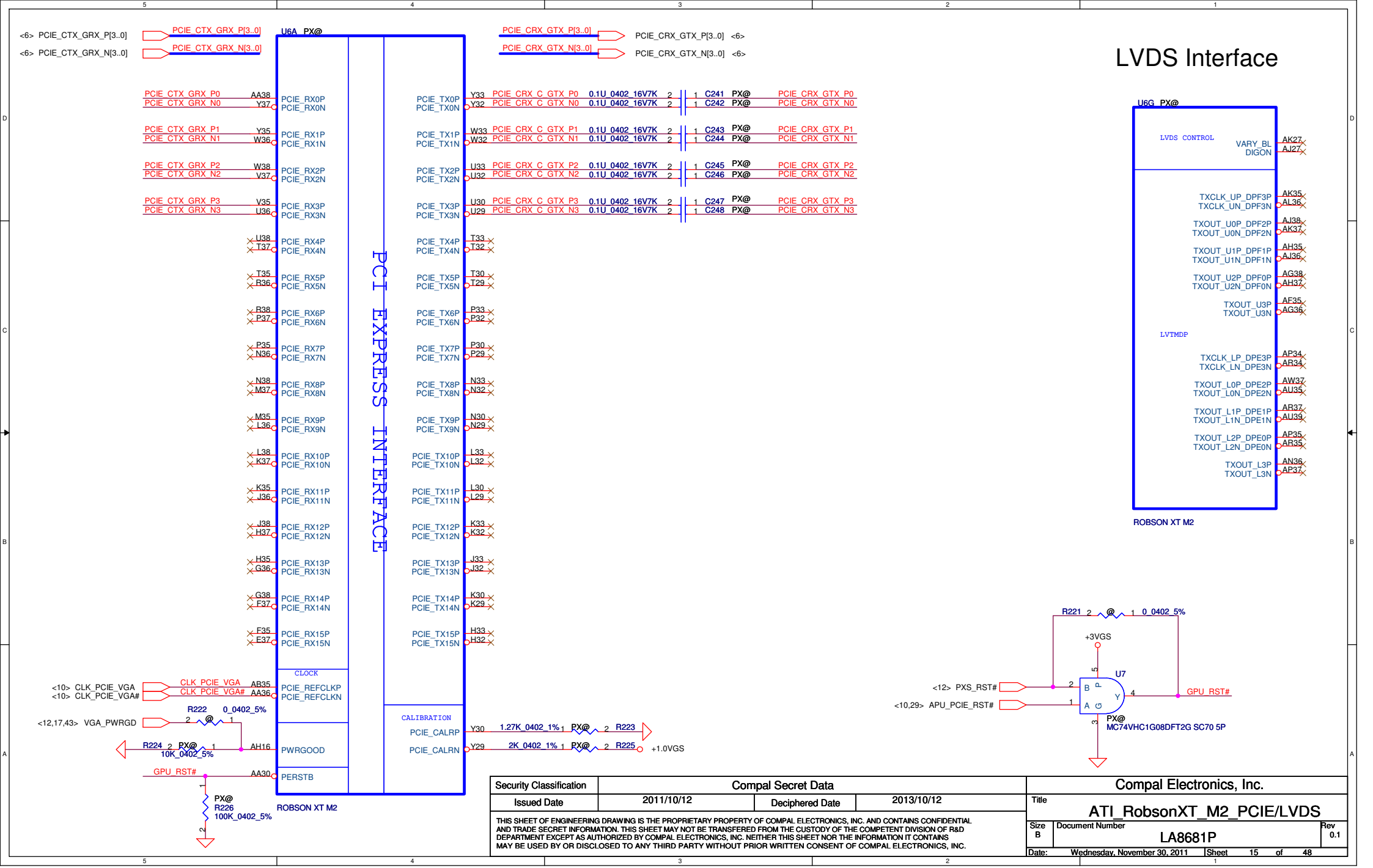
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size	Document Number	Rev
B	LA8681P	0.1

Date: Wednesday, November 30, 2011 Sheet 14 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_PCIE/LVDS

Size	Document Number	Rev
B	LA8681P	0.1

Date: Wednesday, November 30, 2011 Sheet 15 of 48

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

STRAPS

Internal VGA Thermal Sensor

0.60 V level, Please VREFG Divider ans cap close to ASIC

XTALIN Voltage Swing: 1.8 V

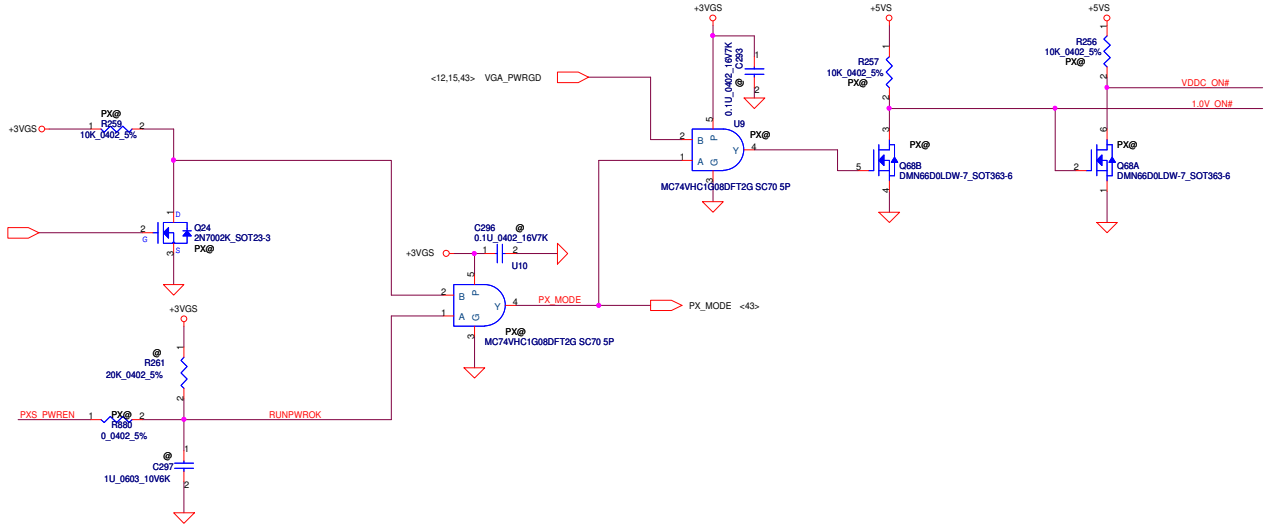
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

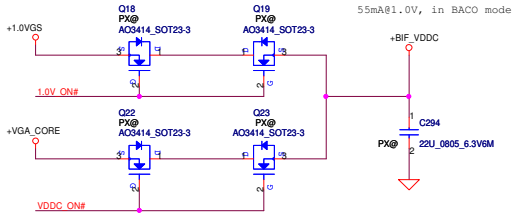
Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_Main_MSIC

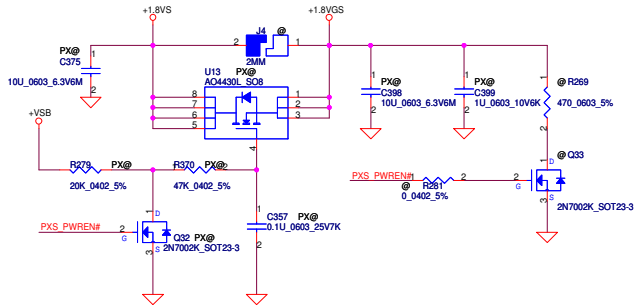
Size	Document Number	Rev
C	LA8681P	0.1

Date: Wednesday, November 30, 2011 Sheet 16 of 48

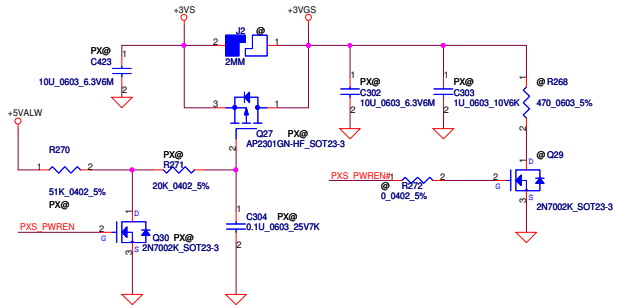


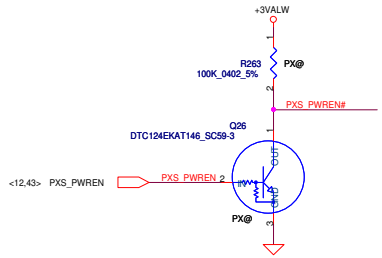


+1.8VS TO +1.8VGS

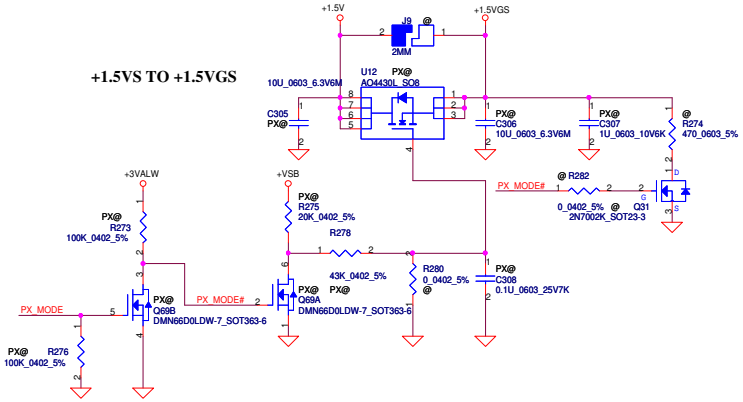


+3.3VS TO +3.3VGS

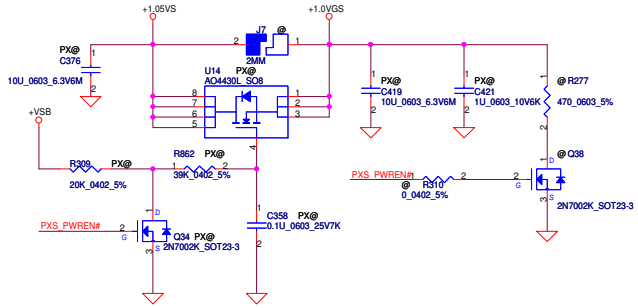




+1.5VS TO +1.5VGS



+1.05VS TO +1.0VGS



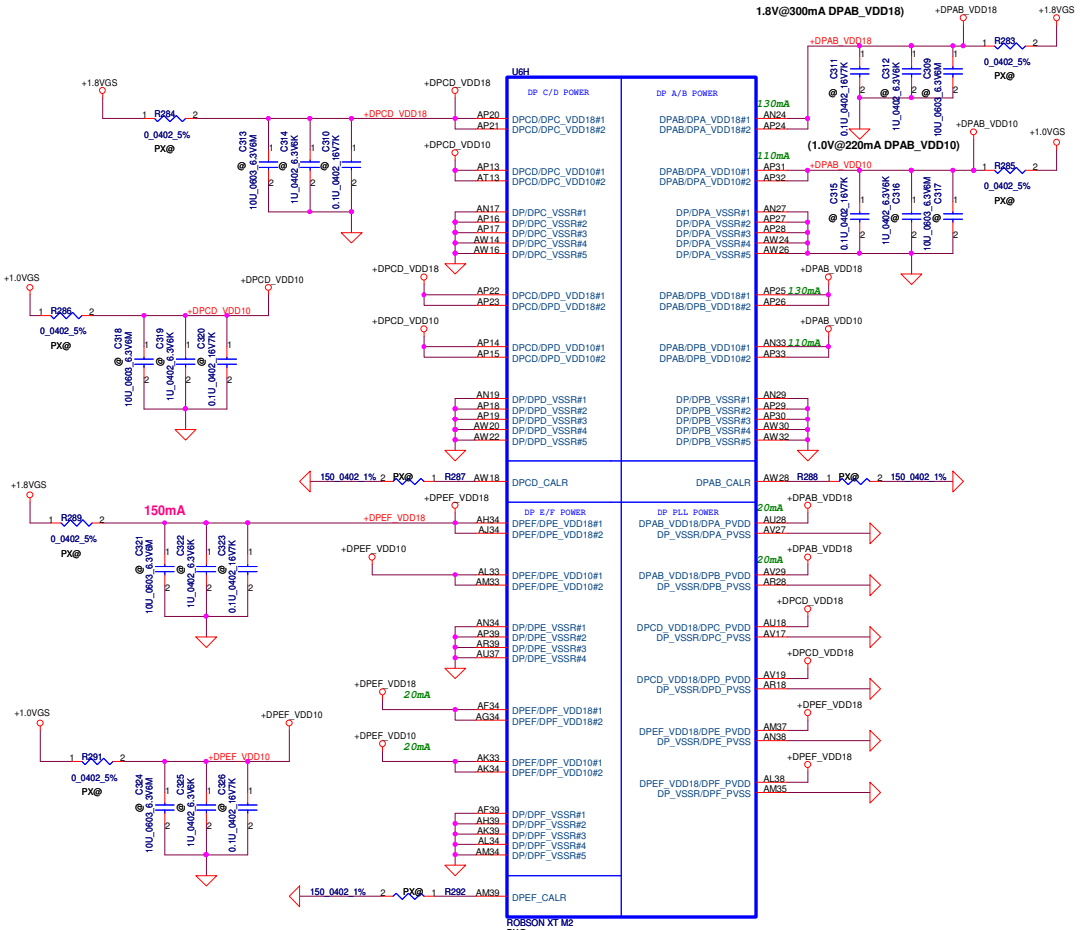
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

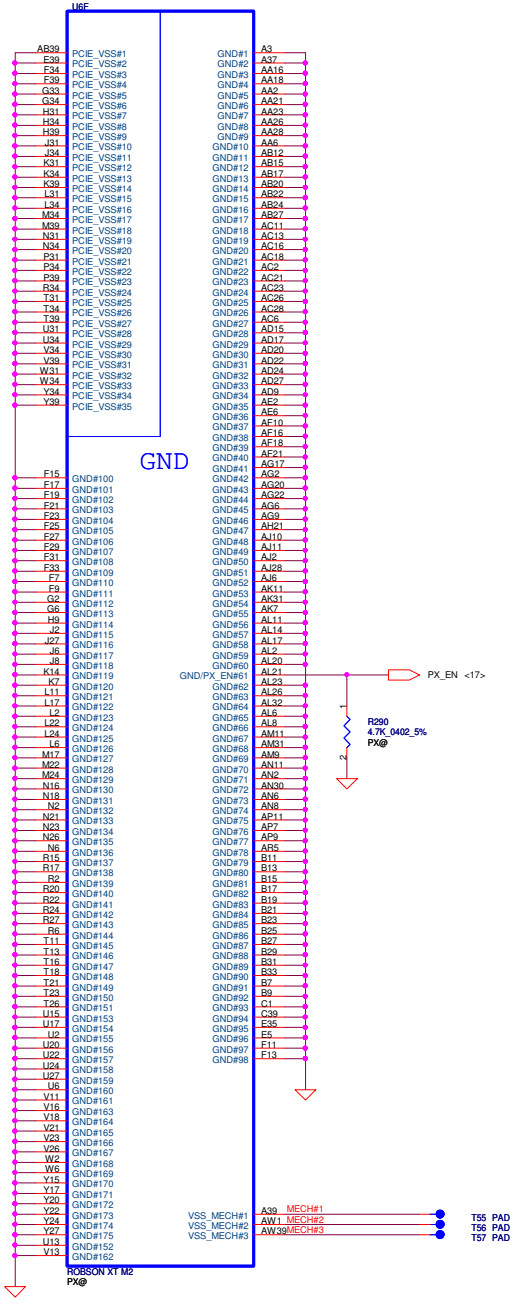
Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_BACO POWER

Size	Document Number	Rev
C	LA8681P	0.1

Date: Wednesday, November 30, 2011 | Sheet 17 of 48





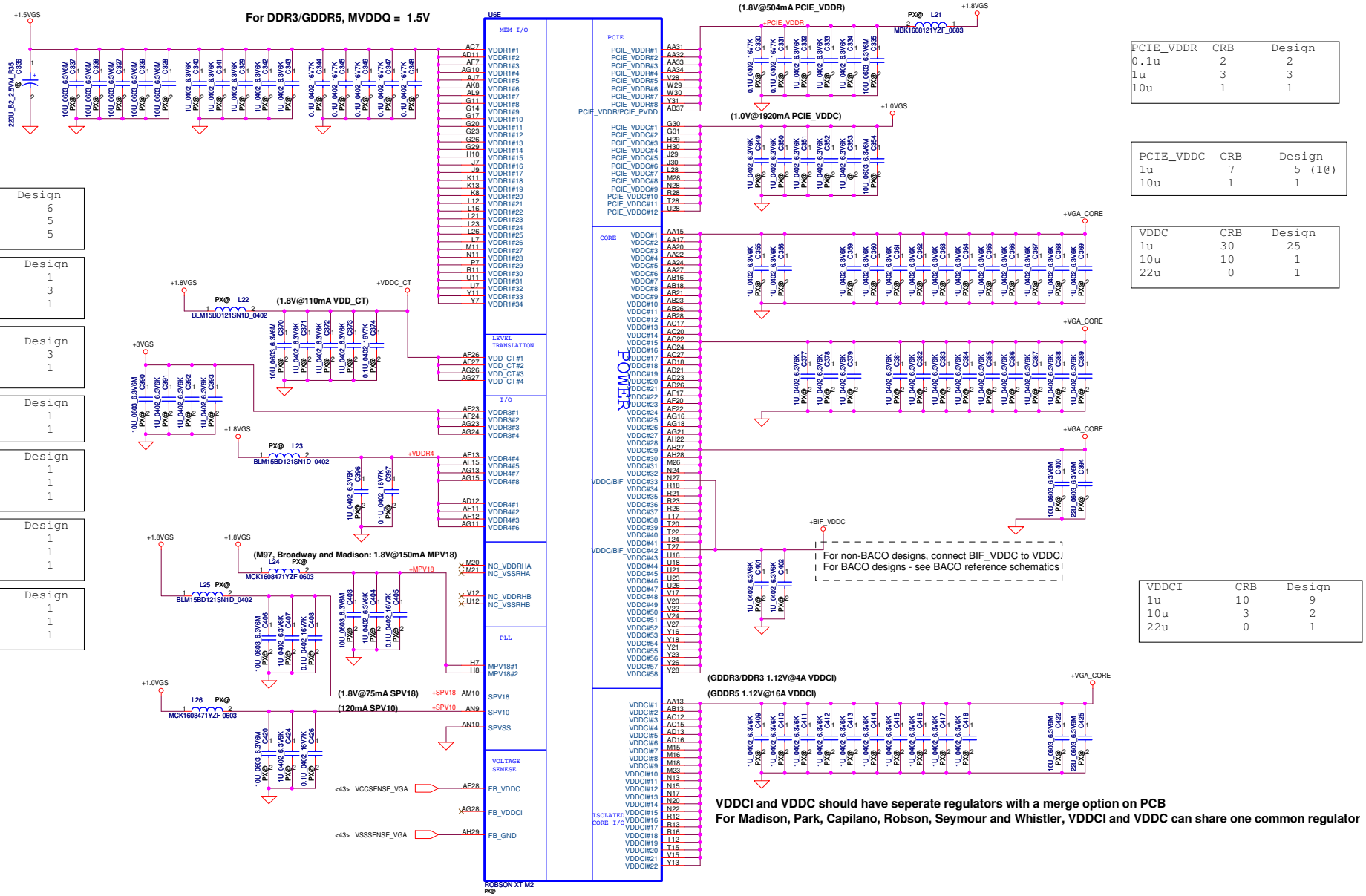
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_PWR_GND

Size	Document Number	Rev
C	LA8681P	0.1

Date: Wednesday, November 30, 2011 Sheet 18 of 48



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

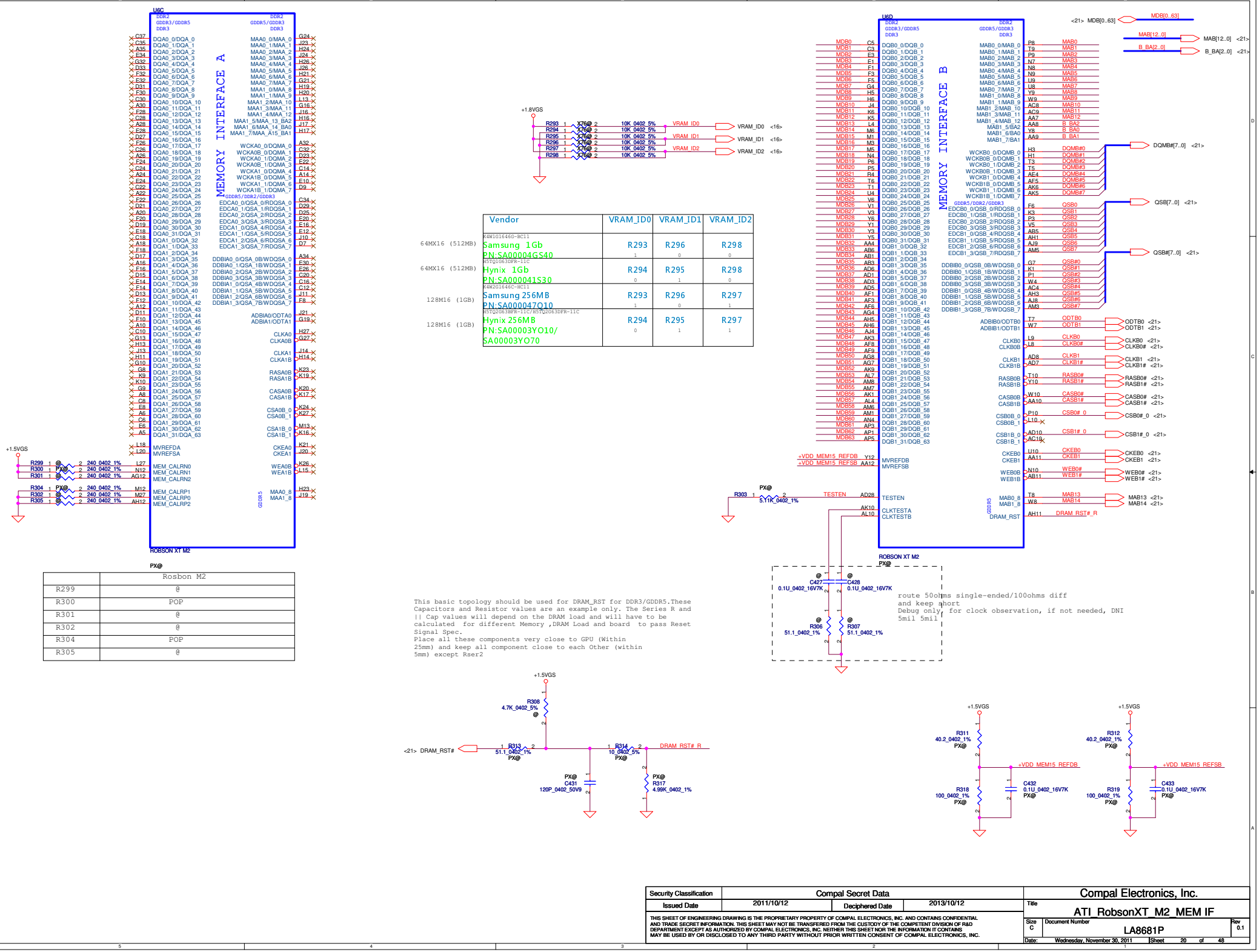
PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/10/12	Deciphered Date 2013/10/12	Title: ATI_RobsonXT_M2_Power
			Size: C; Document Number: LA8681P; Rev: 0.1
			Date: Wednesday, November 30, 2011; Sheet 19 of 48



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (512MB) K4W1G1646G-BC11 Samsung 1Gb PN:SA00004GS40	R293 1	R296 0	R298 0
64MX16 (512MB) H5TQ1G63DFR-11C Hynix 1Gb PN:SA00041S30	R294 0	R295 1	R298 0
128M16 (1GB) K4W2G1646C-HC11 Samsung 256MB PN:SA00047Q10	R293 1	R296 0	R297 1
128M16 (1GB) H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003YO70	R294 0	R295 1	R297 1

PX@

Rosbon M2
R299 @
R300 POP
R301 @
R302 @
R304 POP
R305 @

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

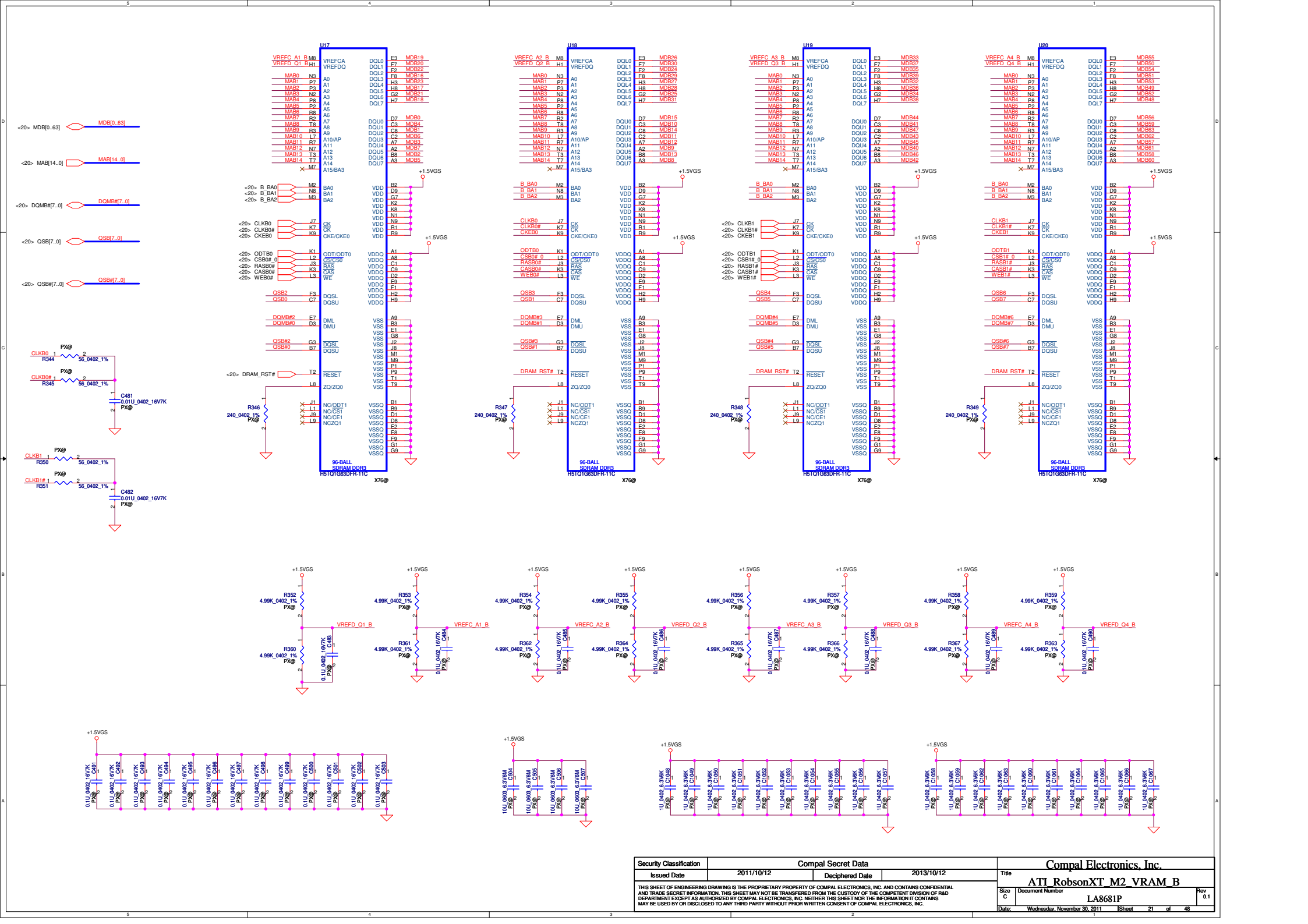
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_MEM IF

Size	Document Number	Rev
C	LA8681P	0.1

Date: Wednesday, November 30, 2011 Sheet 20 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_VRAM_B

Size	Document Number	Rev
C	LA8681P	0.1

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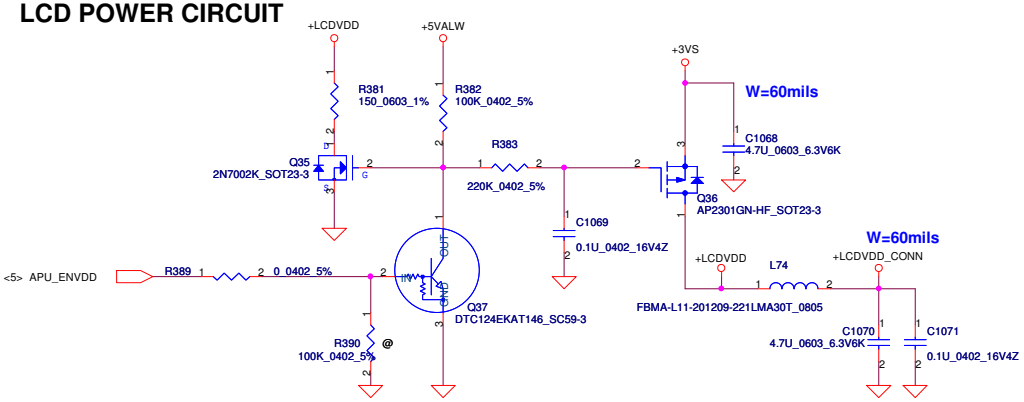
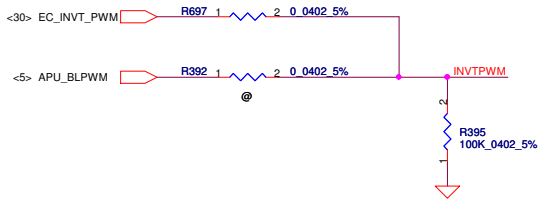
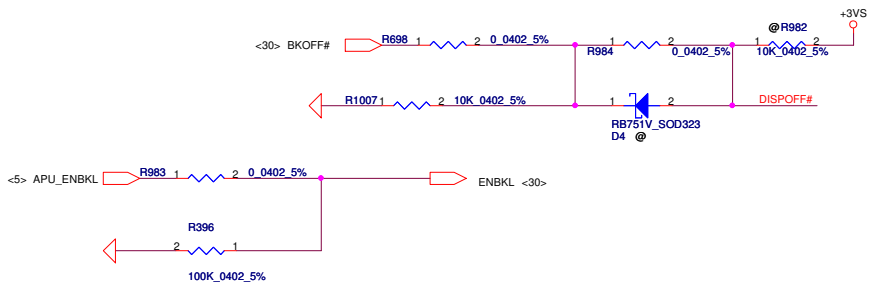
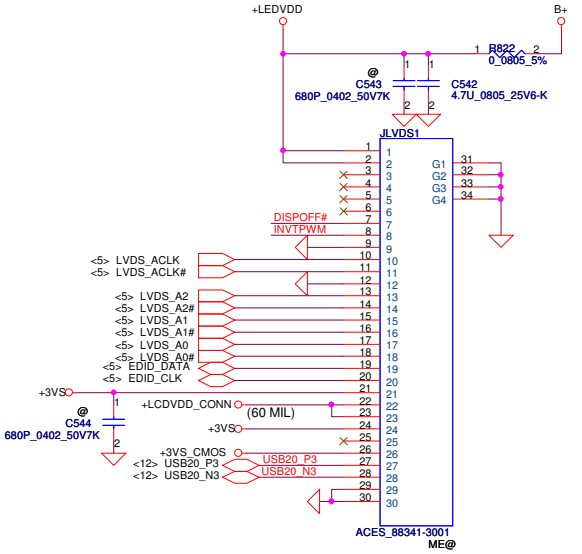
LCD POWER CIRCUIT

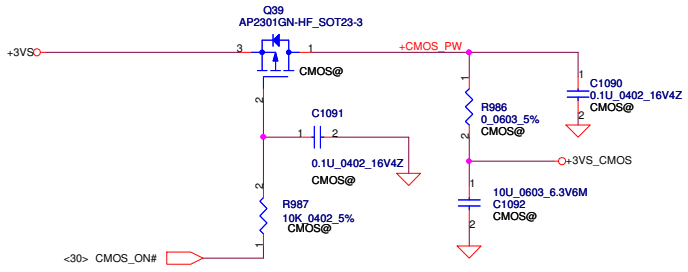








CMOS Camera



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: LVDS/CAMERA

Size	Document Number	Rev
B	LA8681P	0.1

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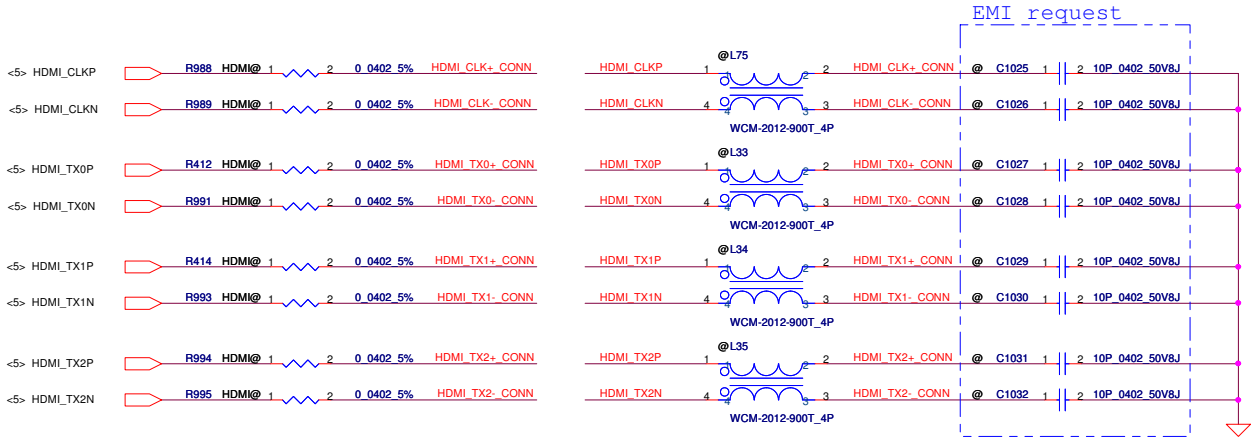
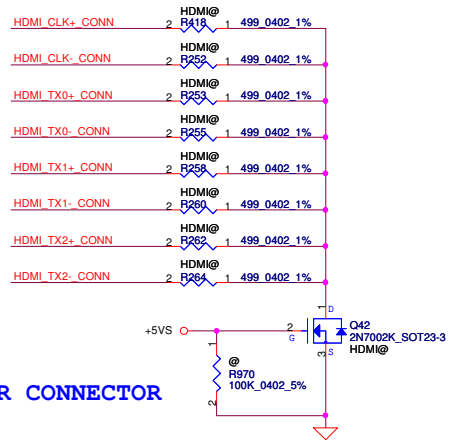
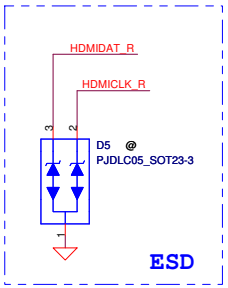
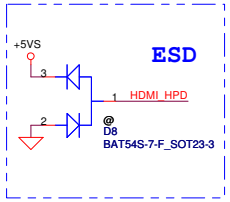
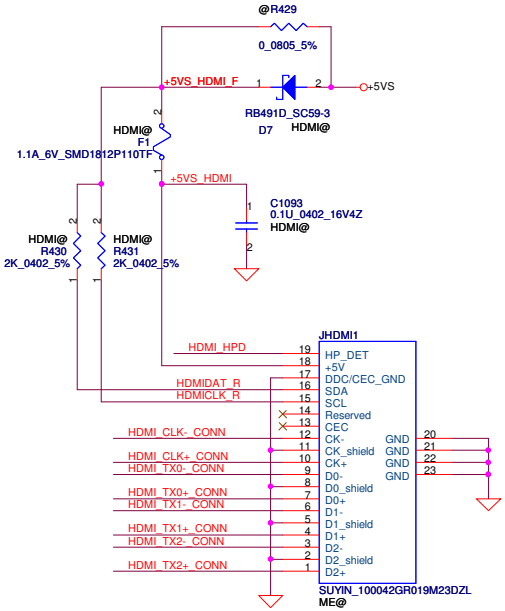
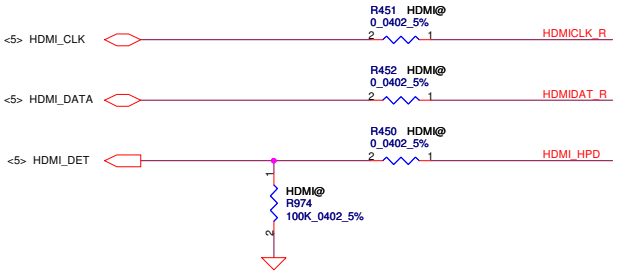












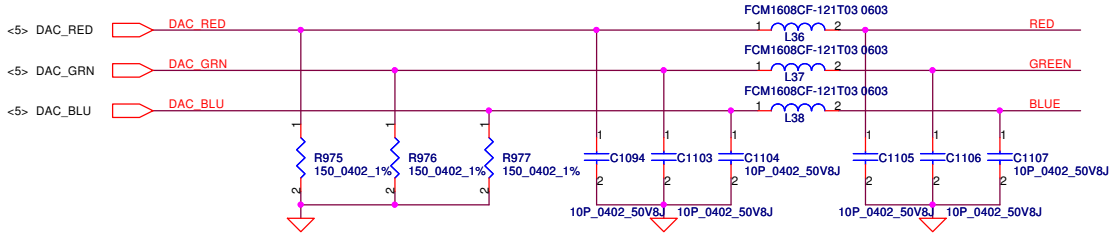
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

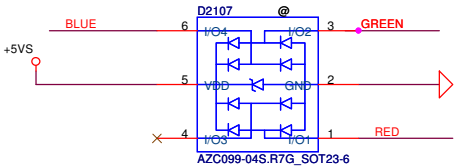
Compal Electronics, Inc.

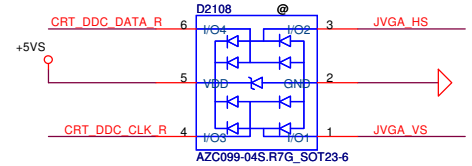
Title: HDMI Connector

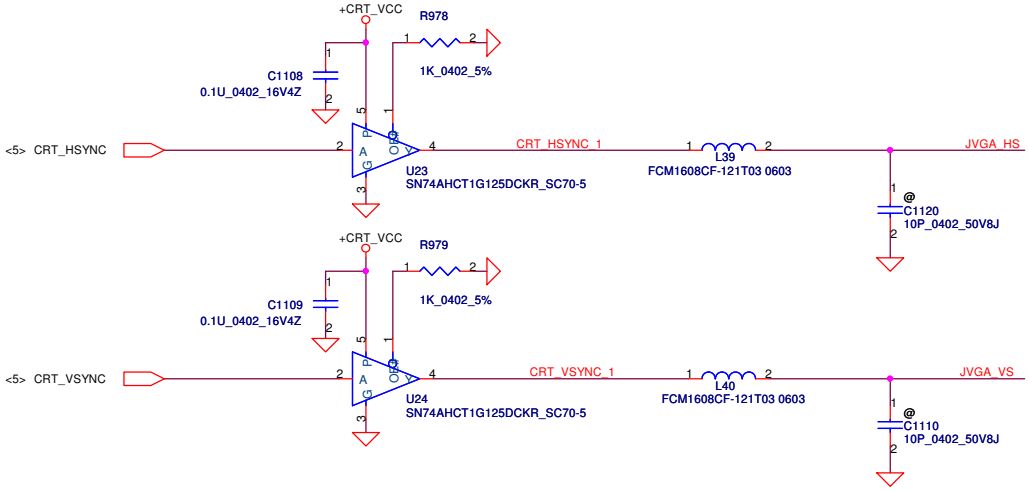
Size	Document Number	Rev
Custom	LA8681P	0.1

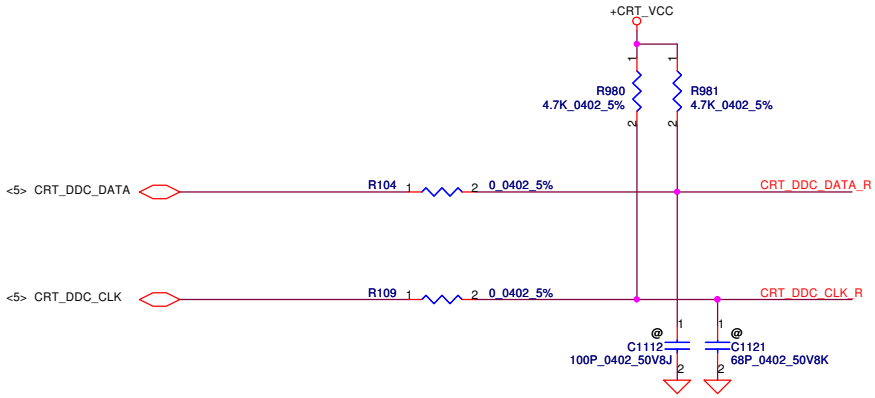
Date: Wednesday, November 30, 2011 Sheet 23 of 48

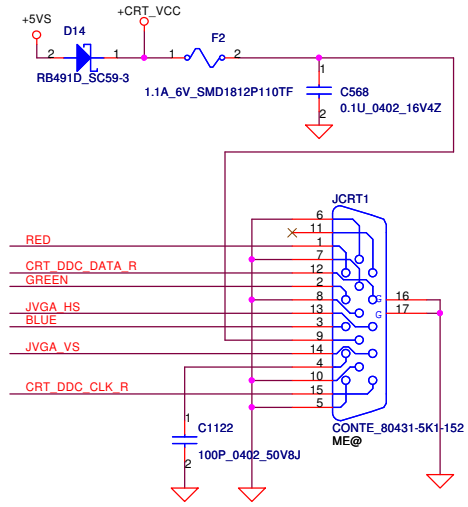












Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA8681P | Rev: 0.1

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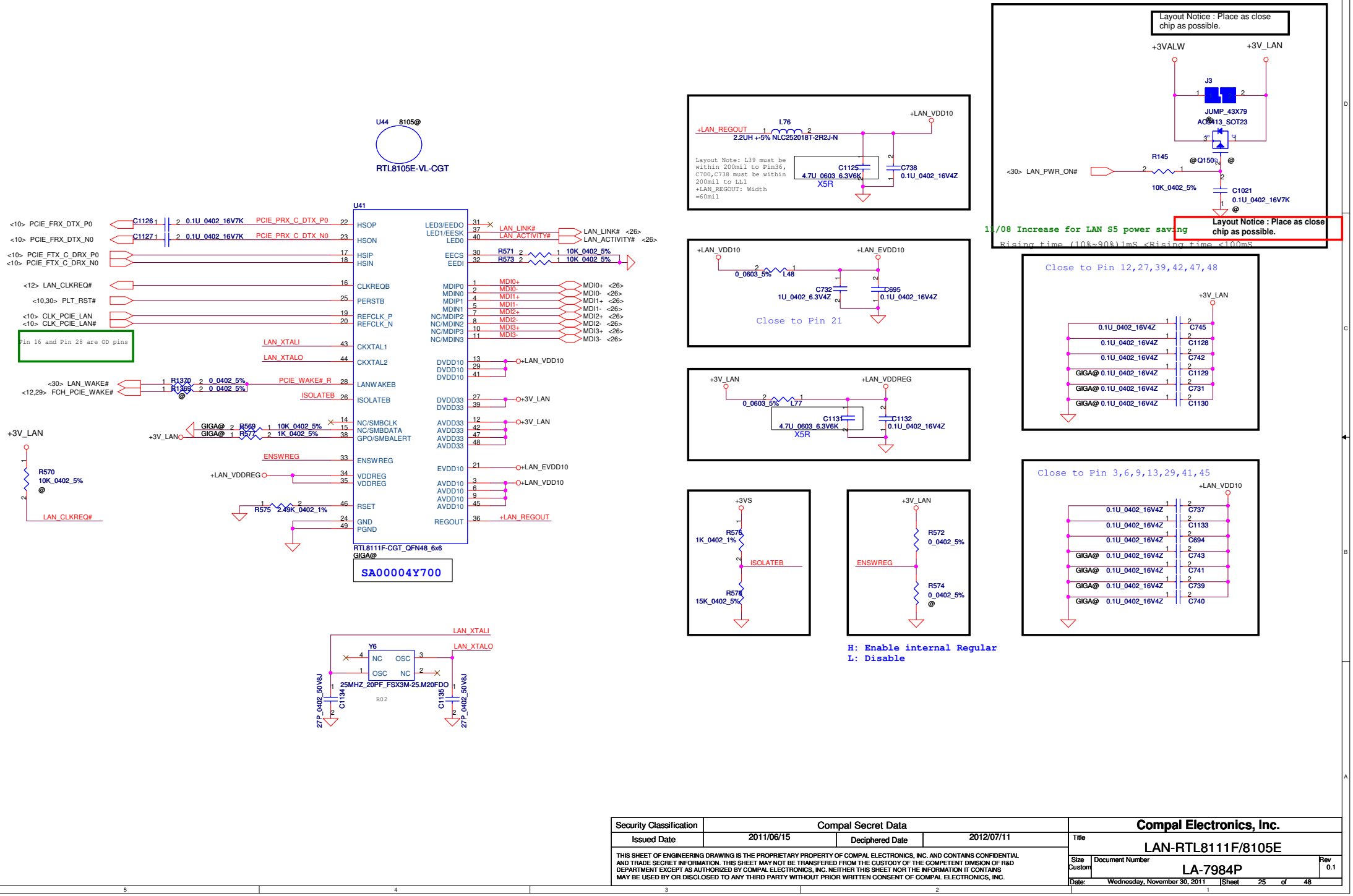


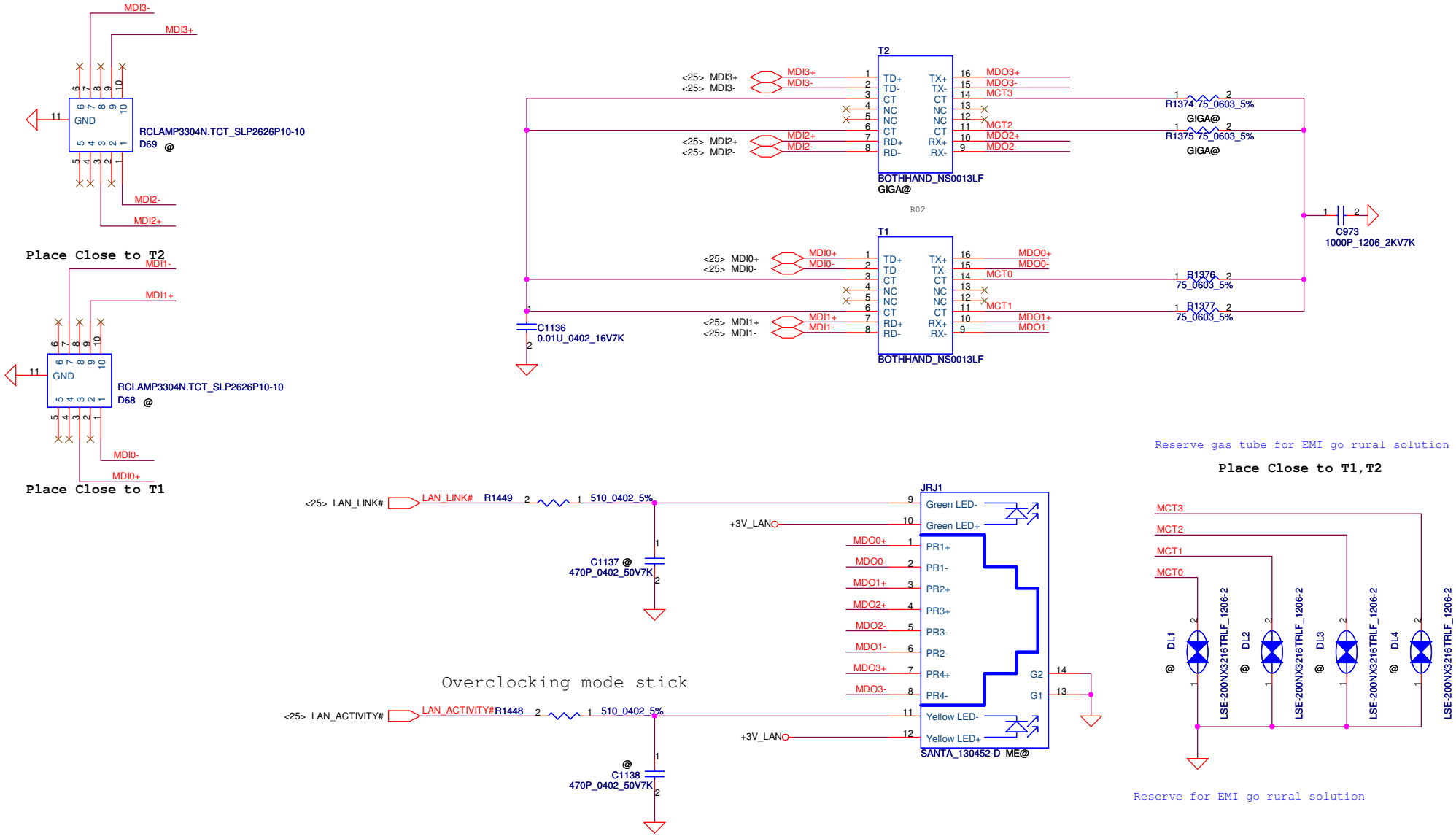
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-RTL8111F/8105E

Size	Document Number	Rev
Custom	LA-7984P	0.1

Date: Wednesday, November 30, 2011 Sheet 25 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN_Transformer

Size	Document Number	Rev
B	LA-7984P	0.1

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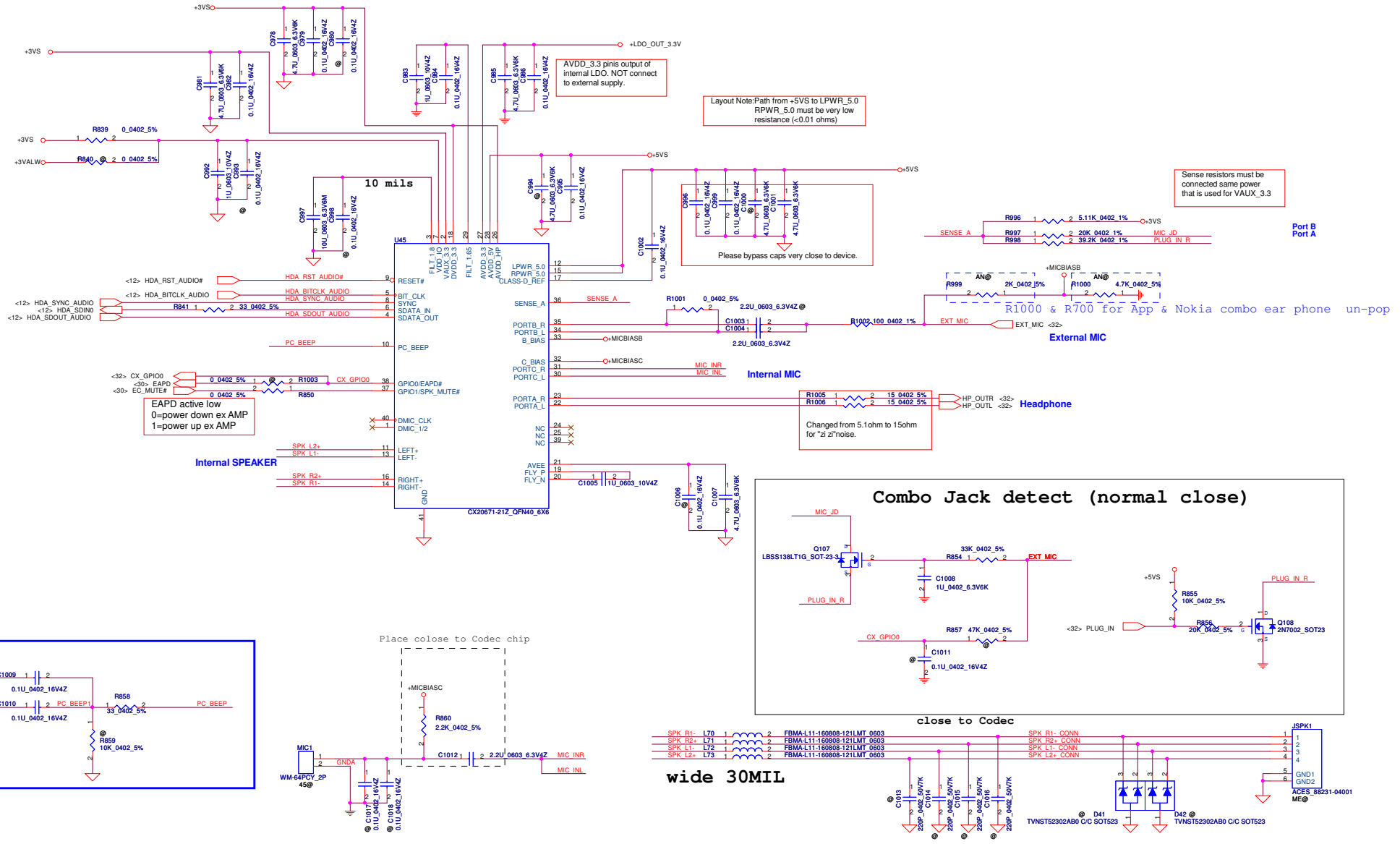
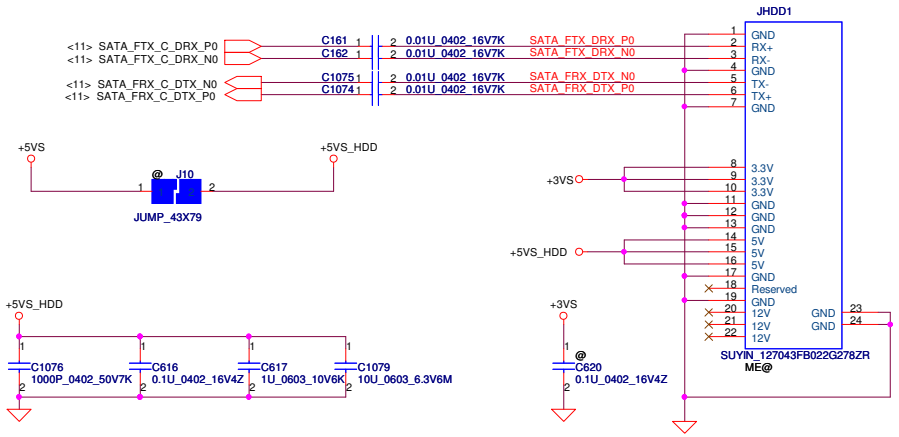
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



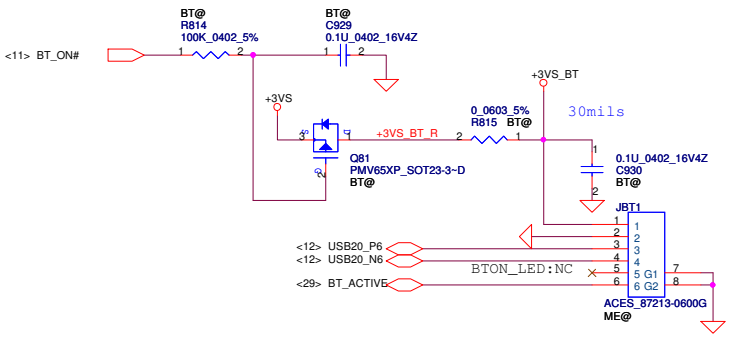
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	CX20671 Codec		
Size	Document Number		Rev
Custom	LA8681P		0.1
Date: Wednesday, November 30, 2011	Sheet	27	of 48

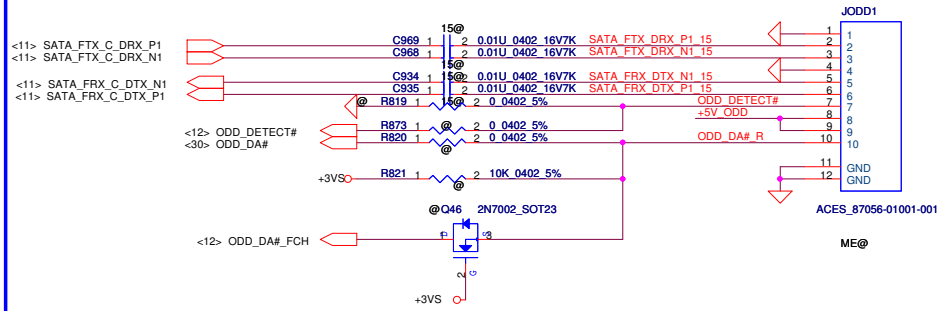
HDD CONN



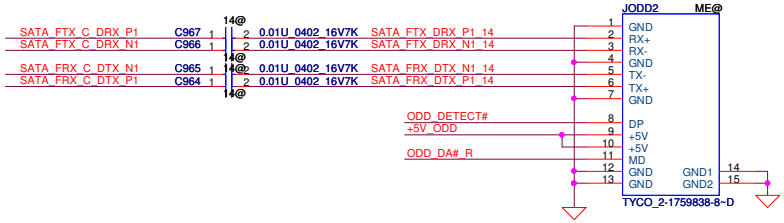
BT MODULE CONN



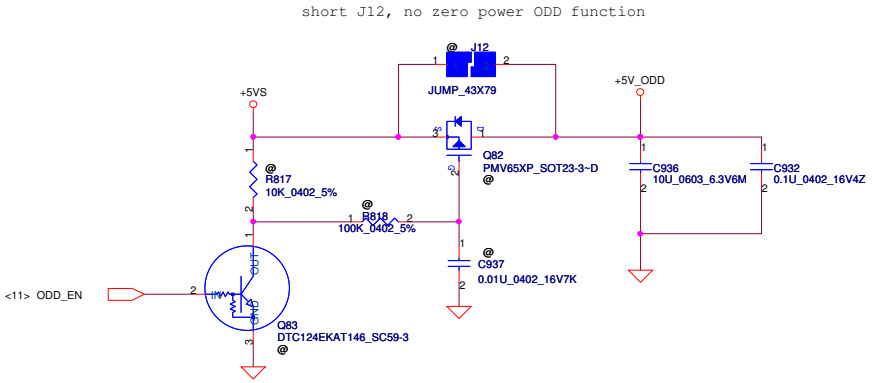
ODD CONN 15"



ODD CONN 14"



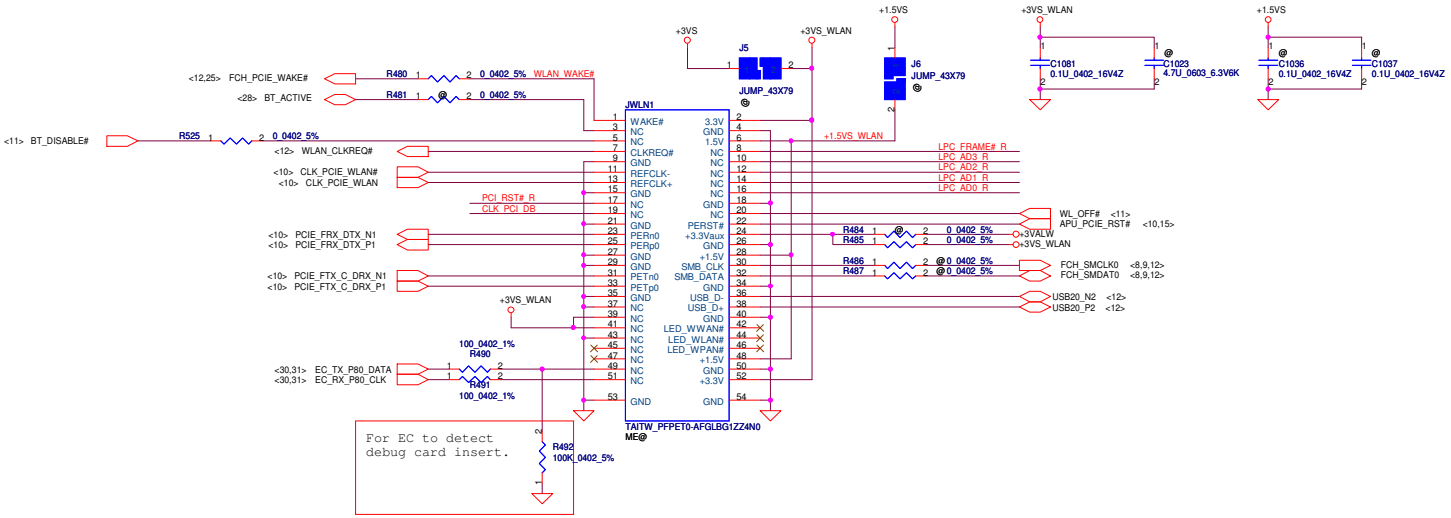
short J12, no zero power ODD function



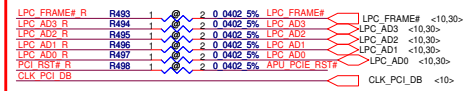
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	HDD/ODD/BT		
Size B	Document Number LA8681P		Rev 0.1
Date: Wednesday, November 30, 2011	Sheet 28 of 48		

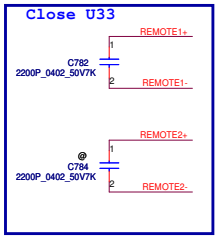
Mini-Express Card for WLAN/WiMAX(Half)



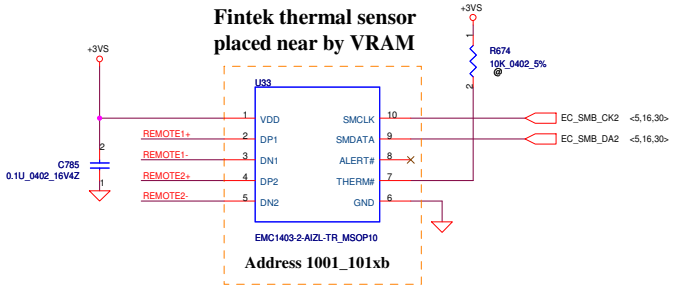
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Close U33



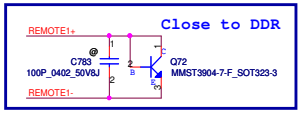
Fintek thermal sensor placed near by VRAM



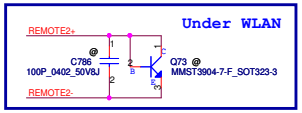
Address 1001_101xb

Change from SA000029210 to SA000046C00 for main source

Close to DDR



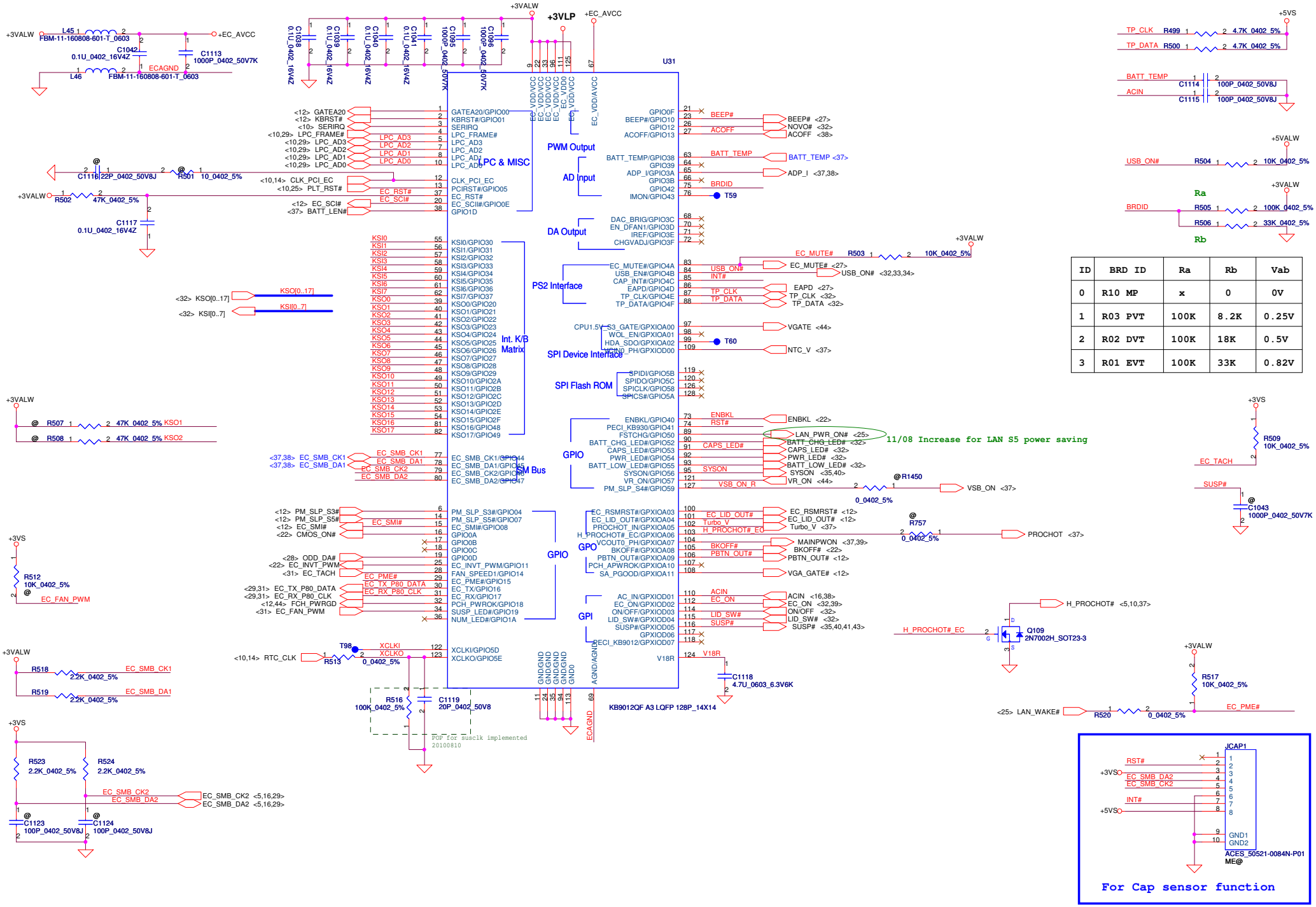
Under WLAN



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	Mini PCIE/Thermal IC		
Size	Document Number		Rev
	LA8681P		0.1
Date:	Wednesday, November 30, 2011	Sheet	29 of 48



ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

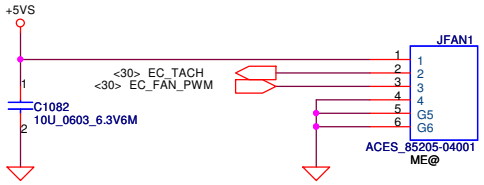
Compal Electronics, Inc.

Title: KB9012/Cap sensor

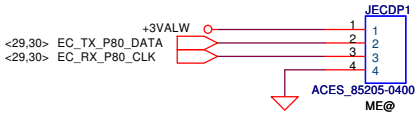
Size	Document Number	Rev
Custom	LA8681P	0.1

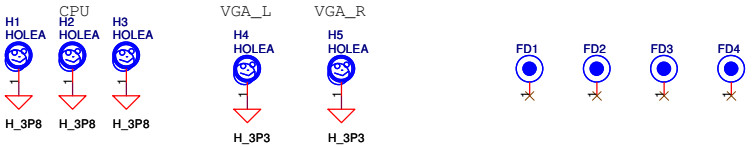
Date: Wednesday, November 30, 2011 | Sheet 30 of 48

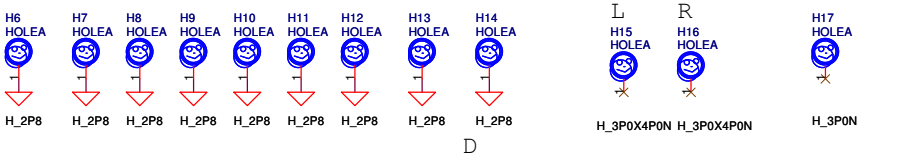
FAN CONN



EC DEBUG PORT







2P8 * 9 pcd

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FAN/SCREW/EC Debug

Size	Document Number	Rev
B	LA8681P	0.1

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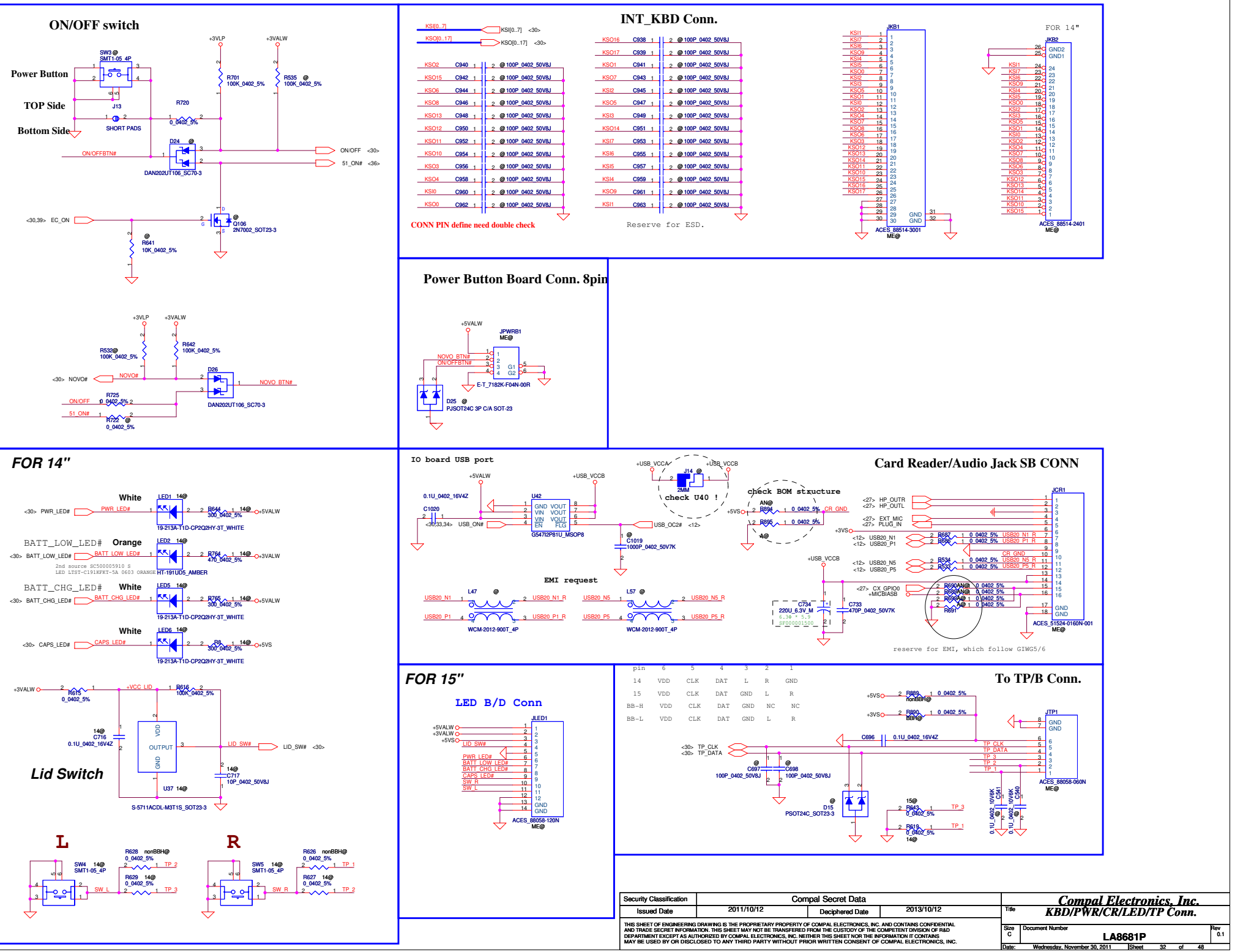
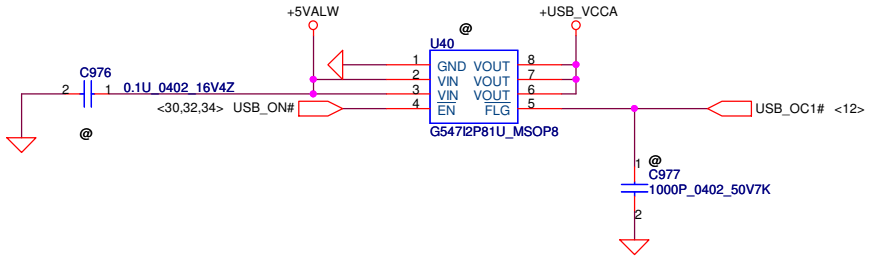
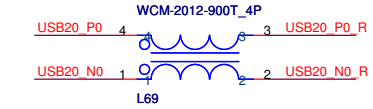


Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

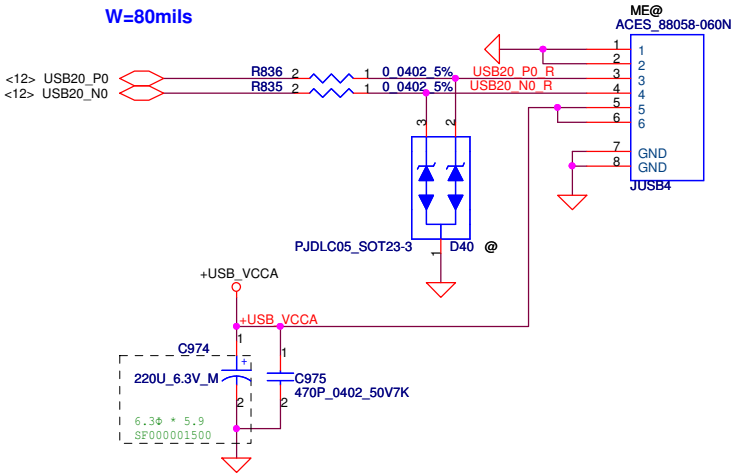
Title	Compal Electronics, Inc. KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA8681P		Rev 0.1
Date: Wednesday, November 30, 2011	Sheet 32 of 48		



Right Ext.USB FFC Conn.



Update to SM070001S00 for EMI request



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: USB cable port

Size	Document Number	Rev
B	LA8681P	0.1

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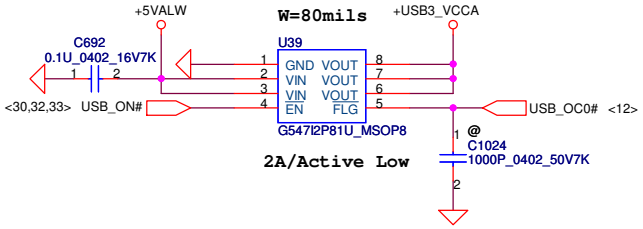

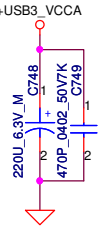

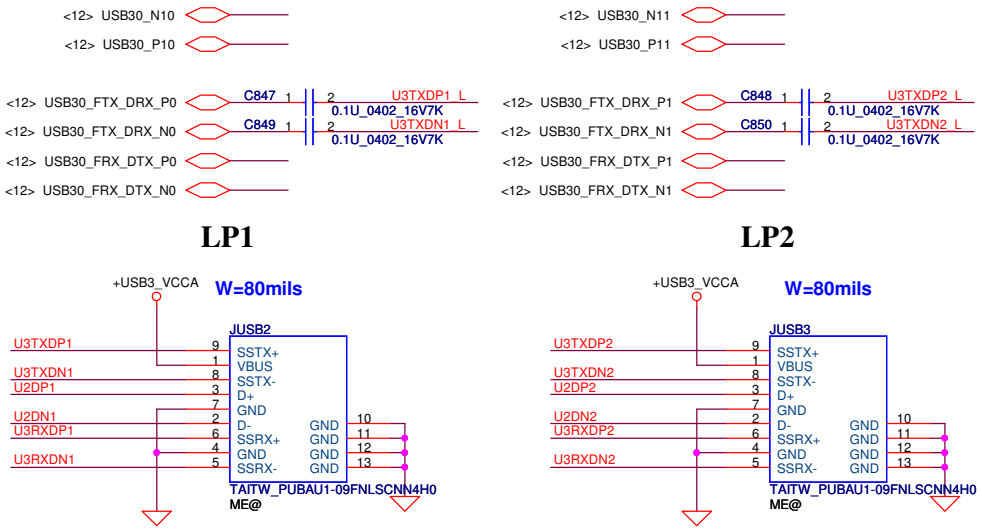

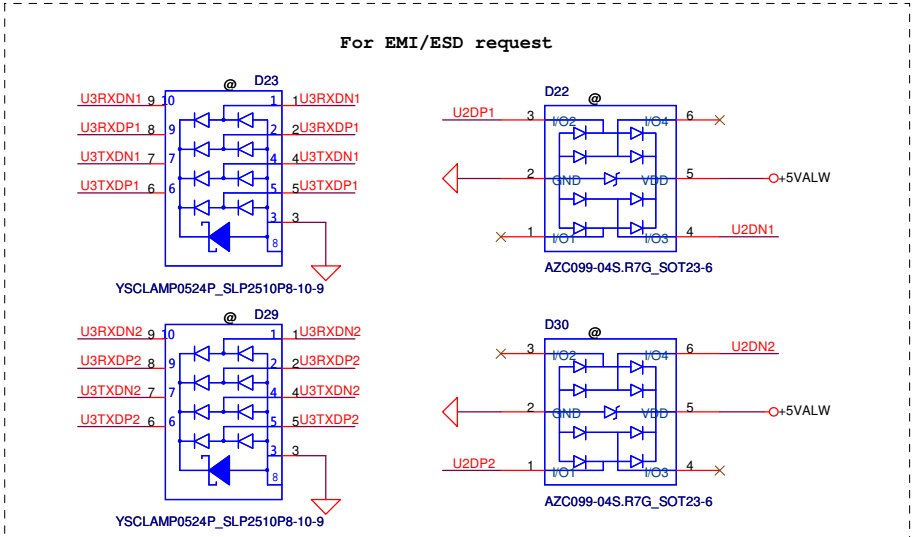

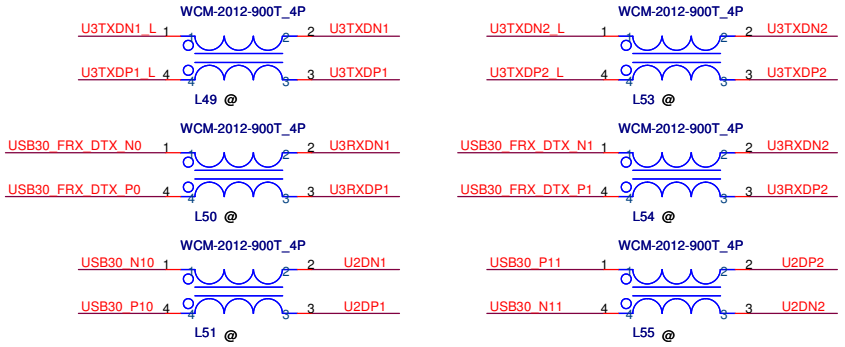

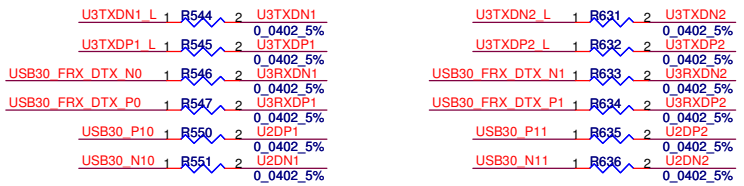

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: Left USB3.0

Size	Document Number	Rev
B	LA8681P	0.1

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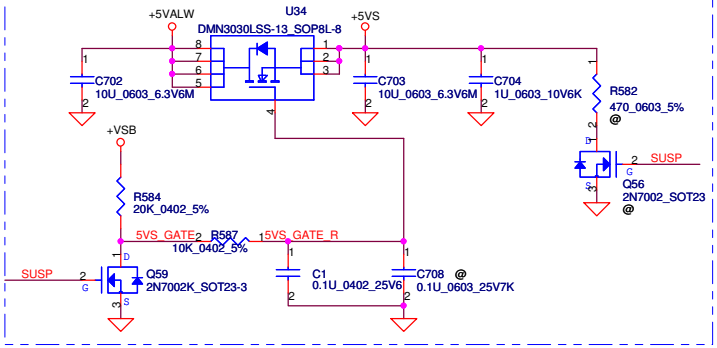
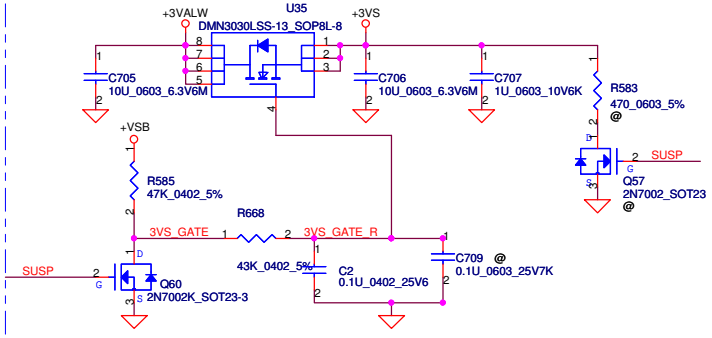
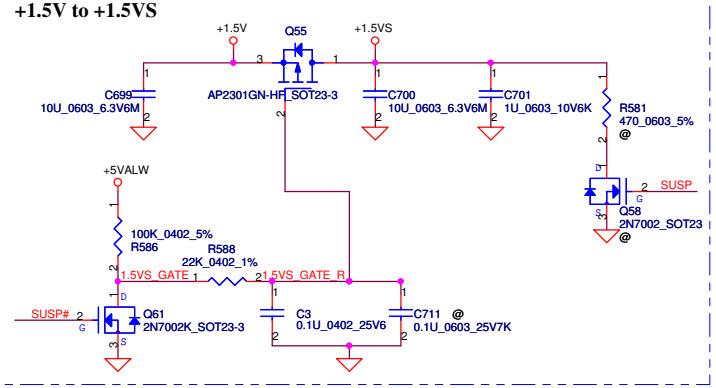
+5VALW TO +5VS



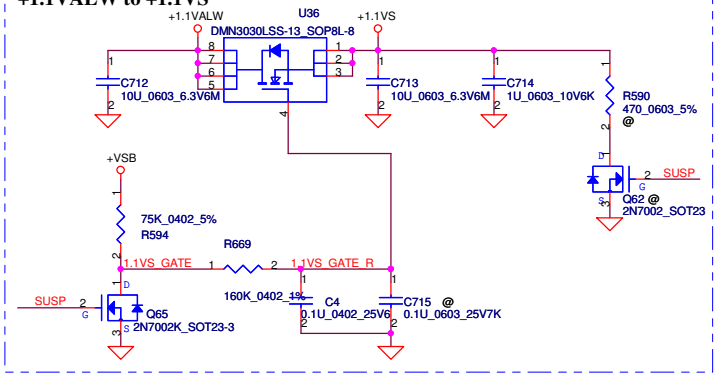
+3VALW TO +3VS

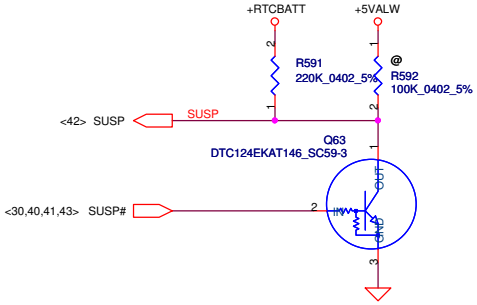


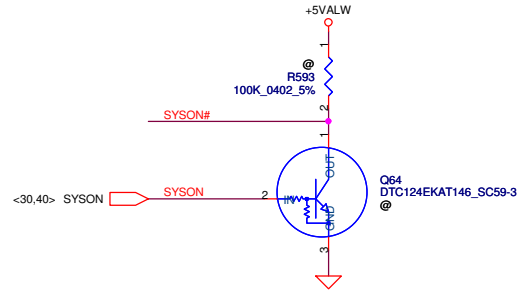
+1.5V to +1.5VS

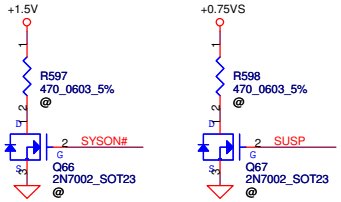


+1.1VALW to +1.1VS









Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA8681P	0.1

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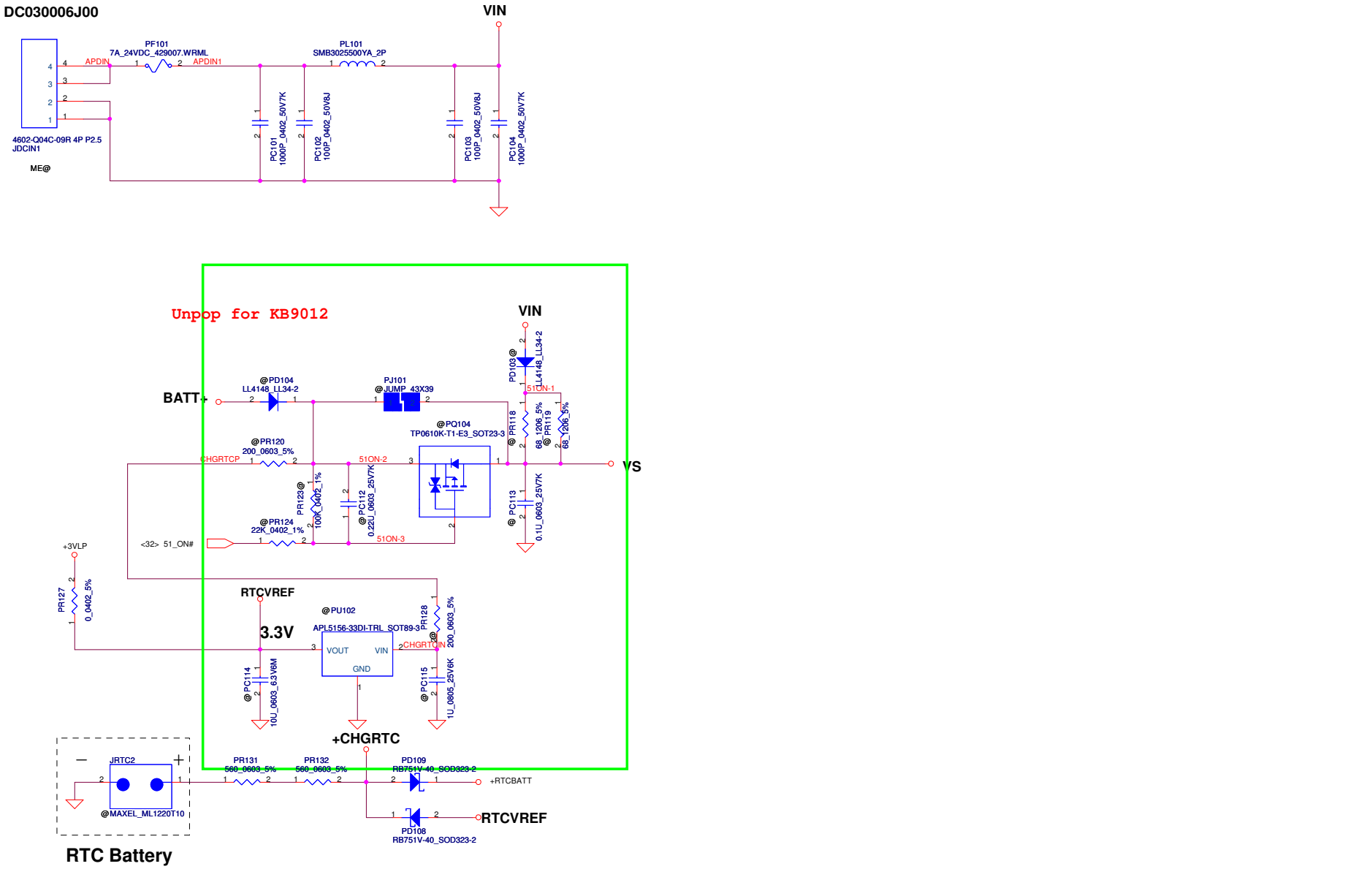


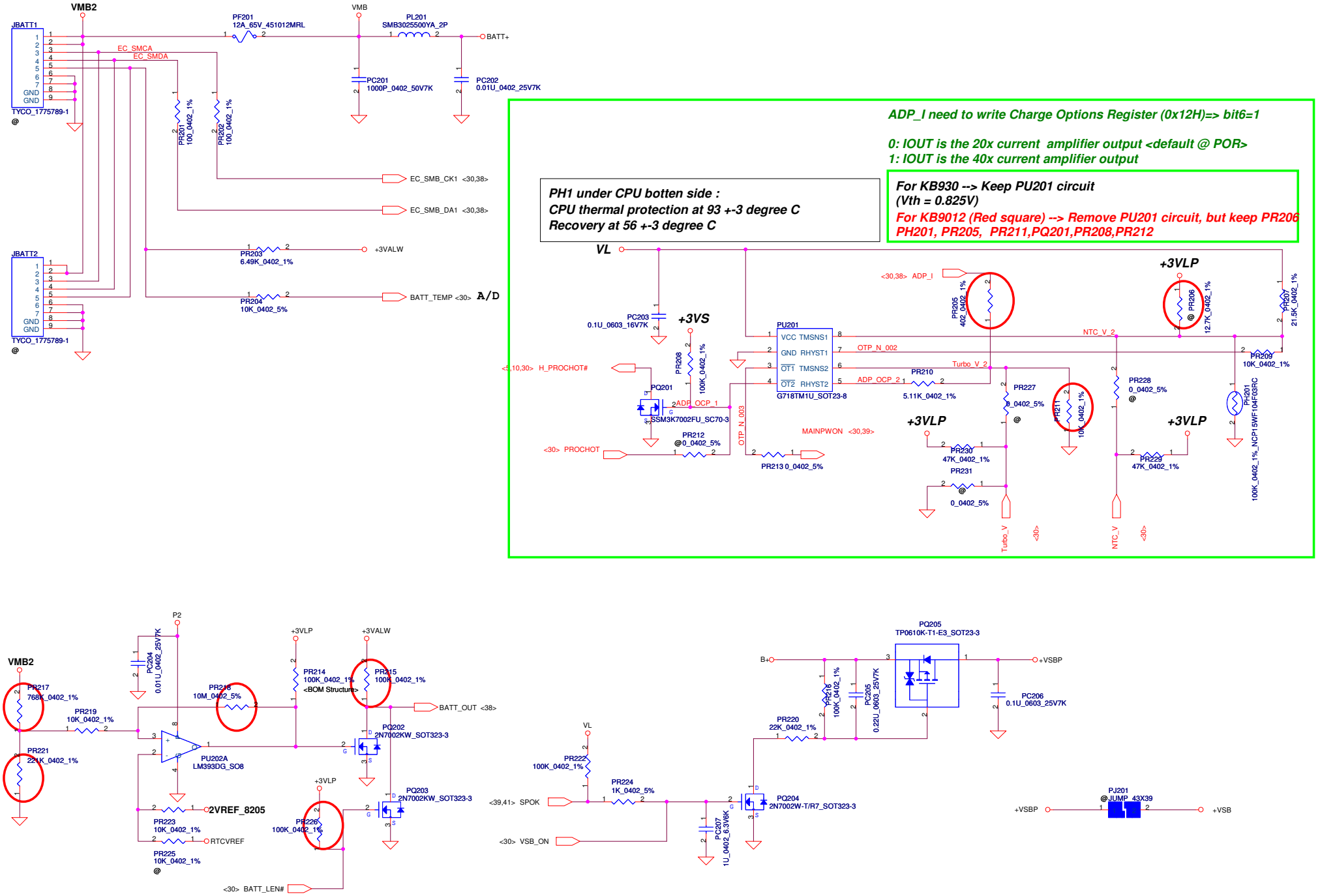
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR DCIN

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, November 30, 2011 Sheet 36 of 48



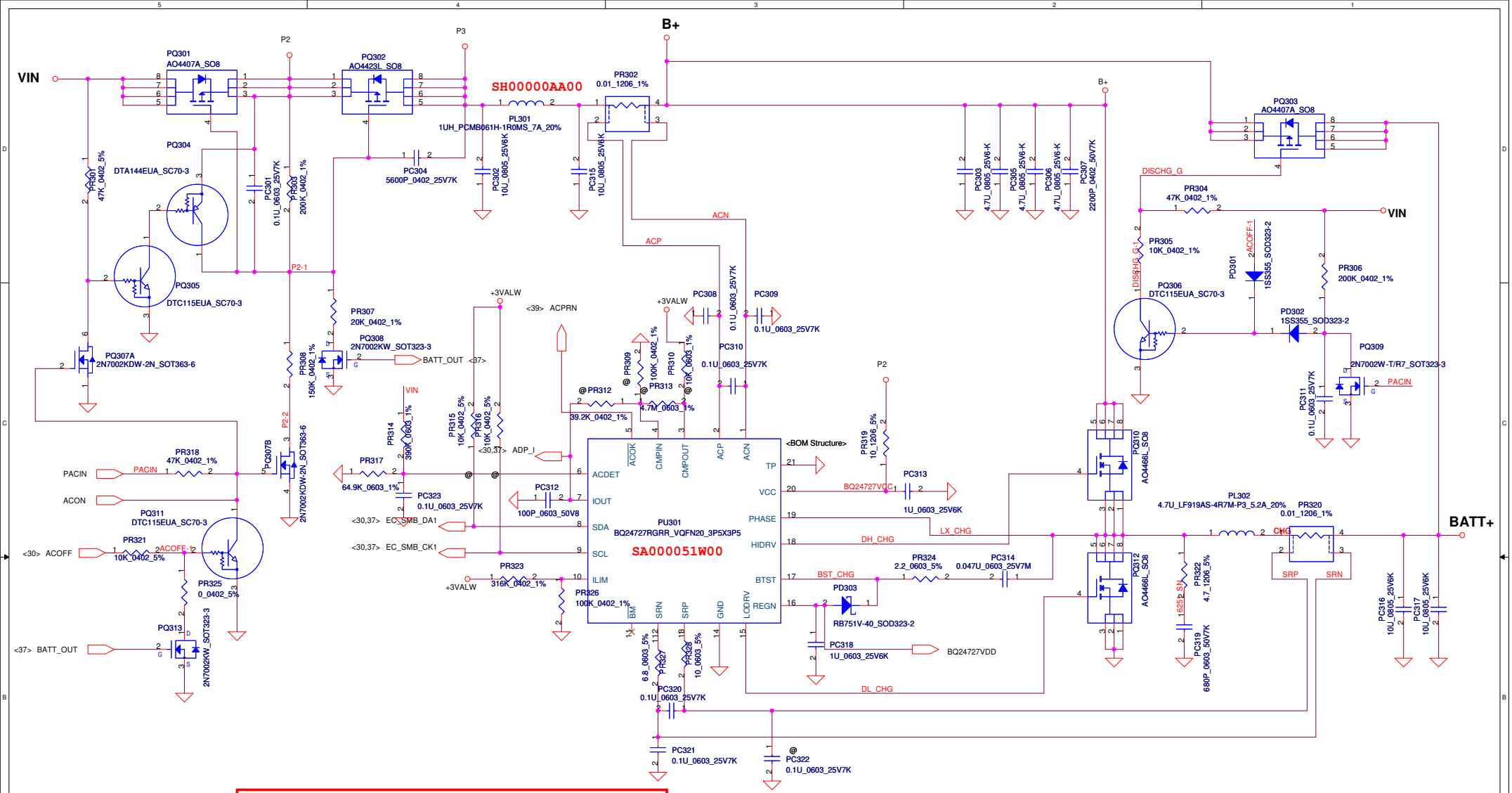
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, November 30, 2011 Sheet 37 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.1

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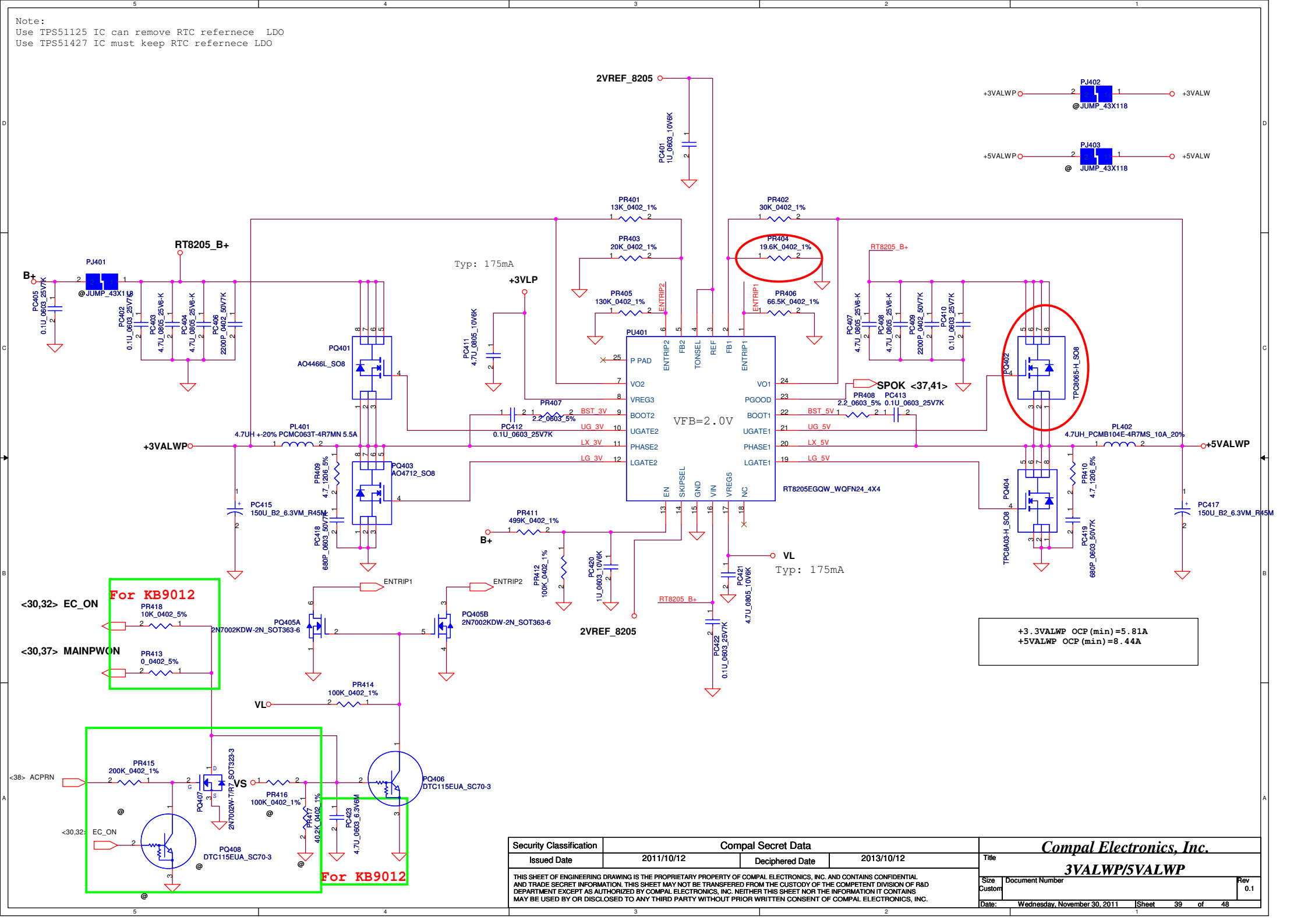
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



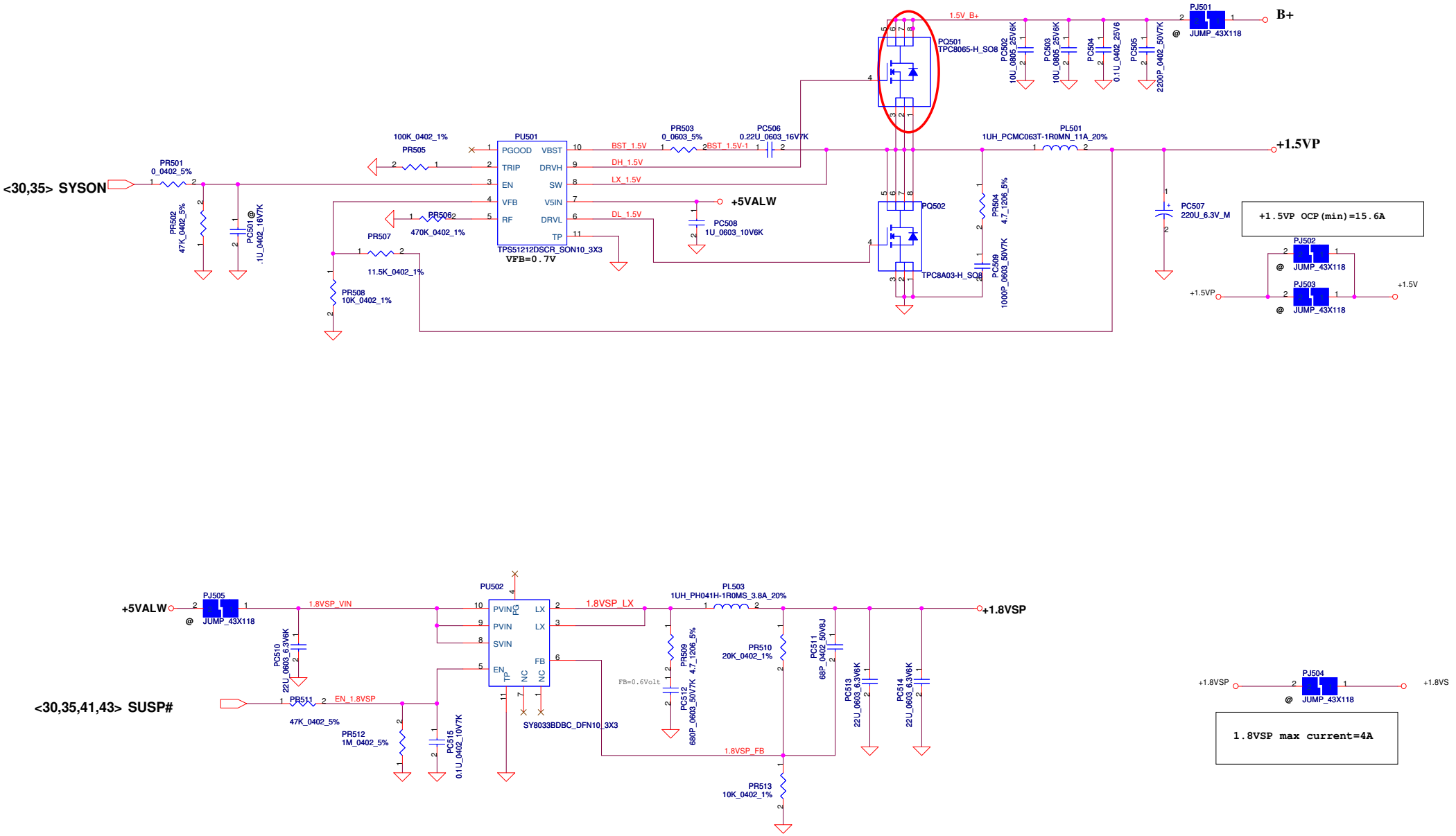
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

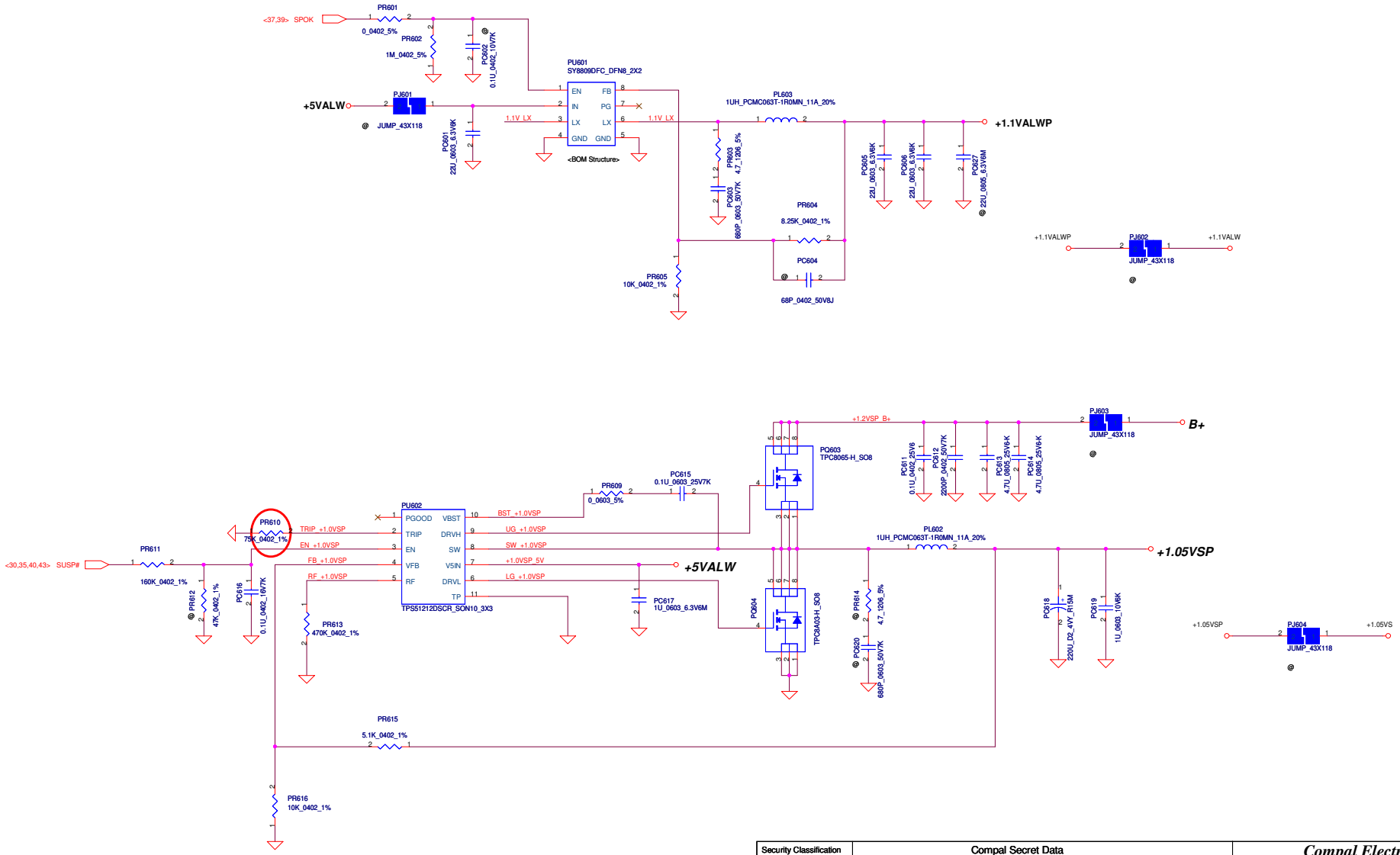
Size	Document Number	Rev
Custom		0.1

Date: Wednesday, November 30, 2011 Sheet 39 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.	
Title	PWR-+1.5VP/+1.8VSP
Size: Custom	Document Number:
Rev: 0.1	
Date: Wednesday, November 30, 2011	Sheet 40 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR +1.1VALWP/+1.0VSP

Size	Document Number	Rev
C		0.1

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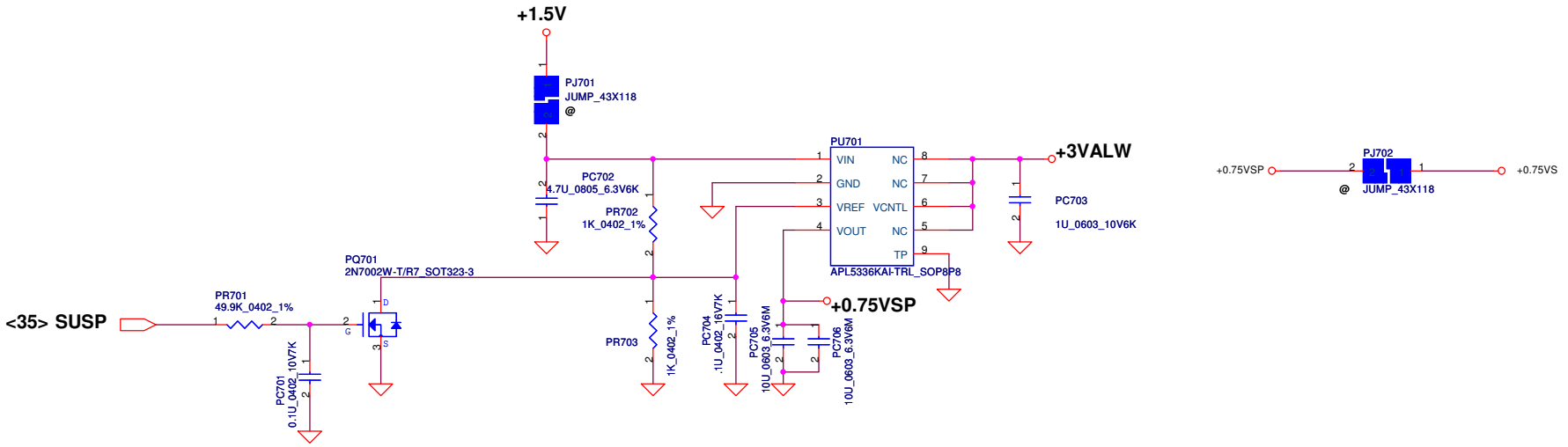


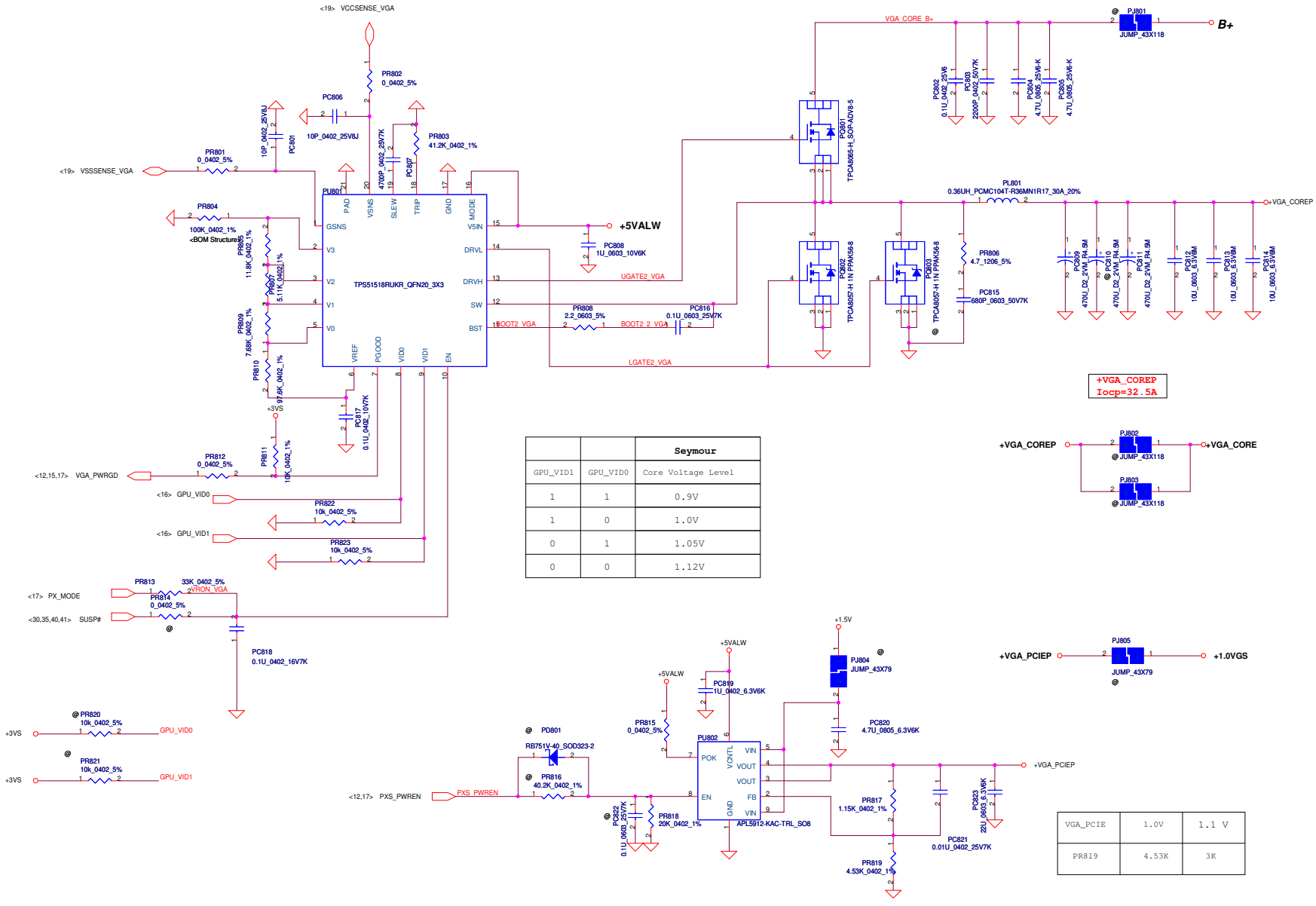
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR +0.75VSP

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, November 30, 2011 Sheet 42 of 48



		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.12V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-VGA_CORE/VGA_PCIE

Size | Document Number | Rev 0.1

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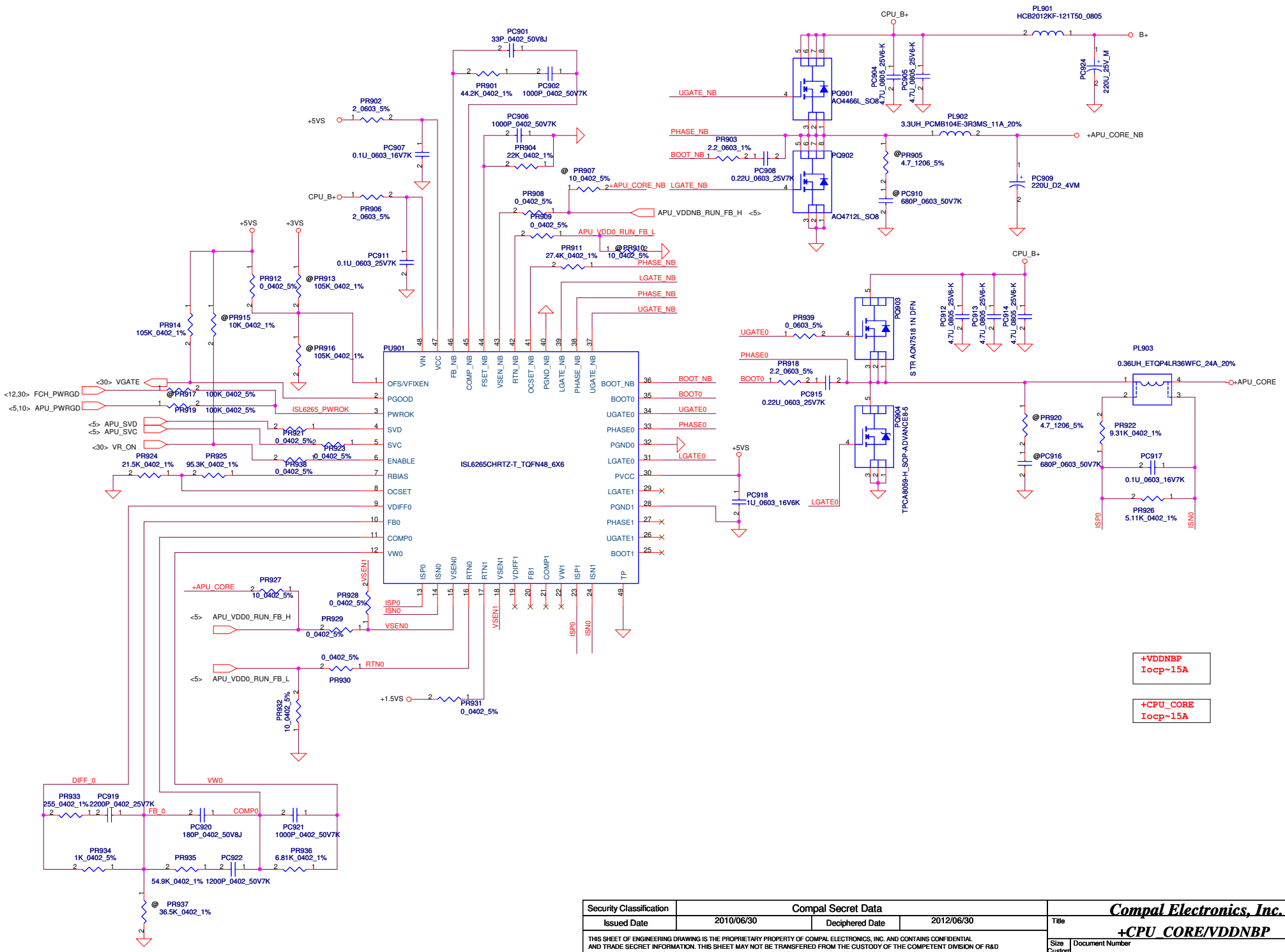

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: +CPU_CORE/VDDNBP

Size	Document Number	Rev
Custom		0.1

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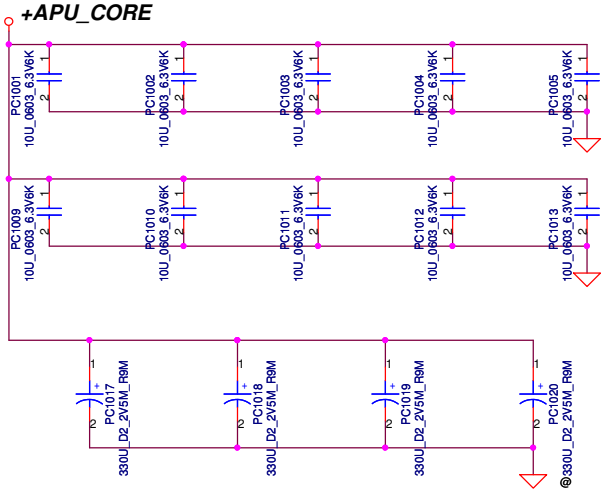
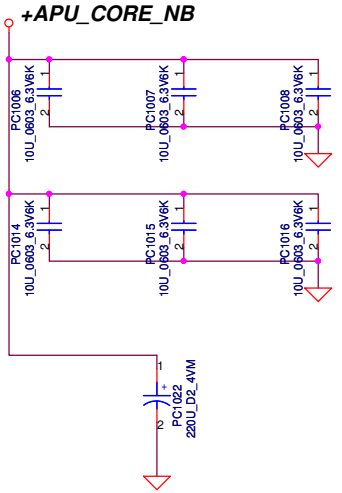
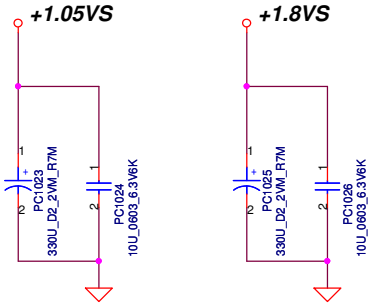
+CPU_CORE



+CPU_CORE_NB





Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size	Document Number	Rev
		0.1

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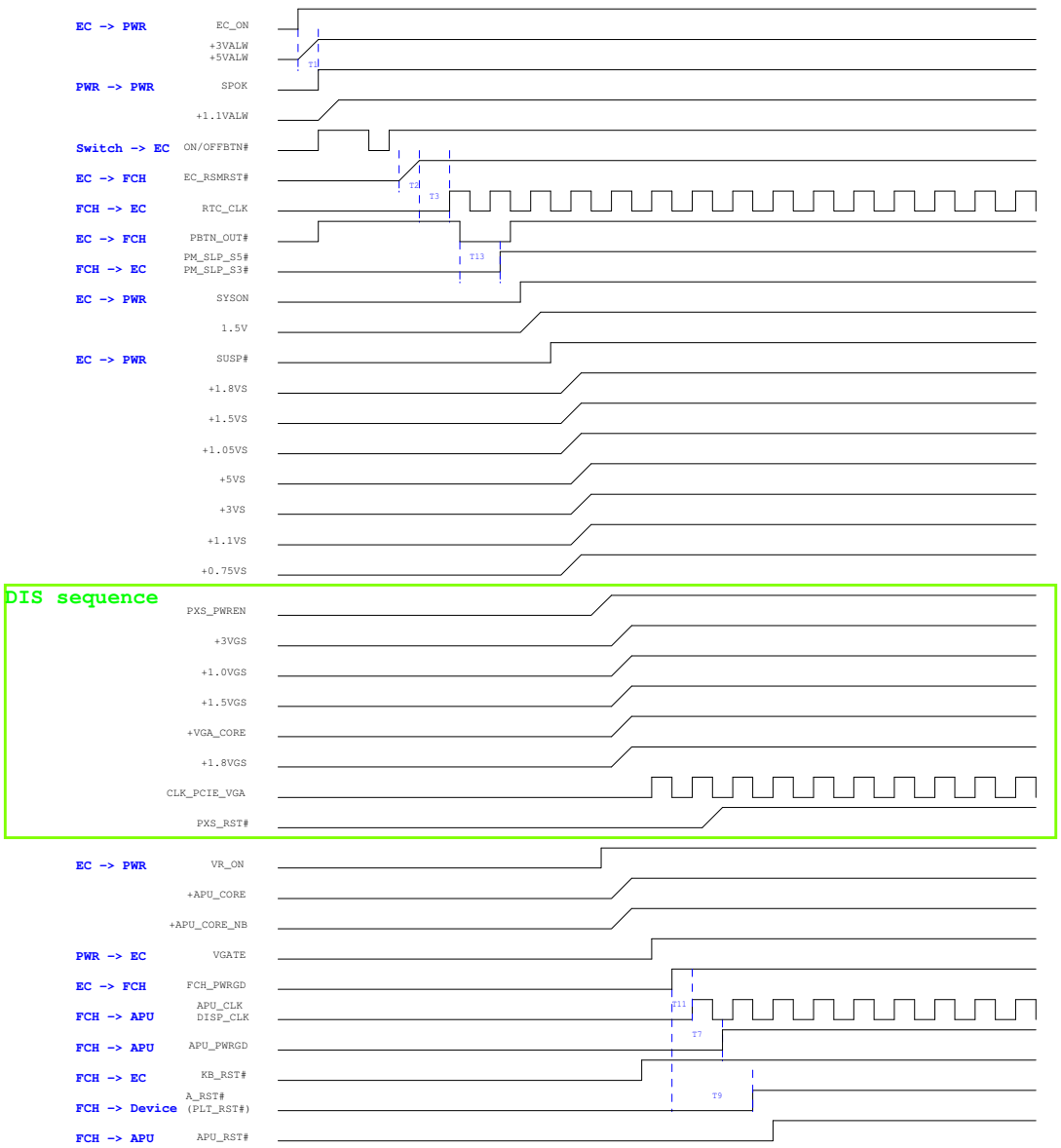
Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	(CPU CORE/VDDNBP)...VR_ON增加PR938				
2	0402 0 歐姆				
3	APU_CORE_NB....PC1021拿掉				
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

QAWGE Power Sequence (AC mode)



1ms< T1 < 100ms : +3VALW rising time, for LAN chip request
+3VALW need rampe up before +1.1VALW or at the same time.

T2 < 50ms : EC_RSMRST# rising time
+3VALW need rampe up before EC_RSMRST# de-assertion at least 10ms
+1.1VALW need rampe up before EC_RSMRST# de-assertion
T3 > 16ms : EC_RSMRST# de-assert to start RTCCLK

T13 > 200ns : PBTN_OUT# to SLP_S3#/S5# de-assertion

+3VS need rampe up before +1.1VS or at the same time.

The time delay between PXS_PWREN assertion
and PXS_RST# de-assertion must be more than 100ms.

CLK_PCIE_VGA should be 100us earlier than PXS_RST# de-assert.

T11< 32ms : FCH_POK assertion to clock out

98ms< T7< 150ms : FCH_POK assertion to APU_PWRGD

KB_RST# should be de-asserted before FCH_POK

101ms< T9< 113ms :
FCH_POK assertion to A_RST# de-assertion

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	PWR - PROCESSOR DECOUPLING		
Size	Document Number		Rev 0.1
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