

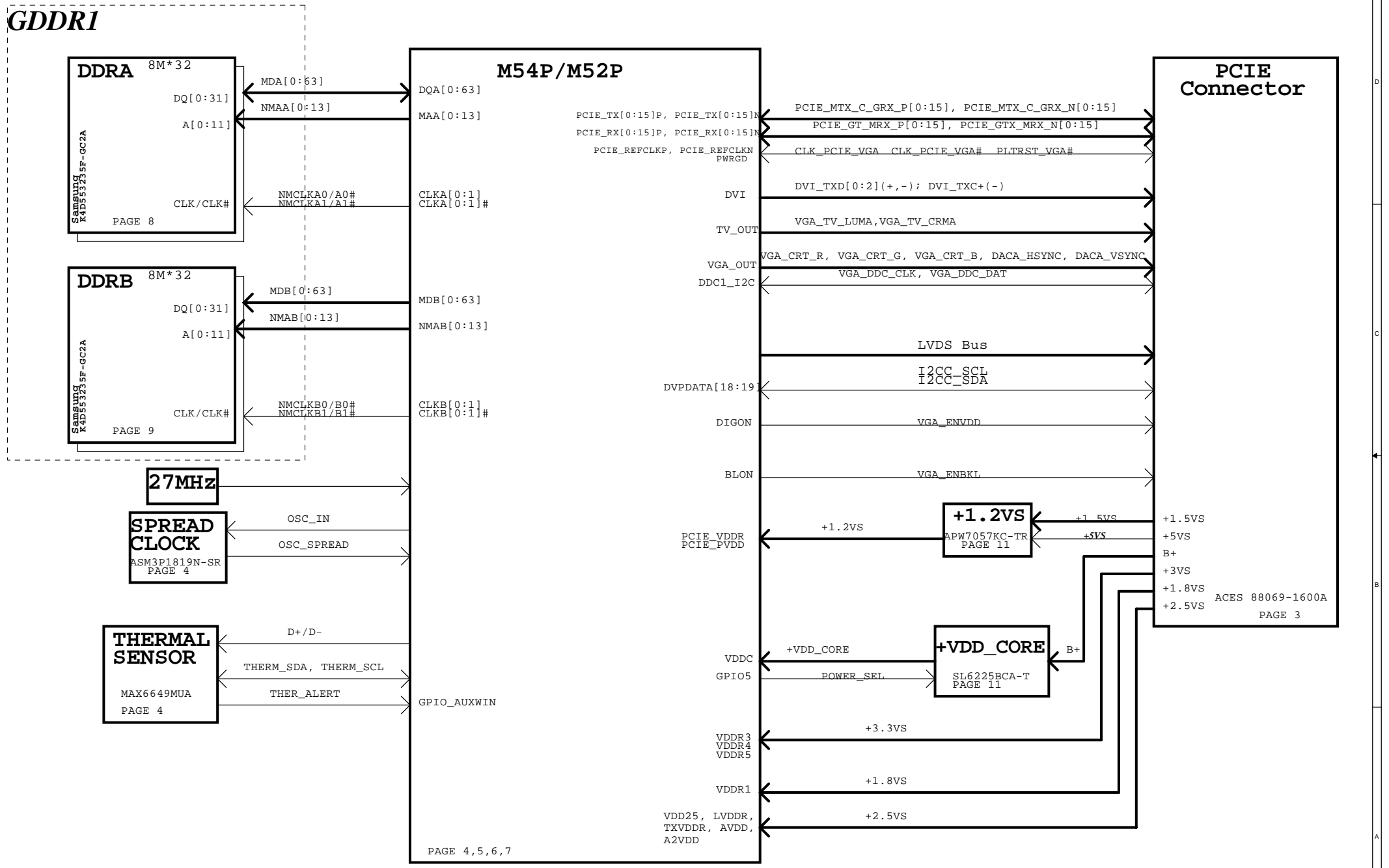


Mini (EFL50) ATI VGA/B M52-P

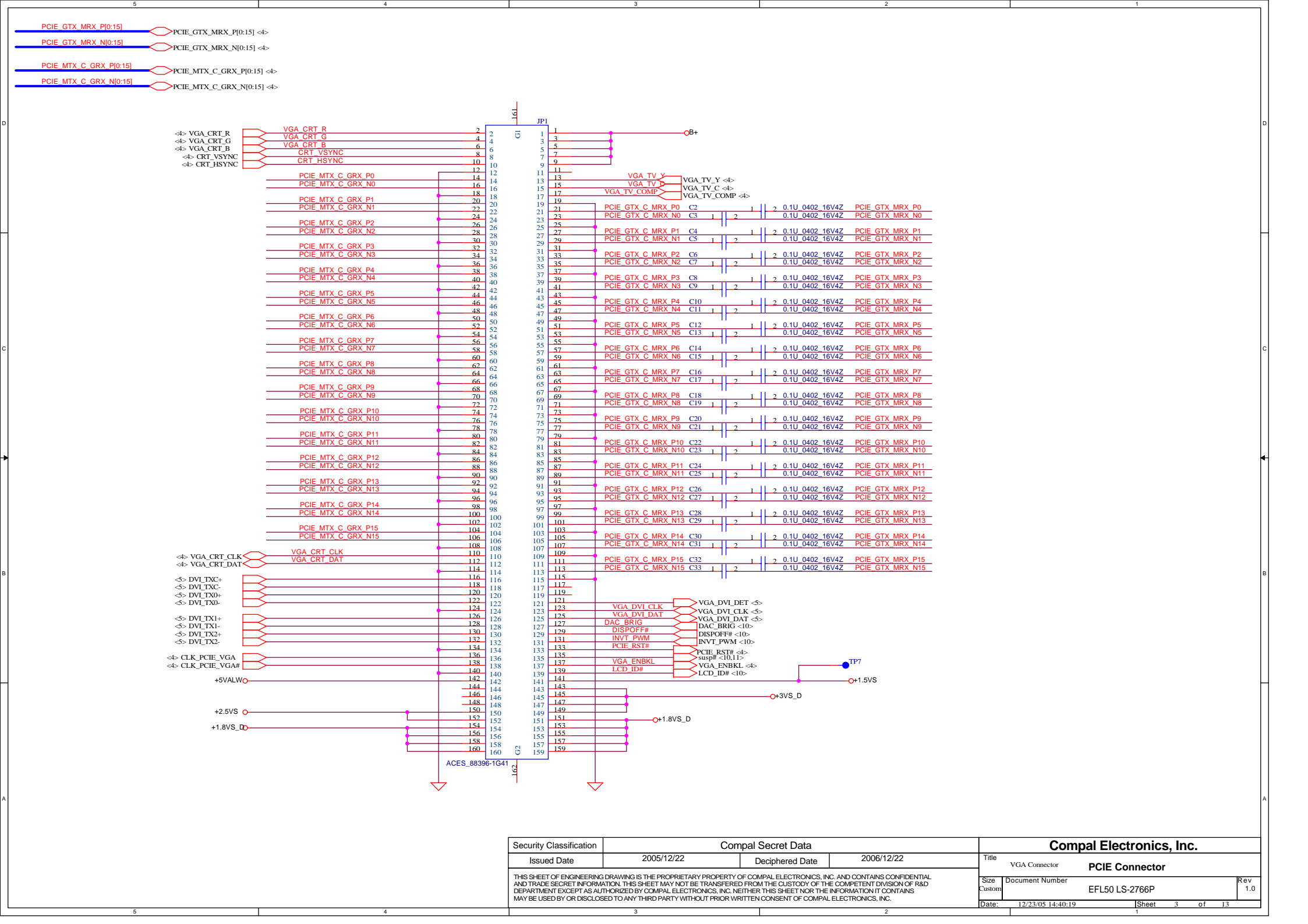
Revision 1.0

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				Date:	122305 14:40:19
				Sheet	1 of 13
				Rev	1.0

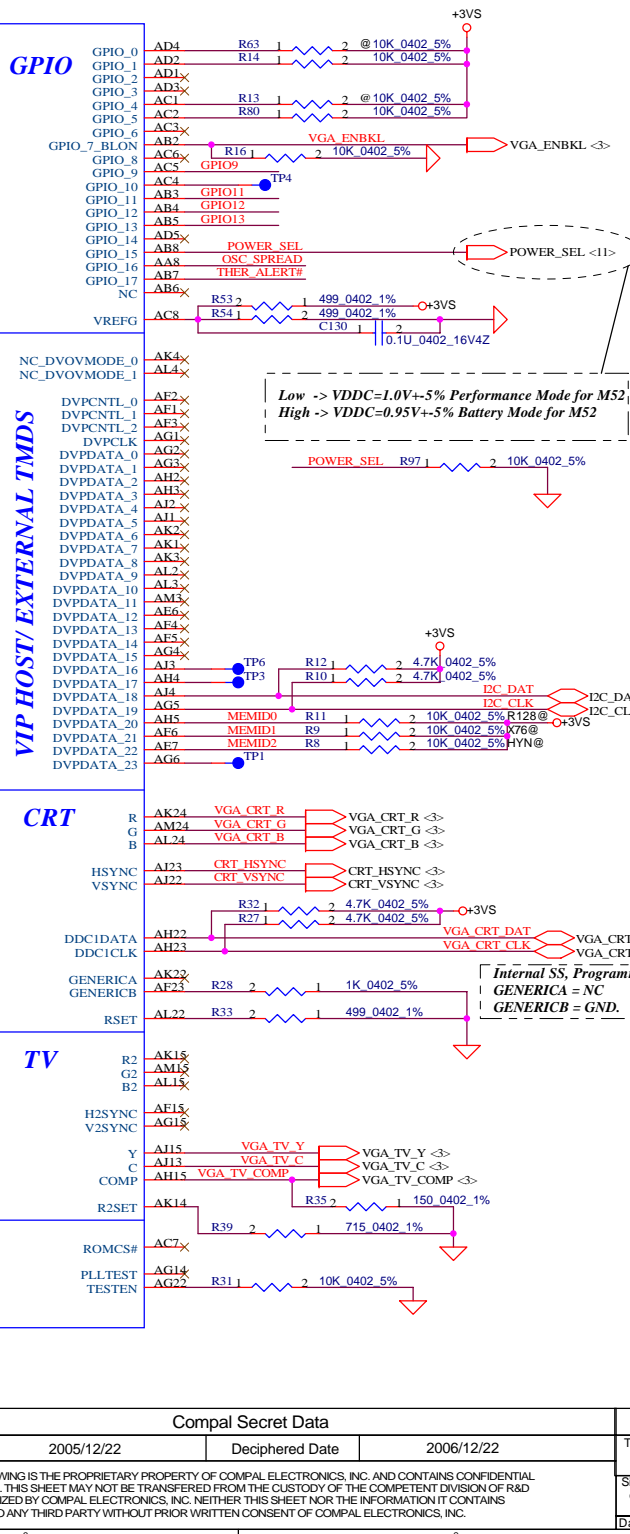
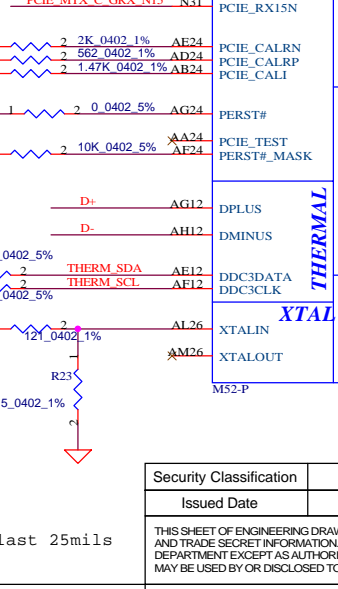
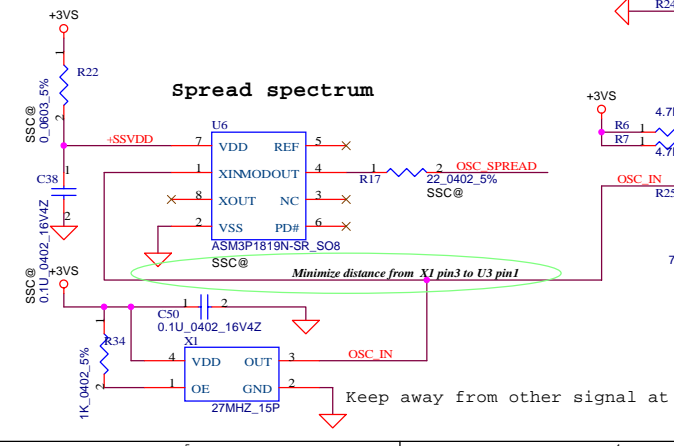
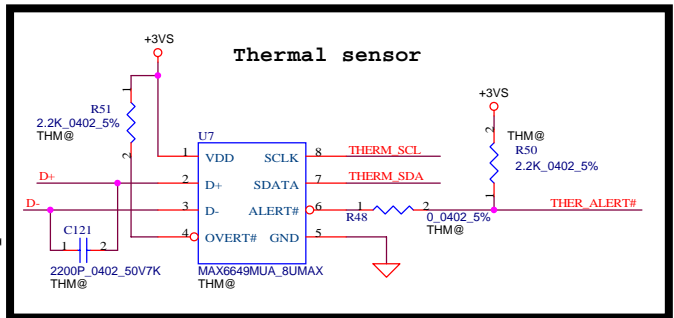
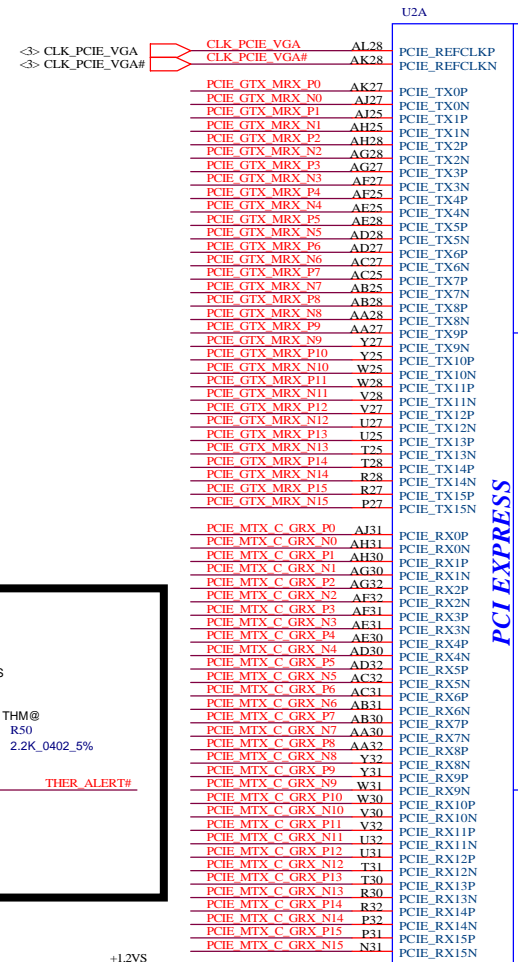
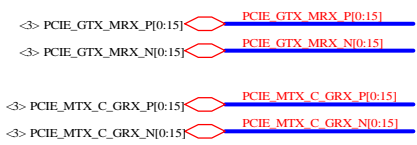
M54P/M52P BLOCK DIAGRAM



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Size	Document Number			Rev	
	EFL50 LS-2766P			1.0	
Date:	122305 14:40:19			Sheet 2 of 13	



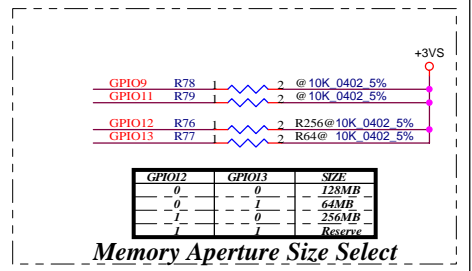
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Date:	12/23/05 14:40:19	Sheet	3 of 13	Rev	1.0



Straps: (Internal pull down)

Transmitter power saving enable	GPIO[0]	0: 50% TX output swing 1: Full TX output swing
Transmitter de-emphasis enable	GPIO[1]	0: TX de-emphasis disable 1: TX de-emphasis enable
Debug Access	GPIO[4]	0: OFF 1: ON
Current bias for the PCI Express PHY PLL	GPIO[5]	GPIO5 = 1 (must be pulled to 3.3V at reset using)
ROM ID Config	GPIO[9, 13:11]	GPIO[9]=1 External ROM Attached GPIO[9]=0 No External ROM For No External ROM: GPIO[13,12] is for MEM_AP_SIZE[1,0] GPIO[11] don't care
VIP_DEVICE	VSYNC	0: Slave VIP host device present 1: No slave VIP host device present

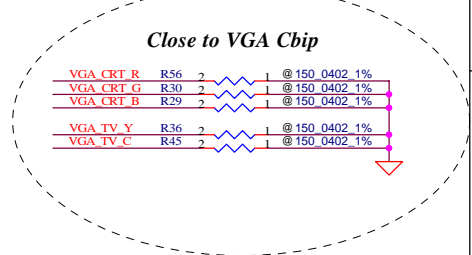
** The readback of this strap is the inverted with respect to the value on the pin*



For DDRII

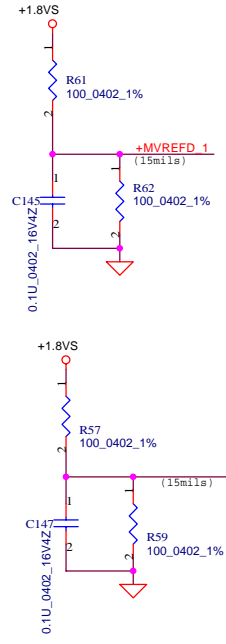
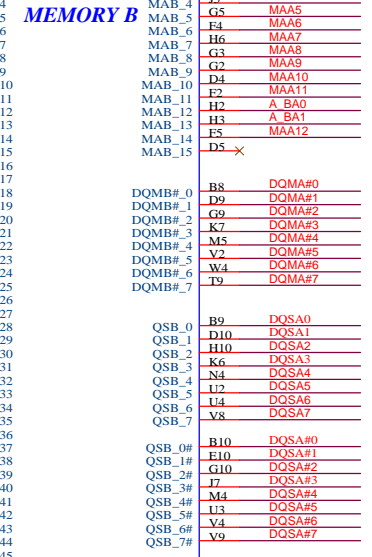
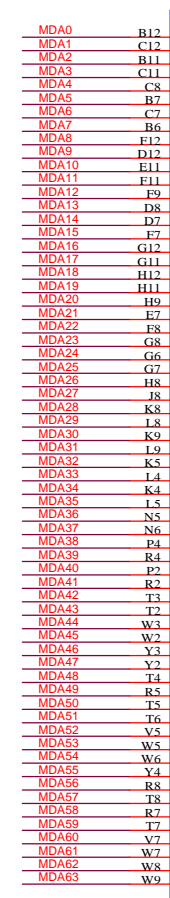
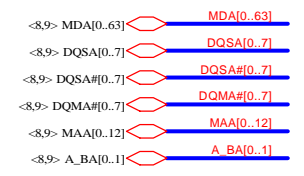
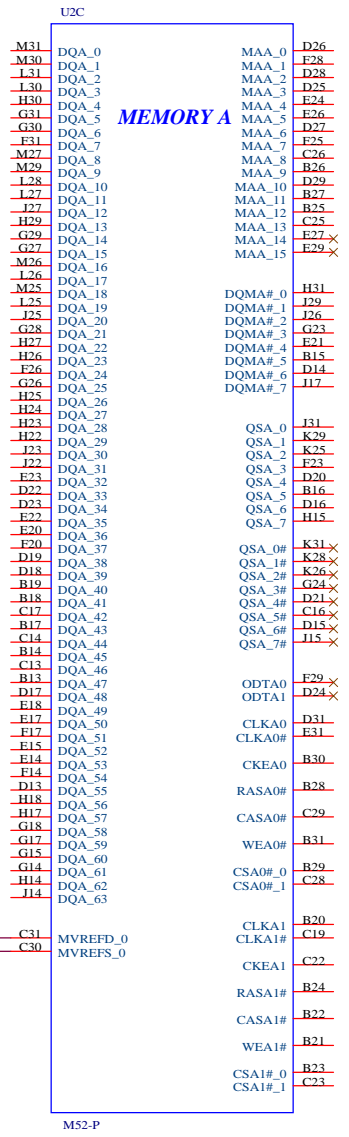
Vedio Memory Config. (VGA Internal PD)

MEMID[2:0]	Size	Size (Speed)	Vender	Chips
0 0 0	64MB	16M16 (300MHz)	Samsung	2
0 0 1	128MB	16M16 (300MHz)	Samsung	4
1 0 0	64MB	16M16 (300MHz)	Hynix	2
1 0 1	128MB	16M16 (300MHz)	Hynix	4

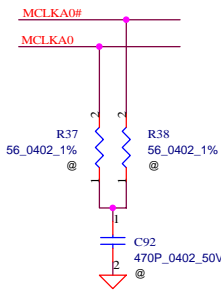


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Date:	122305 14:40:18	Sheet	4 of 13	Rev	1.0

GDDR2

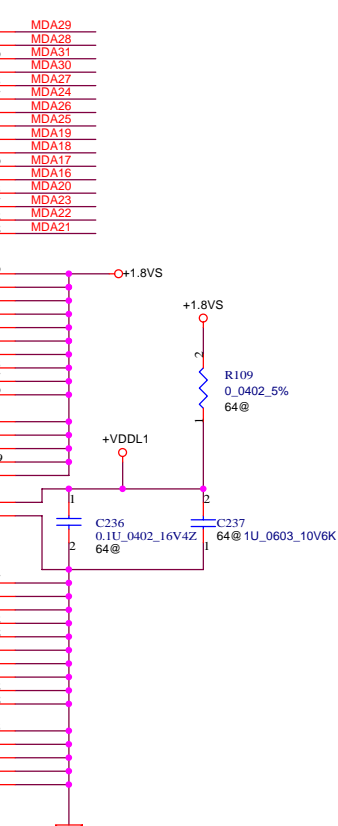
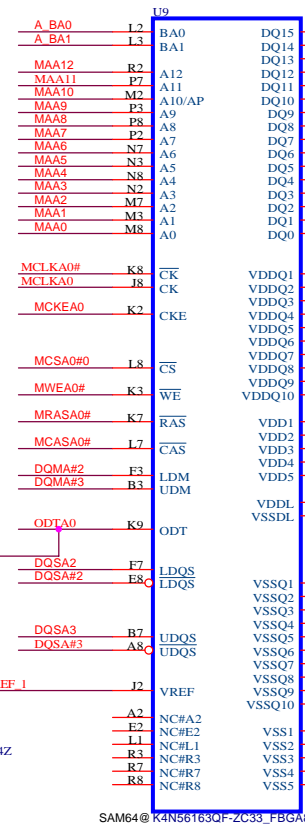
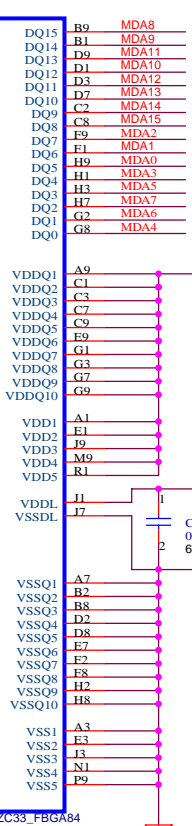
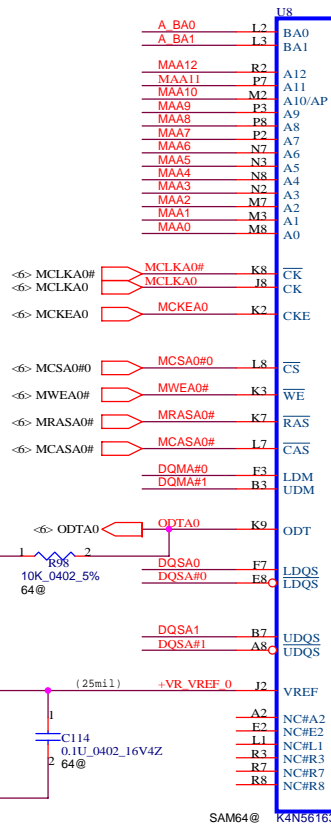


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				Document Number	1.0
				EFL50 LS-2766P	
Date:	122305 14:40:18	Sheet	6	of	13

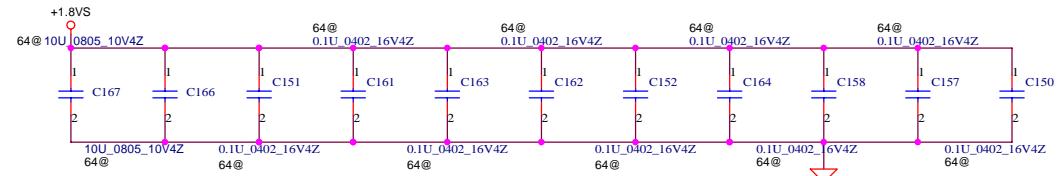
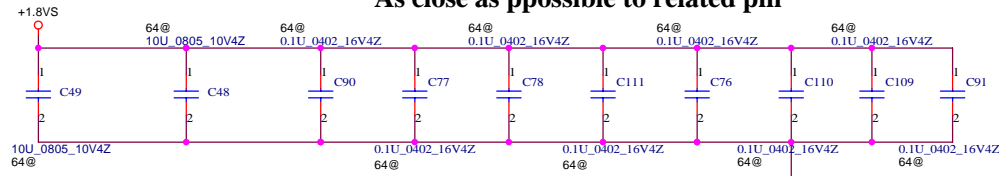


- <6.9> MDA[0..63] MDA[0..63]
- <6.9> DQSA[0..7] DQSA[0..7]
- <6.9> DQSA#[0..7] DQSA#[0..7]
- <6.9> DQMA[0..7] DQMA[0..7]
- <6.9> MAA[0..12] MAA[0..12]
- <6.9> A_BA[0..1] A_BA[0..1]

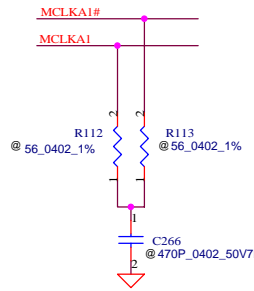
Default VRAM chip is SAM: SA00000YC00.



As close as possible to related pin

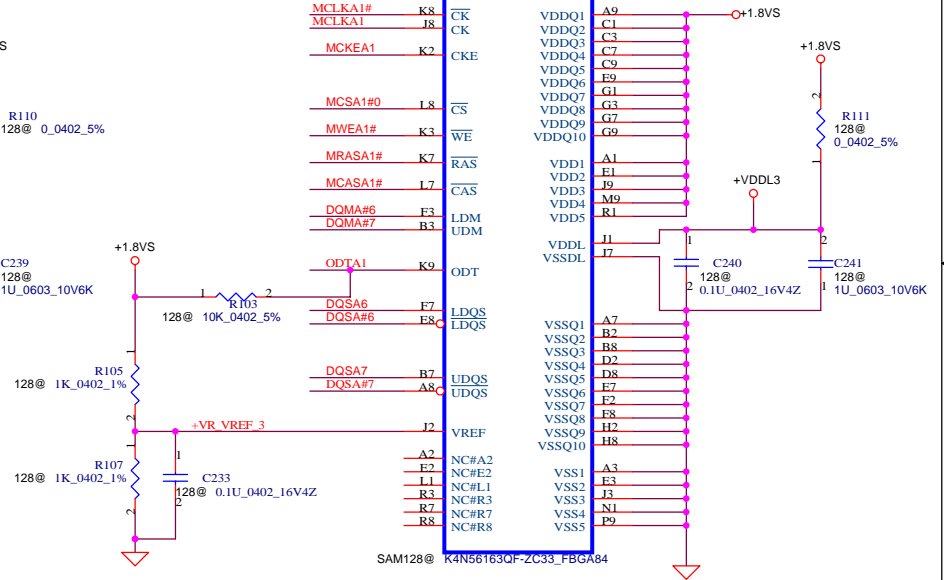
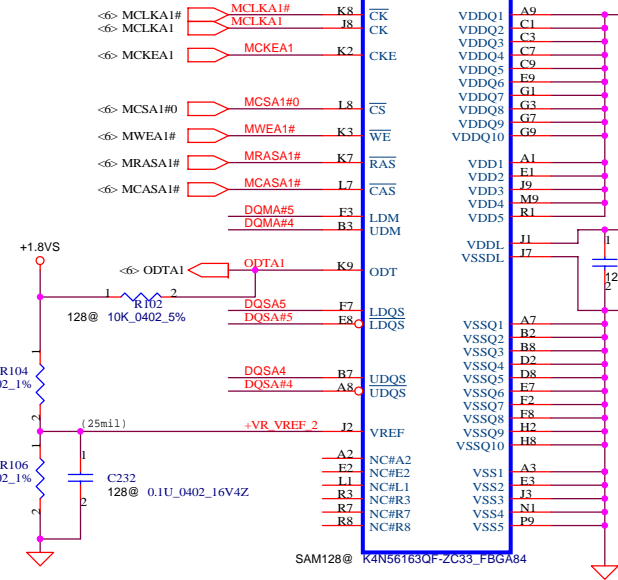
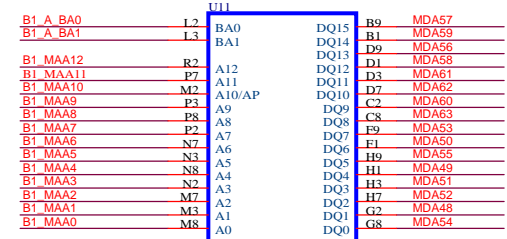
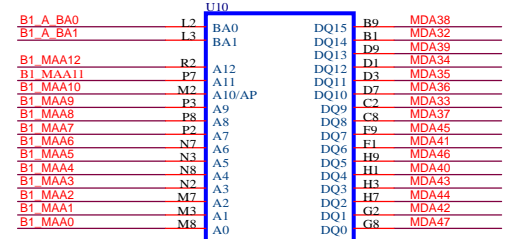
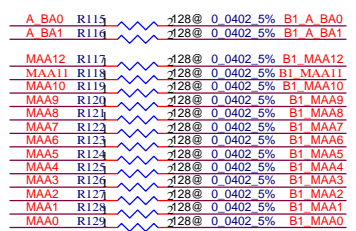


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Size	Document Number			Rev	1.0
Customer	EFL50 LS-2766P			Date:	122305 14:40:19
				Sheet	8 of 13

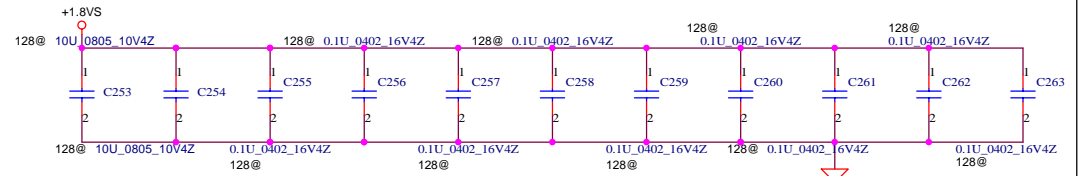
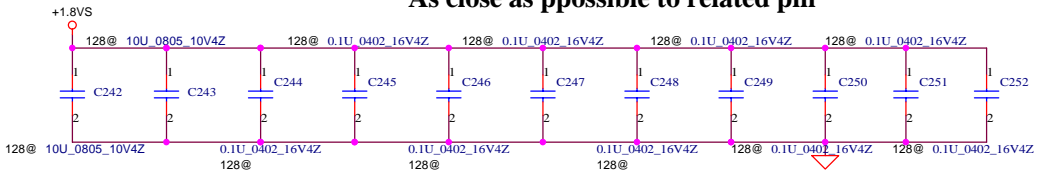


- <6,8> MDA[0..63] — MDA[0..63]
- <6,8> DQSA[0..7] — DQSA[0..7]
- <6,8> DQSA#[0..7] — DQSA#[0..7]
- <6,8> DQMA#[0..7] — DQMA#[0..7]
- <6,8> MAA[0..12] — MAA[0..12]
- <6,8> A_BA[0..1] — A_BA[0..1]

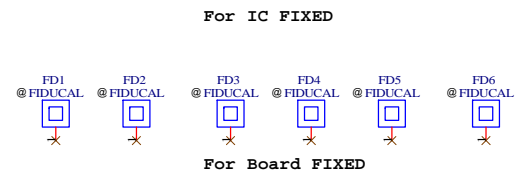
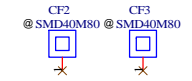
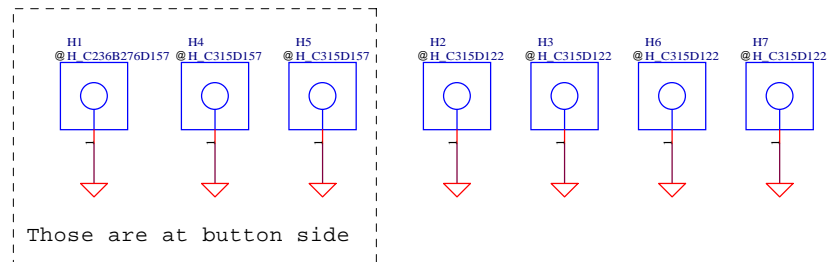
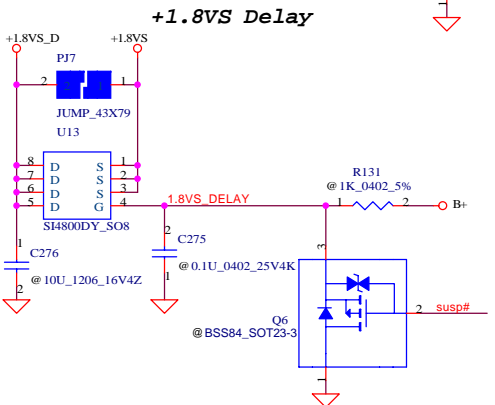
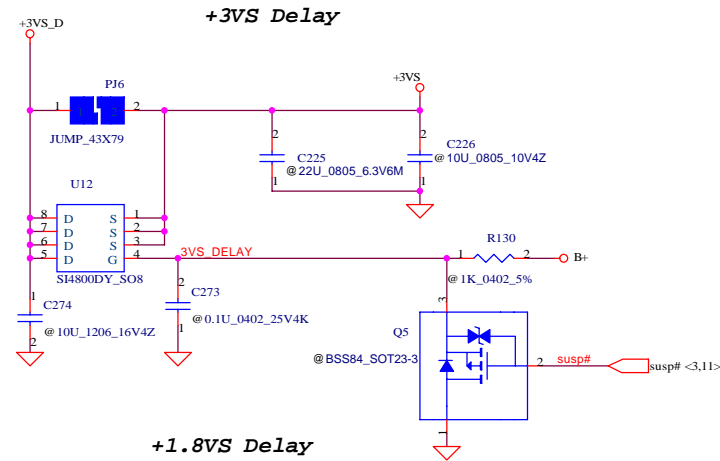
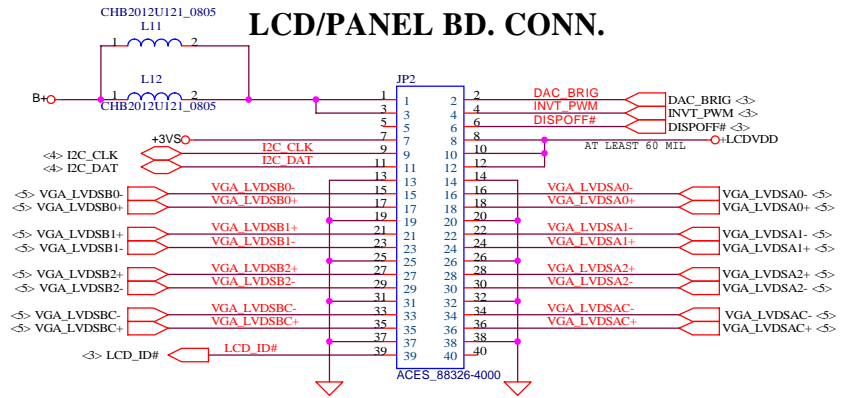
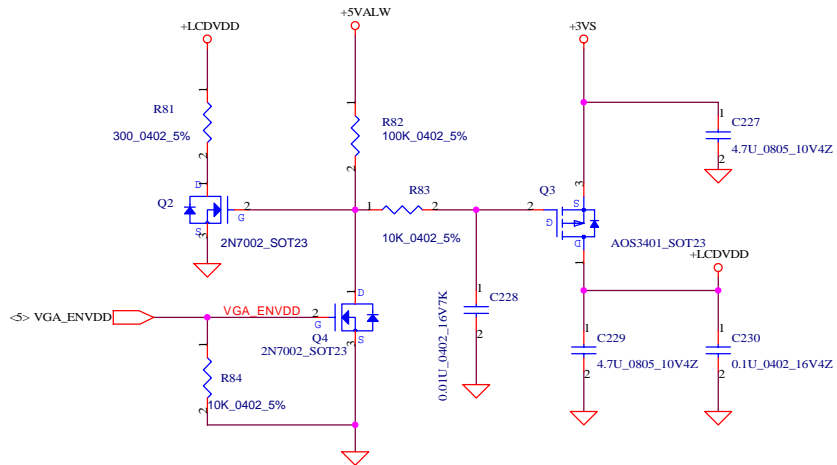
Default VRAM chip is SAM: SA00000YC00.



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Size	Document Number	Date:		Sheet	Rev
Custom	EFL50 LS-2766P	122305 14:40:19		9 of 13	1.0



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				EFL50 LS-2766P	Rev
				Date:	12/23/05 14:40:19
				Sheet	10 of 13

Version change list (P.I.R. List)

===== 2005/12 R0.2 =====

- 01. Reserve +3VS and +1.8VS delay circuit and reserve Jump. == To meet ATI PWR sequence.
Reserve PJ6, PJ7, U12, U13, C273, C274, C275, C276,
Q5, Q6, R130 and R131.
- 02. Change C42, C45, C46, C47 and C51, from 0.1U to 1U. == For 3D hang issue.
- 03. Change C101, from 0.1U to 1U. == For 3D hang issue.
- 04. Add C44 as 330U == For 3D hang issue.
- 05. Delete R63, 10K_0402_5% == PCIE TX power saving.

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				Custom	EFL50 LS-2766P
Date:	122305 14:40:19	Sheet	12	of	13

ZZZ
 DA800005F10
 --PCB ZKD LS-2766P
 REV1 VGA/B

DA800005F10

U8
 SA00000JW00
 --S IC D2 16M16/600
 HY5PS561621AFP-33
 FBGA

HYN64@ SA00000JW00

U9
 SA00000JW00
 --S IC D2 16M16/600
 HY5PS561621AFP-33
 FBGA

HYN64@ SA00000JW00

U10
 SA00000JW00
 --S IC D2 16M16/600
 HY5PS561621AFP-33
 FBGA

HYN128@ SA00000JW00

U11
 SA00000JW00
 --S IC D2 16M16/600
 HY5PS561621AFP-33
 FBGA

HYN128@ SA00000JW00

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