

# ACER\_SJM31

## MAIN BOARD

2009.05.04

DATE	CHANGE NO.	REV
Monday, May 04, 2009	2009.ECO-006289	A

DRAWER	EE	DATE	POWER	DATE	TITLE
DESIGN					ACER SJM31
CHECK RESPONSIBLE					
SIZE:				VER:	SIZE CODE DOC NUMBER REV
FILE NAME: XXXXXXXXXXXXX					C CS D-CS-1310A22753-0-ALG B
PIN XXXXXXXXXXXXX					SHEET 1 of 38

# 1. Schematic Page Description :

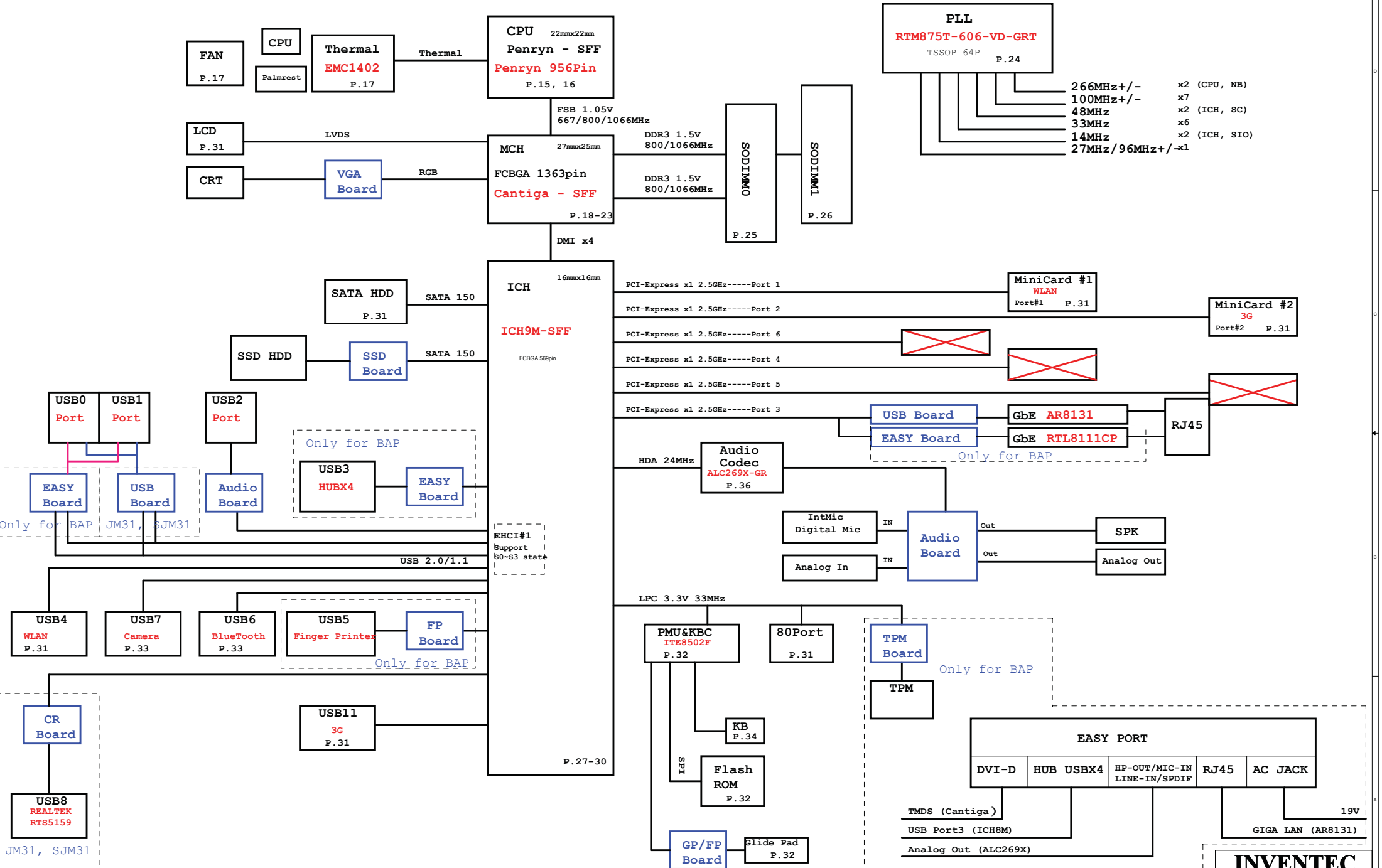
## Montevina Schematic Ver : A02

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- 10. 3VS/5VS/1.5V (DDR3)
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- 13. CPU Core Power
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- 20. Cantiga DDRII(3/6)
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- 23. Cantiga Ground(6/6)
- 24. Clock Generator
- 25. DDR3 SDRAM SO-DIMM0
- 26. DDR3 SDRAM SO-DIMM1
- 27. ICH9M CPU/IDE/SATA(1/4)
- 28. ICH9M PCI/PCIE/DMI/USB(2/4)
- 29. ICH9M GPIO(3/4)
- 30. ICH9M Power/GND(4/4)
- 31. LCD CNN/SATA/3G/WLAN
- 32. KBC ITE8512F
- 33. IO CN 1/3
- 34. IO CN 2/3
- 35. IO CN 3/3
- 36. Audio Codec

<b>INVENTEC</b>			
TITLE <b>SJM31 (Penryn+Cantiga+ICH9M)SFF</b>			
Schematic Page			
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# 3. Block Diagram :

<http://hobi-elektronika.net>



PLL  
RTM875T-606-VD-GRT  
TSSOP 64P P.24

- 266MHz+/- x2 (CPU, NB)
- 100MHz+/- x7
- 48MHz x2 (ICH, SC)
- 33MHz x6
- 14MHz x2 (ICH, SIO)
- 27MHz/96MHz+/-x1

<b>INVENTEC</b>			
TITLE SJM31(Penryn+Cantiga+ICH9M)SFF Block Diagram			
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# 4. Net name Description :

<http://hobi-elektronika.net>

## Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
-----	
VCC CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI/PCIE/DDRIII DLLs for GMCH/Core/PCIE for ICH9m by SLP_S3#_3R
-----	
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

## Part Naming Conventions









- C = Capacitor
- CN = Connector
- D = Diode
- F = Fuse
- L = Inductor
- Q = Transistor
- R = Resistor
- RP = Resistor Pack
- U = Arbitrary Logic Device
- Y = Crystal and Osc

## Net Name Suffix

- # = Active Low signal

# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TVDAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLF Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

**INVENTEC**

TITLE: **SJM31(Penryn+Cantiga+ICH9M)SFF**

ANNOTATIONS

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22782-0-ALG	8
SHEET			8

# 6.Schematic modify Item and History :

- 2009.0108
1. ADD USB P3 for Docking, USB P5 for Finger printer,  
Modify CN5 -----P28
  2. Modify CN20 to 50pin-----P33
  3. Move PWR\_SWIN# from CN14 to CN20
  4. ADD TPM module-----P34

- 2009.0109
1. ADD DOCK\_USB\_EN, DOCK\_CRT\_IN#-----P32,33

- 2009.0112
1. Change power item: R490,R291,BAT CNN TH PIN

## AX1 to A01 change list

1. Change AD\_ON circiut for Green adaptor PC. (Page 12)
2. Change thermal shut down control by PM\_ICH\_PWROK from ALL\_SYSPWRGD. (Page 17)
3. Add PCIE I/F to 3G mini card connector for support EM772 (Page24, Page28, Page31)

## A01 to A02 change list (JM31 A02, SJM31 A01)

1. Add EC\_3VLA soft start circuit --- Change R480 to NU, Add Q28, R378,R738,C374,R299,Q118,R739,C376 (Page 9)
2. Add 3VA porotect diode --- Add D35 (Page 9)
3. For green adaptor --- Change C419 from 0.1uf to 4.7uF , Add Q120, R744,R742,R743 (Page 8, 12)
4. For power consumption --- Change Q37,Q50,Q51 from 6015B0090401 to 6015B0082201, Change Q54,Q38,Q48 from 6015B0086301 to 6015B0089301.(Page 8, 10, 11)
5. Change R29,R30,R31,R32,R33,R34,R35 from 0 Ohm to short pad. (Page 13)
6. For safty ---- Change R231 from 0 Ohm to 330 Ohm, R226 from 665 Ohm to 330 Ohm. (Page 27)
- 7.For 3G leakage ---- Delete R220,R211 (Page 29)
8. Delete reverse HW timing circuit. ---- Delete U7,D13,R237,C376,U9,U8,D9,R222,C327 (Page 29, 32)

## A02 for SJM31 change list

1. R513 change to 470 for SJM31 TP lock LED

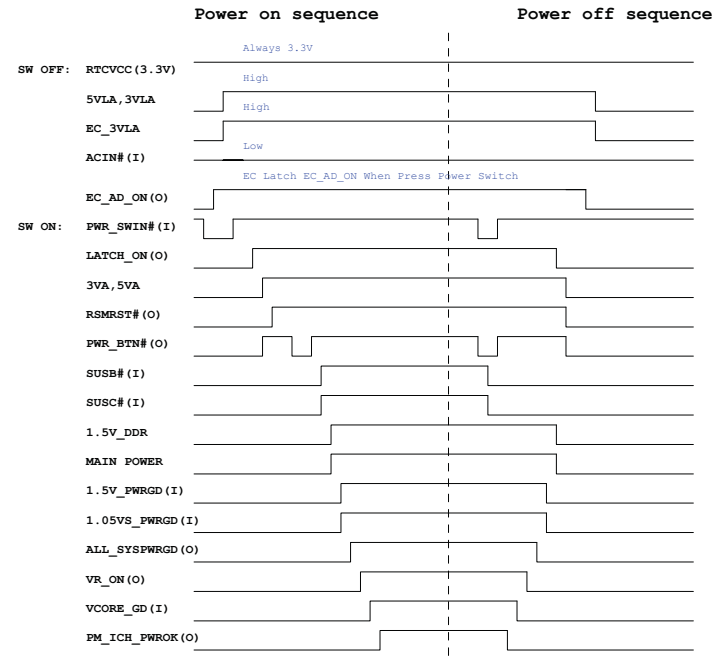
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TITLE <b>SJM31(Penryn+Cantiga+ICH9M)SFF</b>			
Schematic Modify			
SIZE Custom	CODE CS	DOC NUMBER D-CS-1310A22782-0-ALG	REV 8
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# SYSTEM POWER ON/OFF SEQUENCE

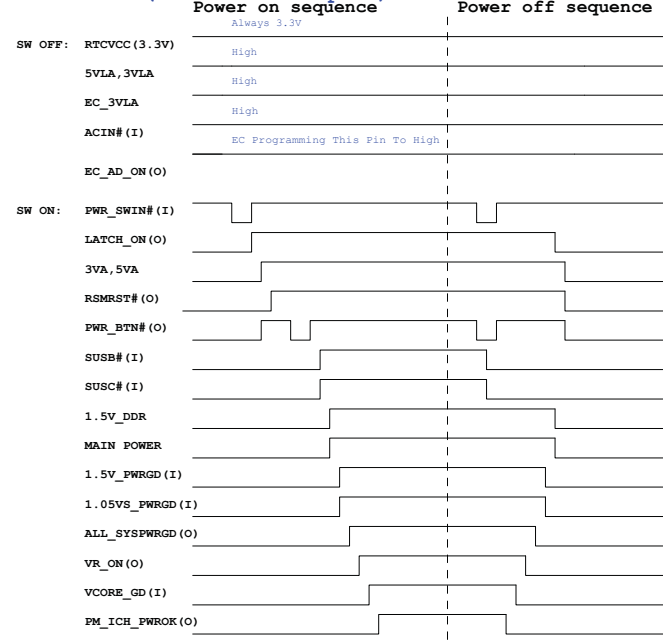
<http://hobi-elektronika.net>

Drawing : Wendy, Huang

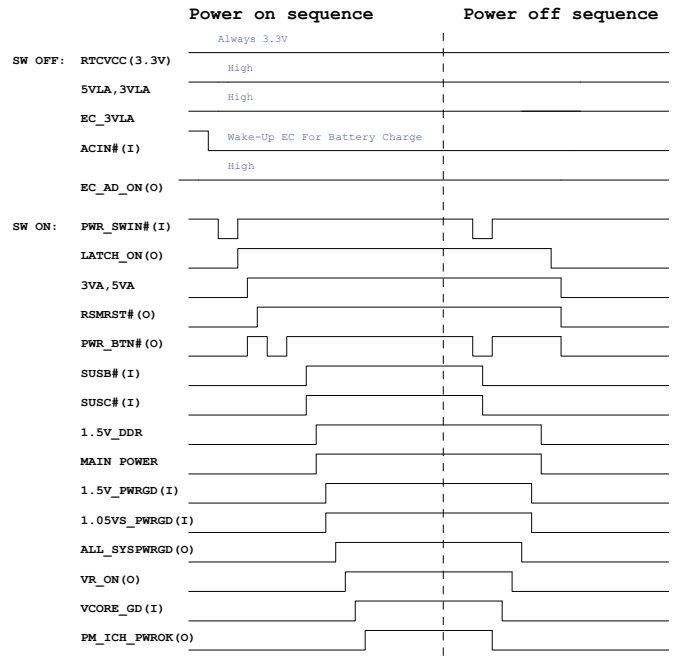
## Power on/off sequence AC insert (without Battery Pack)



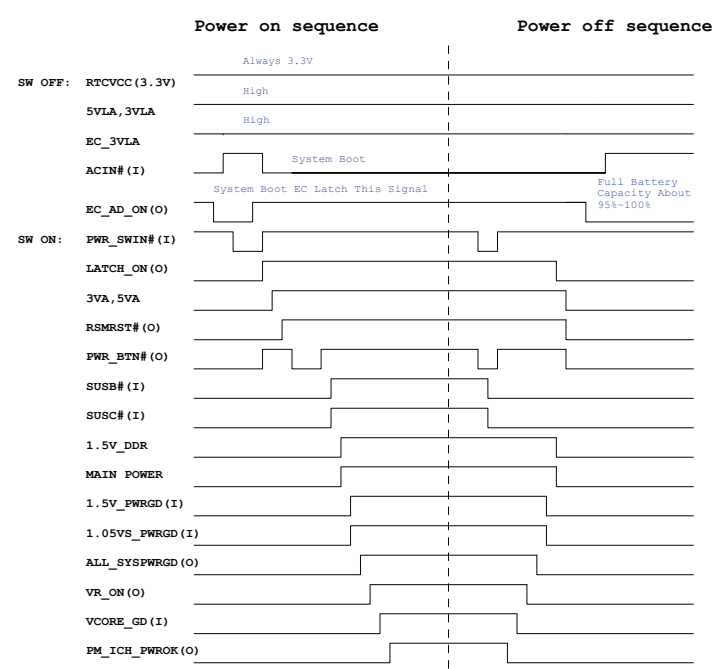
## Power on/off sequence Battery insert (without AC adapter)



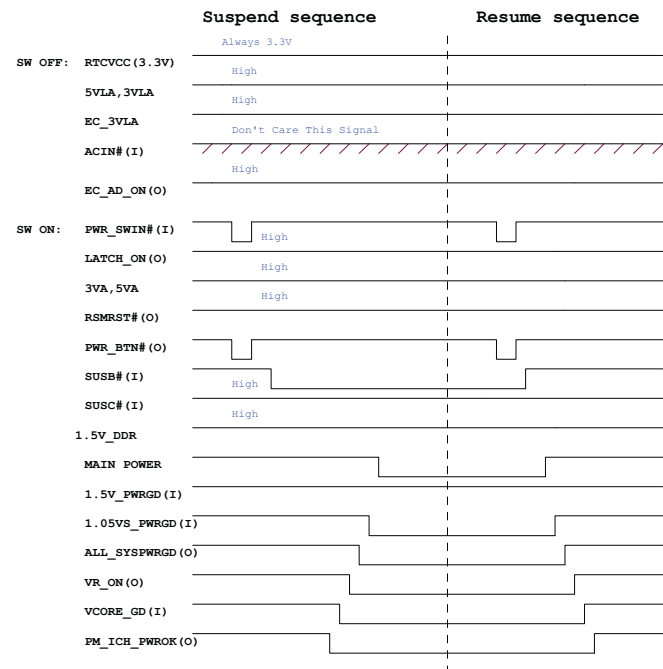
## Power on/off sequence AC insert (with charge over 95%)



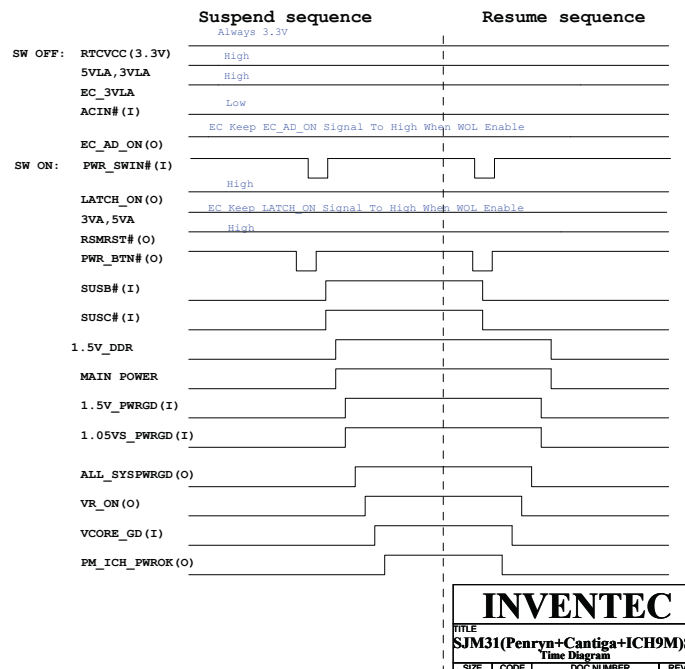
## Power on/off sequence AC insert (without charge over 95%)



## Suspend And Resume Sequence (S3)



## Power on/off sequence after windows shutdown (WOL enable)



**INVENTEC**

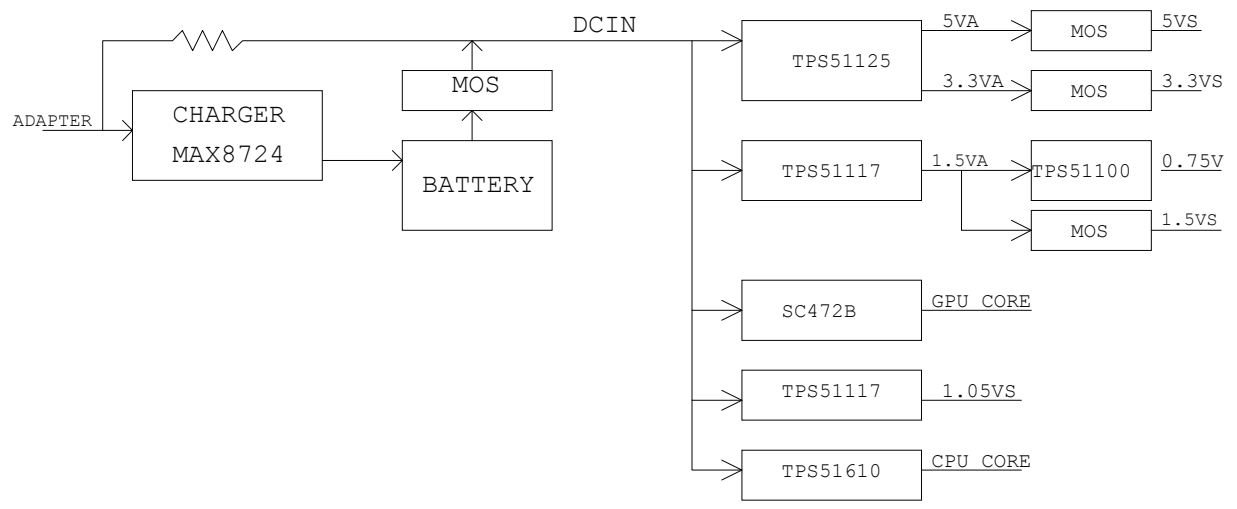
TITLE: SJM31(Penryn+Cantiga+ICH9M)S1P  
Time Diagram

SIZE: Custom	CODE: CS	DOC-NUMBER: D-CS-1310A2752-0-ALG	REV: B
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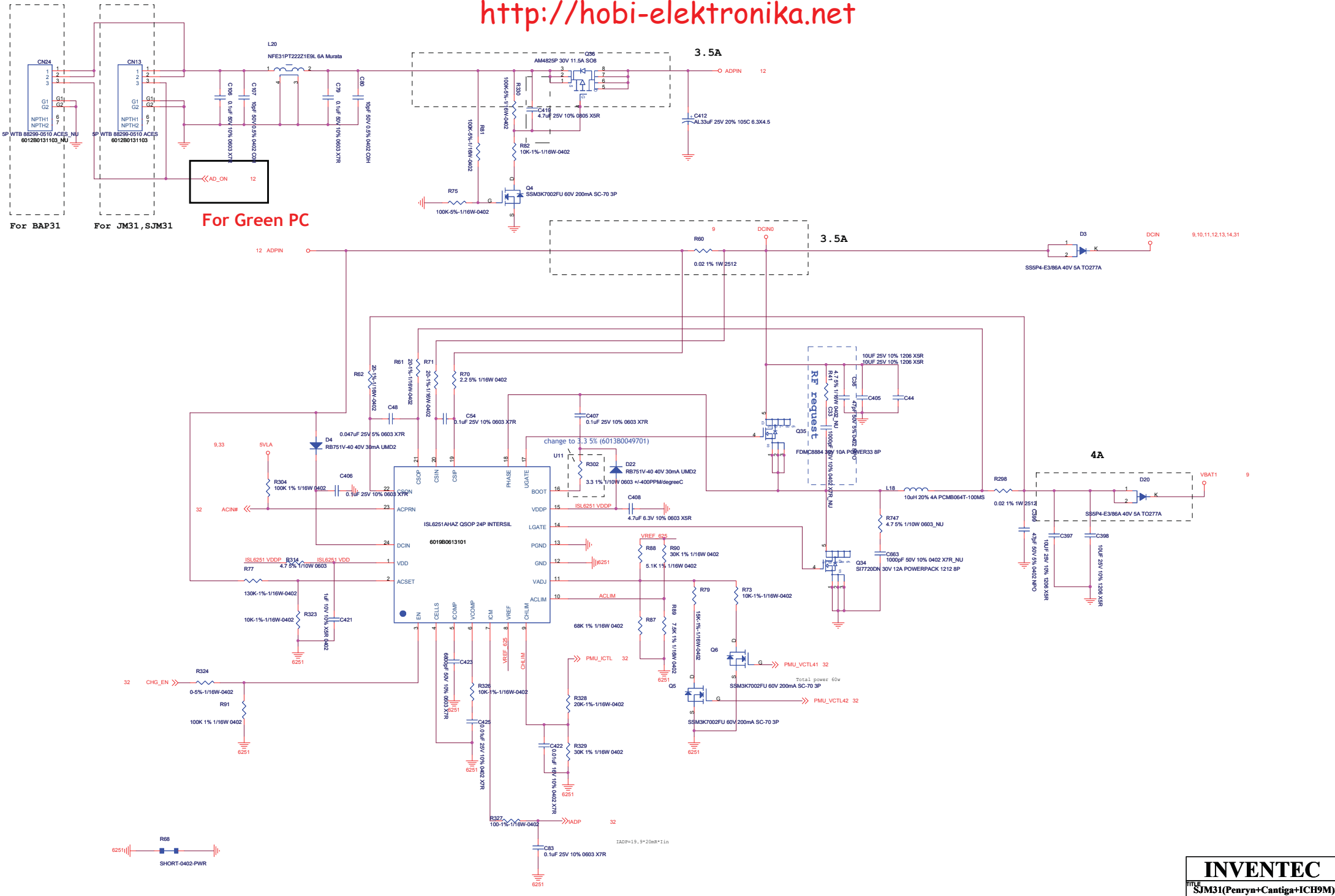
CHANGE by: Miles Liu | DATE: Monday, May 04, 2009 | SHEET: 6 of 36

# Power Block Diagram :

<http://hobi-elektronika.net>



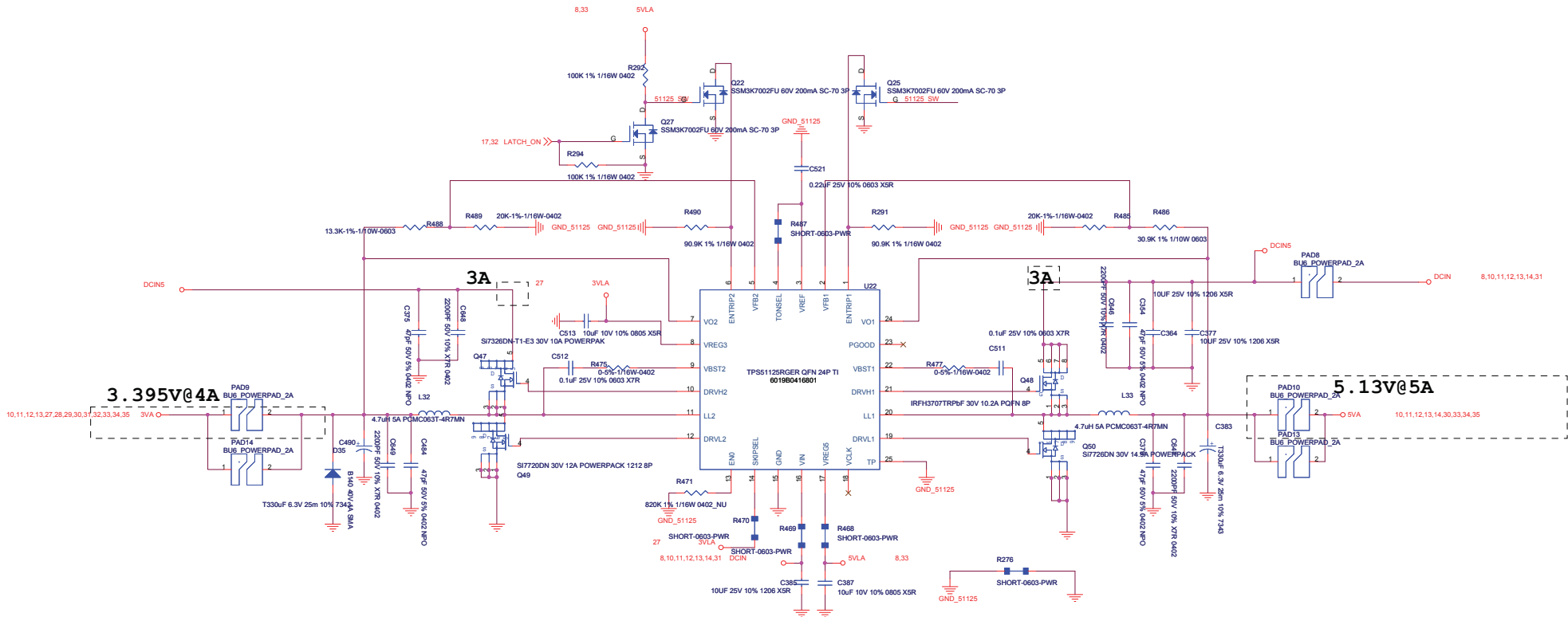
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TITLE: <b>SJM31(Penryn+Cantiga+ICH9M)SFF</b>			
Power Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	D-CS-1310A22782-0-ALG	B
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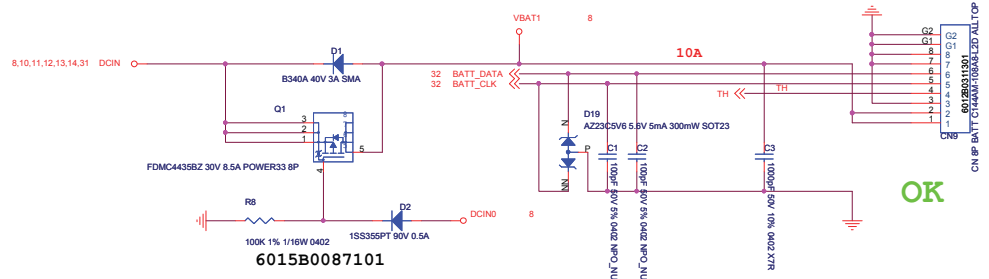
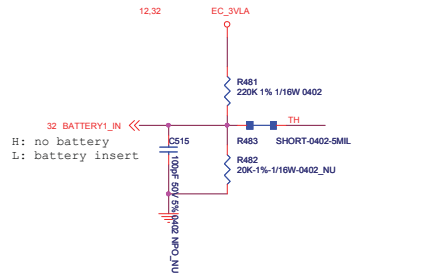
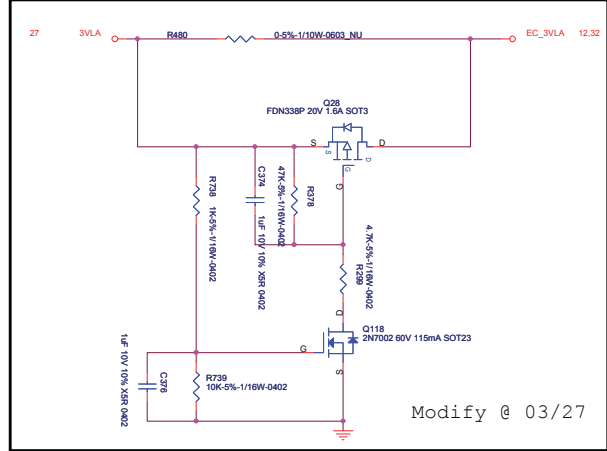
For BAP31      For JM31, SJM31      **For Green PC**

<b>INVENTEC</b>			
TITLE: <b>SJM31(Penryn+Cantiga+ICH9M)SFF</b>			
Adaptor In / Charge			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B
CHANGE by Miles Liu		DATE Monday, May 04, 2009	SHEET 8 of 38

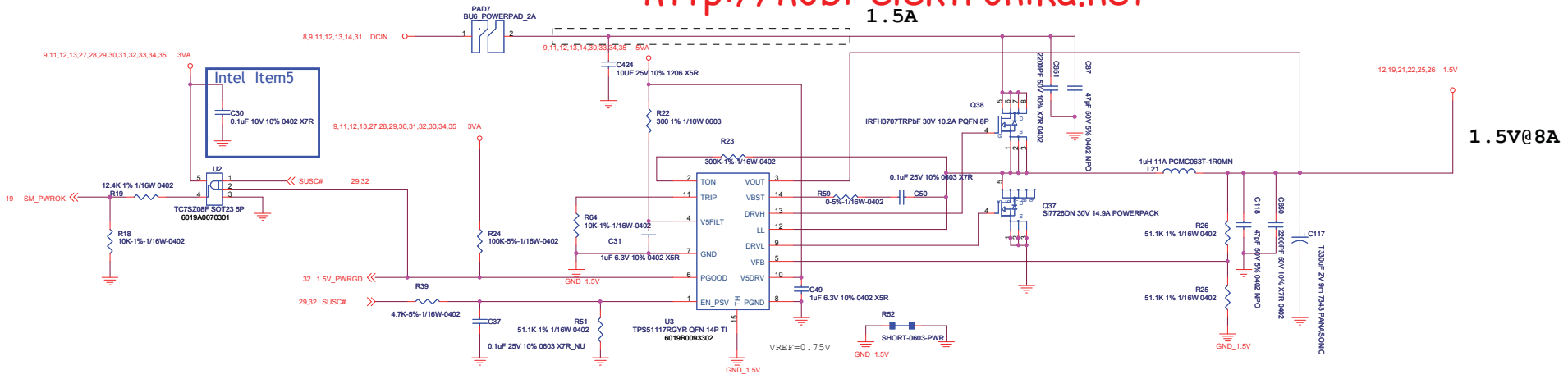




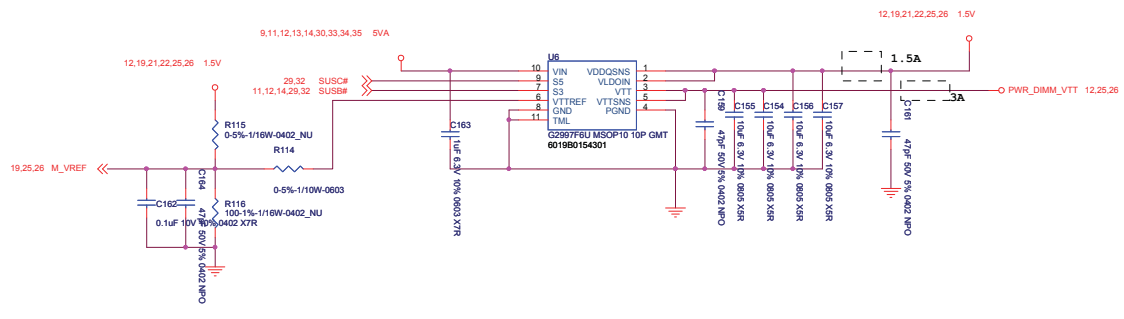
For Green PC



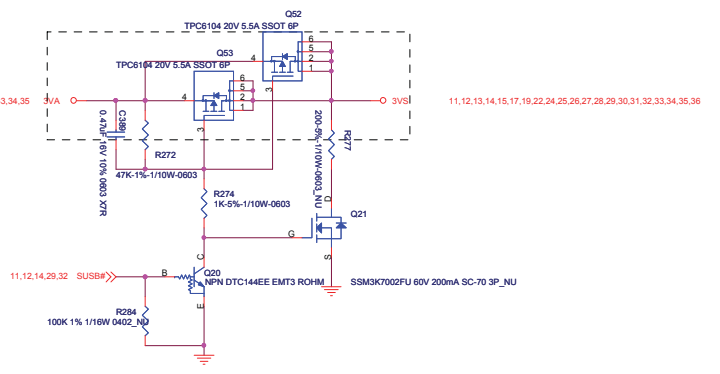
1.5A



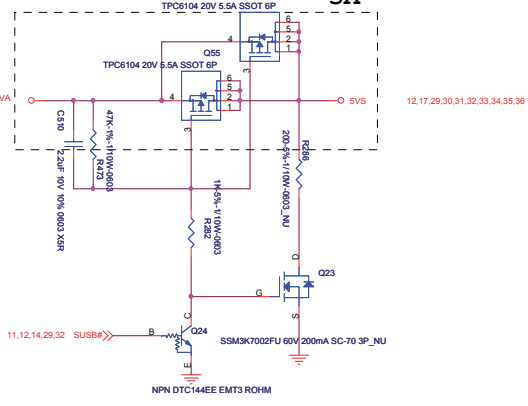
1.5V@8A



5A



5A

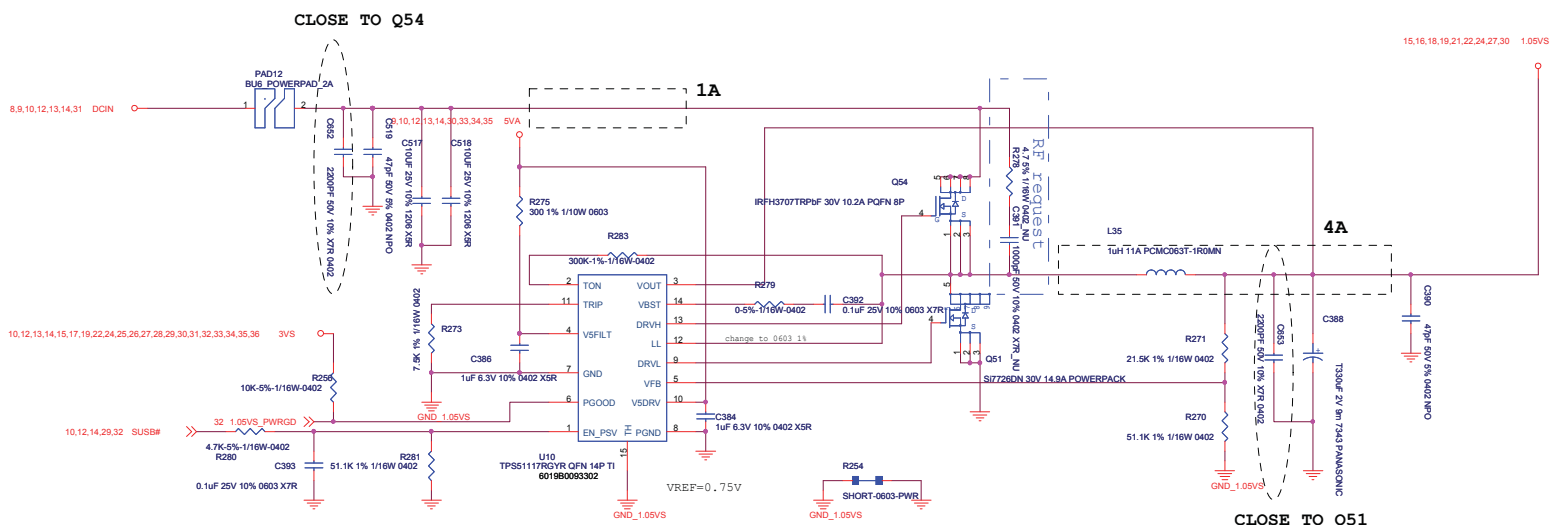
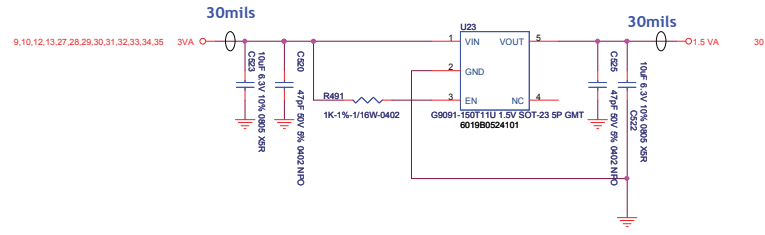
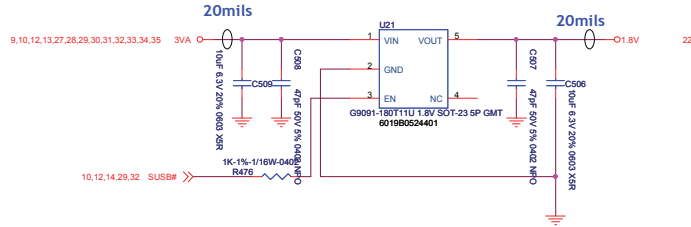


INVENTEC

SJM31(Penryn+Cantiga+ICH9M)SFF

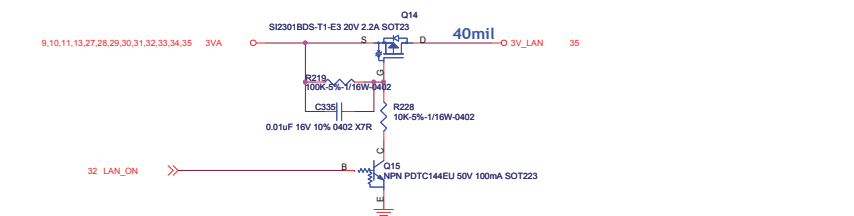
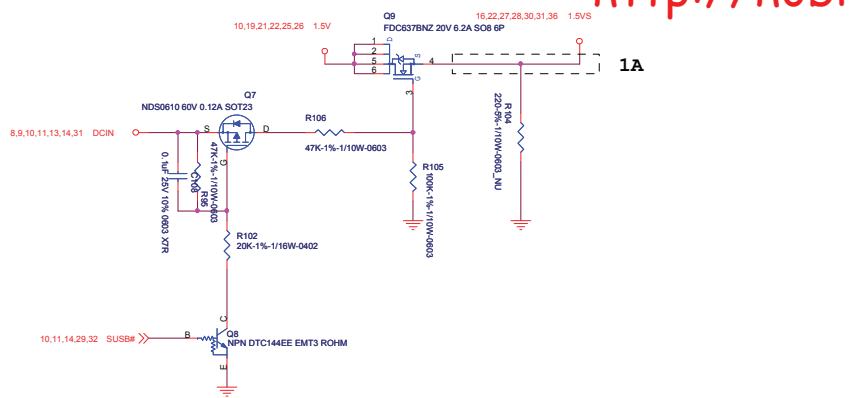
3VS/5V/1.5V (DDR3)

SIZE CODE DOC NUMBER REV  
Custom CS D-CS-1310A22752-0-ALG B



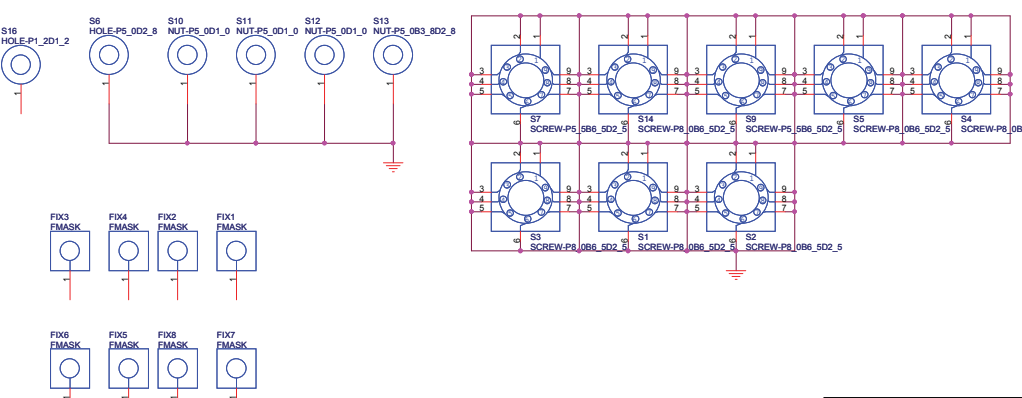
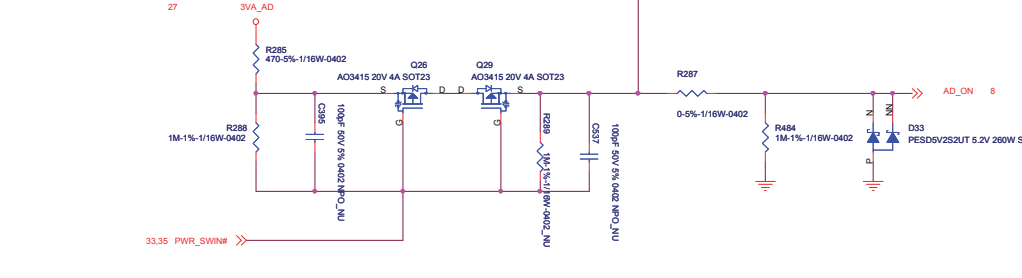
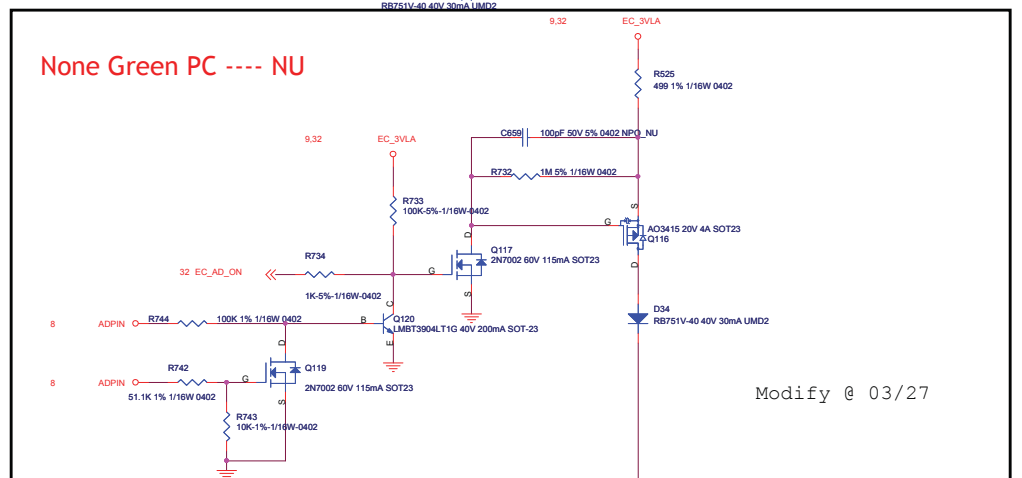
<b>INVENTEC</b>			
TITLE: <b>SJM31(Penryn+Cantiga+ICH9M)SFF</b>			
1.05VS/1.5S/1.5V/1.5VA			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B
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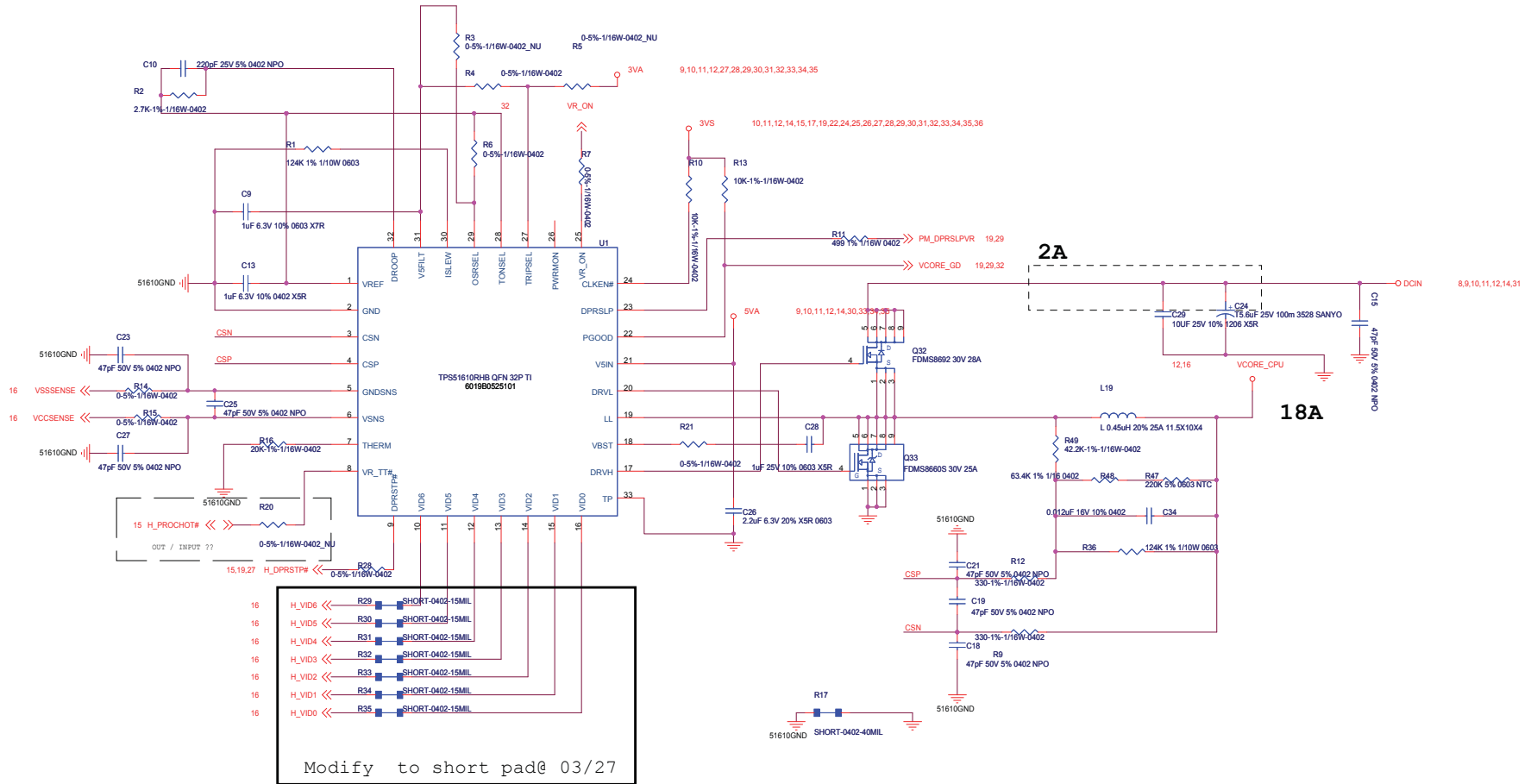
1.5VS

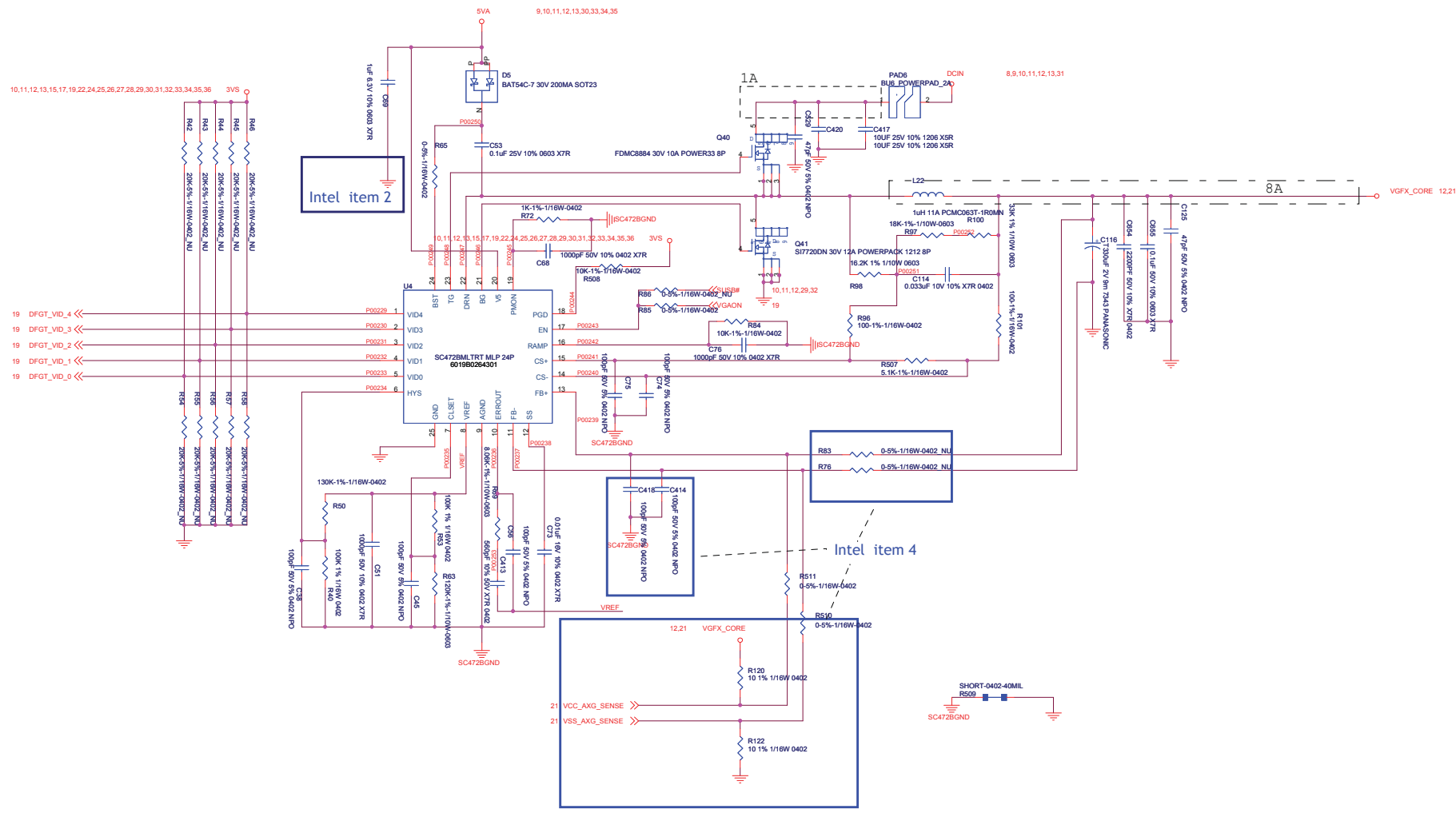


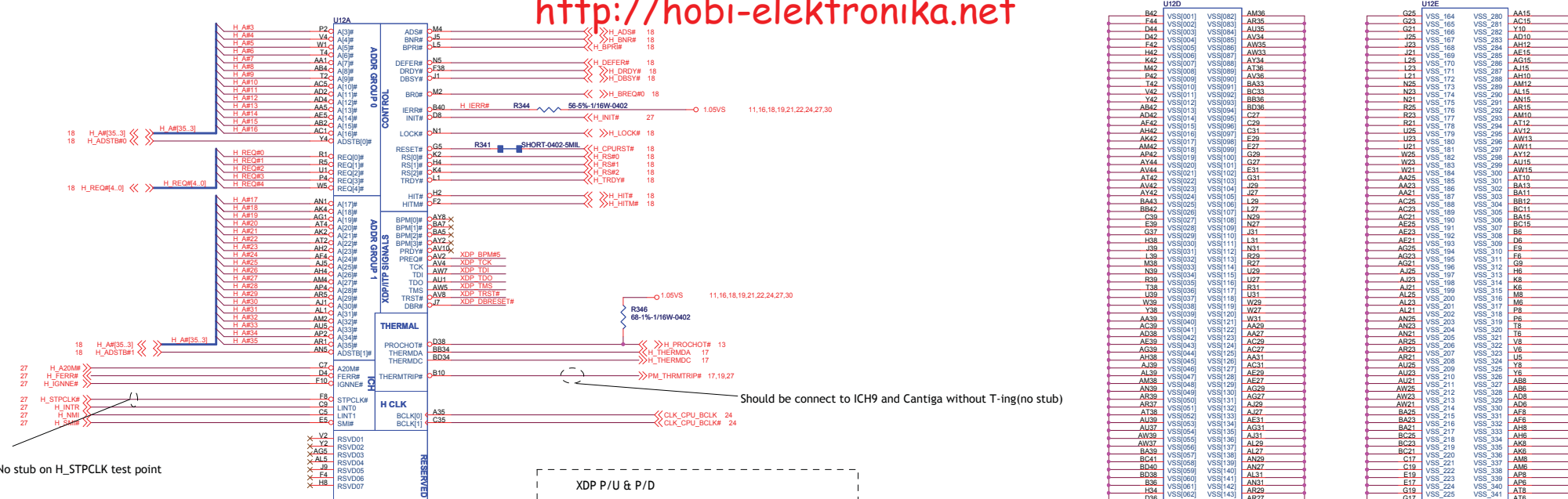
EMI Cap

Pin	Value	Part	Value	Part	Value	Part	Value	Part
10,19,21,22,25,28	1.5V	C300	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31	DCIN	C14	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31
		C14	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31	DCIN	C16	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31
		C16	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31	DCIN	C7	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31
		C7	0.1uF 25V -20%+80% 0402 Y5V	8,9,10,11,13,14,31	DCIN	C4	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
		C4	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36	3VS	C5	0.1uF 10V 10% 0402 X7R	9,10,11,13,27,28,29,30,31,32,33,34,35
		C5	0.1uF 10V 10% 0402 X7R	9,10,11,13,27,28,29,30,31,32,33,34,35	3VA	C150	0.1uF 10V 10% 0402 X7R	14,21 VGFX_CORE
		C150	0.1uF 10V 10% 0402 X7R	14,21 VGFX_CORE		C8	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
		C8	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36	3VS	C303	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
		C303	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36	3VS	C329	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
		C329	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36	3VS	C433	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35
		C433	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35	3VS	C474	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
		C474	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36	3VS	C505	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
		C505	0.1uF 10V 10% 0402 X7R	10,11,13,14,15,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36	3VS	C372	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35
		C372	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35	3VA	C196	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35
		C196	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35	3VA	C52	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35
		C52	0.1uF 10V 10% 0402 X7R	9,10,11,13,14,30,33,34,35	3VA	C132	0.1uF 10V 10% 0402 X7R	10,25,26 PWR_DIMM_VTT
		C132	0.1uF 10V 10% 0402 X7R	10,25,26 PWR_DIMM_VTT		C147	0.1uF 10V 10% 0402 X7R	10,25,26 PWR_DIMM_VTT
		C147	0.1uF 10V 10% 0402 X7R	10,25,26 PWR_DIMM_VTT		C153	0.1uF 10V 10% 0402 X7R	16,22,27,28,30,31,36 1.5VS
		C153	0.1uF 10V 10% 0402 X7R	16,22,27,28,30,31,36 1.5VS		C467	0.1uF 10V 10% 0402 X7R	16,22,27,28,30,31,36 1.5VS
		C467	0.1uF 10V 10% 0402 X7R	16,22,27,28,30,31,36 1.5VS		C92	0.1uF 10V 10% 0402 X7R	16 1.05VS_CPU
		C92	0.1uF 10V 10% 0402 X7R	16 1.05VS_CPU		C143	0.1uF 10V 10% 0402 X7R	16 1.05VS_CPU
		C143	0.1uF 10V 10% 0402 X7R	16 1.05VS_CPU		C71	0.1uF 10V 10% 0402 X7R	13,16 VCORE_CPU
		C71	0.1uF 10V 10% 0402 X7R	13,16 VCORE_CPU		C404	0.1uF 10V 10% 0402 X7R	13,16 VCORE_CPU
		C404	0.1uF 10V 10% 0402 X7R	13,16 VCORE_CPU		C178	0.1uF 10V 10% 0402 X7R	14,21 VGFX_CORE
		C178	0.1uF 10V 10% 0402 X7R	14,21 VGFX_CORE				



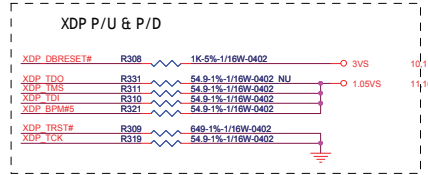






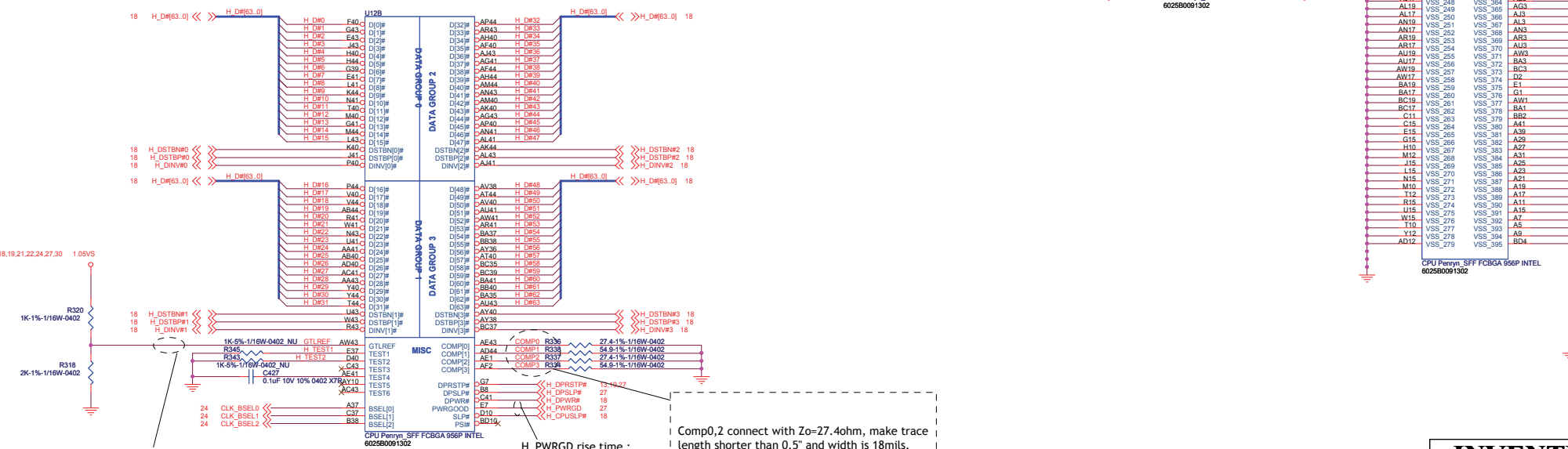
No stub on H\_STPCLK test point

Should be connect to ICH9 and Cantiga without T-ing (no stub)



Rout to TP via and place gnd via w/in 100mils

A# [32-39], APM# [0-1]: Leave escape routing on for future functionality



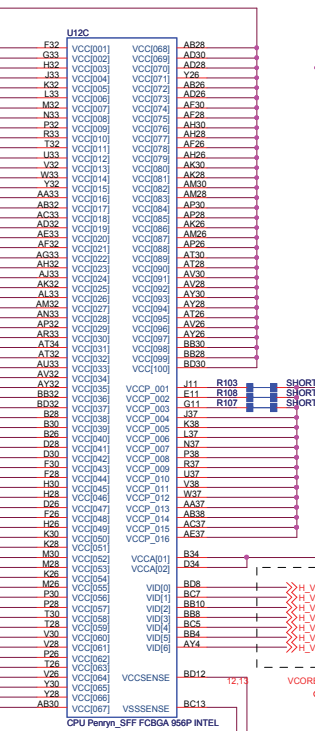
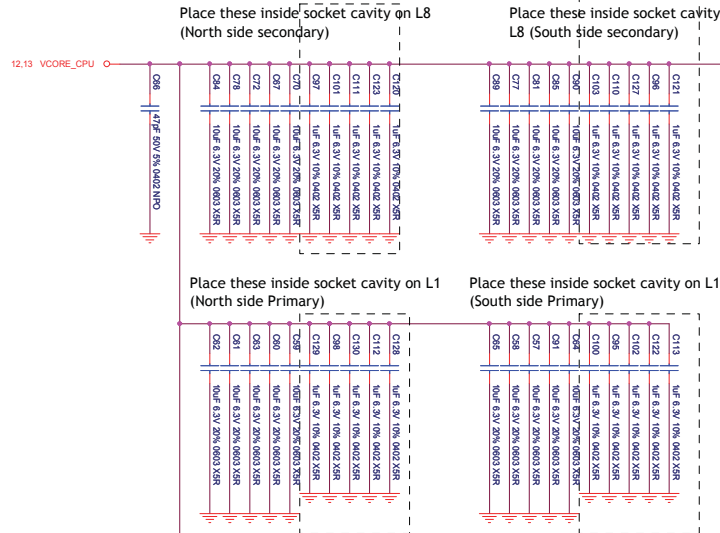
Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.  
 Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

H\_PWRGD rise time :  
 Max : 15ns

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.  
 Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

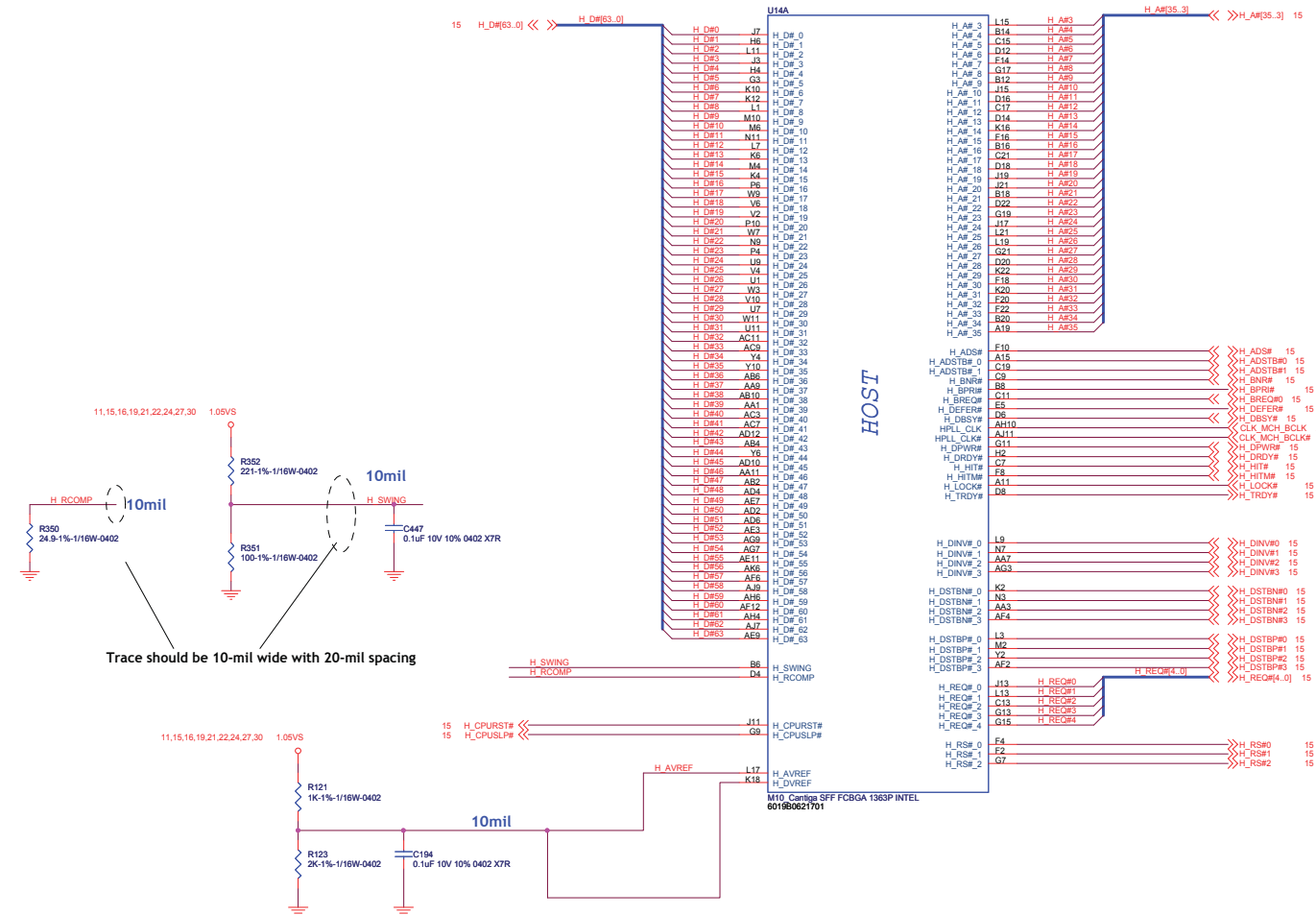
**INVENTEC**  
 SJM31 (Perlyn+Cantiga+ICH9M) SFF  
 Perlyn Processor (I22)

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A222/22-AUG	8
CHANGE by	Miles Liu	DATE	Monday, May 04, 2009
SHEET	16	of	38

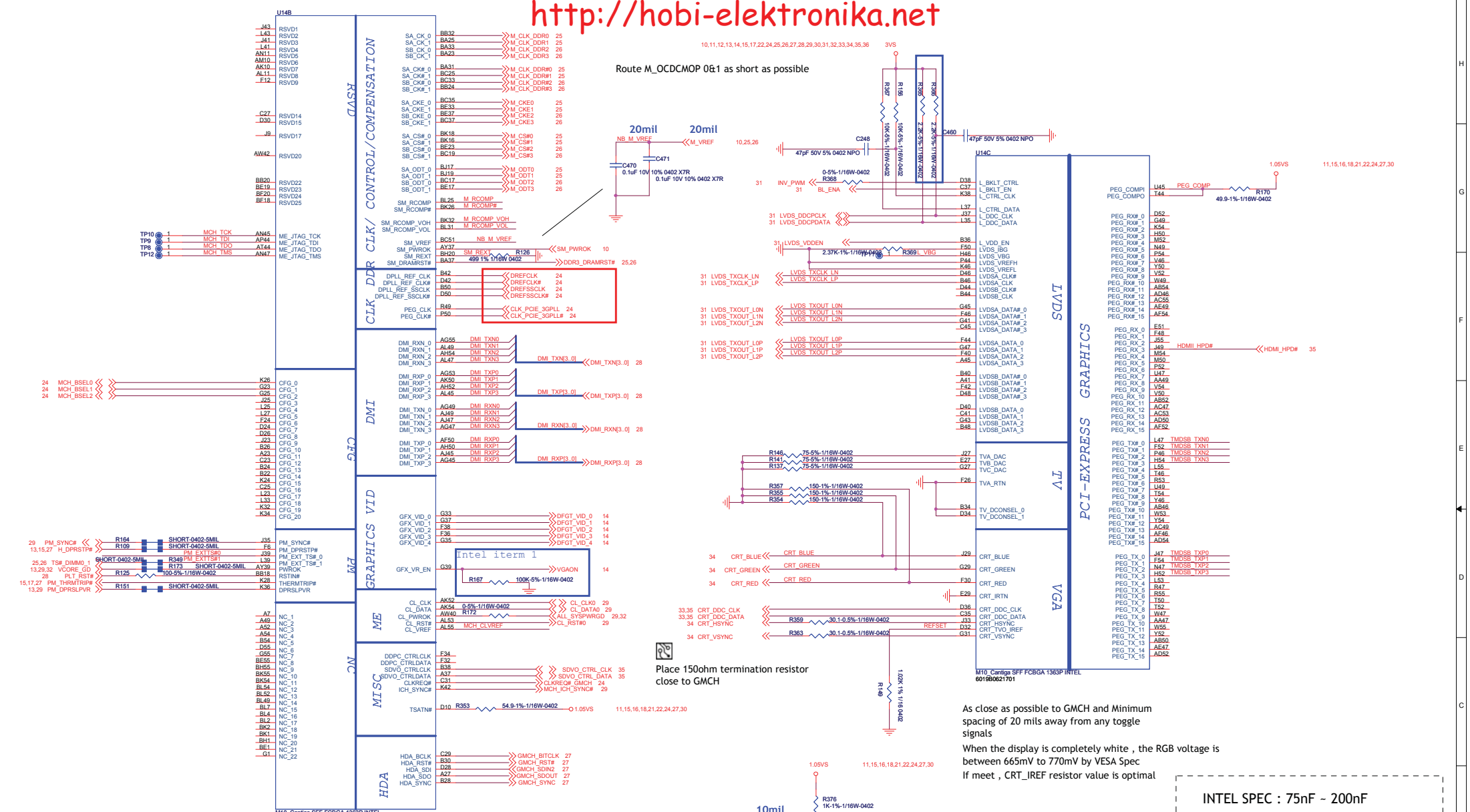




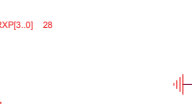
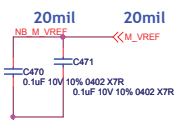




Trace should be 10-mil wide with 20-mil spacing



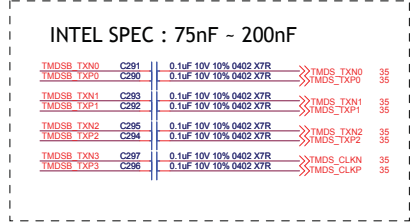
Route M\_OCDMOP 0&1 as short as possible



Place 150ohm termination resistor close to GMCH



As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals  
When the display is completely white , the RGB voltage is between 665mV to 770mV by VESA Spec  
If meet , CRT\_REF resistor value is optimal



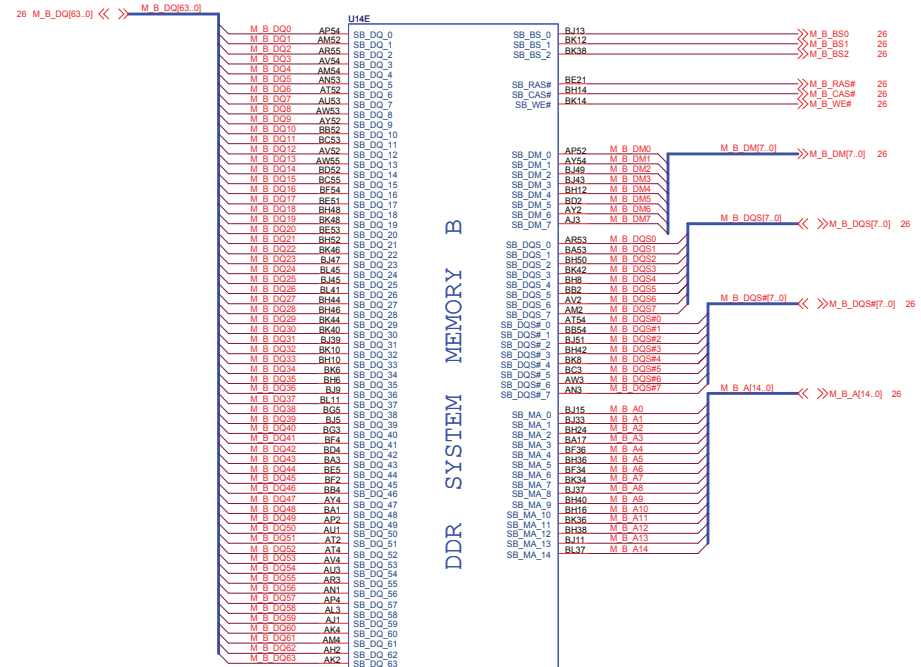
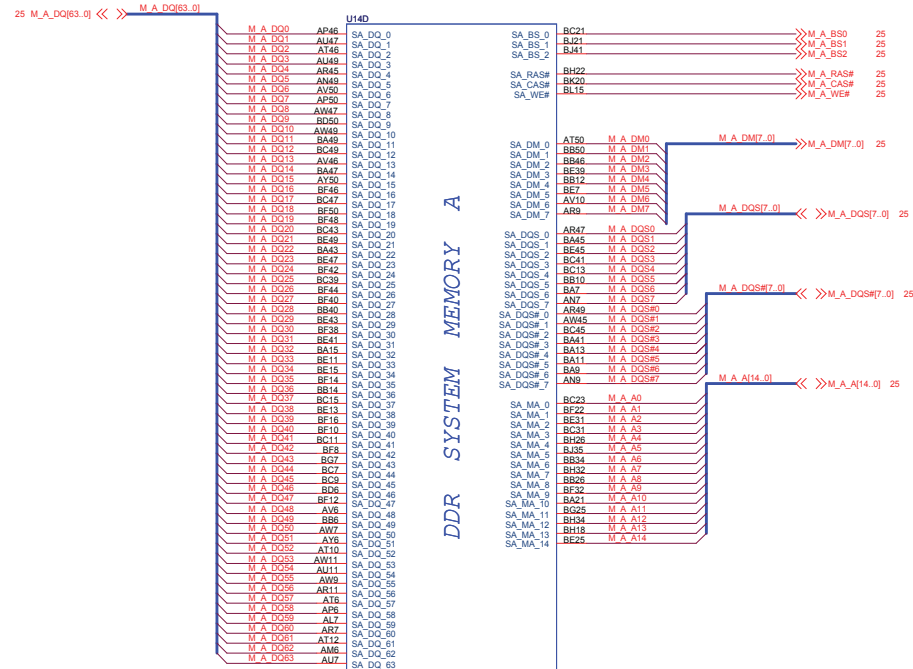
**Cantiga Strapping:**

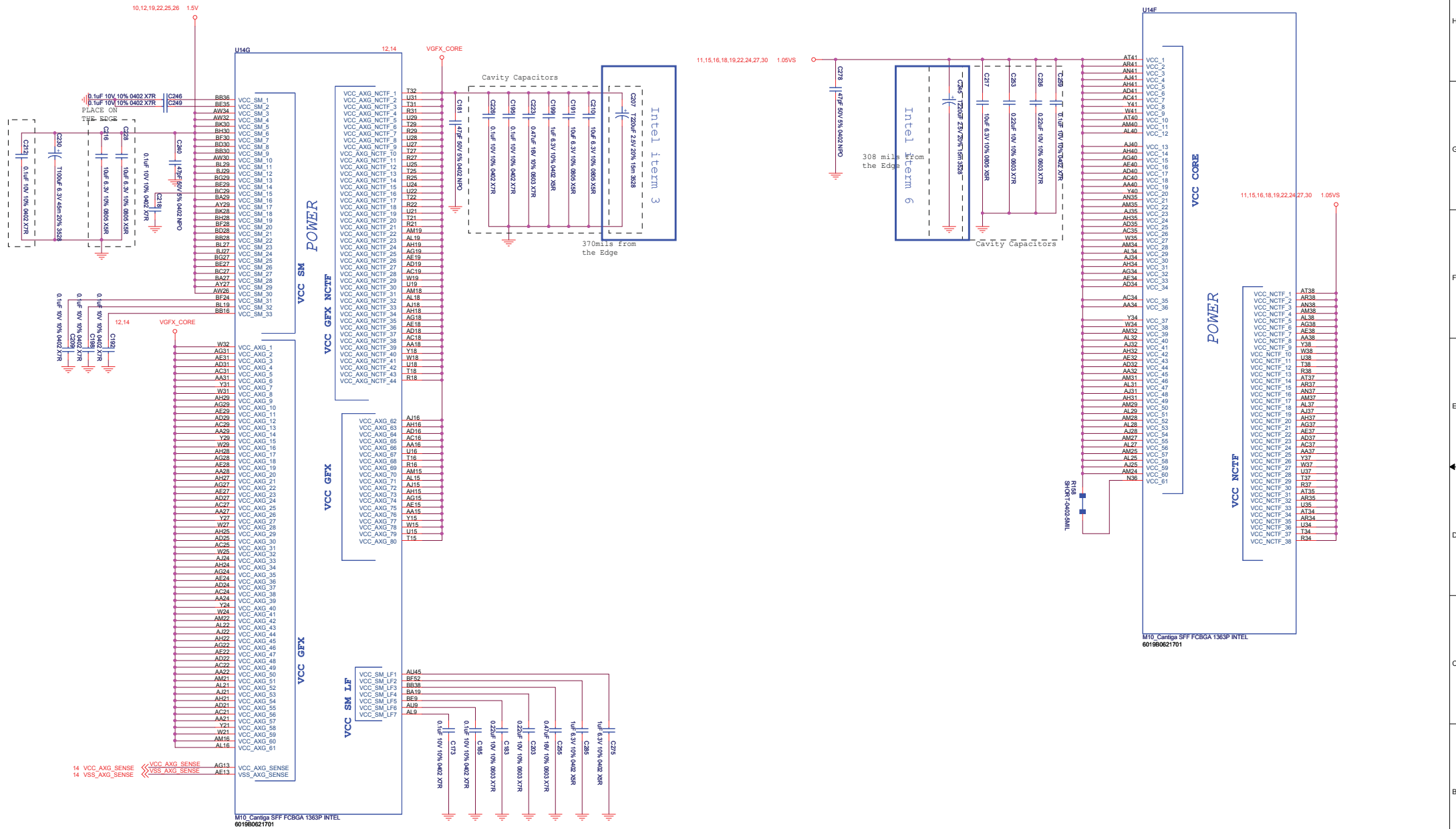
	Low	High
MCH_CFG5	DMIX2	DMIX4
MCH_CFG6 (ITPM Host I/F)	Enable	Disable(default)
MCH_CFG7 (TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIe Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIe loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13 (XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIe x1 is operation	Only SDVO or PCIe x1 with PEG port

**INVENTEC**

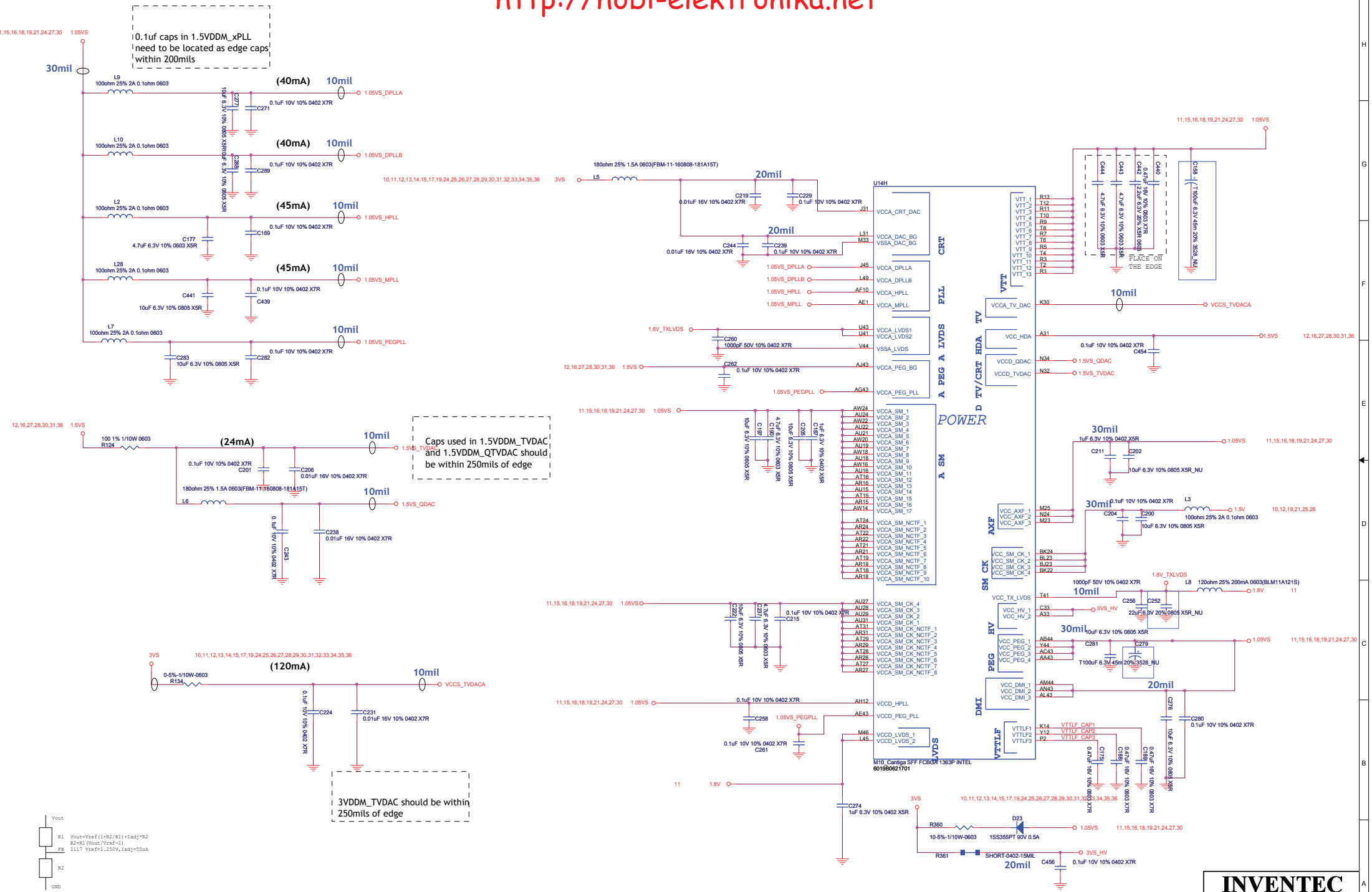
FILE: **SJM31(Pearyn+ Cantiga+ ICH9M)SFF**  
 Cantiga DMI/Graph2/6

SIZE	CODE	DOC NUMBER	REV
Swarm	CS	D-CG-1510M2732-3-ALG	B
SHEET		19	of 36



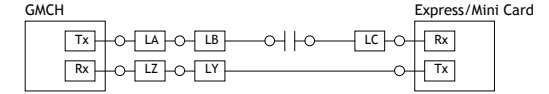
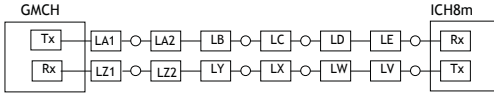


MTO\_Cantiga SFF FCBGA 1363P INTEL 6019B0621701



## DMI Routing Guideline

## PCIe Routing Guideline

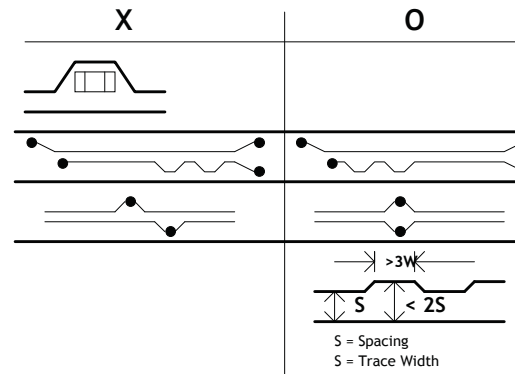
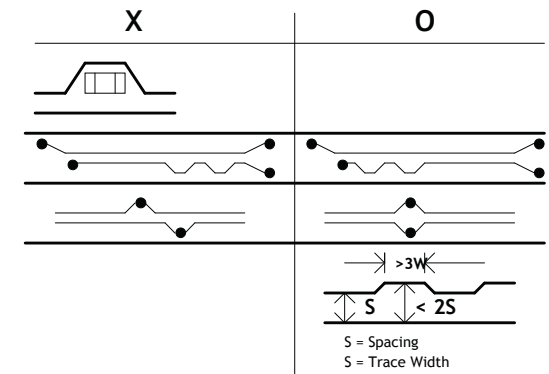


Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LV	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Diddifferential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-LZ (LV+LW+LY+LZ)	Max = 8000 mils	

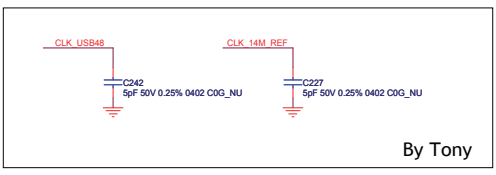
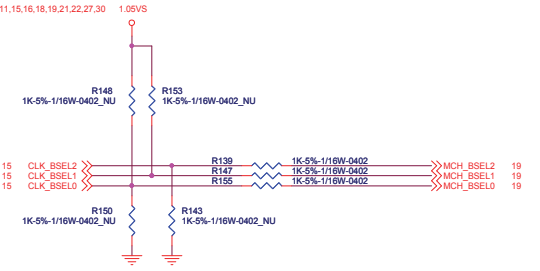
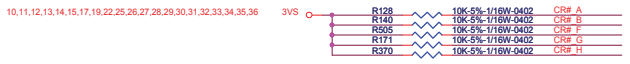
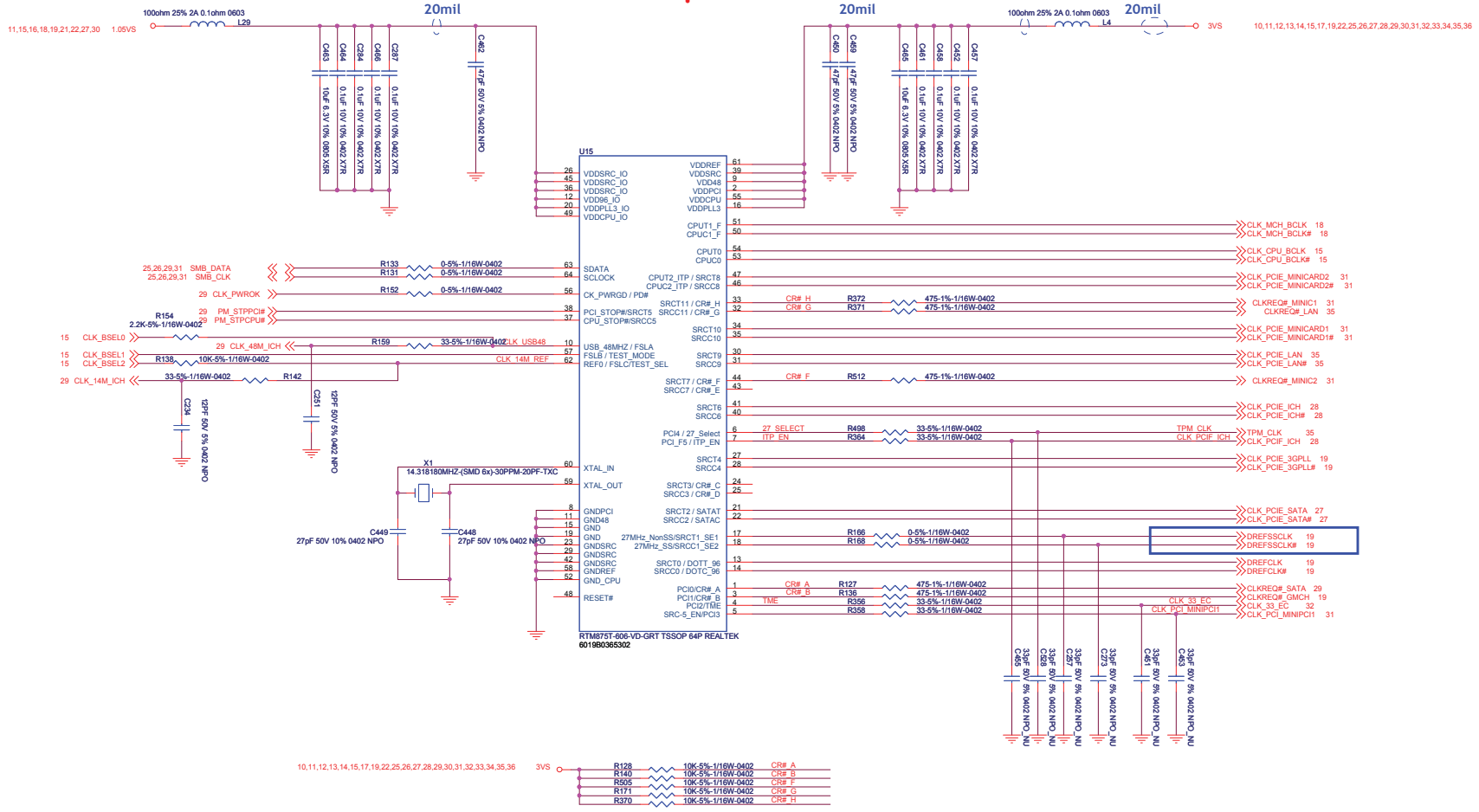
Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 12000 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-LZ (LY+LZ)	Max = 12000 mils	

\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane  
 \*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



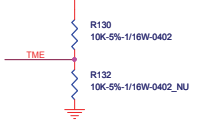
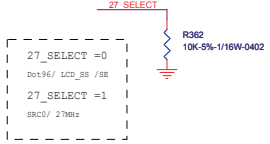
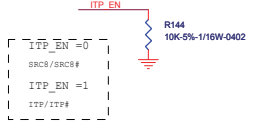
U14i	VSS	C43	AN25	VSS	AM8
BAS5	VSS_1	VSS_100	AG25	VSS_199	VSS_300
AI95	VSS_2	VSS_101	AE25	VSS_200	AK8
AN55	VSS_3	VSS_102	AA25	VSS_201	AN8
AI95	VSS_4	VSS_103	Y25	VSS_202	AF8
AE65	VSS_5	VSS_104	Y25	VSS_203	AD8
AA65	VSS_6	VSS_105	Y25	VSS_204	AB8
US5	VSS_7	VSS_106	Y25	VSS_205	AD8
NS5	VSS_8	VSS_107	BD24	VSS_206	VR
BG34	VSS_9	VSS_108	AN24	VSS_207	FR
BG33	VSS_10	VSS_109	AC24	VSS_208	M8
AE53	VSS_11	VSS_110	AE24	VSS_209	H8
AE53	VSS_12	VSS_111	AA24	VSS_210	H8
AA53	VSS_13	VSS_112	RA1	Y23	B17
US3	VSS_14	VSS_113	MM1	E23	E7
NS3	VSS_15	VSS_114	E41	BD22	BF6
JS3	VSS_16	VSS_115	BD40	BD22	BF6
GS3	VSS_17	VSS_116	AI40	AN22	BA5
E33	VSS_18	VSS_117	AR40	Y22	AW5
K2	VSS_19	VSS_118	AN40	W22	AU5
BG51	VSS_20	VSS_119	W40	R22	AR5
BA51	VSS_21	VSS_120	U40	BL21	AN5
AW51	VSS_22	VSS_121	L40	AY21	AN5
AU51	VSS_23	VSS_122	R40	VSS_220	VSS_321
AR51	VSS_24	VSS_123	K40	AN21	VSS_322
AN51	VSS_25	VSS_124	H40	AG21	VSS_323
AL51	VSS_26	VSS_125	BL39	AE21	VSS_324
AS1	VSS_27	VSS_126	BC39	M21	VSS_325
AG51	VSS_28	VSS_127	BA39	E21	VSS_326
AE51	VSS_29	VSS_128	E39	A21	VSS_327
AA51	VSS_30	VSS_129	A39	BD20	VSS_328
AC51	VSS_31	VSS_130	C39	BD20	VSS_329
W51	VSS_32	VSS_131	BD38	BG19	VSS_330
US1	VSS_33	VSS_132	AI38	AY19	VSS_331
NS1	VSS_34	VSS_133	H38	M19	VSS_332
NS1	VSS_35	VSS_134	RG37	VSS_333	VSS_333
LS1	VSS_36	VSS_135	AI37	BD18	VSS_334
JS1	VSS_37	VSS_136	M37	N18	VSS_335
CS1	VSS_38	VSS_137	E37	H18	VSS_336
CS1	VSS_39	VSS_138	BD36	BL17	VSS_337
BK50	VSS_40	VSS_139	AW36	BG17	VSS_338
AM50	VSS_41	VSS_140	U36	AY17	VSS_339
K50	VSS_42	VSS_141	BL35	M17	VSS_340
RG49	VSS_43	VSS_142	BC35	E17	VSS_341
E49	VSS_44	VSS_143	AY35	A17	VSS_342
C49	VSS_45	VSS_144	AL35	BD16	VSS_343
BG48	VSS_46	VSS_145	AN16	AN16	VSS_344
BB48	VSS_47	VSS_146	AC35	AG16	VSS_345
AY48	VSS_48	VSS_147	AE35	Y16	VSS_346
AV48	VSS_49	VSS_148	AA35	Y16	VSS_347
AT48	VSS_50	VSS_149	Y35	W16	VSS_348
AP48	VSS_51	VSS_150	M35	N16	VSS_349
AM48	VSS_52	VSS_151	E35	H16	VSS_350
AK48	VSS_53	VSS_152	A35	BG15	VSS_351
AH48	VSS_54	VSS_153	BD34	AY15	VSS_352
AF48	VSS_55	VSS_154	AI34	AN15	VSS_353
AD48	VSS_56	VSS_155	AN24	AD15	VSS_354
AB48	VSS_57	VSS_156	U34	VSS_355	VSS_355
Y48	VSS_58	VSS_157	BL33	AC15	VSS_356
V48	VSS_59	VSS_158	BC33	M15	VSS_357
T48	VSS_60	VSS_159	AY33	E15	VSS_358
P48	VSS_61	VSS_160	F33	BD14	VSS_258
IM8	VSS_62	VSS_161	BD32	H14	VSS_259
K48	VSS_63	VSS_162	AN32	BL13	VSS_260
H48	VSS_64	VSS_163	AN32	BG13	VSS_261
BL47	VSS_65	VSS_164	AC32	AY13	VSS_262
BG47	VSS_66	VSS_165	AC32	AI13	VSS_263
E47	VSS_67	VSS_166	Y32	AR13	VSS_264
C47	VSS_68	VSS_167	H32	AI13	VSS_265
A47	VSS_69	VSS_168	B32	AC13	VSS_266
BD46	VSS_70	VSS_169	BL31	W13	VSS_267
AY46	VSS_71	VSS_170	BC31	AI13	VSS_268
AM46	VSS_72	VSS_171	AY31	U13	VSS_269
AK46	VSS_73	VSS_172	AN31	M13	VSS_270
AH46	VSS_74	VSS_173	M31	E13	VSS_271
AG46	VSS_75	VSS_174	E31	A13	VSS_272
AE46	VSS_76	VSS_175	N30	AV12	VSS_273
AA46	VSS_77	VSS_176	H30	BD12	VSS_274
AW46	VSS_78	VSS_177	AN29	AP12	VSS_275
AS46	VSS_79	VSS_178	AN29	AN12	VSS_276
AT46	VSS_80	VSS_179	M29	AK12	VSS_277
AP46	VSS_81	VSS_180	A29	V12	VSS_278
AM46	VSS_82	VSS_181	AW28	V12	VSS_279
AK46	VSS_83	VSS_182	AN28	P12	VSS_280
AH46	VSS_84	VSS_183	AD28	H12	VSS_281
AG46	VSS_85	VSS_184	AC28	BG11	VSS_282
AE46	VSS_86	VSS_185	Y28	VSS_283	VSS_283
AA46	VSS_87	VSS_186	H28	AG11	VSS_284
AW46	VSS_88	VSS_187	F28	E11	VSS_285
AS46	VSS_89	VSS_188	AN27	BD10	VSS_286
AT46	VSS_90	VSS_189	AP10	AY10	VSS_287
AP46	VSS_91	VSS_190	A27	VSS_288	VSS_288
AM46	VSS_92	VSS_191	AD27	H10	VSS_289
AK46	VSS_93	VSS_192	BF26	BL9	VSS_290
AH46	VSS_94	VSS_193	BD26	E9	VSS_291
AG46	VSS_95	VSS_194	N26	AG	VSS_292
AE46	VSS_96	VSS_195	H26	BD8	VSS_293
AA46	VSS_97	VSS_196	BL25	BB8	VSS_294
AW46	VSS_98	VSS_197	AY25	VSS_295	VSS_295
AS46	VSS_99	VSS_198	AU25	AV8	VSS_296
AT46	VSS_100	VSS_199		VSS_297	VSS_297
AP46	VSS_200	VSS_200		VSS_298	VSS_298
	VSS_201	VSS_201		VSS_299	VSS_299
	VSS_202	VSS_202		VSS_300	VSS_300

M10\_Cantiga SFF PCBGA 1363P INTEL  
 IC\_M10\_Cantiga SFF.pdf



By Tony

FSA	F5B	F5C	F5B CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266



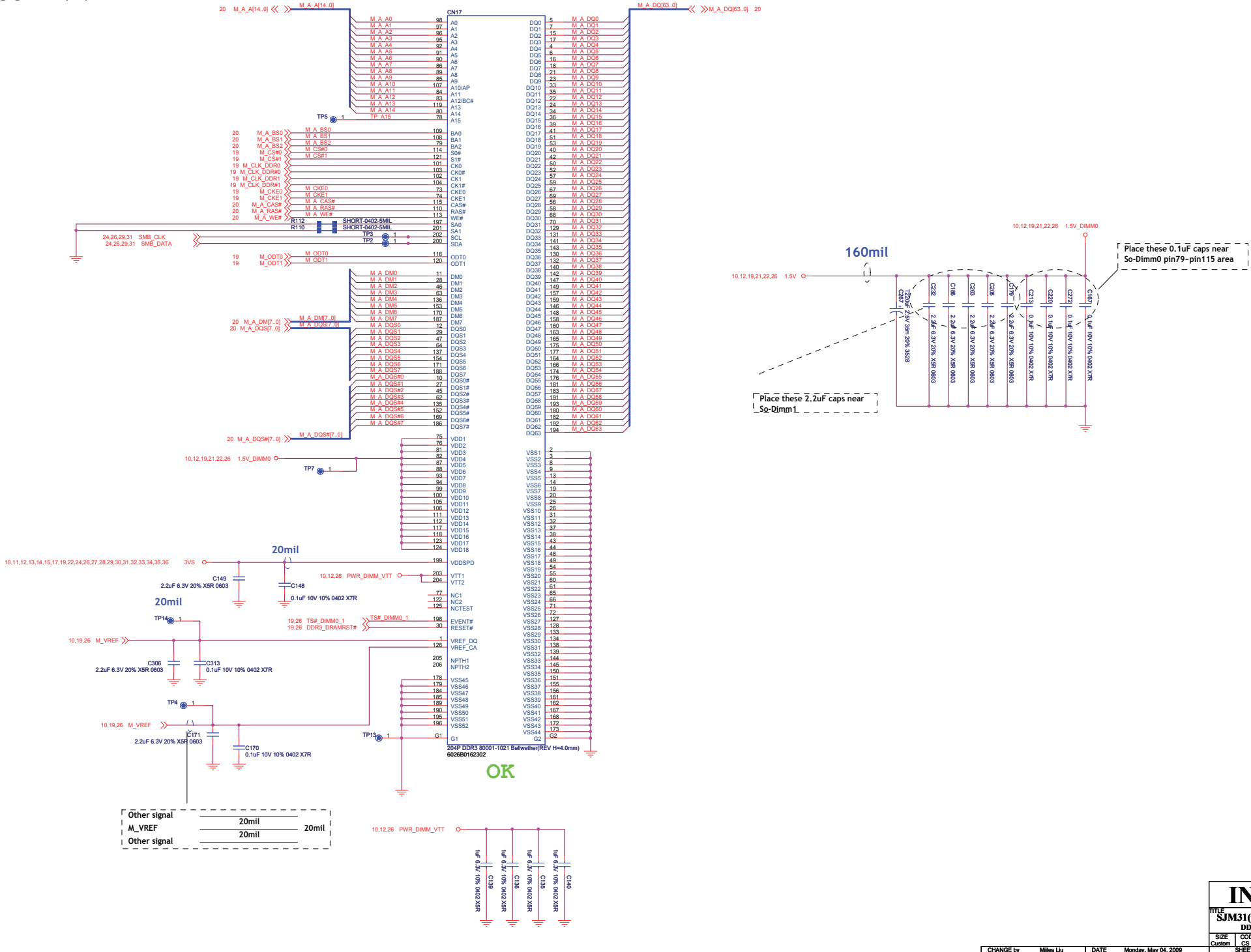
CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

**INVENTEC**  
 TITLE: **SJM31(Penryn+Cantiga+ICH9M)SFF**  
 Clock Generator

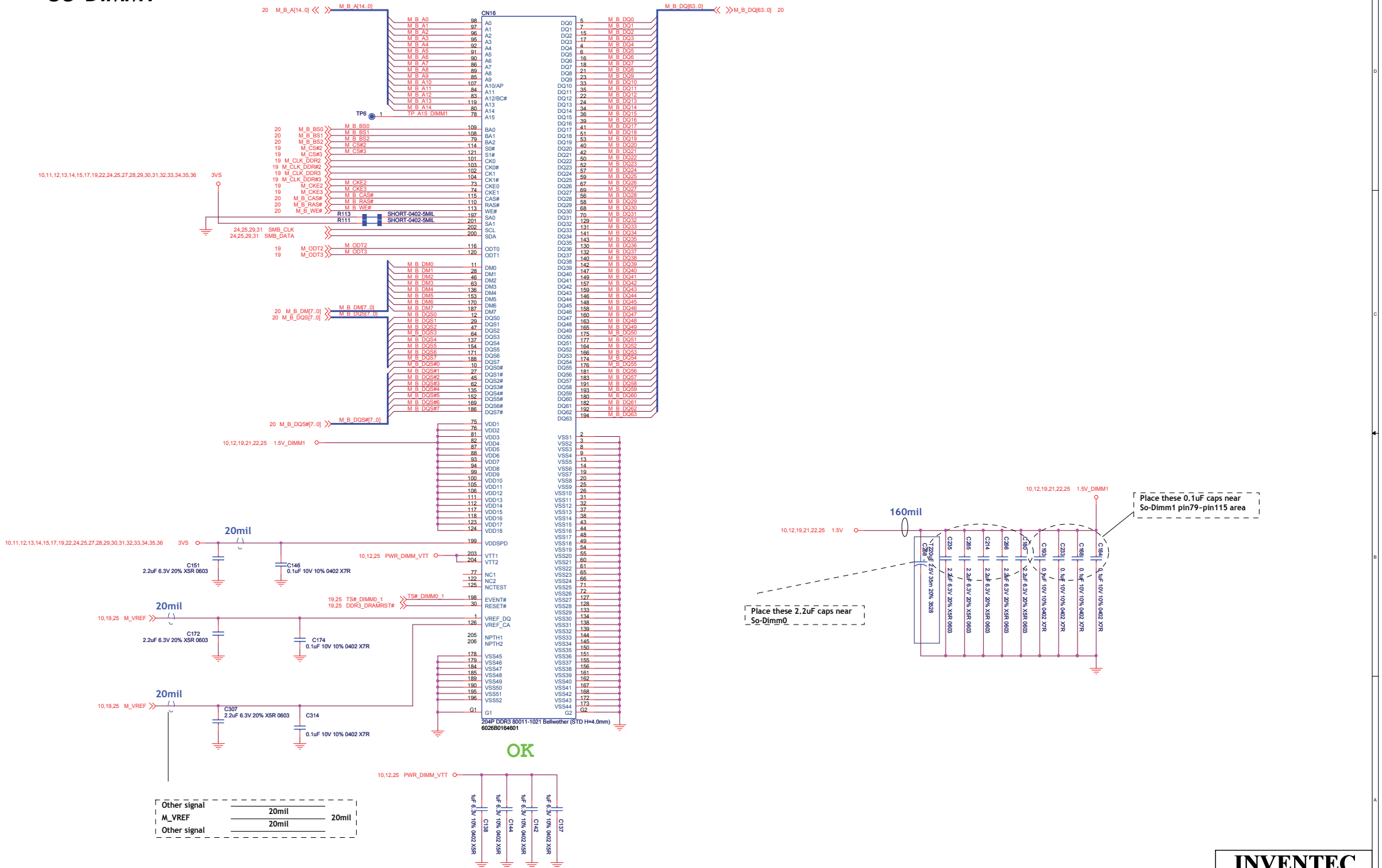
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22782-0-ALG	6
SHEET		24	of 36



SO-DIMMO



# SO-DIMM1



OK

**INVENTEC**  
 TITLE: SJM31(Penryn+Cantiga+ICH9M)SFF  
 DDR3 SDRAM SO-DIMM1

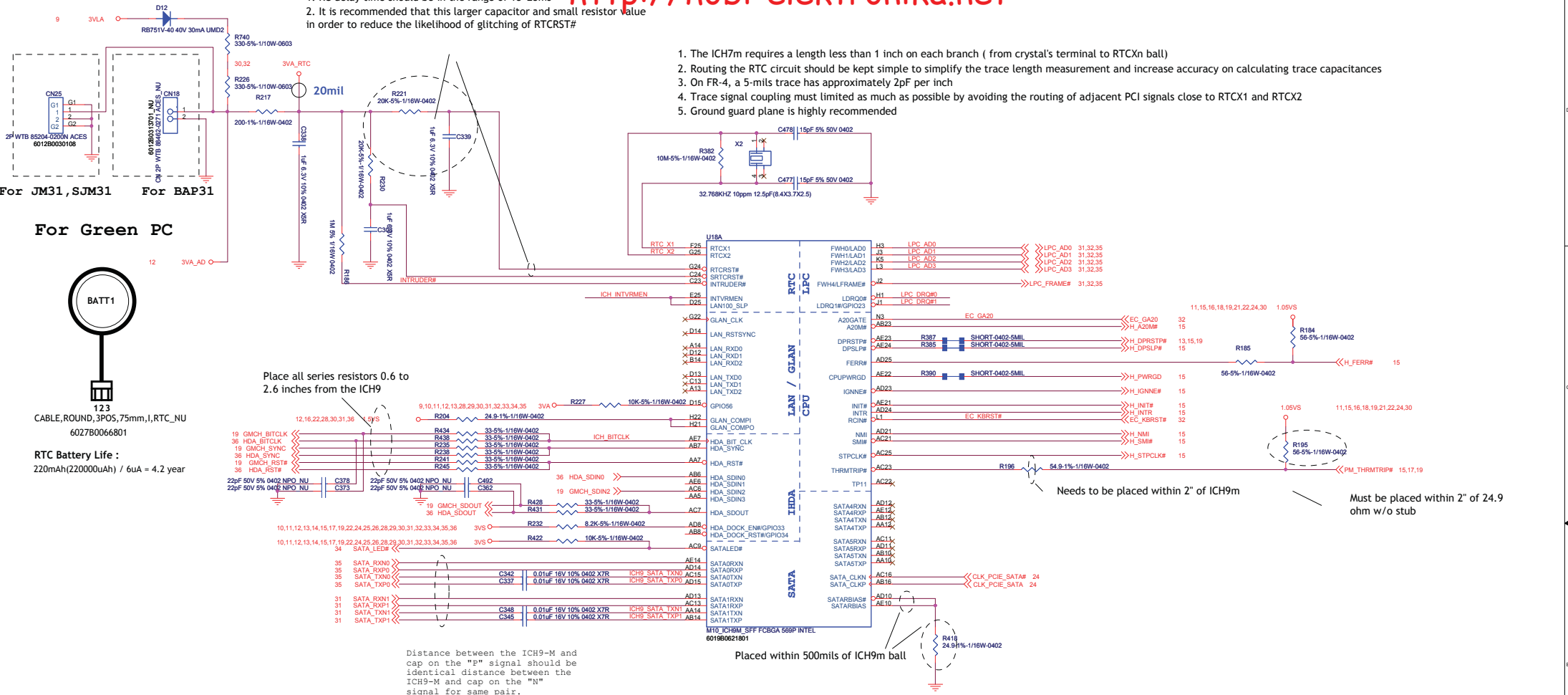
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22782-0-ALG	8
SHEET		26	of 36

# RTC Circuit

<http://hobi-elektronika.net>

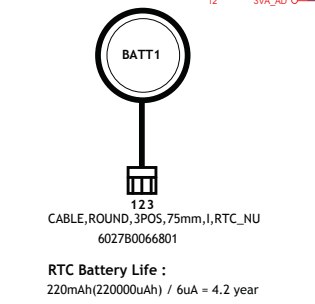
1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch ( from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



For JM31, SJM31 For BAP31

For Green PC



Place all series resistors 0.6 to 2.6 inches from the ICH9

Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub

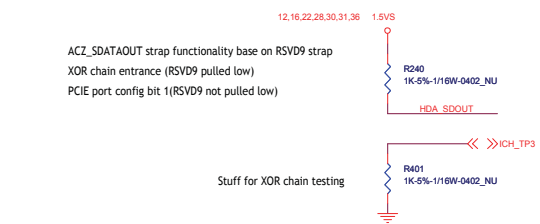
Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Placed within 500mils of ICH9m ball

## ICH9m internal VR enable strap

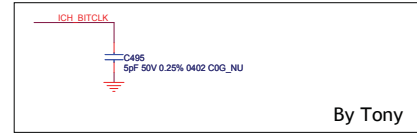
	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1\_05, VccSus1\_5, VccCl1\_5, VccLAN1\_05 and VccCl1\_05



XOR Chain Entrance Strap - to be updated	ICH TP3	HDA SDOOUT	Description
0	0	0	RSDV9
0	1	0	Enter XOR Chain
1	0	0	Normal Operation (Default)
1	1	1	See PCIe port config bit 1

Short pins AG1 and AG2 at the package



**INVENTEC**

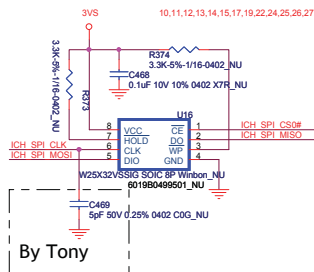
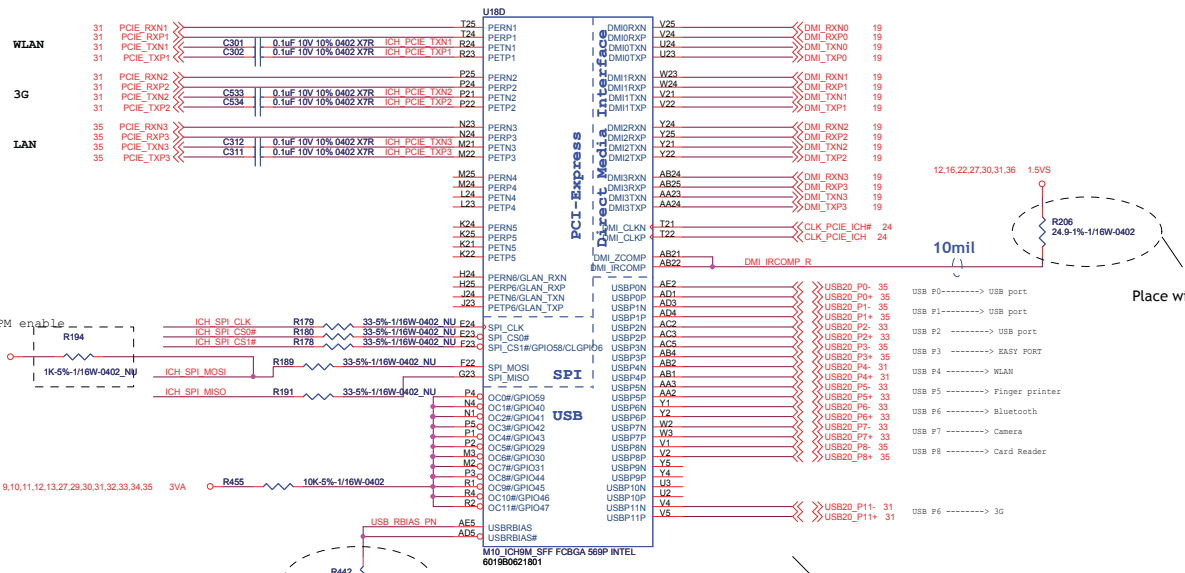
TITLE: **SJM31(Penryn+Cantiga+ICH9M)SFF**

IC19M CPU/IDE/SATA(L14)

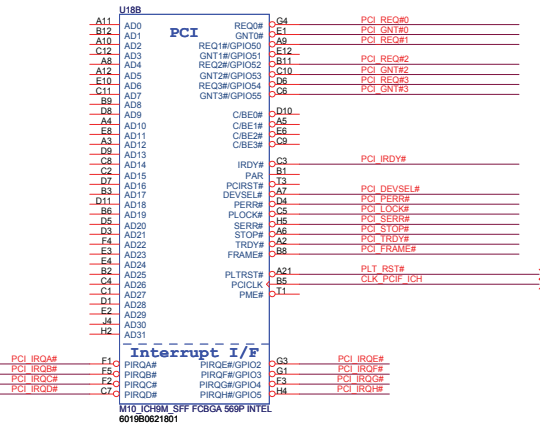
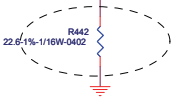
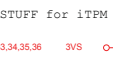
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22782-0-ALG	8

SHEET 27 of 38

PCIe AC coupling caps need to be within 250mils of the driver

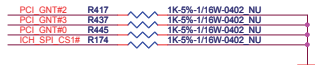
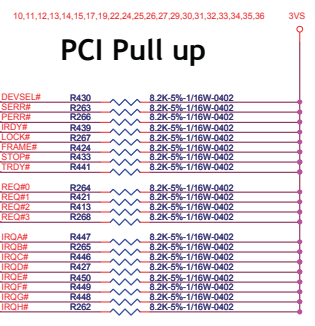


By Tony



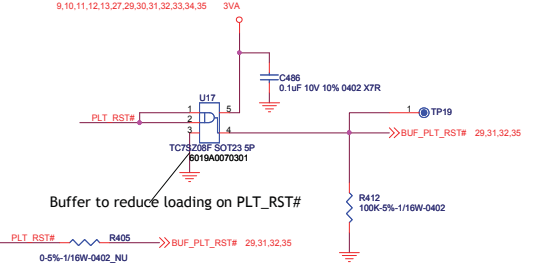
Place within 500mils of ICH

Place within 500mils of ICH  
5/5 mils spacing on microstrip



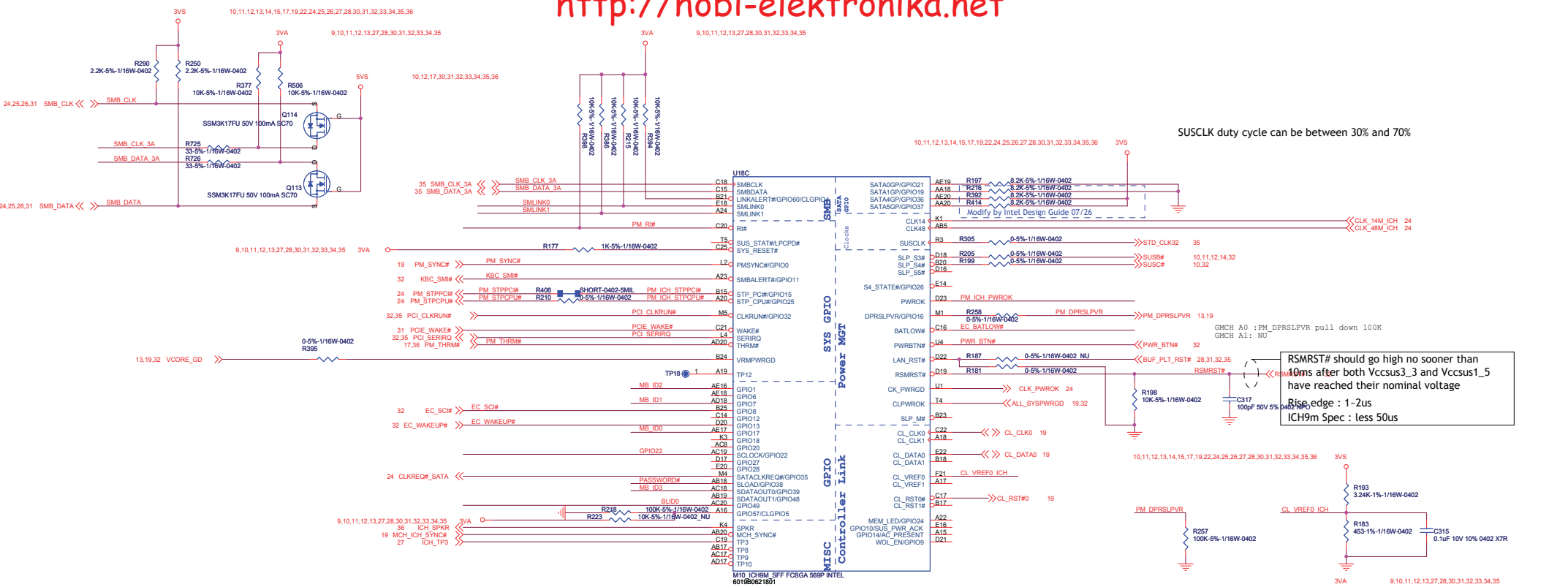
PCI\_GNT#3 No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPL_CS1#	LPC
1	1	LPC
1	0	PCI
0	1	SPI

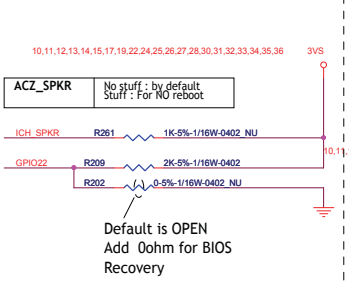


Check BIOS type

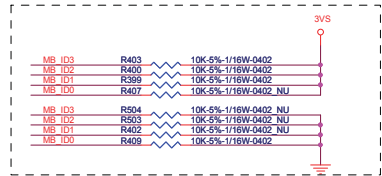
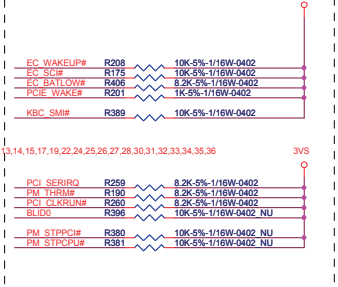
**INVENTEC**  
 TITLE: SJM31(Pearlyn+Catiga+ICH9M)SFF  
 ICH9M PCI/PCIE/DMI/USB(Z4)  
 SIZE: Custom SHEET: 28 of 36  
 CODE: CS  
 DOC NUMBER: D-CS-1310A22732-9-ALG  
 REV: S  
 CHANGE by: Miles Liu DATE: Monday, May 04, 2009



**ICH9m strap**

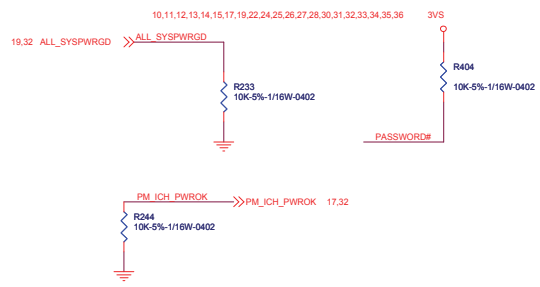


**PMU P/U**



**BIOS ID setting**

Project	MB_ID3 GPIO 39	MB_ID2 GPIO 1	MB_ID1 GPIO 7	MB_ID0 GPIO 17
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0



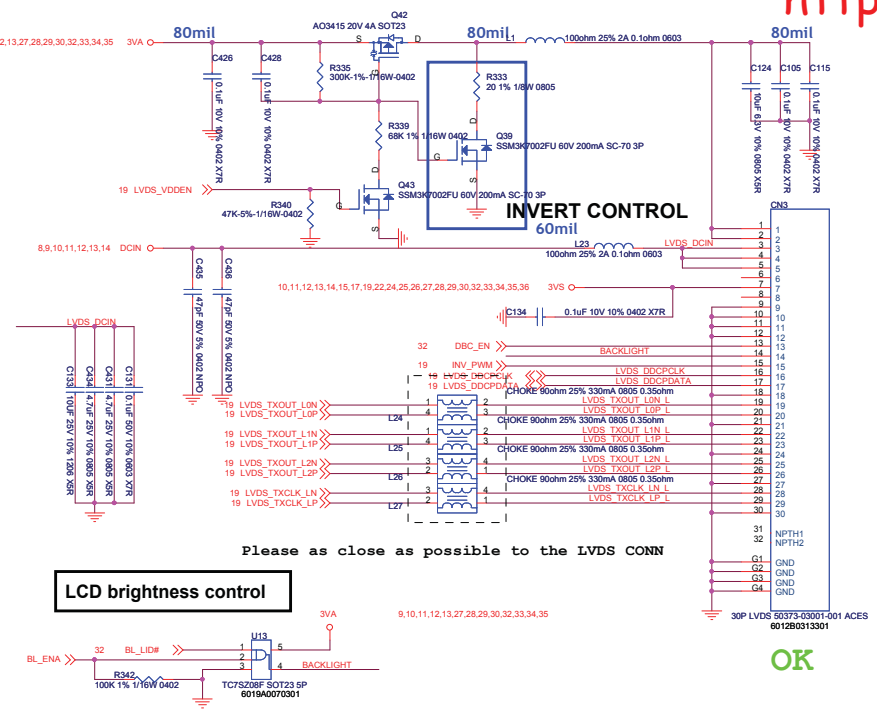
**INVENTEC**

TITLE: **SJM31(Penryn+Cantiga+ICH9M)SFF**  
 ICH9M GPIO(3/4)

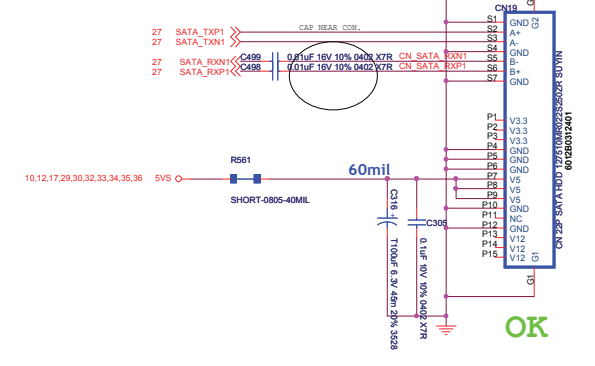
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2272-0-ALG	8
SHEET		29	of 38



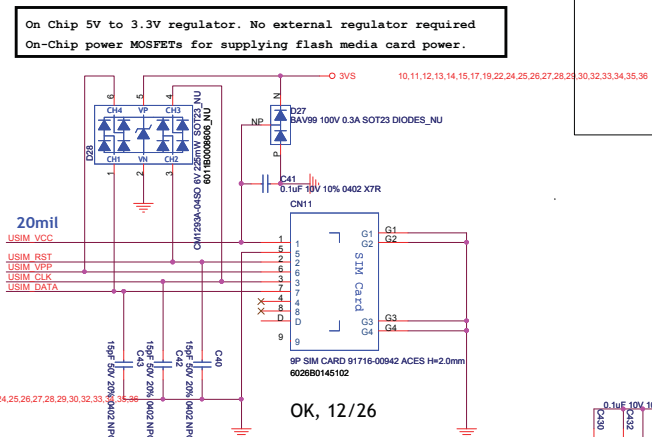
LVDS Interface



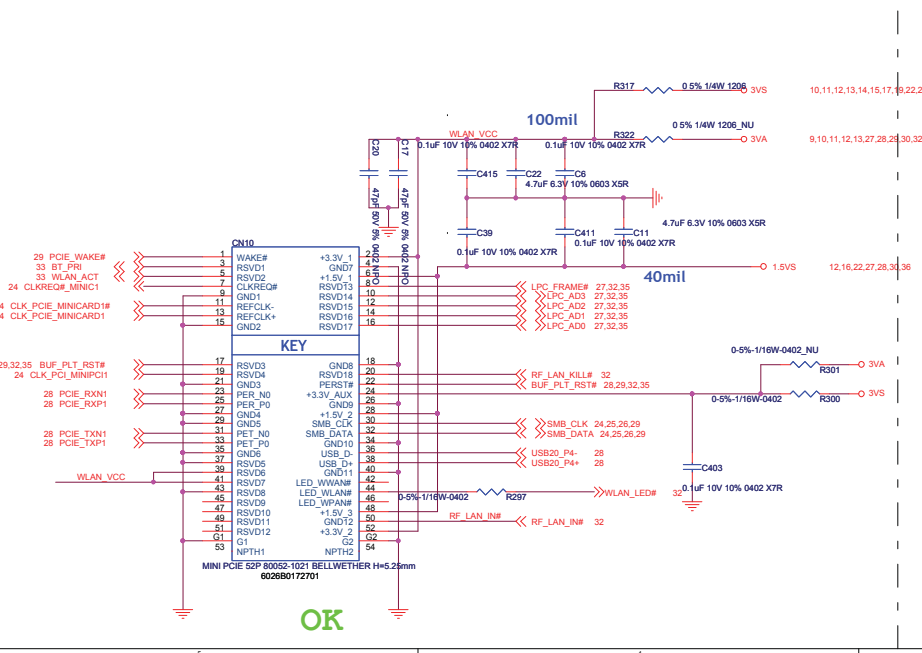
HDD I/F



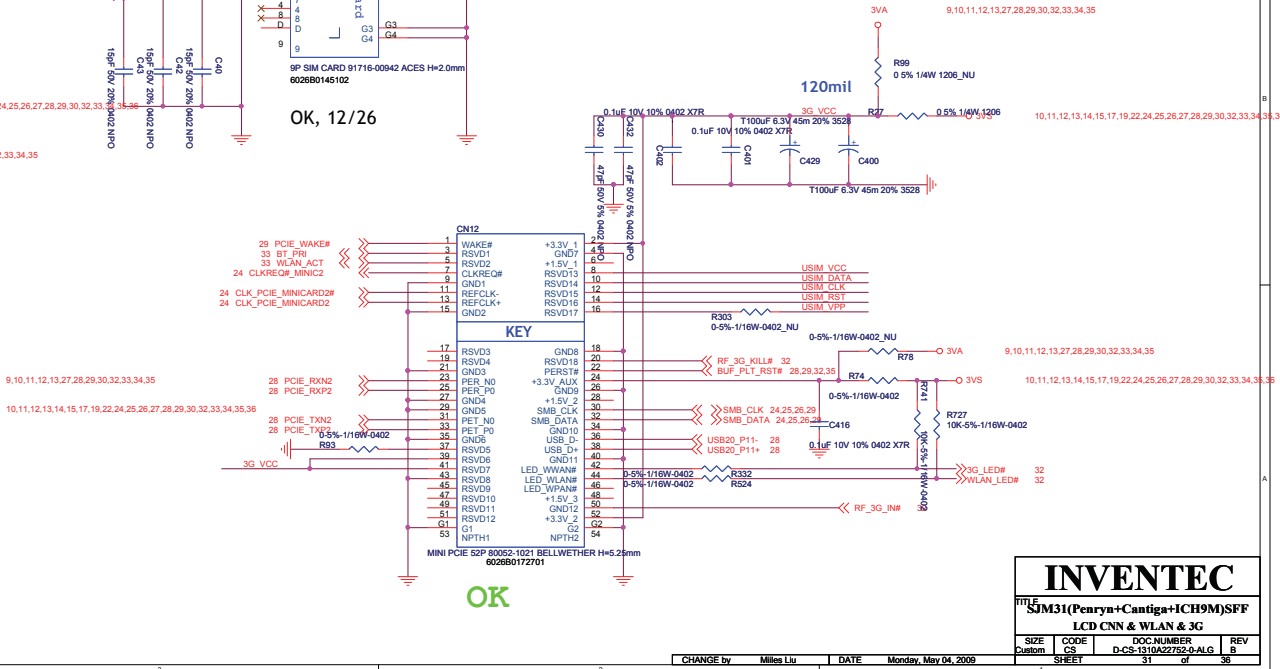
SIM CARD slot



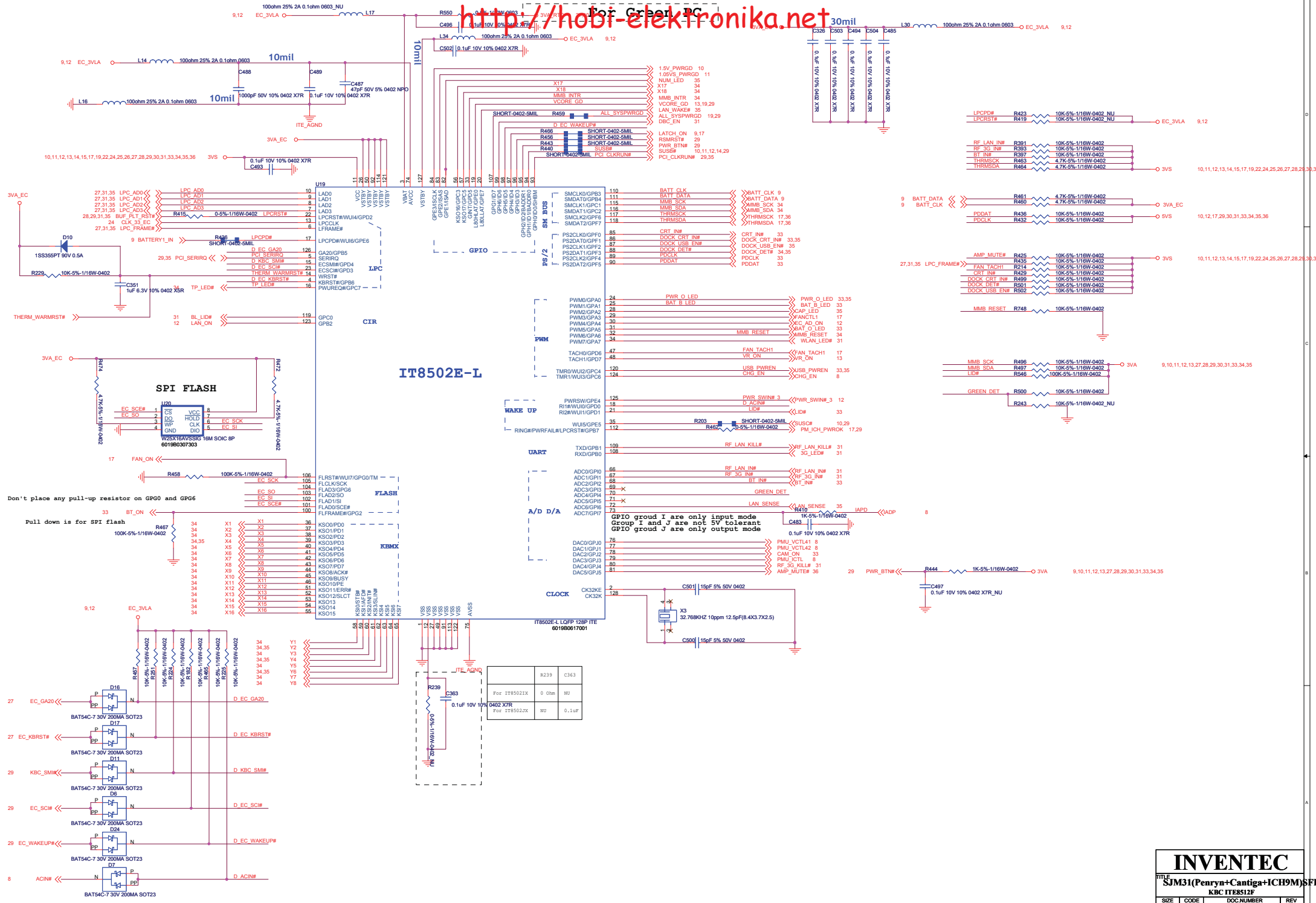
PCIe Mini Card(WLAN)



PCIe Mini Card for 3G



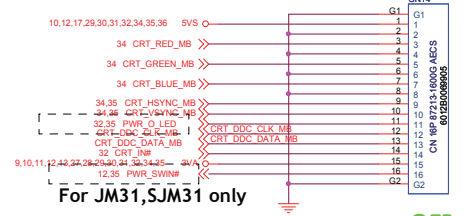
**INVENTEC**  
 TITLE: **UM31(Penryn+Cantiga+I19M)SFF**  
 LCD CNN & WLAN & 3G  
 SIZE: Custom CODE: CS DOC NUMBER: D-CS-1310A22752-D.ALG REV: B  
 CHANGE by: Miles Lu DATE: Monday, May 04, 2009 SHEET: 31 of 38





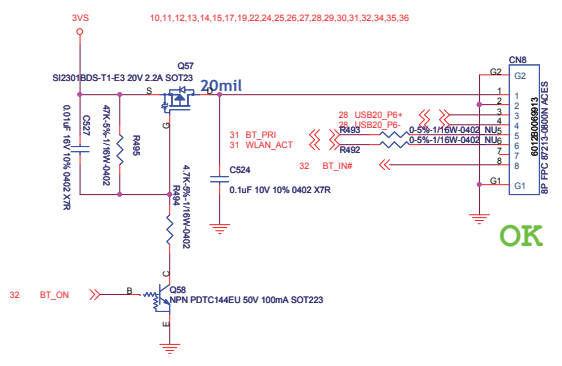
# VGA Board CN

(CRT+ PWR SW)



OK

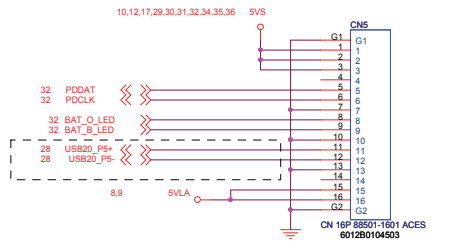
# Bluetooth CON.



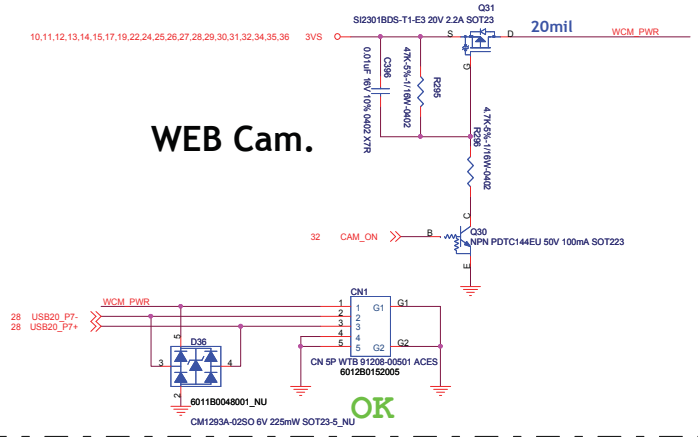
OK

# GLIDE PAD Board

For BAP31 only



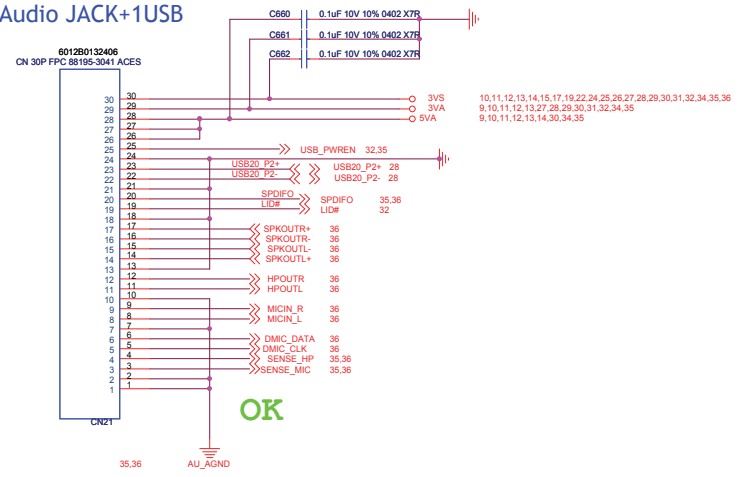
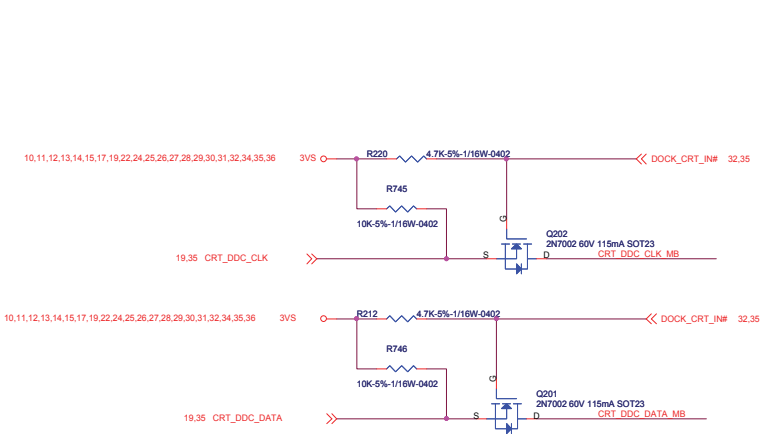
# WEB Cam.



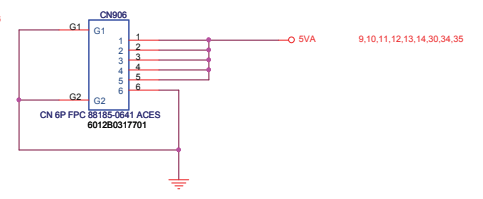
OK

# AUDIO Board CN

(Audio JACK+1USB)



OK

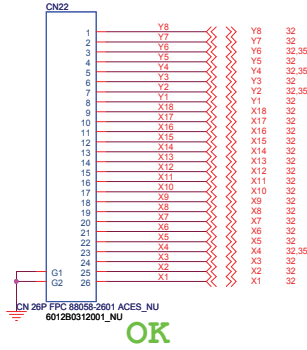
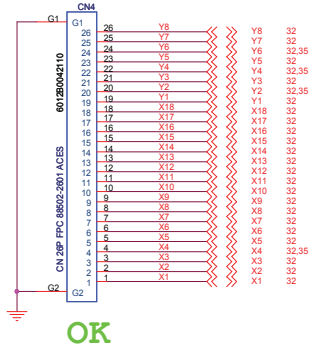


# INVENTEC

TITLE			
SJM31(Penryn+Cantiga+ICH9M)SFF			
Daughter Connector			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2232-0-ALG	B
SHEET		33	36

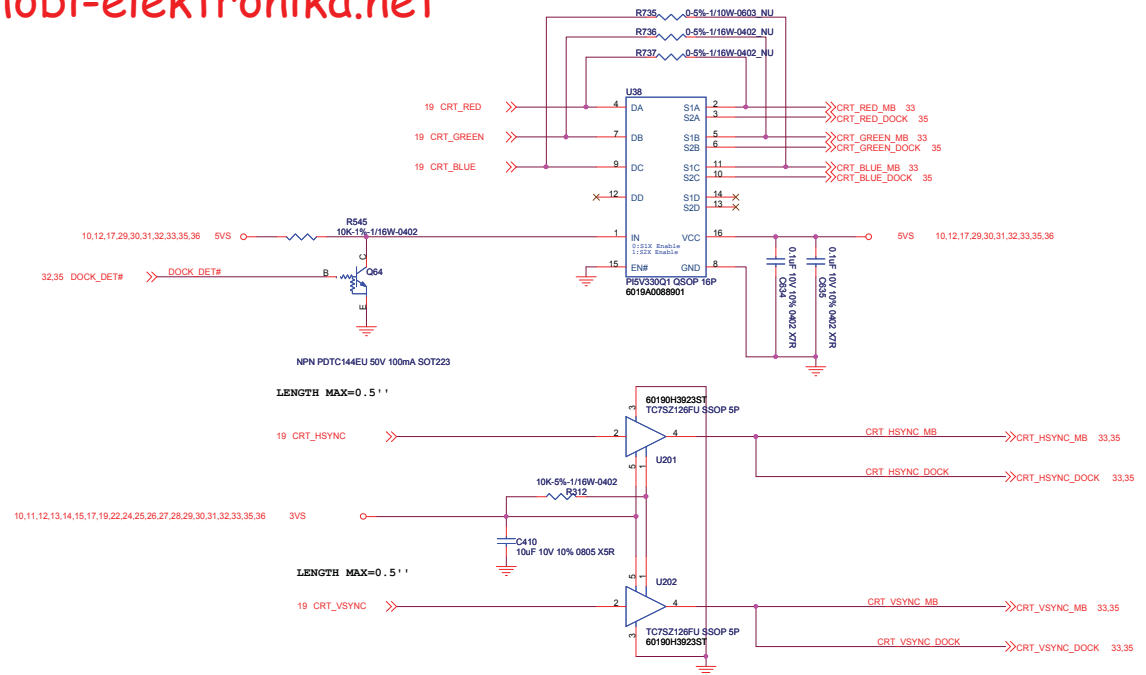
To K/B(For JM31,BAP31)

To K/B (For SJM31)

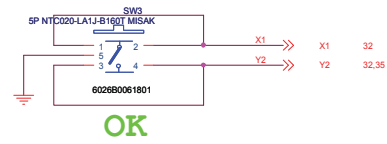


OK

OK

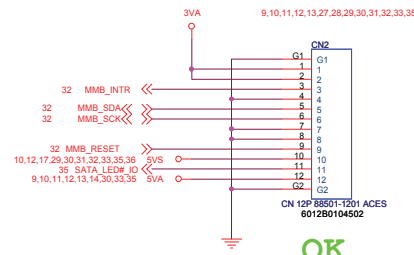


SW (FOR SJM31)



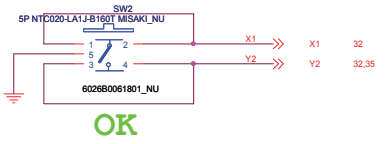
OK

SW Sensor BOARD(For JM31,SJM31)

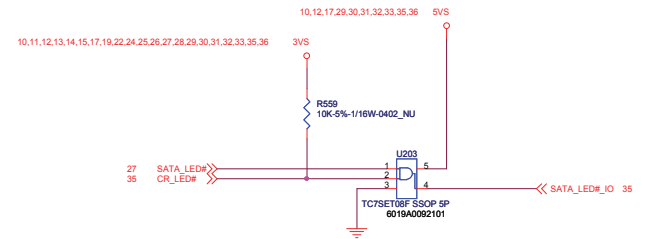


OK

SW (FOR JM31,BAP31)



OK



JM31 ---- 120 Ohm  
SJM31 ---- 470 Ohm

GP lock Button / LED(FOR SJM31)

GP lock Button / LED(FOR BAP31)

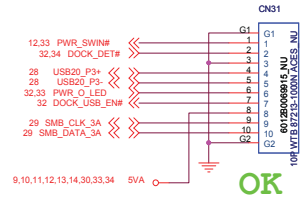
GP lock Button / LED(FOR JM31)

INVENTEC

MODEL  
SJM31(Penrya+Cantiga+ICH9M)SFF  
BDP

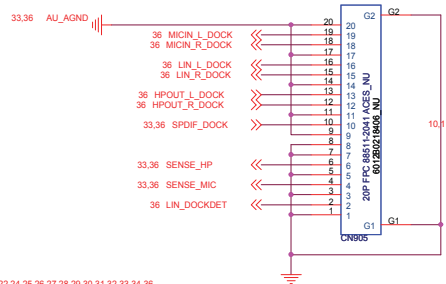
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22732-0-ALG	B
SHEET	34	9	36

MB(USB) TO EASY/B



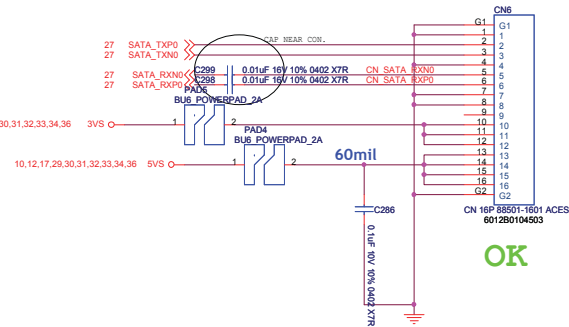
OK

MB(AUDIO) TO EASY/B(For BAP31)



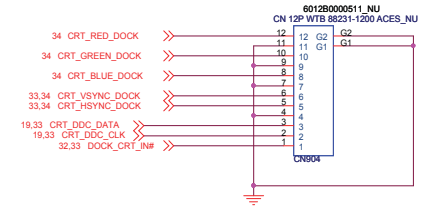
OK

SSD I/F

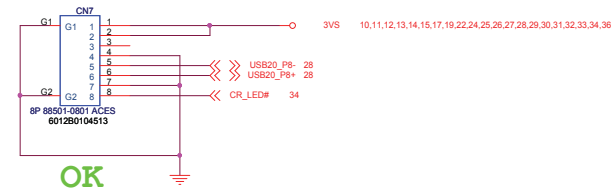


OK

MB (RGB) TO EASY/B

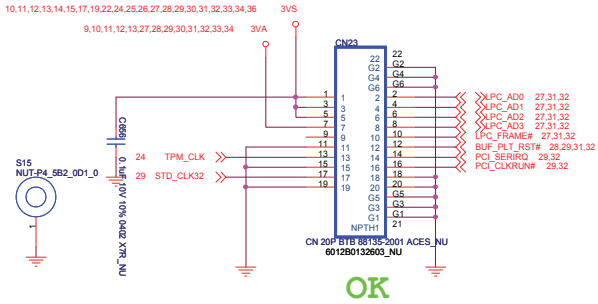


Card Reader BOARD CN



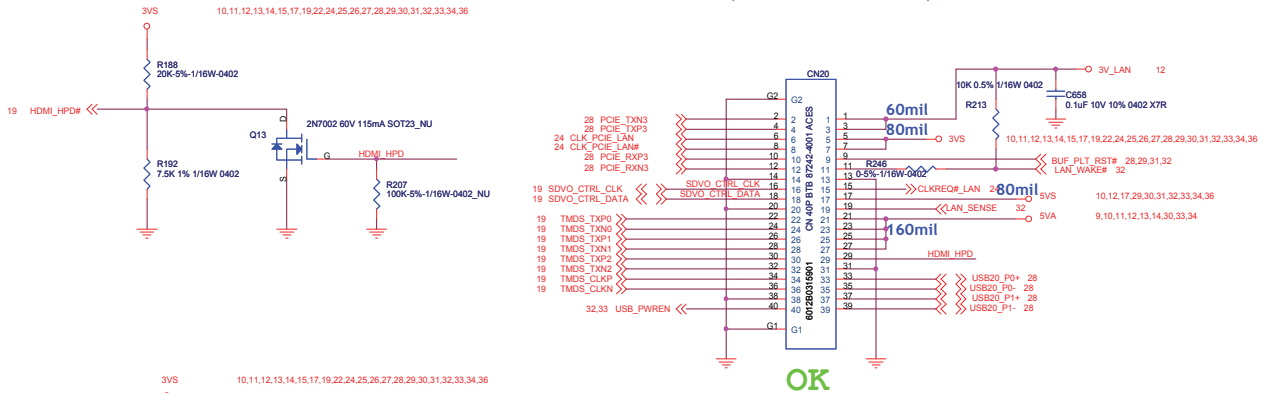
OK

TPM CN



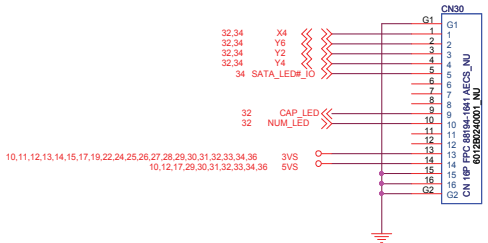
OK

USB Board CN (LAN+HDMI+2USB)

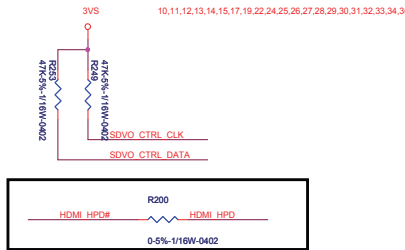


OK

SW/B CN



OK



INVENTEC SJM31(Penrya+Cantiga+ICH9M)SFF BDP. Table with columns: SIZE, CODE, DOC NUMBER, REV, CS, ALG, B.

