

Compal Confidential

KAL90/KALH0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

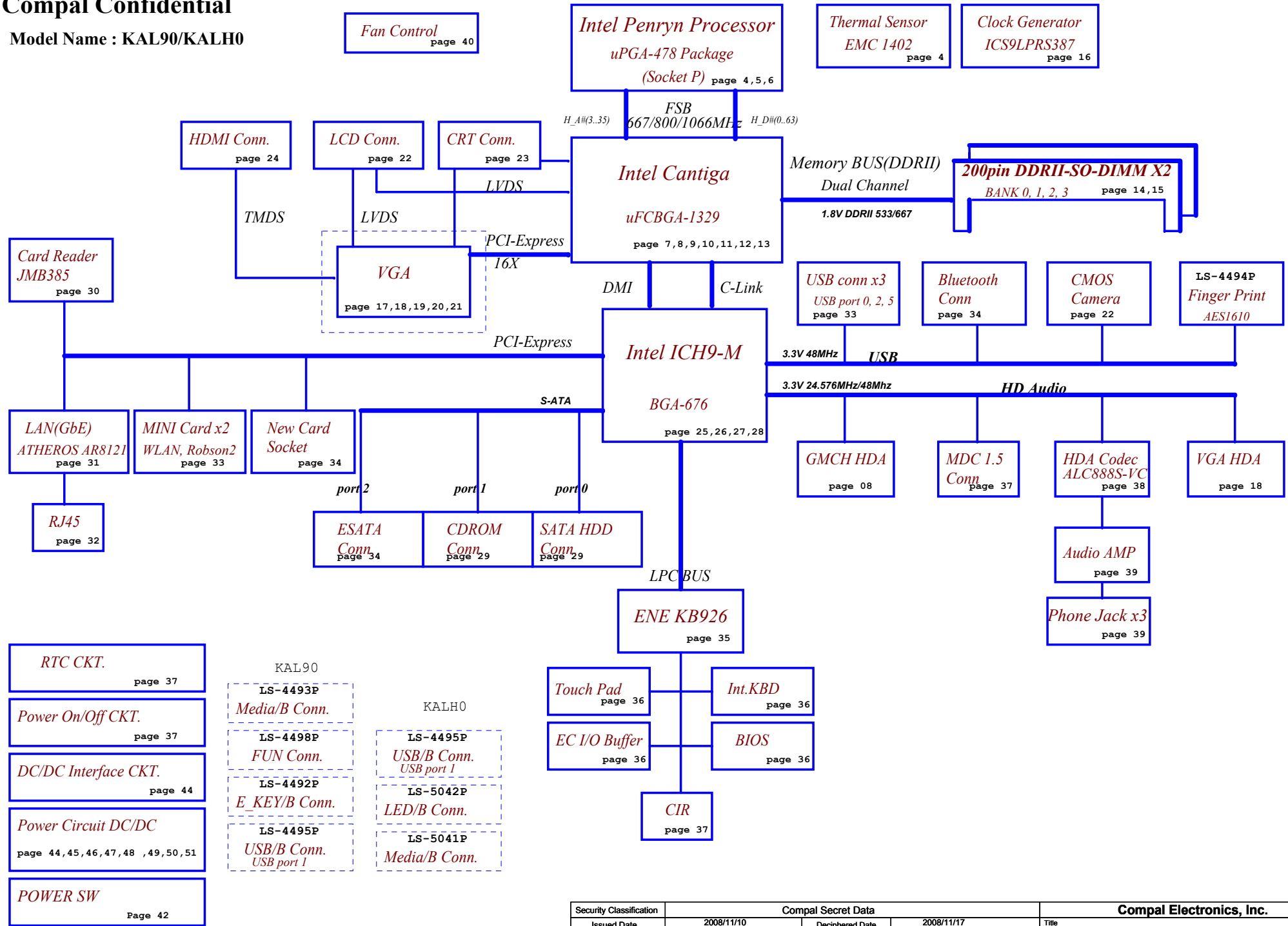
2008-12-17

REV: 1.0

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Model Name : KAL90/KALH0



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- Power On/Off CKT. page 37
- DC/DC Interface CKT. page 44
- Power Circuit DC/DC page 44, 45, 46, 47, 48, 49, 50, 51
- POWER SW Page 42

- KAL90
- LS-4493P Media/B Conn.
 - LS-4498P FUN Conn.
 - LS-4492P E_KEY/B Conn.
 - LS-4495P USB/B Conn. USB port 1
- KALH0
- LS-4495P USB/B Conn. USB port 1
 - LS-5042P LED/B Conn.
 - LS-5041P Media/B Conn.

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
KAL90	JAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@

BOM Configuration Table

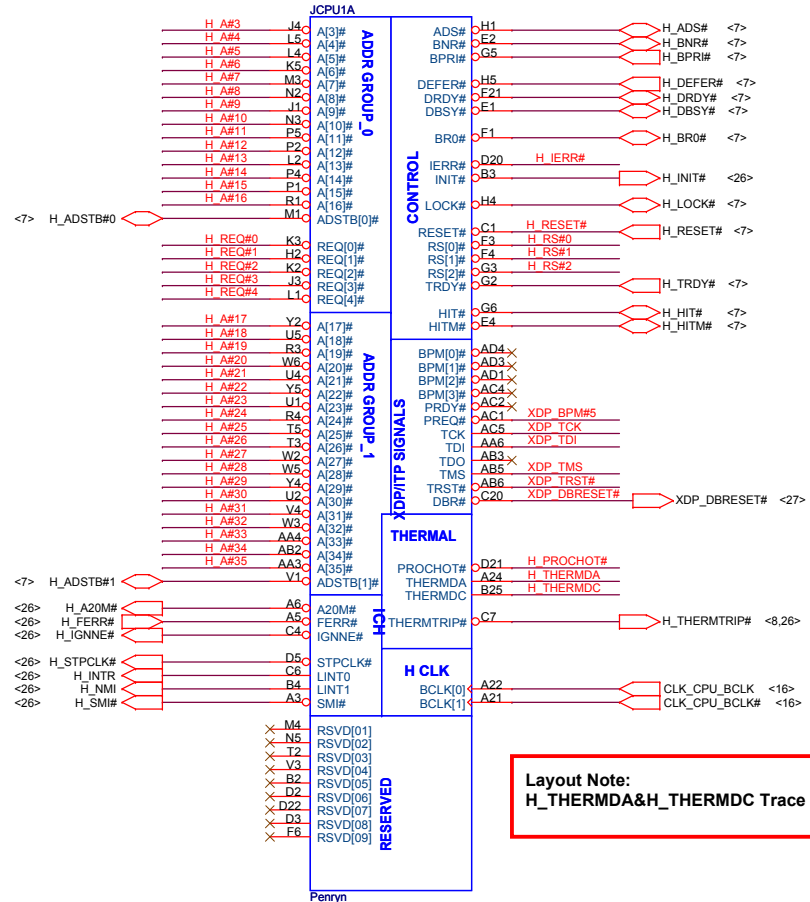
Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX: KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX: KAL90@/PM@/888VC@/8121@
KAL90-GM45	XXXXXXXXXX: KALH0@/GM@/888VC@/8121@/GM45@
KAL90-GL40	XXXXXXXXXX: KALH0@/GM@/888VC@/8121@/GL40@
KAL90-PM45	XXXXXXXXXX: KALH0@/PM@/888VC@/8121@

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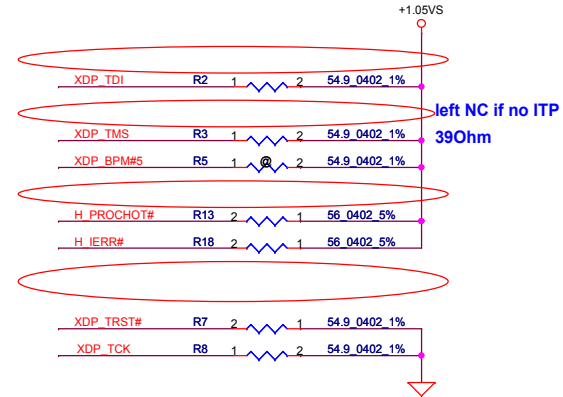
<7> H_A#(3..35) H_A#(3..35)

<7> H_REQ#(0..4) H_REQ#(0..4)

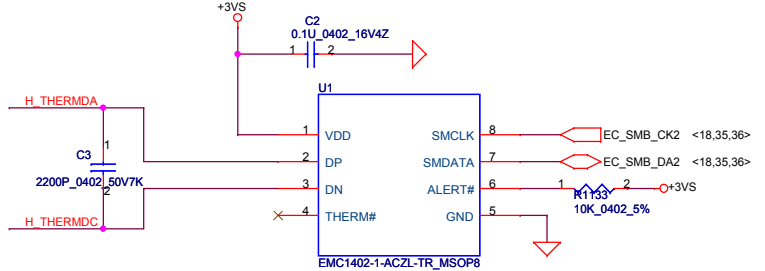
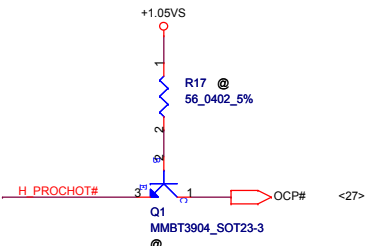
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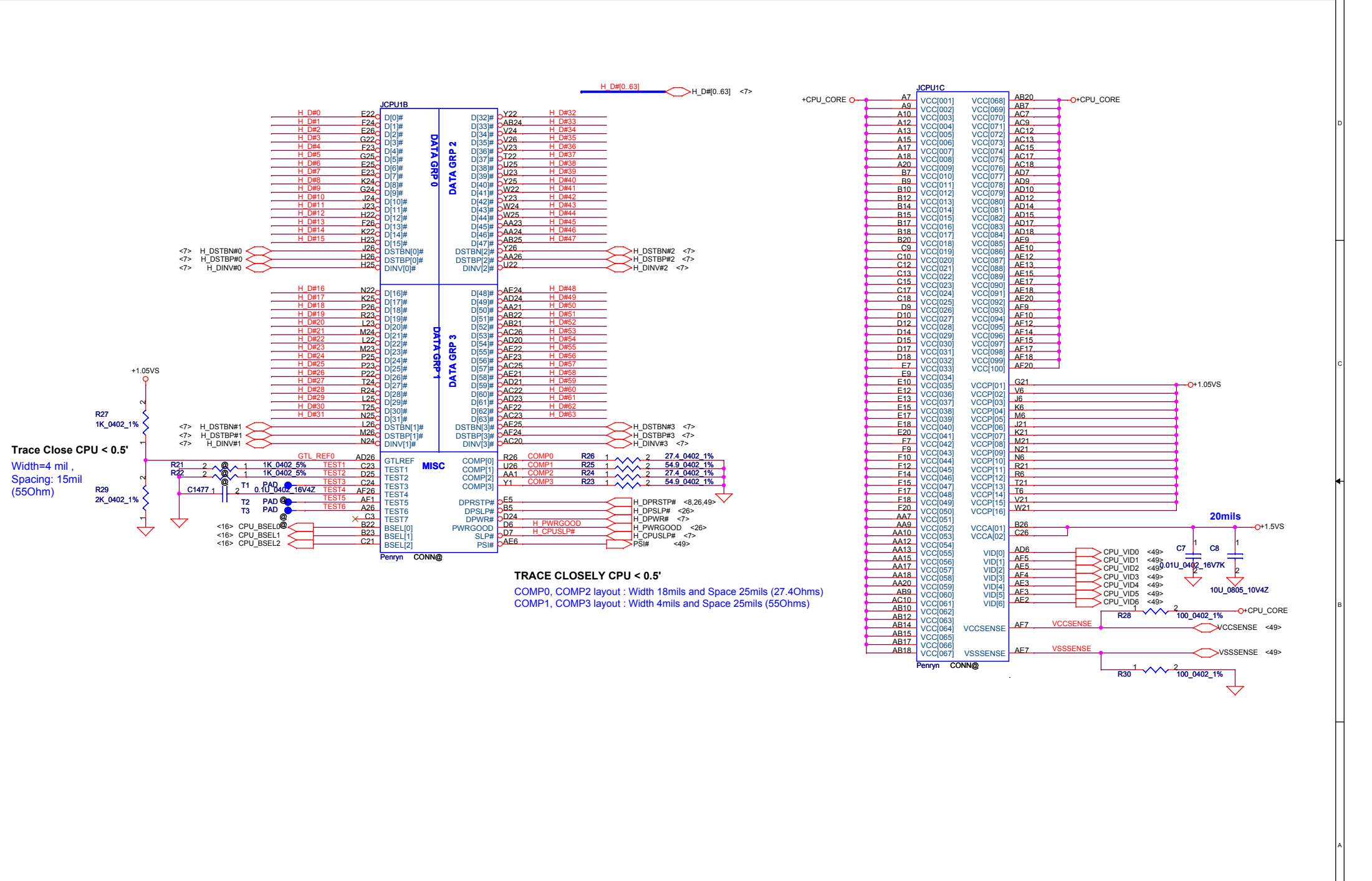


Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166





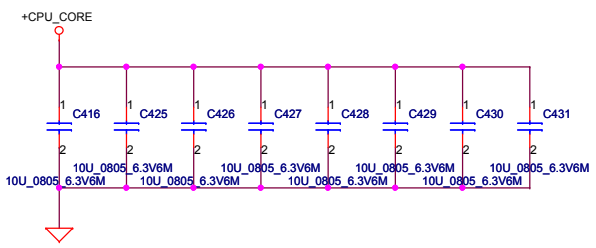
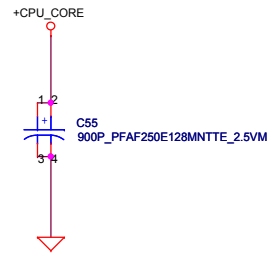
Trace Close CPU < 0.5'
 Width=4 mil,
 Spacing: 15mil
 (55Ohm)

TRACE CLOSELY CPU < 0.5'
 COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
 COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

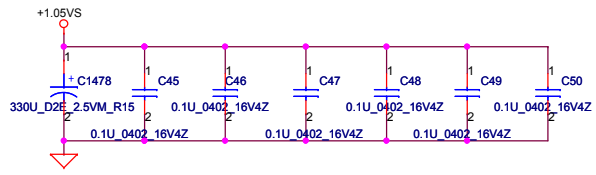
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JCPU1D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
F3	VSS[081]	VSS[162]
		VSS[163]

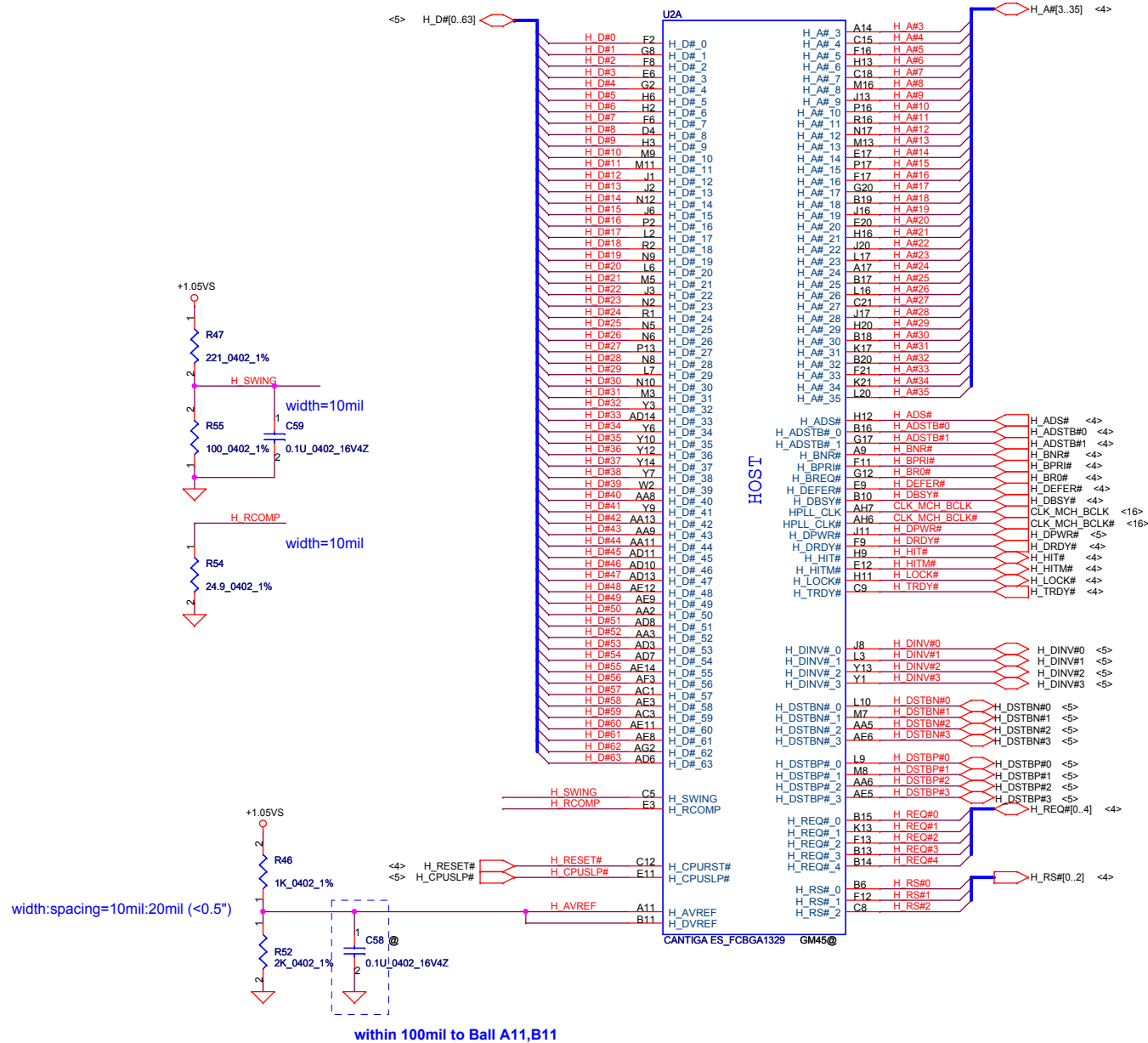
Penryn CONN@



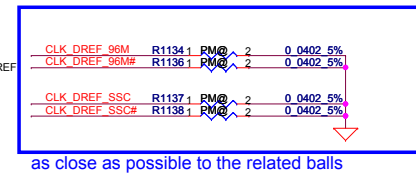
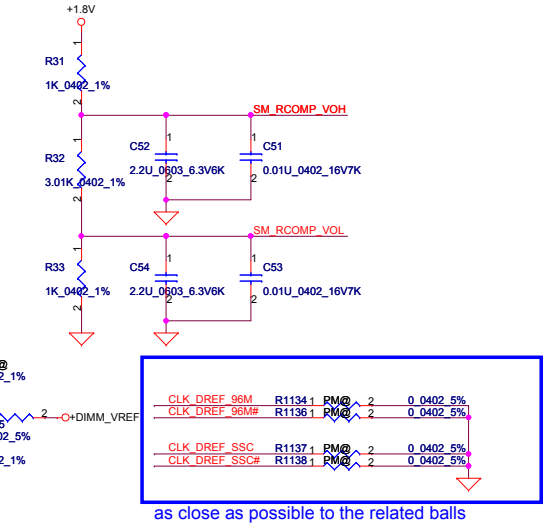
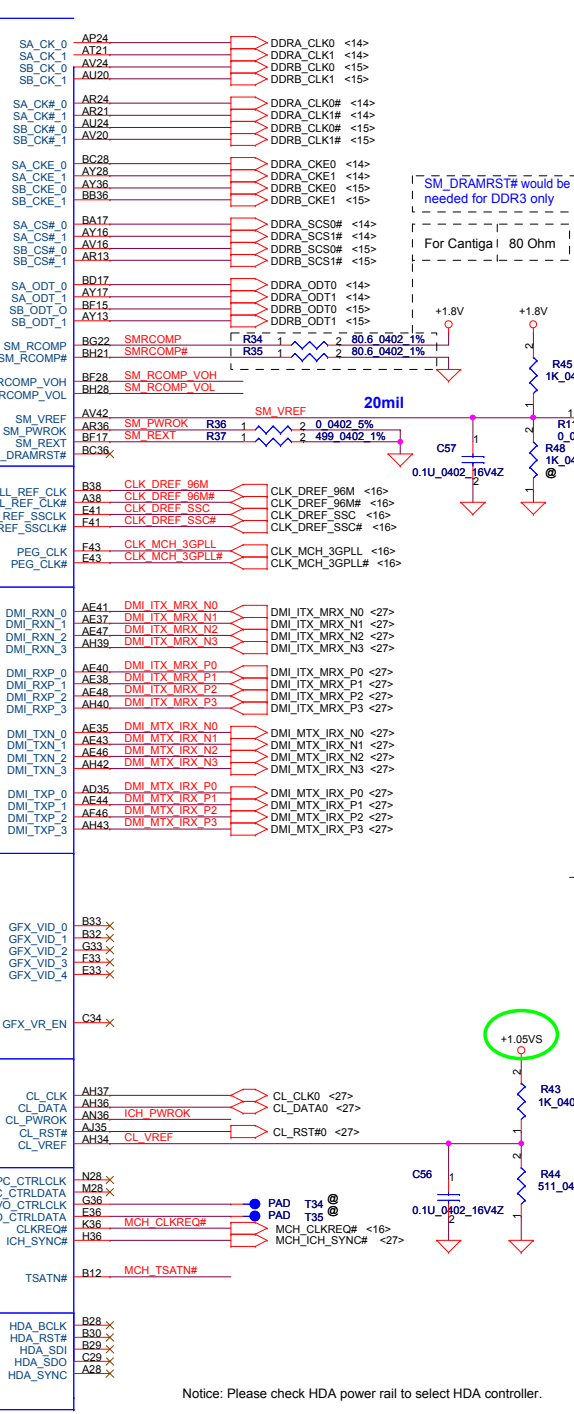
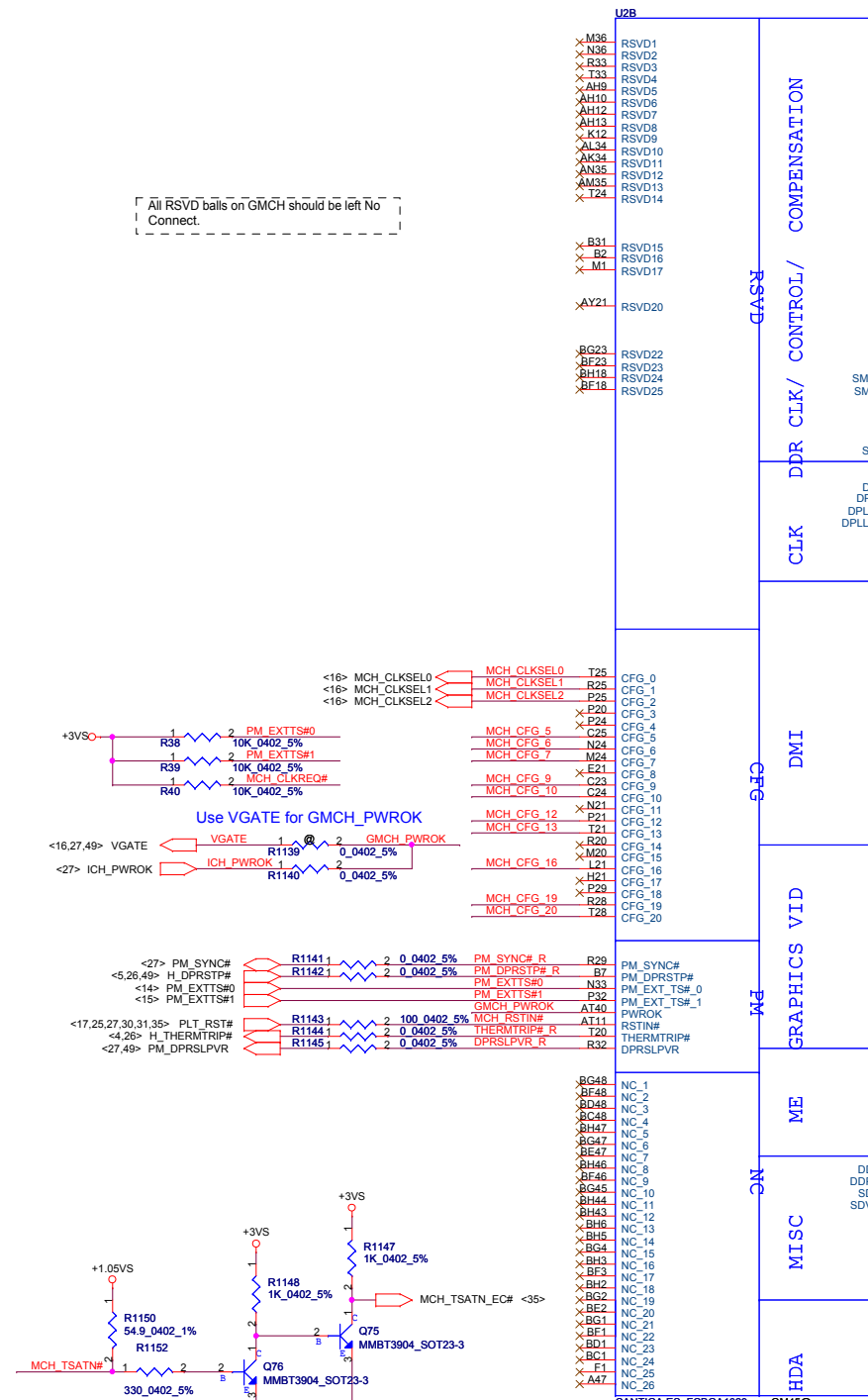
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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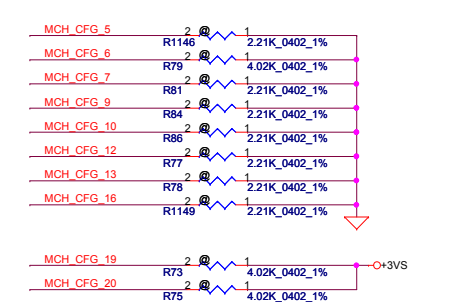
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as close as possible to the related balls

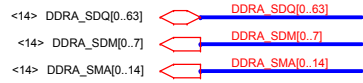
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIE Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIE disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

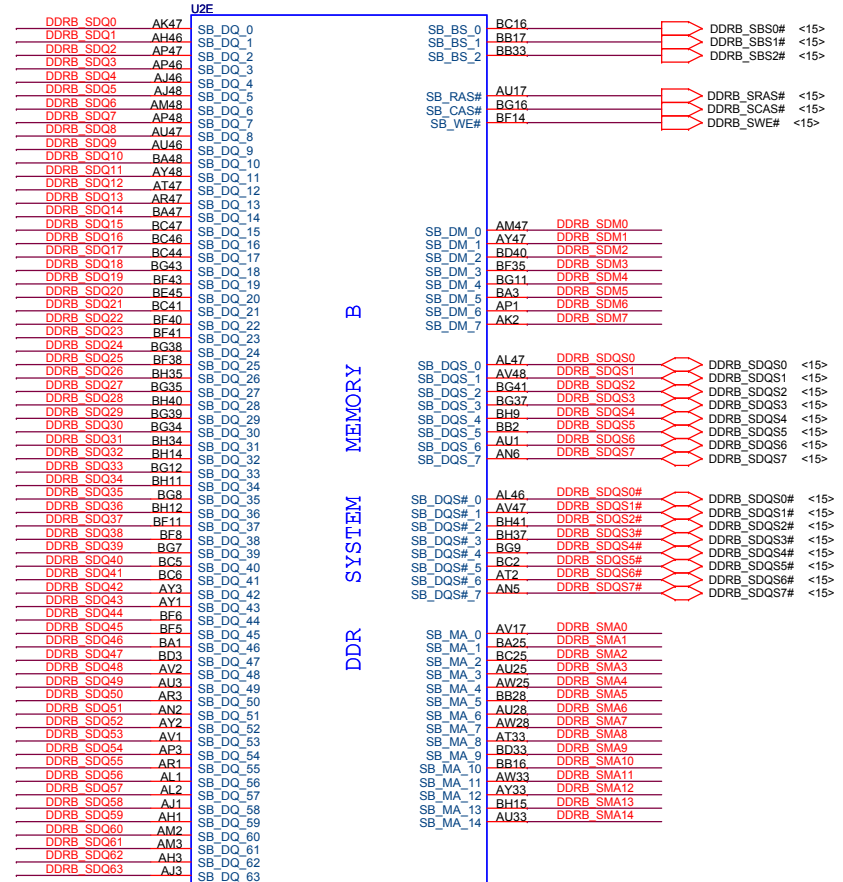


Notice: Please check HDA power rail to select HDA controller.

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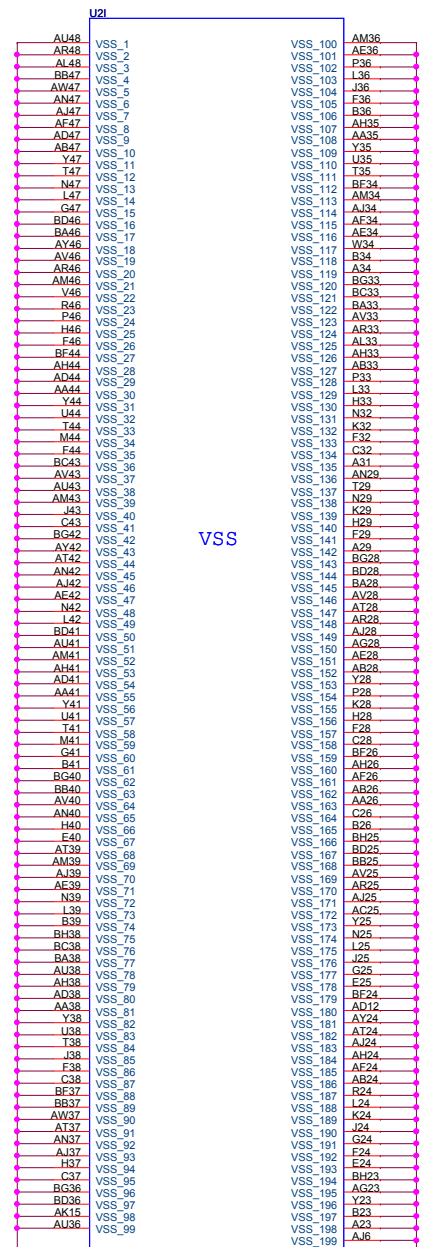


CANTIGA_ES_FCBGA1329 GM45@



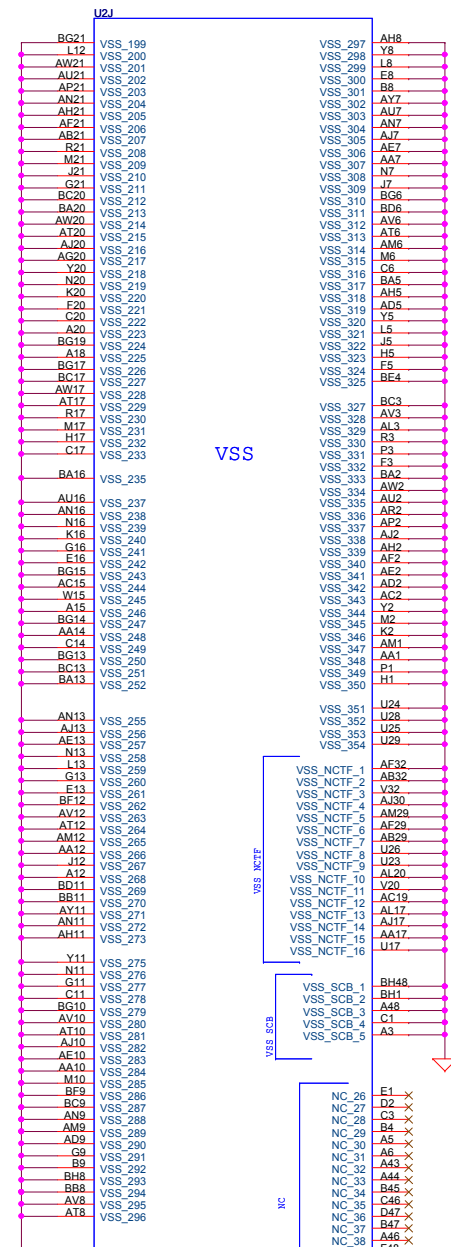
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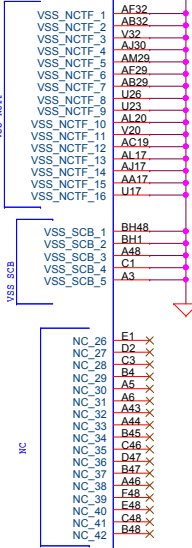
VSS

CANTIGA ES_FCBGA1329
GM45@



VSS

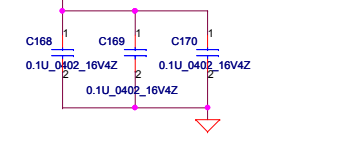
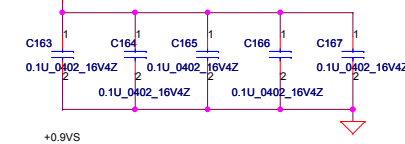
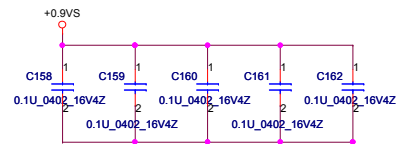
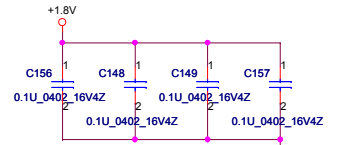
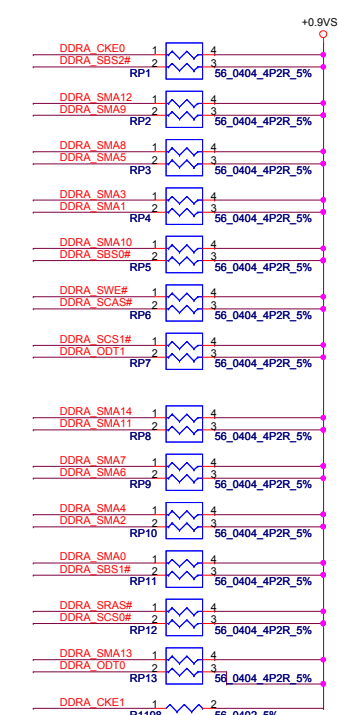
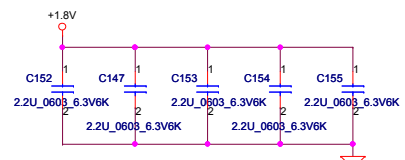
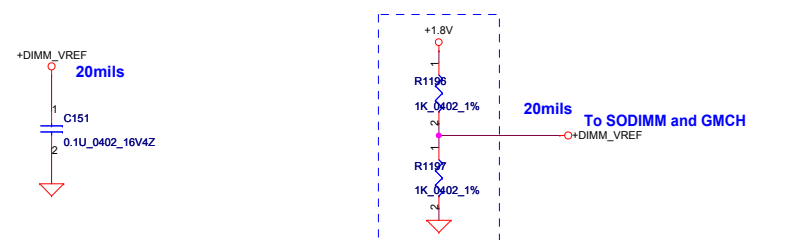
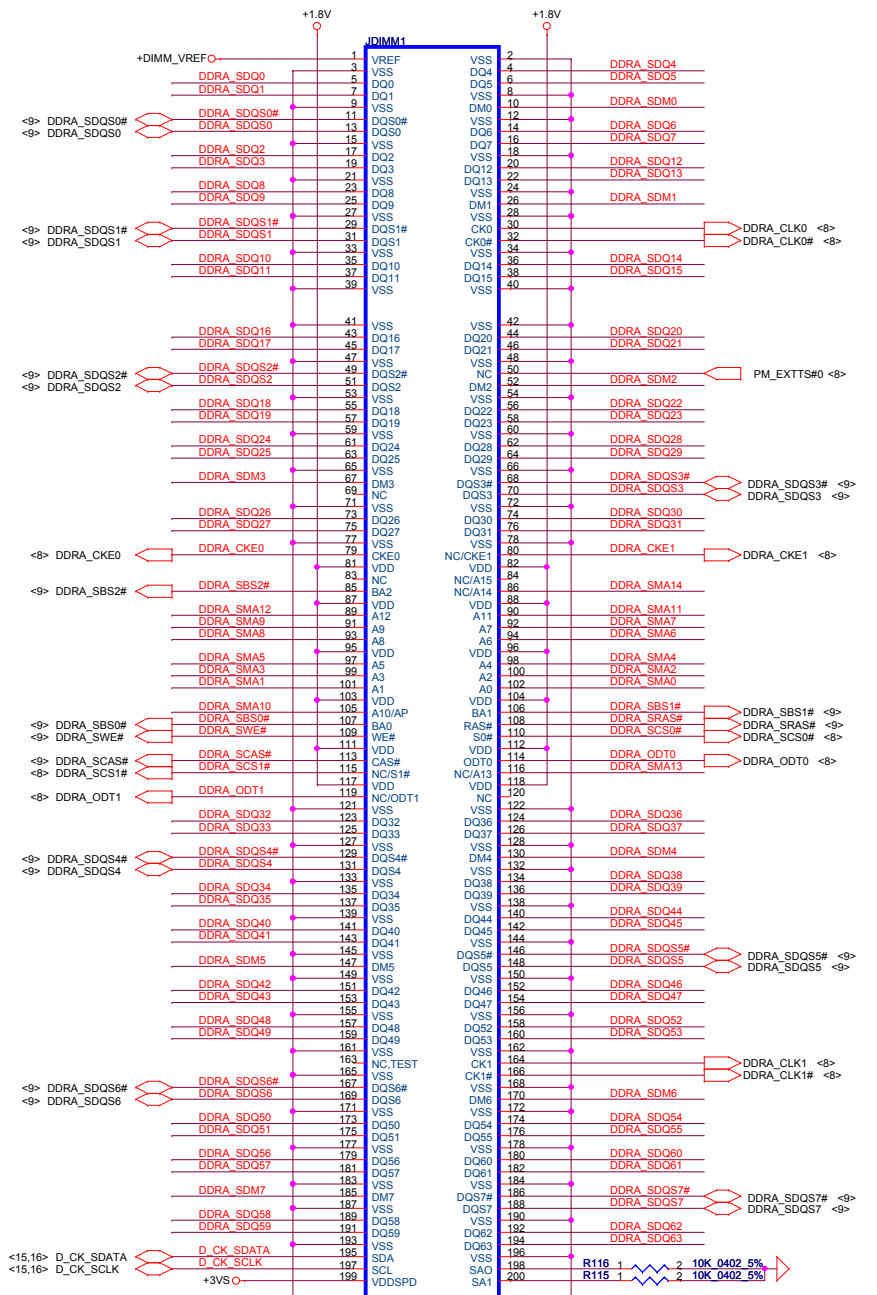
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GM45@



NC

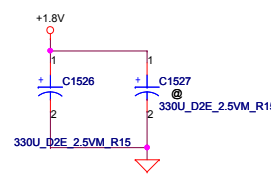
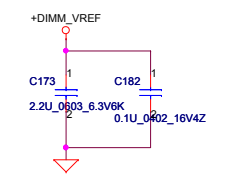
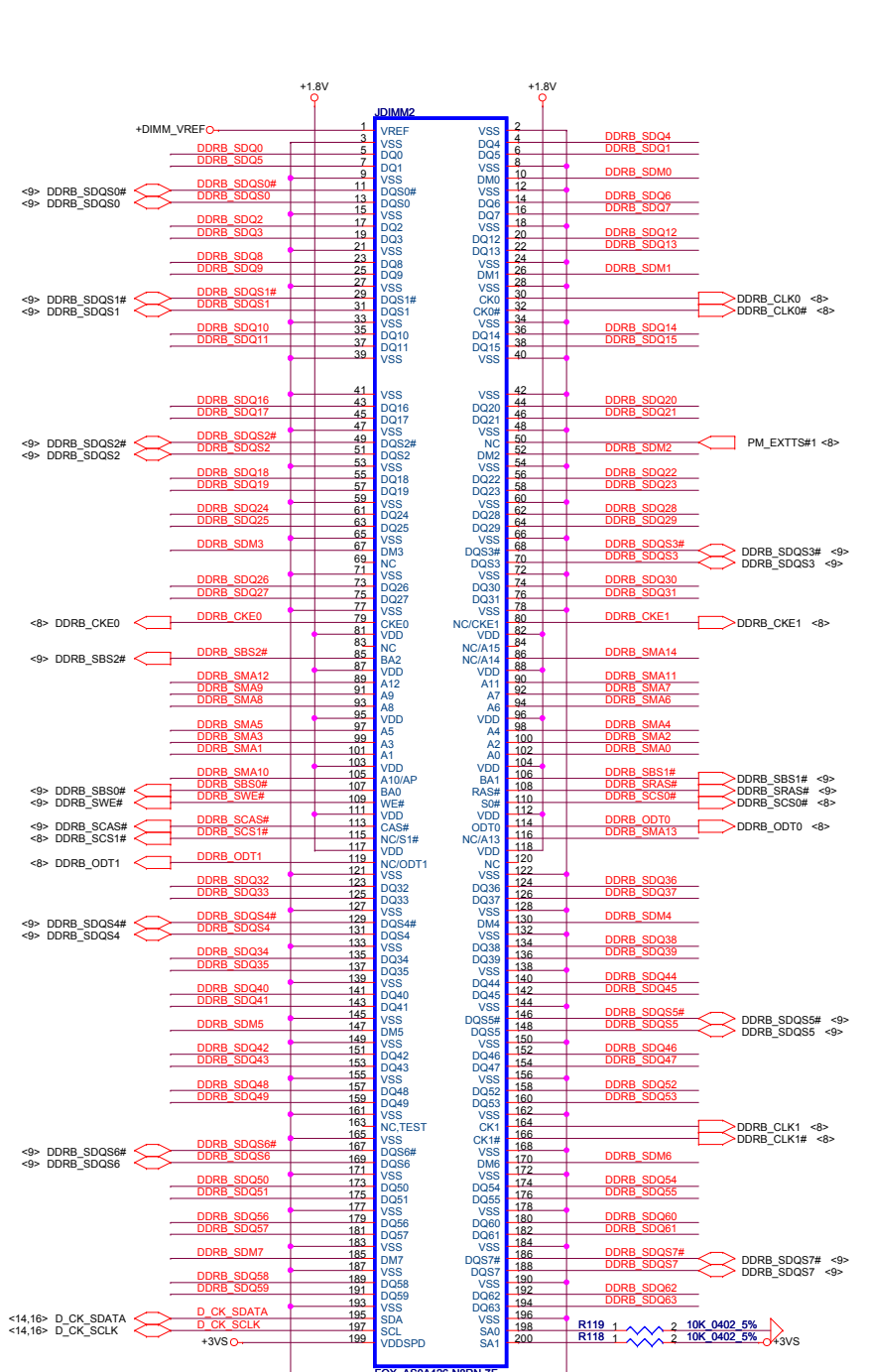
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Issued Date	2008/11/10	Deciphered Date
		2008/11/17
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Compal Electronics, Inc.			
Title Cantiga GMCH(1/7)-GTL			
Size	Document Number	Rev	
Customer	KAL90KALH0	0.2	
Date:	Thursday, November 20, 2008	Sheet	13 of 52

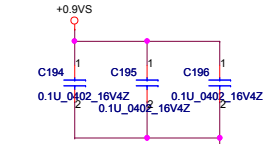
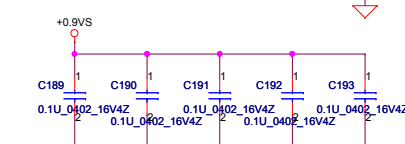
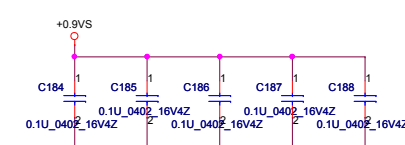
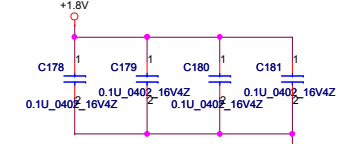
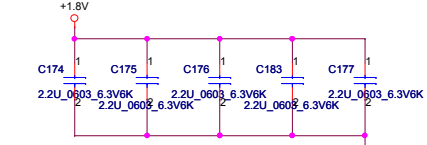
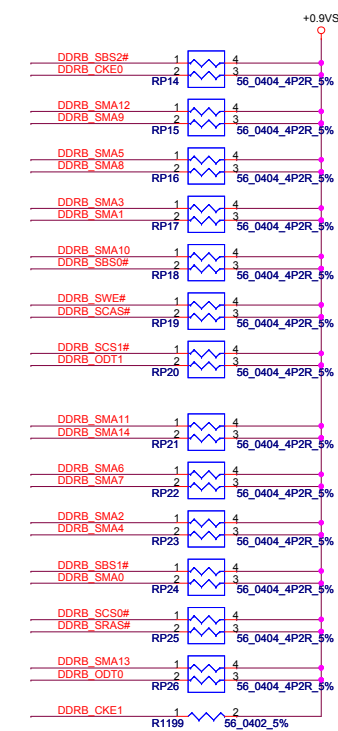


DIMM0 REV H:10.1mm (BOT)

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title		
				DDRII-SODIMMO		
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				Date:	Thursday, November 20, 2008	Sheet 14 of 52



- <-> DDRB_SMA[0..14] <-> DDRB_SMA[0..14]
- <-> DDRB_SDQ[0..63] <-> DDRB_SDQ[0..63]
- <-> DDRB_SDM[0..7] <-> DDRB_SDM[0..7]

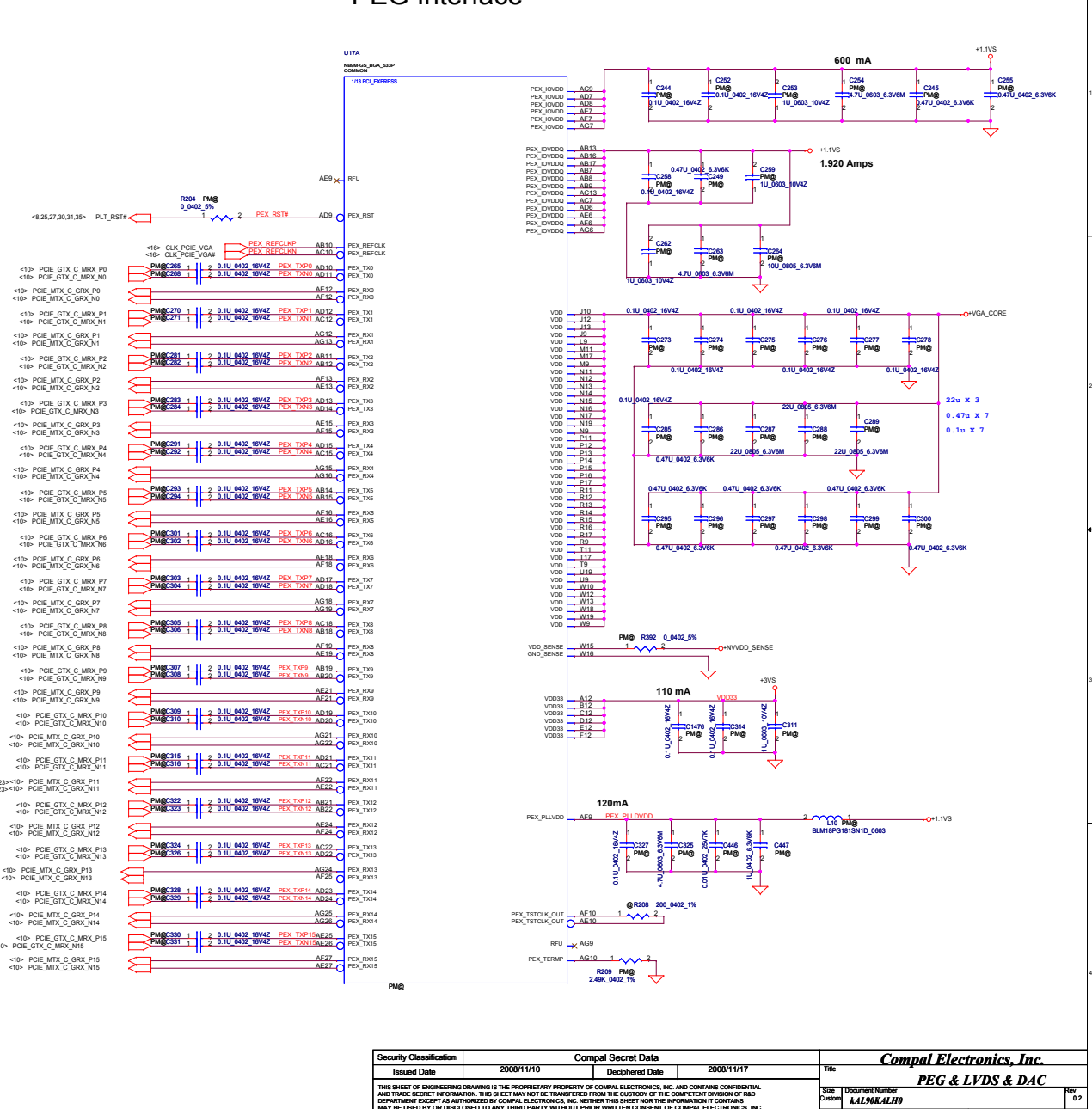
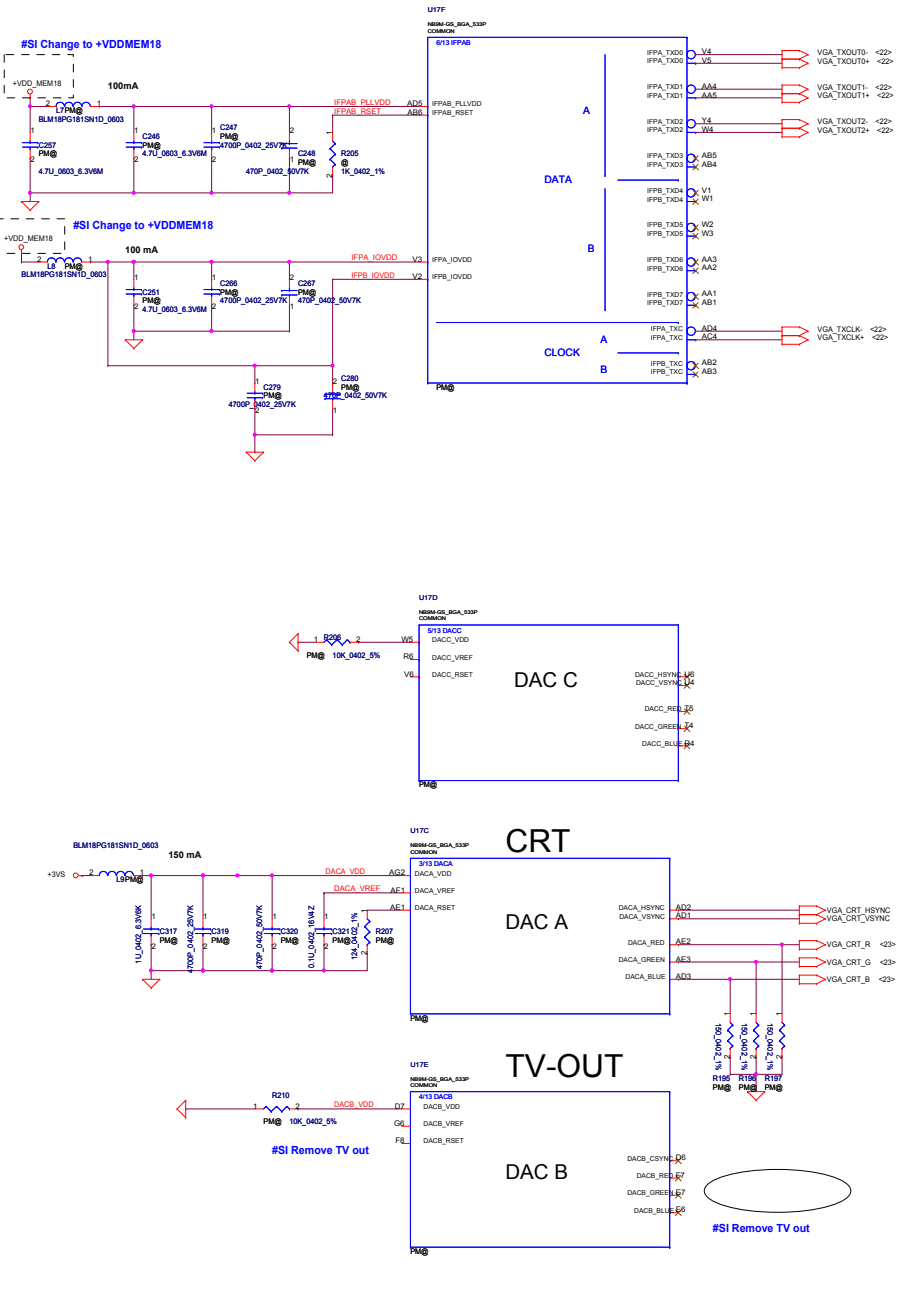


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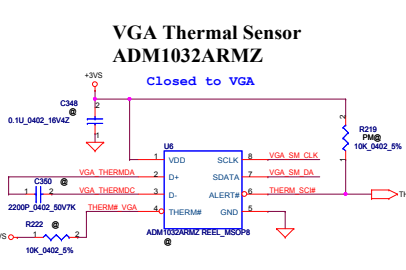
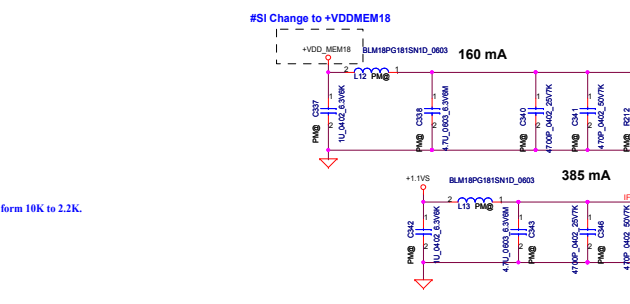
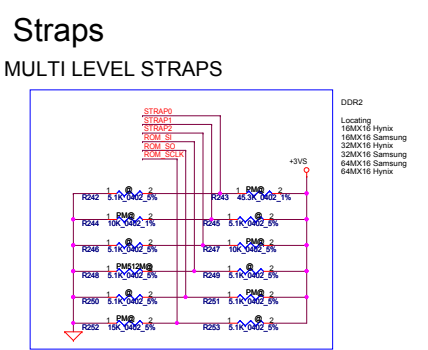
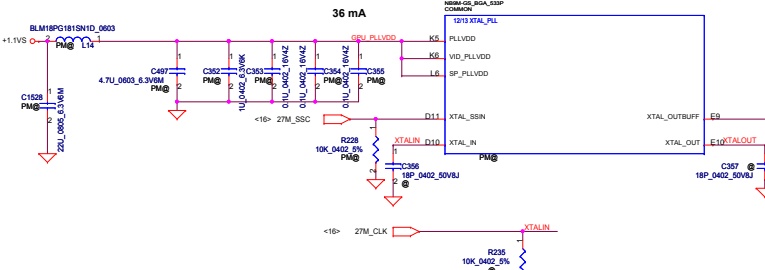
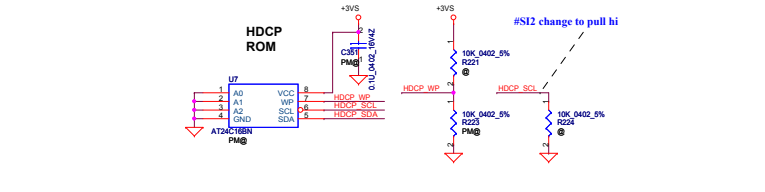
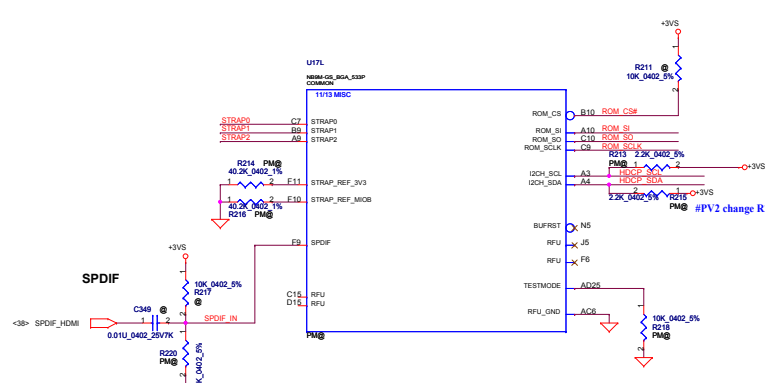
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				Date:	Thursday, November 20, 2008	Sheet 15 of 52

LVDS & DAC Interface

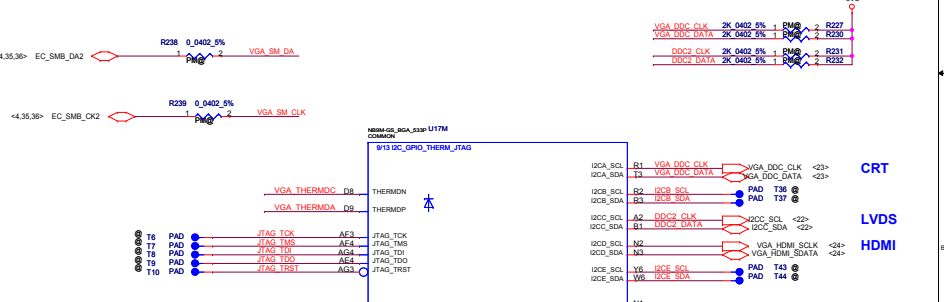
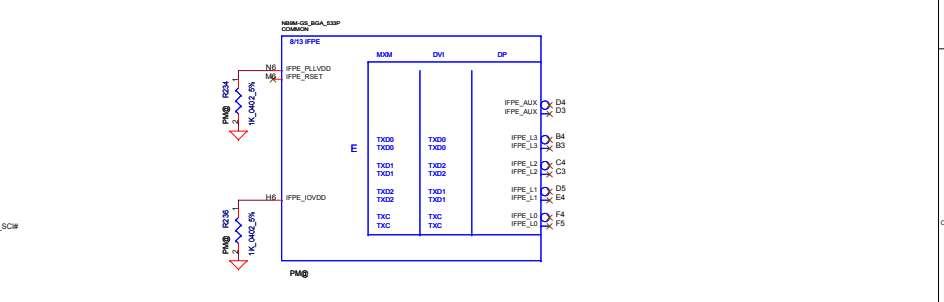
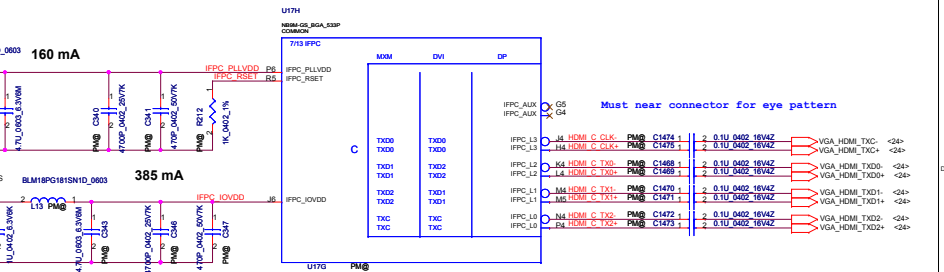
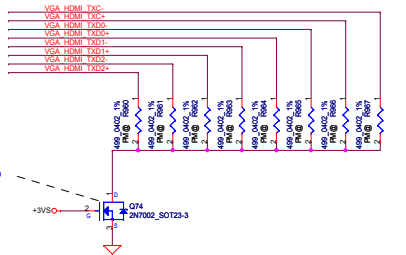
PEG Interface



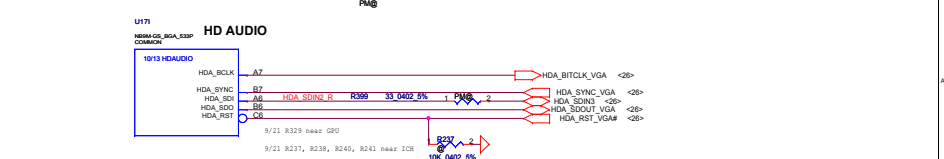
Security Classification	Compal Secret Data		Title	
Issued Date	2008/11/10	Deciphered Date	2008/11/17	File
				PEG & LVDS & DAC
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	KAL59KALH0	02		02
Date	Thursday, November 20, 2008	Sheet	17	of
			17	02



GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



GPU_VID1	GPU_VID0	+VGA_CORE
0	0	0.9V
0	1	1.17V
1	0	unused



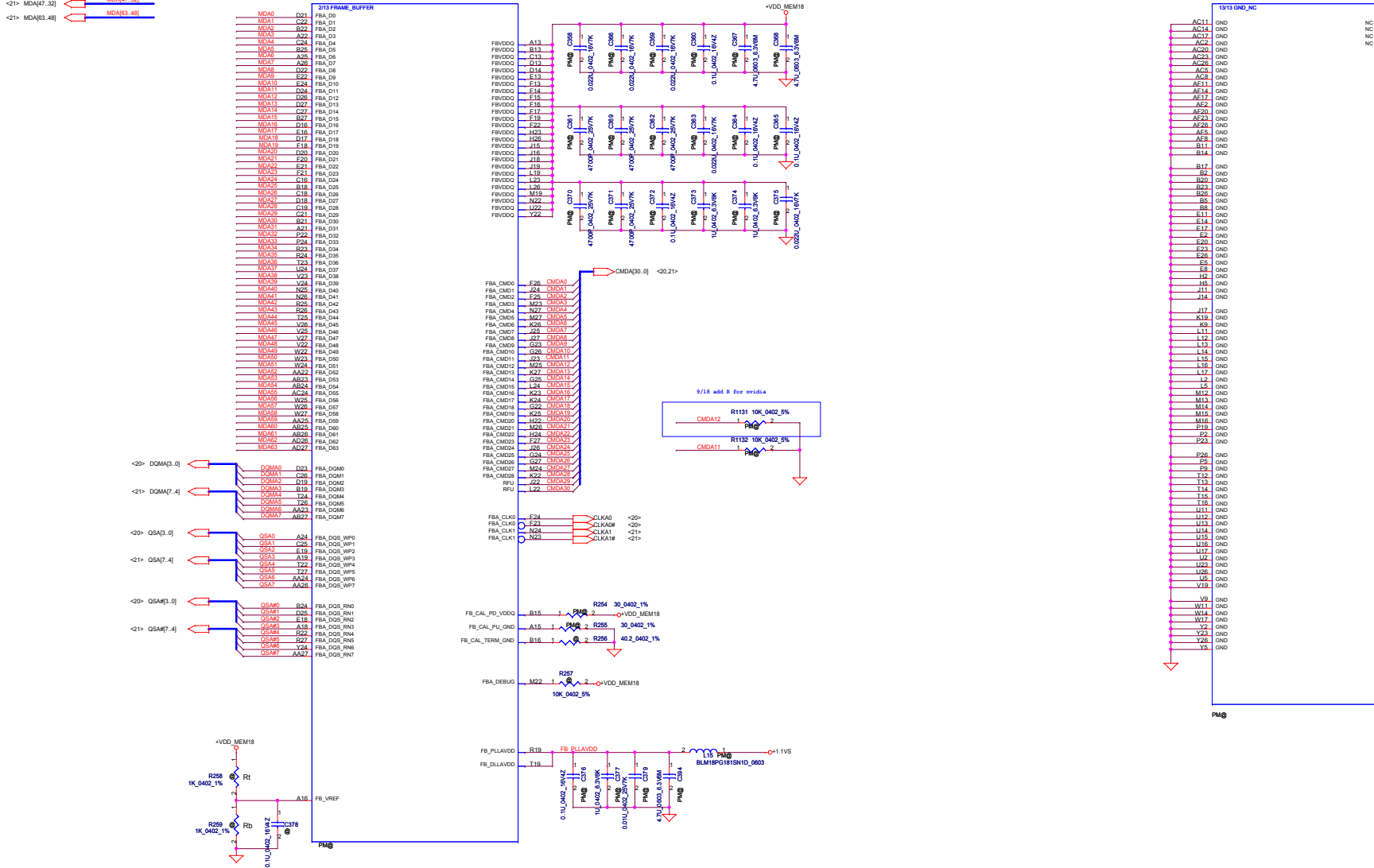
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		2008/11/10	2008/11/17			Straps & HDMI

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Author: MALAKALHO
Date: Thursday, November 20, 2008 | Sheet: 18 of 62

VRAM Interface

- <20> MDA[15..0] ← MDA15_01
- <20> MDA[31..16] ← MDA31_16
- <21> MDA[47..32] ← MDA47_32
- <21> MDA[63..48] ← MDA63_48



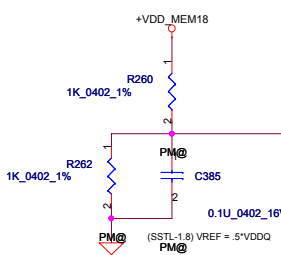
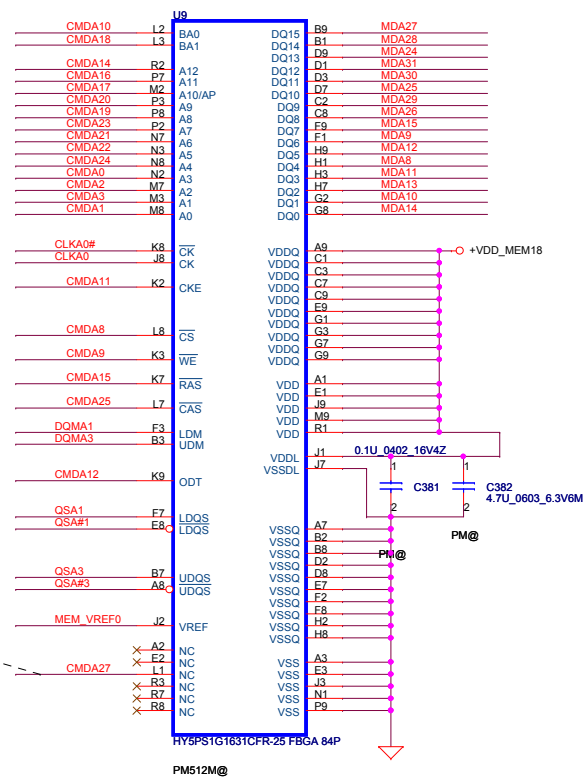
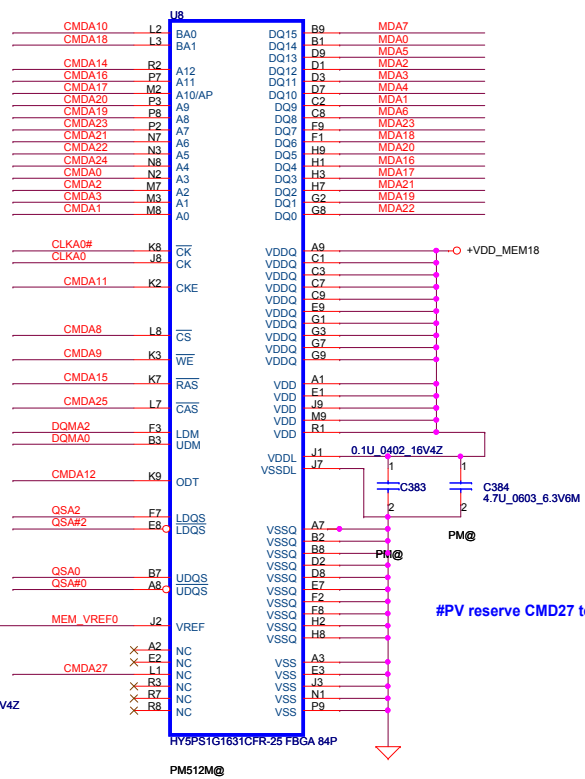
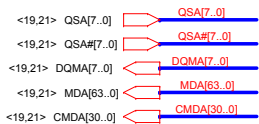
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2008/11/10	Deciphered Date	2008/11/17	VRAM / GND
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Size	Document Number	Page		0.2
Custom	KAL90KALHO	Date		Thursday, November 20, 2008 19 of 62

VRAM DDR2 chips (256MB & 512MB)

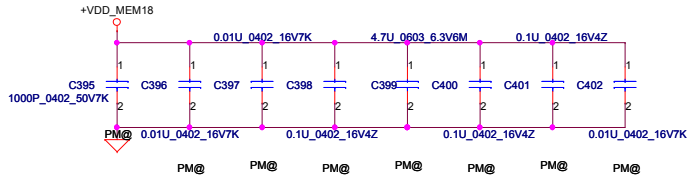
32Mx16 DDR2 400MHz *4==>256MB

64Mx16 DDR2 400MHz*4==>512MB

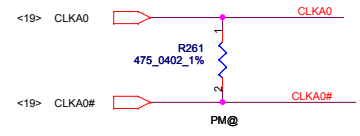
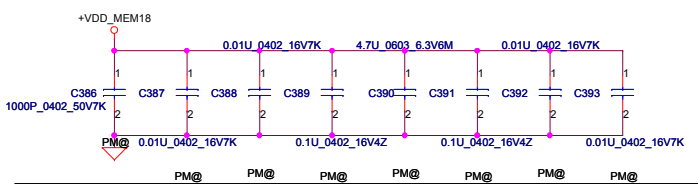
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CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



DDR2 BGA MEMORY



DDR BGA MEMORY



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Date: Thursday, November 20, 2008				Rev 0.1
Sheet 7 of 16				

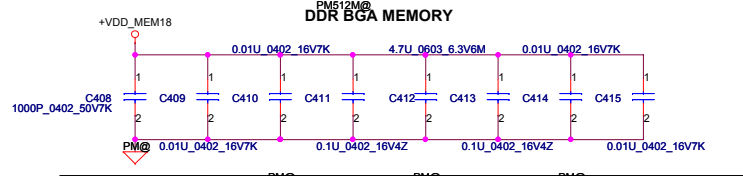
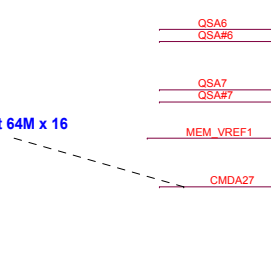
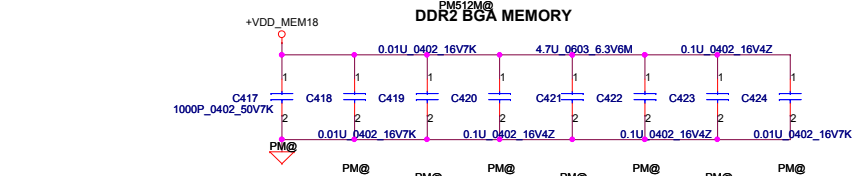
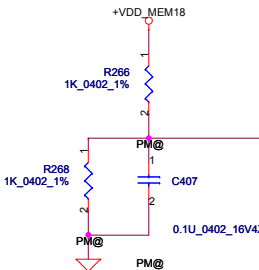
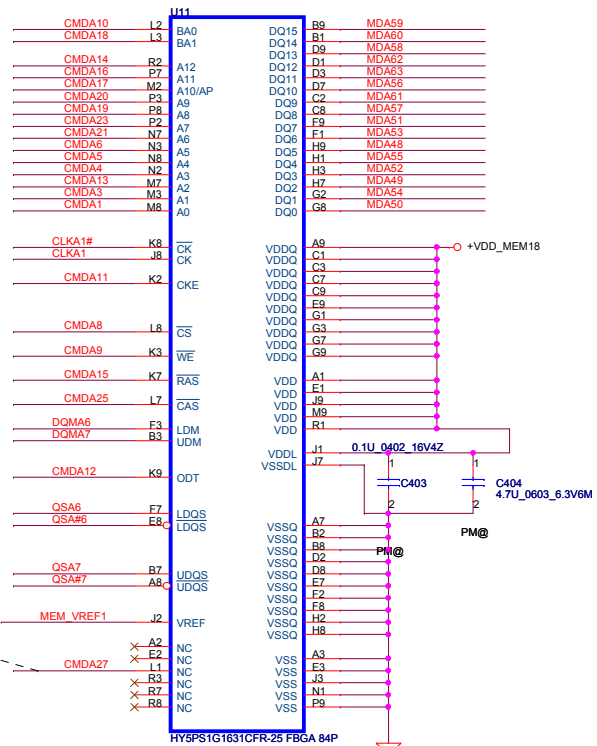
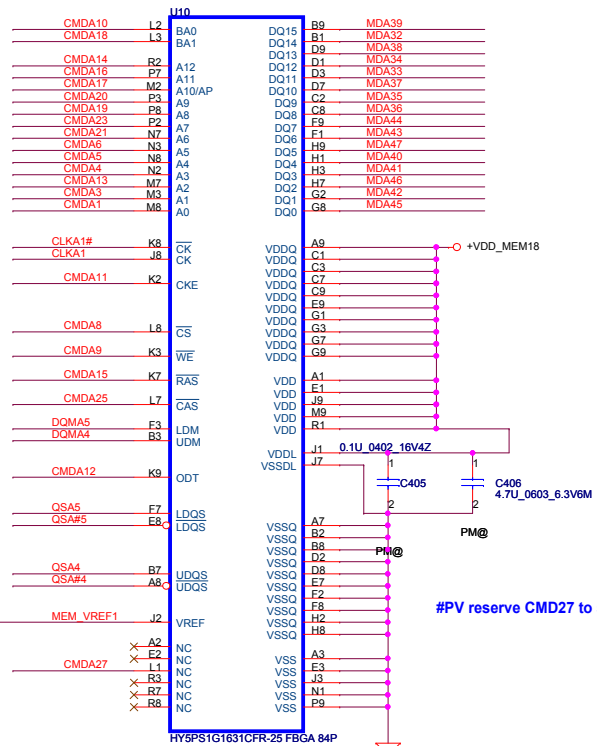
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

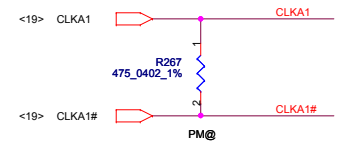
64Mx16 DDR2 400MHz*4==>512MB

Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

- <19,20> DQMA[7..0] ← DQMA[7..0]
- <19,20> CMDA[30..0] ← CMDA[30..0]
- <19,20> QSA#[7..0] ← QSA[7..0]
- <19,20> QSA[7..0] ← QSA[7..0]
- <19,20> MDA[63..0] ← MDA[63..0]

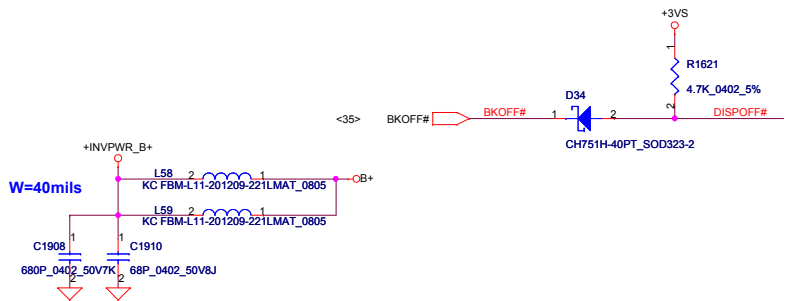
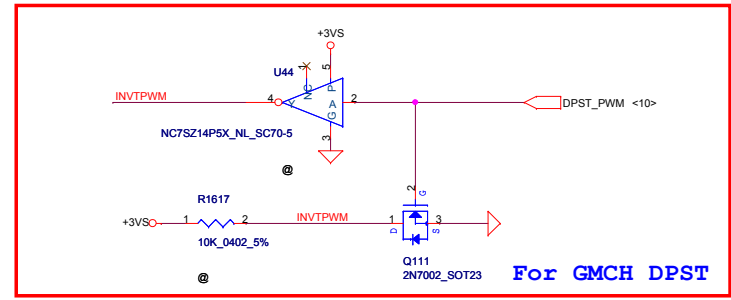
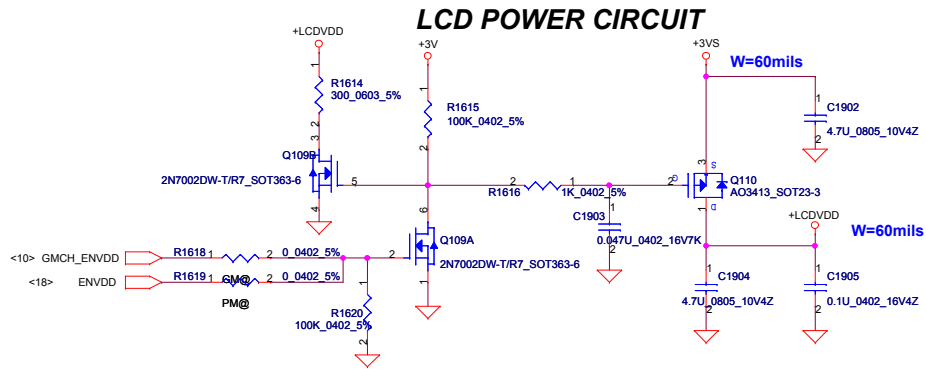


#PV reserve CMD27 to suport 64M x 16

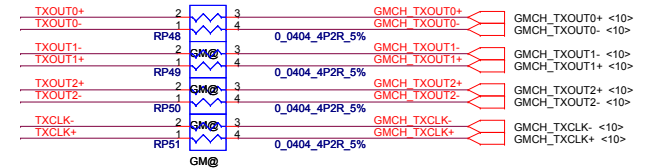
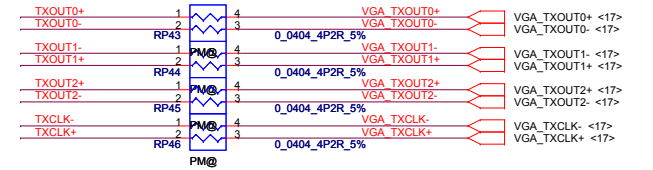
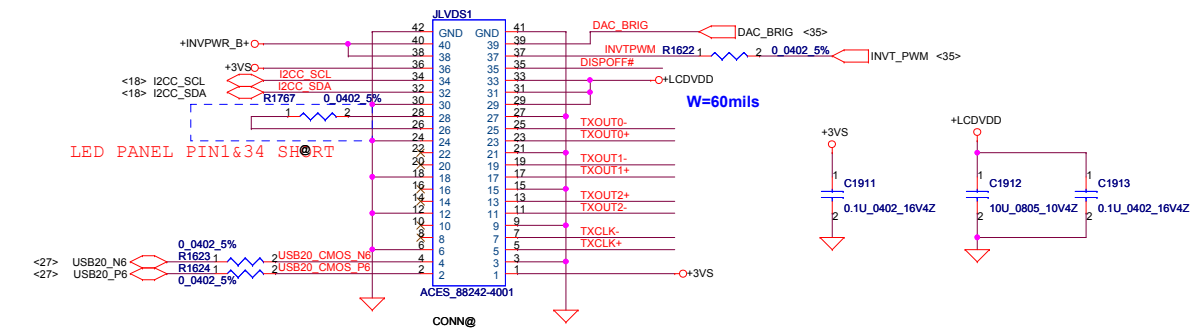


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Issued Date	2008/11/10			Deciphered Date	2008/11/17			

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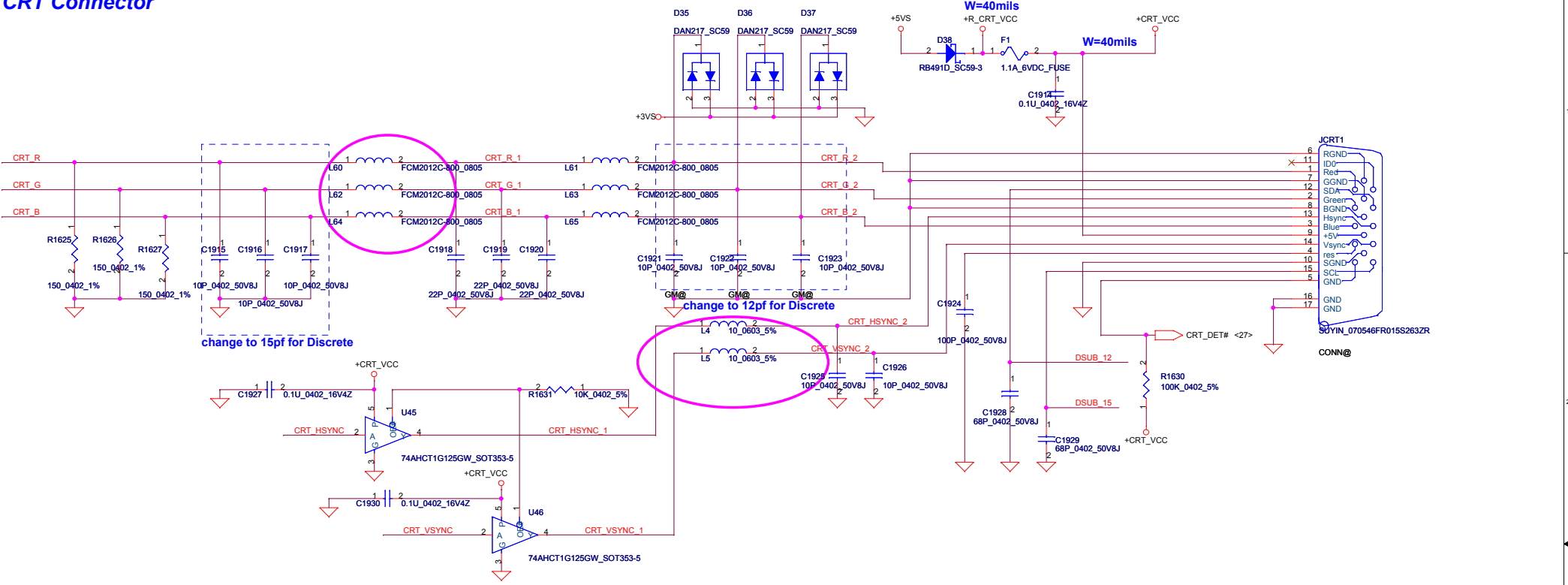


LCD/PANEL BD. Conn.

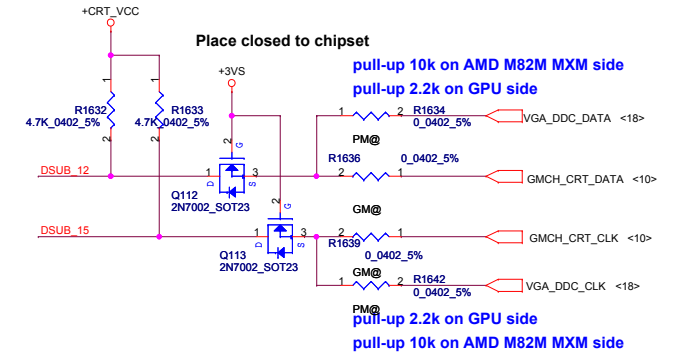


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Size	Document Number	Customer		Rev	
	KAL90KALH0	KAL90KALH0		0.2	
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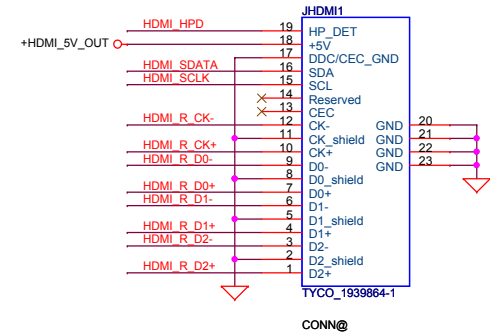
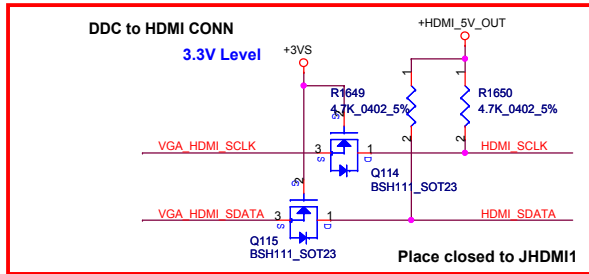
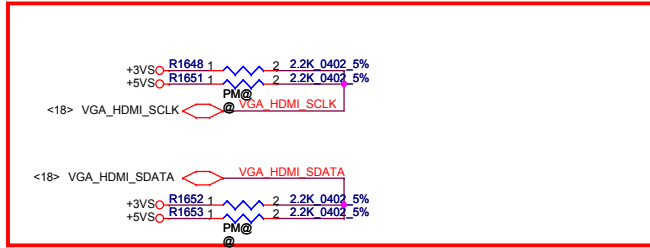
CRT Connector



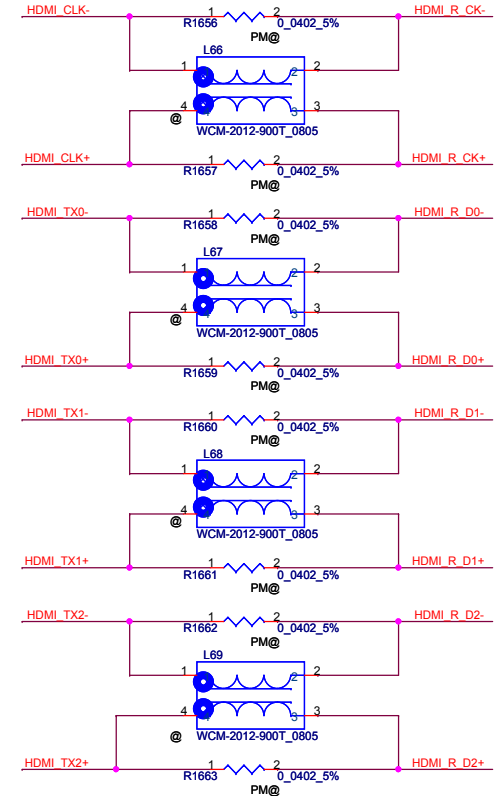
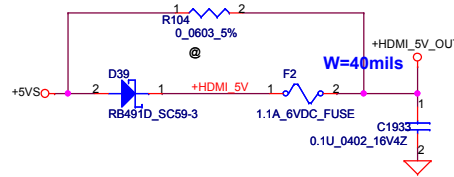
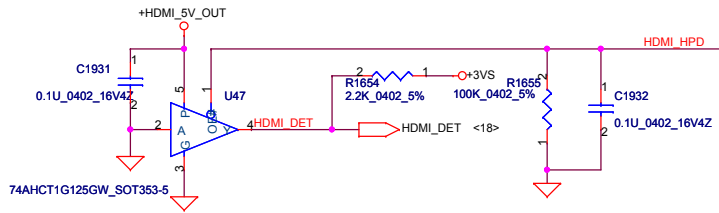
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 - <10> GMCH_CRT_HSYNC R1637 1 GM@ 2 30.1_0402_1% CRT_HSYNC
 - <10> GMCH_CRT_B R1638 1 GM@ 2 0_0402_5% CRT_B
 - <10> GMCH_CRT_G R1640 1 GM@ 2 0_0402_5% CRT_G
 - <10> GMCH_CRT_R R1641 1 GM@ 2 0_0402_5% CRT_R
- GM@
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- <17> VGA_CRT_VSYNC R1643 1 2 0_0402_5% CRT_VSYNC
 - <17> VGA_CRT_HSYNC R1644 1 PM@ 2 0_0402_5% CRT_HSYNC
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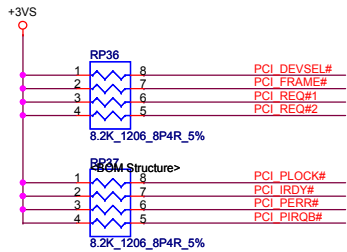
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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Size B	Document Number	Date:		Sheet	Rev
	kAL90KALH0	Thursday, November 20, 2008		23	0.2
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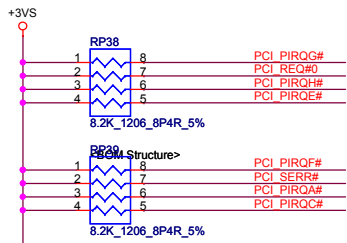
MP:Update HDMI Hot Plug DET circuit.



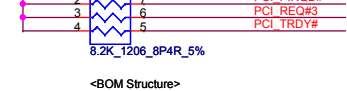
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				HDMI Connector	
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				Date	Thursday, November 20, 2008
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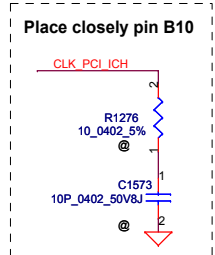
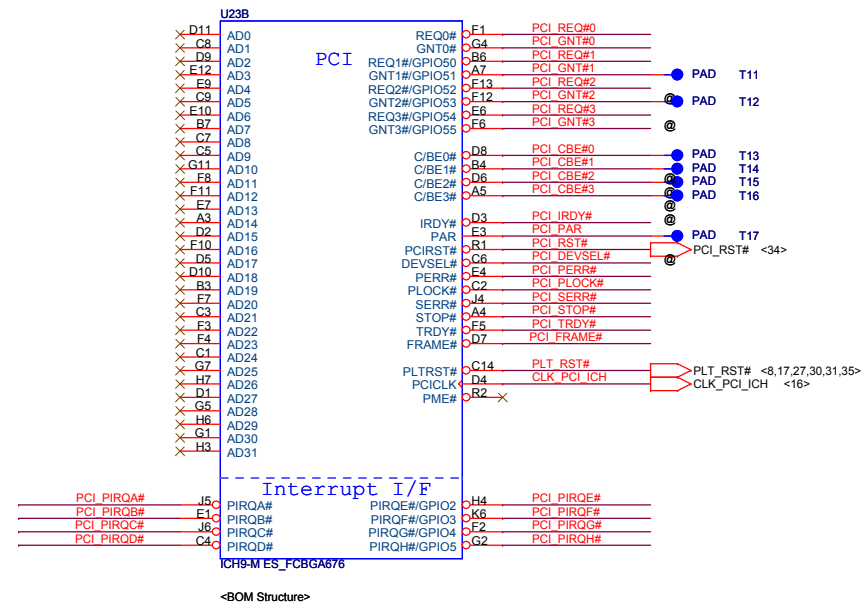


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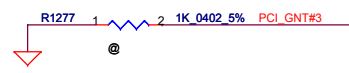


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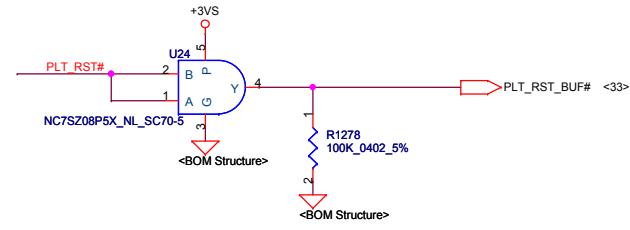
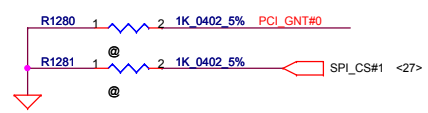
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)



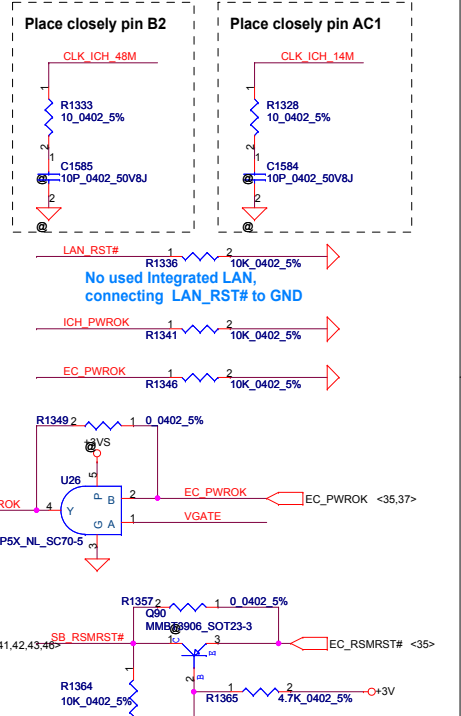
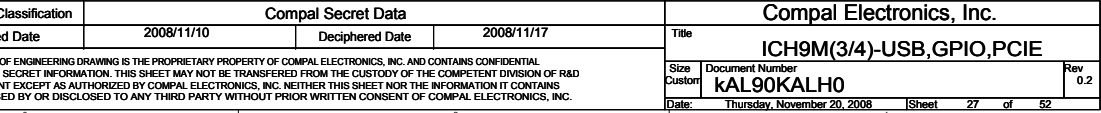
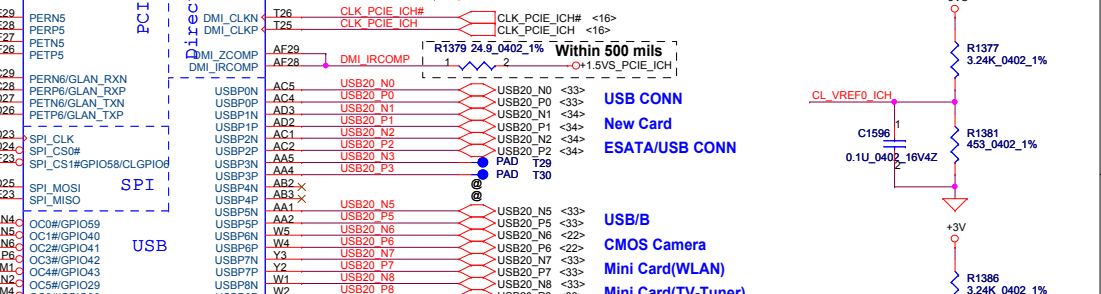
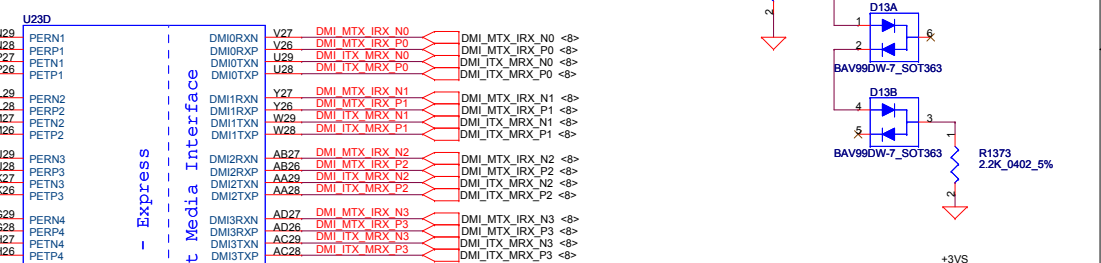
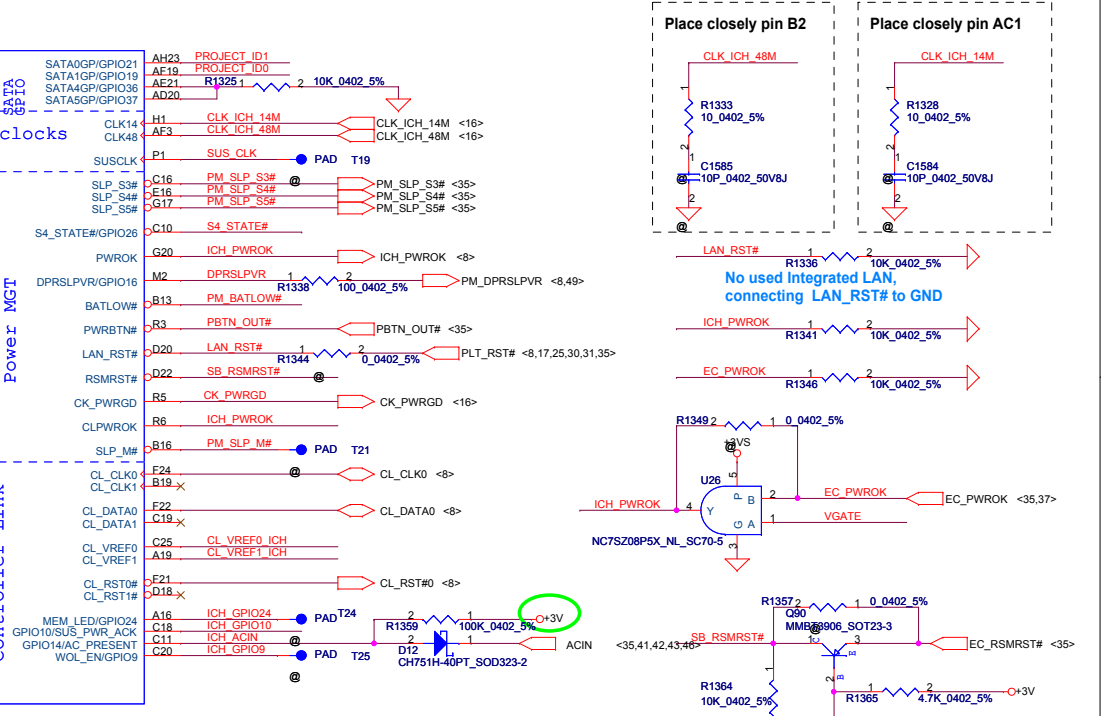
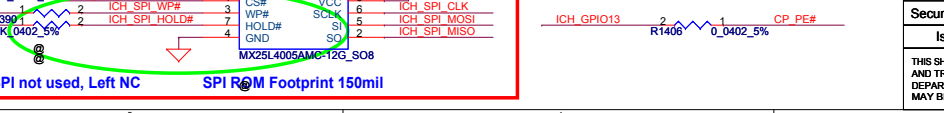
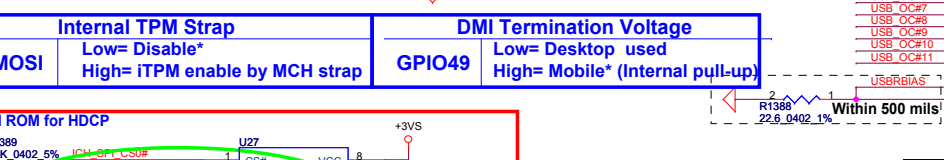
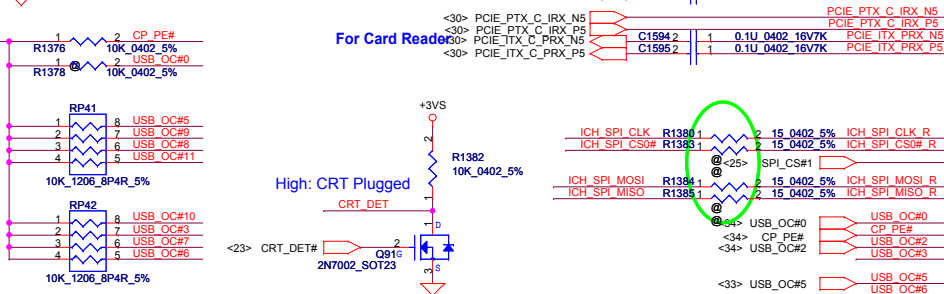
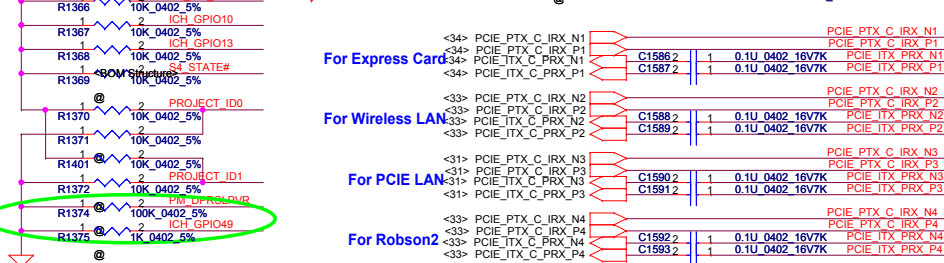
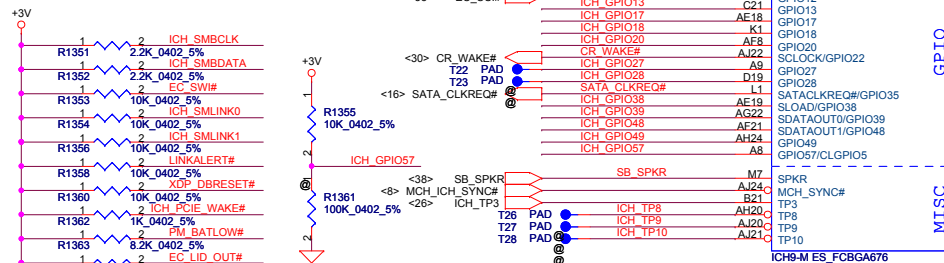
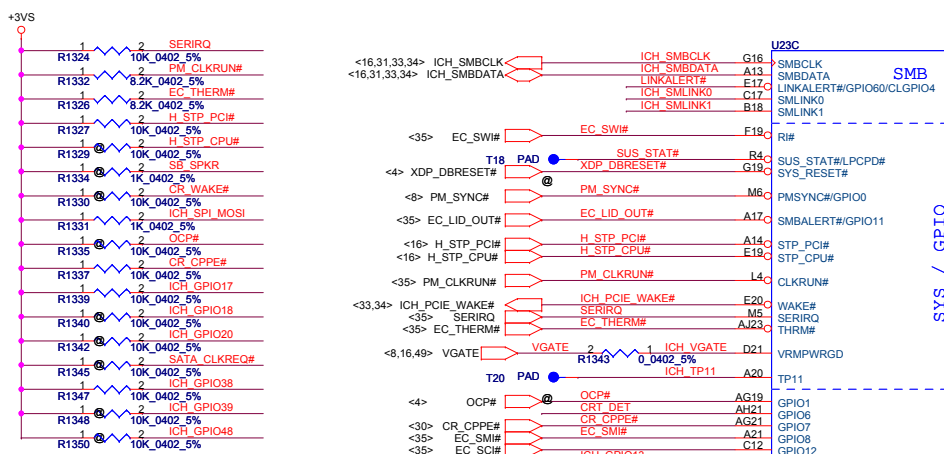
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

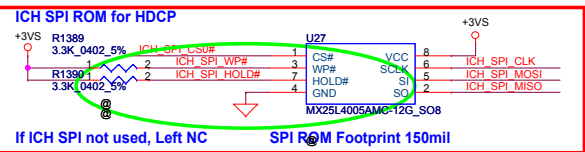


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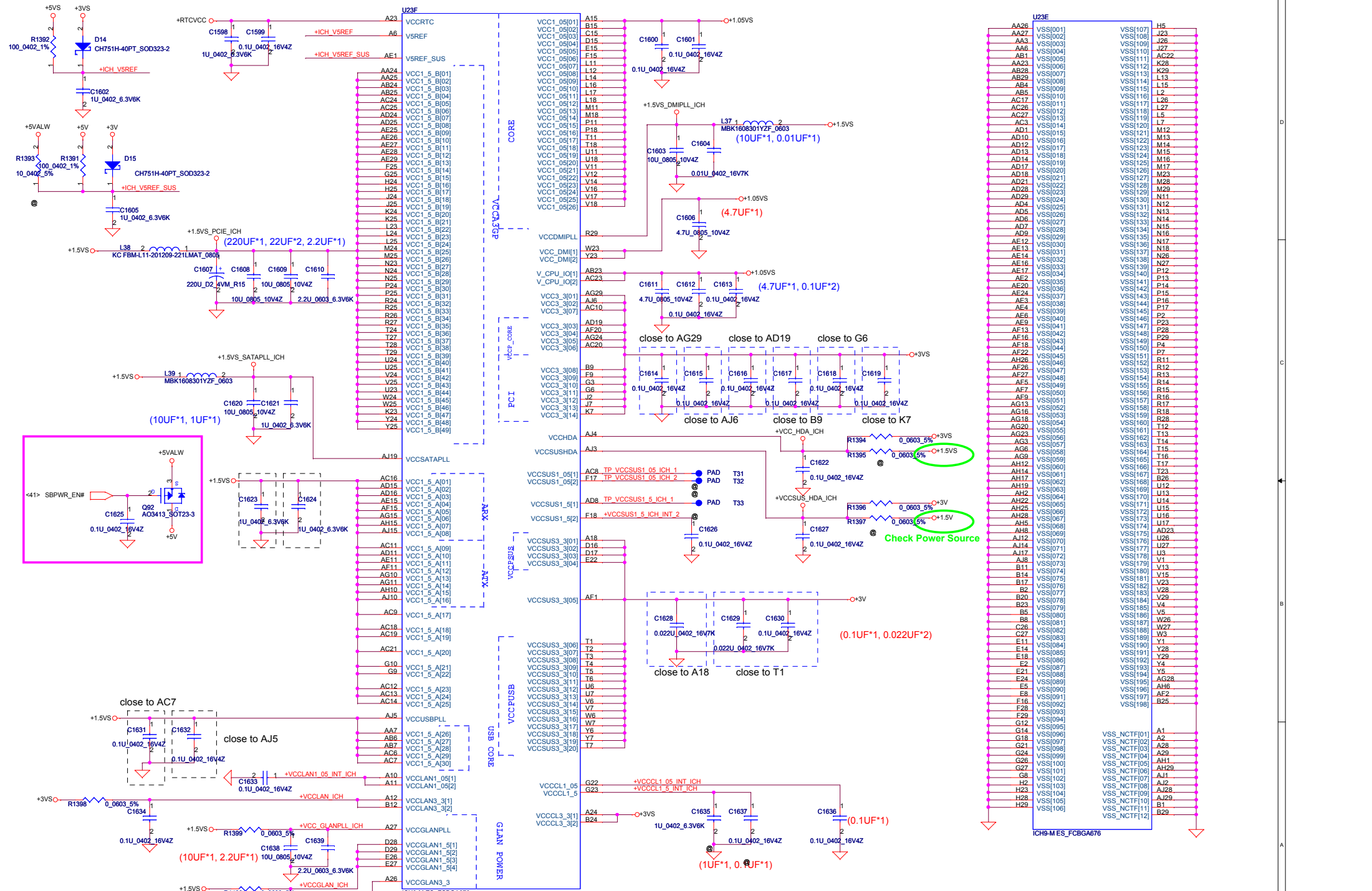
Internal TPM Strap
 Low= Disable*
 High= iTPM enable by MCH strap

DMITermination Voltage
 Low= Desktop used
 High= Mobile* (Internal pull-up)



No Reboot Strap
 Low= Default*
 High= "No Reboot"

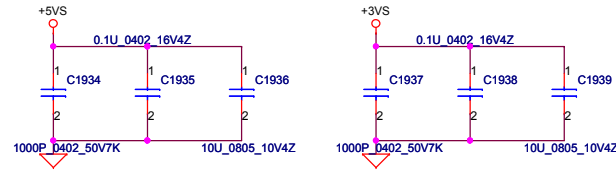
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Compal Electronics, Inc. ICH9M(3/4)-USB,GPIO,PCIE			
Size	Document	Customer	Rev
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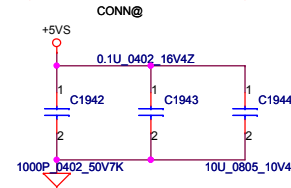
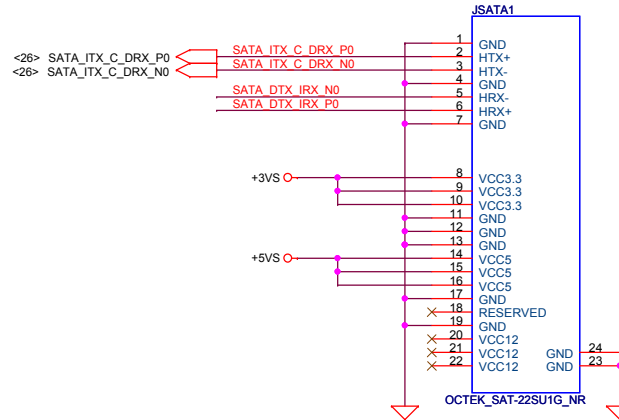
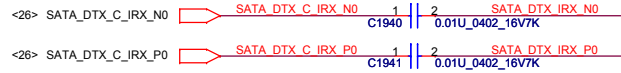
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Issued Date	2008/11/10	Deciphered Date
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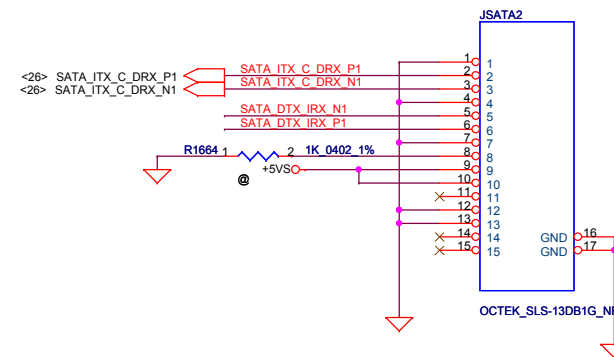
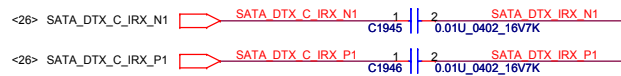
Compal Electronics, Inc.		
ICH9M(4/4)-POWER&GND		
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SATA HDD Conn.

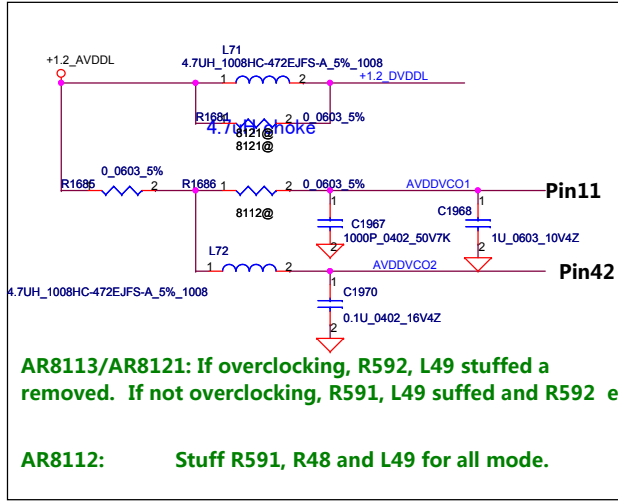
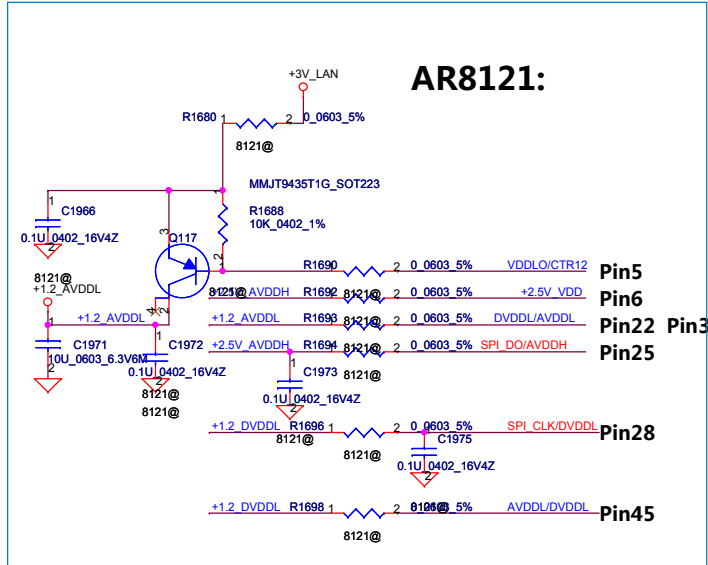


SATA ODD Conn.



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Size	Document Number	Rev		Date	
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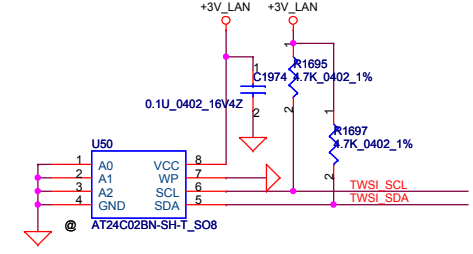
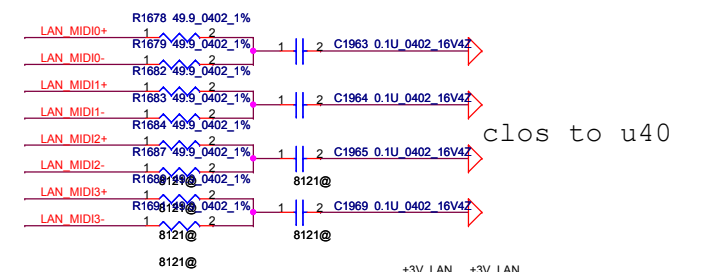
AR8121:



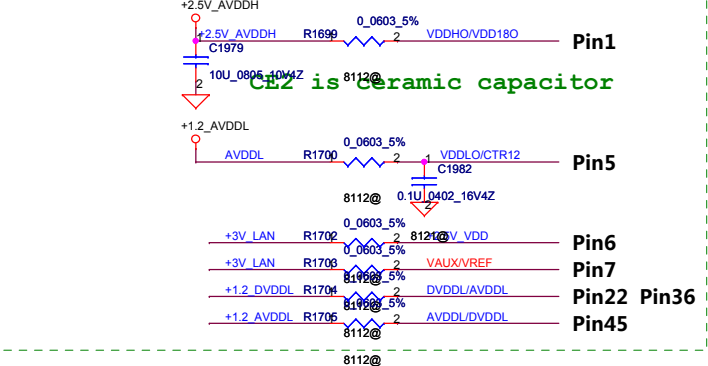
AR8113/AR8121: If overclocking, R592, L49 stuffed and removed. If not overclocking, R591, L49 stuffed and R592 removed.

AR8112: Stuff R591, R48 and L49 for all mode.

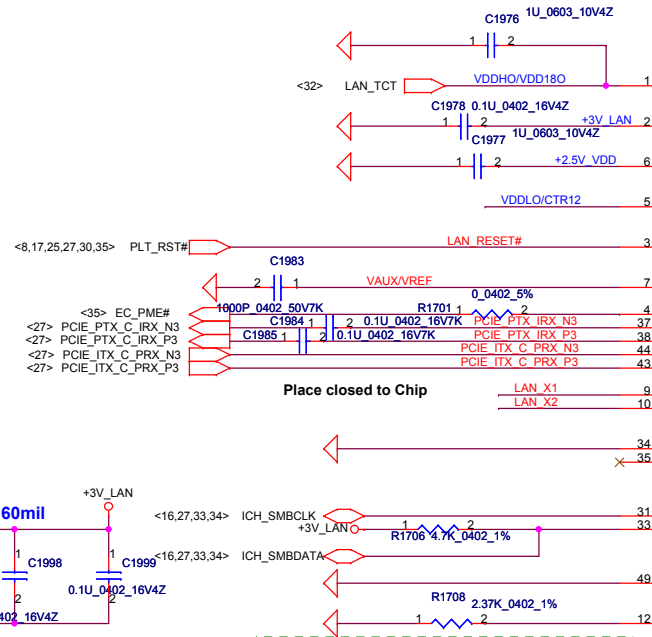
LAN AR8121/8112



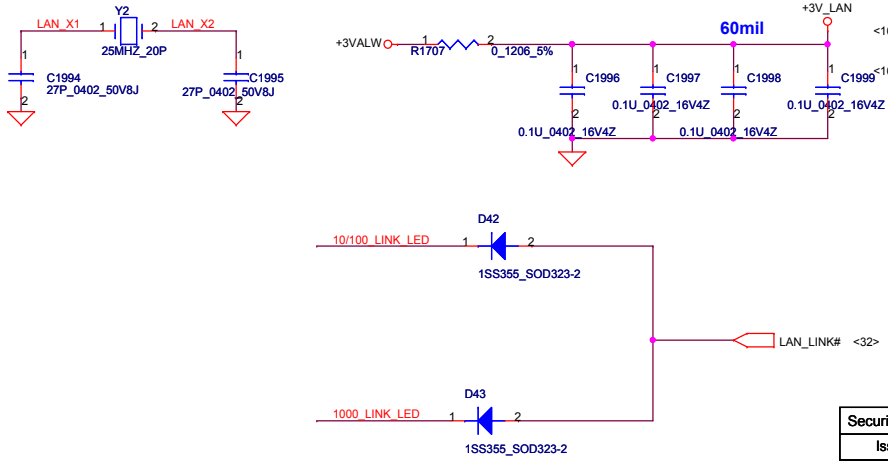
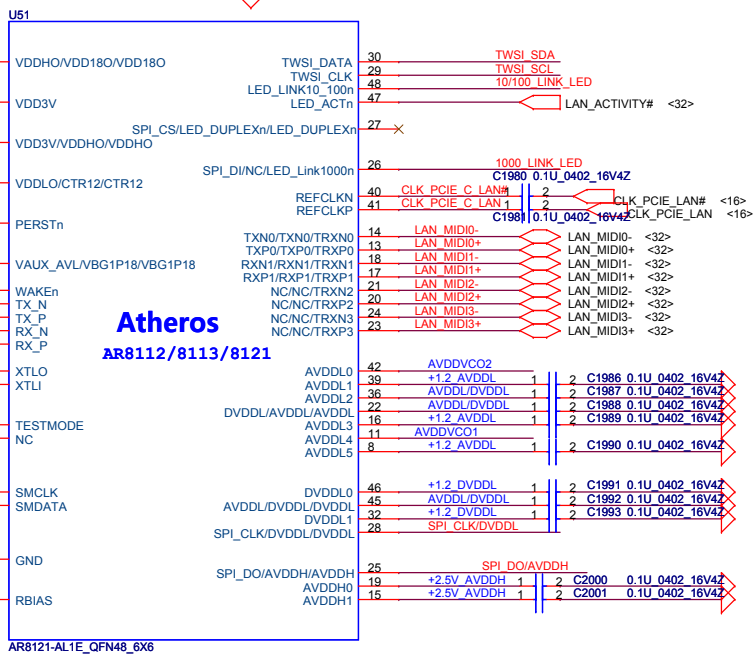
AR8112:



Cap is ceramic capacitor

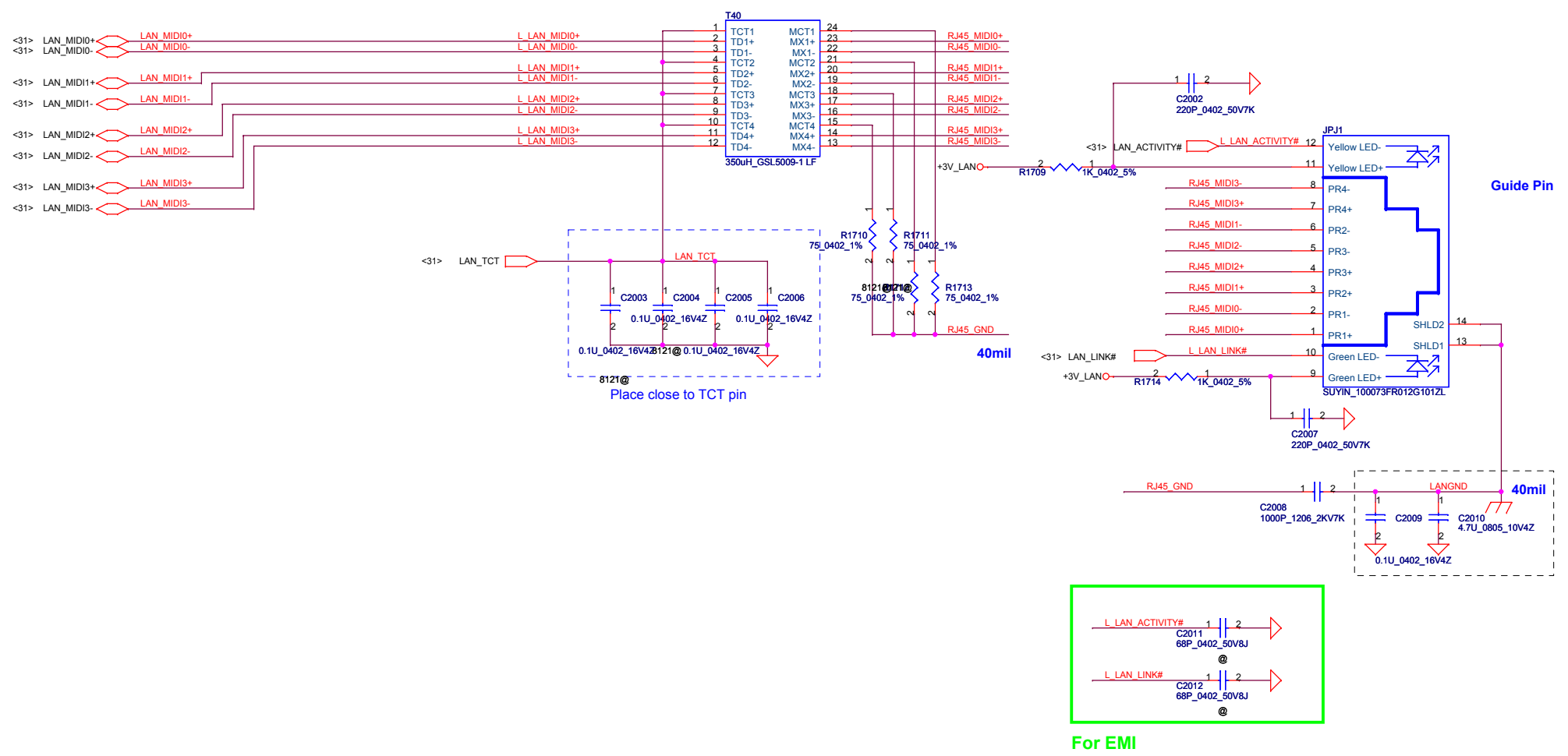


For AR8112: R294=2.49K
For AR8113/8121: R294=2.37K



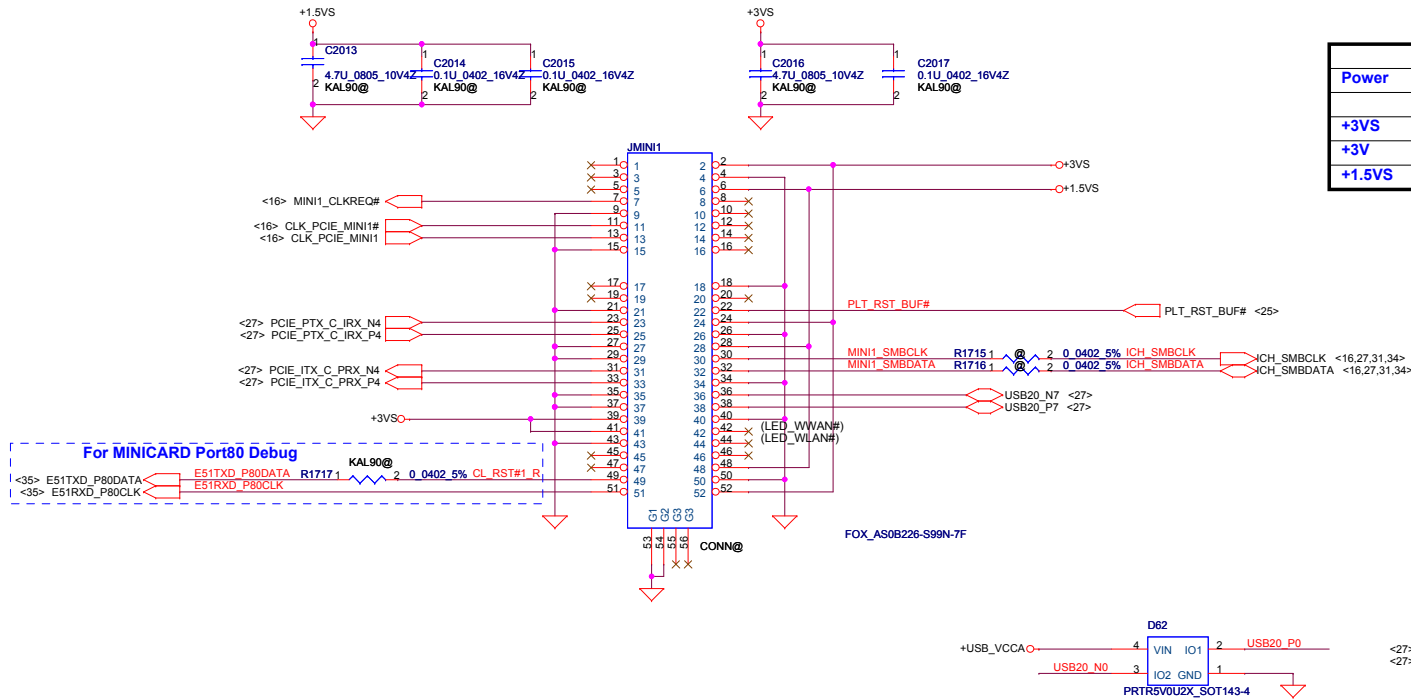
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LAN AR8121/8112



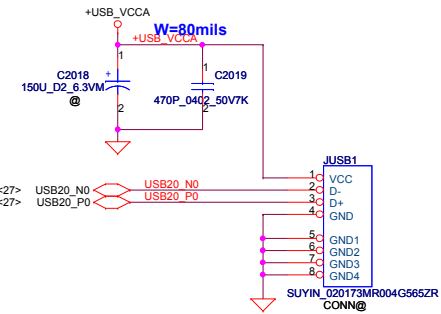
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For Robson2

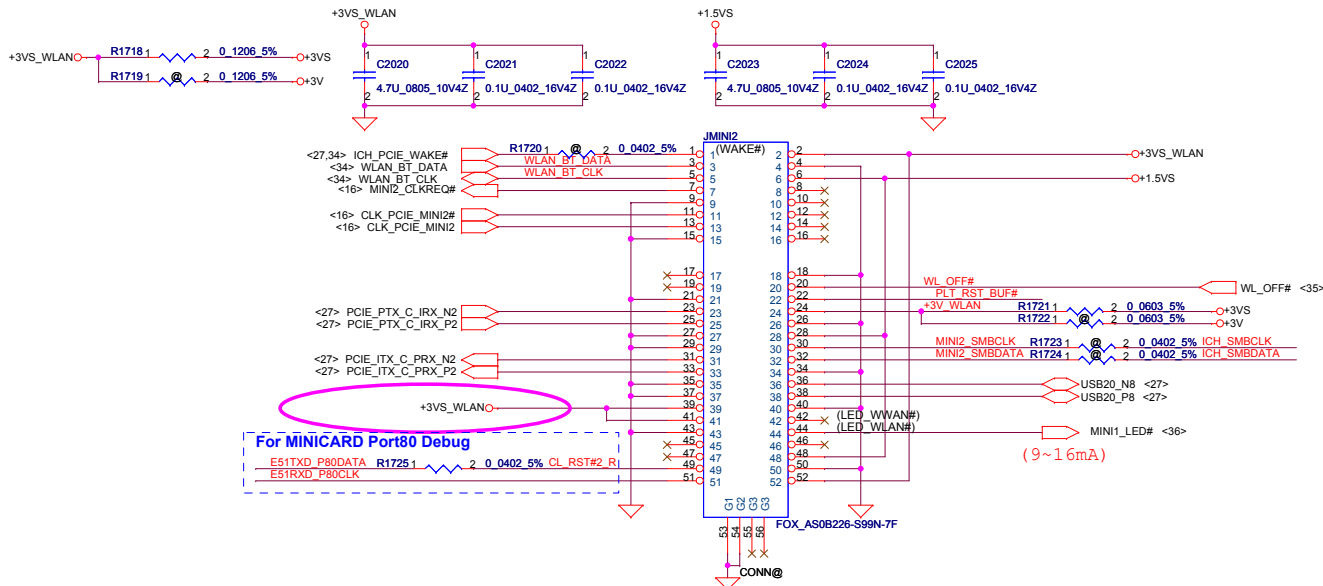


Power	Mini Card Power Rating	
	Primary Power (mA)	Auxiliary Power (mA)
+3VS	1000	750
+3V	330	250
+1.5VS	500	375

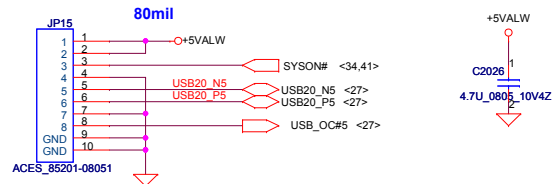
USB CONN.



For Wireless LAN

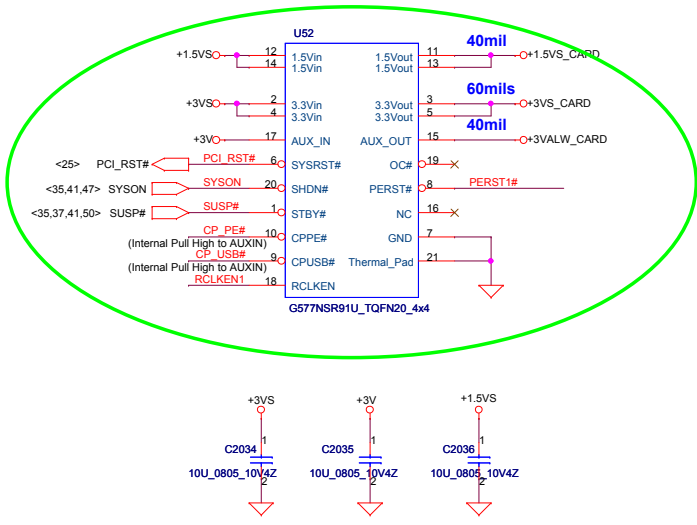


To USB/B Connector

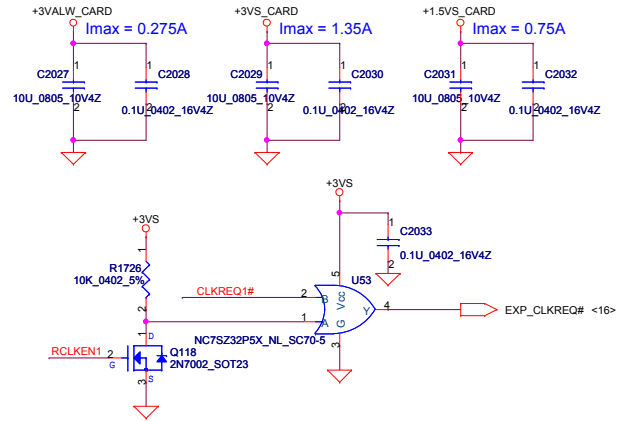
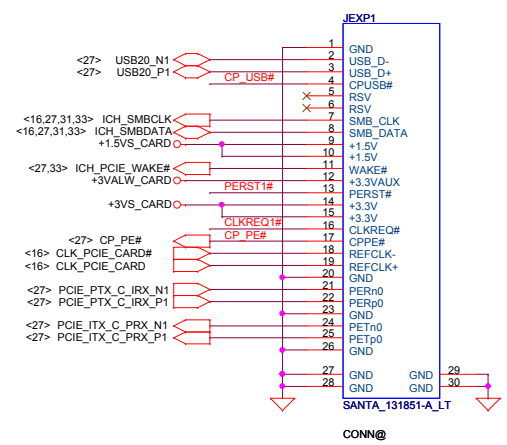


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				MINI CARD (WLAN & Robson2)	
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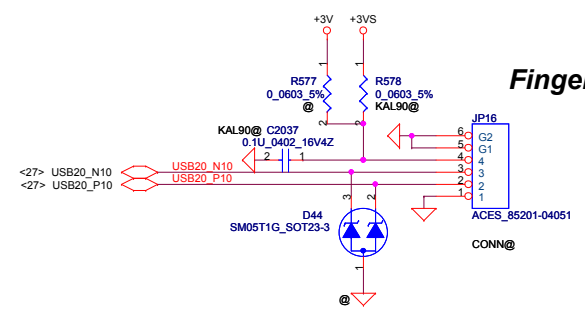
New Card Power Switch



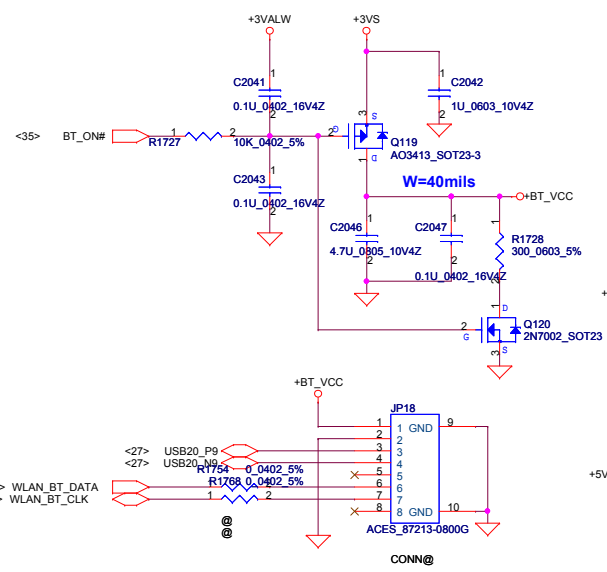
New Card Socket (Left/TOP)



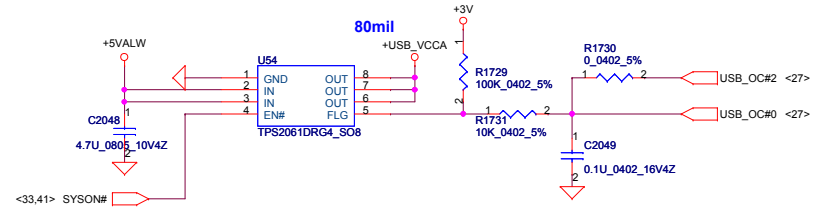
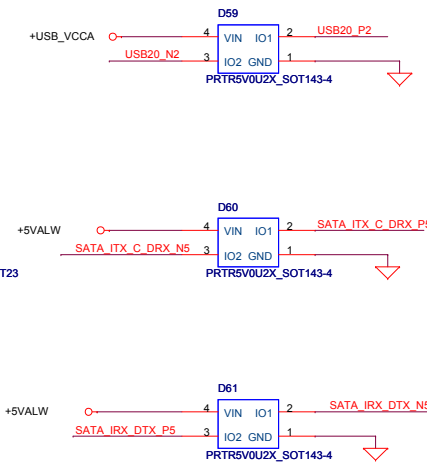
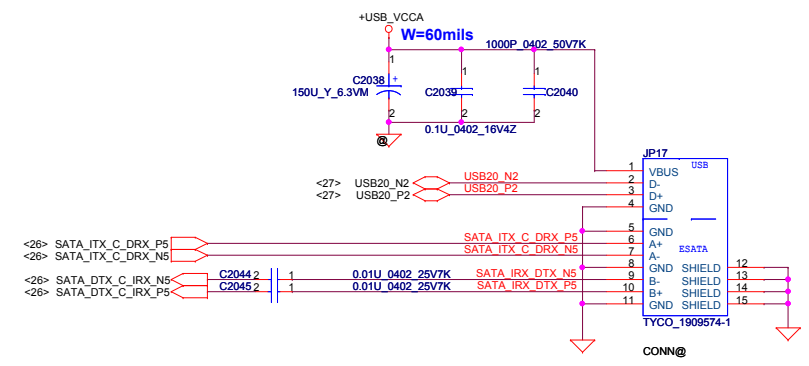
Finger Print Conn.



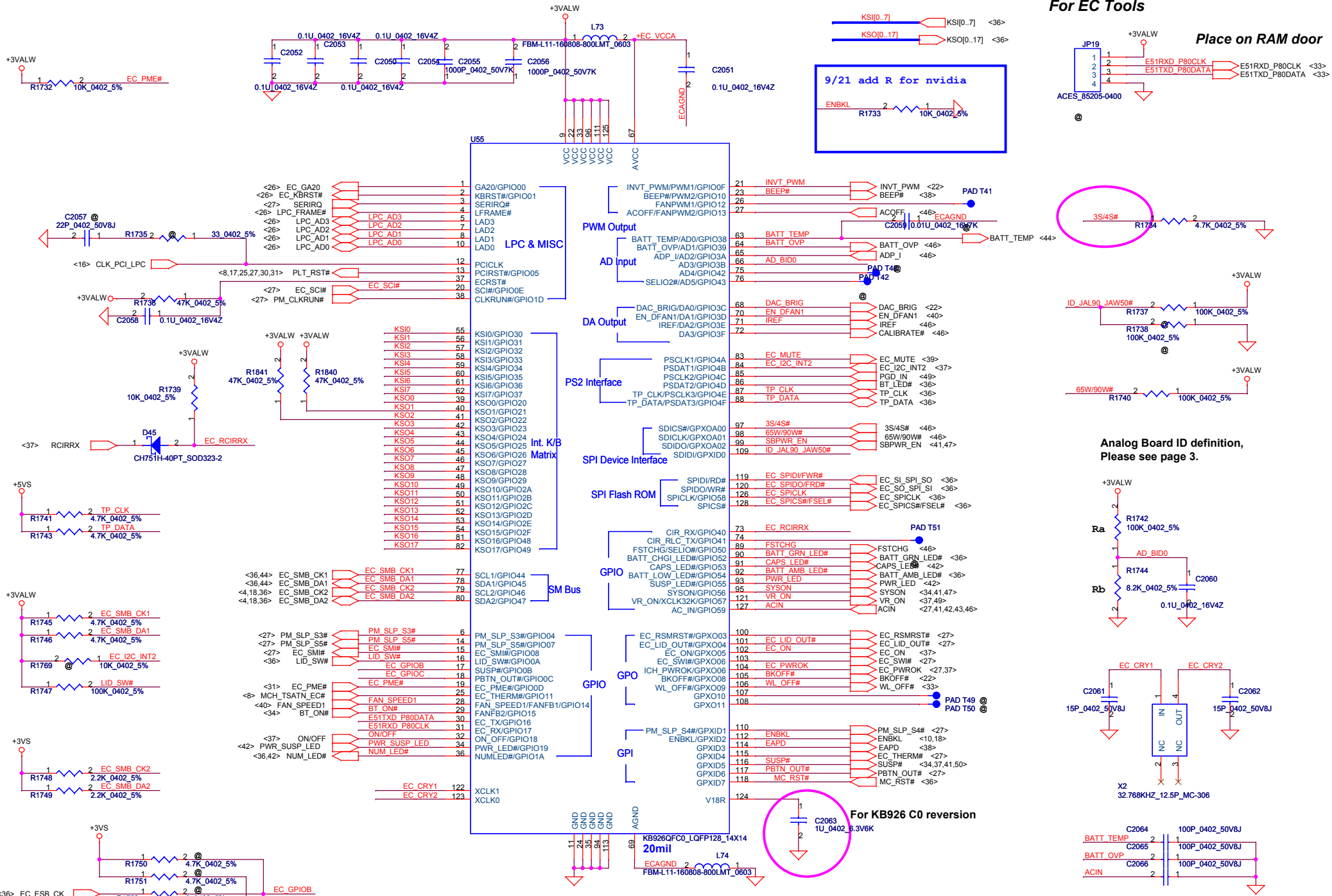
Bluetooth Conn.



ESATA CONN

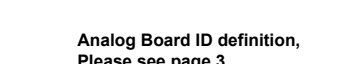
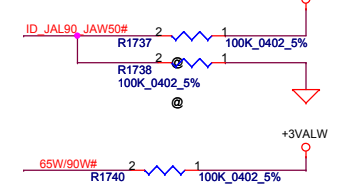
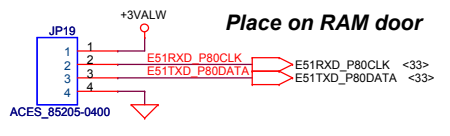
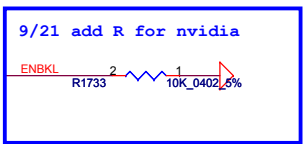


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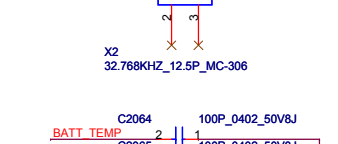
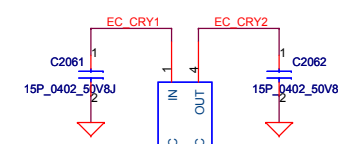
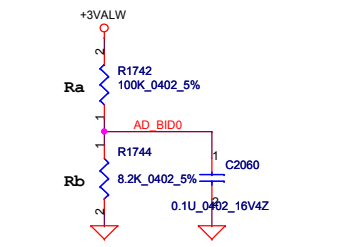


For EC Tools

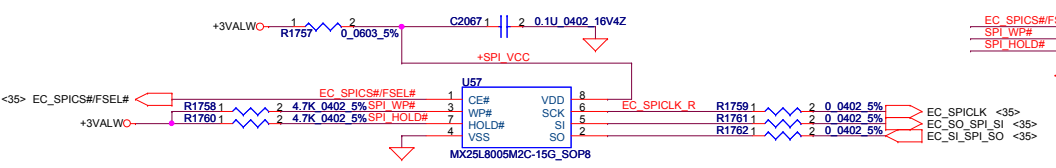
Place on RAM door



Analog Board ID definition, Please see page 3.

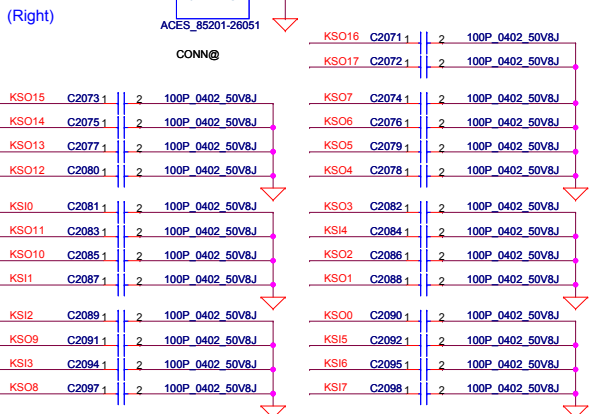
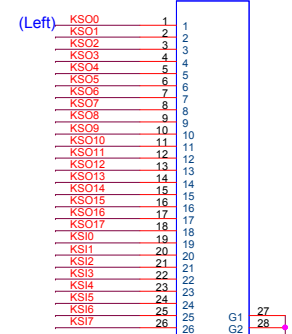
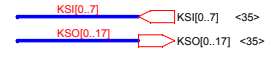


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B	KAL90KALH0	0.2			
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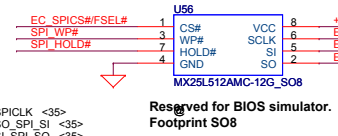
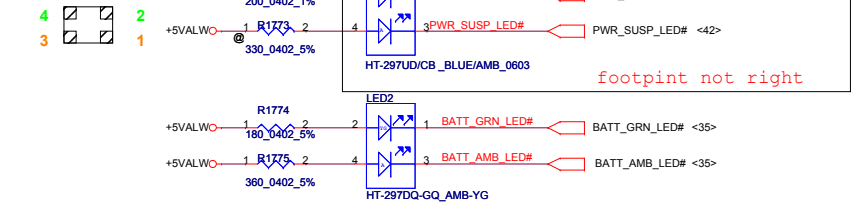


ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

INT_KBD Conn.

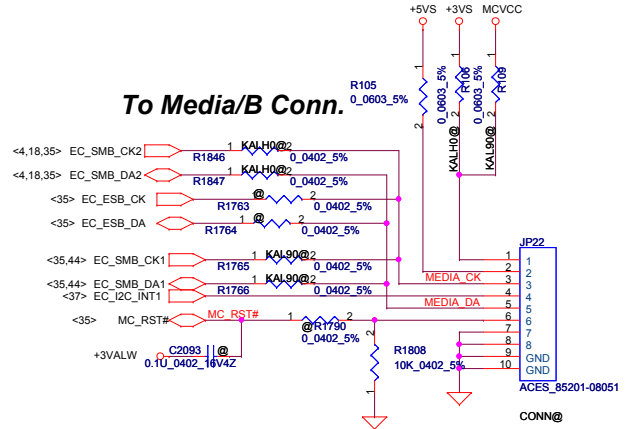


Compal Footprint

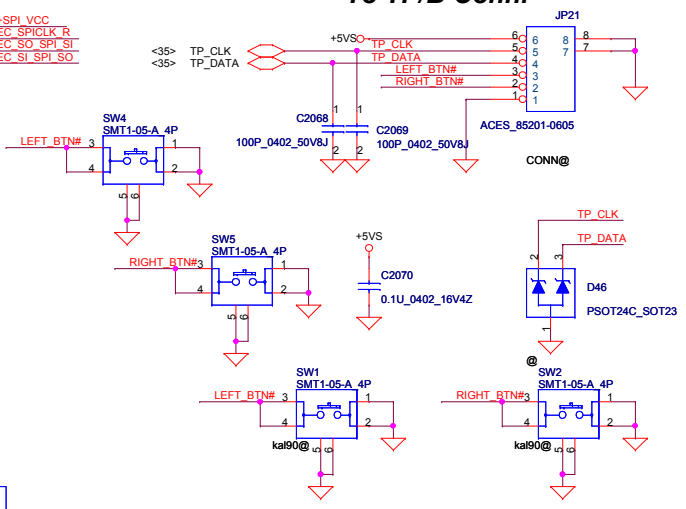


Reserved for BIOS simulator.
 Footprint S08

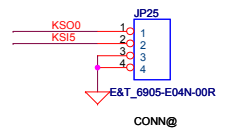
To Media/B Conn.



To TP/B Conn.

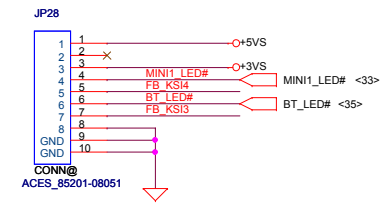


e-key/B

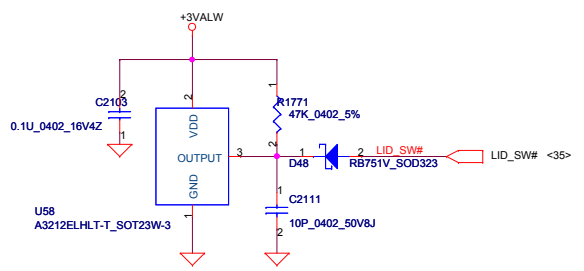


To BTN/B Conn.

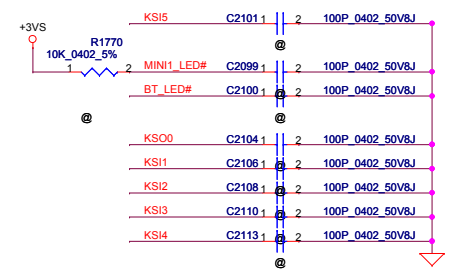
KSx	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#



Lid Switch (Hall Effect Switch)



FOR EMI

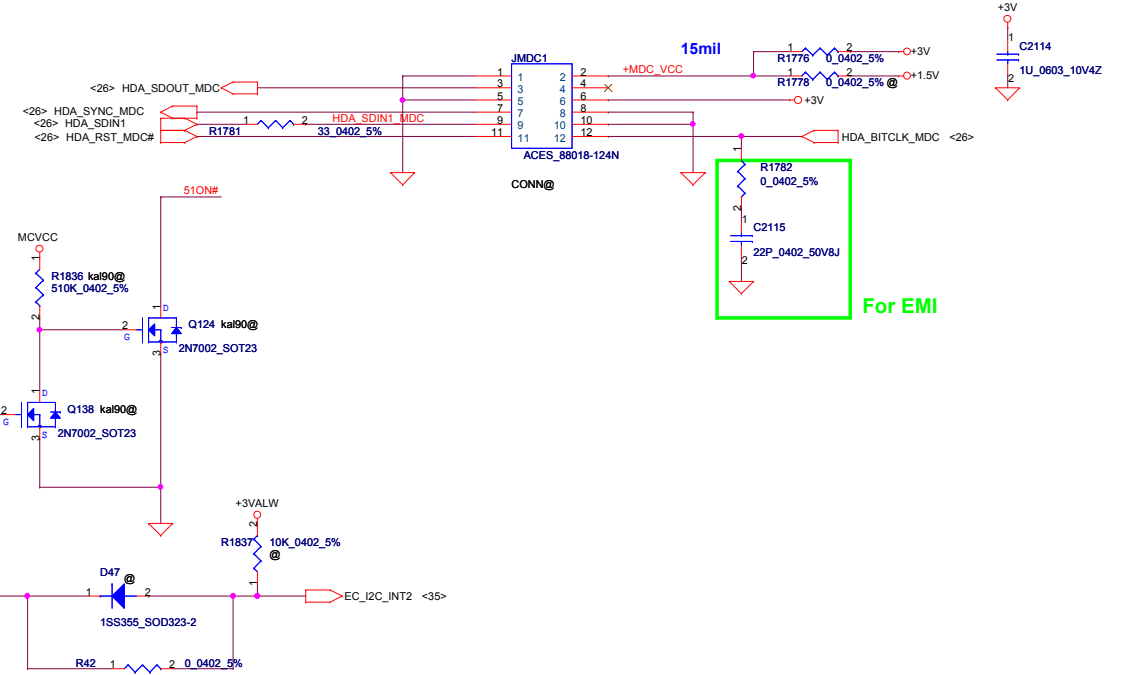
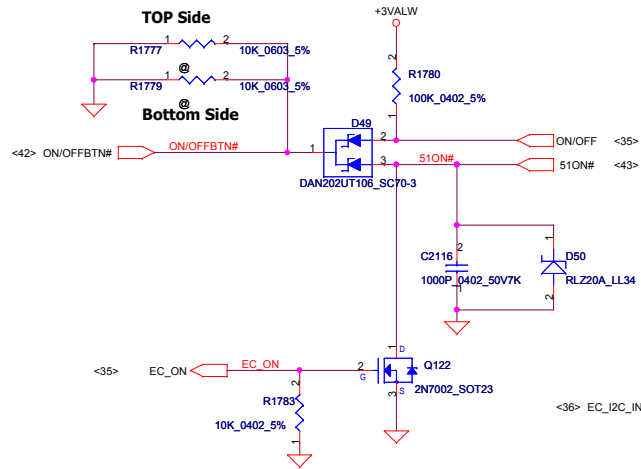


Security Classification				Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title		BIOS, I/O Port & K/B Connector		
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				B	KAL90KALH0			
				Date:	Tuesday, January 06, 2009	Sheet	36	of 52

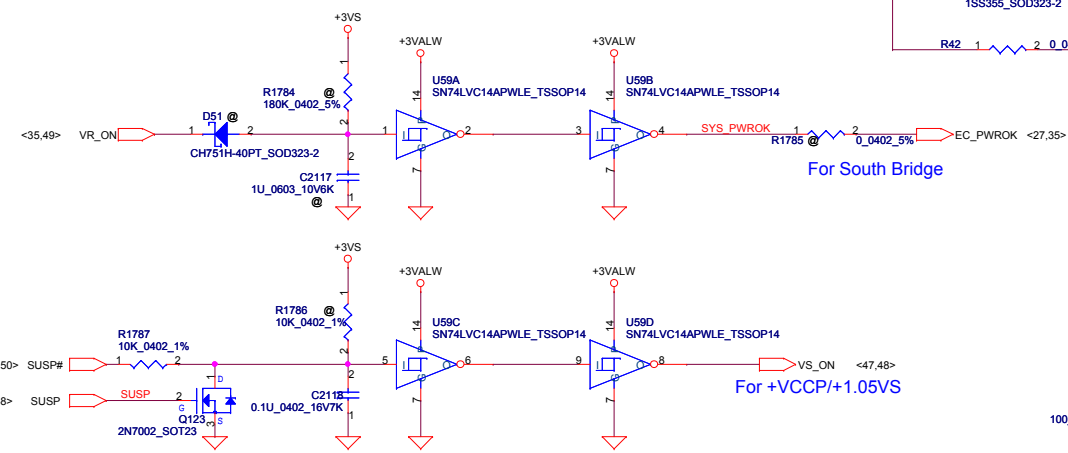
Power Button

HDA MDC Conn.

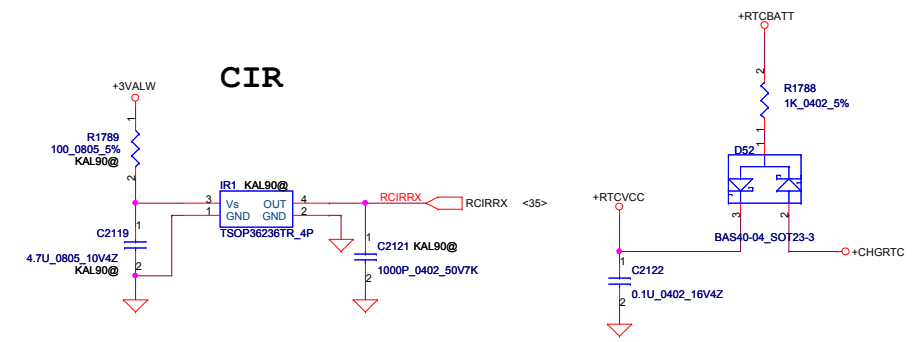
ON/OFF switch



Power ON Circuit

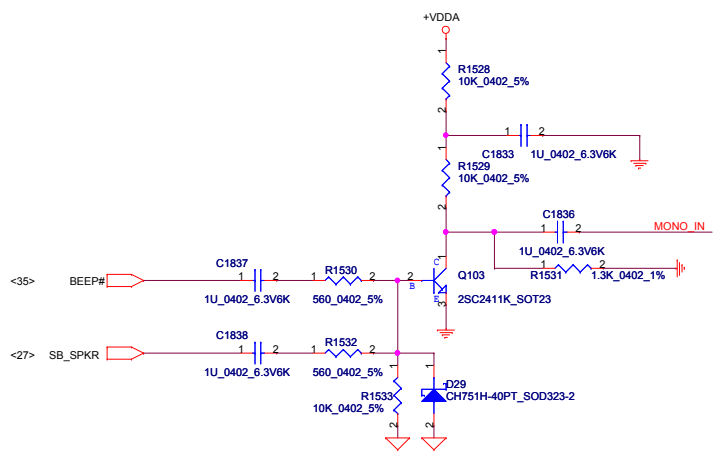


CIR



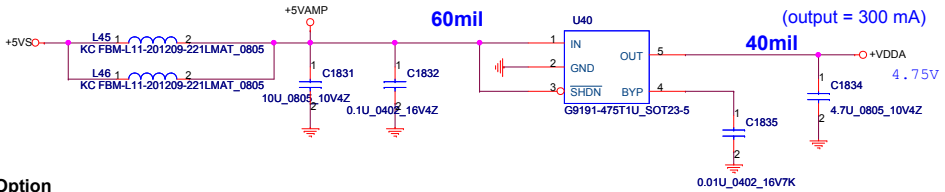
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title		
				Power OK, Reset, RTC, CIR, MDC		
Size	Document Number			Rev		
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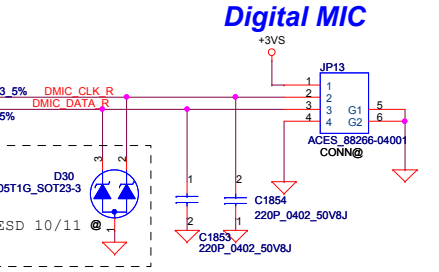
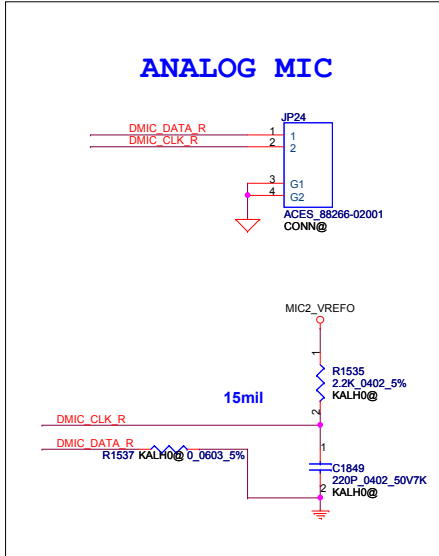
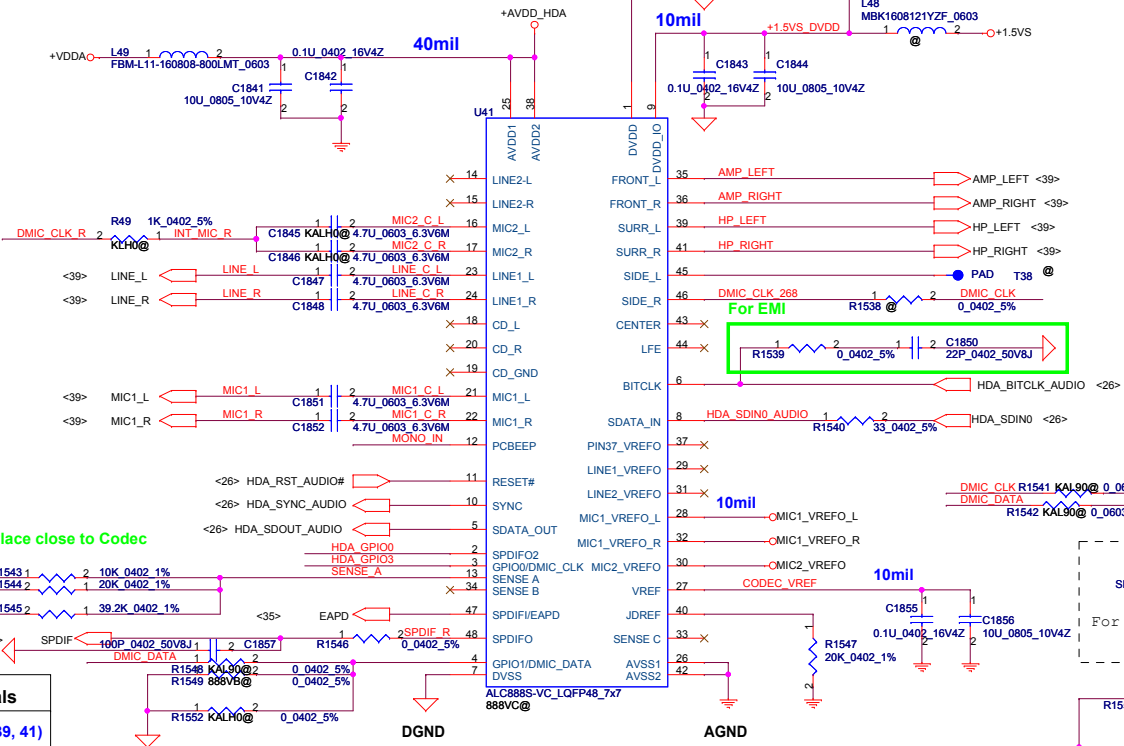


BOM Option

ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@



HD Audio Codec



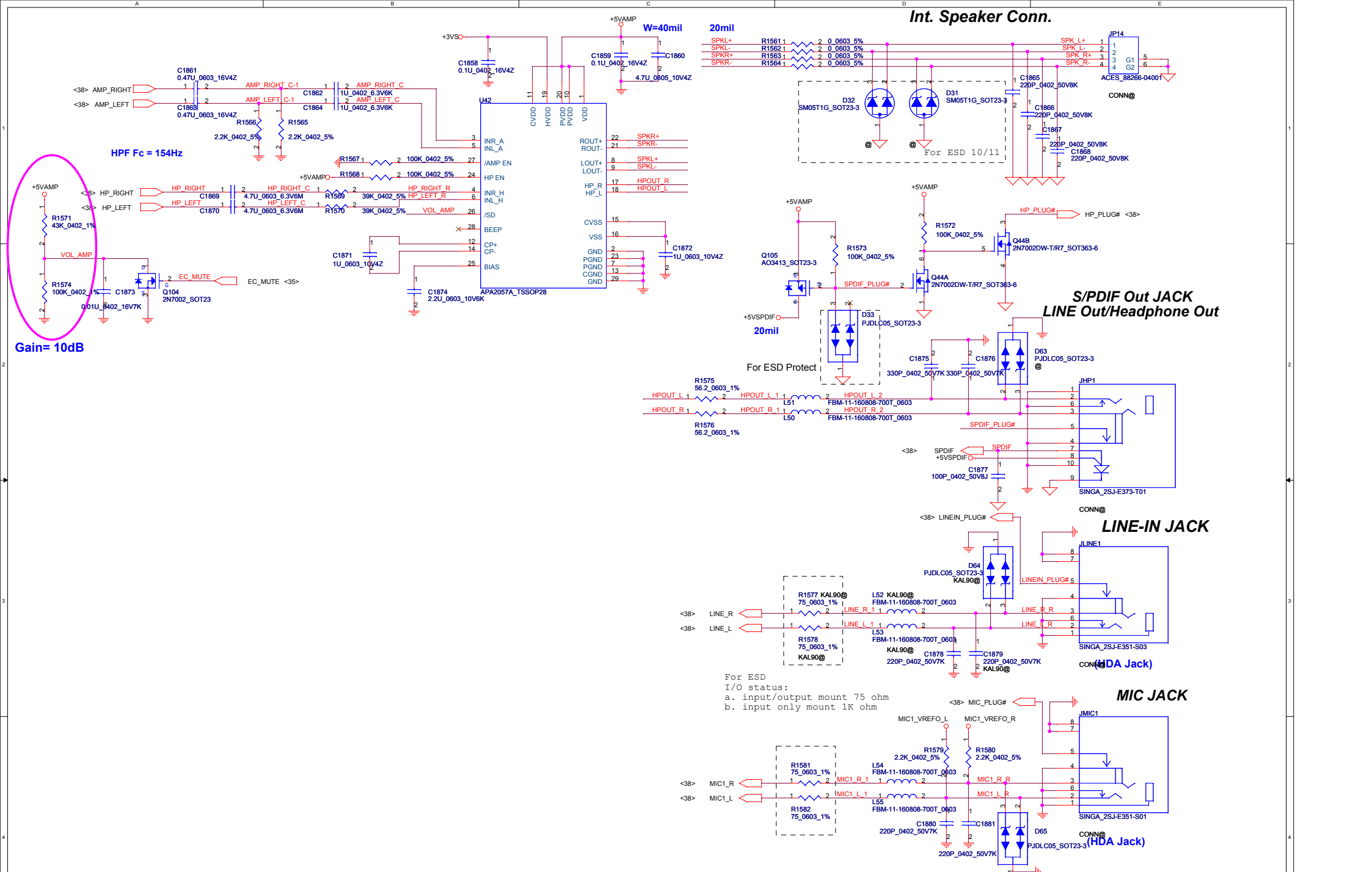
Place close to Codec

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
5.1K	PORT-H (PIN 45, 46)	

Security Classification	Compal Secret Data	
Issued Date	2008/11/10	Deciphered Date
		2008/11/17

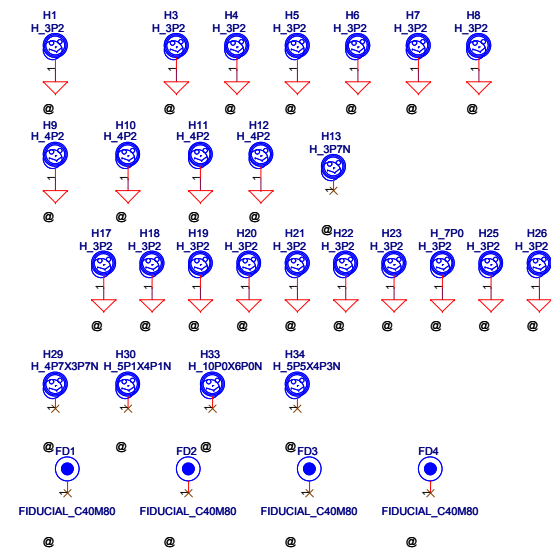
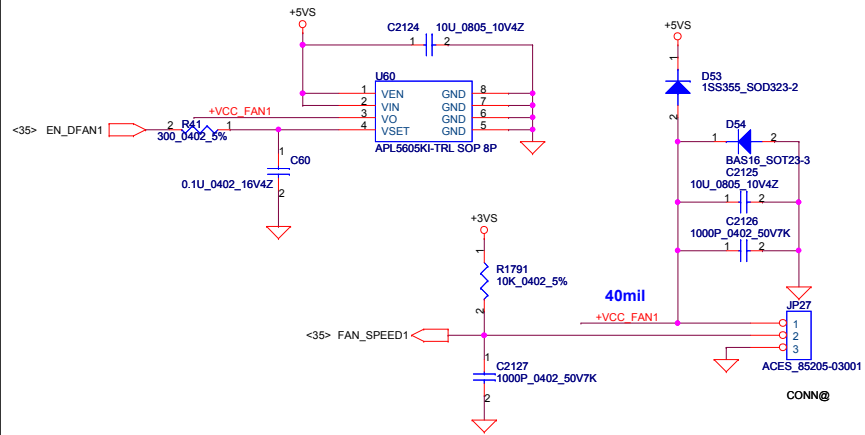
Compal Electronics, Inc.		
HD Audio Codec ALC888S-VC		
Size B	Document Number	Rev
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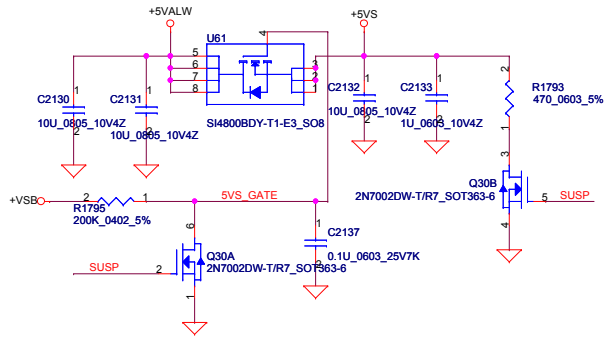
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title
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Size	Document Number	Rev		
B	KAL90KALHO	0.2		
Date:	Tuesday, January 06, 2009	Sheet	39	of 52

FAN1 Conn

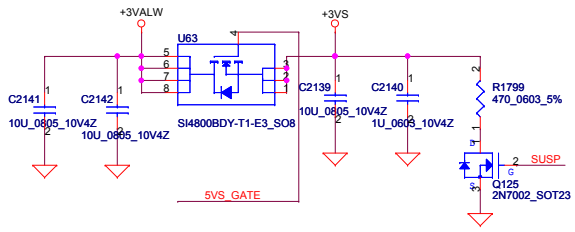


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Size	Document Number			Rev	
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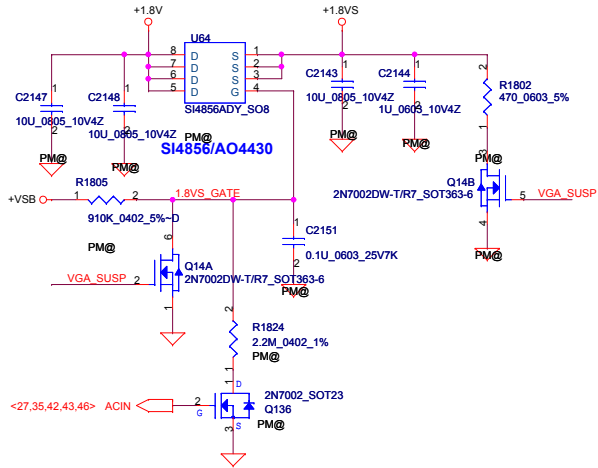
+5VALW TO +5VS



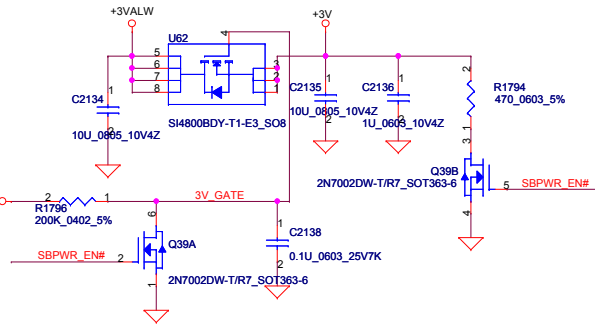
+3VALW TO +3VS



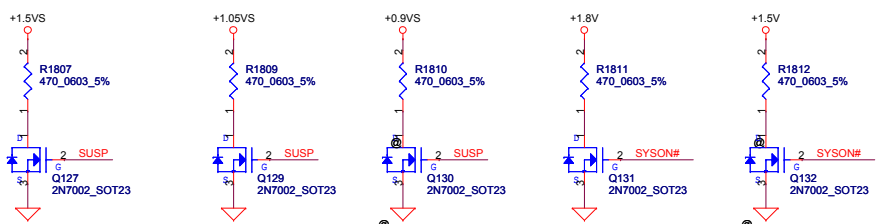
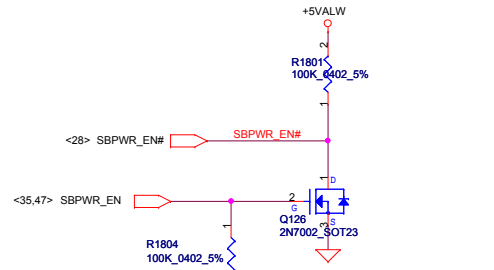
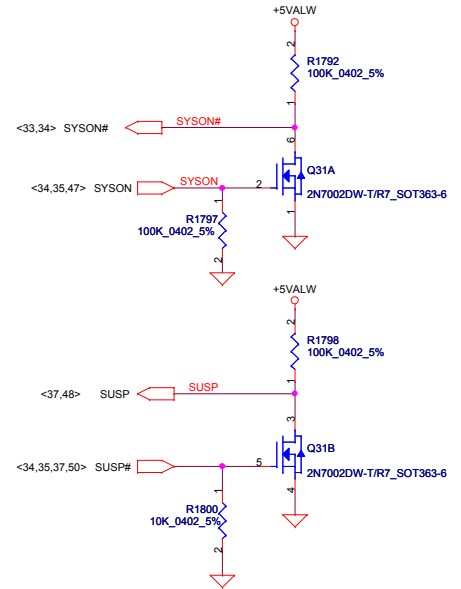
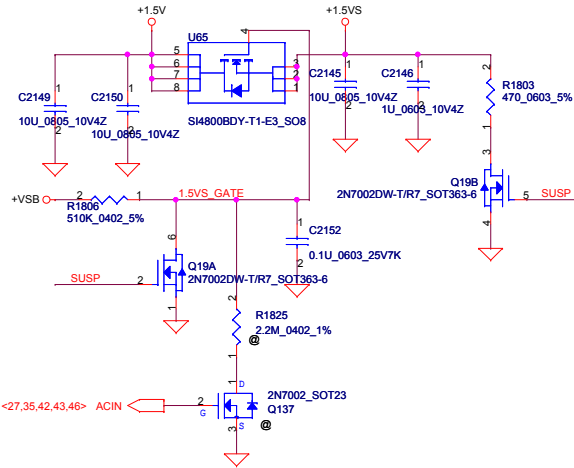
+1.8V to +1.8VS



+3VALW TO +3V_SB(ICH8M AUX Power)

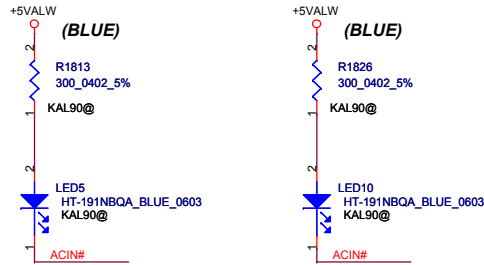


+1.5V to +1.5VS

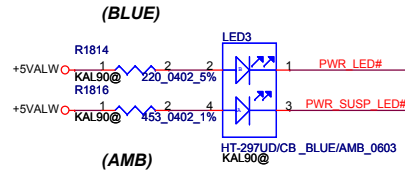


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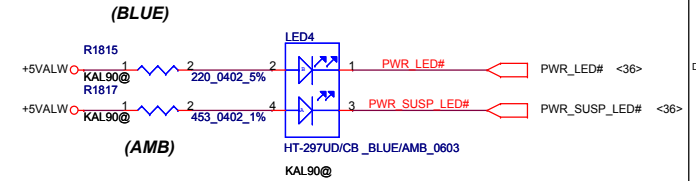
Enlightener LED



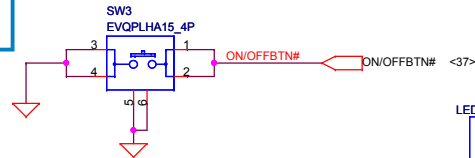
ON/OFF LED LEFT



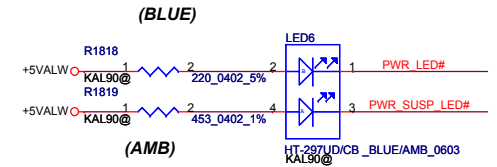
ON/OFF LED RIGHT



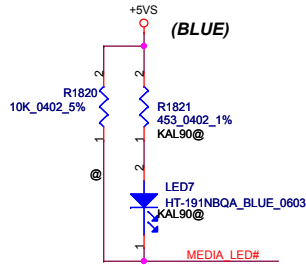
ON/OFF Button



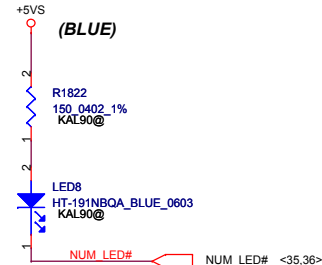
ON/OFF LED DOWN



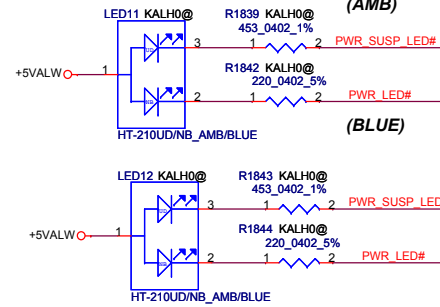
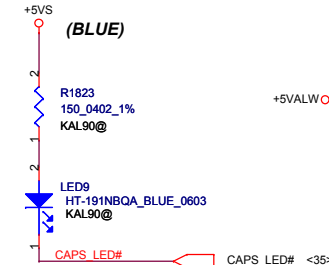
MEDIA_LED



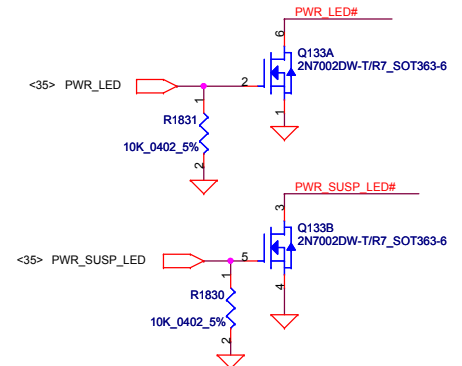
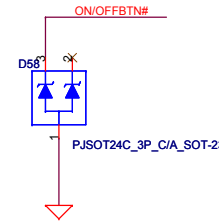
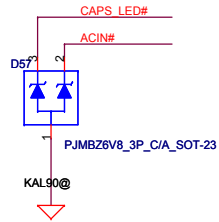
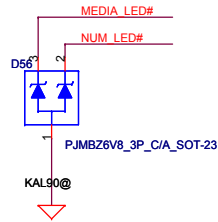
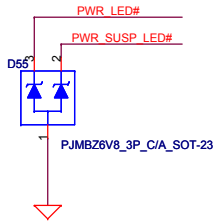
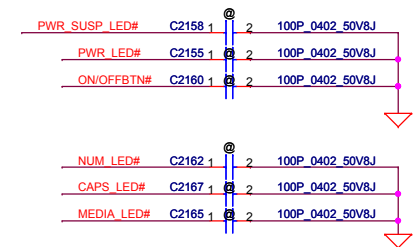
NUM_LED



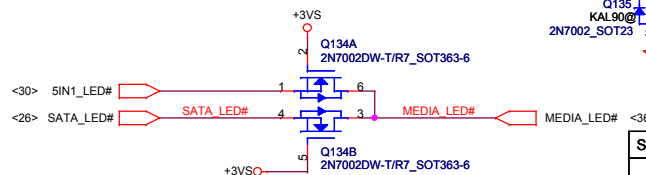
CAPS_LED



FOR EMI



**D1 D2 D3 USE PANJIT PJM26V8
SCA0000I00
6.8V**

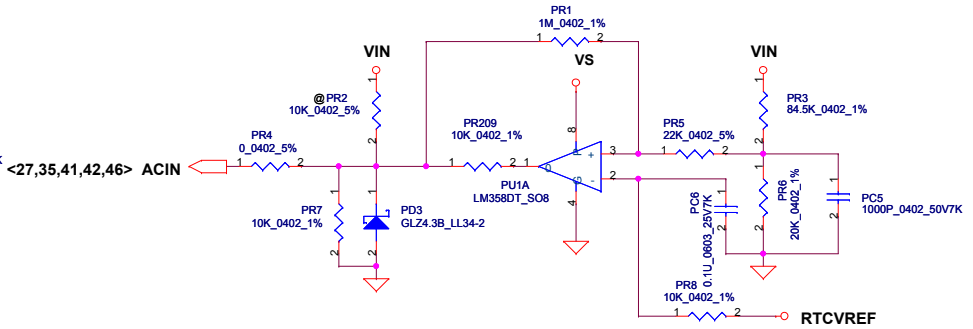
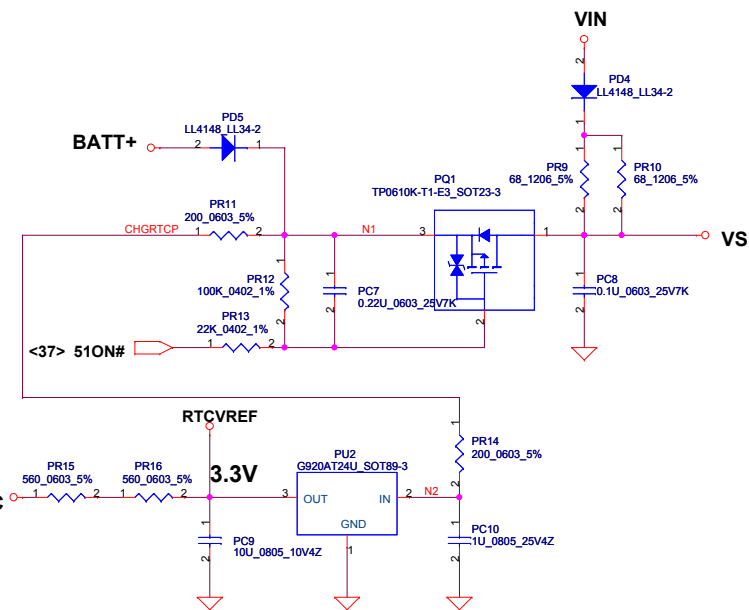
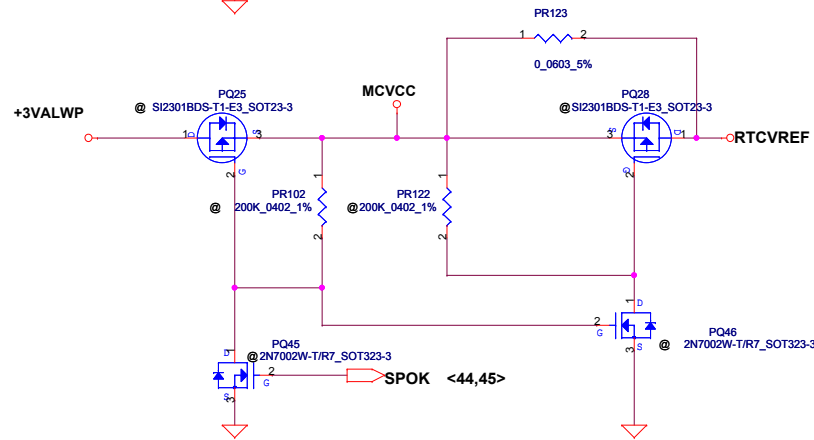
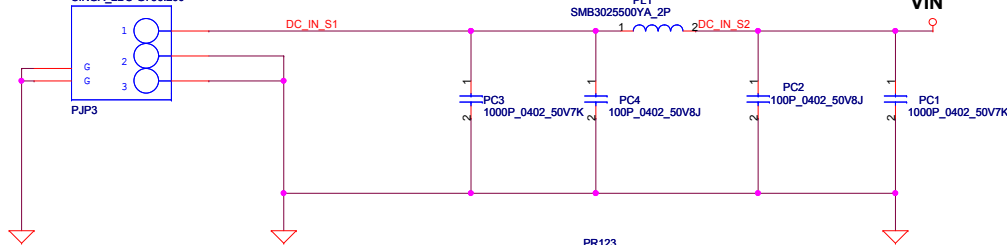


**D4 USE
PJSOT24C 3P C/A SOT-23
SCA0000E00
24V**

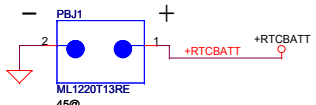
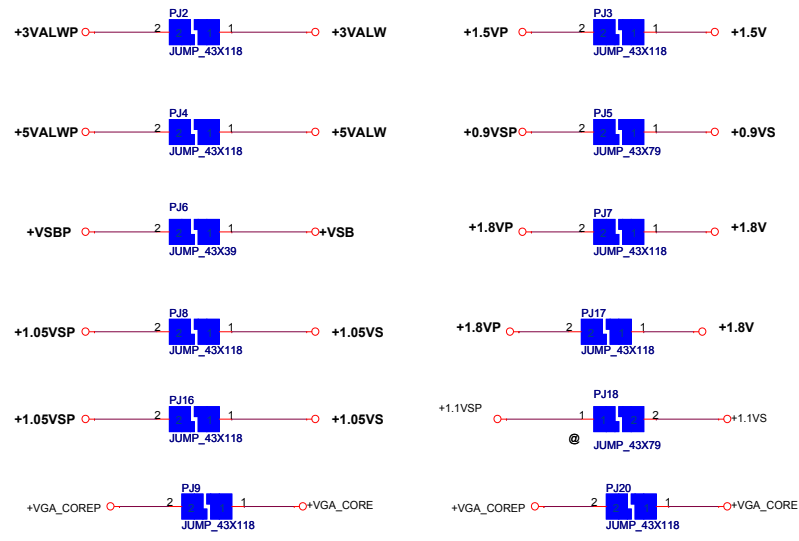
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Date:	Wednesday, December 24, 2008	Sheet	42	of	52

DC231000500

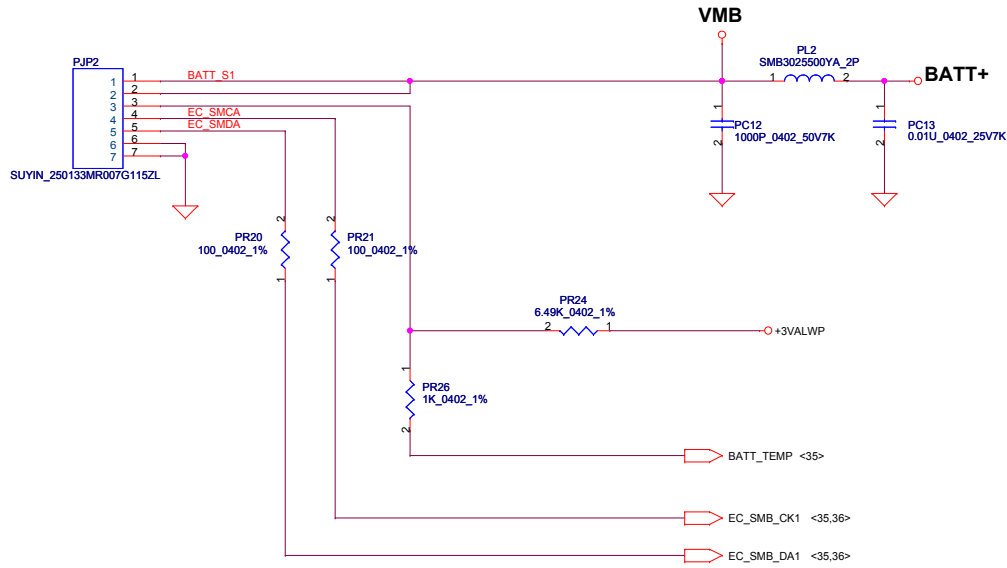
<BOM Structure>
SINGA_ZDC-G756I200



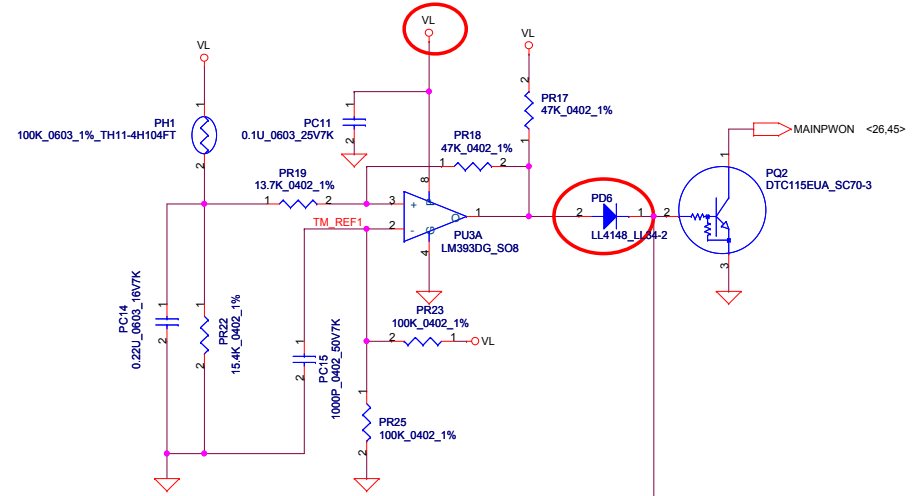
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



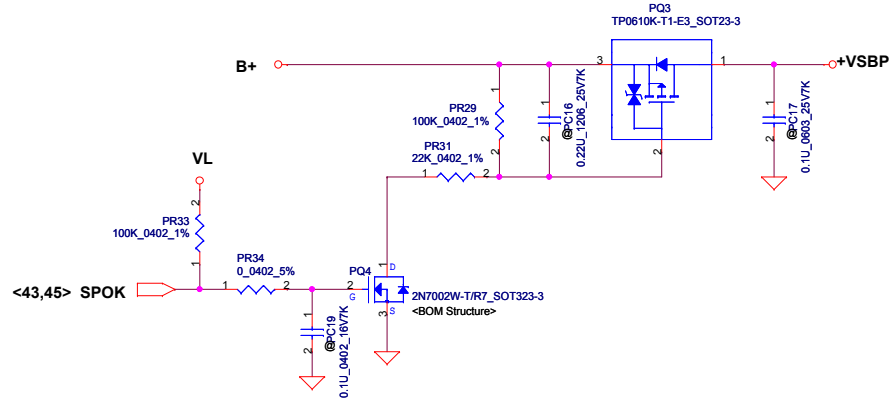
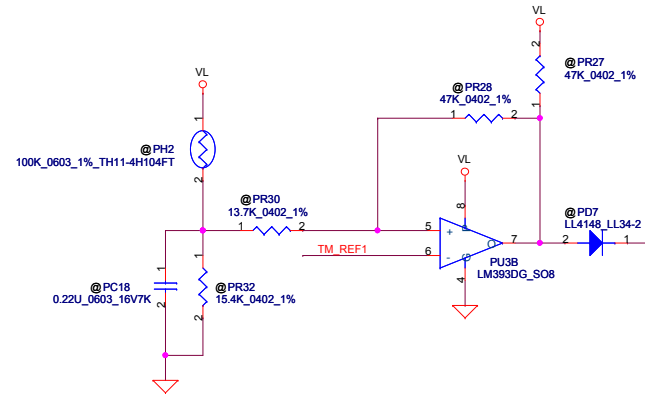
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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Size	Document Number	Rev		0.2	
Customer	KAL90KALH0	Date:		Tuesday, December 09, 2008	
		Sheet	43	of 52	



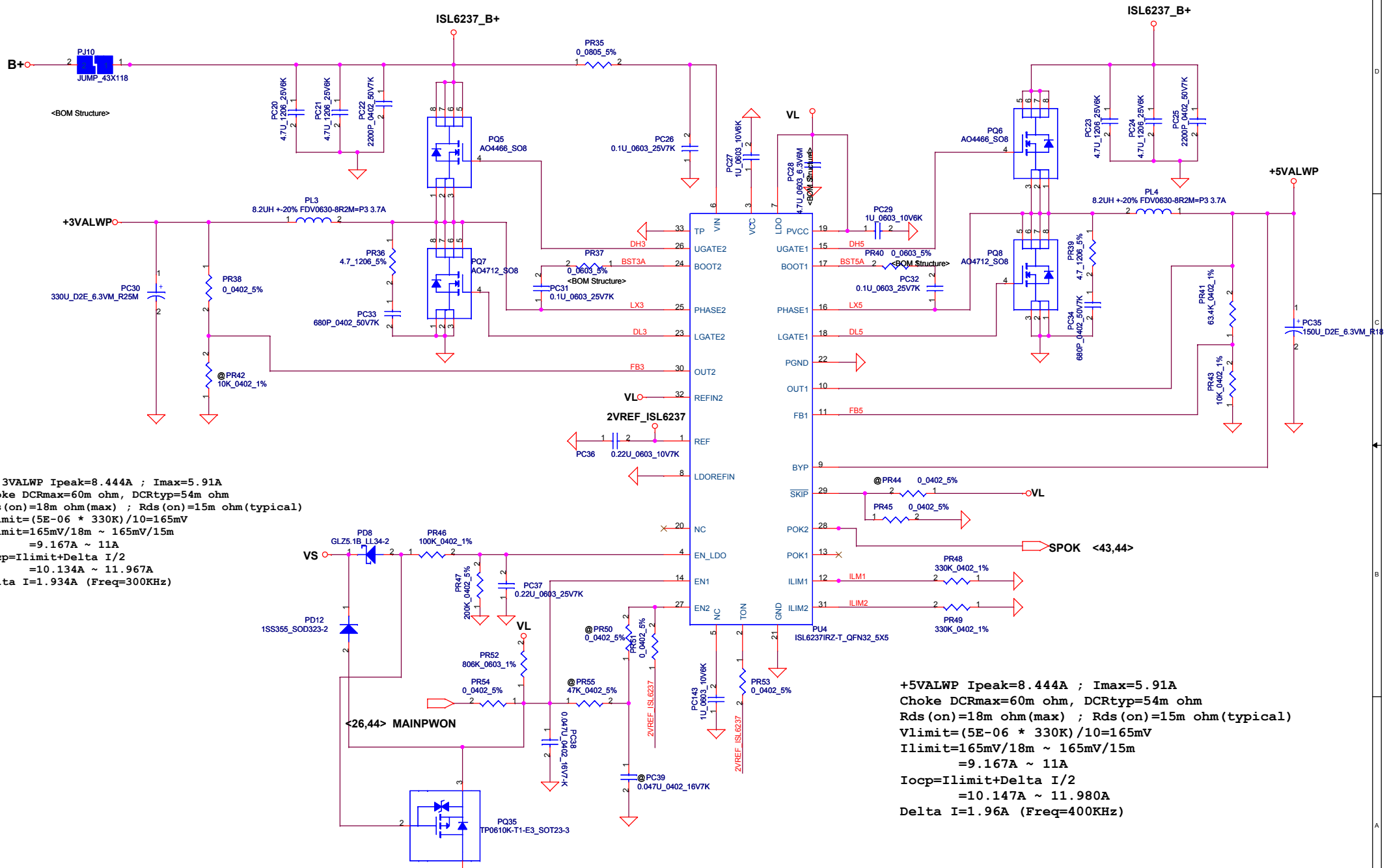
PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



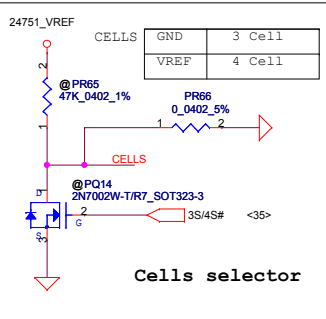
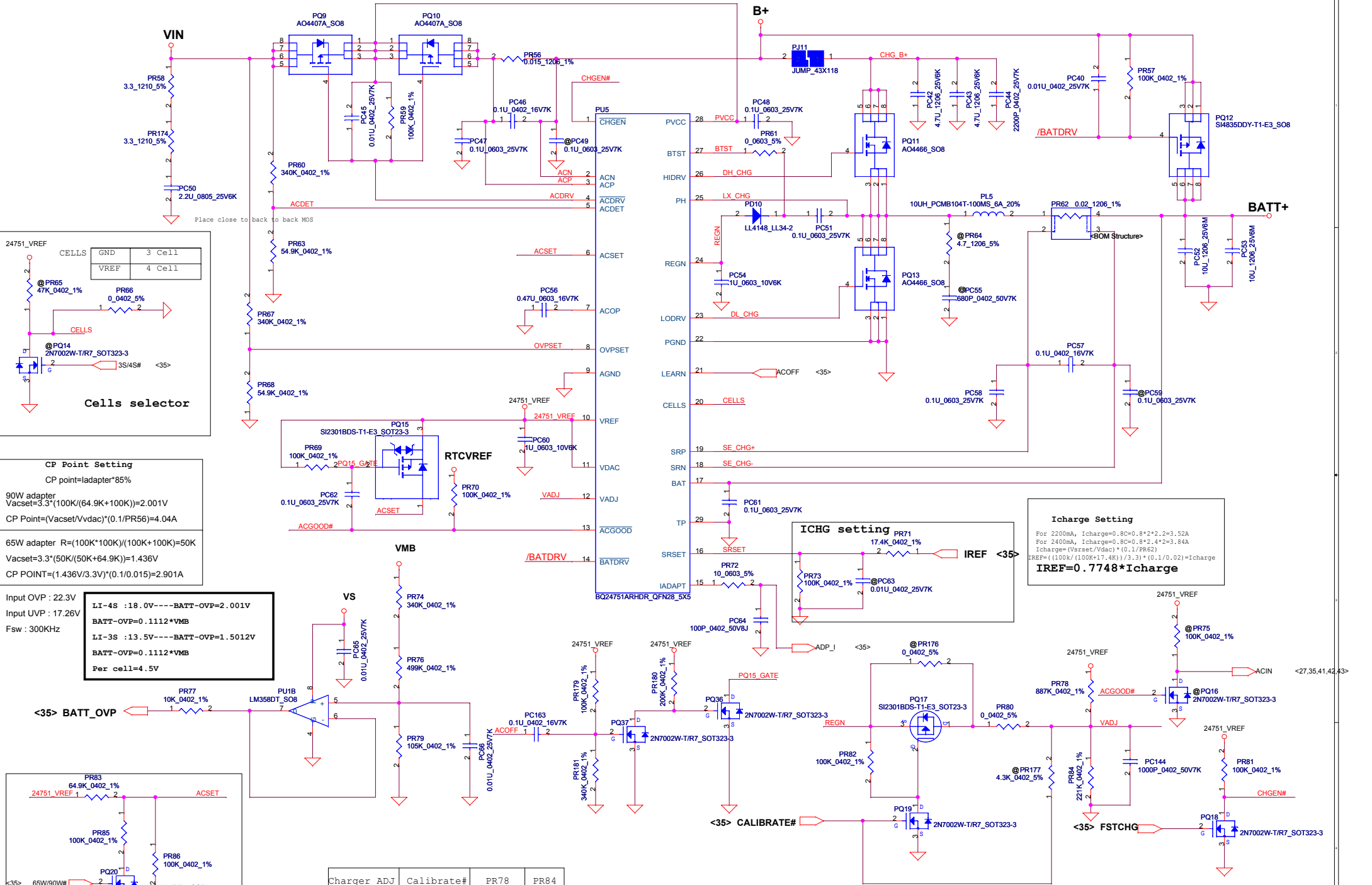
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

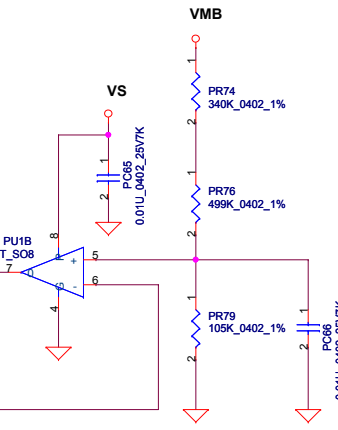
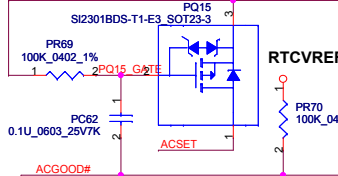
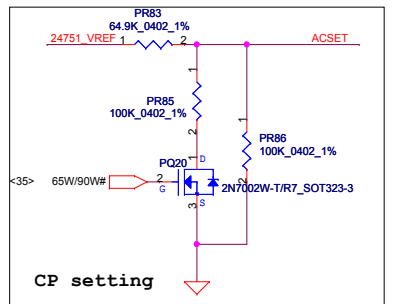
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				+5VALWP/+3VALWP	
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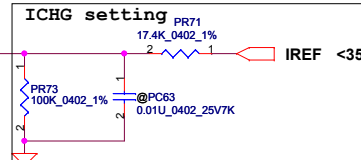
CP Point Setting
 CP point=ladapter*85%
 90W adapter
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$
 $CP\ Point = (V_{acset} / V_{vdac}) \cdot (0.1 / PR56) = 4.04A$
 65W adapter $R = (100K \cdot 100K) / (100K + 100K) = 50K$
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$
 $CP\ POINT = (1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V --- BATT-OVP=2.001V
 BATT-OVP=0.1112 * VMB
 LI-3S : 13.5V --- BATT-OVP=1.5012V
 BATT-OVP=0.1112 * VMB
 Per cell=4.5V



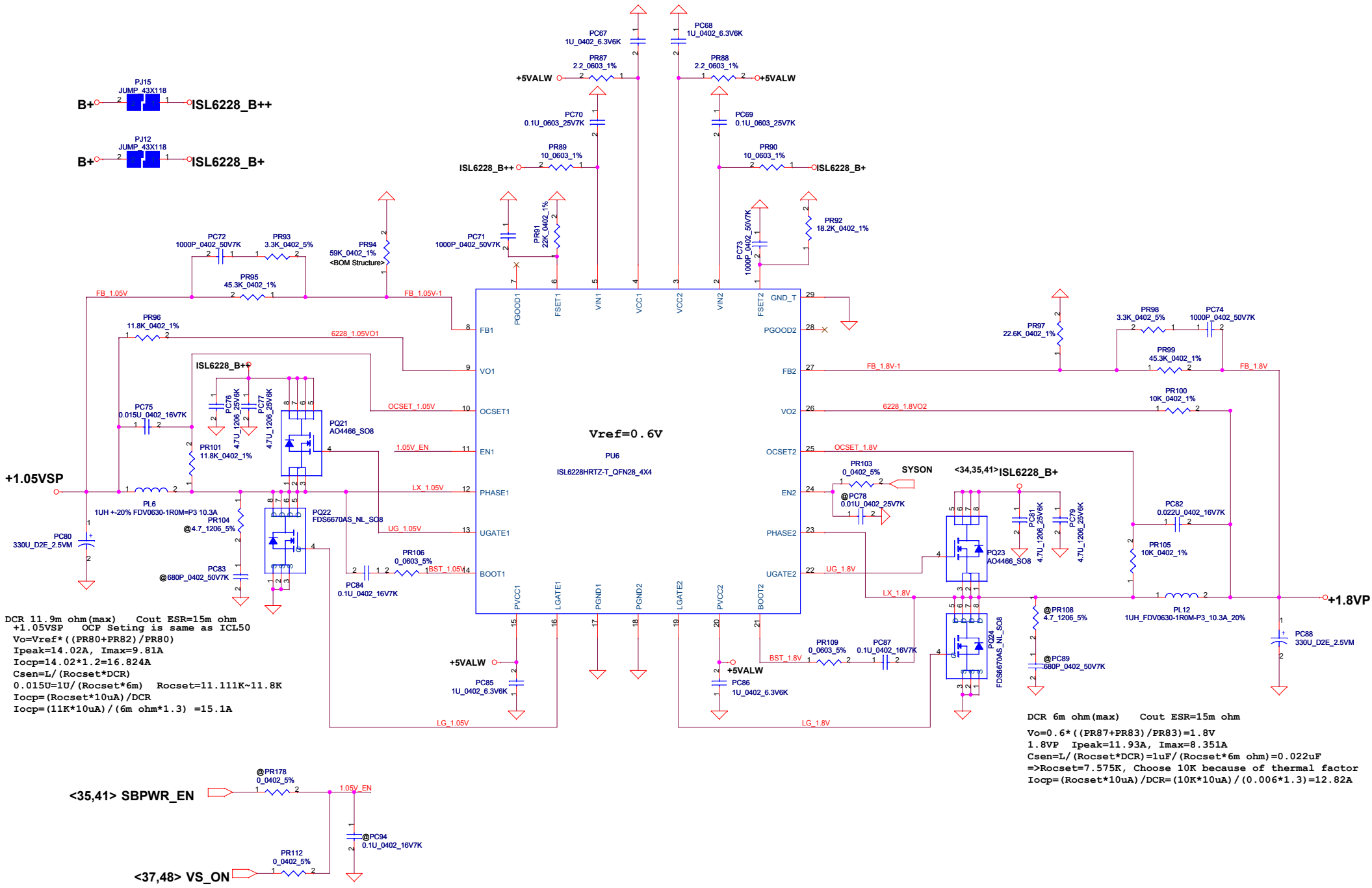
Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@



Icharge Setting
 For 2200mA, $I_{charge} = 0.8 \cdot 2 \cdot 2.2 = 3.52A$
 For 2400mA, $I_{charge} = 0.8 \cdot 0.8 \cdot 2.4 = 3.84A$
 $I_{charge} = (V_{acset} / V_{dacc}) \cdot (0.1 / PR62)$
 $I_{REF} = (100K / (100K + 17.4K)) / 3.3 \cdot (0.1 / 0.02) = I_{charge}$
 $I_{REF} = 0.7748 \cdot I_{charge}$

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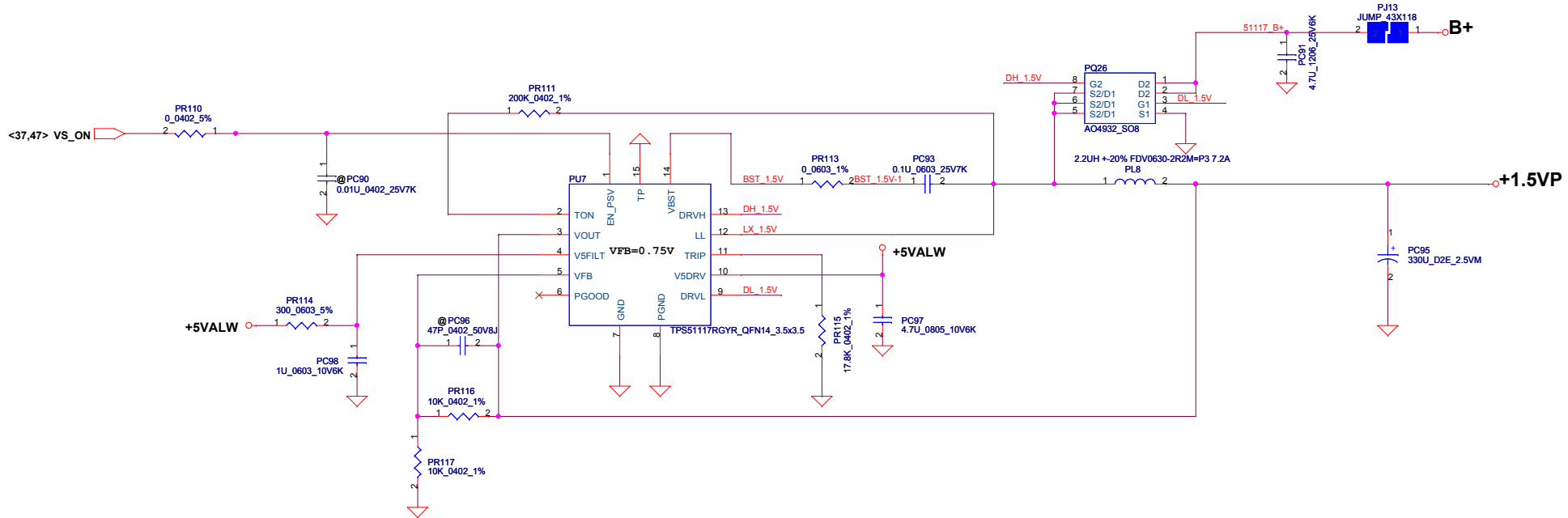
Compal Electronics, Inc.			
CHARGER			
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DCR 11.9m ohm(max) Cout ESR=15m ohm
+1.05VSP OCP Setting is same as ICL50
 $V_o = V_{ref} * ((PR80 + PR82) / PR80)$
 $I_{peak} = 14.02A, I_{max} = 9.81A$
 $I_{ocp} = 14.02 * 1.2 = 16.824A$
 $C_{sen} = L / (Rocset * DCR)$
 $0.015u = 1u / (Rocset * 6m) Rocset = 11.111K \sim 11.8K$
 $I_{ocp} = (Rocset * 10uA) / DCR$
 $I_{ocp} = (11K * 10uA) / (6m ohm * 1.3) = 15.1A$

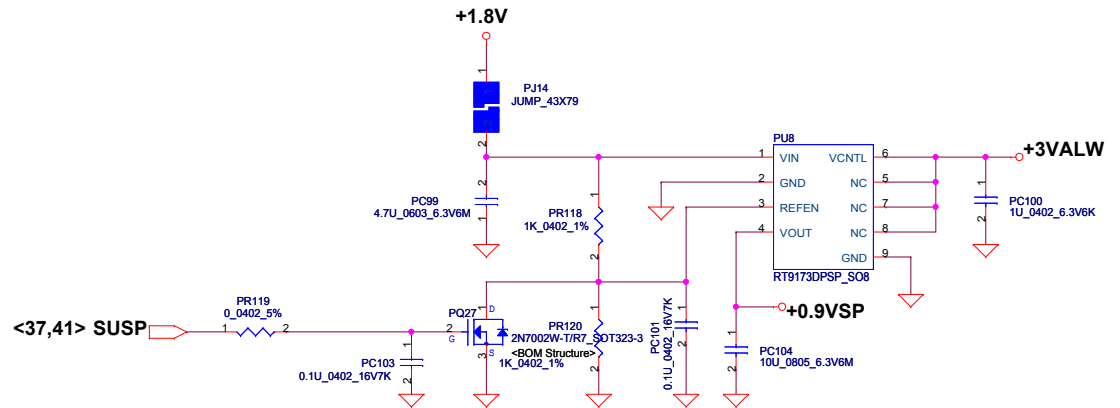
DCR 6m ohm(max) Cout ESR=15m ohm
 $V_o = 0.6 * ((PR87 + PR83) / PR83) = 1.8V$
 $1.8VP I_{peak} = 11.93A, I_{max} = 8.351A$
 $C_{sen} = L / (Rocset * DCR) = 1uF / (Rocset * 6m ohm) = 0.022uF$
 $\Rightarrow Rocset = 7.575K, Choose 10K because of thermal factor$
 $I_{ocp} = (Rocset * 10uA) / DCR = (10K * 10uA) / (0.006 * 1.3) = 12.82A$

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				1.8VP / 1.05VSP	
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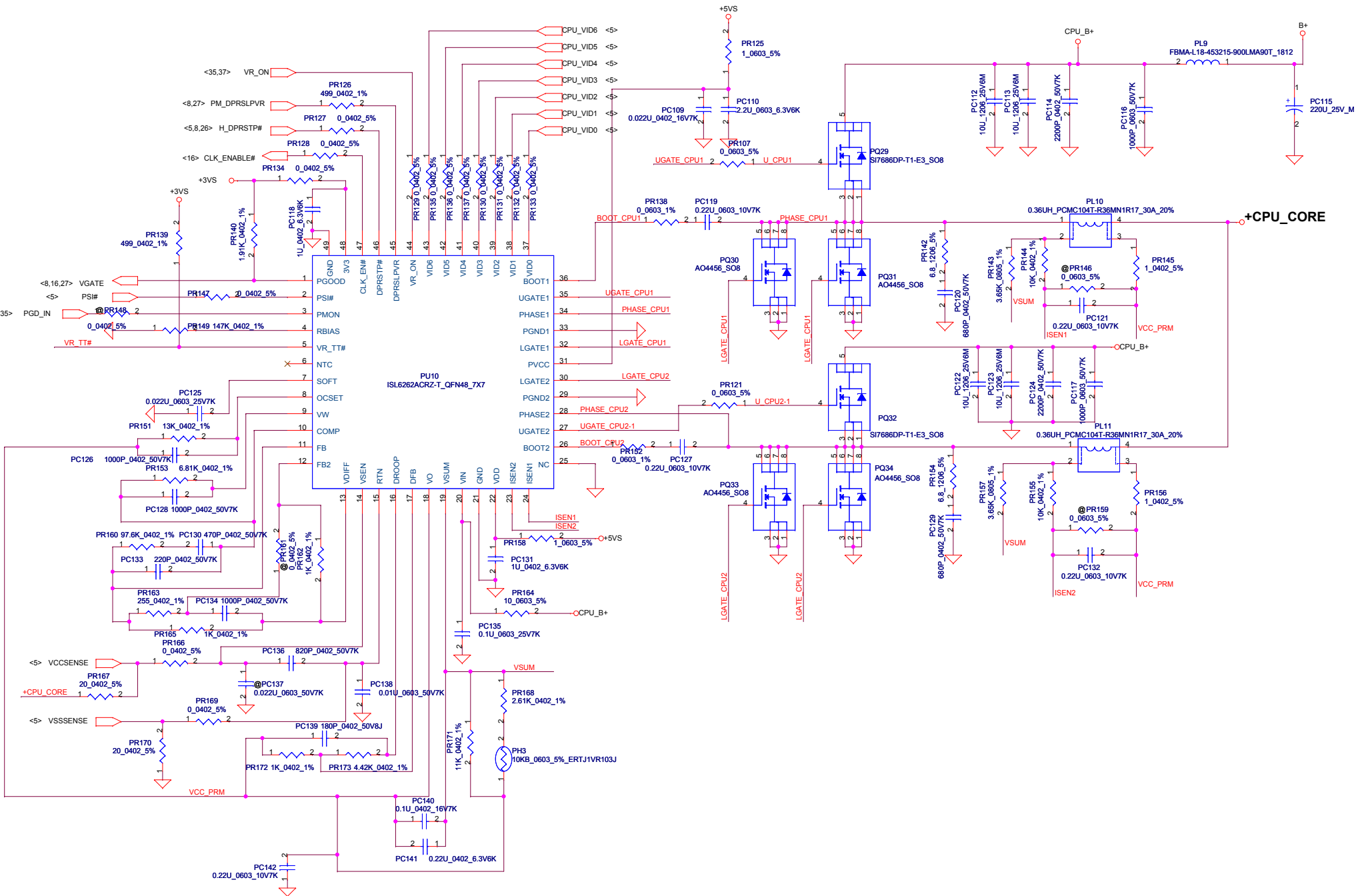


VFB=0.75V
 $V_o = VFB * (1 + PR87 / PR88) = 0.75 * (1 + 4.02K / 10K) = 1.05V$
 $T_{on} = 200K$
 $F_{sw} = 400KHz$

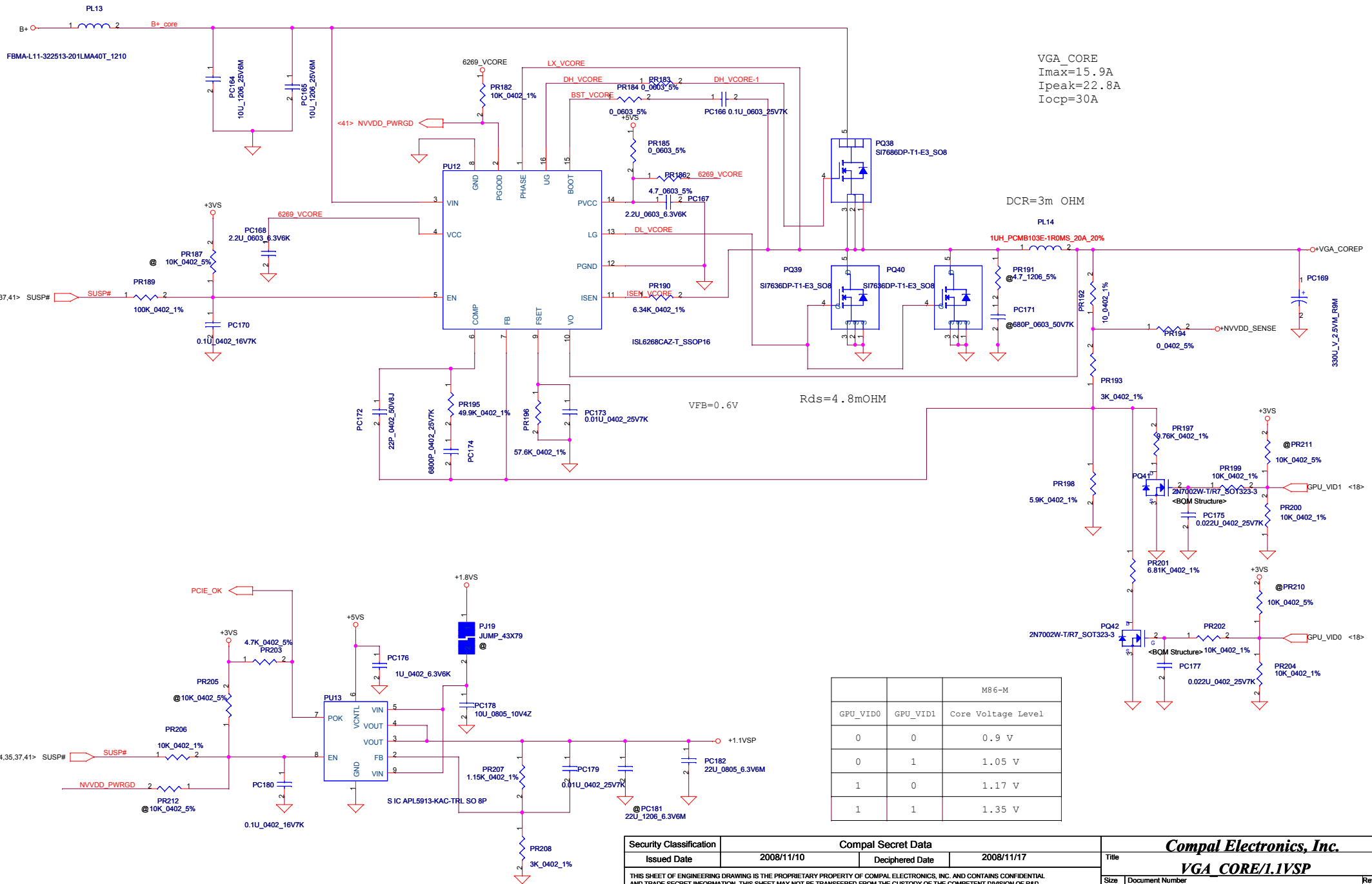
$C_{out} ESR = 15m\ ohm$
 $I_{peak} = 14.02A, I_{max} = 9.81A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * F_{sw}) = 2.4872A$
 $\Rightarrow 1/2 \Delta I = 1.243A$
 $V_{trip} = R_{trip} * I_{uA} = 17.8K * 10uA = 0.178V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.243A$
 $= 0.178 / (0.0115 * 1.2) + 1.243 = 12.898A + 1.243A = 14.141A$
 $I_{ocpmax} = (0.178 / (0.009 * 1.1)) + 1.243A = 17.98A + 1.243A = 19.22A$
 $I_{ocp} = 14.141A \sim 19.22A$



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VGA_CORE
 I_{max}=15.9A
 I_{peak}=22.8A
 I_{ocp}=30A

M86-M		
GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.05 V
1	0	1.17 V
1	1	1.35 V

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VGA CORE/1.1VSP		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	cpu load line fail	Measure cpu load line can't fit spec	0.2	49	change the resistance value of pr173.from 4.42k to 3.83k	2008/08/08	DVT
2	Change resistance size	EMI request	0.2	49	Change pc116 and pc117 size from 0402 to 0603	2008/08/08	DVT
3	Change p-mos part number	Vender change EOL	0.2	46	PQ12 part number from 4835bdy to 483500y	2008/08/08	DVT
4	Change device size	device too large can't fit layout space	0.2	44-50	PQ4, PQ14, PQ16, PQ18, PQ19, PQ20, PQ27, PQ36, PQ37, PQ41, PQ42 change to sot323-3	2008/08/12	DVT
5	Change resistance value	1.05V tranient fail	0.2	47	PR94 from 60.4k to 59k	2008/08/12	DVT
6	change resistance	for hdmi	0.2	45	pr41 change from 61.3k to 63.4k	2008/08/14	DVT
7							
8							
9							
10							
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				PIR (PWR)	
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A --> C Change List

- 1120-----
 Page 35,Chang
 R1745,R1746 to 4.7K SD028470180
- 1120-----
 Page 36,Add
 R106,R109,R1846,R1847 to 0R
- 1120-----
 Page 37,Add
 R1845 to 10K
- 1120-----
 Page 37,Add
 R49 to 1K, JP24 to ACES_88266_02001
- 1217-----
 Page 42,Delete
 R1814,R1815,R1816,R1817,R1818,R1819
- 0106-----
 Page 39, Delete D63 for Microsoft certification;
 Page 36, Delelte R1773, modify value or R1774, R1775 for LED color.

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