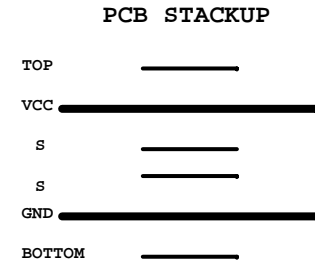
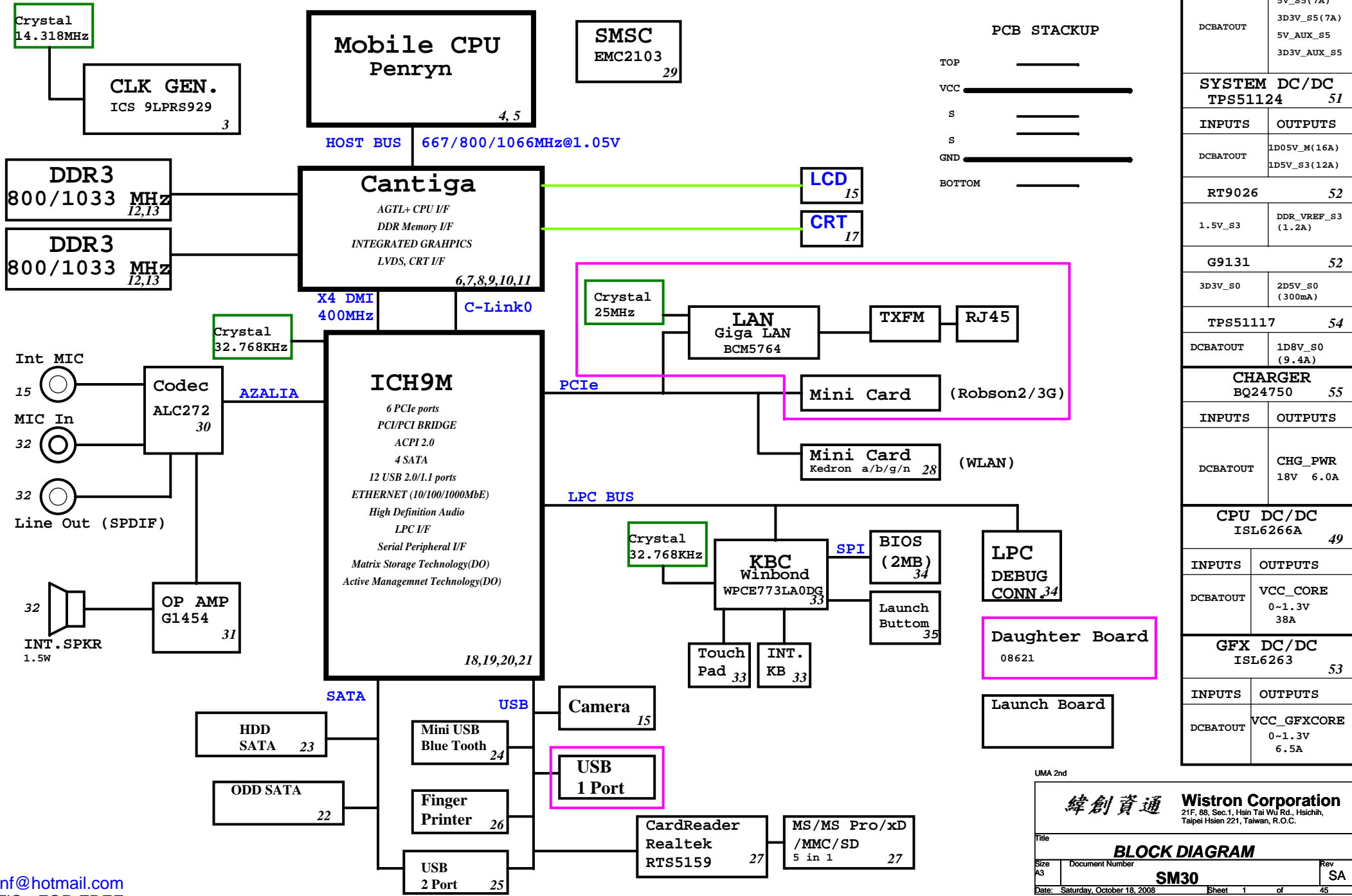


# SM30 Block Diagram

Project code: 91.4BT01.001  
 PCB P/N : 48.4BT01.001  
 Revision : 08239-SA



<b>SYSTEM DC/DC</b> TPS51125 50	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
<b>SYSTEM DC/DC</b> TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	LD05V_M(16A) LD5V_S3(12A)
RT9026 52	
1.5V_S3	DDR_VREF_S3 (1.2A)
G9131 52	
3D3V_S0	2D5V_S0 (300mA)
TPS51117 54	
DCBATOUT	1D8V_S0 (9.4A)
<b>CHARGER</b> BQ24750 55	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 1.8V 6.0A
<b>CPU DC/DC</b> ISL6266A 49	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A
<b>GFX DC/DC</b> ISL6263 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

UMA 2nd

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Title: **BLOCK DIAGRAM**

Size A3 Document Number **SM30** Rev SA

Date: Saturday, October 18, 2008 Sheet 1 of 45

# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

# ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/IHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

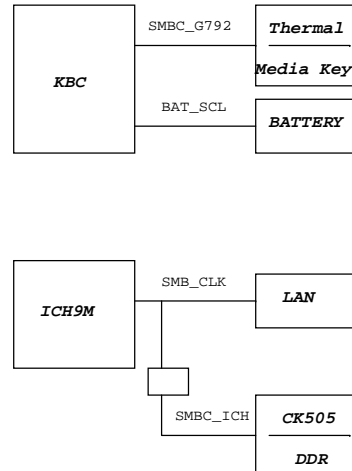
### NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

## SMBus

### USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	NC
3	MINIC2(WLAN)
4	CAMERA
5	NC
6	FingerPrint
7	BLUETOOTH
8	NC
9	USB1(IO board)
10	MINIC1(IO BOARD)
11	CARD READER

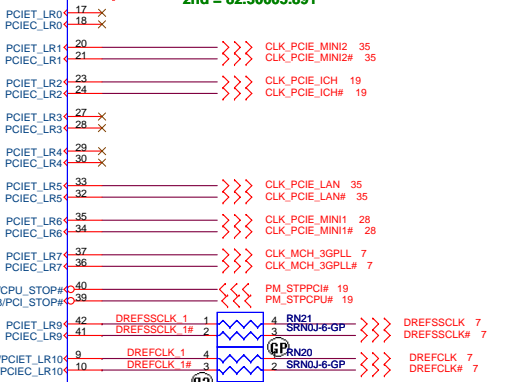
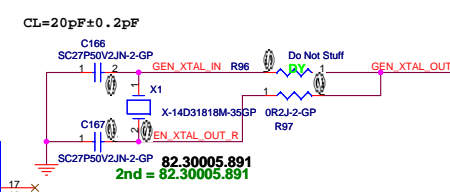
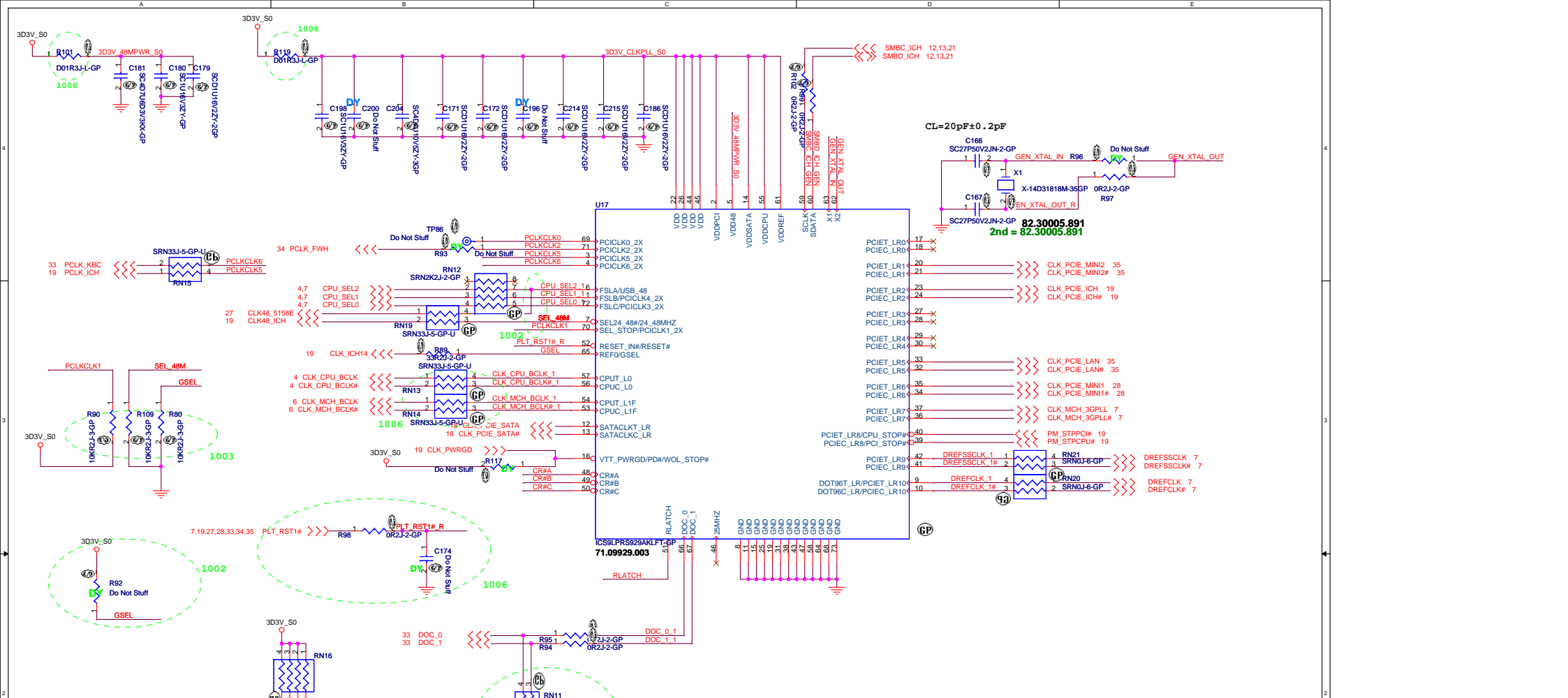


## PCIE Routing

LANE1	LAN BCM5764
LANE2	MiniCard WLAN
LANE3	MiniCard(Robson2G/3G)

UMA 2nd

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<b>Reference</b>			
Title	Document Number	Rev	SA
	<b>SM30</b>		
Date: Saturday, October 16, 2008	Sheet 2 of 45		



SEL2 FSLC	SEL1 FSLB	SEL0 FSLA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

GSEL	DOT Freq
0	100MHZ
1	96MHZ

SEL_STOP	Selects pin 39/40
0	PCI_STOP#/CPU_STOP#
1	PCIEX outputs

SEL24_48# / 24_48MHZ	OUTPUT
0	24MHZ
1	48MHZ

DOC_0	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

DOC_1	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

UMA 2nd

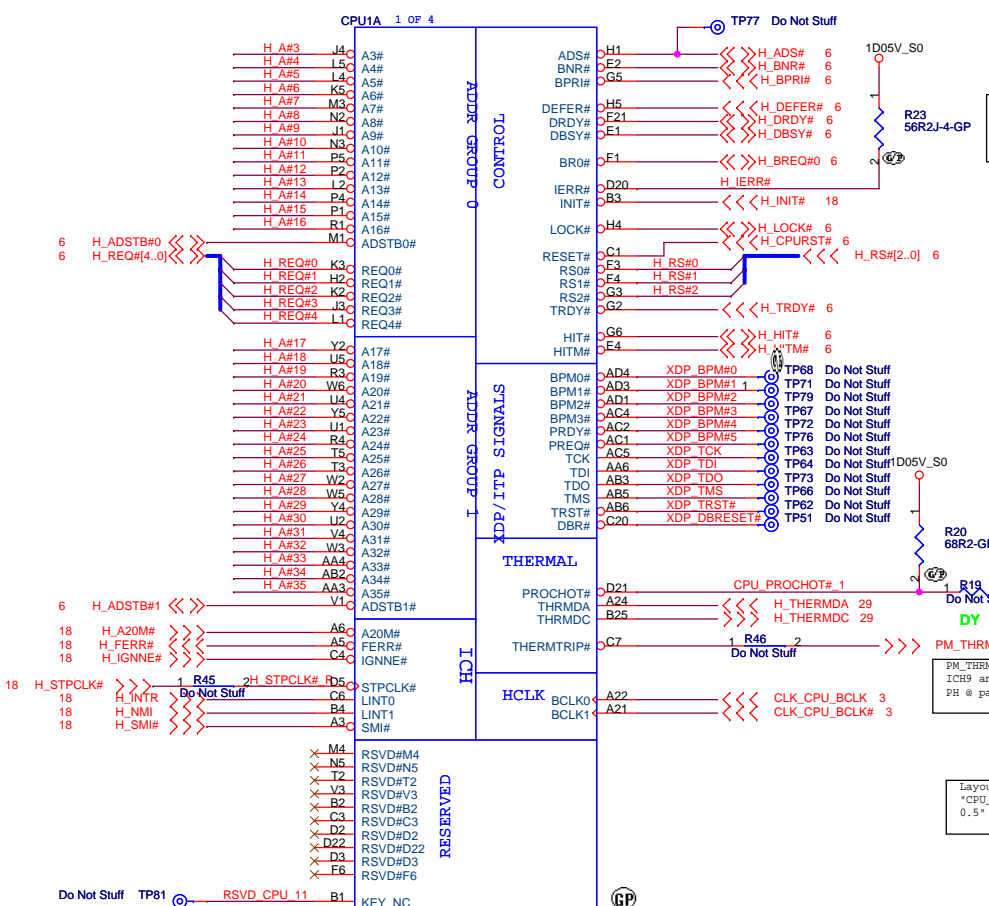
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Title: **Clock Generator**

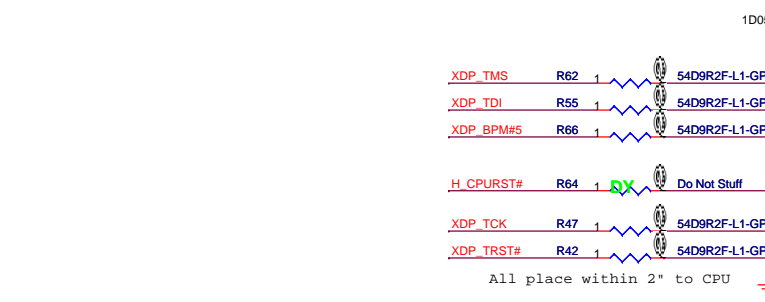
Size: Document Number **SM30** Rev **SA**

Date: Monday, October 27, 2008 Sheet 3 of 45

6 H\_A#(35..3) <<<>>> H\_A#(35..3)



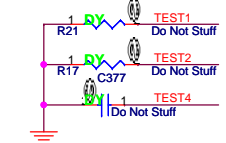
BGA479-SKT-8-GP-U3  
**62.10053.401**  
 2nd: 62.10053.401



Place testpoint on H\_IERR# with a GND 0.1" away

PM\_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48

Layout Note: "CPU\_GTLREF0" 0.5" max length.

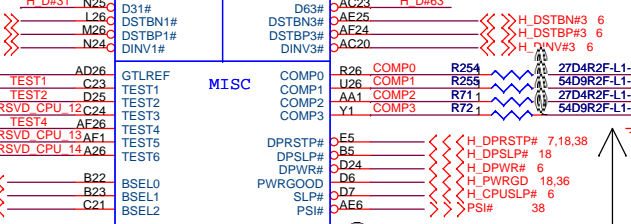
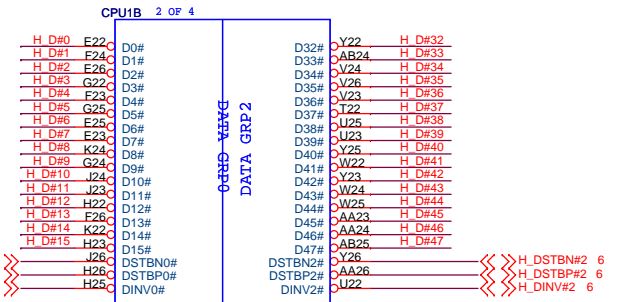


Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

H DPRSTP# TP50 Do Not Stuff  
 H DPSP# TP156 Do Not Stuff  
 H DPWR# TP47 Do Not Stuff  
 H PWRGD# TP61 Do Not Stuff  
 H CPUSLP# TP60 Do Not Stuff  
 H INIT# TP157 Do Not Stuff  
 H CPURST# TP75 Do Not Stuff

Place these TP on button-side, easy to measure.

H DINV#[3..0] <<>> H\_DINV#[3..0] 6  
 H\_DSTBN#[3..0] <<>> H\_DSTBN#[3..0] 6  
 H\_DSTBP#[3..0] <<>> H\_DSTBP#[3..0] 6  
 H\_D#(63..0) <<>> H\_D#(63..0) 6



Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

UMA 2nd

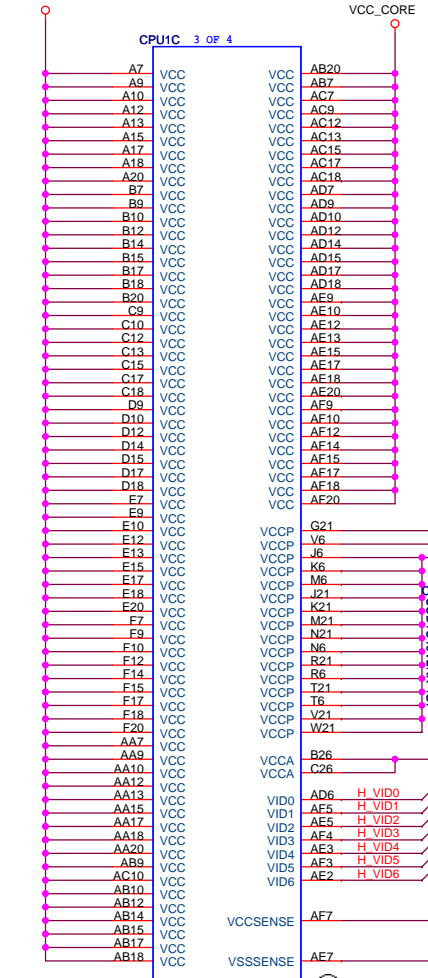
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Title: **CPU (1 of 2)**

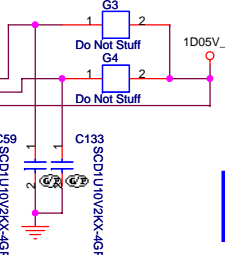
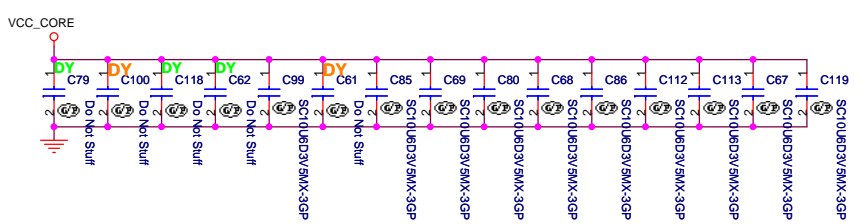
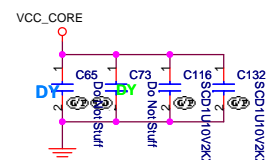
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Date: Saturday, October 18, 2008 Sheet 4 of 45

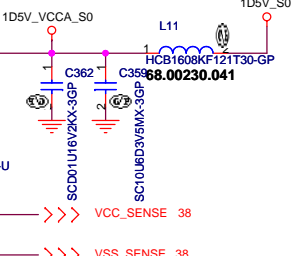
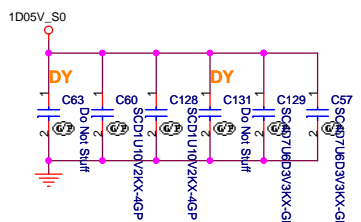
VCC\_CORE



BGA479-SKT-8-GP-U3  
62.10053.401



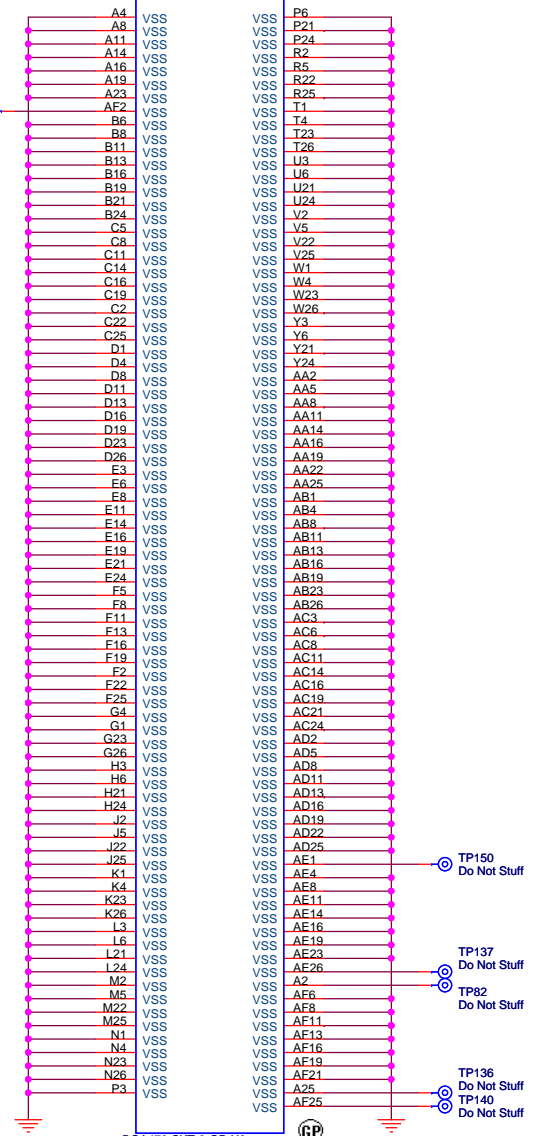
layout note: "1D5V\_VCCA\_S0 as short as possible"



Layout Note:  
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:  
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

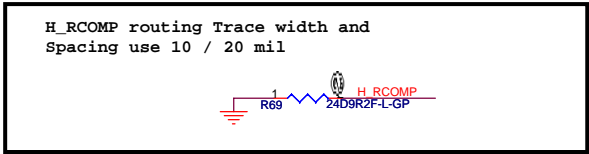
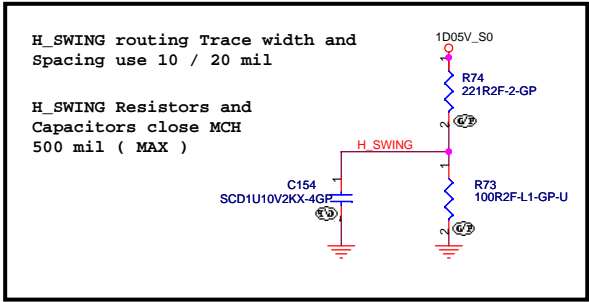
CPU1D 4 OF 4



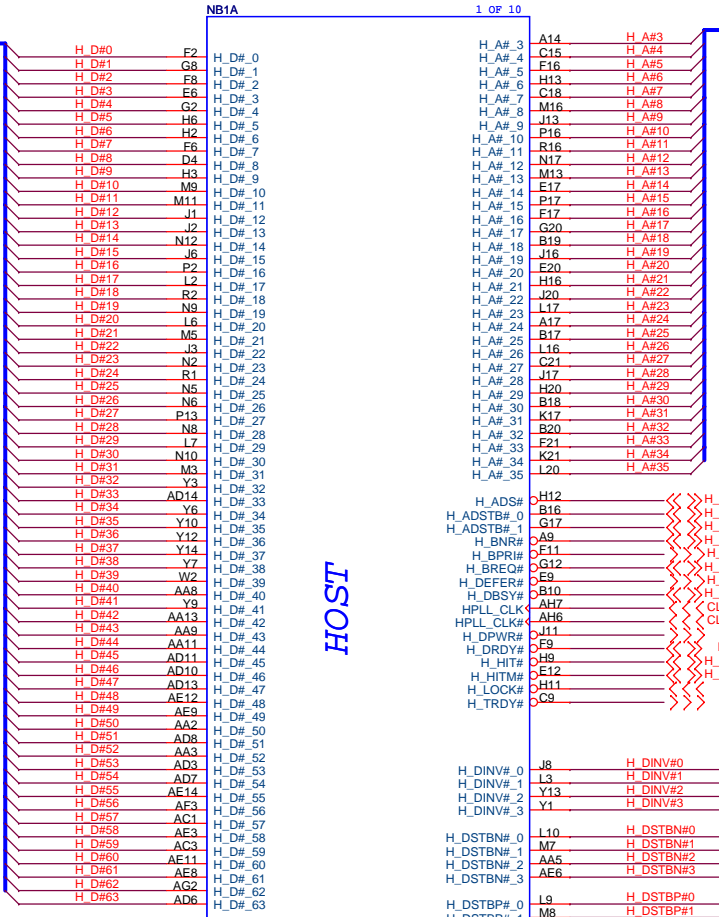
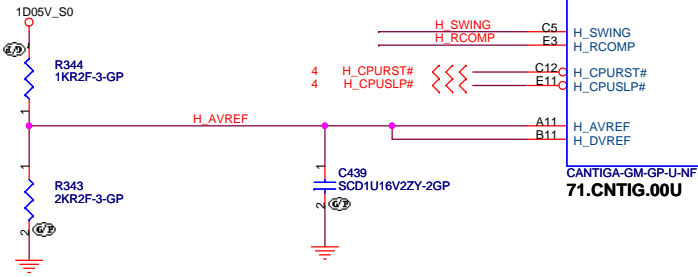
BGA479-SKT-8-GP-U3  
62.10053.401

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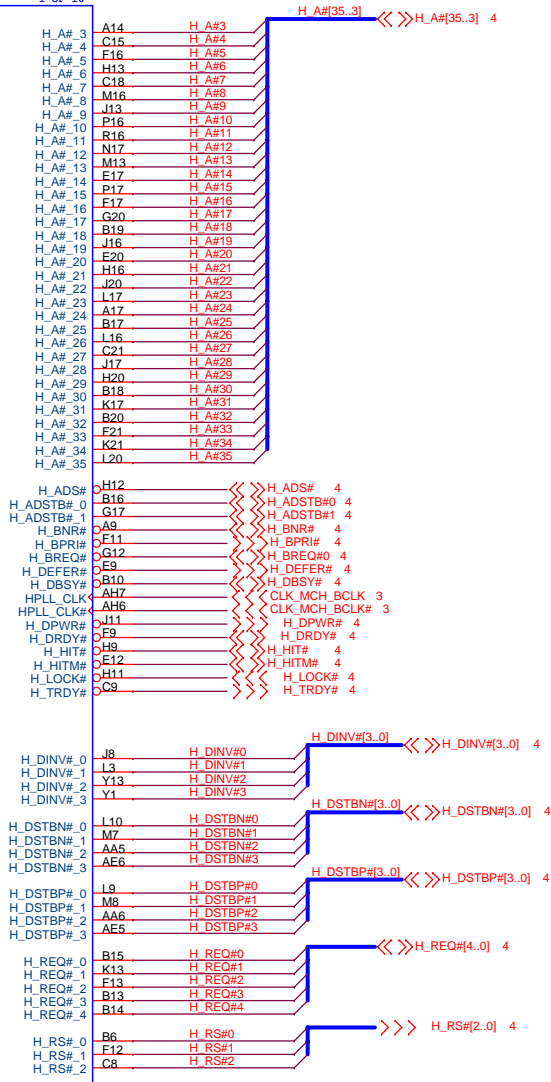
Title <b>CPU (2 of 2)</b>		
Size	Document Number	Rev SA
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Place them near to the chip ( < 0.5" )



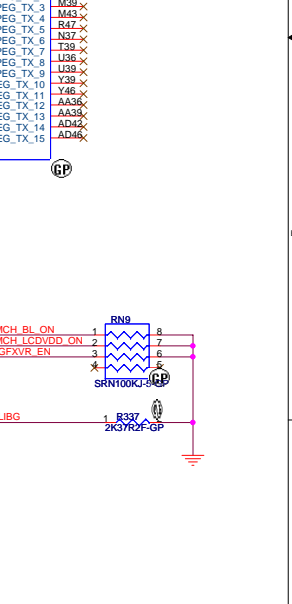
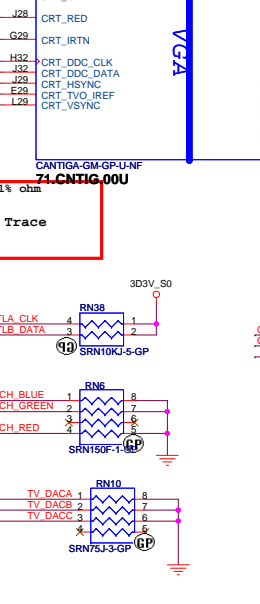
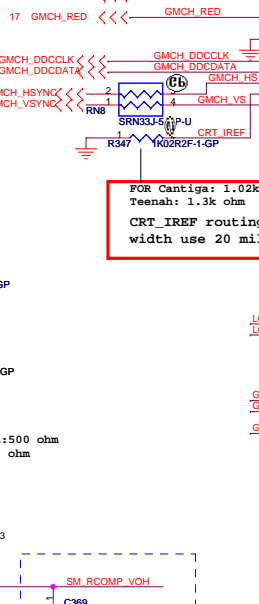
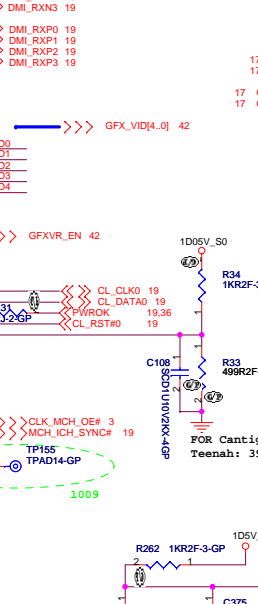
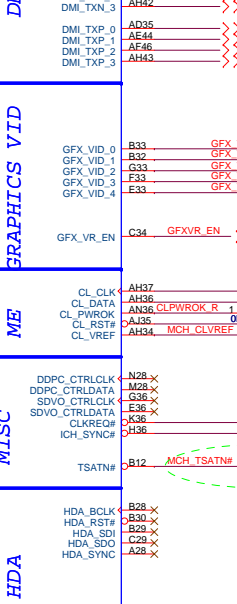
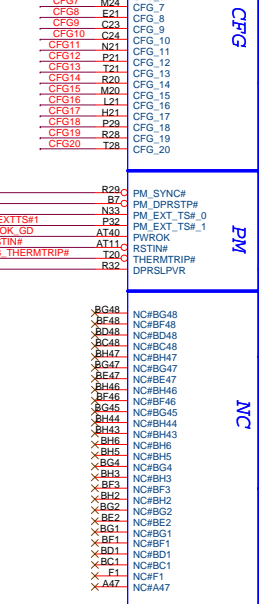
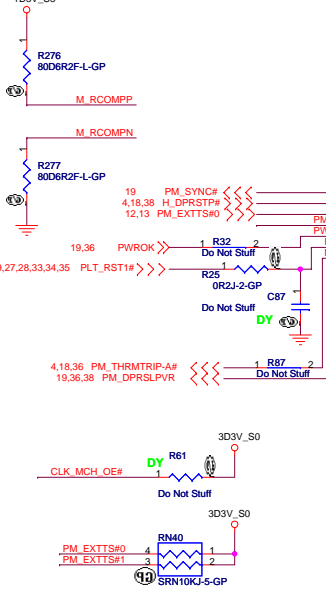
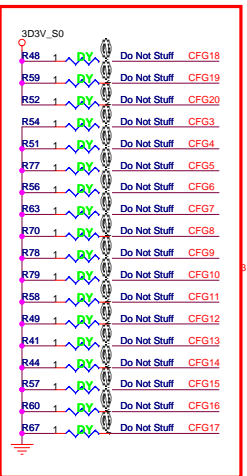
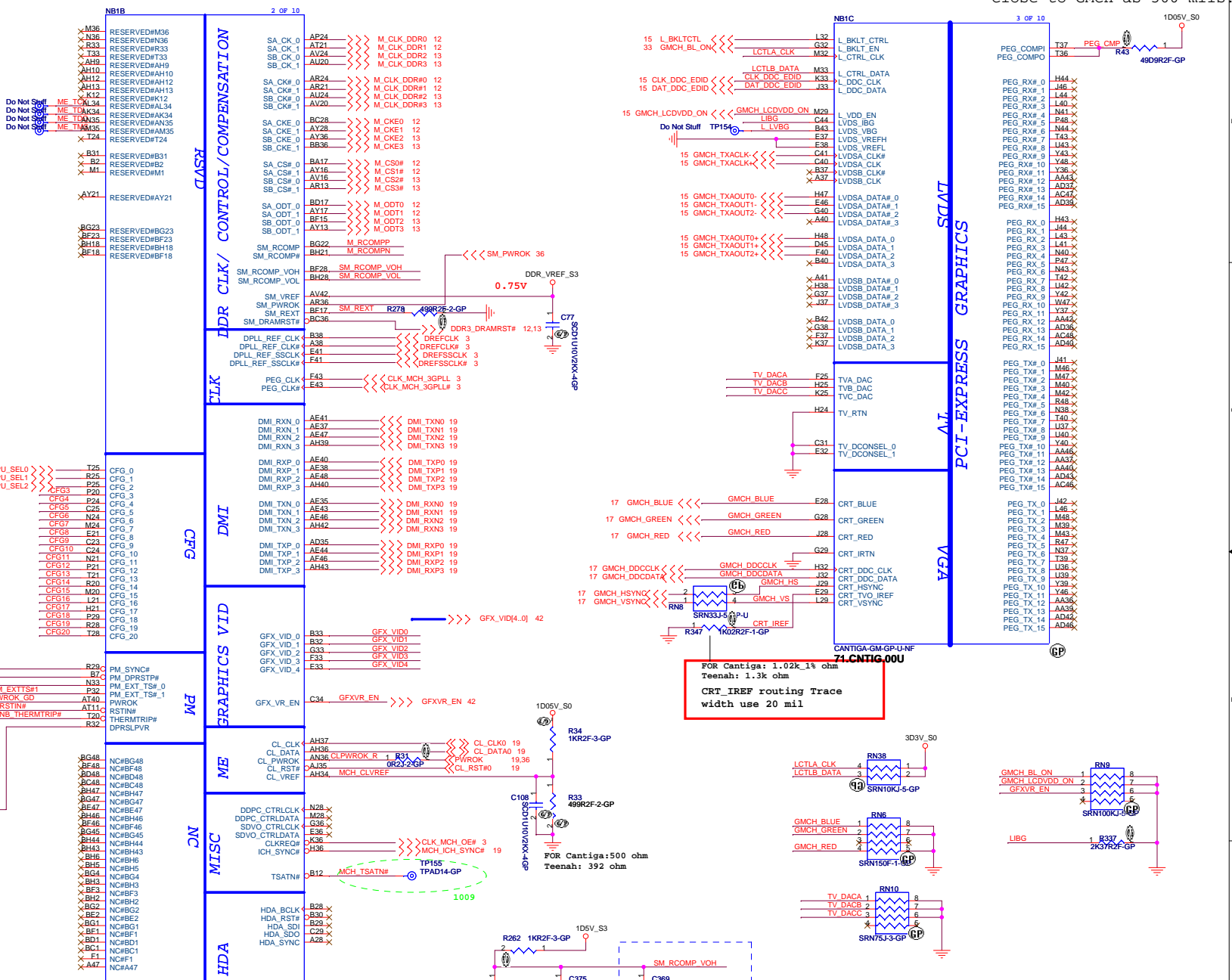
HOST

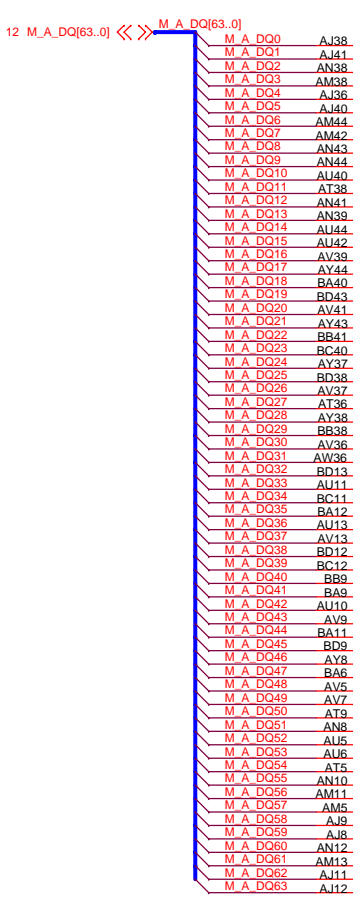


# Strap Pin Table

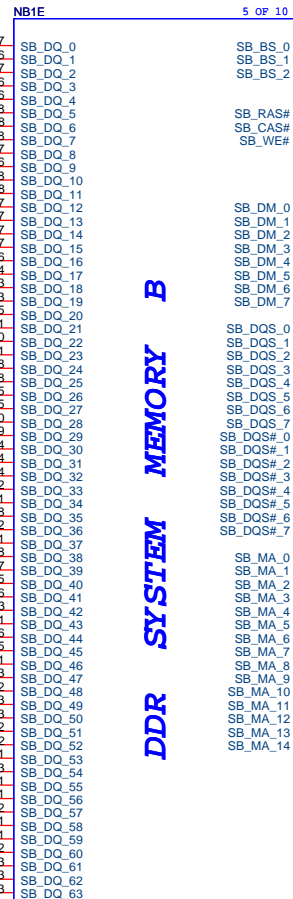
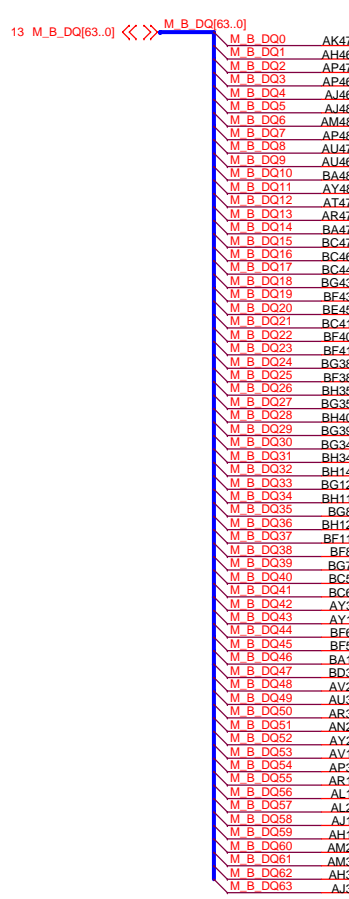
CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz	011 = FSB 667MHz Others = Reserved
CFG4:3, 8, 11, 14:15; 17; 18	Reserved	
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *	
CFG6 (ITPM Host Interface)	Low = The ITPM Host Interface is disabled High = The ITPM Host Interface is enabled *	
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality	
CFG9 (PCIe Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation: Lane Numbered in Order *	
CFG10 (PCIe Loopback enable)	Low = Enabled High = Disabled *	
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *	
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *	
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *	
CFG19 (DMI Lane Reversal)	Low = Normal operation: Lane Numbered in Order High = Reverse Lanes DMI x 4 mode[MCH->CH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->CH]: (3->0, 2->1)	
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIe)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIe is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port	
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present	
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIe disabled	
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present	

Close to GMCH as 500 mils.



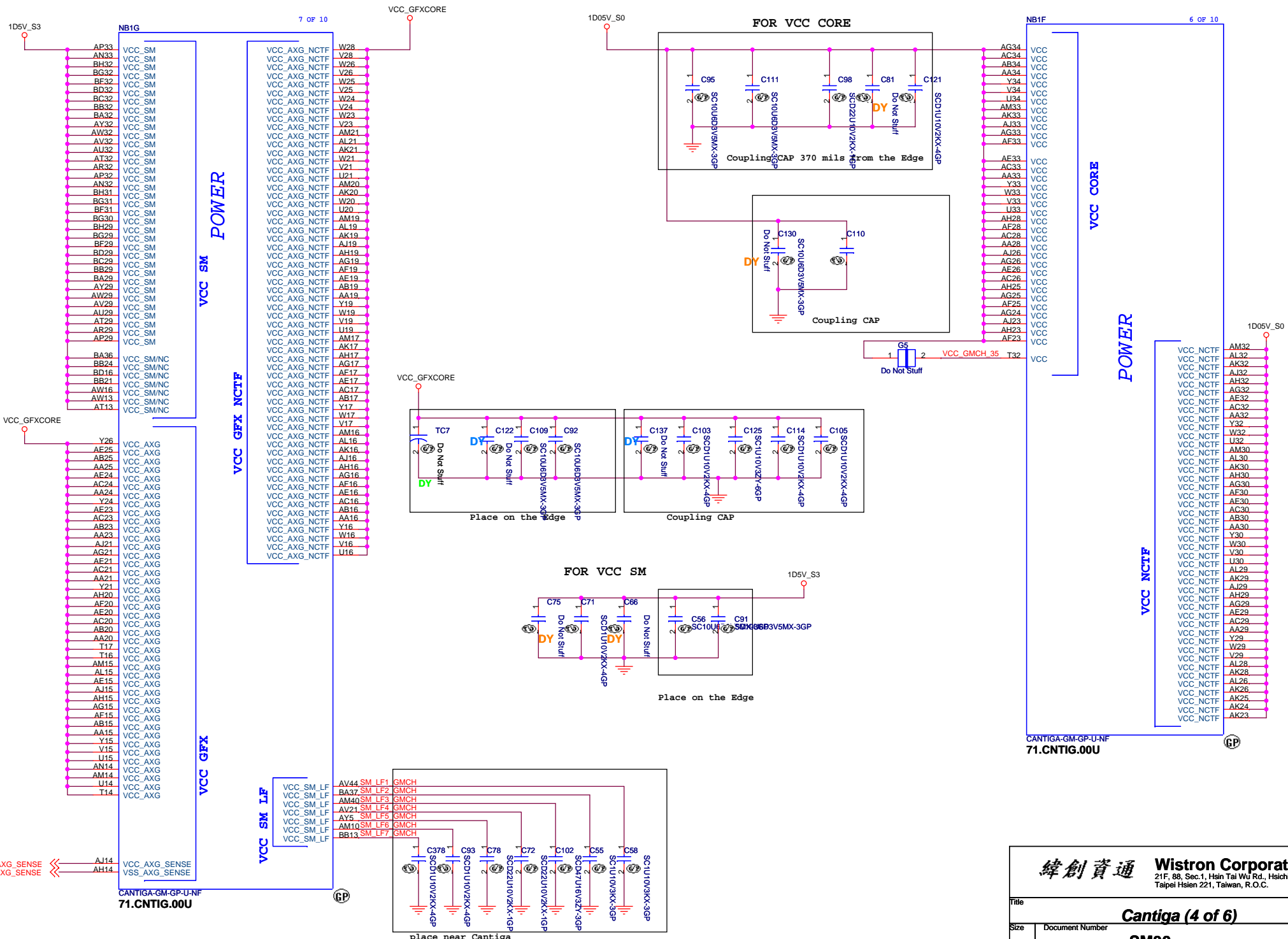


CANTIGA-GM-GP-U-NF  
 71.CNTIG.00U



CANTIGA-GM-GP-U-NF  
 71.CNTIG.00U





42 VCC\_AXG\_SENSE <<< AJ14  
 42 VSS\_AXG\_SENSE <<< AH14

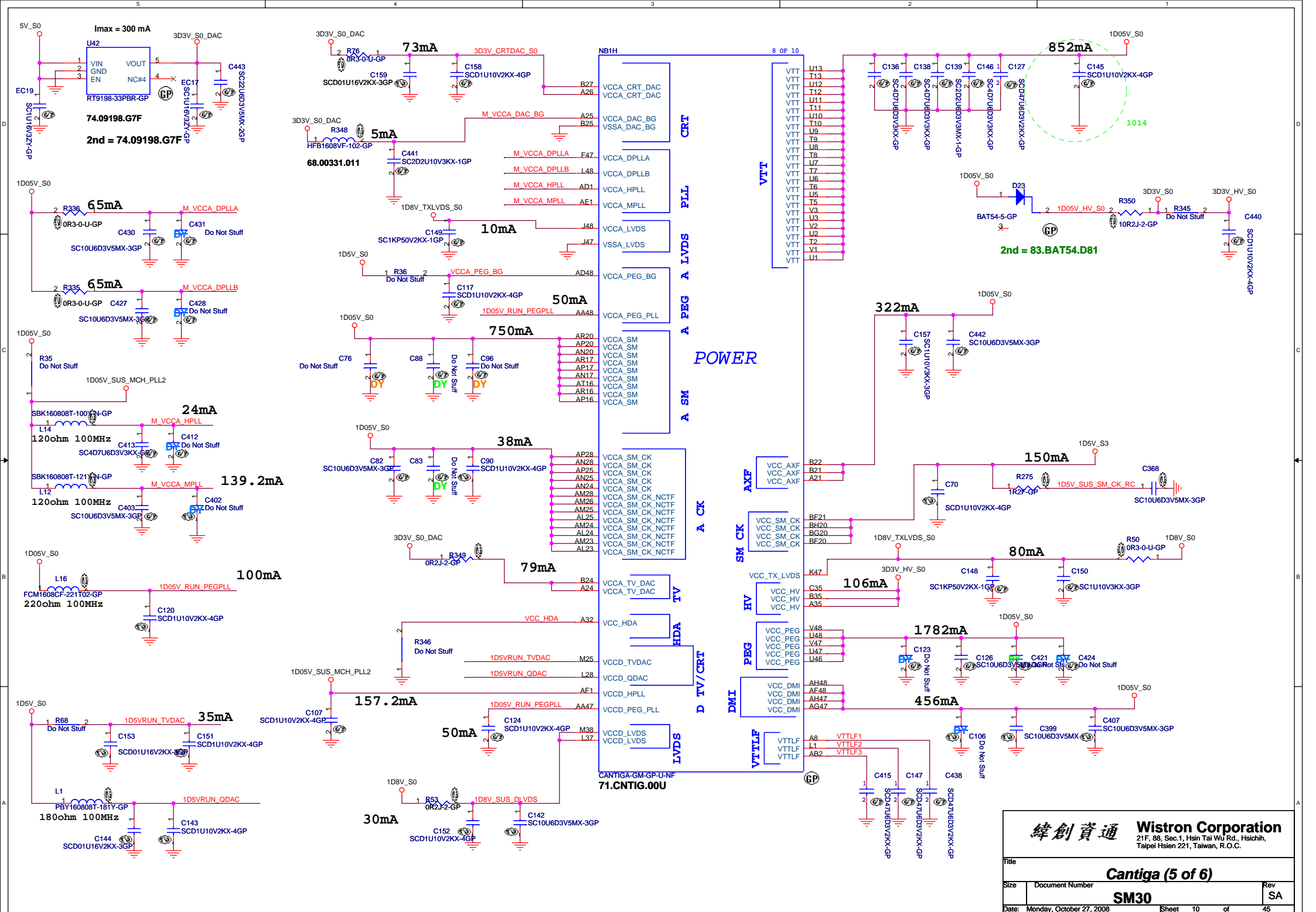
CANTIGA-GM-GP-U-NF  
 71.CNTIG.00U

VCC SM LF  
 VCC\_SM\_LF1 GMCH  
 VCC\_SM\_LF2 GMCH  
 VCC\_SM\_LF3 GMCH  
 VCC\_SM\_LF4 GMCH  
 VCC\_SM\_LF5 GMCH  
 VCC\_SM\_LF6 GMCH  
 VCC\_SM\_LF7 GMCH

place near Cantiga

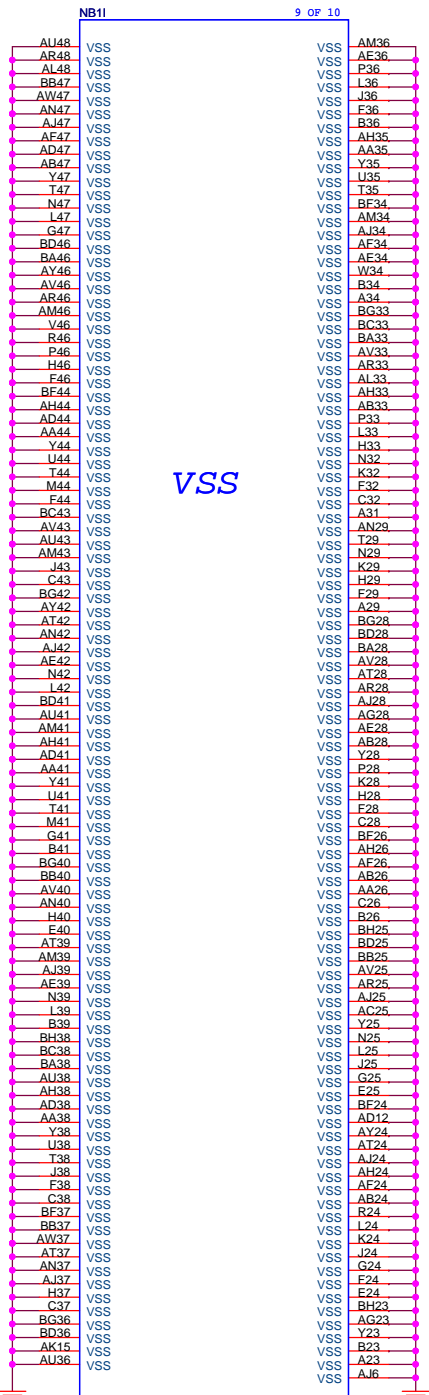
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Title		<b>Cantiga (4 of 6)</b>	
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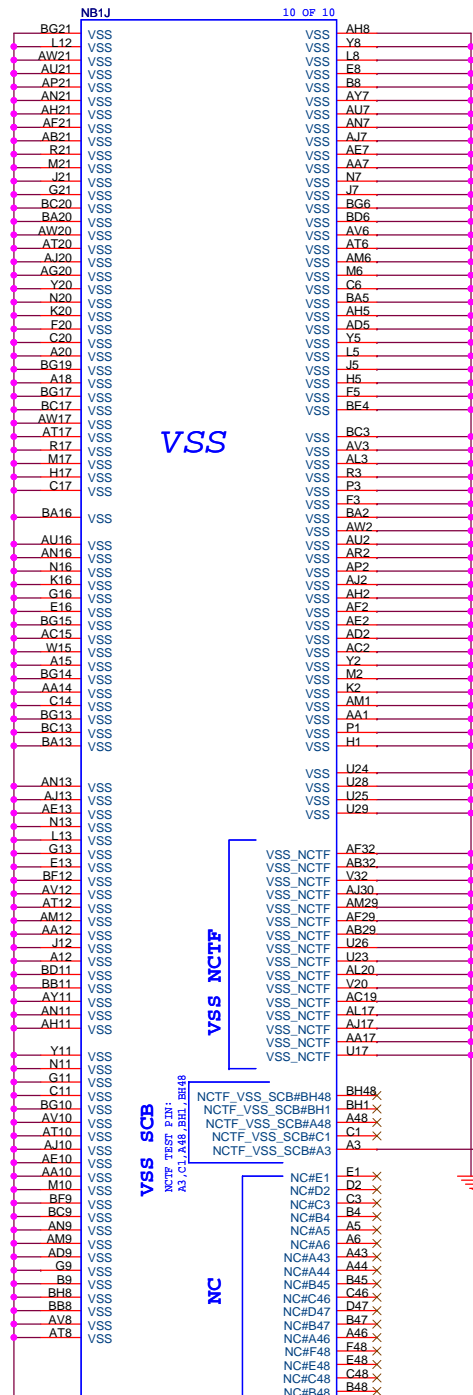


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Title		
<b>Cantiga (5 of 6)</b>		
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		<b>SA</b>
<b>SM30</b>		
Date: Monday, October 27, 2008	Sheet 10	of 45



CANTIGA-GM-GP-U-NF  
71.CNTIG.00U

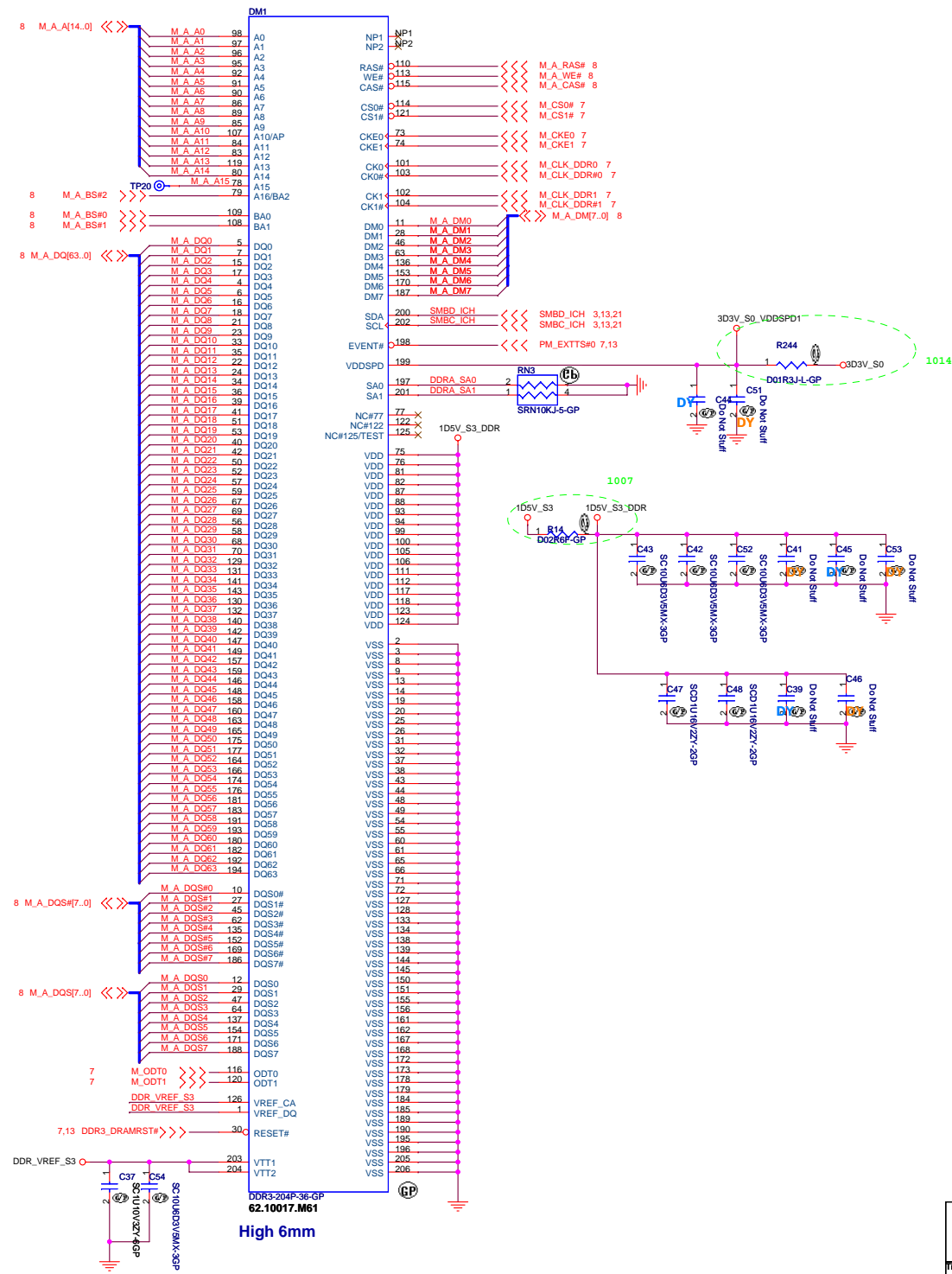


CANTIGA-GM-GP-U-NF  
71.CNTIG.00U

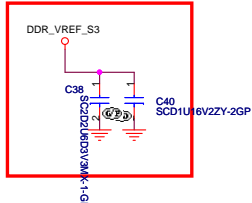


<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>Cantiga (6 of 6)</b>			
Size	Document Number	Rev	SA
<b>SM30</b>			
Date:	Saturday, October 18, 2008	Sheet	11 of 45

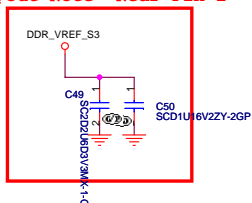
# DDR3 SOCKET\_1



Layout Note : Near Pin 126



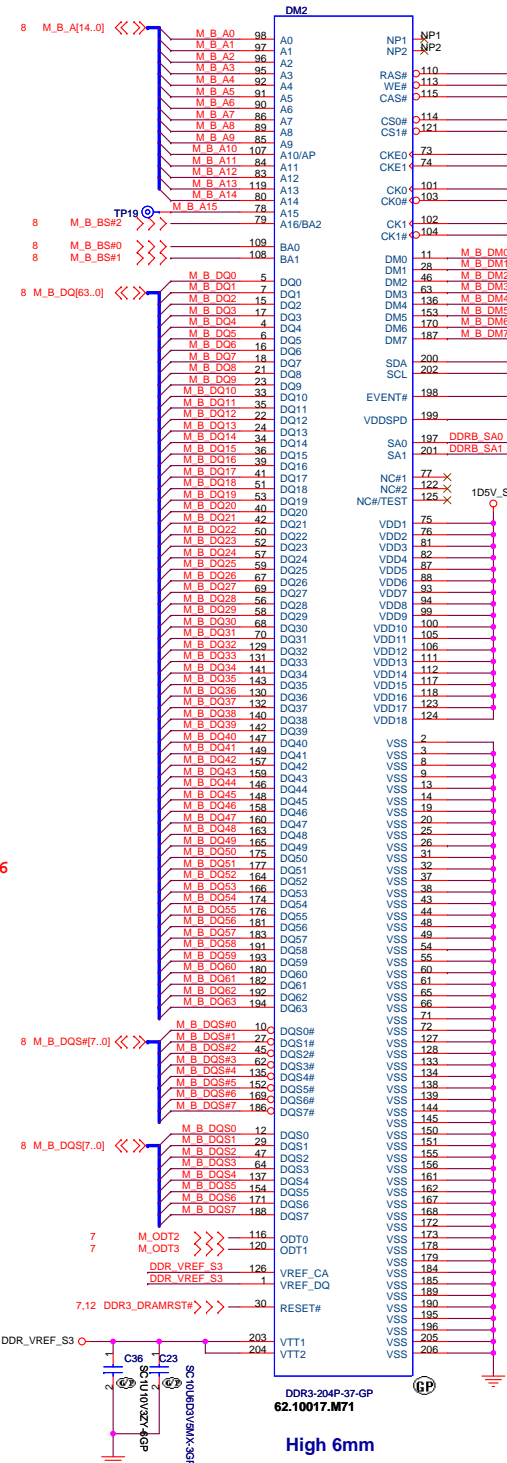
Layout Note : Near Pin 1



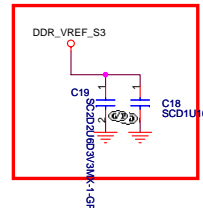
High 6mm

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File: <b>DDR3 Socket</b>	
Size: Document Number	Rev: SA
<b>SM30</b>	
Date: Monday, October 27, 2008	Sheet 12 of 45

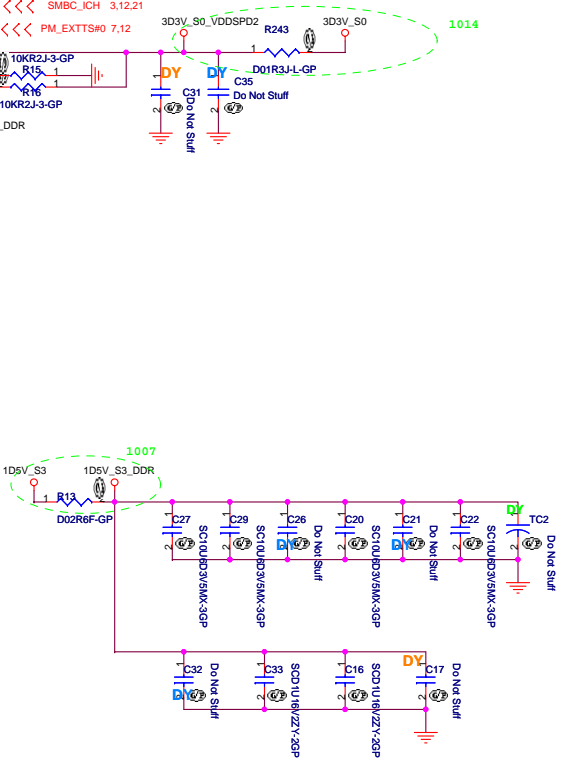
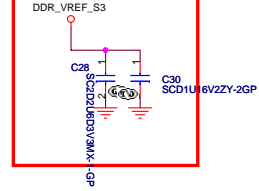
# DDR3 SOCKET\_2



Layout Note : Near Pin 126



Layout Note : Near Pin 1



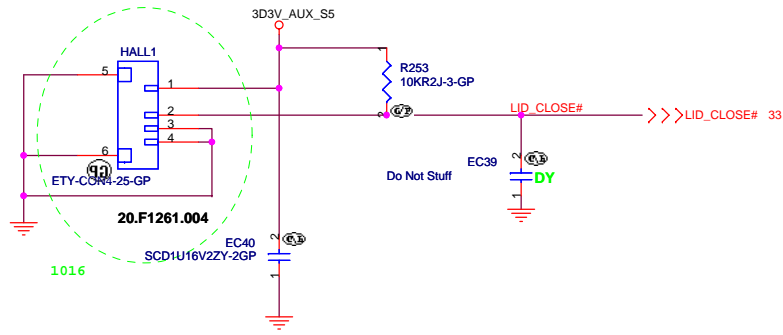
High 6mm

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

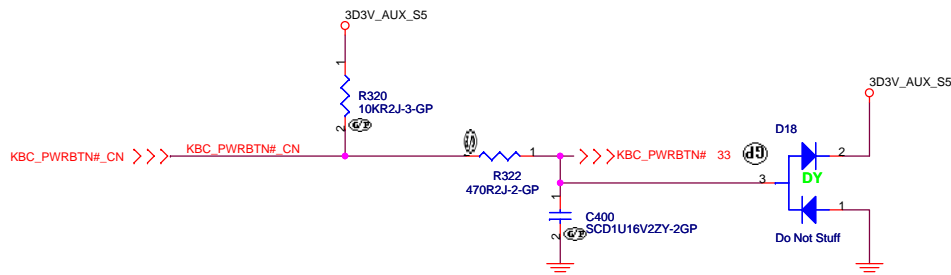
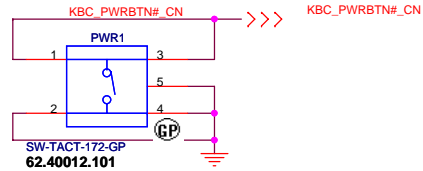
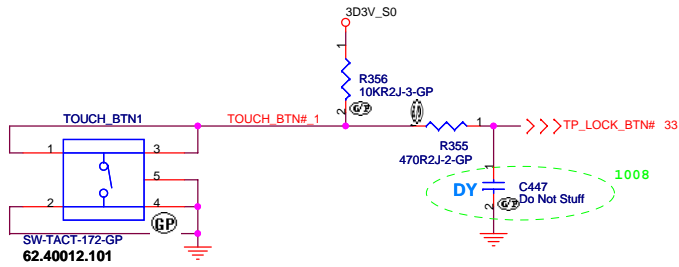
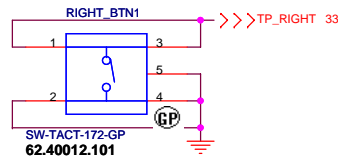
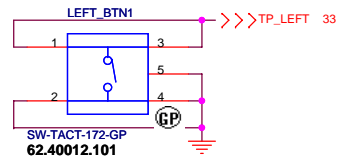
Title		
DDR3 Termination Resistor		
Size	Document Number	Rev
	SM30	SA
Date:	Monday, October 27, 2008	Sheet 13 of 45

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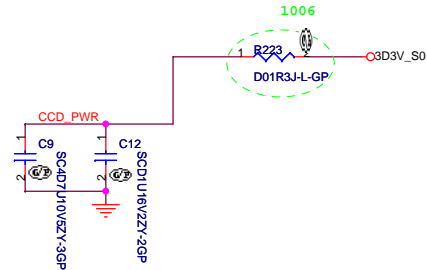
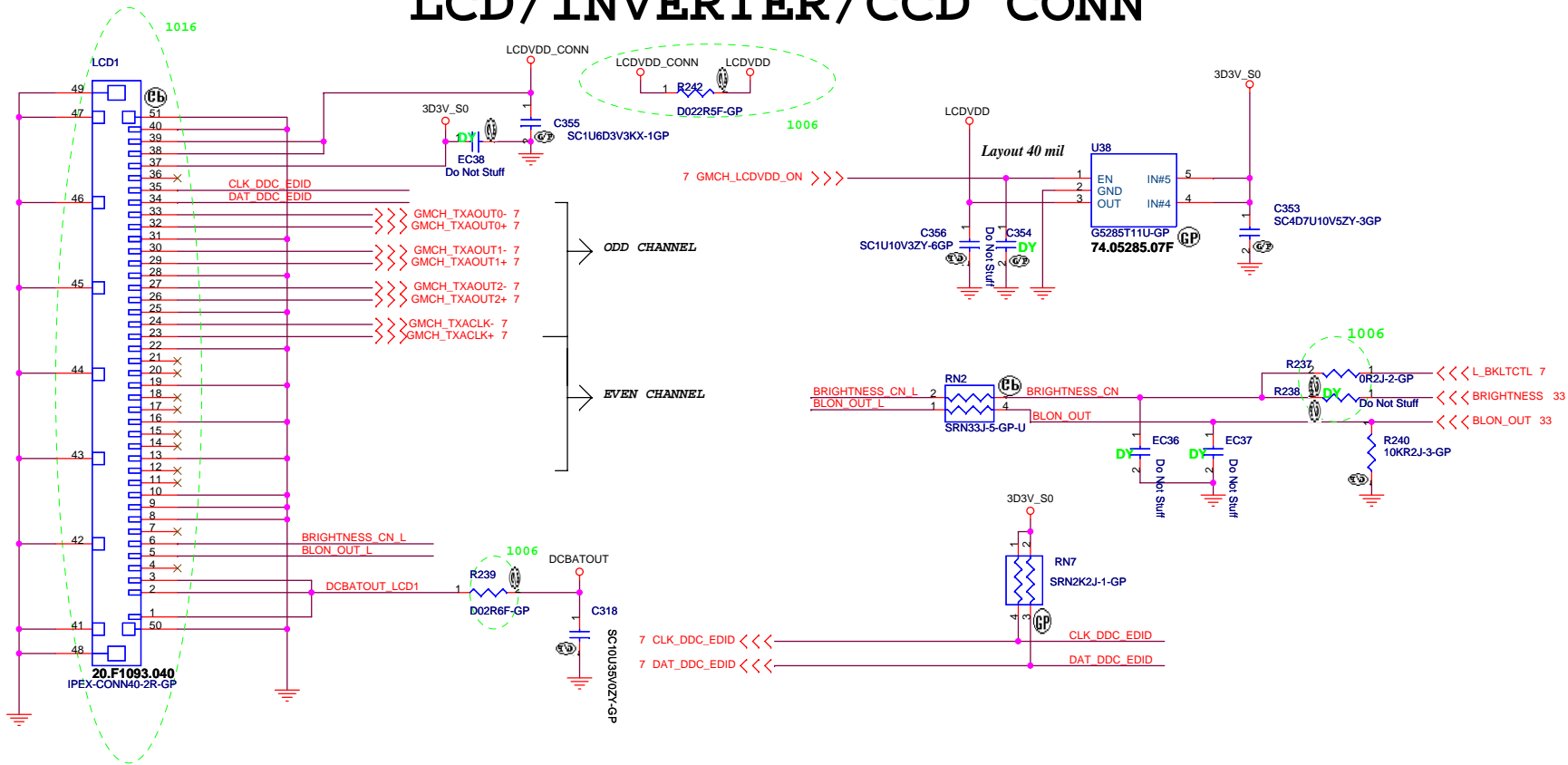
# Cover Up Switch



74.00268.A7B  
74.00268.C7B

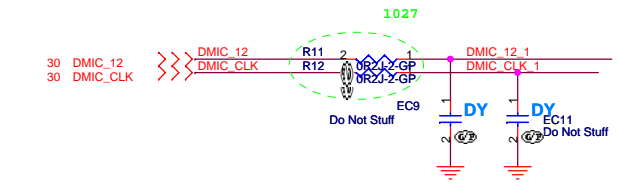
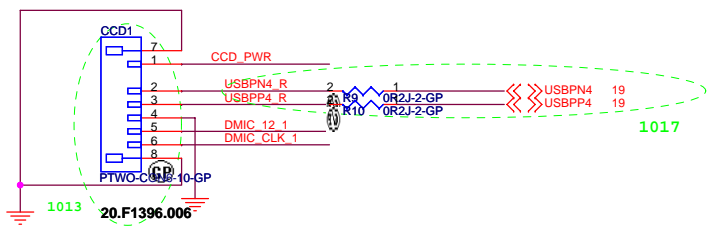


# LCD/INVERTER/CCD CONN



CCD1 Conn. Test Point

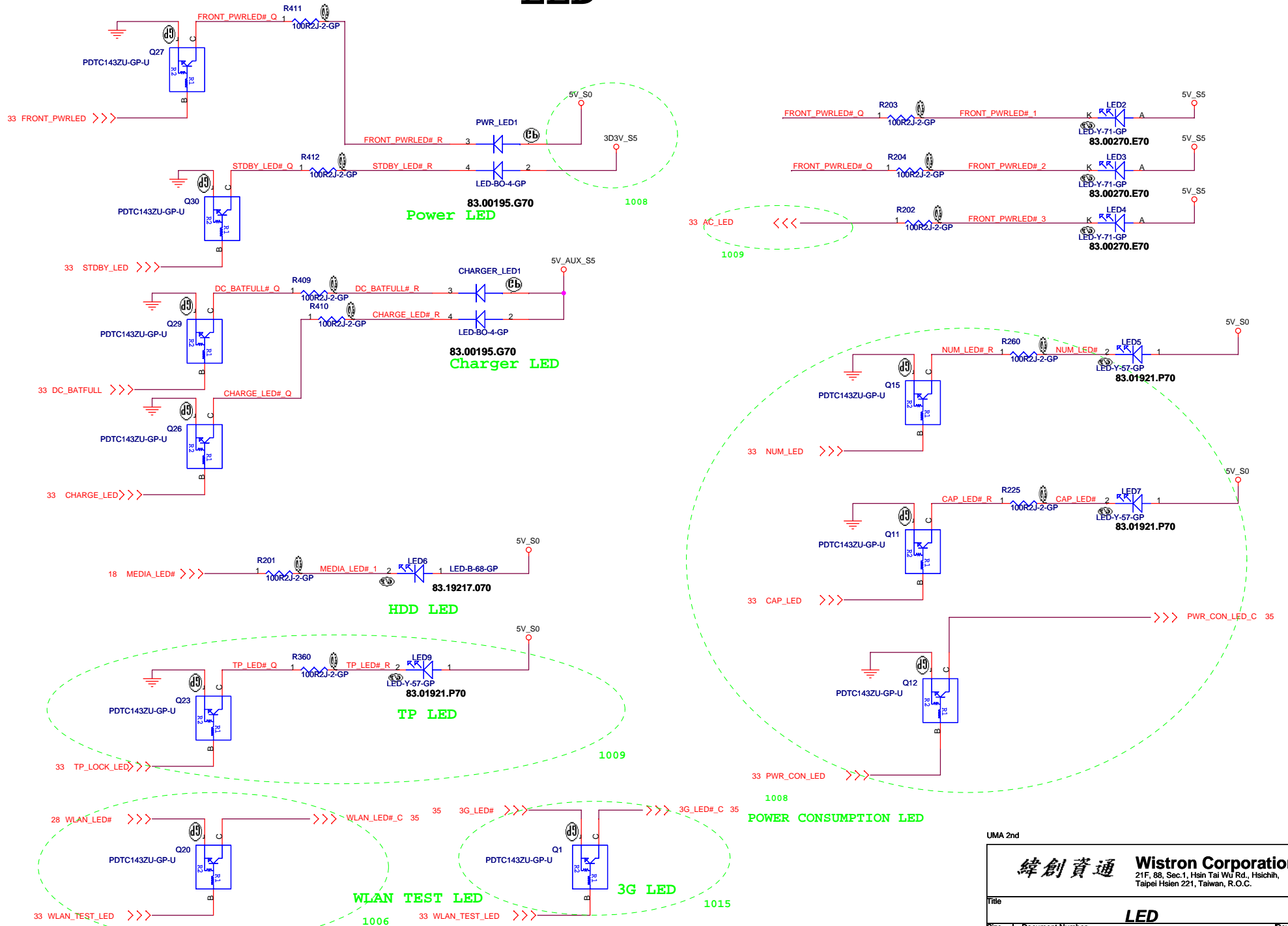
- CCD\_PWR 1 TP11 Do Not Stuff
- USBPN4\_R 1 TP15 Do Not Stuff
- USBPP4\_R 1 TP14 Do Not Stuff
- DMIC\_CLK\_1 1 TP17 Do Not Stuff
- DMIC\_12\_1 1 TP16 Do Not Stuff



UMA 2nd

<b>緯創資通 Wistron Corporation</b>	
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<b>Title LCD CONN</b>	
<b>Size</b>	<b>Document Number SM30</b>
<b>Date:</b> Monday, October 27, 2008	<b>Rev SA</b>
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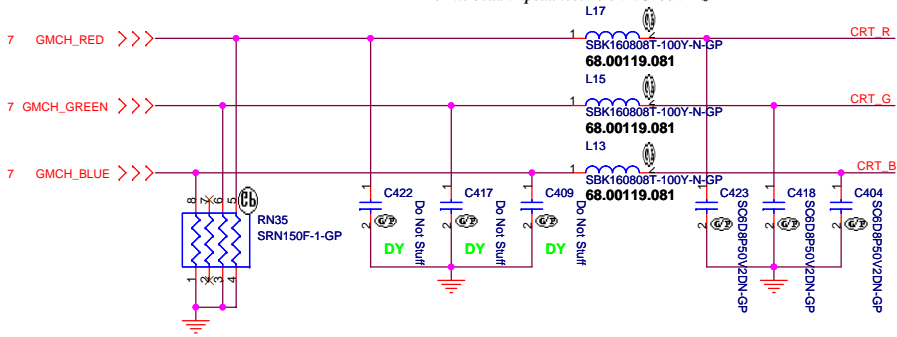
# LED





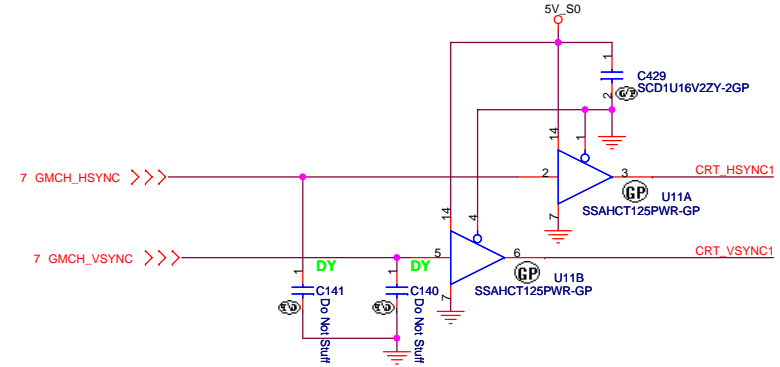
Layout Note:  
Place these resistors  
close to the CRT-out  
connector

Ferrite bead impedance: 10 ohm@100MHz.

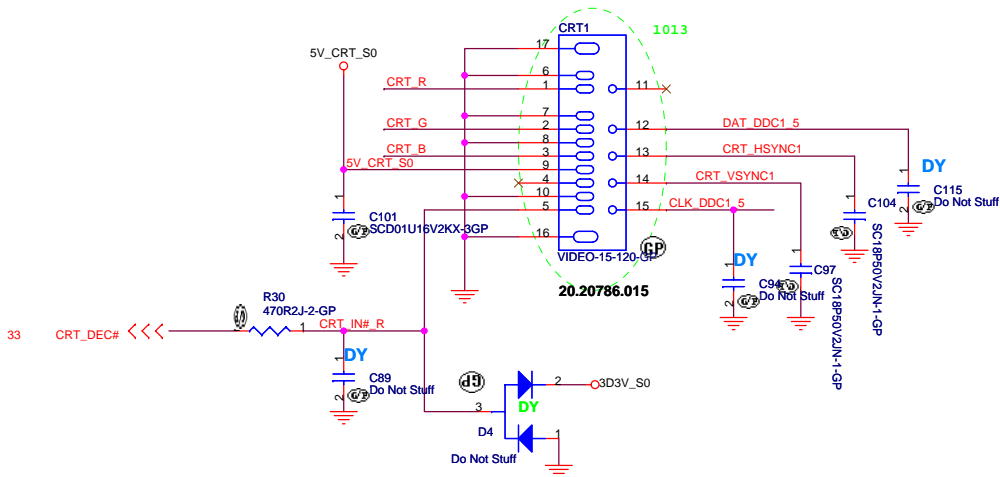


Layout Note:  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

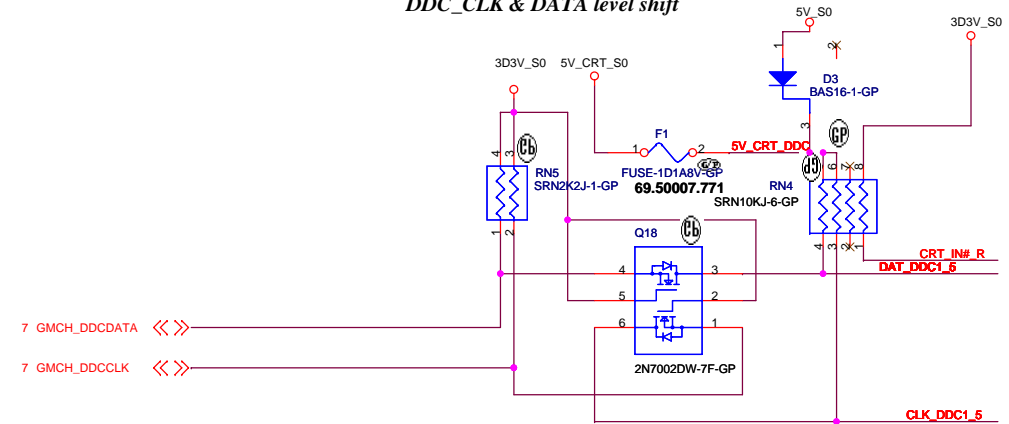
### Hsync & Vsync level shift



## CRT I/F & CONNECTOR



### DDC\_CLK & DATA level shift

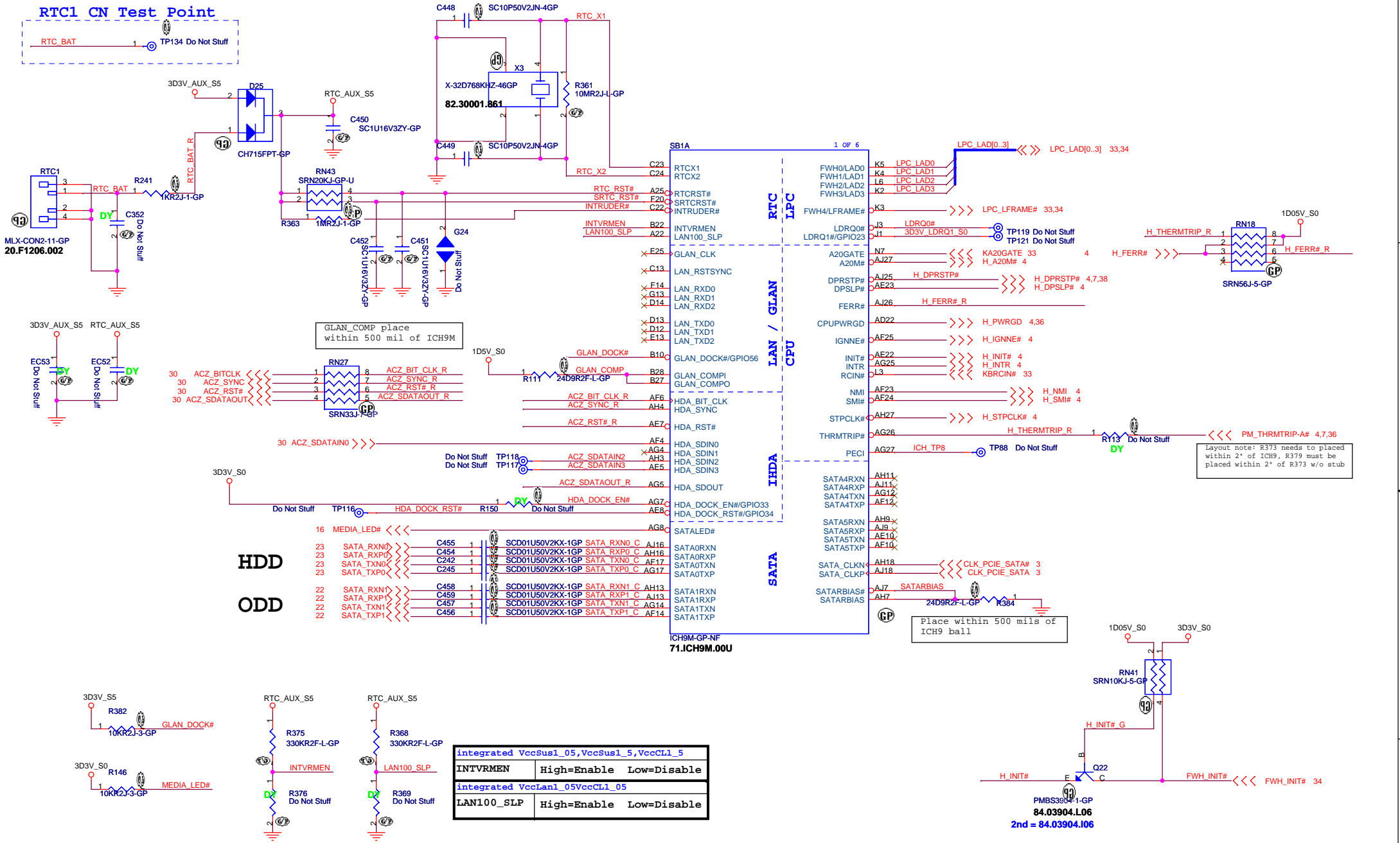
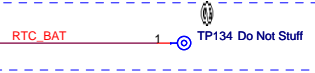


UMA 2nd

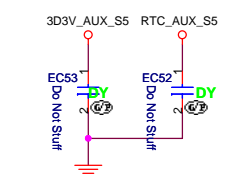
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>CRT CONN</b>	
Size	Document Number	Rev SA	
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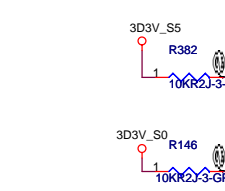
**RTC1 CN Test Point**



MLX-CON2-11-GP  
20.F1206.002



**HDD**  
**ODD**



integrated VccSus1\_05, VccSus1\_5, VccCLI\_5

INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCLI_05	
LAN100_SLP	High=Enable Low=Disable

integrated VccLan1\_05VccCLI\_05



integrated VccLan1\_05VccCLI\_05

Layout note: R373 needs to be placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub

Place within 500 mils of ICH9 ball

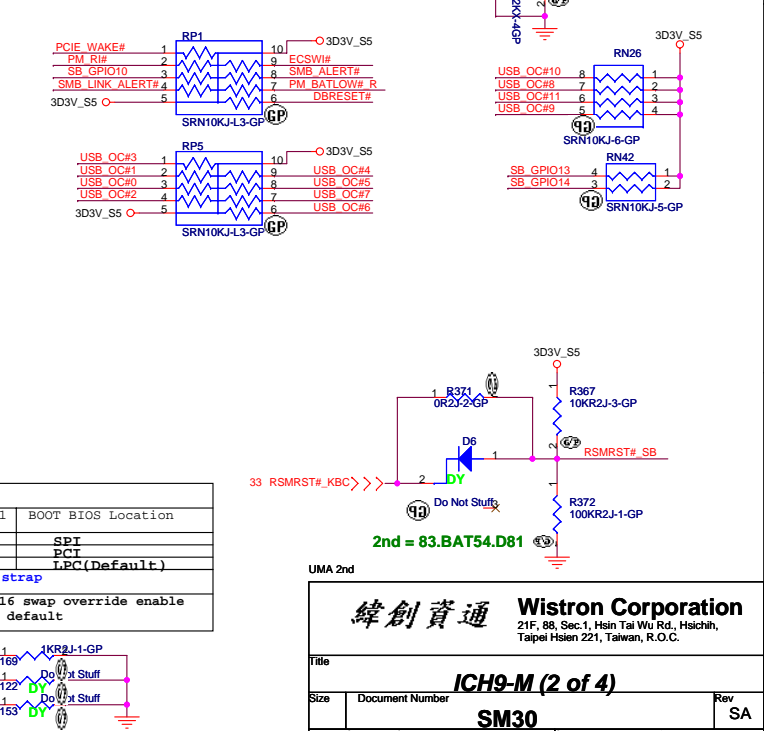
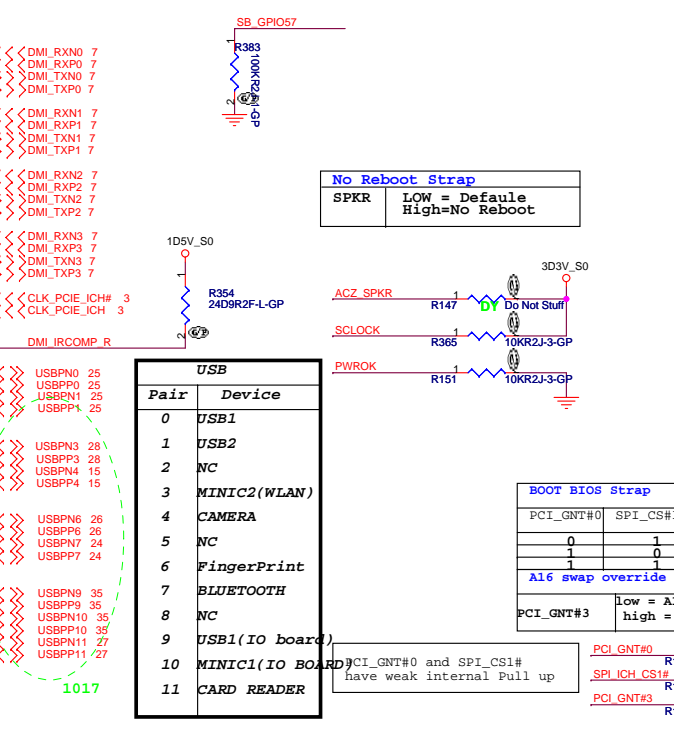
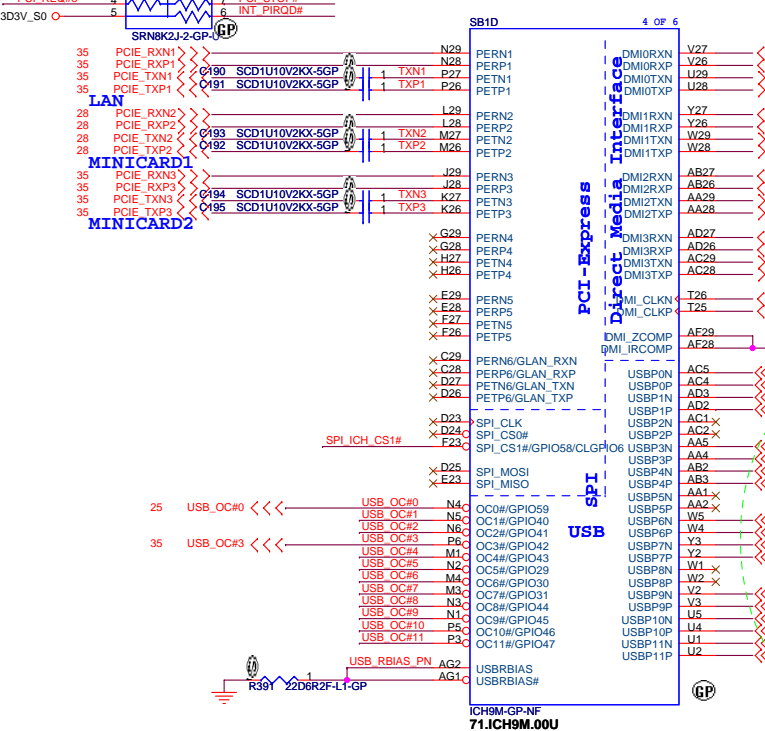
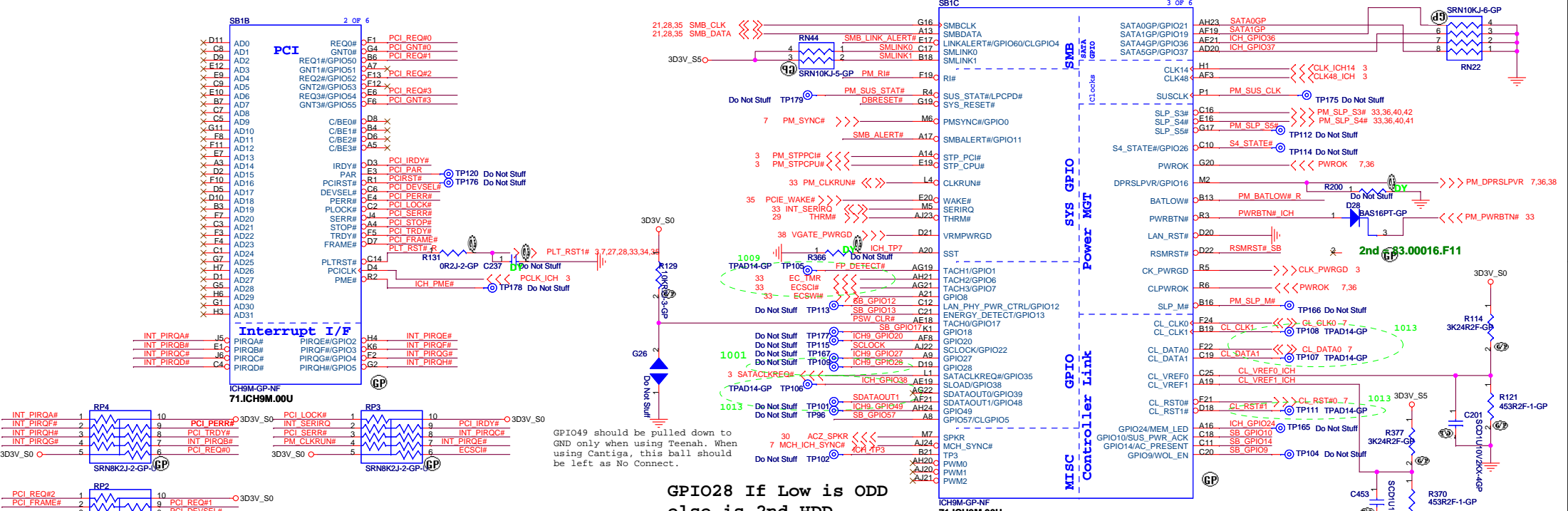
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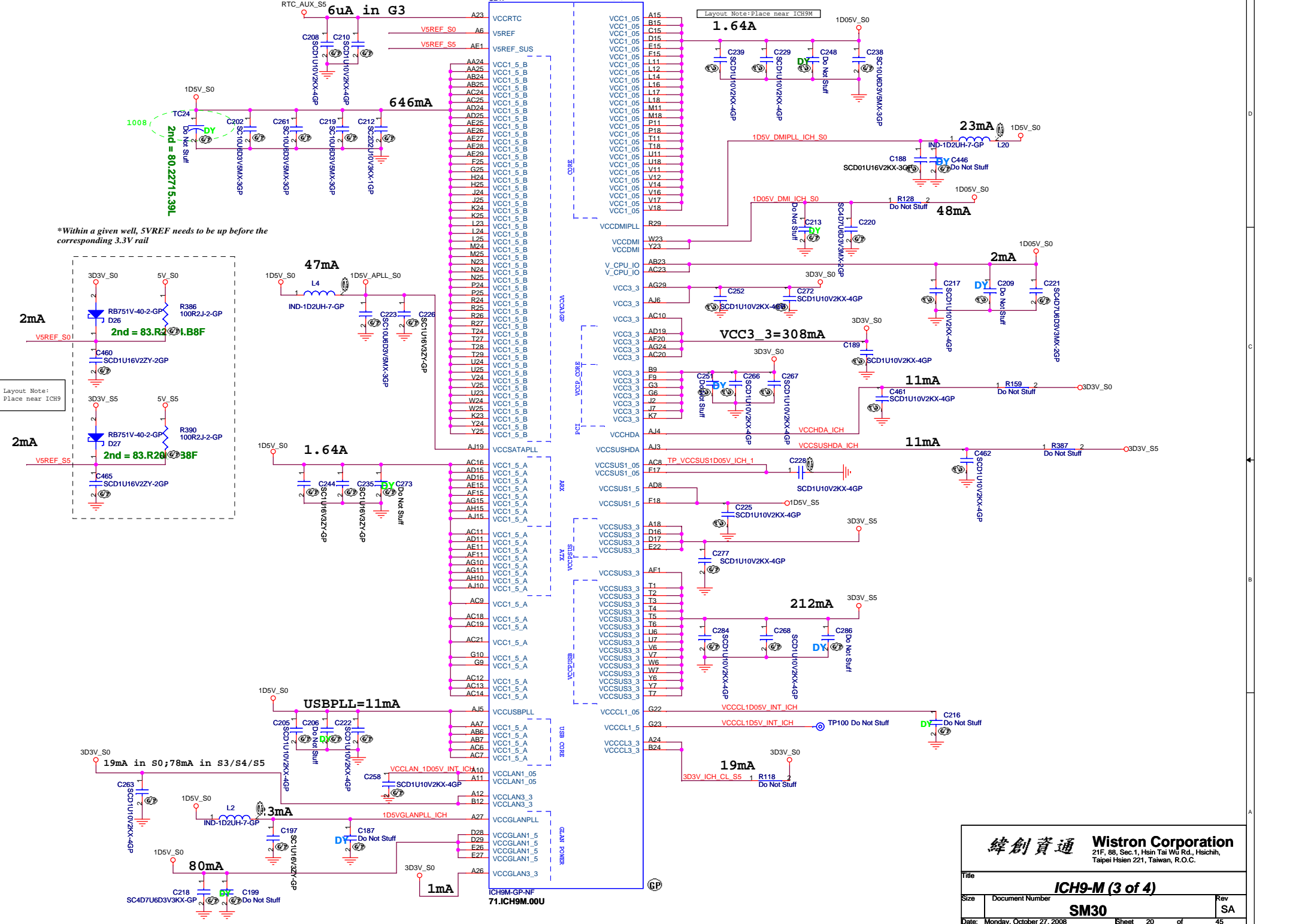
Title: **ICH9-M (1 of 4)**

Size: Document Number **SM30** Rev SA

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\*Within a given well, SVREF needs to be up before the corresponding 3.3V rail



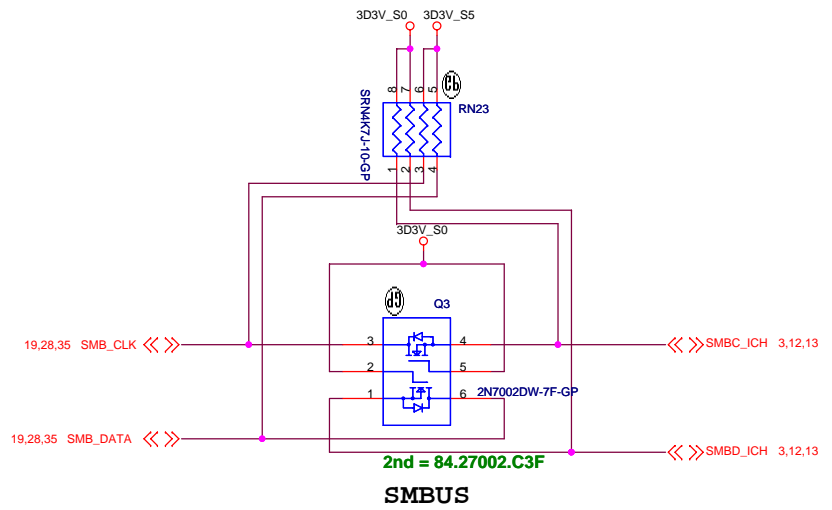
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>ICH9-M (3 of 4)</b>			
Size	Document Number	Sheet	Rev
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SB1E		5 OF 6
AA26	VSS	VSS
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	VSS
AA23	VSS	AC22
AB28	VSS	K28
AB29	VSS	K29
AB4	VSS	L13
AB5	VSS	L15
AC17	VSS	L2
AC26	VSS	L26
AC27	VSS	L27
AC3	VSS	L5
AD1	VSS	L7
AD10	VSS	M12
AD12	VSS	M13
AD13	VSS	M14
AD14	VSS	M15
AD17	VSS	M16
AD18	VSS	M17
AD21	VSS	M23
AD28	VSS	M28
AD29	VSS	M29
AD4	VSS	N11
AD5	VSS	N12
AD6	VSS	N13
AD7	VSS	N14
AD9	VSS	N15
AE12	VSS	N16
AE13	VSS	N17
AE14	VSS	N18
AE16	VSS	N26
AE17	VSS	N27
AE2	VSS	P12
AE20	VSS	P13
AE24	VSS	P14
AE3	VSS	P15
AE4	VSS	P16
AE6	VSS	P17
AE9	VSS	P2
AF13	VSS	P23
AF16	VSS	P28
AF18	VSS	P29
AF22	VSS	P4
AF26	VSS	P7
AF27	VSS	R11
AF5	VSS	R12
AF7	VSS	R13
AF9	VSS	R14
AG13	VSS	R15
AG16	VSS	R16
AG18	VSS	R17
AG20	VSS	R18
AG23	VSS	R28
AG3	VSS	T12
AG6	VSS	T13
AG9	VSS	T14
AH12	VSS	T15
AH14	VSS	T16
AH17	VSS	T17
AH19	VSS	T23
AH2	VSS	B26
AH22	VSS	U12
AH25	VSS	U13
AH5	VSS	U14
AH8	VSS	U15
AJ12	VSS	U16
AJ14	VSS	U17
AJ17	VSS	AD23
AJ8	VSS	U26
B11	VSS	U27
B14	VSS	V1
B17	VSS	V13
B2	VSS	V15
B20	VSS	V23
B23	VSS	V28
B5	VSS	V29
B8	VSS	V4
C26	VSS	V5
C27	VSS	W26
E11	VSS	W27
E14	VSS	W3
E18	VSS	Y1
E2	VSS	Y28
E21	VSS	Y29
E24	VSS	Y4
E5	VSS	Y5
F8	VSS	AG28
F16	VSS	AH6
F28	VSS	AF2
F29	VSS	B25
G12	VSS	VSS
G14	VSS	VSS
G18	VSS	VSS
G21	VSS	VSS
G24	VSS	VSS
G26	VSS	VSS
G27	VSS	VSS
G8	VSS	VSS
H2	VSS	VSS
H23	VSS	VSS
H28	VSS	VSS
H29	VSS	VSS

NCTF TEST PIN:		
A1	NCTF_VSS#A1	A1
A2	NCTF_VSS#A2	A2
B1	NCTF_VSS#B1	B1
A29	NCTF_VSS#A29	A29
A28	NCTF_VSS#A28	A28
B29	NCTF_VSS#B29	B29
AJ1	NCTF_VSS#AJ1	AJ1
AJ2	NCTF_VSS#AJ2	AJ2
AH1	NCTF_VSS#AH1	AH1
AJ28	NCTF_VSS#AJ28	AJ28
AJ29	NCTF_VSS#AJ29	AJ29
AH29	NCTF_VSS#AH29	AH29

- TP172 Do Not Stuff
- TP169 Do Not Stuff
- TP174 Do Not Stuff
- TP162 Do Not Stuff
- TP163 Do Not Stuff
- TP161 Do Not Stuff
- TP171 Do Not Stuff
- TP168 Do Not Stuff
- TP173 Do Not Stuff
- TP164 Do Not Stuff
- TP159 Do Not Stuff
- TP160 Do Not Stuff

ICH9M-GP-NF  
71.ICH9M.00U

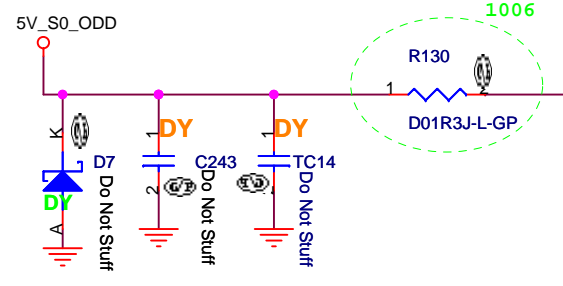
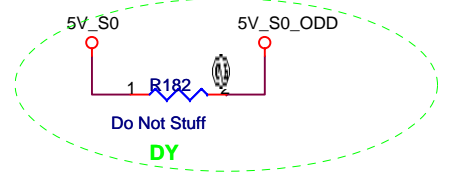
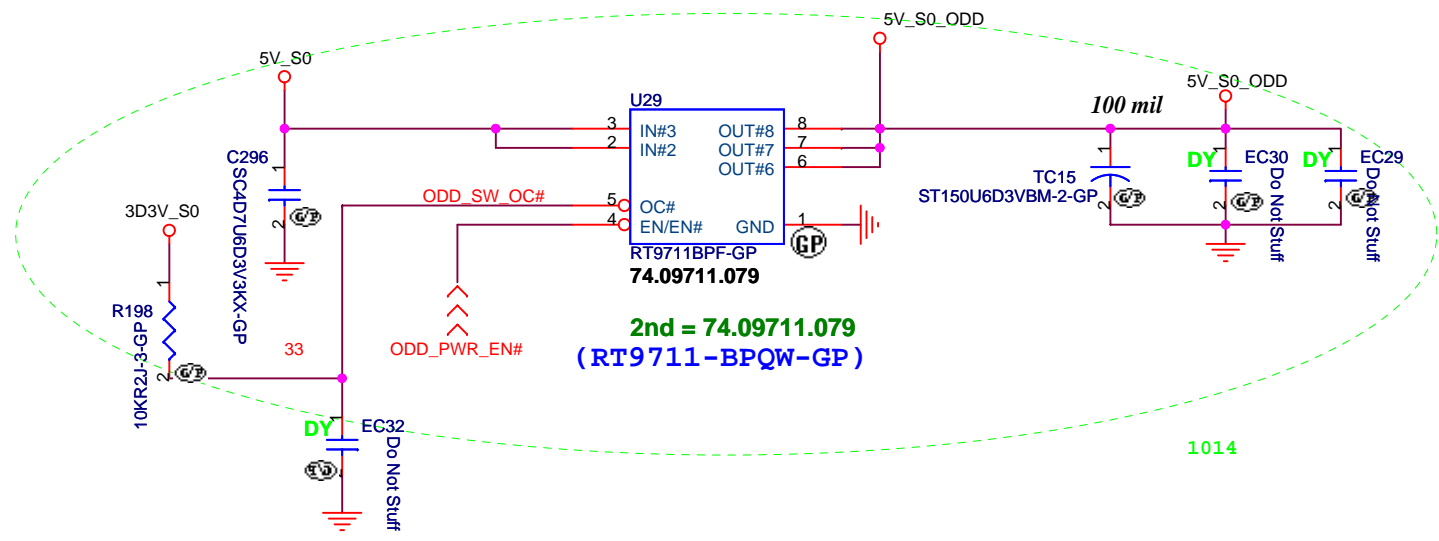


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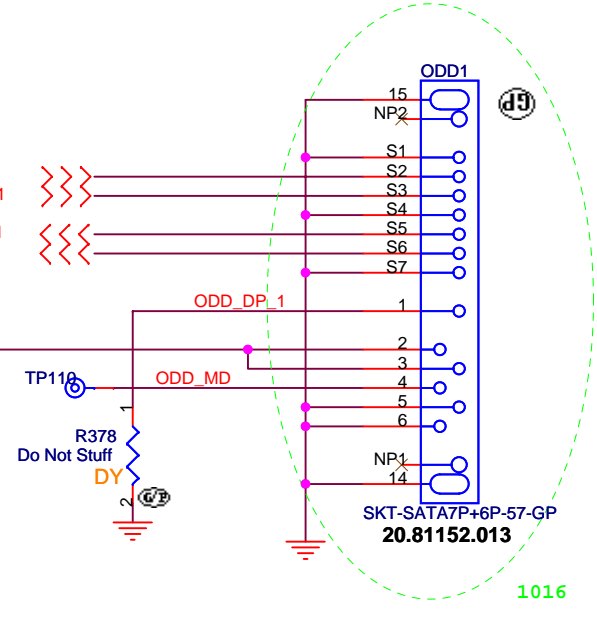
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>ICH9-M (4 of 4)</b>	
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# ODD Connector



18 SATA\_TXP1  
18 SATA\_TXN1  
18 SATA\_RXN1  
18 SATA\_RXP1



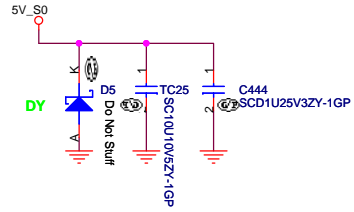
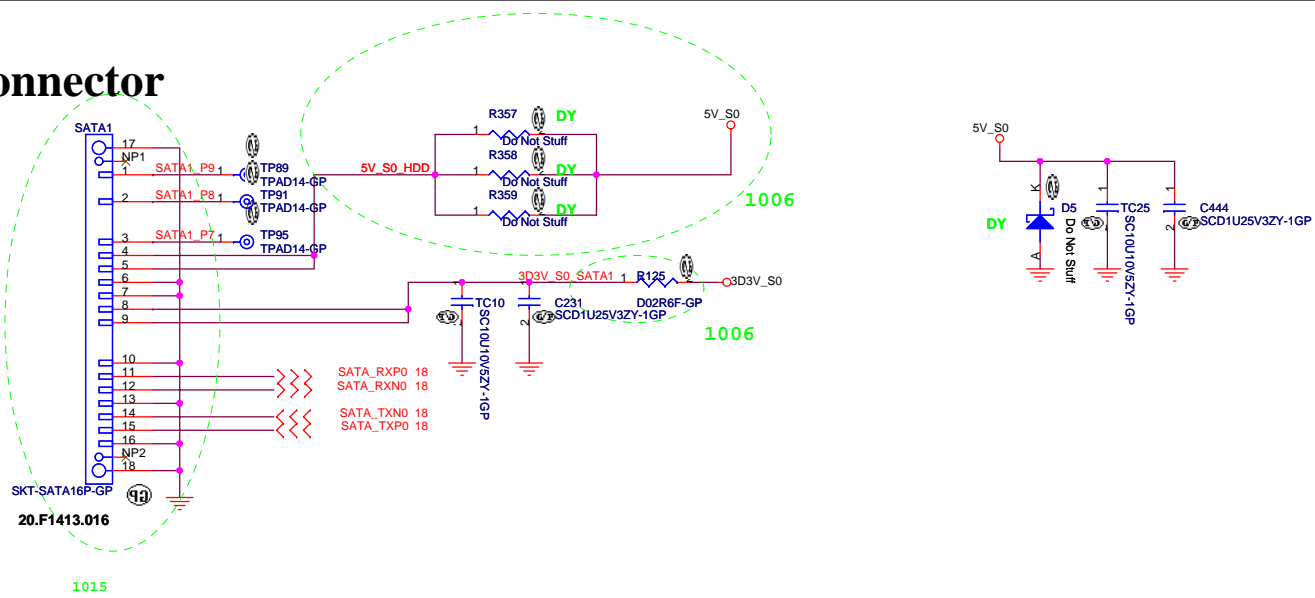
33 ODD\_DP <<< R373 10KR2J-3-GP ODD\_DP\_1 1006

**If Low is ODD  
else is 2nd HDD**

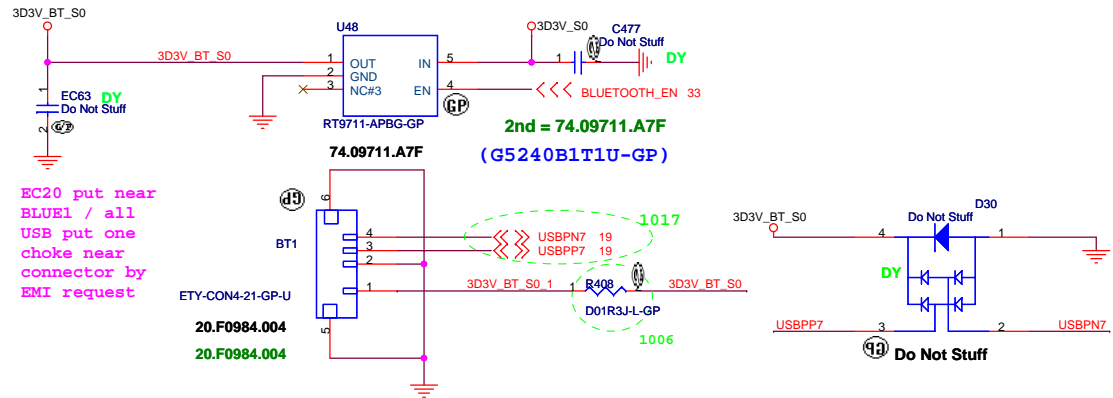
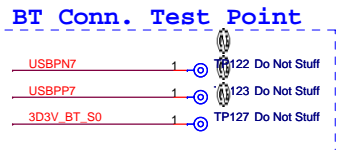
UMA 2nd

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>ODD</b>			
Size	Document Number		Rev
	<b>SM30</b>		SA
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# SATA Connector



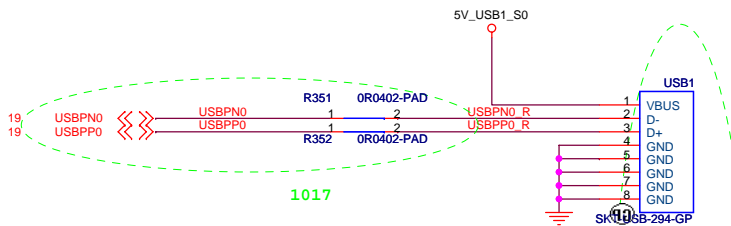
# BLUETOOTH MODULE



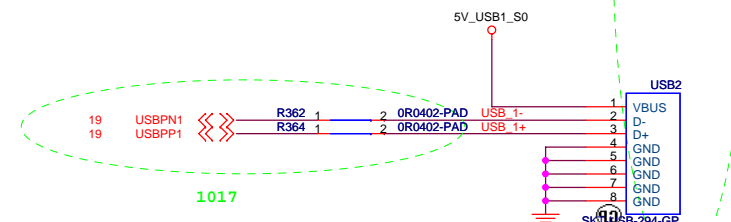
EC20 put near BLUE1 / all USB put one choke near connector by EMI request

**Need check conn.**

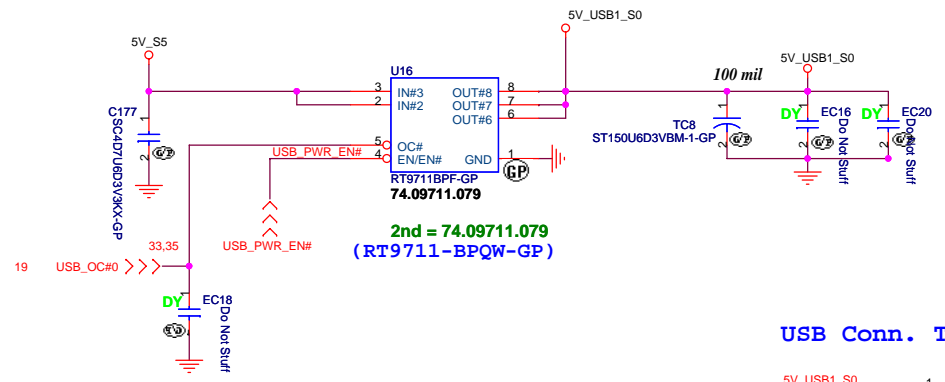




22.10321.211



22.10321.211

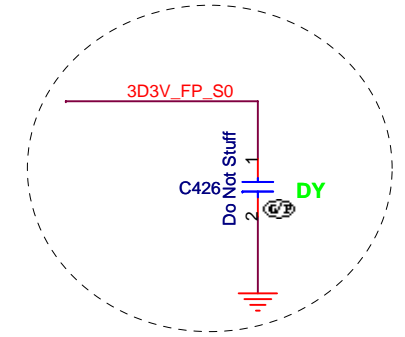
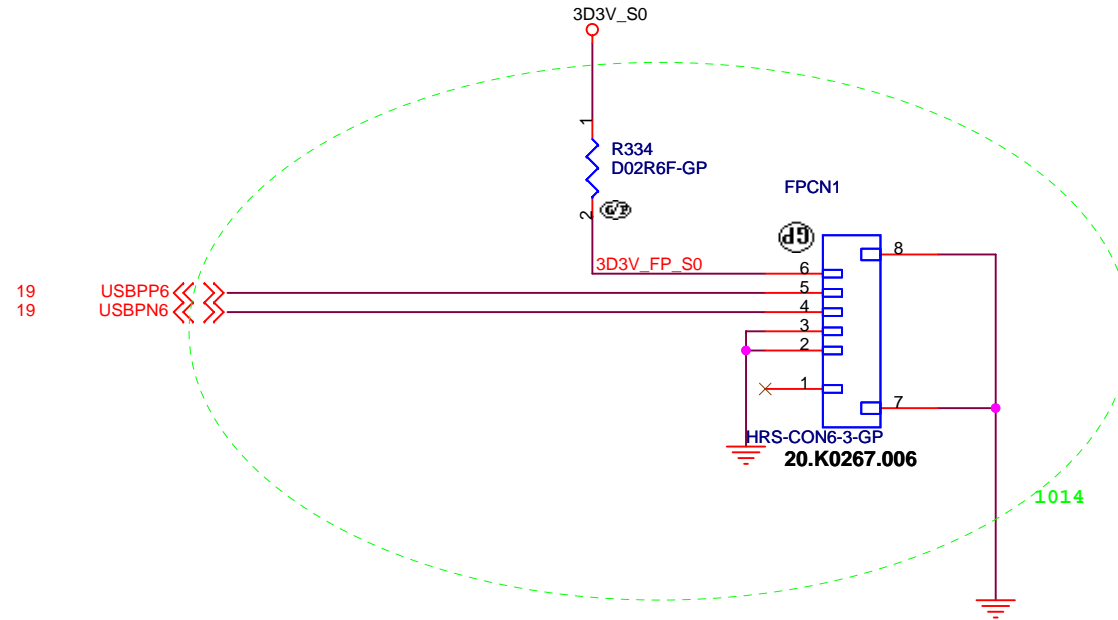
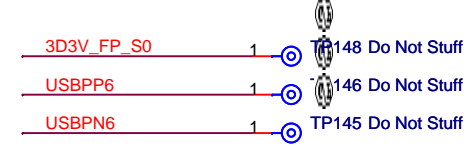


**USB Conn. Test Point**

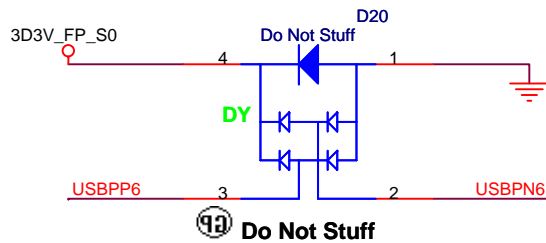
5V_USB1_S0	1	37	Do Not Stuff
USBPN0_R	1	34	Do Not Stuff
USBPP0_R	1	35	Do Not Stuff
USB 1-	1	99	Do Not Stuff
USB 1+	1	TP103	Do Not Stuff

# Finger printer

## FP Conn. Test Point



For EMI



UMA 2nd

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Finger Printer**

Size

Document Number

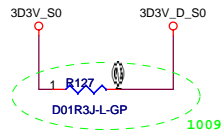
**SM30**

Rev

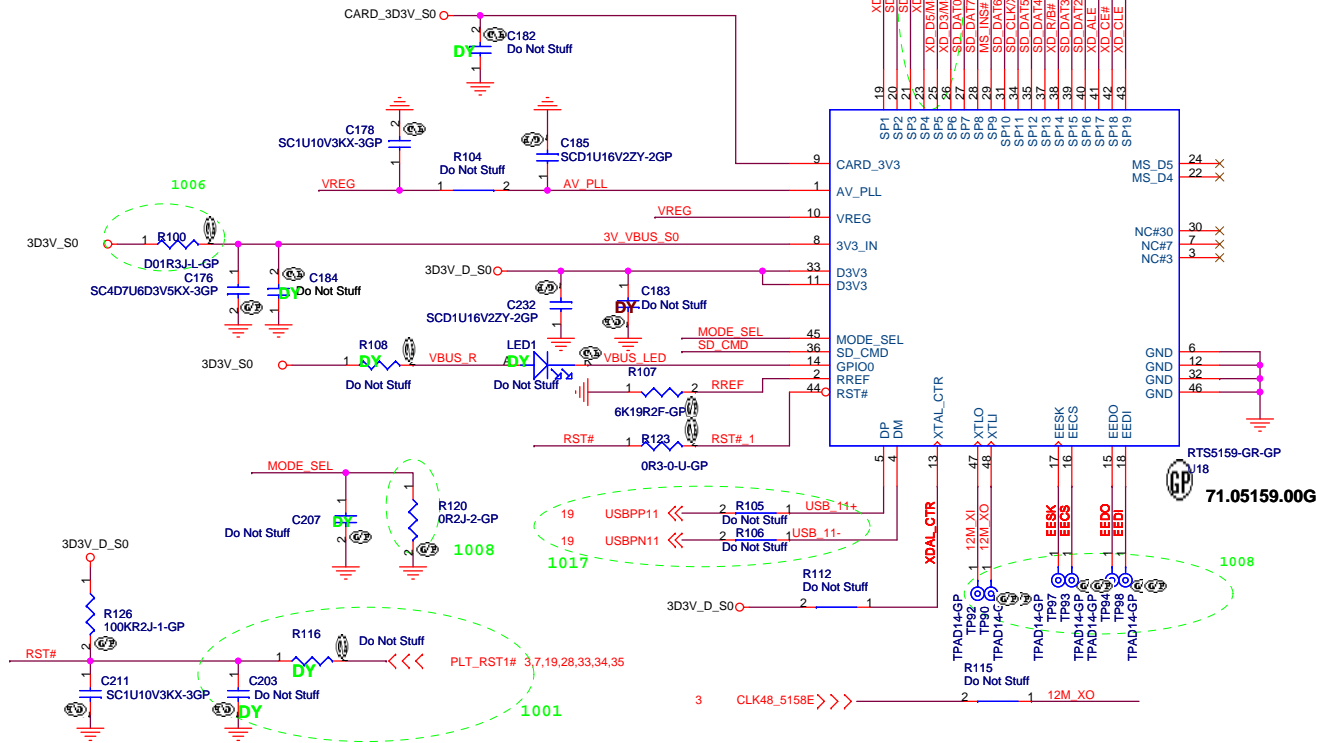
**SA**

Date: Saturday, October 18, 2008

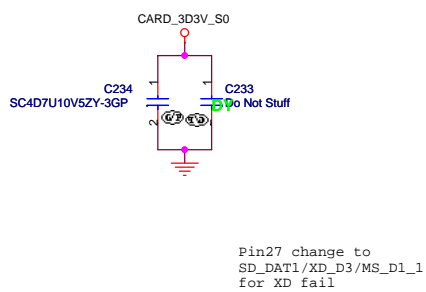
Sheet 26 of 45



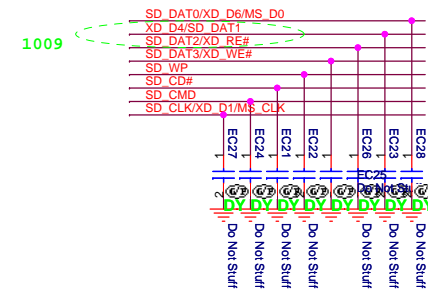
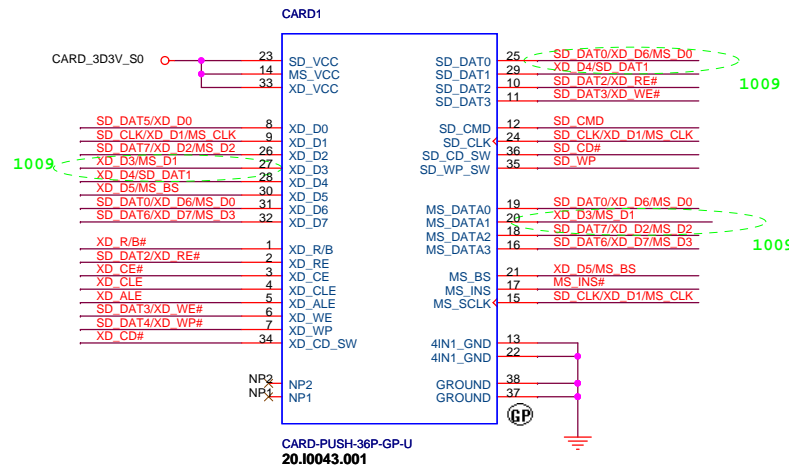
C726 close to U70  
3V\_BUS\_S0 & 3D3V\_D\_S0 need to 20 mil



### 5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin27 change to  
SD\_DAT1/XD\_D3/MS\_D1\_1  
for XD fail

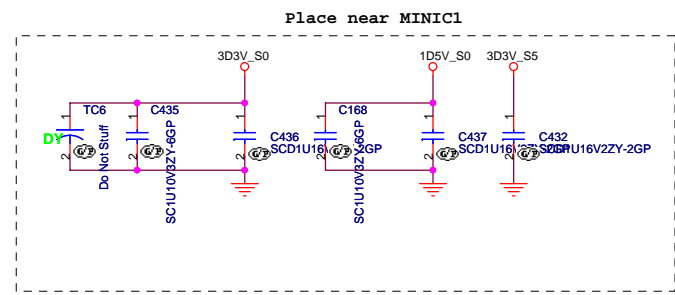
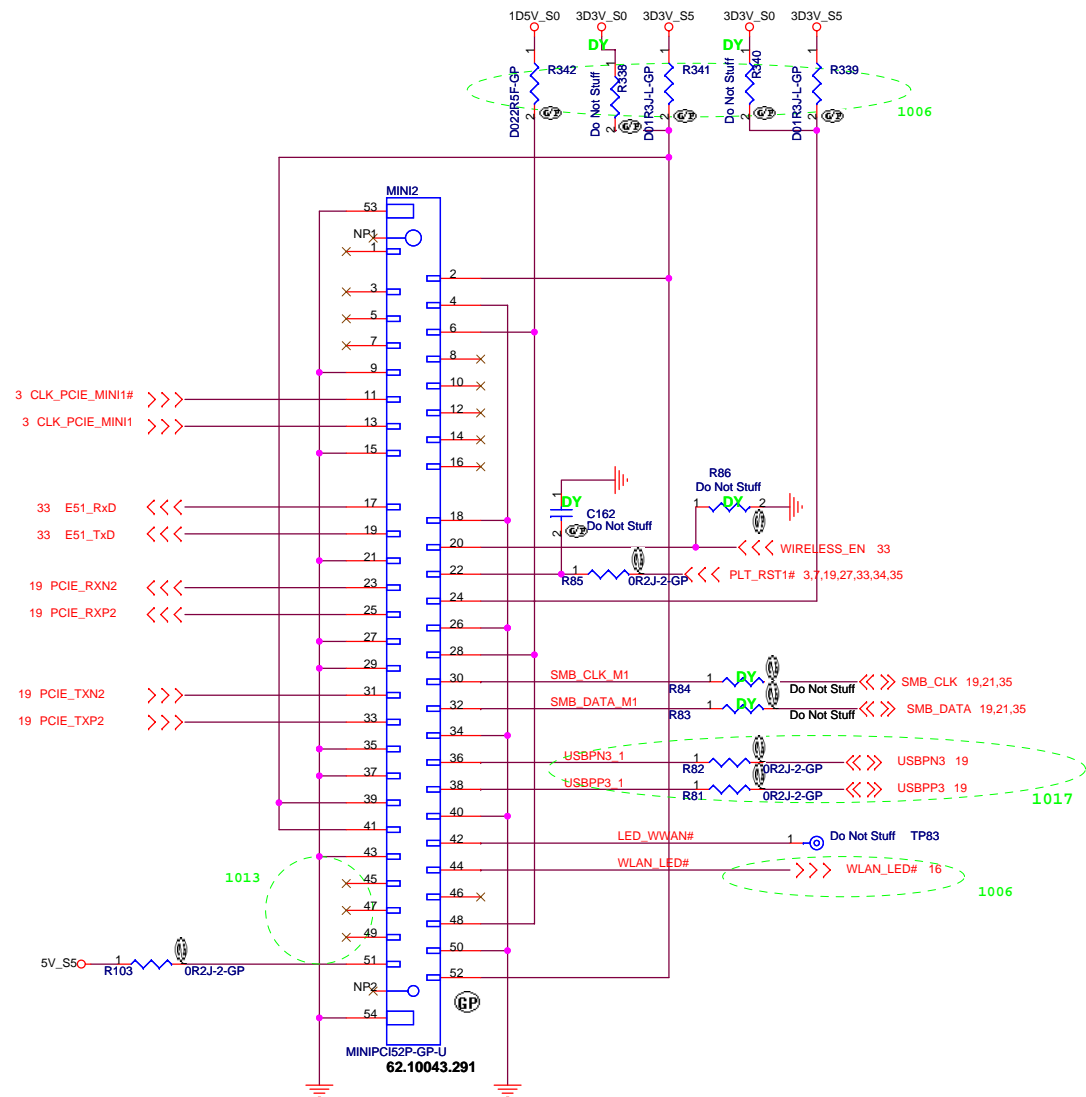


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

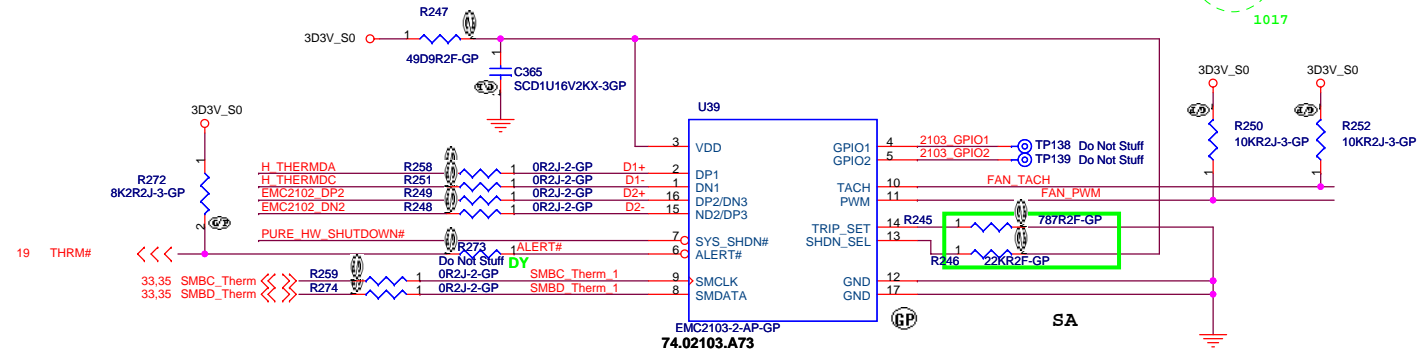
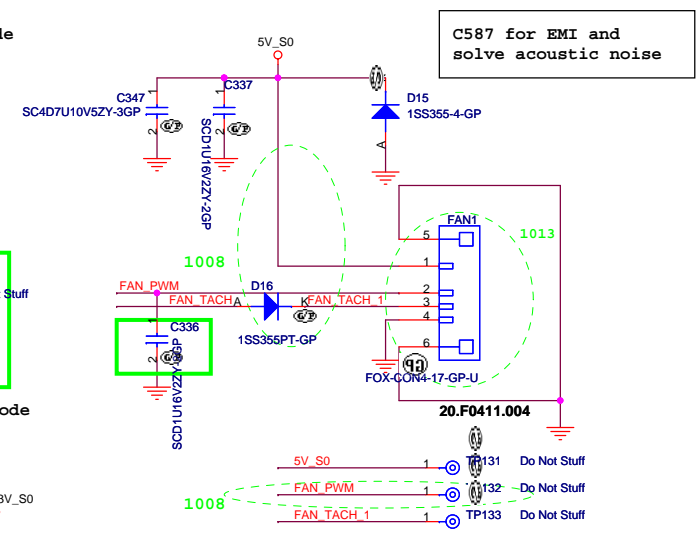
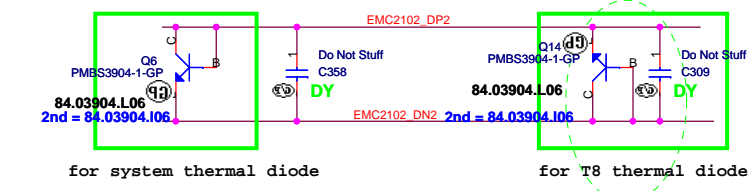
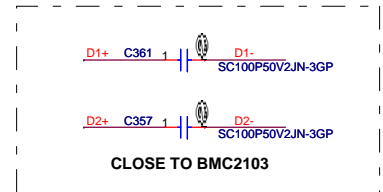
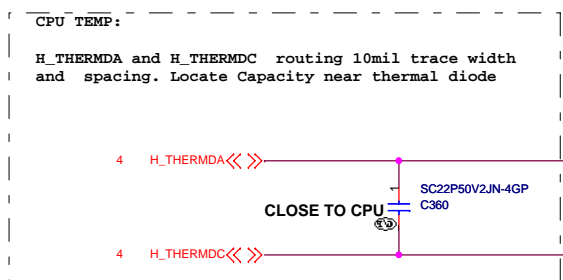
Title: **CARDREADER- RTS5158E**  
 Size: Document Number: **SM30** Rev: **SA**  
 Date: Saturday, October 18, 2008 Sheet 27 of 45

# Mini Card Connector(WLAN)



UMA 2nd

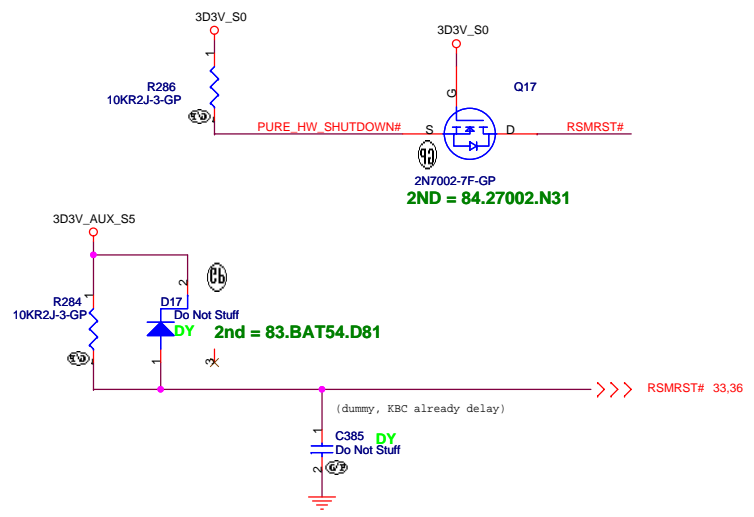
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MINI CARD</b>	
Title Size A3	Document Number <b>SM30</b>
Date: Saturday, October 18, 2008	Rev <b>SA</b>
Sheet 28 of 45	



ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL

SHDN SEL	
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET	
Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100



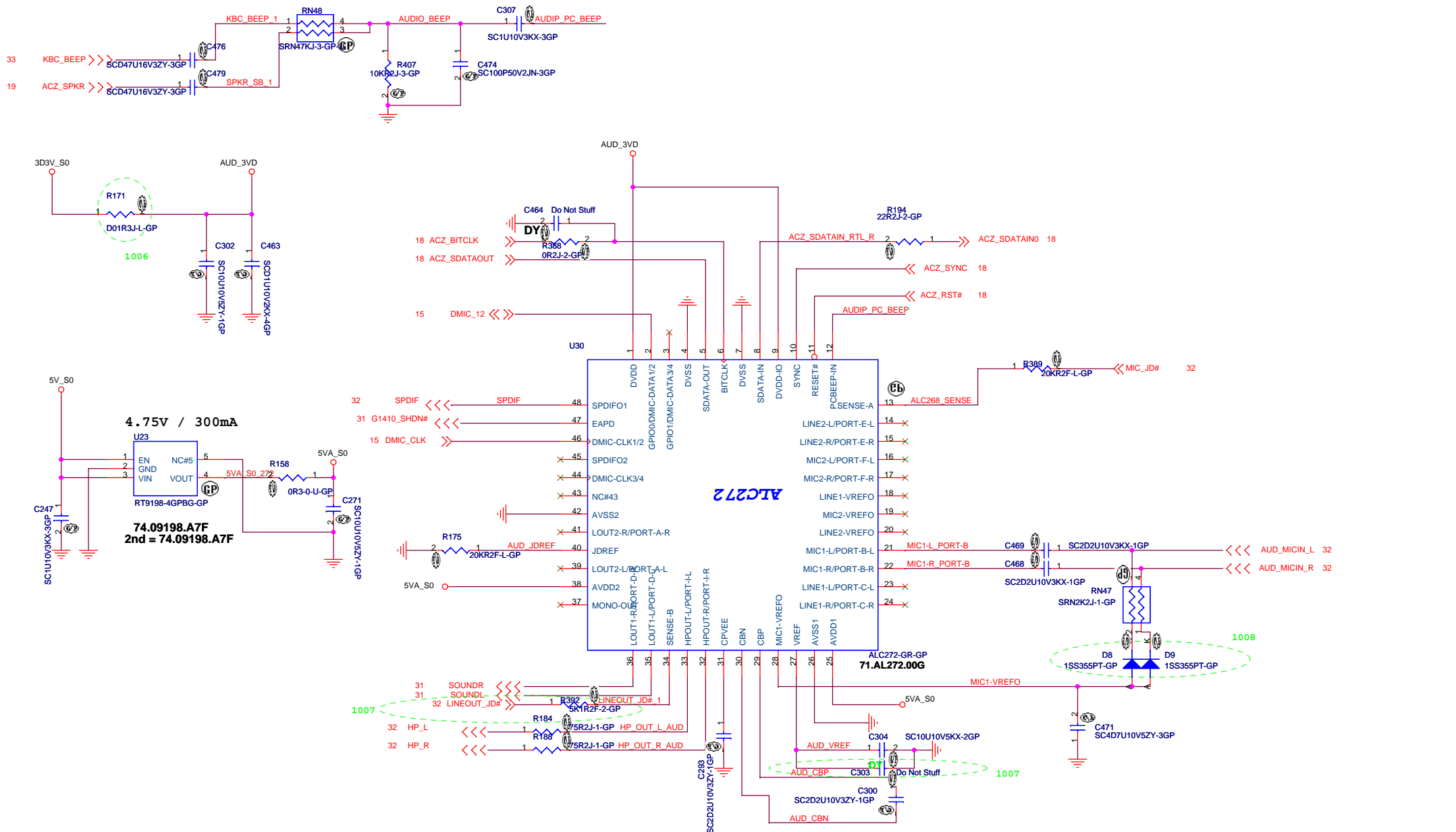
UMA 2nd

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controller**

Size: Document Number **SM30** Rev SA

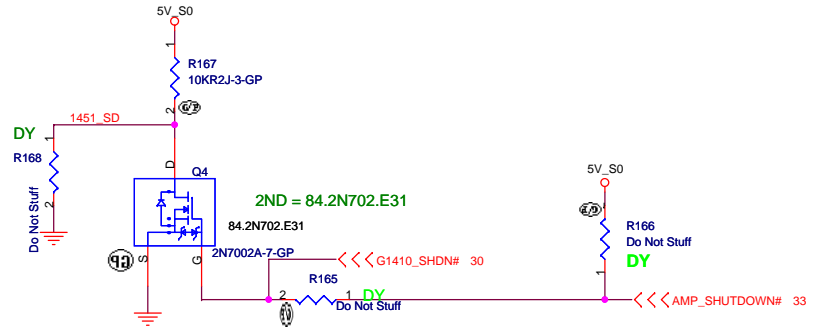
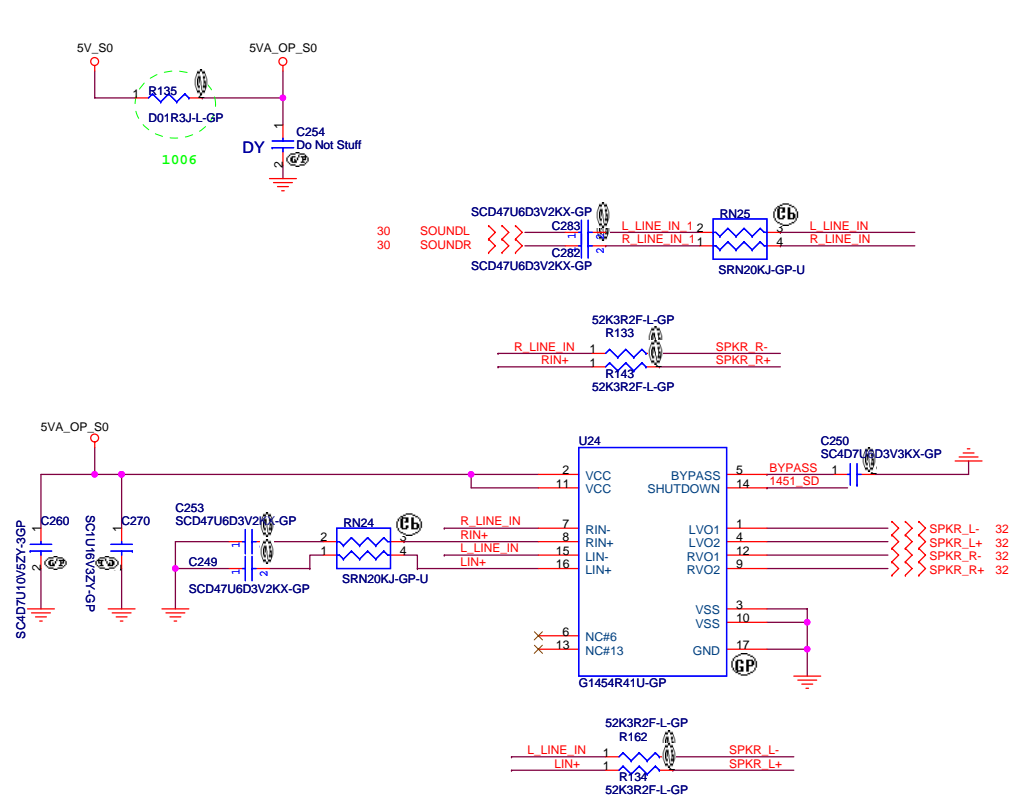
Date: Saturday, October 18, 2008 Sheet 29 of 45



UMA 2nd

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <span style="float: right;">Azalia codec ALC268</span>			
Size	Document Number	Rev	
A3	SM30	SA	
Date: Saturday, October 18, 2008		Sheet	45

# AUDIO OP AMPLIFIER

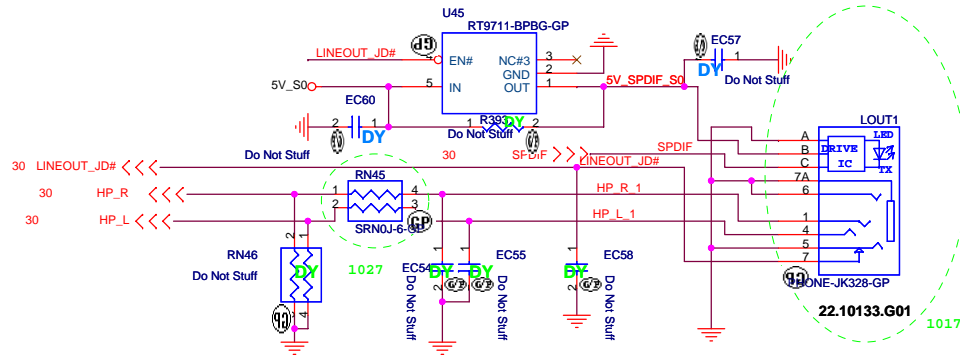


UMA 2nd

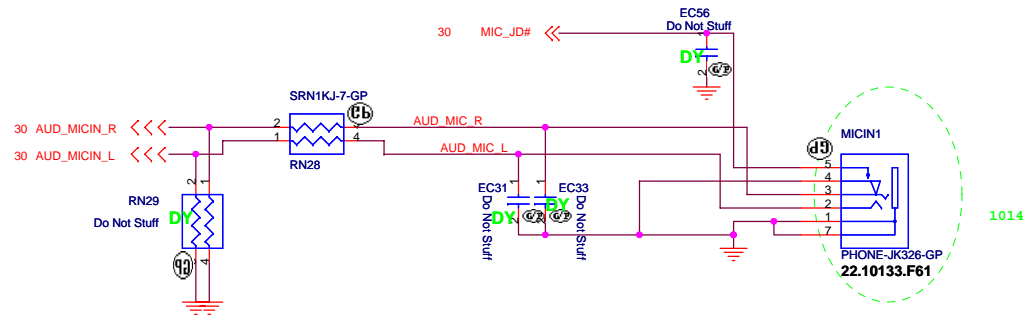
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
AUDIO AMP			SA
Size	Document Number	SM30	
Date:	Saturday, October 18, 2008	Sheet	31 of 45

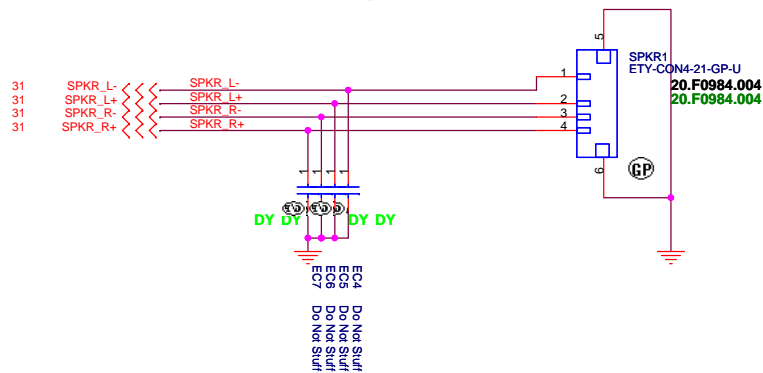
# LINE OUT



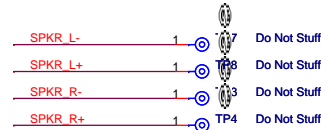
# MIC IN



# Internal Speaker



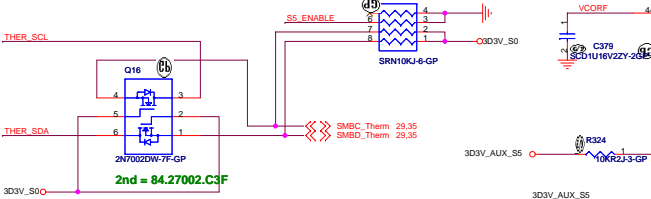
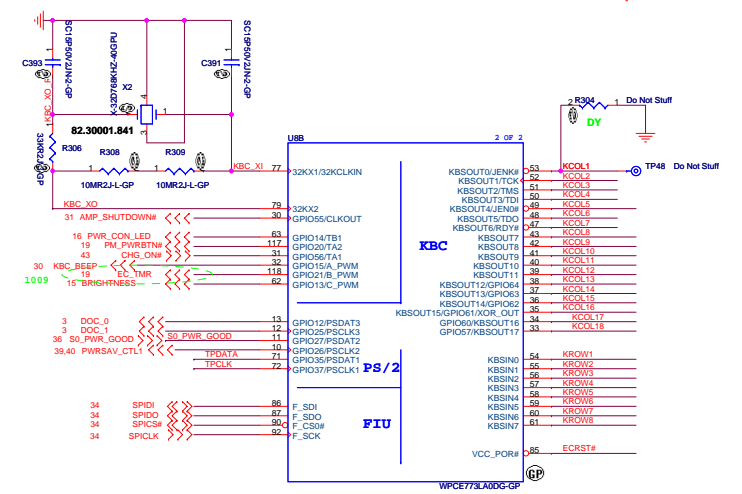
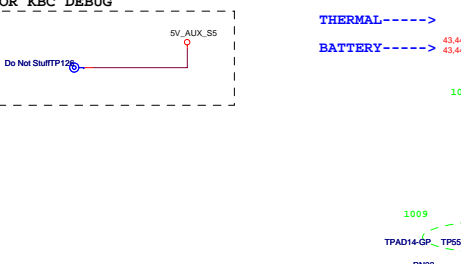
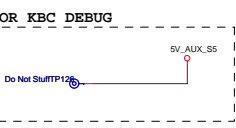
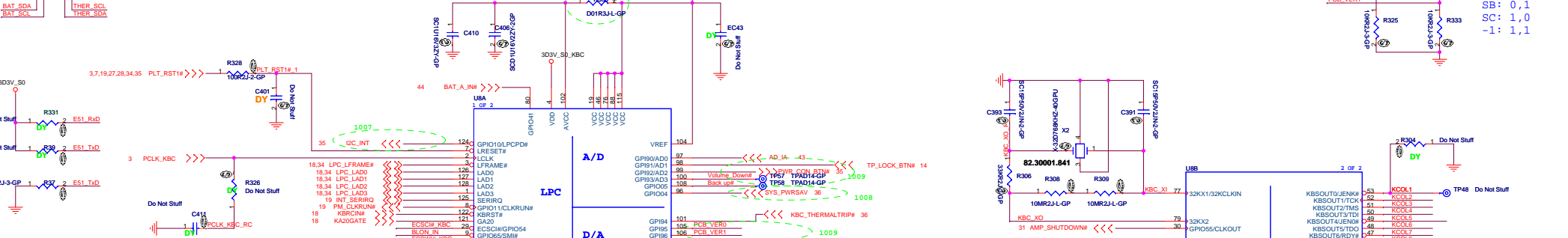
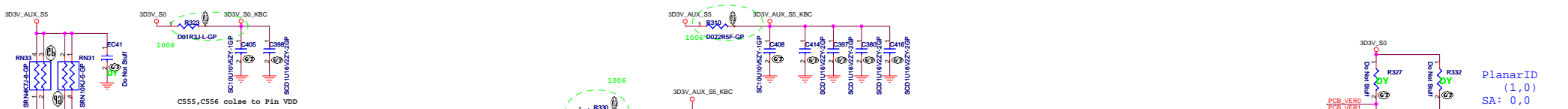
## SPKR1 Conn. Test Point



UMA 2nd

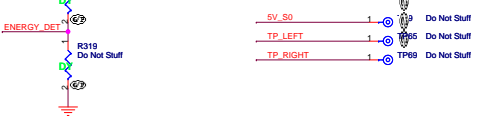
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<h2>AUDIO JACK</h2>			
Size	Document Number	Rev	
	SM30	SA	
Date:	Monday, October 27, 2008	Sheet	32 of 45



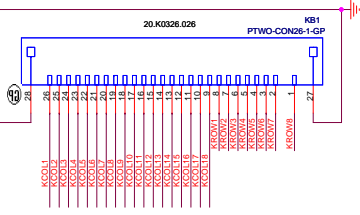
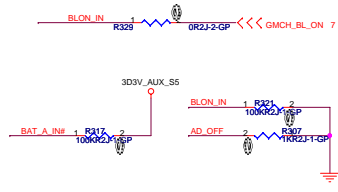


**Internal Keyboard Connector**

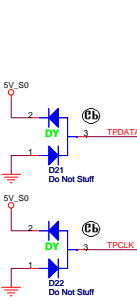
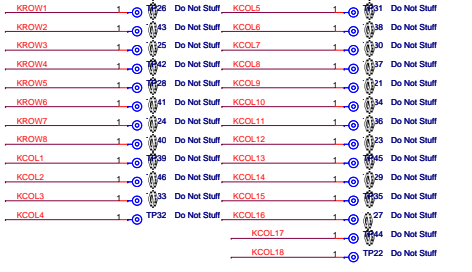
**TPOINTCN1 Conn. Test Point**



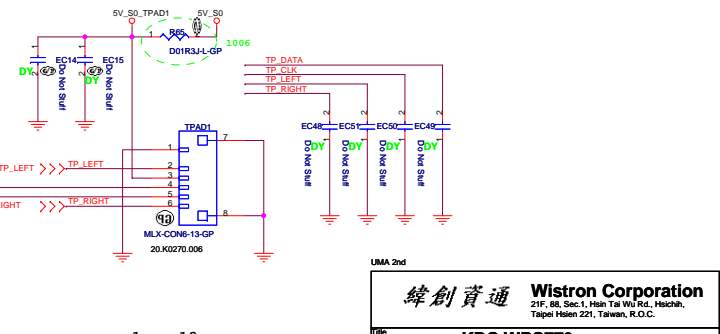
**TOUCH PAD**



**KB1 CN Test Point**



**TOUCH PAD Conn Test Point**



MB PIN DEFINE: 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
 KB PIN DEFINE: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24



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UMA 2nd

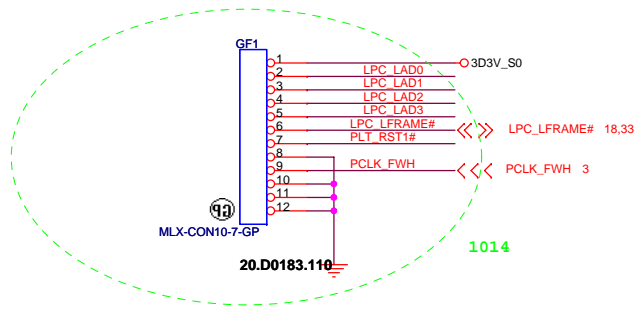
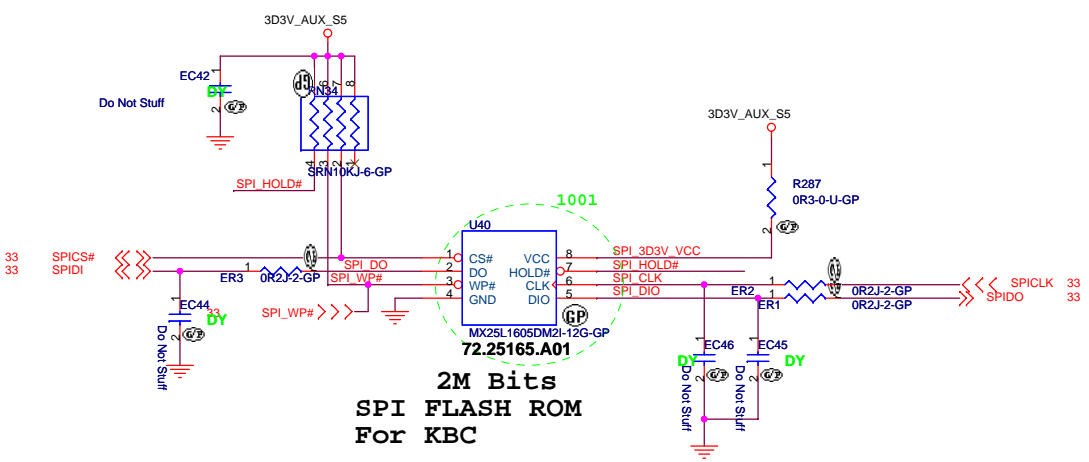
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC WPC773**

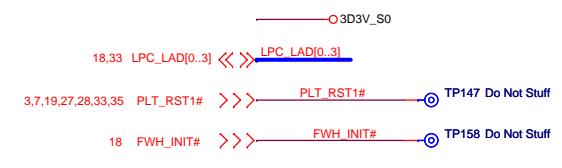
Size: Document Number: **SM30** Rev: SA

Date: Saturday, October 18, 2008 Sheet: 33 of 45

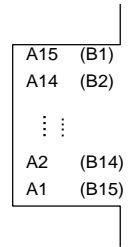




**GOLDEN FINGER FOR DEBUG BOARD**



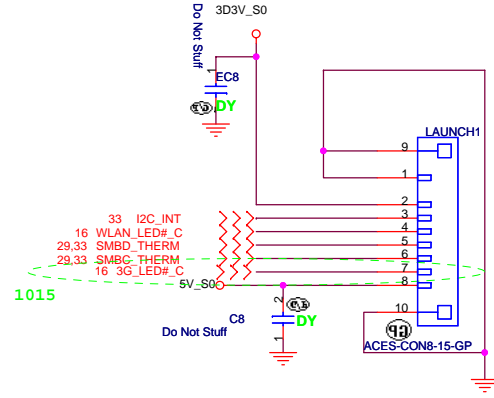
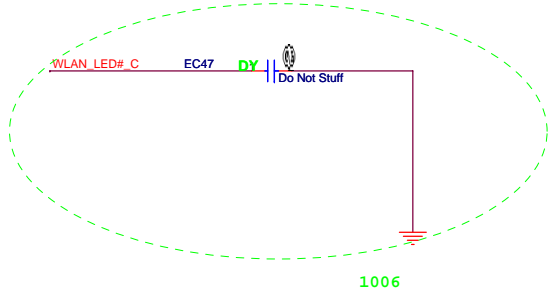
**TOP VIEW**



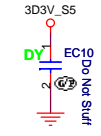
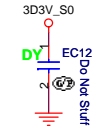
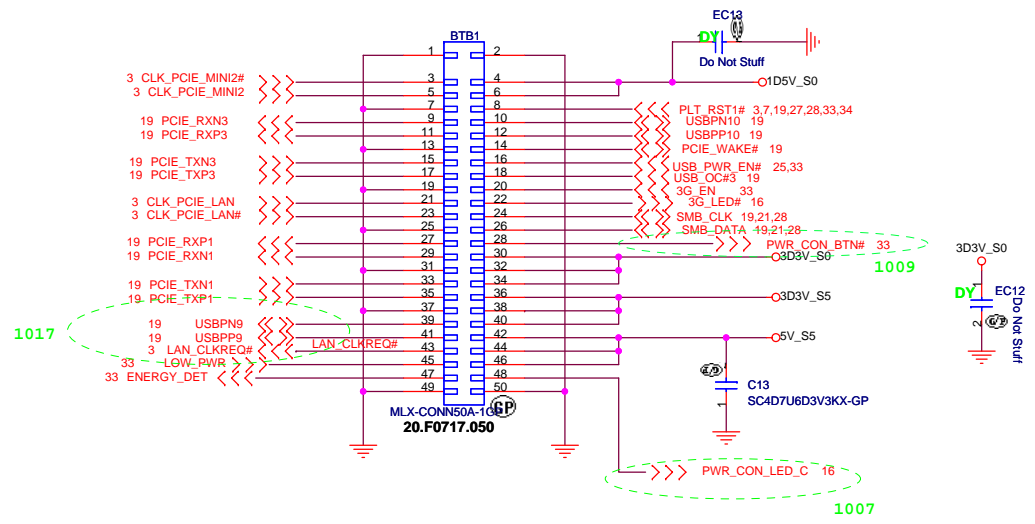
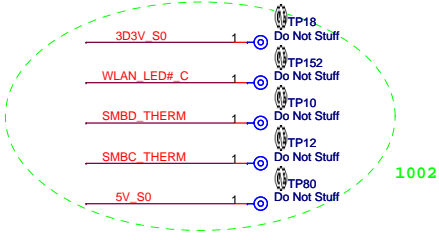
**(BOTTOM VIEW)**

UMA 2nd

<b>緯創資通 Wistron Corporation</b>		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
<b>BIOS &amp; TPM</b>			
Size	Document Number	Rev	SA
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Date: Saturday, October 18, 2008		Sheet 34	of 45



**LAUNCH Test Point**



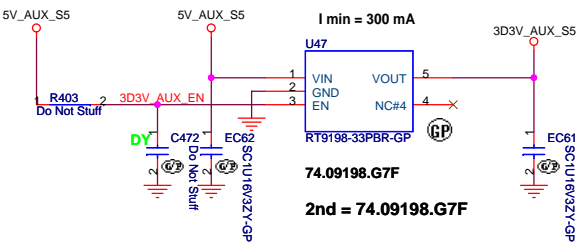
UMA 2nd

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

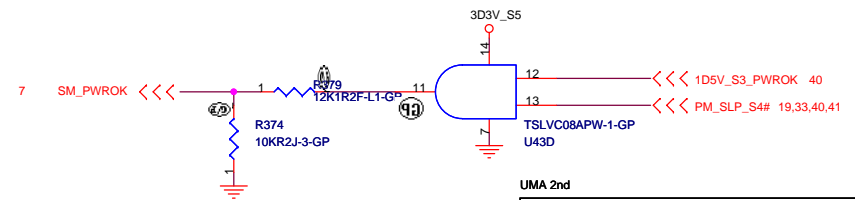
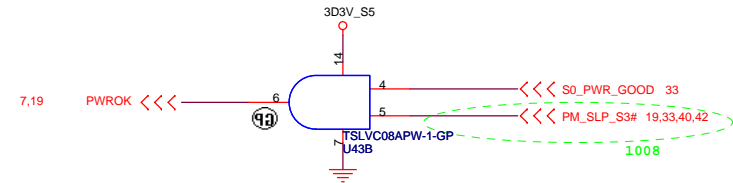
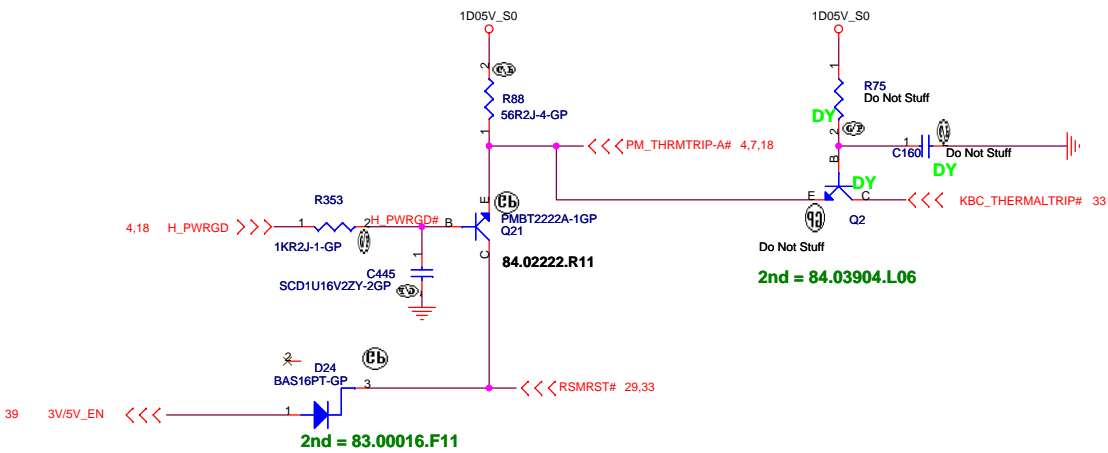
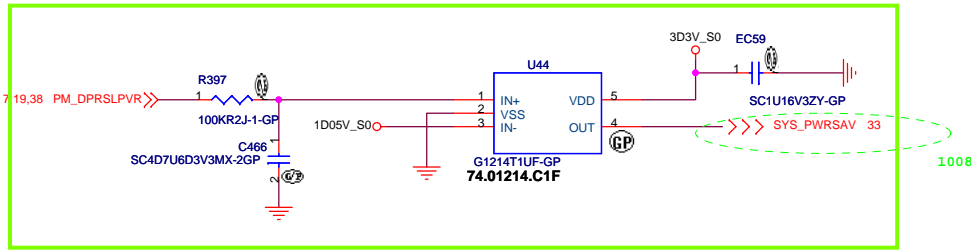
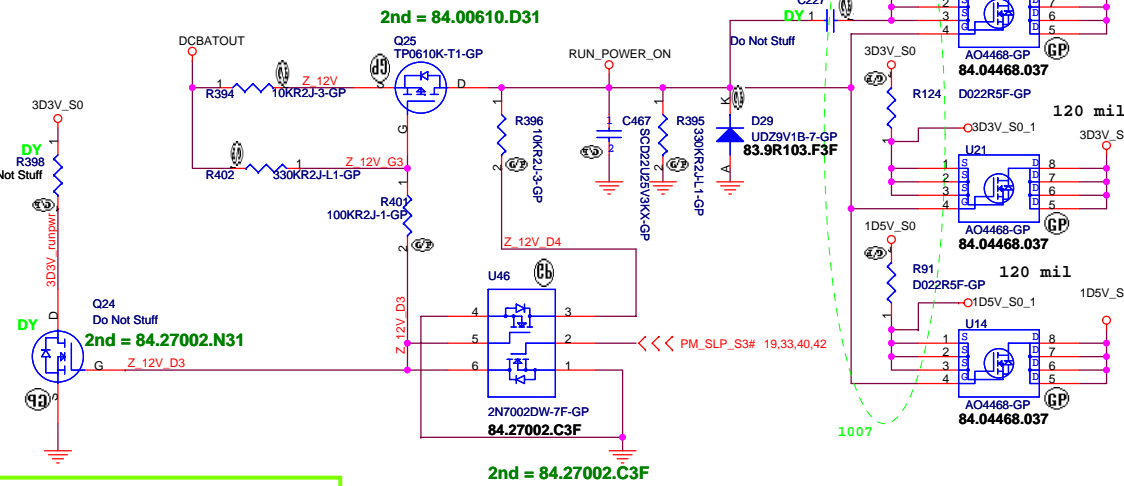
Title <b>LAUNCH</b>		
Size	Document Number <b>SM30</b>	Rev SA
Date: Saturday, October 18, 2008	Sheet 35 of	45

# Aux Power

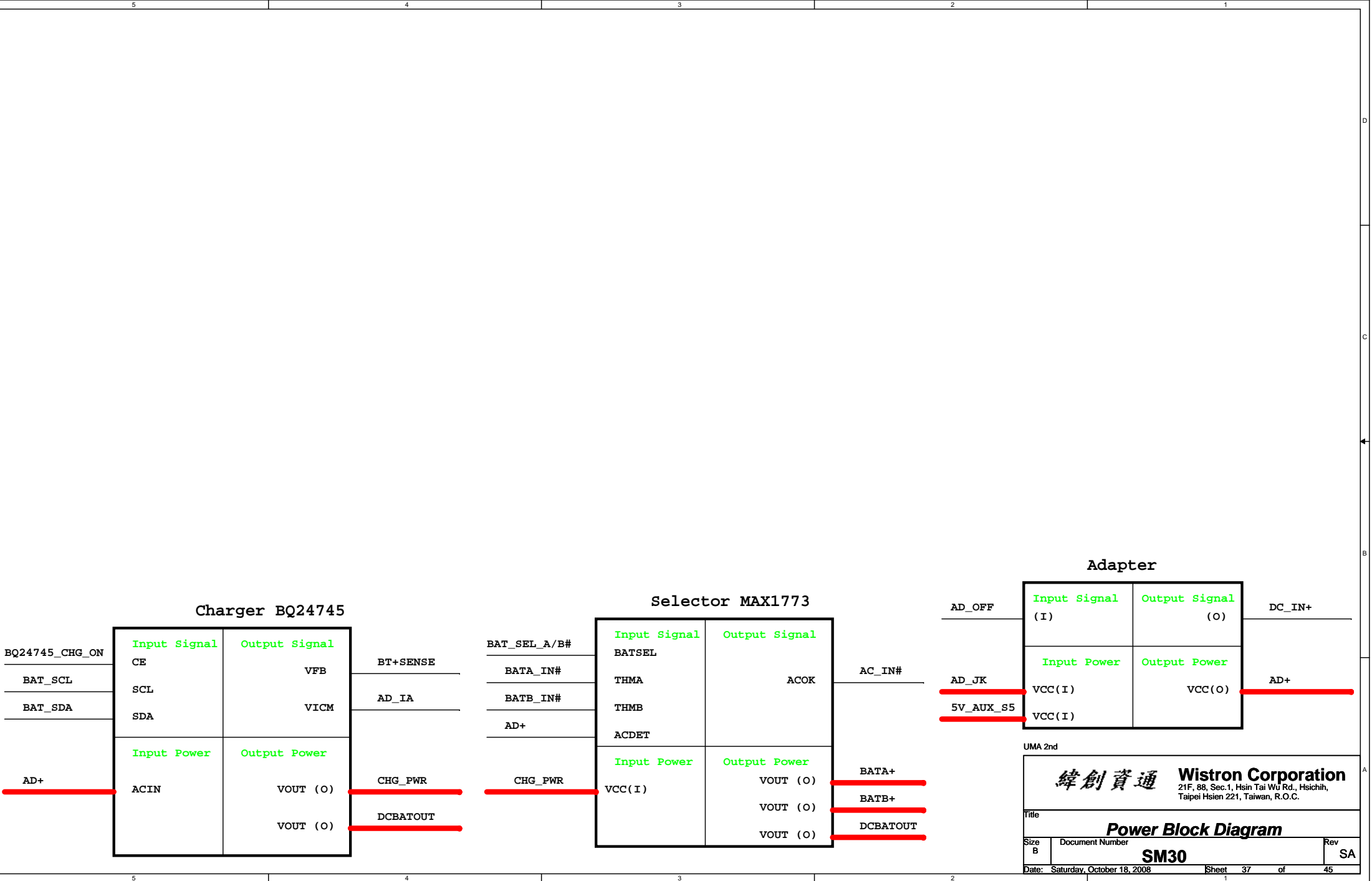
3D3V\_AUX\_S5



# Run Power



UMA 2nd



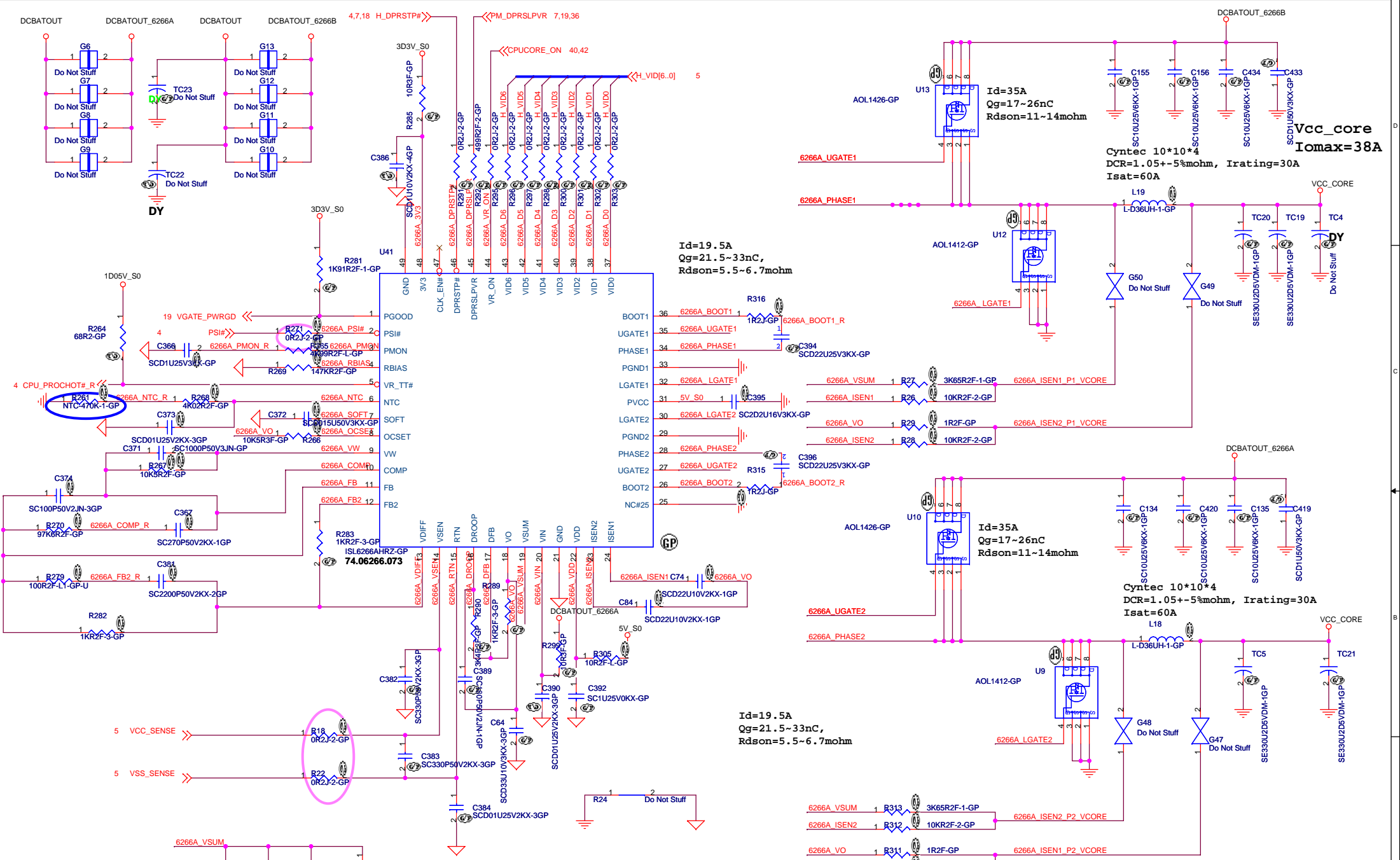
UMA 2nd

**緯創資通 Wistron Corporation**  
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size B	Document Number	Rev
	<b>SM30</b>	SA

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**Vcc\_core**  
**Iomax=38A**  
 Cyntec 10\*10\*4  
 DCR=1.05+-5%moHM, Irating=30A  
 Isat=60A

**Id=19.5A**  
**Qg=21.5~33nC,**  
**Rdson=5.5~6.7mohm**

**Id=35A**  
**Qg=17~26nC**  
**Rdson=11~14mohm**

**Id=19.5A**  
**Qg=21.5~33nC,**  
**Rdson=5.5~6.7mohm**

**Id=35A**  
**Qg=17~26nC**  
**Rdson=11~14mohm**

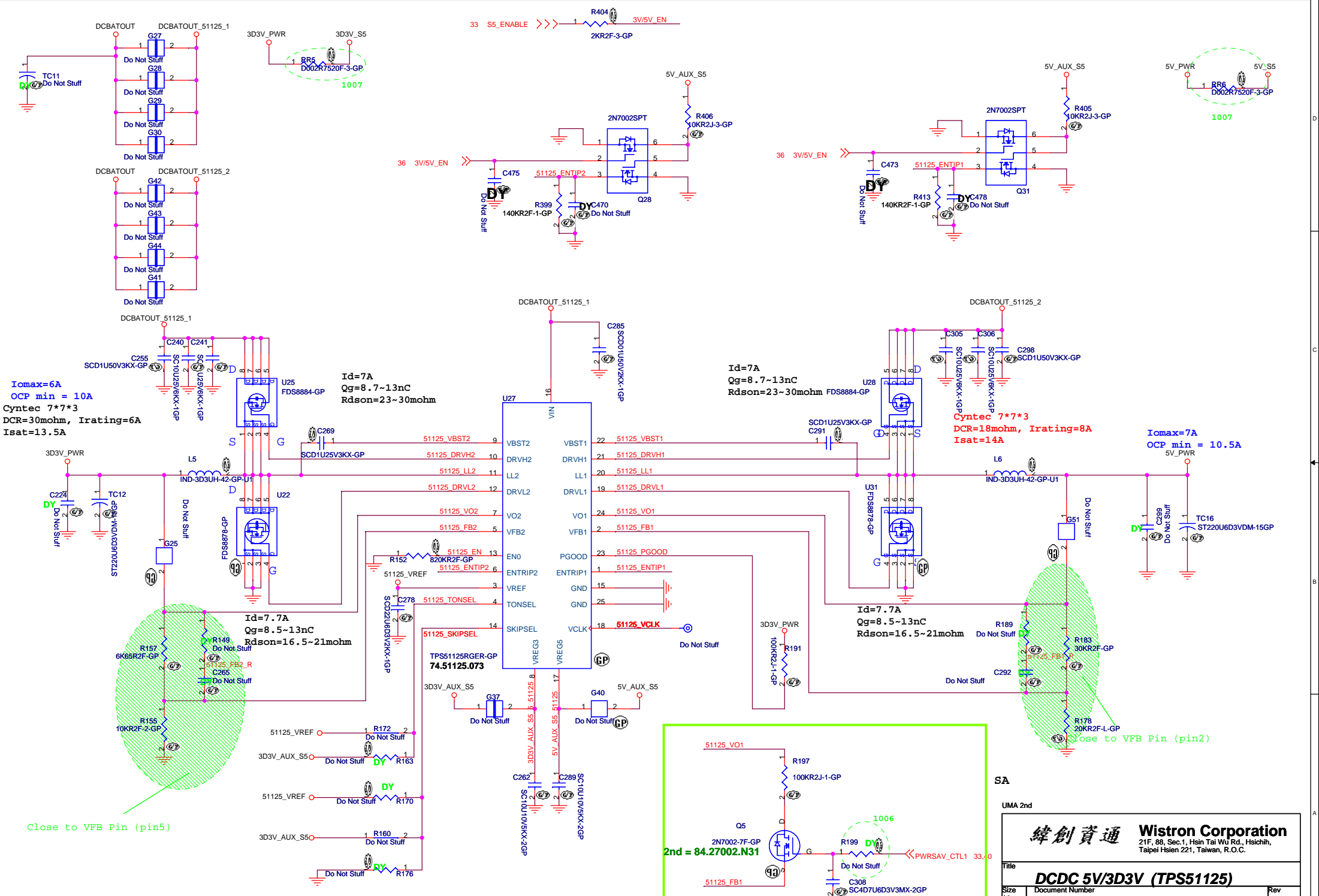
UMA 2nd

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6266A CPU CORE**

Size A3	Document Number	Rev
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**I<sub>omax</sub>=6A**  
**OCP min = 10A**  
**Cyntec 7\*7\*3**  
**DCR=30mohm, Irating=6A**  
**Isat=13.5A**

**I<sub>d</sub>=7A**  
**Q<sub>g</sub>=8.7~13nC**  
**R<sub>dson</sub>=23~30mohm**

**I<sub>d</sub>=7A**  
**Q<sub>g</sub>=8.7~13nC**  
**R<sub>dson</sub>=23~30mohm**

**Cyntec 7\*7\*3**  
**DCR=18mohm, Irating=8A**  
**Isat=14A**

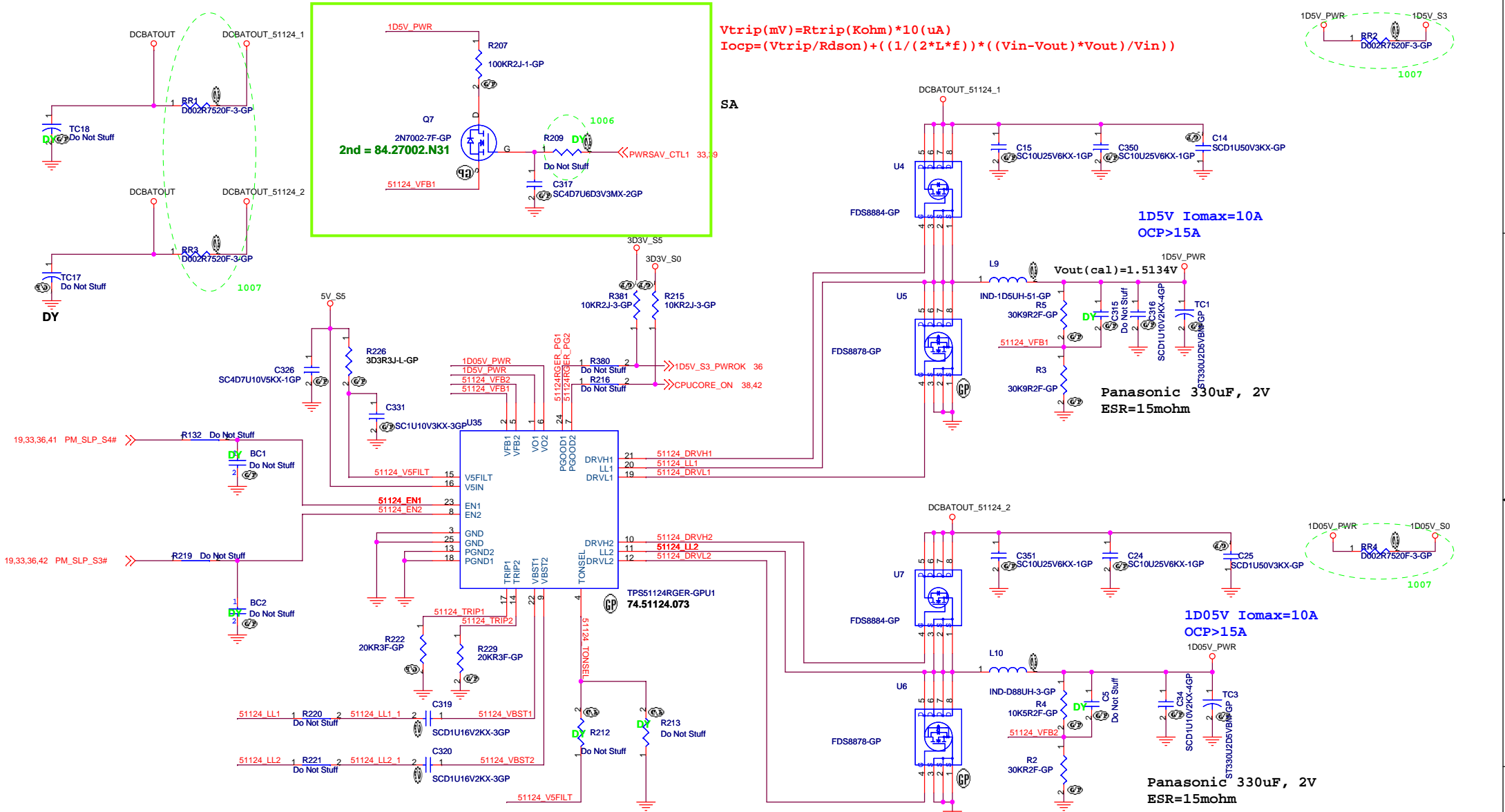
**I<sub>omax</sub>=7A**  
**OCP min = 10.5A**  
**5V\_PWR**

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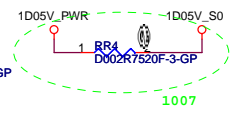
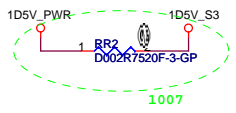
緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

**DCDC 5V/3D3V (TPS51125)**

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$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$   
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$



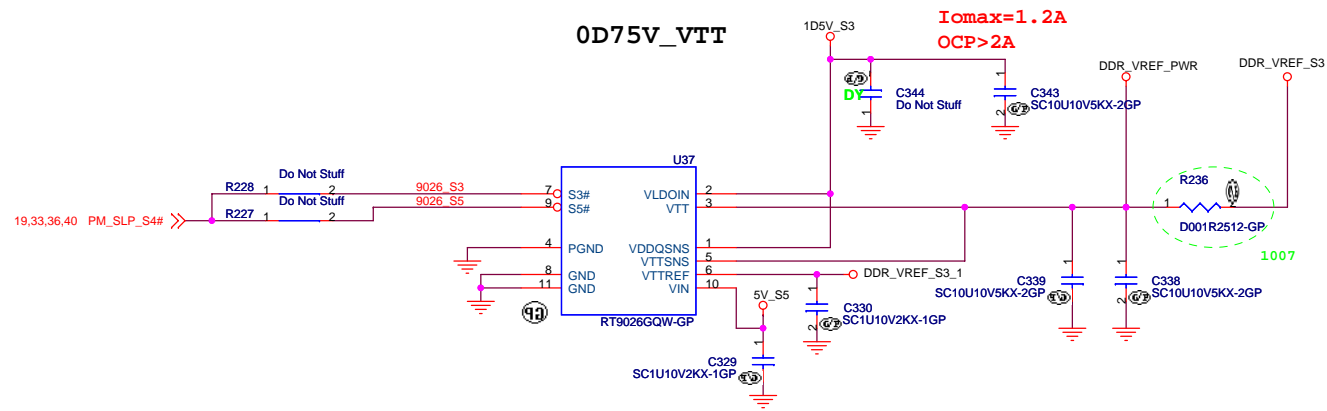
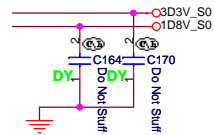
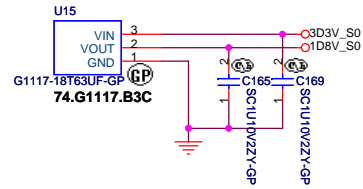
	GND	OPEN	V5FILT
<b>TONSEL</b>	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2) / R2$  --> PWM mode  
 $V_{out} = 0.764V * (R1+R2) / R2$  --> Skip Mode

UMA 2nd

<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>TPS51124 1D5V 1D05V</b>	
Title	
Size A3	Document Number
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<b>SM30</b>	Rev SA

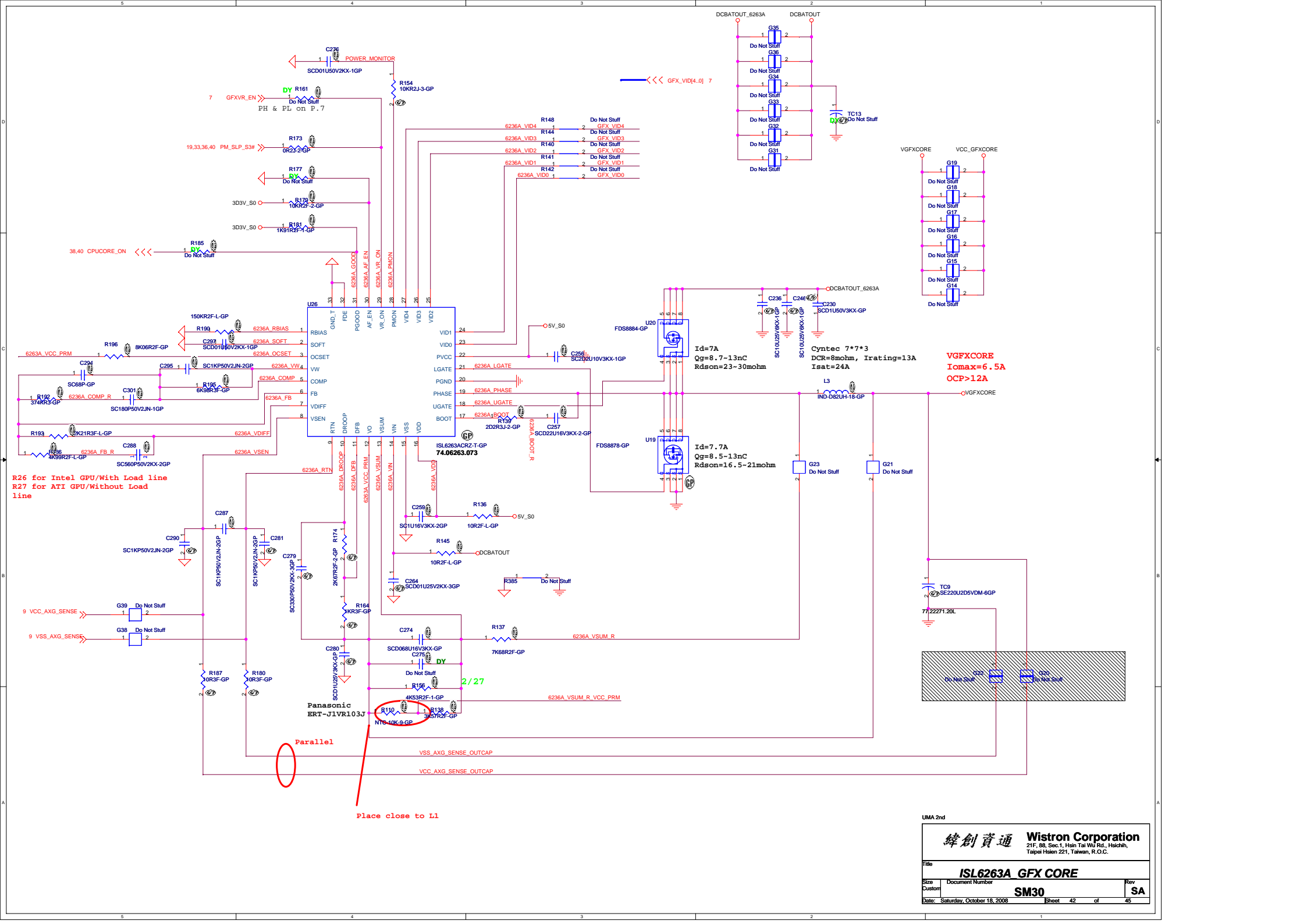




UMA 2nd

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>0D75V &amp; 1D8V</b>		
Size	Document Number	Rev			SA
A3		<b>SM30</b>			
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7 GFXVR\_EN <<< PH & PL on P. 7

19.33.36.40 PM\_SLP\_S3#

3D3V\_S0

38.40 CPUCORE\_ON <<<

6263A VCC\_PRM

6263A COMP\_R

6263A FB\_R

R26 for Intel GPU/With Load line  
R27 for ATI GPU/Without Load line

9 VCC\_AXG\_SENSE

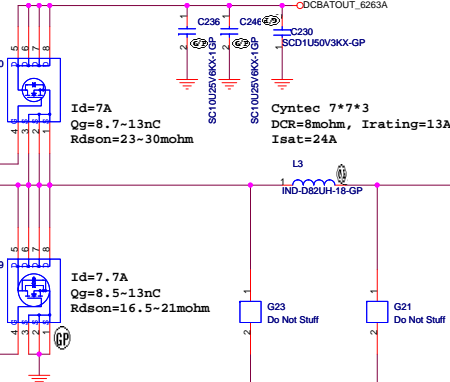
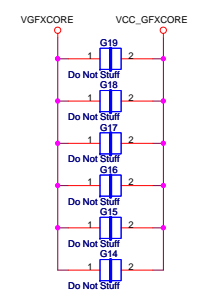
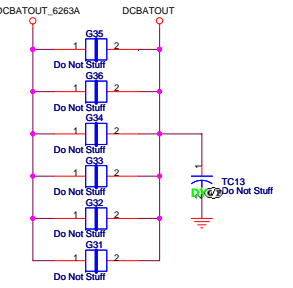
9 VSS\_AXG\_SENSE

Parallel

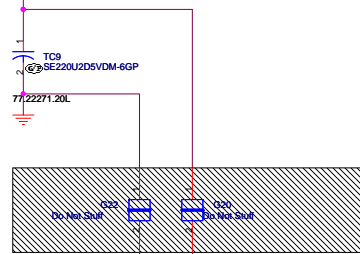
Place close to L1

<<< GFX\_VID[4..0] 7

- R148 Do Not Stuff 6236A\_VID4 GFX\_VID4
- R144 Do Not Stuff 6236A\_VID3 GFX\_VID3
- R140 Do Not Stuff 6236A\_VID2 GFX\_VID2
- R141 Do Not Stuff 6236A\_VID1 GFX\_VID1
- R142 Do Not Stuff 6236A\_VID0 GFX\_VID0



VGGFXCORE  
Iomax=6.5A  
OCP>12A



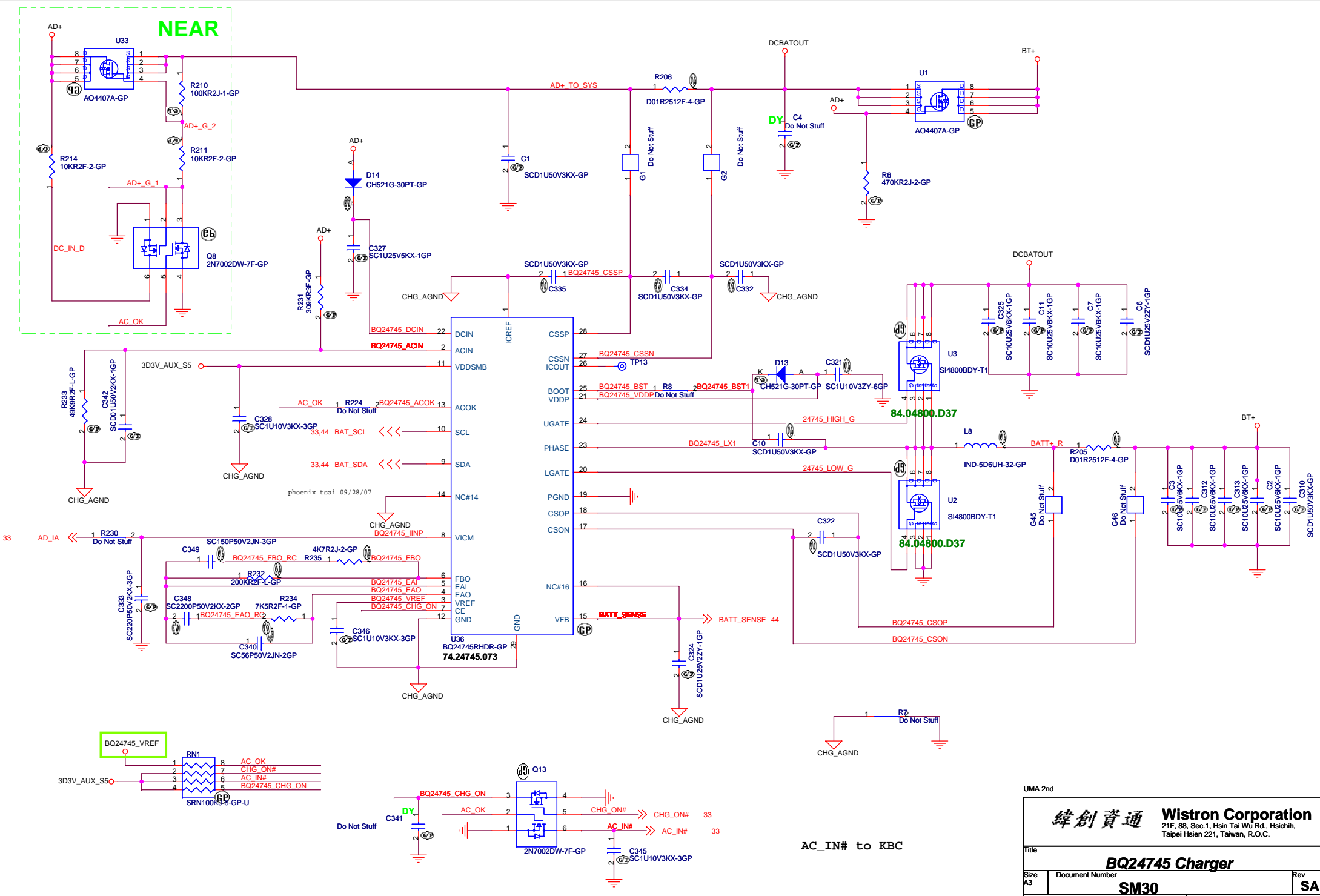
Panasonic ERT-J1VR103J

VSS\_AXG\_SENSE\_OUTCAP

VCC\_AXG\_SENSE\_OUTCAP

UMA 2nd		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>ISL6263A GFX CORE</b>		
Size Custom	Document Number <b>SM30</b>	Rev <b>SA</b>
Date: Saturday, October 18, 2008	Sheet 42 of	45

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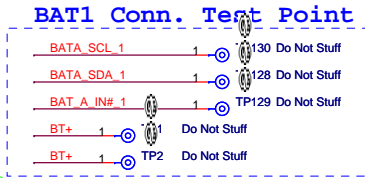
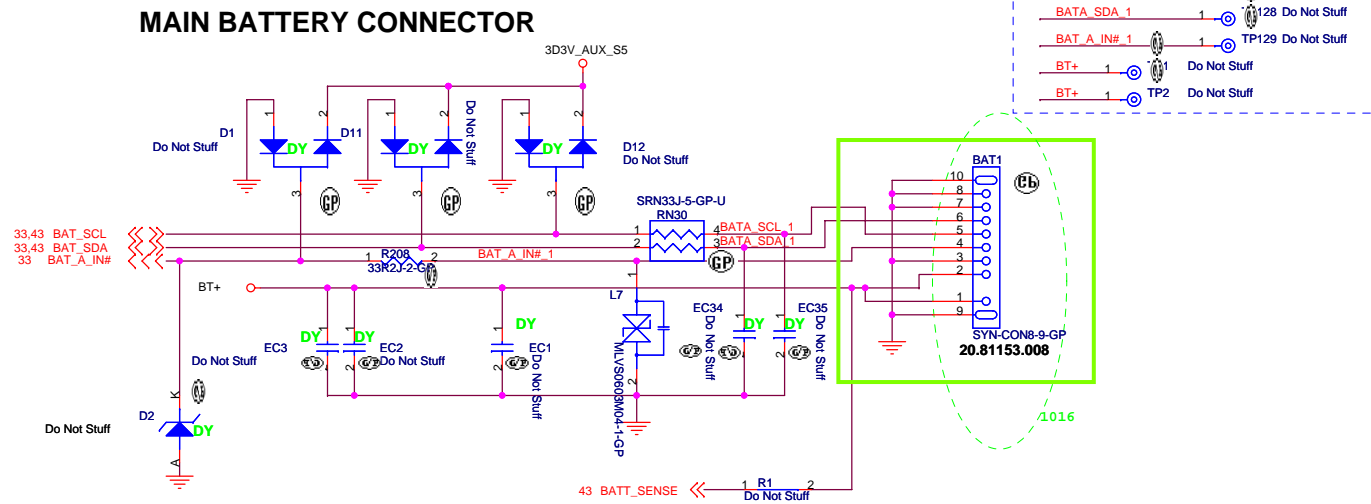
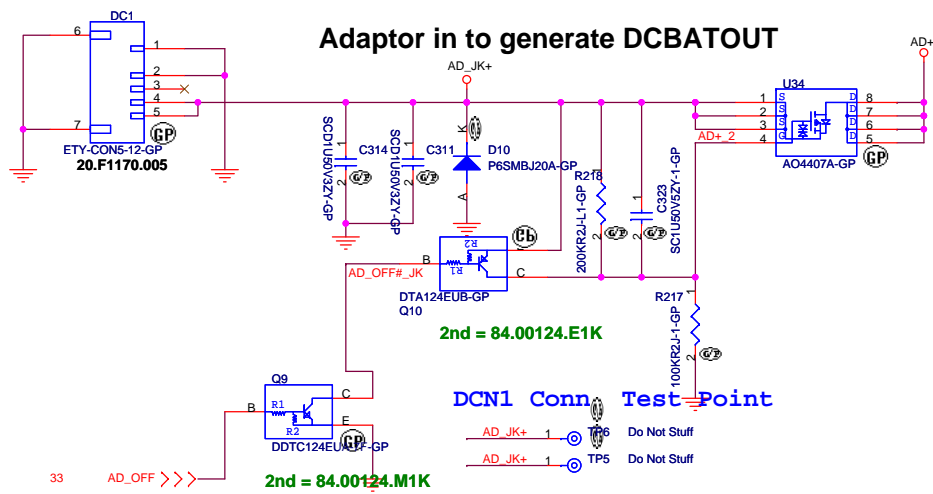
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Taipei Hsien 221, Taiwan, R.O.C.

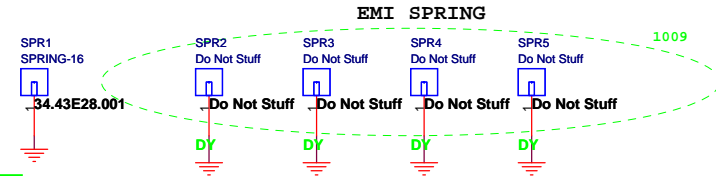
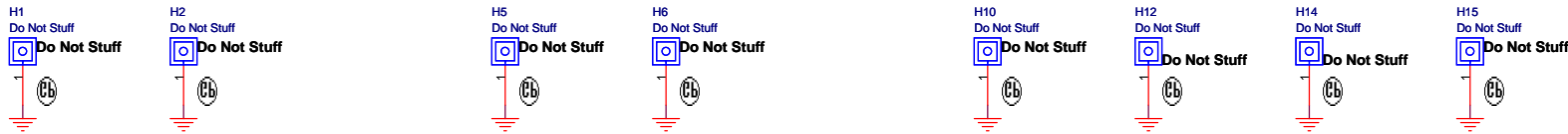
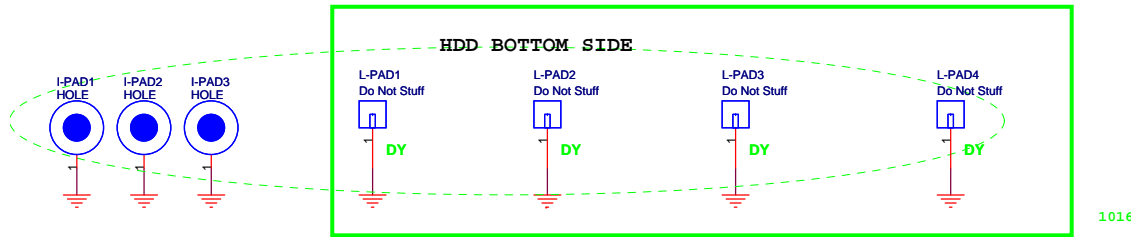
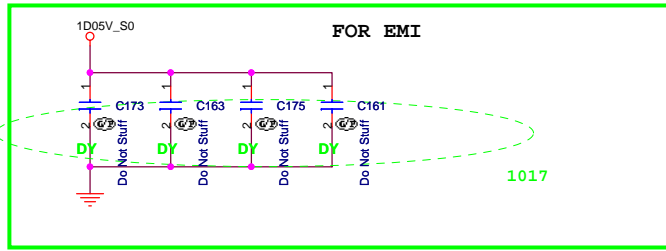
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Size: A3 | Document Number: **SM30** | Rev: **SA**

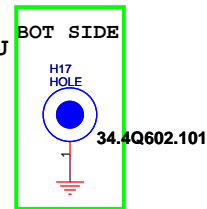
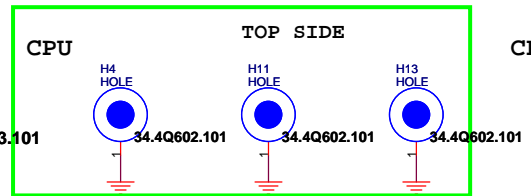
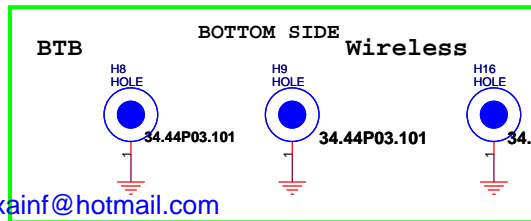
Date: Saturday, October 18, 2008 | Sheet: 43 of 45



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Stand off Location



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<p>Title: <b>EMI/Spring/Boss</b></p>	
Size: Document Number	Rev: SA
<p><b>SM30</b></p>	
Date: Monday, October 20, 2008	Sheet 45 of 45