

# ACER\_BAP31

## MAIN BOARD

2008.12.29

DATE	CHANGE NO.	REV.
Tuesday, March 10, 2009		X01

DRAWER	EE	DATE	POWER	DATE	TITLE
DESIGN					<b>INVENTEC</b>
CHECK					<b>ACER JM31</b>
RESPONSIBLE					
SIZE				VER:	SIZE CODE DOC-NUMBER REV
FILE NAME: XXXX-XXXX-XXXX					G X01 D-CS-1310A2284501.AMG X01
PN: XXXXXXXXXX					SHEET 1 of 136

# 1. Schematic Page Description :

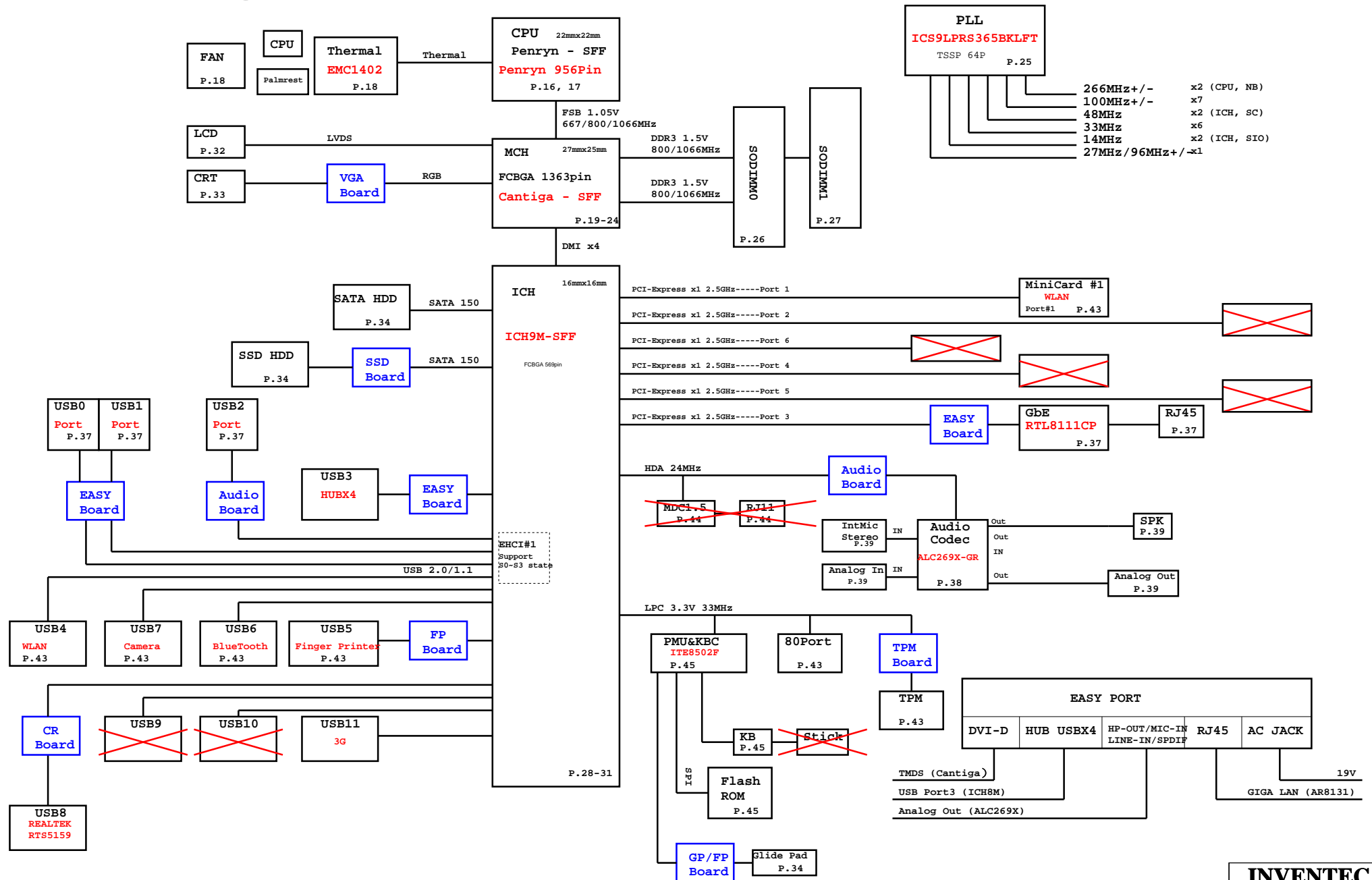
## Montevina Schematic Ver : X01

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- |                                  |                                 |
|----------------------------------|---------------------------------|
| 1. Title                         | 24. Clock Generator             |
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<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF			
Schematic Page			
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# 3. Block Diagram :



<b>INVENTEC</b>			
TITLE			
BAP31 (Penryn+Cantiga+ICH9M)SFF			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A284501-ALG	X01
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# 4. Net name Description :

## Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
-----	
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
-----	
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

## Part Naming Conventions

C	= Capacitor
CN	= Connector
D	= Diode
F	= Fuse
L	= Inductor
Q	= Transistor
R	= Resistor
RP	= Resistor Pack
U	= Arbitrary Logic Device
Y	= Crystal and Osc

## Net Name Suffix

# = Active Low signal

# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+HMEI+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA OBD- SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	4.75V-5.0V-5.25V 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

**INVENTEC**

TITLE  
BAP31 (Penryn+Cantiga+ICH9M)SFF

ANNOTATIONS

SIZE CODE DOC NUMBER REV  
Custom X01 D-CS-1310A284501ALG X01

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# 6.Schematic modify Item and History :

2009.0108

1. ADD USB P3 for Docking, USB P5 for Finger printer,  
Modify CN5 -----P28
2. Modify CN20 to 50pin-----P33
3. Move PWR\_SWIN# from CN14 to CN20
4. ADD TPM module-----P34

2009.0109

1. ADD DOCK\_USB\_EN, DOCK\_CRT\_IN#-----P32,33

2009.0112

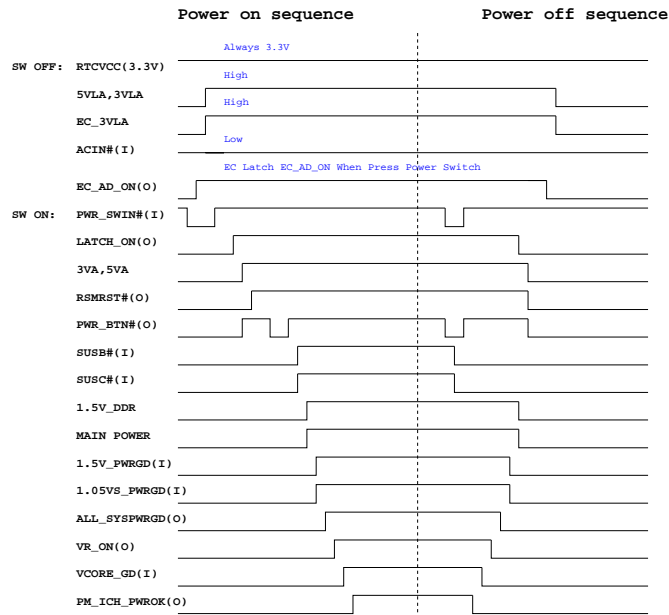
1. Change power item: R490,R291,BAT CNN TH PIN

<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF			
Schematic Modify			
SIZE Custom	CODE X01	DOC NUMBER D-CS-1310A2284501-ALG	REV X01
CHANGE by Miles Liu		DATE Tuesday, March 10, 2009	SHEET 5 of 38

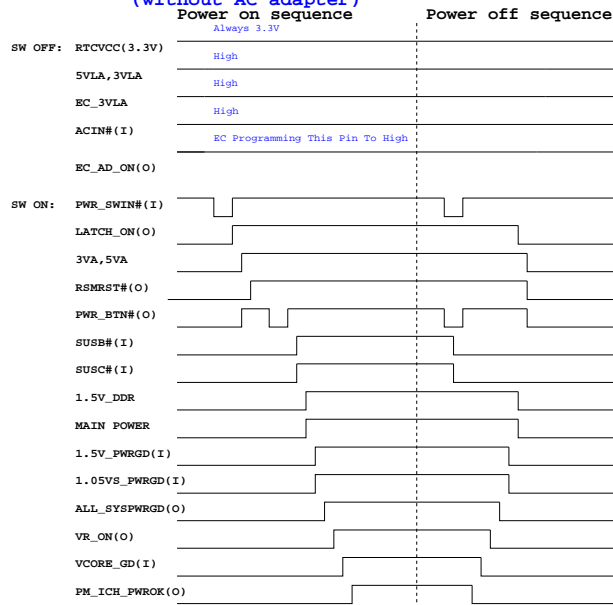
# SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

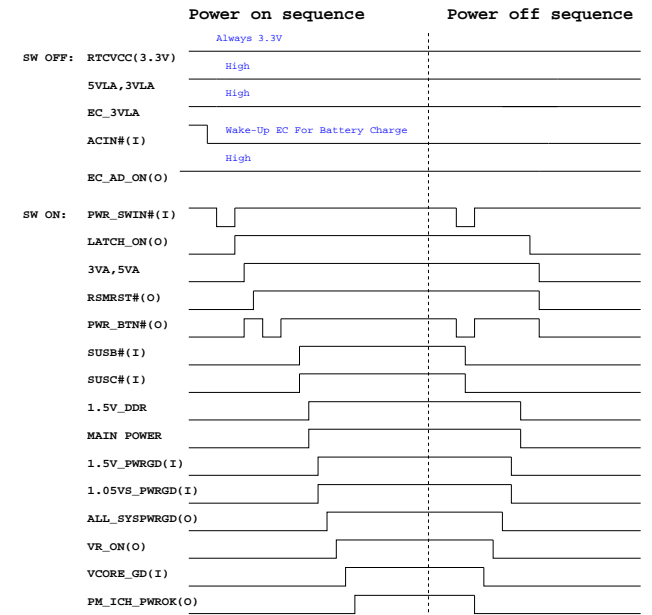
## Power on/off sequence AC insert (without Battery Pack)



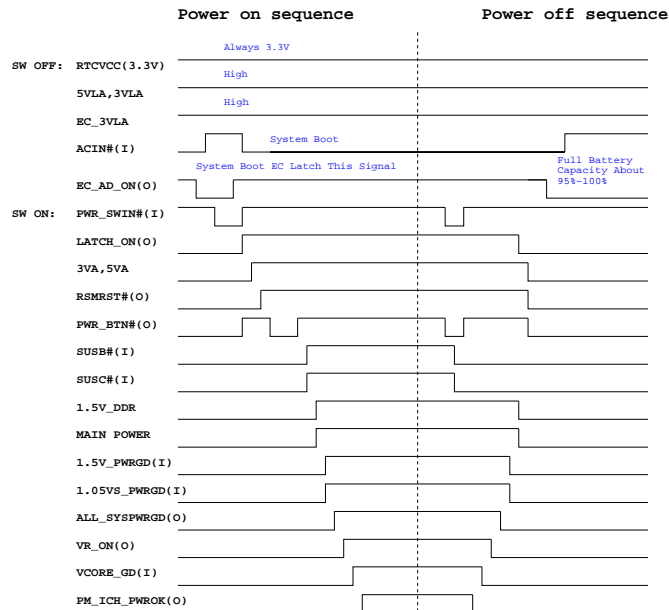
## Power on/off sequence Battery insert (without AC adapter)



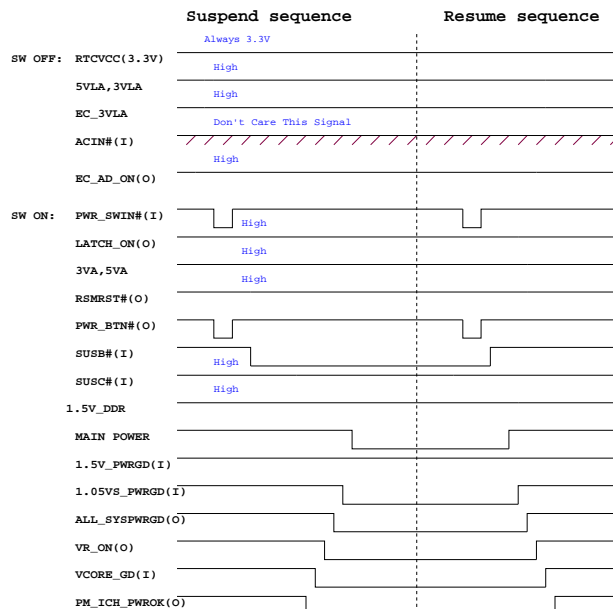
## Power on/off sequence AC insert (with charge over 95%)



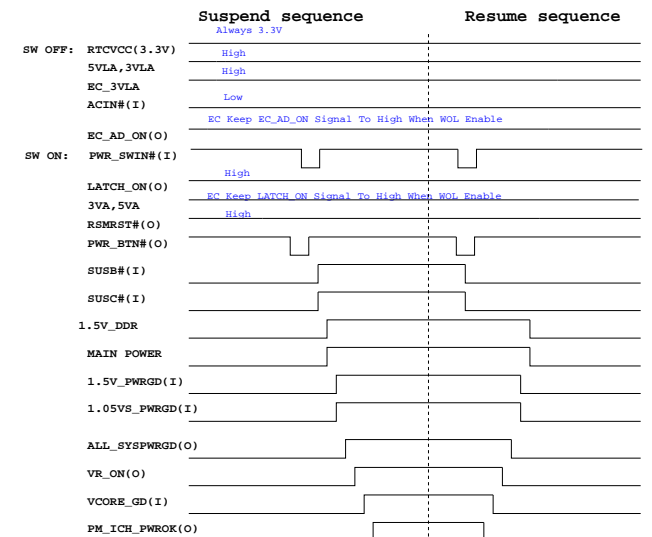
## Power on/off sequence AC insert (without charge over 95%)



## Suspend And Resume Sequence (S3)



## Power on/off sequence after windows shutdown (WOL enable)



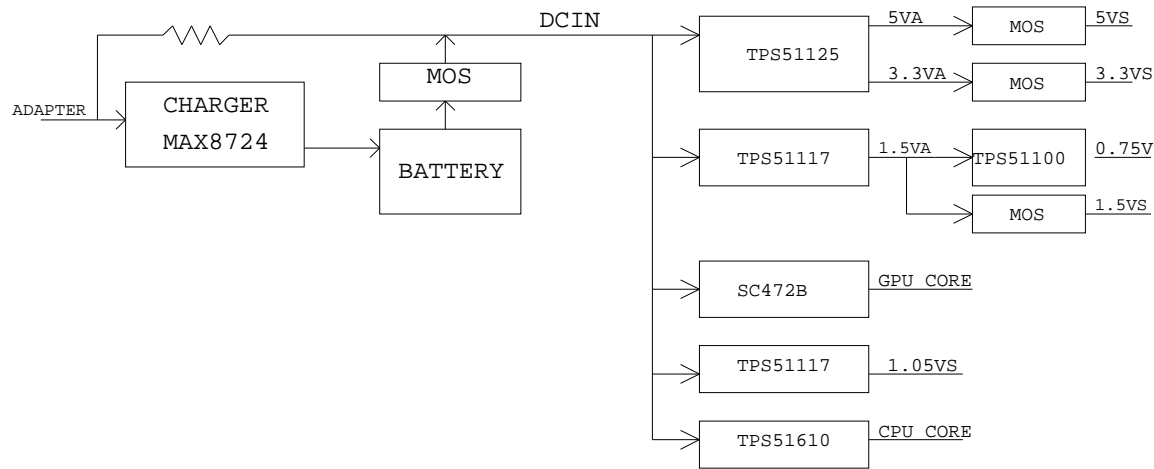
**INVENTEC**

FILE: BAP31 (Penryn+Camtiga+ICH9M)S3FF  
Time Diagram

SIZE	CODE	DOC NUMBER	REV
Custom	YH	D-SS-310A228400-ALG	YH
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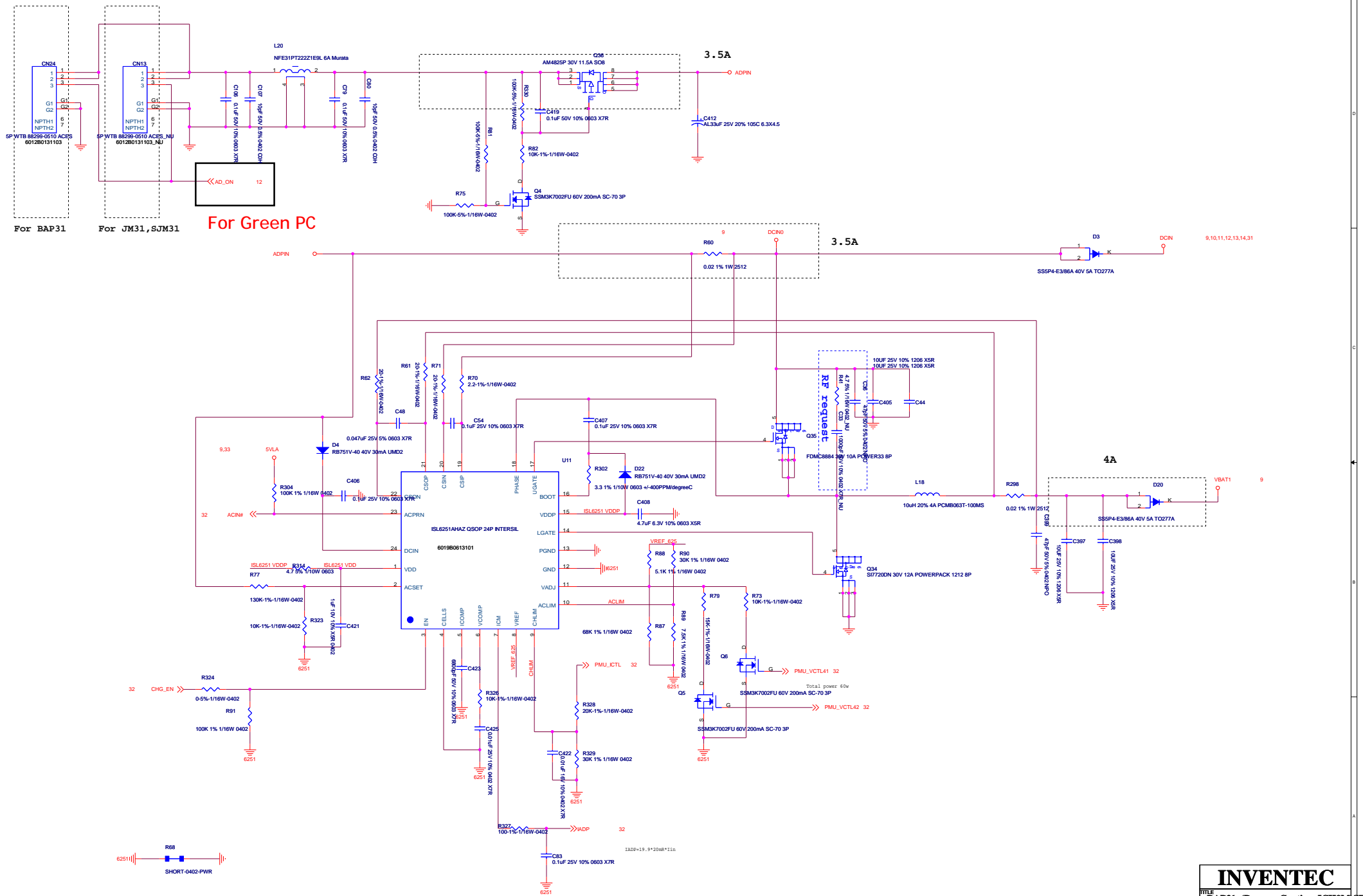
CHANGE by: Miles Liu DATE: Tuesday, March 10, 2009

# Power Block Diagram :



<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF			
Power Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	X01	D-CS-1310A284501-ALG	X01
SHEET		7	38

CHANGE by Milin Liu DATE Tuesday, March 10, 2009



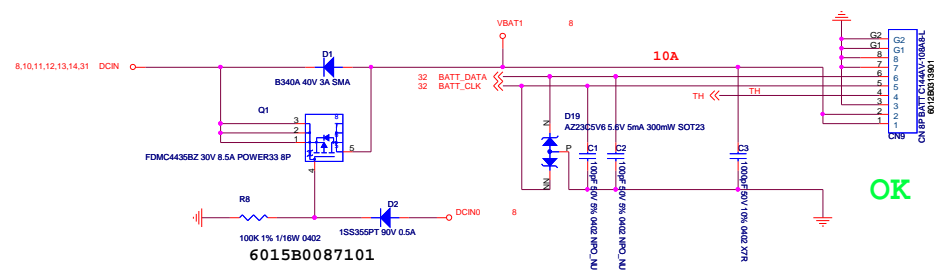
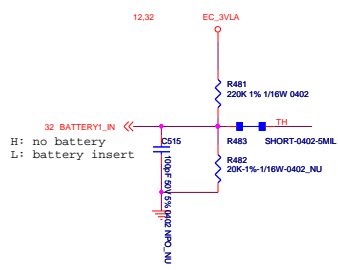
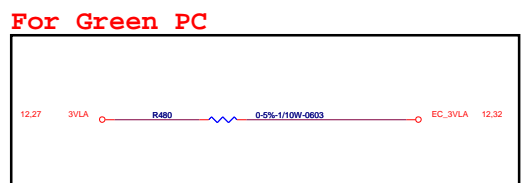
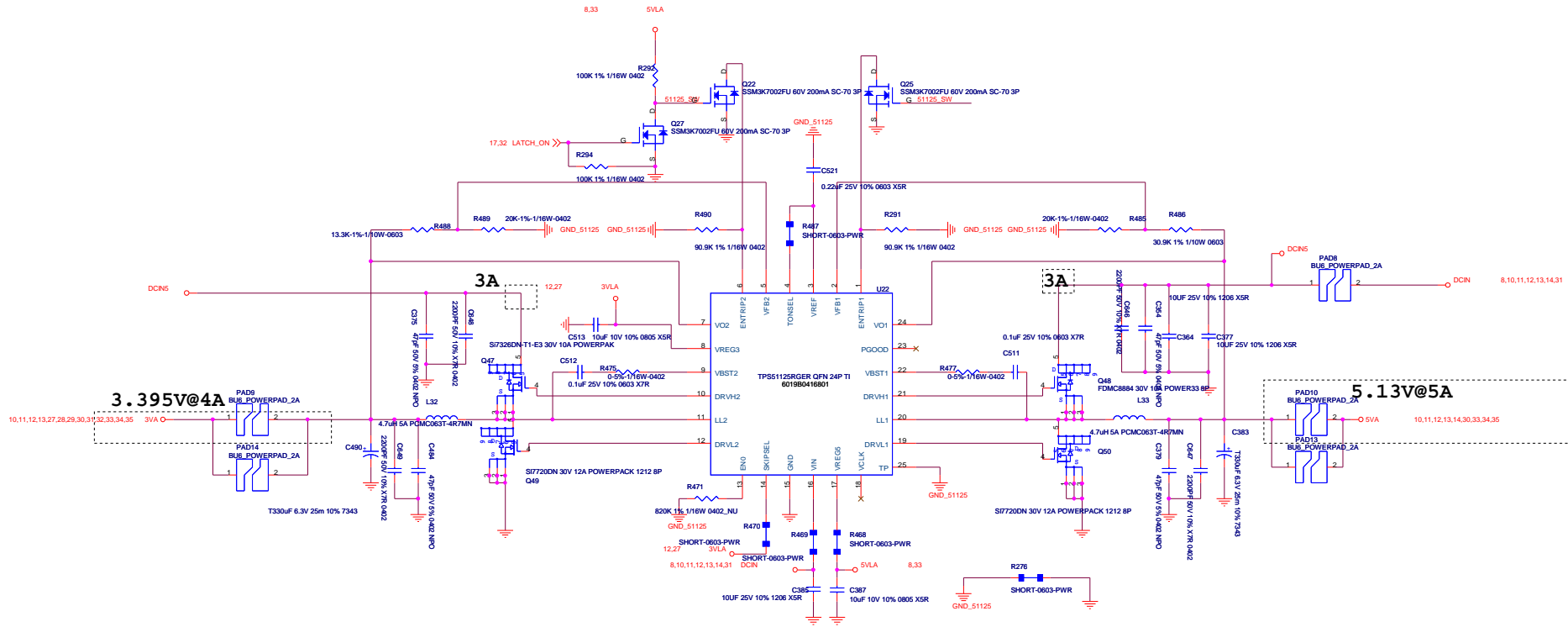
For Green PC

For BAP31

For JM31, SJM31

<b>INVENTEC</b>			
TITLE: BAP31 (Penryn+Contiga+ICH9M)SF			
Adaptor In / Charge			
SIZE: Custom	CODE: X01	DRAWING NUMBER: D-CS-1310A2264501-ALG	REV: X01
CHANGE by: Miller Liu	DATE: Tuesday, March 10, 2009	SHEET: 8	of 36





**INVENTEC**

TITLE: **BAP31 (Penryn+Cantiga+ICH9M)SF**

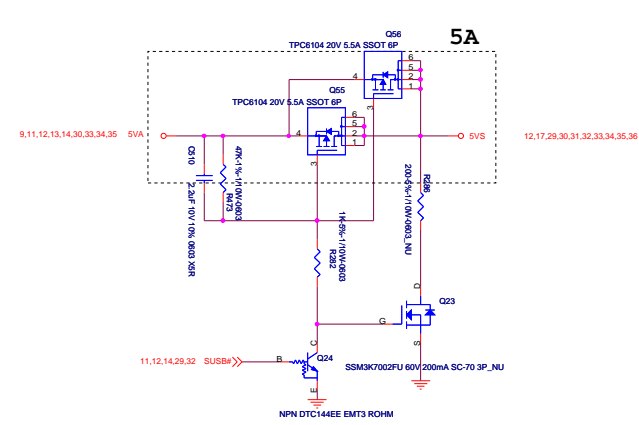
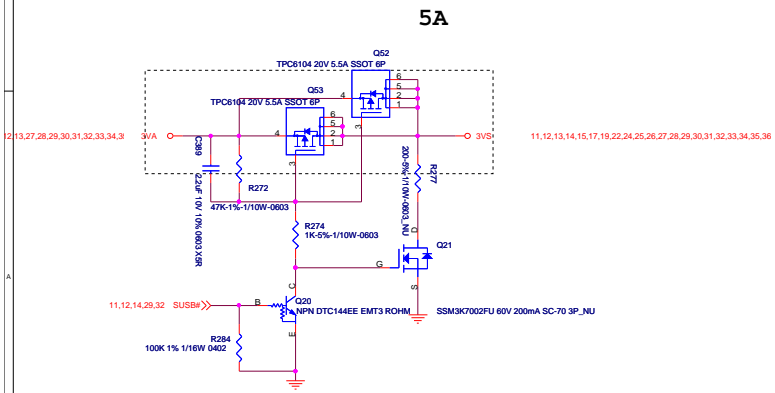
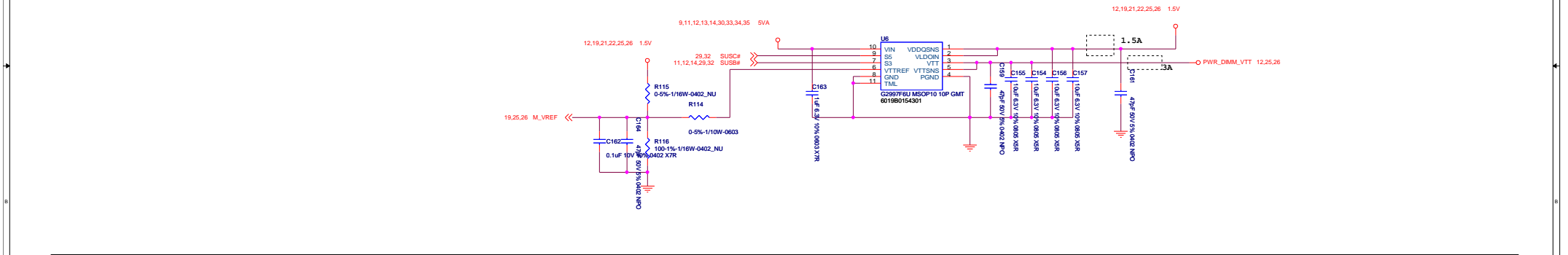
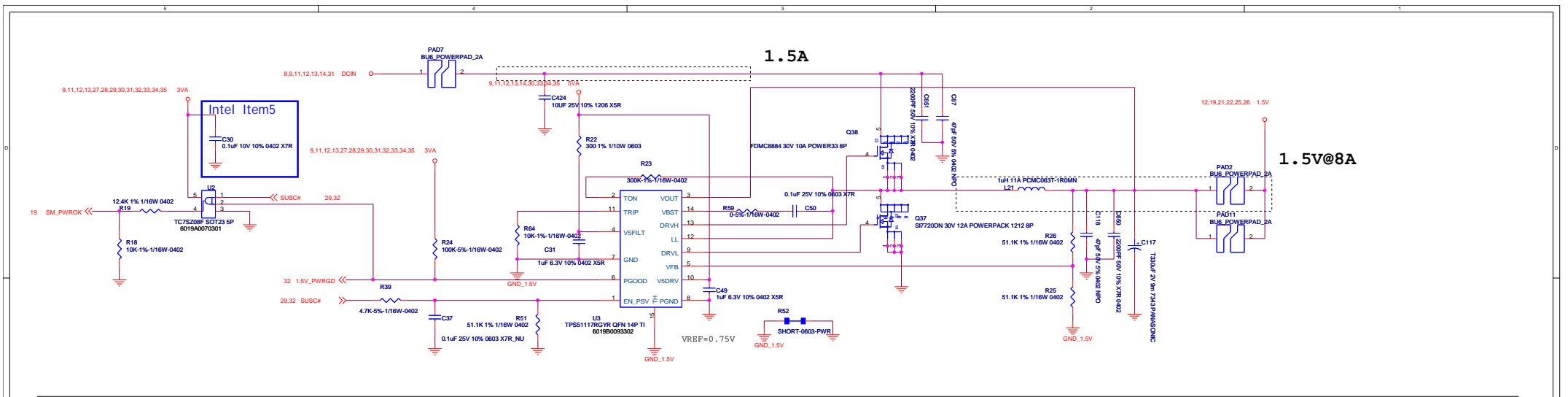
SIZE: Custom

CODE: X01

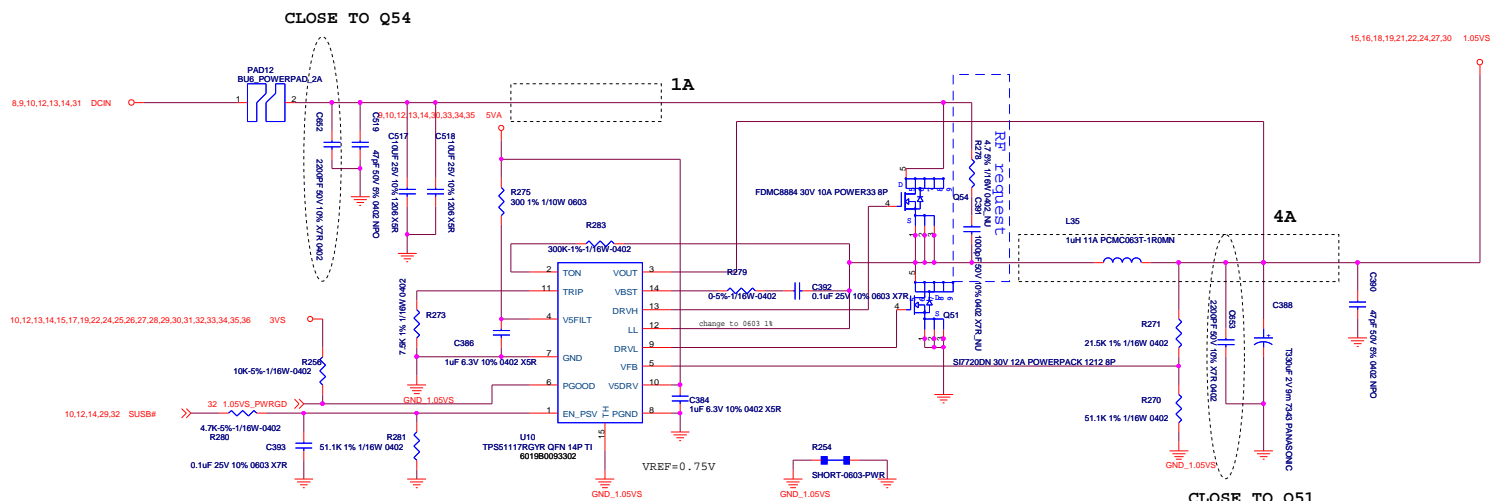
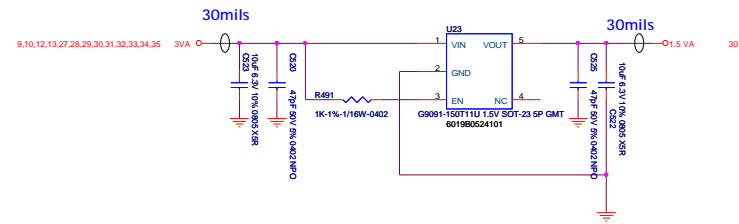
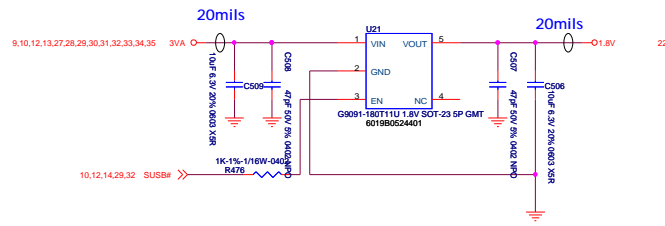
REV: X01

D-C-S: 1310A2264501-ALG

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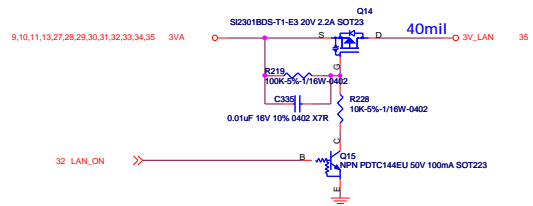
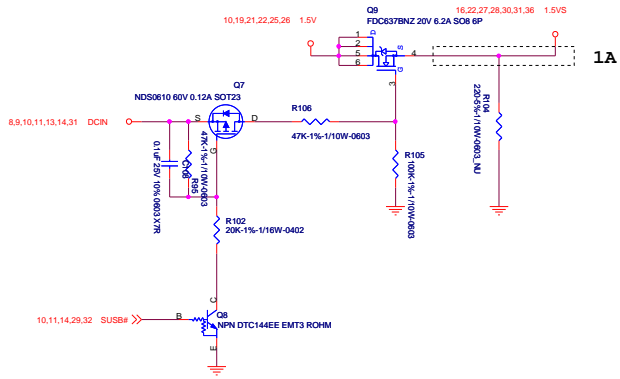


<b>INVENTEC</b>			
TITLE <b>BAP31 (Penryn+Cartiga+ICH9M)SF</b>			
SIZE <b>3VS/5VS/1.5V (DDR3)</b>			
CODE X01	DOC NUMBER D-CS-1310A2264501-ALG	REV X01	
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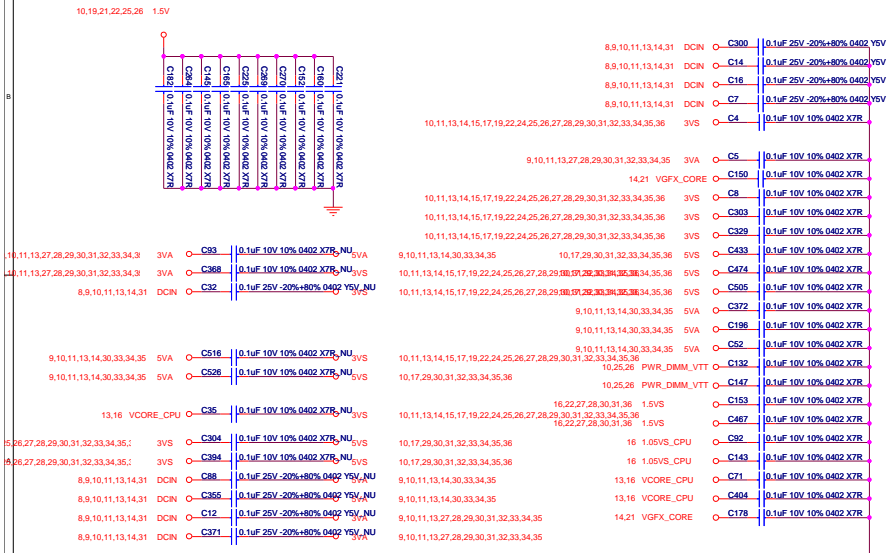


<b>INVENTEC</b>			
TITLE <b>BAP31 (Penryn+Cantiga+ICH9M)SF</b>			
1.05VS/1.5V/1.8V/1.5VA			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
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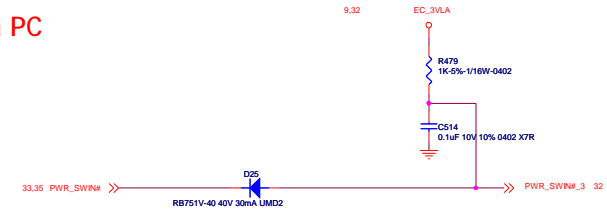
# 1.5VS



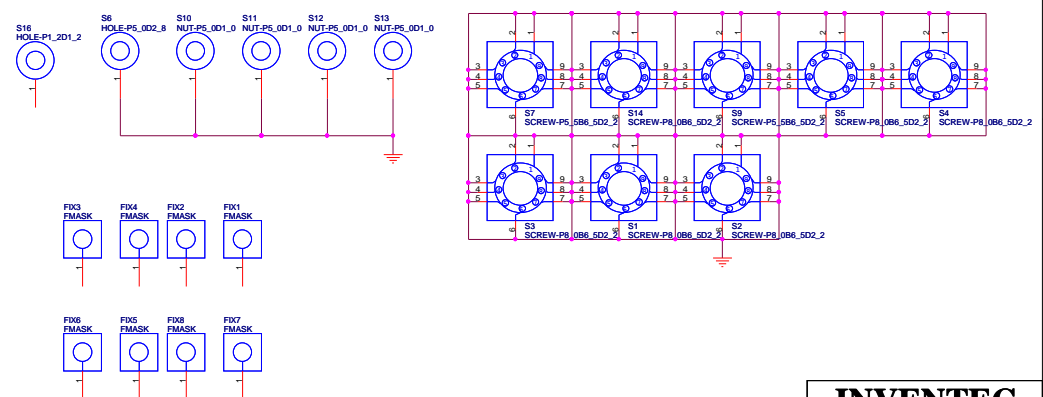
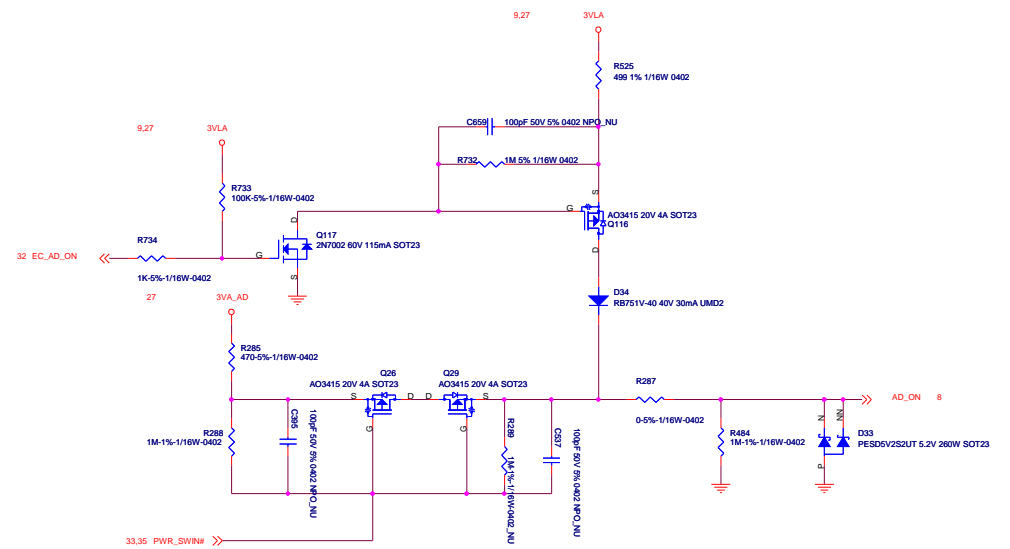
# EMI Cap



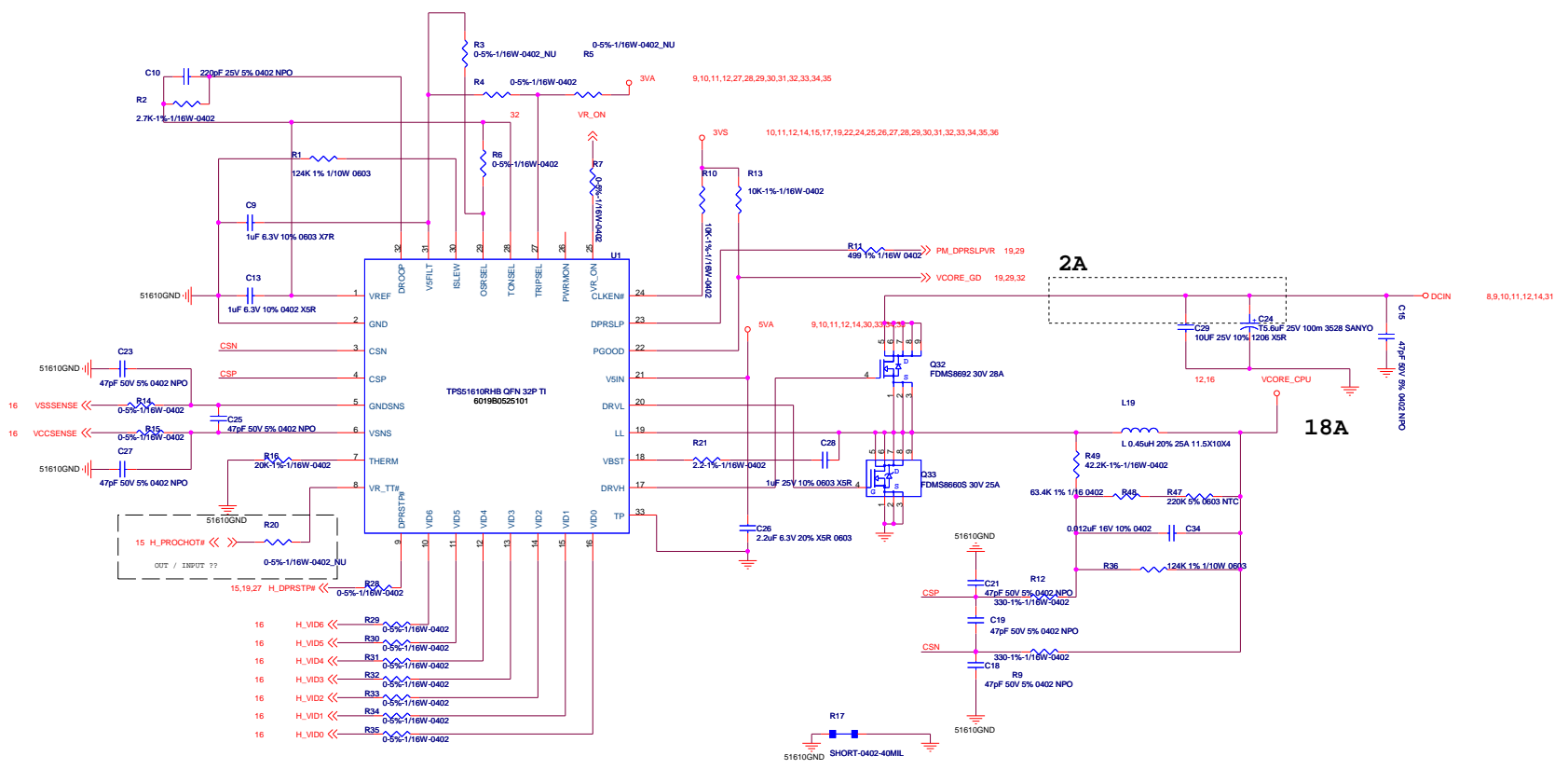
# For Green PC



# None Green PC ---- NU

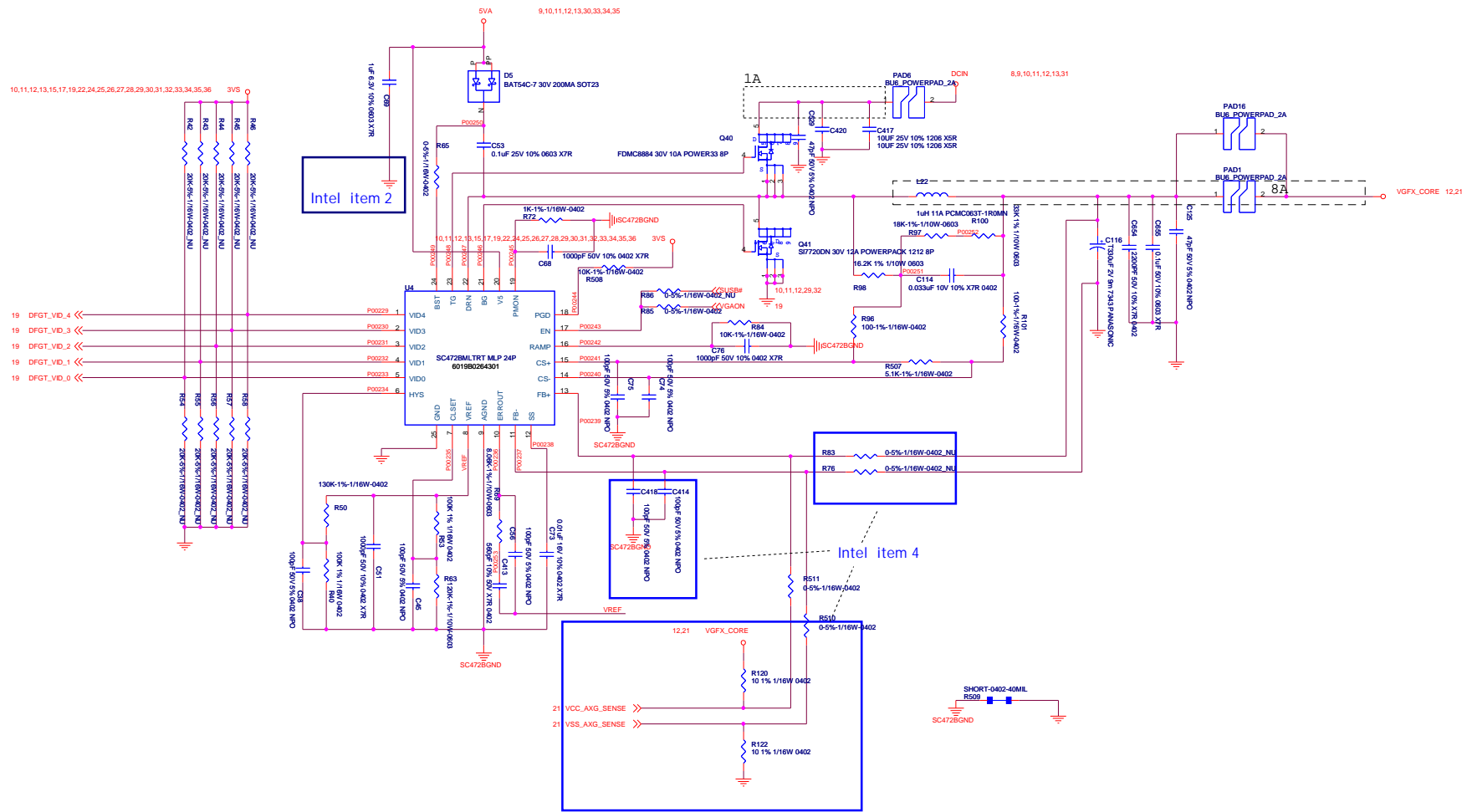


<b>INVENTEC</b>			
TITLE <b>BAP31 (Penryn+Cantiga+ICH9M)SF</b>			
Power on latch			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
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<b>INVENTEC</b>			
TITLE: BAP31 (Penryn+Centiga+ICH9M)SFF			
CPU Core Power			
SIZE	CODE	DOC NUMBER	REV
C	X01	D-CS-1310A2284501ALG	X01
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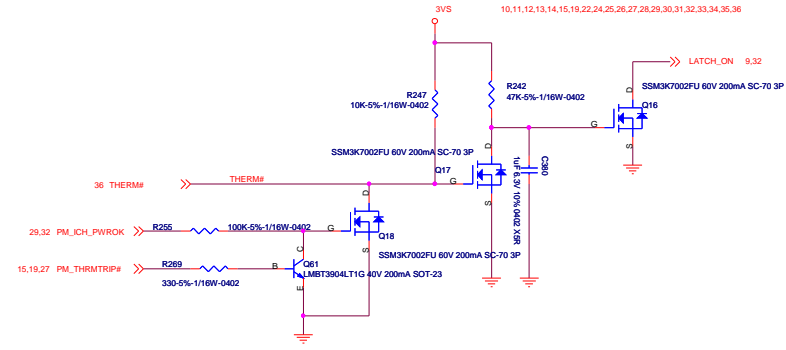
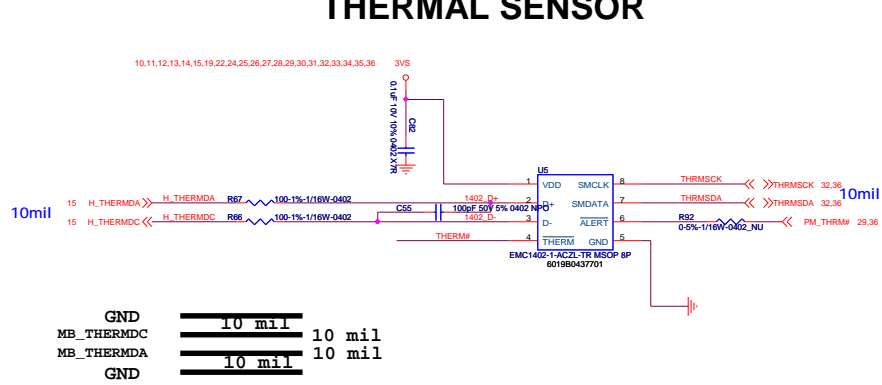
<b>INVENTEC</b>			
TITLE <b>BAP31 (Penryn+Cantiga+ICH9M)SF</b>			
GPU CORE			
SIZE Custom	CODE X01	DOC NUMBER D-CS-1310A2264501-ALG	REV X01
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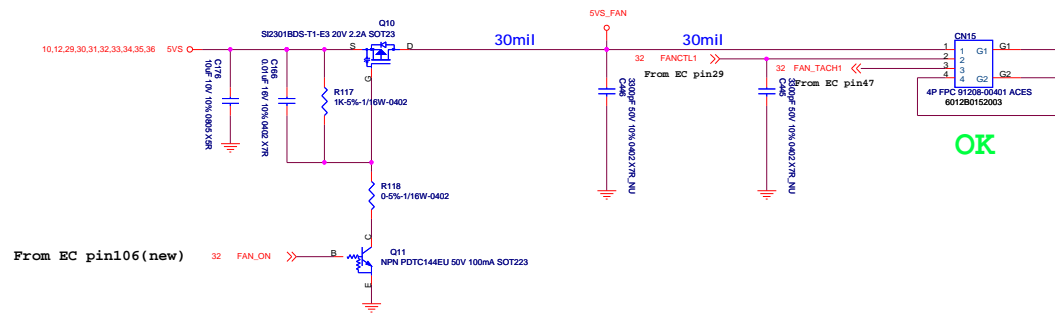




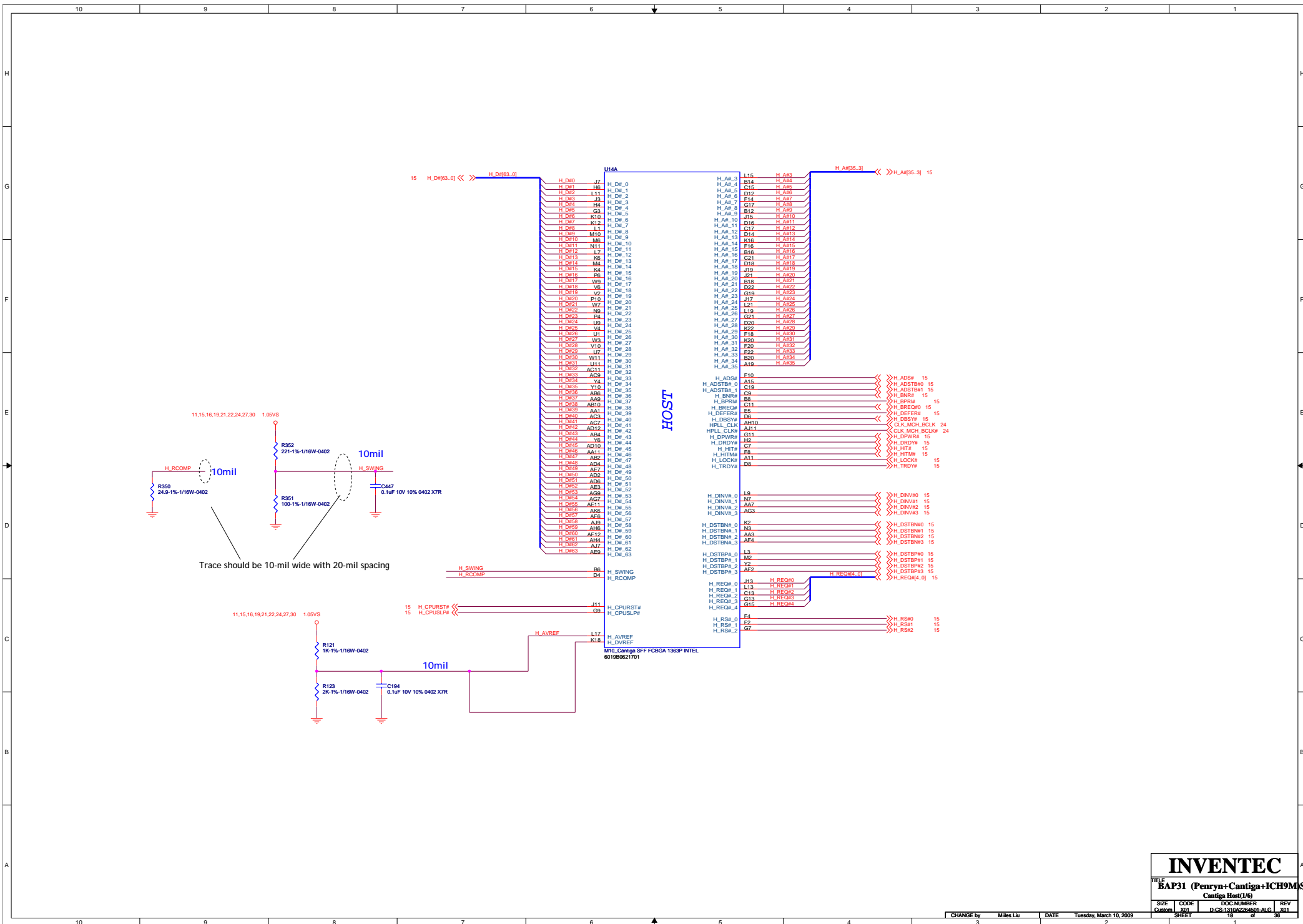
# THERMAL SENSOR



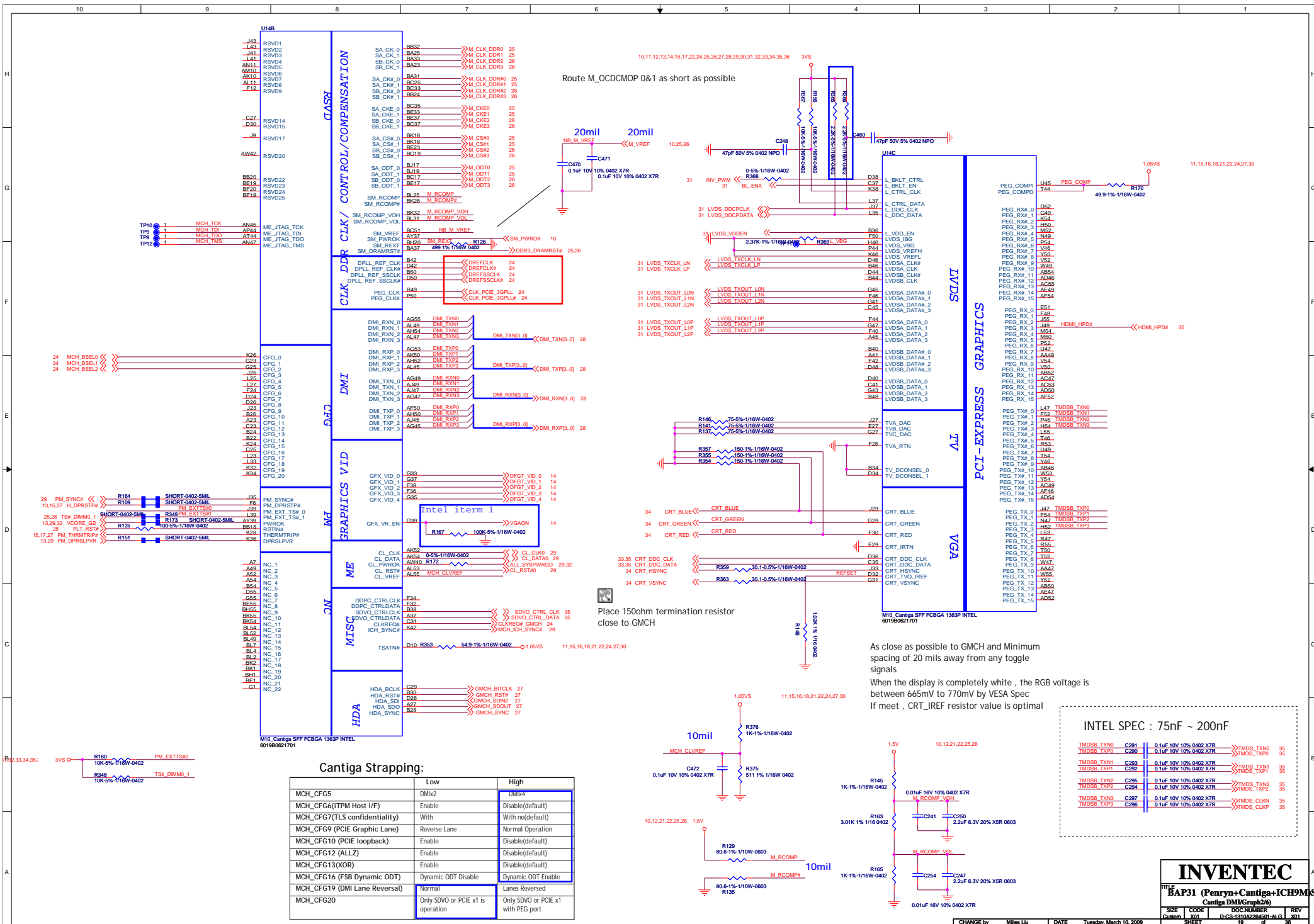
# Fan control



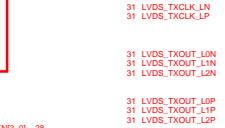
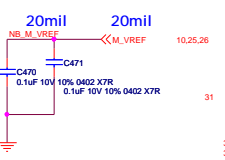
<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Contiga+ICH9M)SFF			
CPU Thermal			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A284501-ALG	X01
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<b>INVENTEC</b>			
TITLE: <b>BAP31 (Penryn+Camiga+ICH9M)SFF</b>			
Camiga Host(1/6)			
SIZE	CODE	DOCNUMBER	REV
Custom	X01	D-CS-1310A2284501-ALG_L_X01	1
CHANGE by Miles Lu		DATE Tuesday, March 10, 2009	SHEET 1 of 38



Route M\_OCDCMOP 0&1 as short as possible



Place 150ohm termination resistor close to GMCH



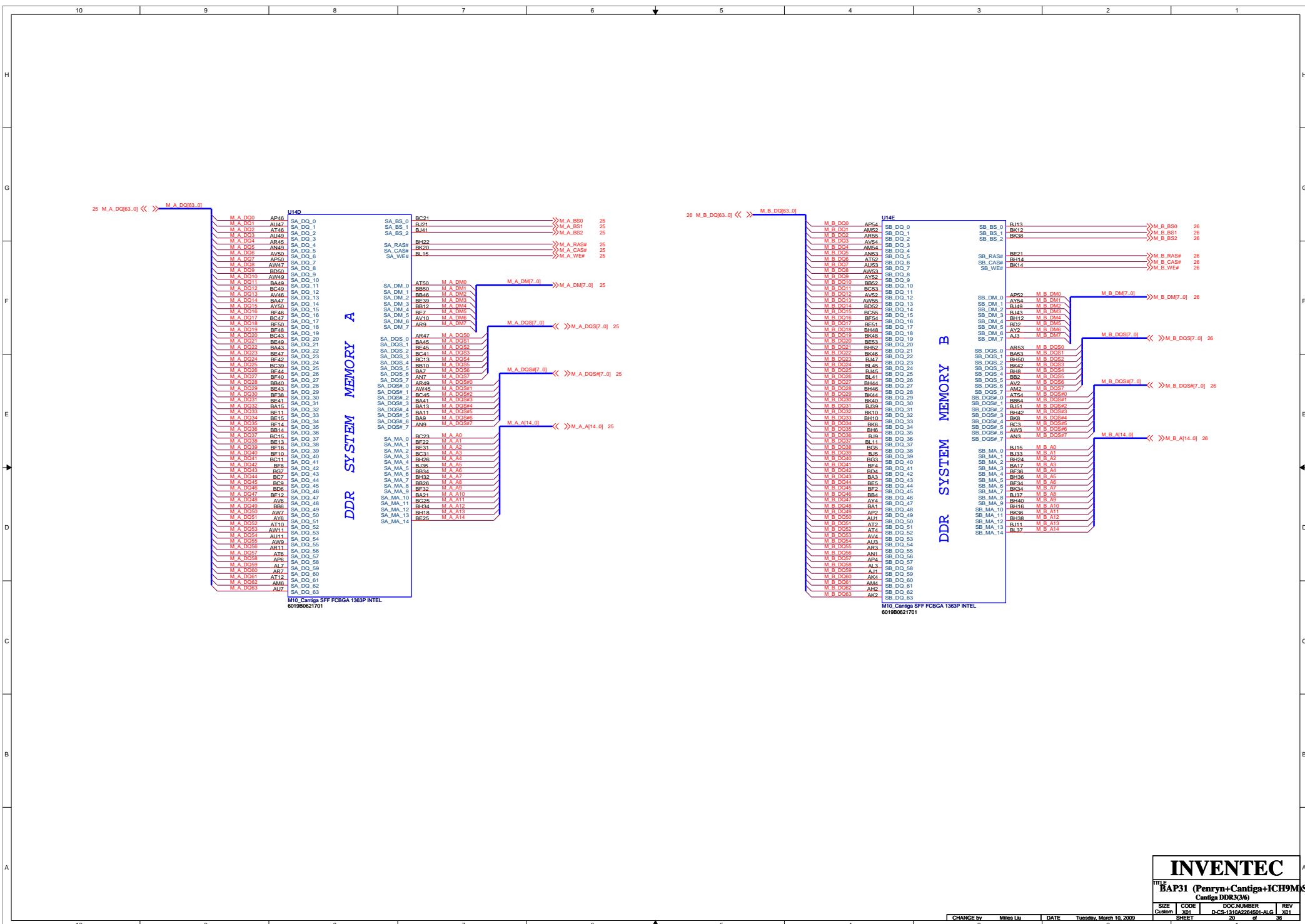
Cantiga Strapping:

	Low	High
MCH_CFG5	DmiI2	DmiI4
MCH_CFG6(TPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIe Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIe loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIe x1 is operation	Only SDVO or PCIe x1 with PEG port

INTEL SPEC : 75nF ~ 200nF

- TMSB\_TXN0 C291 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXN0 35
- TMSB\_TXP0 C290 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXP0 35
- TMSB\_TXN1 C293 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXN1 35
- TMSB\_TXP1 C292 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXP1 35
- TMSB\_TXN2 C295 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXN2 35
- TMSB\_TXP2 C294 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXP2 35
- TMSB\_TXN3 C297 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXN3 35
- TMSB\_TXP3 C296 0.1uF 10V 10% 0402 X7R >>>TMSB\_TXP3 35

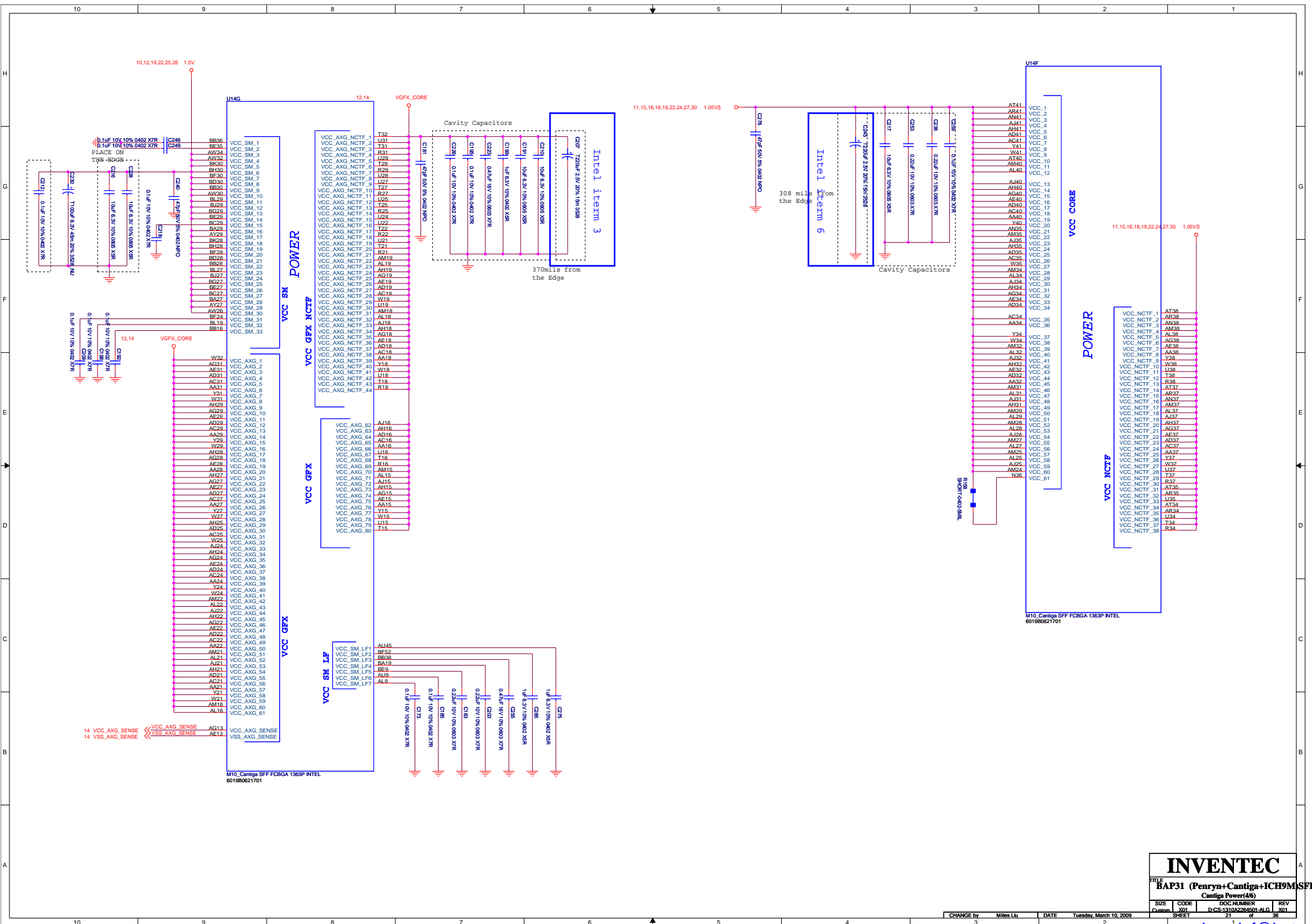
**INVENTEC**  
 TITLE: BAP31 (Penryn+ Cantiga-I CH9M) SFF  
 Cantiga DMI/Graphic2/6  
 SIZE: Custom X11  
 CODE: 01  
 DOC NUMBER: D-CS-1310A2284601-ALG\_X01  
 REV: 01  
 SHEET: 19 of 38

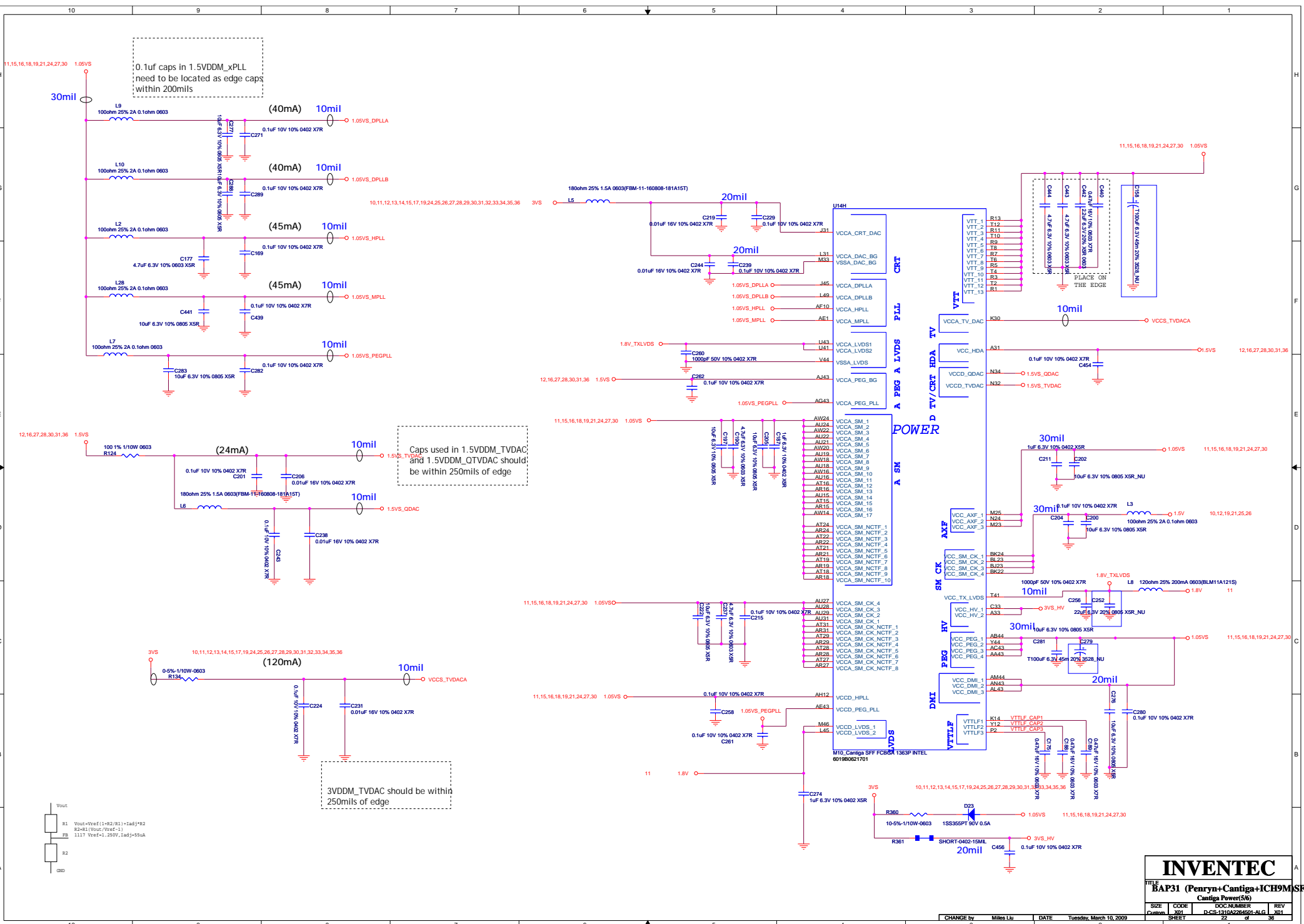


M10, Cantiga SFF FC8GA 1363P INTEL  
601980621701

M10, Cantiga SFF FC8GA 1363P INTEL  
601980621701

**INVENTEC**  
 TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF  
 Cantiga DDR3(36)  
 SIZE: Custom    CODE: X01    DOC NUMBER: D-CS-1310A2284501-ALG\_L\_X01    REV: 20  
 CHANGE BY: Miles Lu    DATE: Tuesday, March 10, 2009    SHEET: 1 of 36





0.1uF caps in 1.5VDDM\_xPLL need to be located as edge caps within 200mils

Caps used in 1.5VDDM\_TVDAC and 1.5VDDM\_QTVDAC should be within 250mils of edge

3VDDM\_TVDAC should be within 250mils of edge

$V_{out} = V_{ref} \left( 1 + \frac{R2}{R1} \right) + I_{adj} R2$   
 $I_{adj} = \frac{V_{ref}}{R1} \left( \frac{R2}{R1} + 1 \right) + I_{adj}$   
 $I_{adj} = 1.25V \left( \frac{R2}{R1} + 1 \right) + I_{adj}$

- U14H VCCA\_CRT\_DAC
- M33 VCCA\_DAC\_BG
- M33 VSSA\_DAC\_BG
- L31 VCCA\_DPLLA
- M33 VCCA\_DPLLB
- M33 VCCA\_HPLL
- M33 VCCA\_MPLL
- L43 VCCA\_LVDS1
- L41 VCCA\_LVDS2
- V44 VSSA\_LVDS
- A43 VCCA\_PEG\_BG
- AG43 VCCA\_PEG\_PLL
- AV24 VCCA\_SM\_1
- AV24 VCCA\_SM\_2
- AV24 VCCA\_SM\_3
- AV22 VCCA\_SM\_4
- AV20 VCCA\_SM\_5
- AV19 VCCA\_SM\_6
- AV18 VCCA\_SM\_7
- AV17 VCCA\_SM\_8
- AV16 VCCA\_SM\_9
- AV15 VCCA\_SM\_10
- AT18 VCCA\_SM\_11
- AT16 VCCA\_SM\_12
- AT15 VCCA\_SM\_13
- AT14 VCCA\_SM\_14
- AT13 VCCA\_SM\_15
- AT12 VCCA\_SM\_16
- AV14 VCCA\_SM\_17
- AT24 VCCA\_SM\_NCTF\_1
- AR24 VCCA\_SM\_NCTF\_2
- AT22 VCCA\_SM\_NCTF\_3
- AR22 VCCA\_SM\_NCTF\_4
- AT21 VCCA\_SM\_NCTF\_5
- AR21 VCCA\_SM\_NCTF\_6
- AT19 VCCA\_SM\_NCTF\_7
- AT18 VCCA\_SM\_NCTF\_8
- AR18 VCCA\_SM\_NCTF\_9
- AV14 VCCA\_SM\_NCTF\_10
- AL27 VCCA\_SM\_CK\_4
- AL26 VCCA\_SM\_CK\_3
- AL25 VCCA\_SM\_CK\_2
- AL24 VCCA\_SM\_CK\_1
- AT31 VCCA\_SM\_CK\_NCTF\_1
- AT29 VCCA\_SM\_CK\_NCTF\_2
- AT28 VCCA\_SM\_CK\_NCTF\_3
- AT27 VCCA\_SM\_CK\_NCTF\_4
- AT26 VCCA\_SM\_CK\_NCTF\_5
- AT25 VCCA\_SM\_CK\_NCTF\_6
- AT24 VCCA\_SM\_CK\_NCTF\_7
- AT23 VCCA\_SM\_CK\_NCTF\_8
- AT22 VCCA\_SM\_CK\_NCTF\_9
- AT21 VCCA\_SM\_CK\_NCTF\_10
- AH12 VCCD\_HPLL
- AE43 VCCD\_PEG\_PLL
- M46 VCCD\_LVDS\_1
- L45 VCCD\_LVDS\_2
- M274 1uF 6.3V 10% 0402 X7R

**INVENTEC**

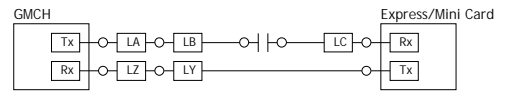
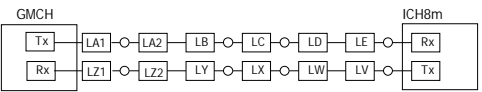
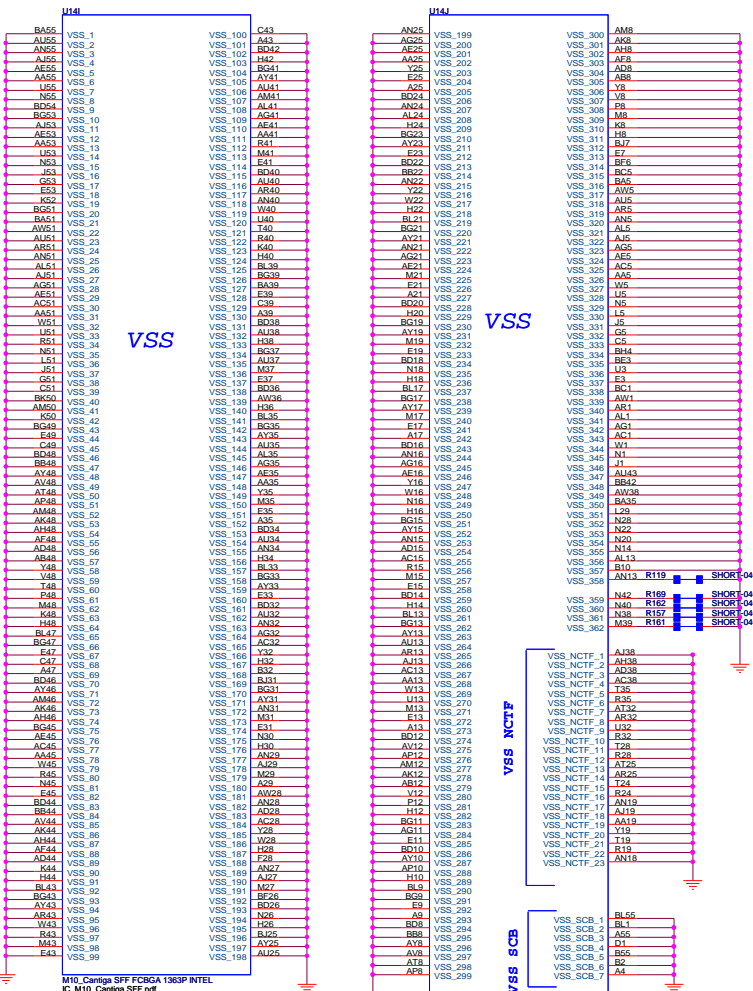
TITLE: BAP31 (Penryn+Cantiga+ICH9M) SFF Cantiga Power (56)

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2284501-ALG_X01	22

CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 2 of 36

# DMI Routing Guideline

# PCIe Routing Guideline



Breakout/in LA/LZ	Main Route	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

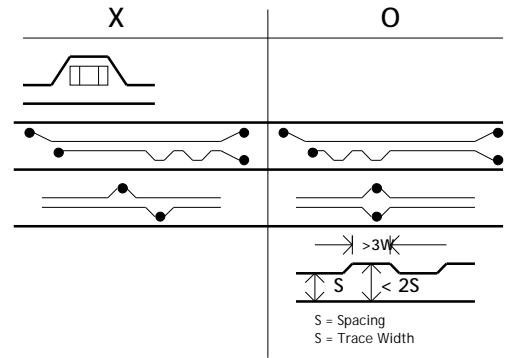
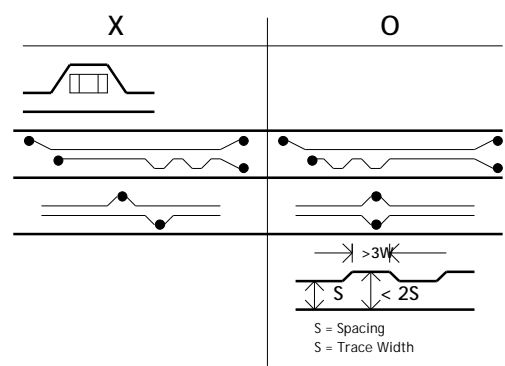
Breakout/in LA/LZ	Main Route	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip			Microstrip
				Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal Diddential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	No routing over plane splits No routing over voids
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-LI (LA-LB-LC-LD-LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV-LW-LX-LY-LZ)	Max = 8000 mils	

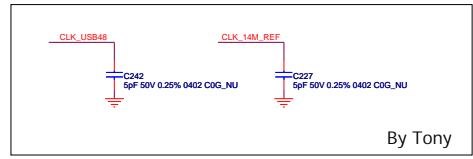
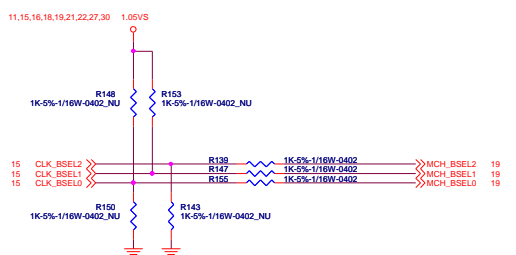
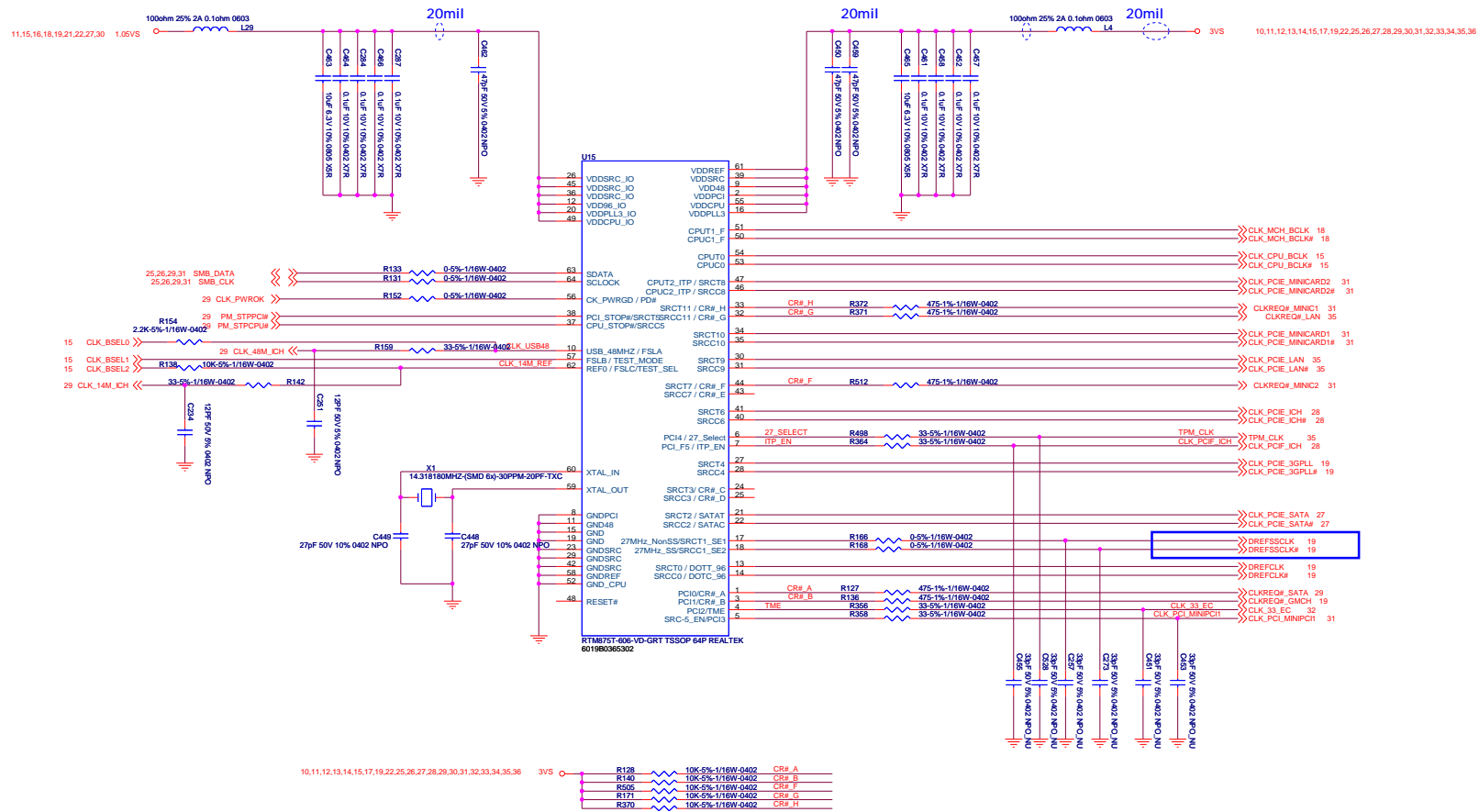
Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal Diddential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	No routing over plane splits No routing over voids
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe Ch)	Max = 10750 mils	
Trace Length-L1 (LA-LB-LC)	Max = 12000 mils	
Trace Length-LY (PCIe Ch to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY-LZ)	Max = 12000 mils	

\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane  
\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

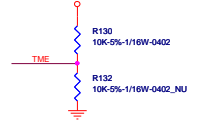
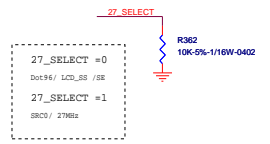
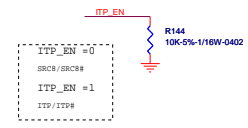
\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane  
\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



**INVENTEC**  
 TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF  
 Cantiga Ground(6/6)  
 SIZE: X01  
 CODE: X01  
 SHEET: 23 of 38  
 REV: 01  
 DOC NUMBER: D-CS-1310A2284501-ALG



FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *

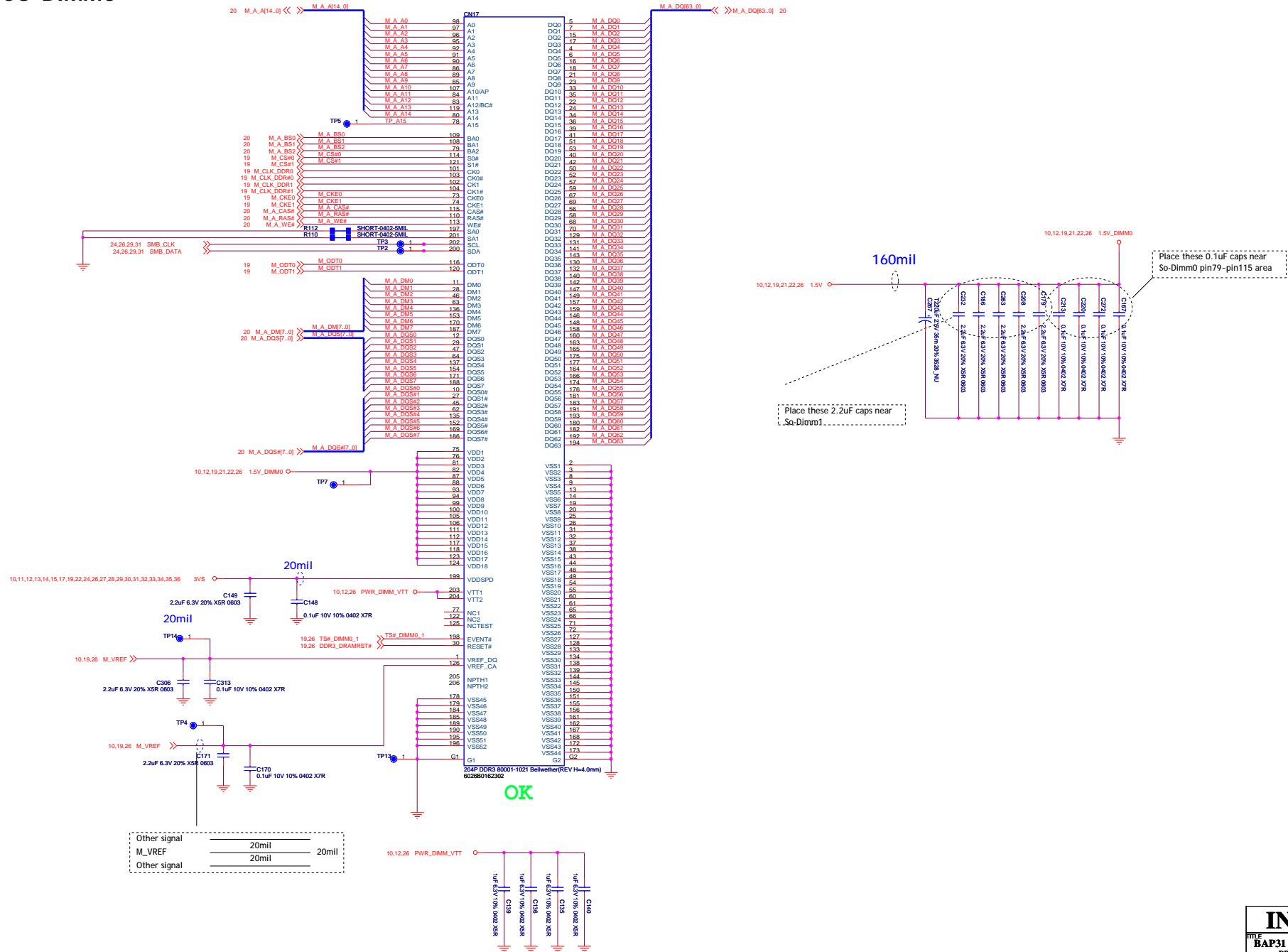


CR#_A:	Byte 5 bit 6--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

**INVENTEC**  
 TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF  
 Clock Generator  
 SIZE: Custom X01  
 CODE: X01  
 SHEET: 24 of 36  
 CHANGE by: Milon Liu  
 DATE: Tuesday, March 10, 2009

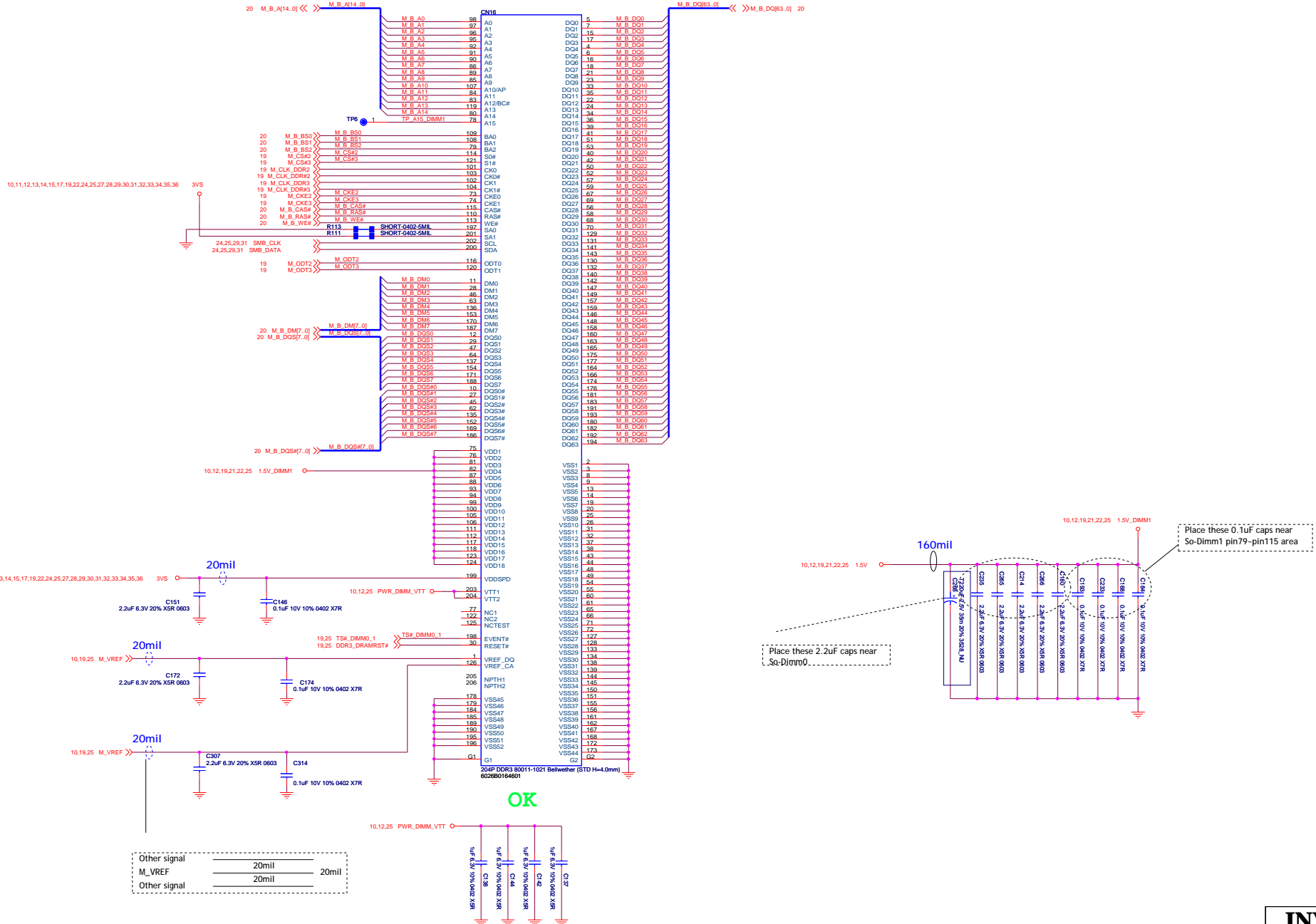


# SO-DIMMO



<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF DDR3 SDRAM SO-DIMMO			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2284501.ALG	X01
CHANGE by		DATE	REV
Miles Liu		Tuesday, March 10, 2009	26
SHEET		of	38

# SO-DIMM1

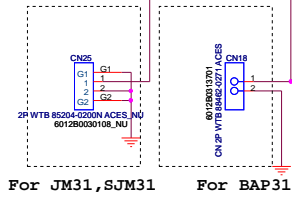


<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF			
DDR3 SDRAM SO-DIMM1			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A284501.ALG	X01
SHEET		26	of 36

# RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch ( from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

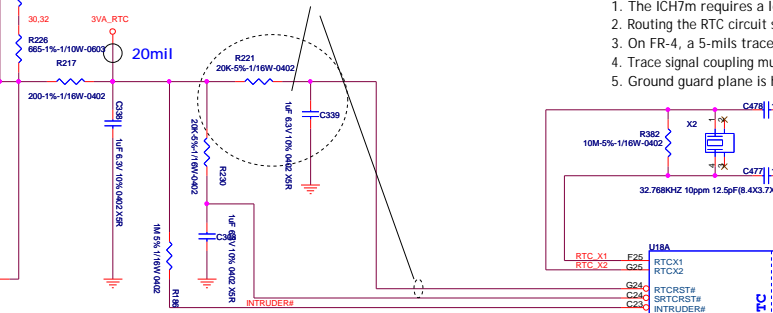


For Green PC

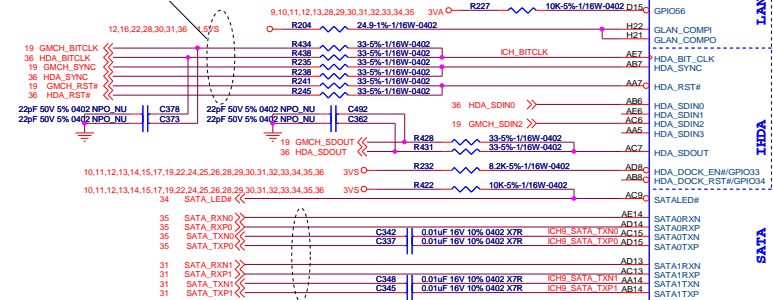


123  
CABLE\_ROUND\_3POS\_75mm\_I\_RTC\_NU  
6027B0066801

RTC Battery Life :  
220mAh(220000uAh) / 6uA = 4.2 year



Place all series resistors 0.6 to 2.6 inches from the ICH9



Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

Placed within 500mils of ICH9m ball

Short pins AG1 and AG2 at the package

ICH8m internal VR enable strap

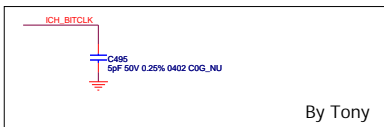
INTVRMEN	Enable	Disable
0	1(Default)	0

Internal VRM enabled for VccSus1\_05, VccSus1\_5, VccCL1\_5, VccLAN1\_05 and VccCL1\_05

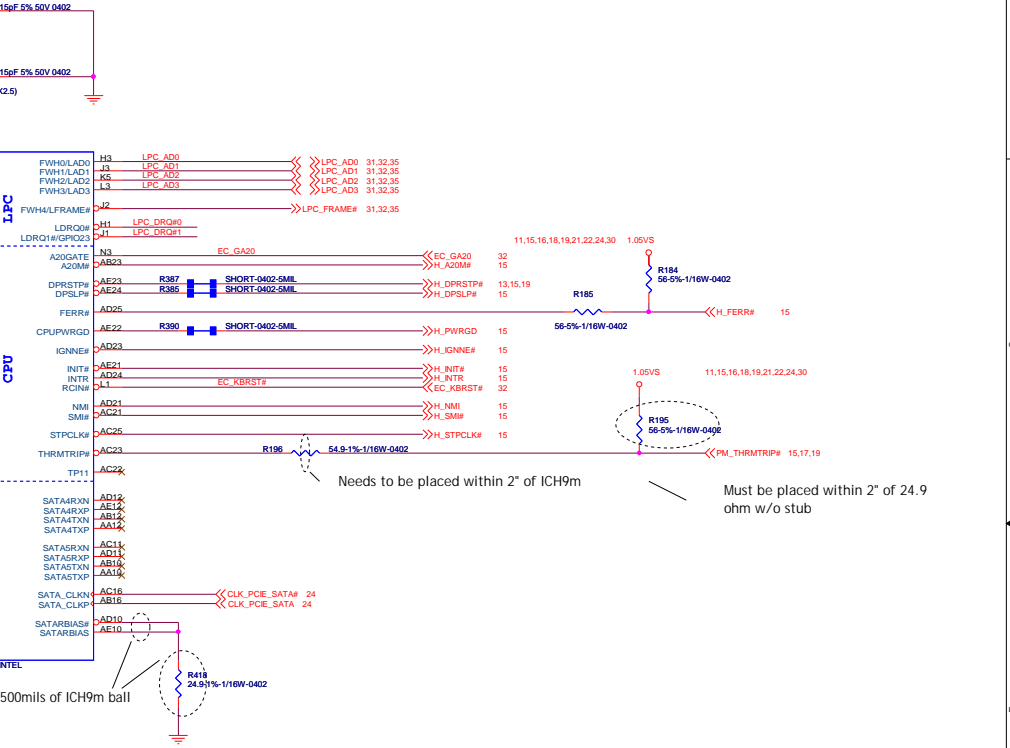
ACZ\_SDATAOUT strap functionality base on RSVD9 strap  
XOR chain entrance (RSVD9 pulled low)  
PCIe port config bit 1 (RSVD9 not pulled low)

Stuff for XOR chain testing

Chip	Pin	Mode	Description
0	0	0	Normal Operation
0	1	1	Enter XOR Chain
1	0	0	Normal Operation (Default)
1	1	1	Enter XOR Chain

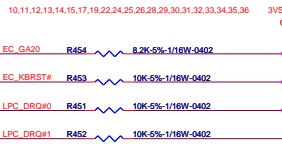


By Tony



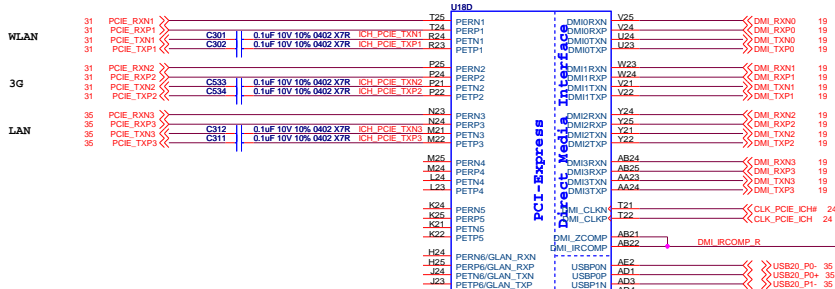
Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9 ohm w/o stub



**INVENTEC**  
 TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF  
 ICH9M CPU/DE/SATA(1/4)  
 Size: Custom | Code: D-CS-1310A2264501-ALG | Rev: X01  
 SHEET: 27 of 38

PCIe AC coupling caps need to be within 250mils of the driver



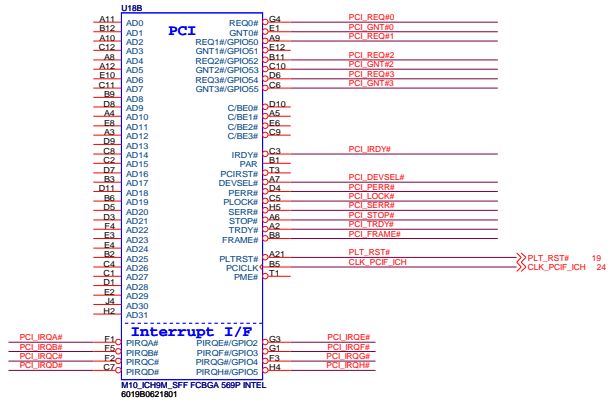
STUFF for ITPM enable



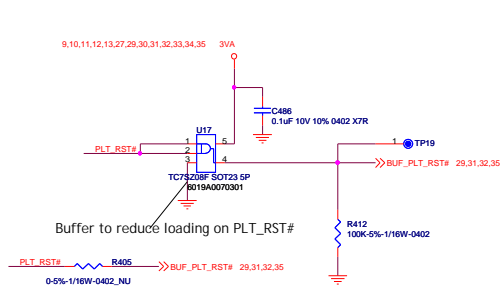
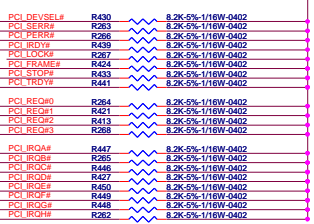
By Tony

Place within 500mils of ICH

Place within 500mils of ICH  
5/5 mils spacing on microstrip



PCI Pull up

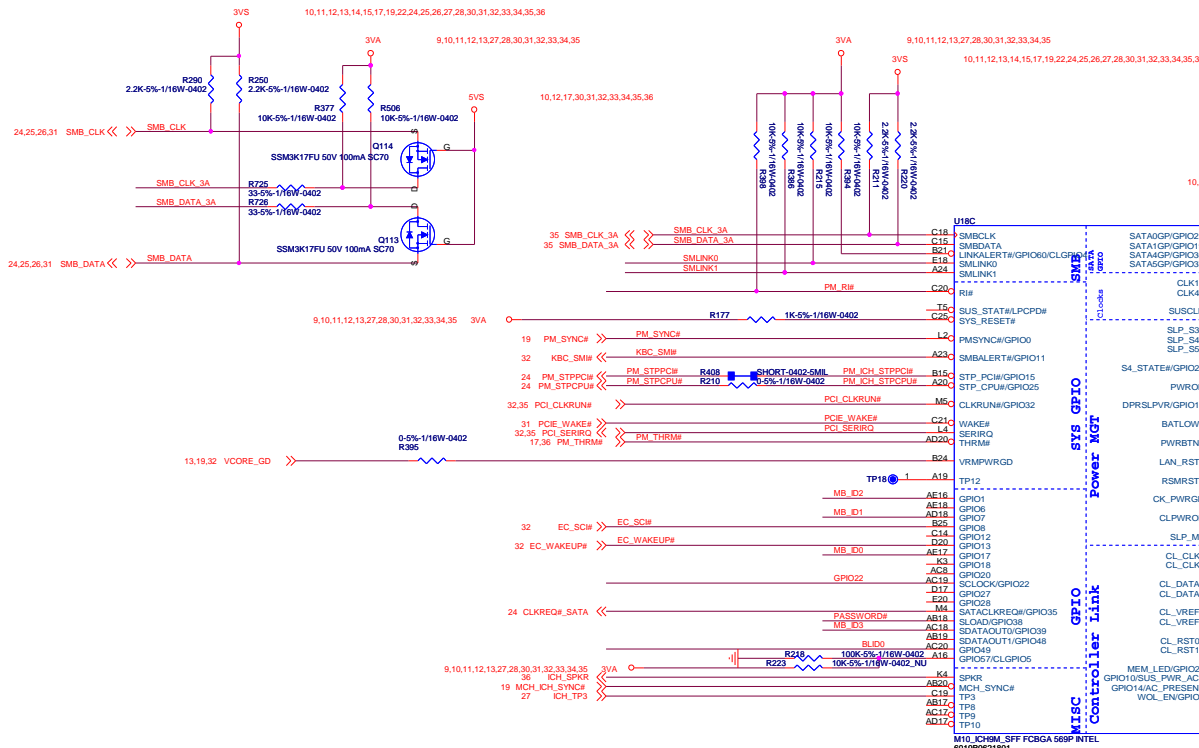


PCI\_GNT#3 No stuff : by default  
Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

**INVENTEC**  
 TITLE: BAP31 (Penryn+Cntiga+ICH9M)SFF  
 ICH9M PCI/PCIE/DMI/USB(24)  
 SIZE: Custom CODE: 201 DOCNUMBER: D-CS-1310A228491-ALG\_REV: 201  
 CHANGE BY: Miles Lu DATE: Tuesday, March 10, 2009 SHEET: 29 of 36

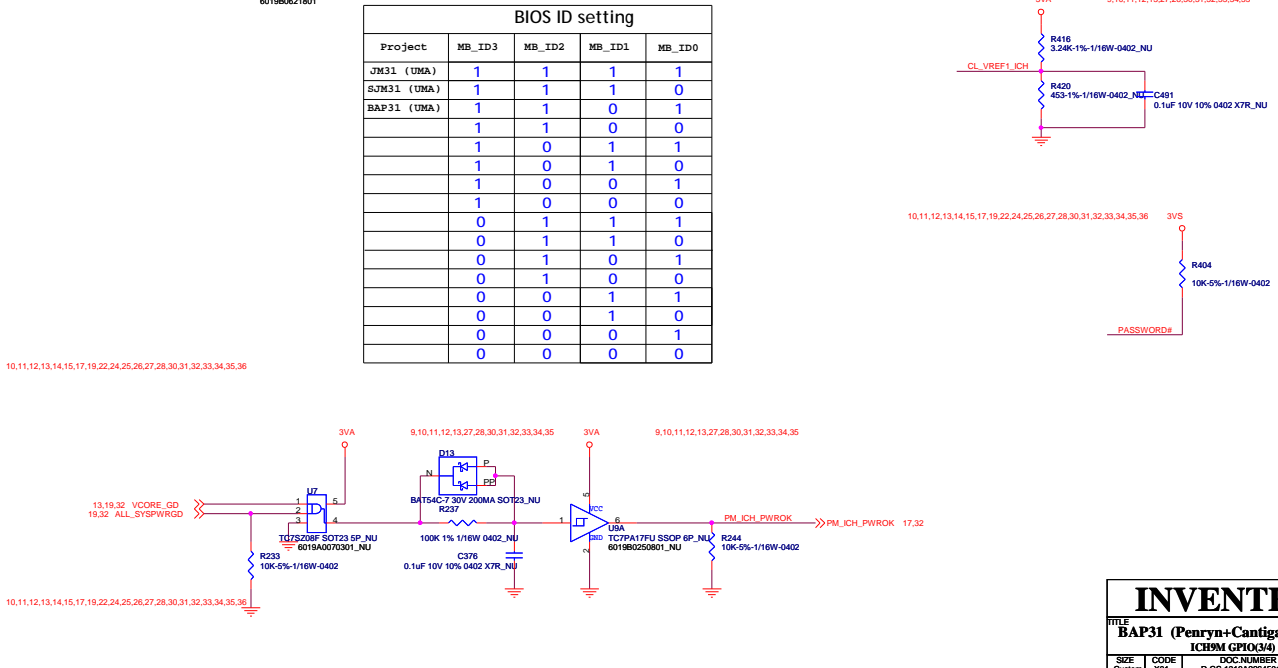
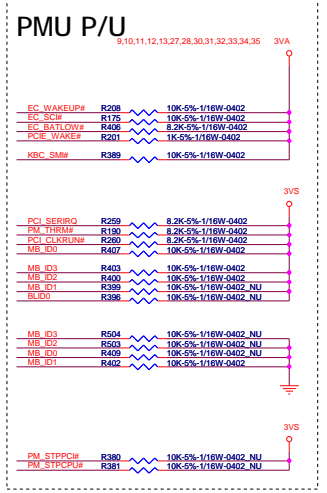
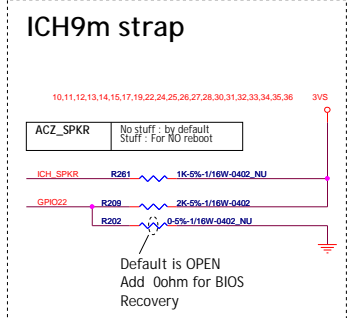


SUSCLK duty cycle can be between 30% and 70%

RSMRST# should go high no sooner than 10ms after both Vccsus3\_3 and Vccsus1\_5 have reached their nominal voltage  
Rise edge : 1-2us  
1CH9m Spec : less 50us

BIOS ID setting

Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	0	1
	1	0	1	0
	0	1	1	1
	0	1	0	1
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0



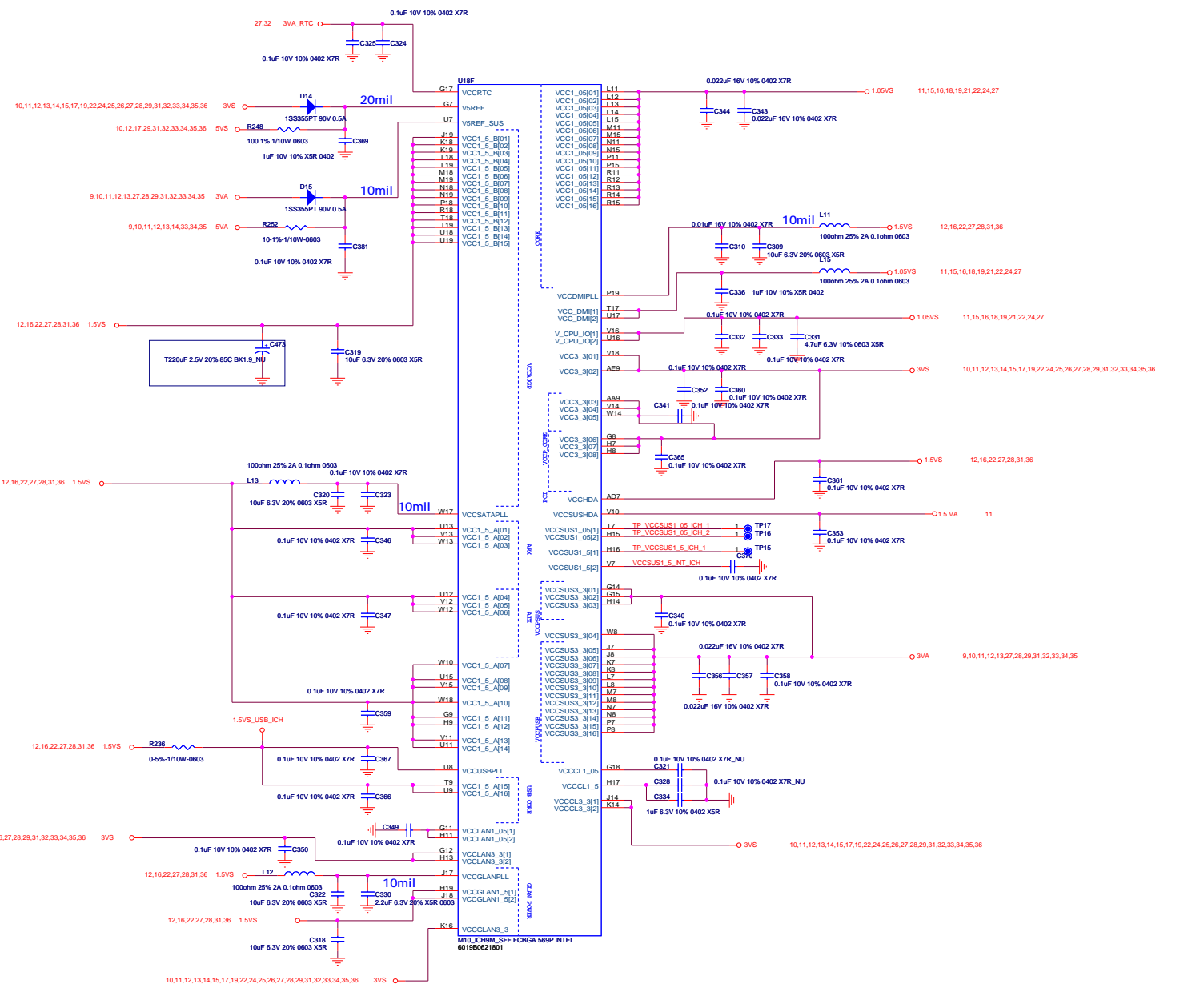
**INVENTEC**

TITLE: BAP31 (Penryn+Contiga+ICH9M)SFF  
ICH9M GPIO(3/4)

SIZE: Custom X01  
CODE: X01  
SHEET: 29 of 38

DOC NUMBER: D-CS-1310A284501.ALG  
REV: X01

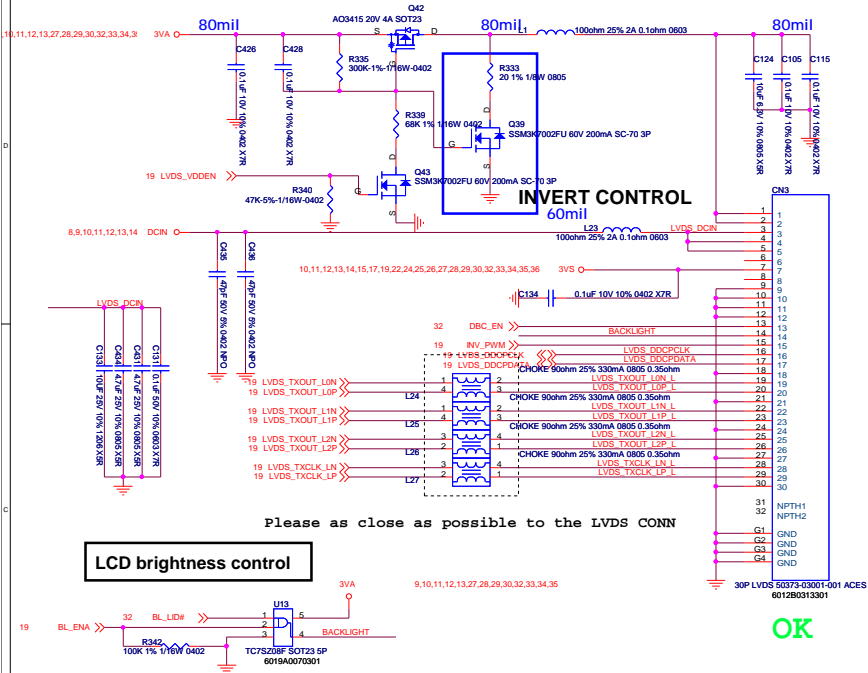
CHANGE by: Milon Liu DATE: Tuesday, March 10, 2009



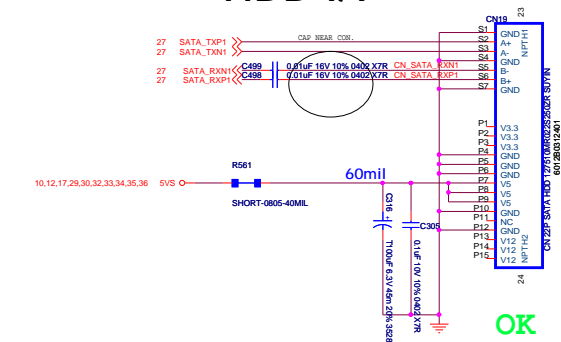
LIBE	LIBE	LIBE
B4	VSS1001	VSS1007
B7	VSS1002	VSS1008
B10	VSS1003	VSS1009
B13	VSS1004	VSS1100
B16	VSS1005	VSS1101
B19	VSS1006	VSS1102
B22	VSS1007	VSS1103
D2	VSS1008	VSS1104
D24	VSS1009	VSS1105
E5	VSS1010	VSS1106
E7	VSS1011	VSS1107
E9	VSS1012	VSS1108
E11	VSS1013	VSS1109
E13	VSS1014	VSS1200
E15	VSS1015	VSS1201
E17	VSS1016	VSS1202
E19	VSS1017	VSS1203
E21	VSS1018	VSS1204
E23	VSS1019	VSS1205
G6	VSS1020	VSS1206
G10	VSS1021	VSS1207
G12	VSS1022	VSS1208
G14	VSS1023	VSS1209
G16	VSS1024	VSS1210
G18	VSS1025	VSS1300
G20	VSS1026	VSS1301
G22	VSS1027	VSS1302
H10	VSS1028	VSS1303
H12	VSS1029	VSS1304
H20	VSS1030	VSS1305
H22	VSS1031	VSS1306
J5	VSS1032	VSS1307
J6	VSS1033	VSS1308
J10	VSS1034	VSS1309
J12	VSS1035	VSS1310
J14	VSS1036	VSS1311
J16	VSS1037	VSS1312
J20	VSS1038	VSS1313
J22	VSS1039	VSS1314
J24	VSS1040	VSS1315
K2	VSS1041	VSS1316
K6	VSS1042	VSS1317
K10	VSS1043	VSS1318
K12	VSS1044	VSS1319
K14	VSS1045	VSS1320
K16	VSS1046	VSS1321
K18	VSS1047	VSS1322
K20	VSS1048	VSS1323
L2	VSS1049	VSS1324
L4	VSS1050	VSS1325
L6	VSS1051	VSS1326
L10	VSS1052	VSS1327
L12	VSS1053	VSS1328
L14	VSS1054	VSS1329
L16	VSS1055	VSS1330
L20	VSS1056	VSS1331
L22	VSS1057	VSS1332
M2	VSS1058	VSS1333
M6	VSS1059	VSS1334
M10	VSS1060	VSS1335
M12	VSS1061	VSS1336
M14	VSS1062	VSS1337
M16	VSS1063	VSS1338
M20	VSS1064	VSS1339
M22	VSS1065	VSS1340
N2	VSS1066	VSS1341
N6	VSS1067	VSS1342
N10	VSS1068	VSS1343
N12	VSS1069	VSS1344
N14	VSS1070	VSS1345
N16	VSS1071	VSS1346
N18	VSS1072	VSS1347
N20	VSS1073	VSS1348
N22	VSS1074	VSS1349
N24	VSS1075	VSS1350
N26	VSS1076	VSS1351
P2	VSS1077	VSS1352
P6	VSS1078	VSS1353
P10	VSS1079	VSS1354
P12	VSS1080	VSS1355
P14	VSS1081	VSS1356
P16	VSS1082	VSS1357
P18	VSS1083	VSS1358
P20	VSS1084	VSS1359
R2	VSS1085	VSS1360
R6	VSS1086	VSS1361
R10	VSS1087	VSS1362
R12	VSS1088	VSS1363
R14	VSS1089	VSS1364
R16	VSS1090	VSS1365
R18	VSS1091	VSS1366
R20	VSS1092	VSS1367
R22	VSS1093	VSS1368
R24	VSS1094	VSS1369
R26	VSS1095	VSS1370
R28	VSS1096	VSS1371
T2	VSS1097	VSS1372
T6	VSS1098	VSS1373
T10	VSS1099	VSS1374
T12	VSS1100	VSS1375
T14	VSS1101	VSS1376
T16	VSS1102	VSS1377
T18	VSS1103	VSS1378
T20	VSS1104	VSS1379
T22	VSS1105	VSS1380
T24	VSS1106	VSS1381
VSS_NCTF01	VSS_NCTF01	A1
VSS_NCTF02	VSS_NCTF02	A2
VSS_NCTF03	VSS_NCTF03	A3
VSS_NCTF04	VSS_NCTF04	A25

**INVENTEC**  
 TITLE BAP31 (Penryn+Contiga+ICH9M)SFF  
 ICBM Power/GND(4)  
 SIZE Custom X01  
 DOC NUMBER D-CS-1310A284501.ALG  
 REV 1  
 SHEET 30 of 36

### LVDS Interface

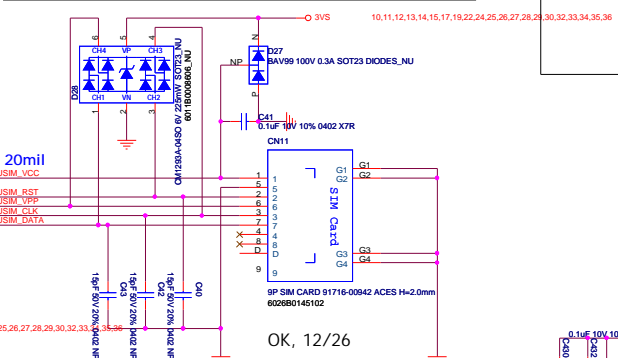


### HDD I/F

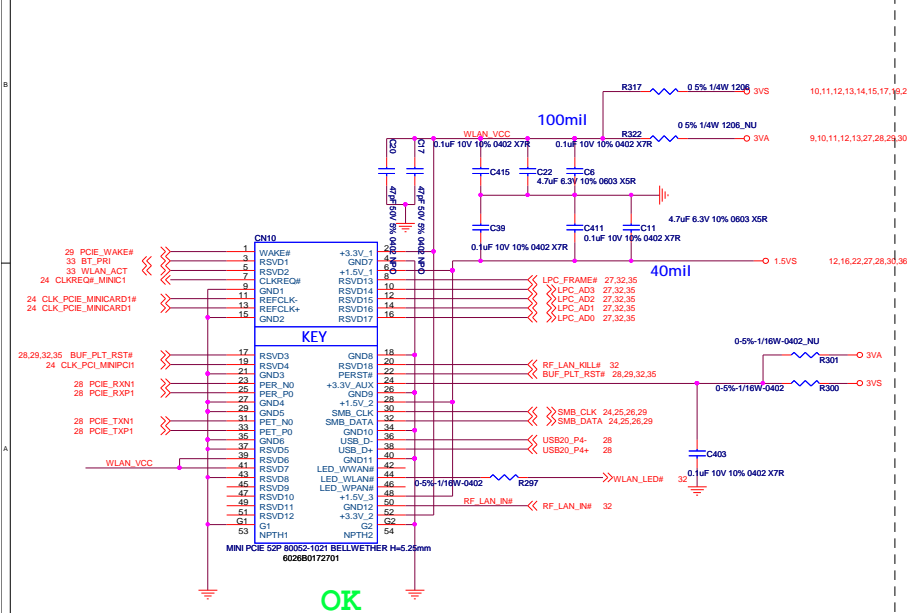


### SIM CARD slot

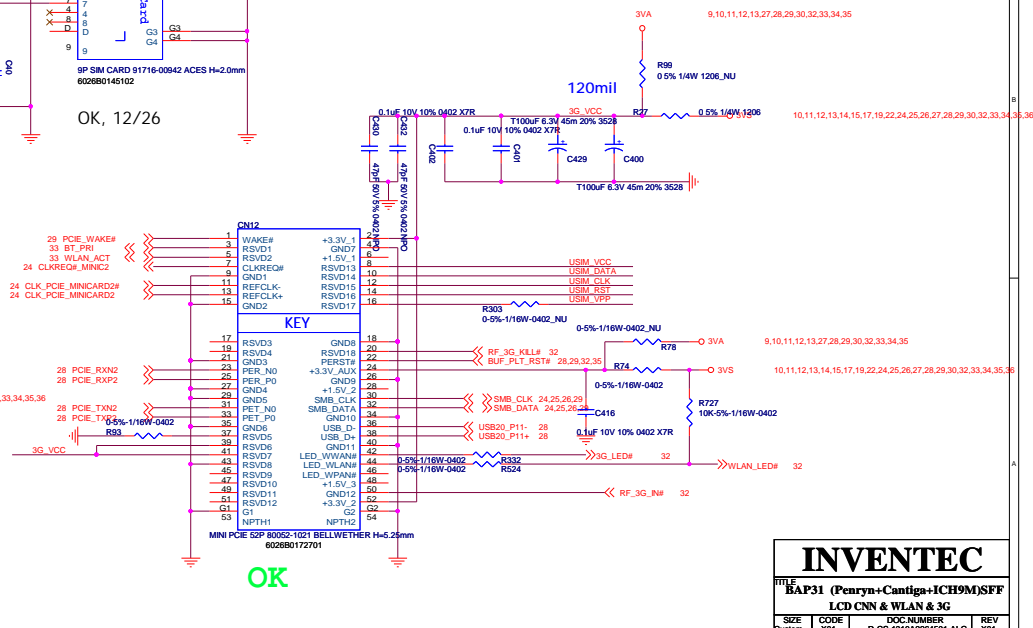
On Chip 5V to 3.3V regulator. No external regulator required  
On-Chip power MOSFETs for supplying flash media card power.



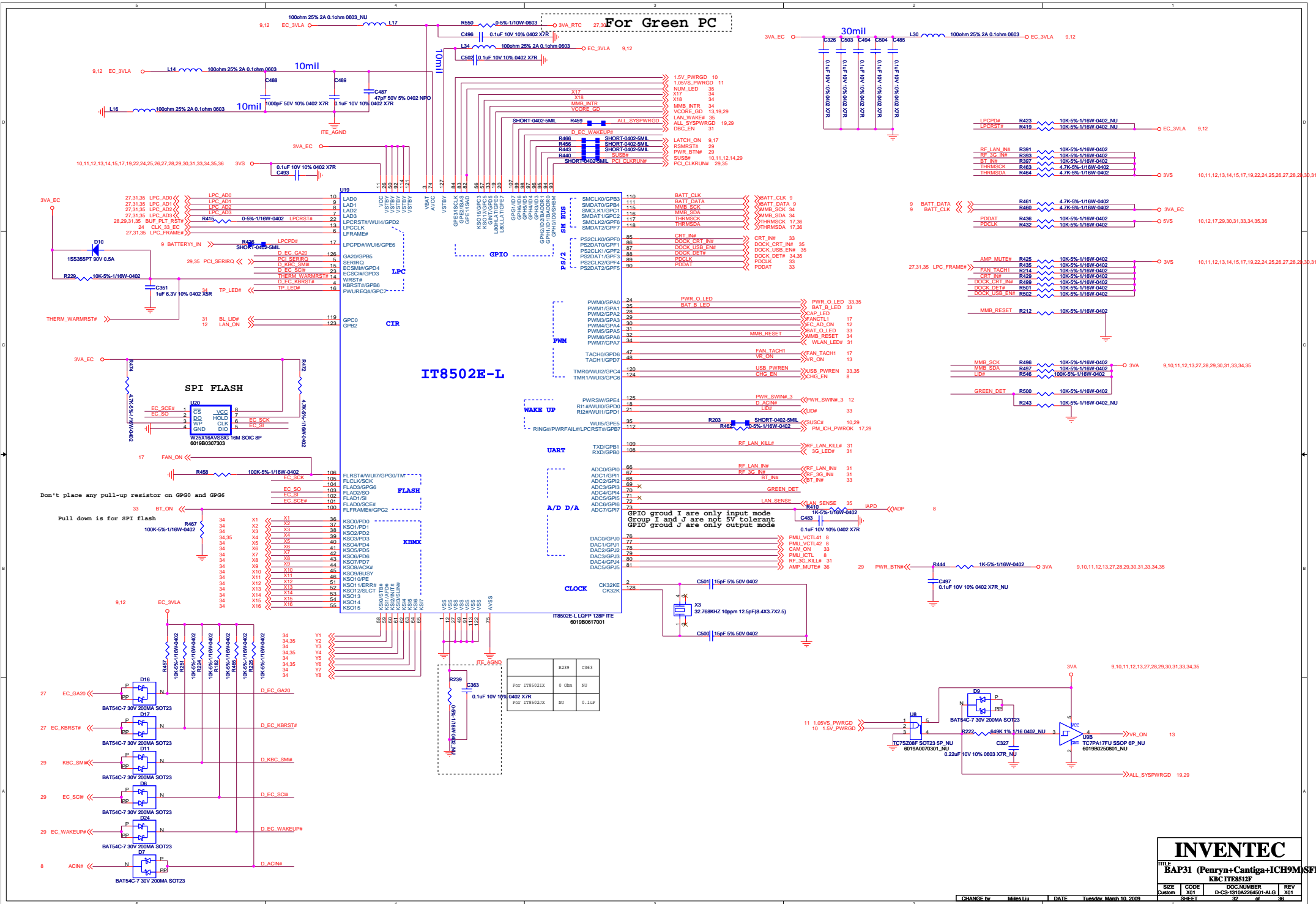
### PCIE Mini Card(WLAN)



### PCIE Mini Card for 3G

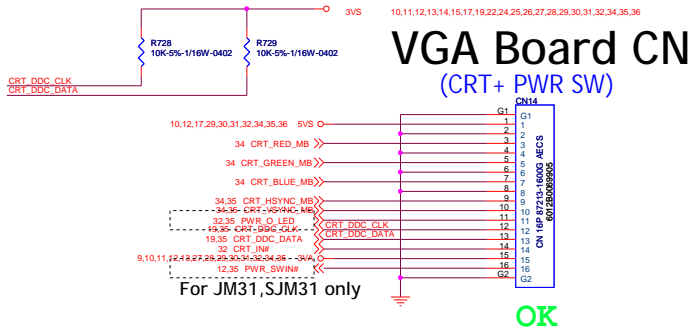


**INVENTEC**  
 TITLE: BAP31 (Penryn+Centiga+ICH9M)SFF  
 LCD CNN & WLAN & 3G  
 SIZE: Custom  
 CODE: X01  
 SHEET: 31 of 36

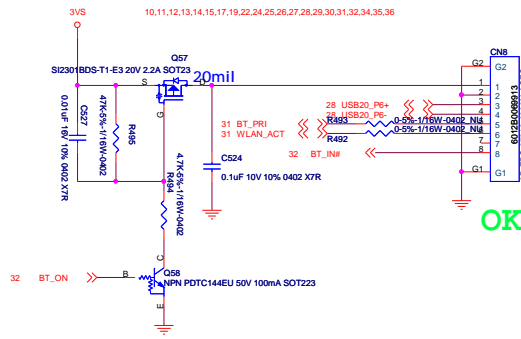


<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Contiga+ICH9M)SF			
KBC IT8512F			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
CHANGE by	Miller Liu	DATE	Tuesday, March 10, 2009
		SHEET	32 of 36

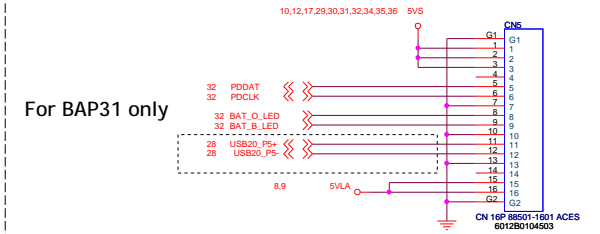




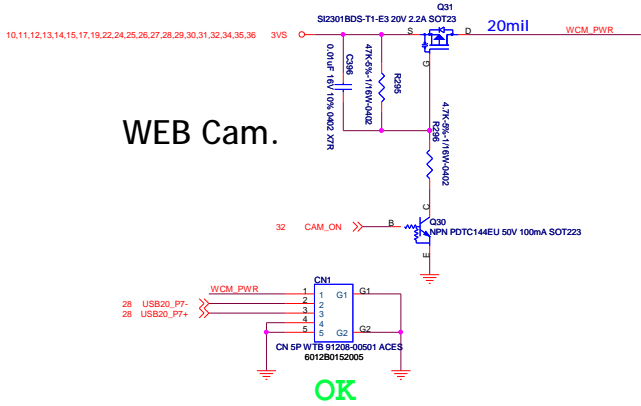
## Bluetooth CON.



## GLIDE PAD Board

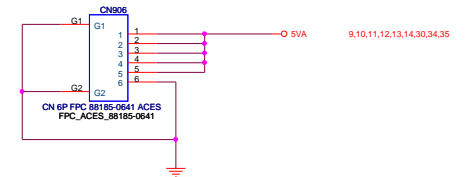
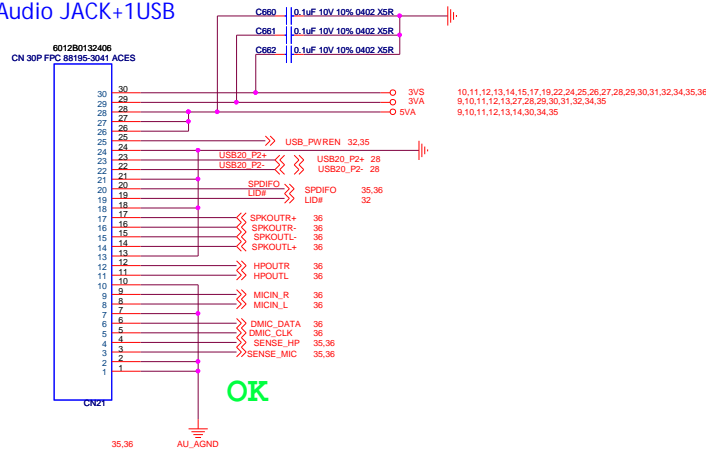


## WEB Cam.



## AUDIO Board CN

(Audio JACK+1USB)



**INVENTEC**

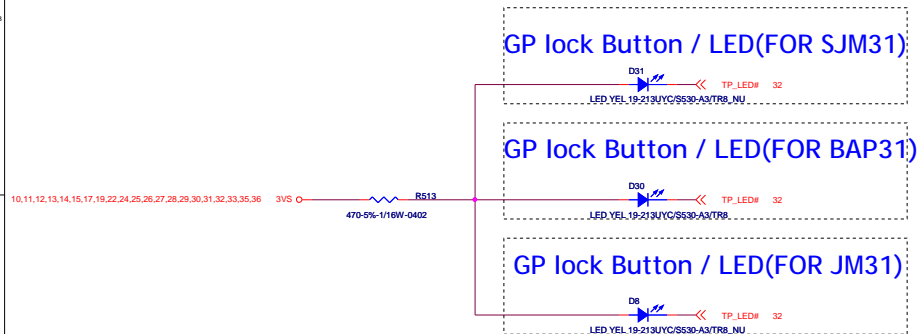
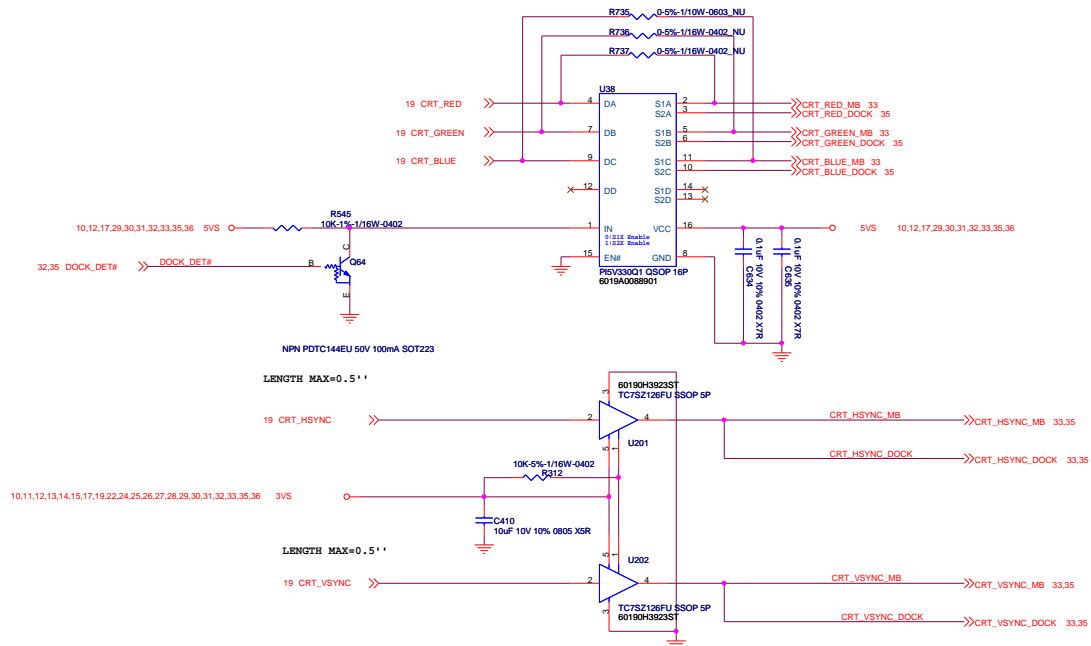
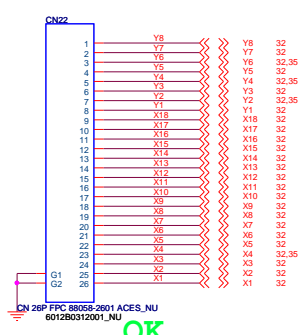
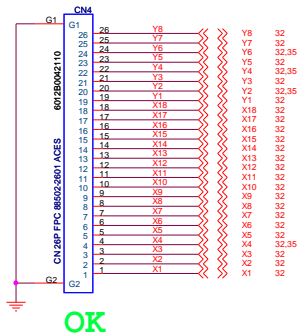
TITLE BAP31 (Penryn+Contiga+ICH9M)S1 Daughter Connector

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

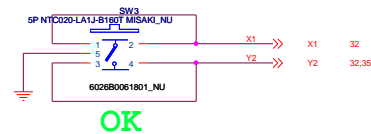
CHANGE by Milos Liu DATE Tuesday, March 10, 2009 SHEET 33 of 36

To K/B(For JM31,BAP31)

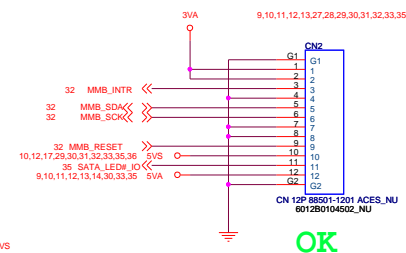
To K/B (For SJM31)



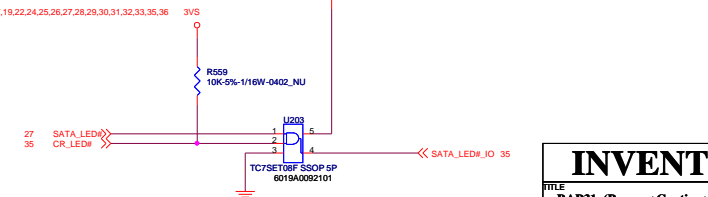
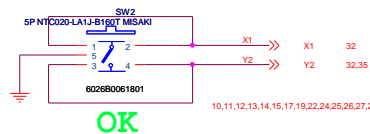
SW (FOR SJM31)



SW Sensor BOARD(For JM31,SJM31)

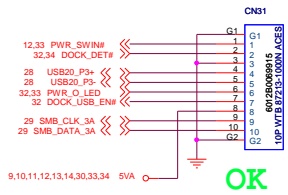


SW (FOR JM31,BAP31)



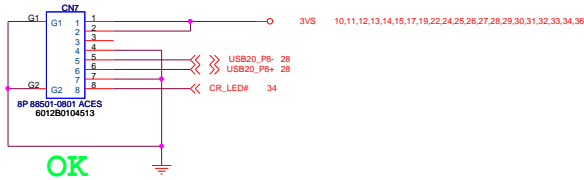
<b>INVENTEC</b>			
TITLE <b>BAP31 (Penryn+Cantiga+ICH9M)SFP</b>			
B3P			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A264501-ALG	X01
CHANGE by: Milin Liu			DATE: Tuesday, March 10, 2009
SHEET			34 of 36

# MB(USB) TO EASY/B



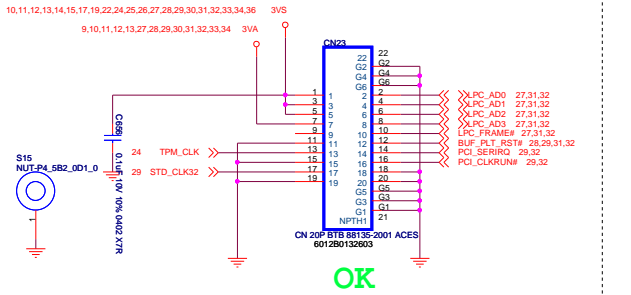
OK

# Card Reader BOARD CN



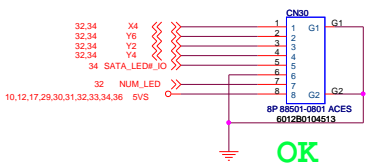
OK

# TPM CN



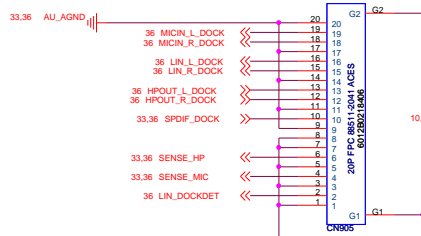
OK

# SW/B CN



OK

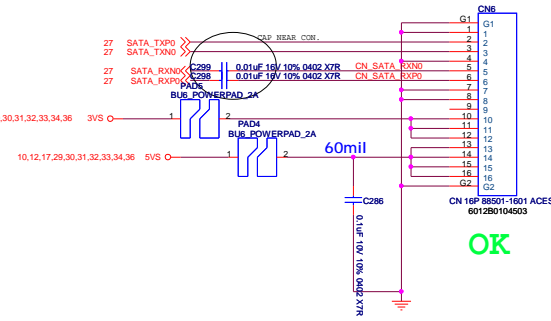
# MB(AUDIO) TO EASY/B(For BAP31)



OK

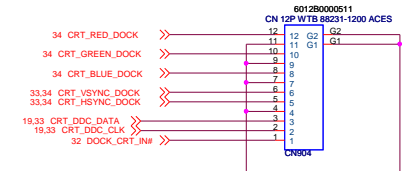
# For BAP31(EASY/B)

# SSD I/F

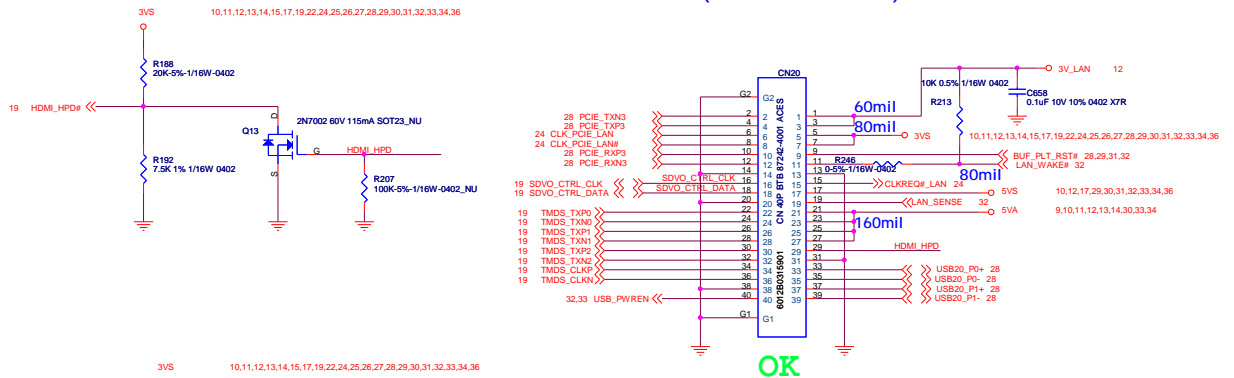


OK

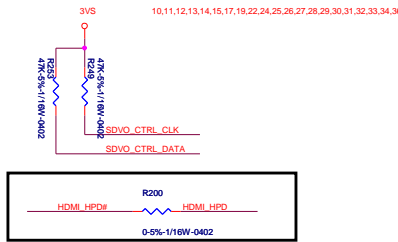
# MB(RGB) TO EASY/B



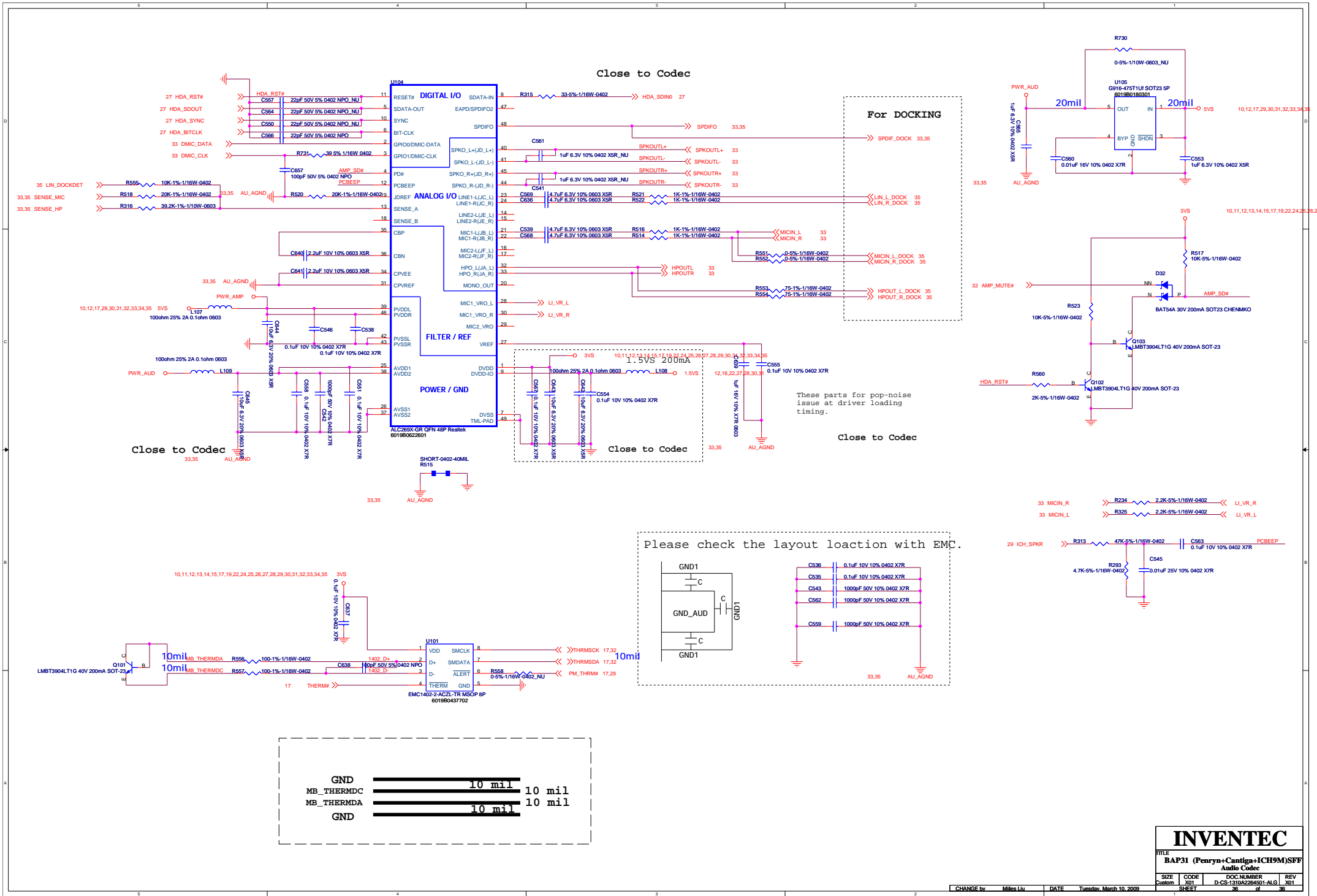
# USB Board CN (LAN+HDMI+2USB)



OK



<b>INVENTEC</b>			
TITLE BAP31 (Penryn+Centiga+ICH9M)SFP			
B3P			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A264501-ALG	X01
SHEET			36



GND	10 mil	10 mil
MB_THERMDC	10 mil	10 mil
MB_THERMDA	10 mil	10 mil
GND	10 mil	10 mil

**INVENTEC**

TITLE  
BAP31 (Penryn+Cantiga+ICH9M)SFP  
Audio Codec

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Milina Liu    DATE: Tuesday, March 10, 2009    SHEET: 36 of 36