

MODEL:	REV:	CHANGE LIST:	MODEL : ZL5 MB			
ZL5 MotherBoard	1A	FIRST RELEASE	PAGE	FROM	TO	
	2A	01. Page2 : Unstaff R202 for correct clock setting 02. Page3 : Delete JP2, Unstaff C561 and C559 ~ C562, C567 change P/N to CH6101M9A07 due to the height limitaion 03. Page5 : Change DDR MD terminator resistor array to 56ohm 4P2R type 04. Page9 : Change R20 to 6.2K, Unstaff C13 05. Page10 : Modify the CRT circuit due to the bad signal quality of CM2009 (Delete U1, Add D25, D28 ~ D32, Q35, Q36, R405, R404, R406, U31, U32) 06. Page11 : RN5, RN7, RN8, RN11, RN20, RN21 change P/N to CJ282084N01 07. Page12 : Modify the power good circuit (Delete D15, Add R402, R403) 08. Page16 : Modify the lan led circuit to fit to the right led color definition (R350, R353 change to pull high, Add D26, D27, CN3 change footprint) 09. Page17 : CN7, CN8 change footprint 10. Page19 : HOLE25 change to TOP layer 11. Page20 : Cancel the HOLD# ciruit (Unstaff R95, R111, D5, D7, Q17, Staff Q15, R99) 12. Page21 : SW2, SW3 change P/N to DHPPS11BD0 13. Page22 : Add PR123, PD16, PC149; PD13 change P/N to BC05FA20Z01; PU12 change P/N to AL001999W16 14. Page23 : PR63 change to 11K/F; PD15 change P/N to BC10QS04C01; Staff PC77 1000P 15. Page25 : PL8, PL9 change size to RC0805; PD8, PD9 change P/N to BC10QS04C01 16. Page26 : Unstaff PQ4; PR101, PR105 change P/N to CS31003B919; PU9 change P/N to AJ017720W06 17. Delete JP1, JP2 ~ JP6 18. U20 change P/N to AJ007600T25 19. L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L18, L24, L26, L27, L40, L43, L47, L48, L49, L50 change P/N to CX0QNT03004 20. PQ3, PQ4, PQ5, PQ6, PQ8, PQ9, PQ10, PQ12, PQ13, PQ14, PQ15, PQ16, PQ18, PQ24, PQ32, PQ33, PQ35, Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q11, Q26, Q27, Q34 change P/N to BAM70020074	1	3A	3B	
				2	3A	3B
				3	3A	3B
				4	3A	3B
				5	3A	3B
				6	3A	3B
				7	3A	3B
				8	3A	3B
				9	3A	3B
				10	3A	3B
				11	3A	3B
				12	3A	3B
				13	3A	3B
				14	3A	3B
				15	3A	3B
				16	3A	3B
				17	3A	3B
				18	3A	3B
				19	3A	3B
				20	3A	3B
		3A	01. Page2 : Staff R176 33ohm for 302ELV clock 02. Page4 : Staff C131, C175, C188, C189 03. Page9 : Staff R295(0ohm), R294 change P/N to CS00002JB03, Unstaff Y4, C31, C554 for 302ELV clock; Add C710 ~ C713, R407 ~ R410 for EMI reserved. 04. Page10 : D17 change p/n to BC05FA20Z01 to enlarge the current limit; L1 ~ L3 change p/n to CX808600101 for EMI 05. Page12 : C633, C634 change P/N to CH01806JB07 to adjust RTC accuracy; Add JP1 for RTC reset 06. Page15 : Add C709 07. Page17 : Unstaff CN8, CN10; Add C700 ~ C708 for EMI 08. Page19 : Delete HOLE18; Staff PAD4 for modem cable	21	3A	3B
				22	3A	3B
				23	3A	3B
				24	3A	3B
				25	3A	3B
			26	3A	3B	
	3B	01. Page17 : L36, R274, R279 change p/n to CX8HS121001; Staff R270, R273 100pF 02. Page18 : L54, L55 change p/n to CX8HS121001; Unstaff R260, R261, R265, R271, R278 03. Page19 : Staff PAD9(FDMK1004010) for EMI 04. Page22 : Unstaff PR112 for thermal shutdown working properly 05. Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q11, Q18, Q26, Q27, Q34, Q35, Q36, PQ3, PQ4, PQ5, PQ6, PQ8, PQ9, PQ10, PQ12, PQ13, PQ14, PQ15, PQ16, PQ18, PQ24, PQ32, PQ33, PQ35 change p/n to BAN70020Z13				



PROJECT : ZL5

APPROVE BY: SAINT LIN

DRAWING BY:DILBERT YU

REV 3B

COVER SHEET 1 OF 1

MB ASSY'S P/N : 31ZL5MB0009

PROJECT LEADER: SAINT LIN

DOCUMENT NO:

DATE :2005/3/9

ZL5 Block Diagram

CLK-GEN
ICS 952801
Page 2

- HOST 200MHz
- ZCLK 133MHz
- AGP 66MHz
- PCI 33MHz
- USB 48MHz
- REF 14.318MHz

3V/5V
Page 22

- 3V_ALWAYS
- 5VPCU
- 3V_S5
- 1.8V_S5
- 3VSUS
- 5VSUS
- +3V
- +5V
- 15V

2.5V/1.25V
Page 23

- 2.5VSUS
- 1.25VREF
- +2.5V
- DDR_VTT

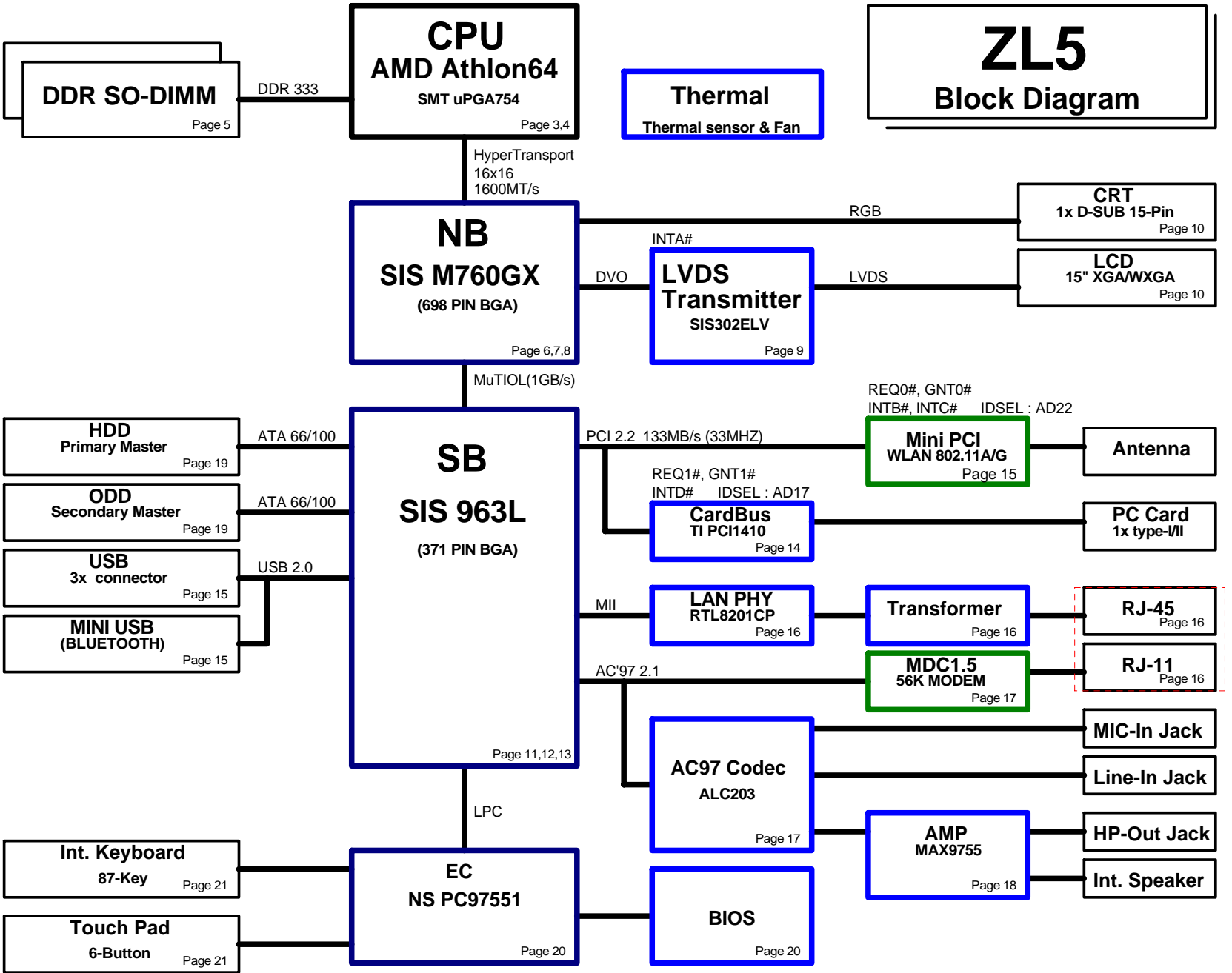
**1.2V/1.5V
1.8V**
Page 24

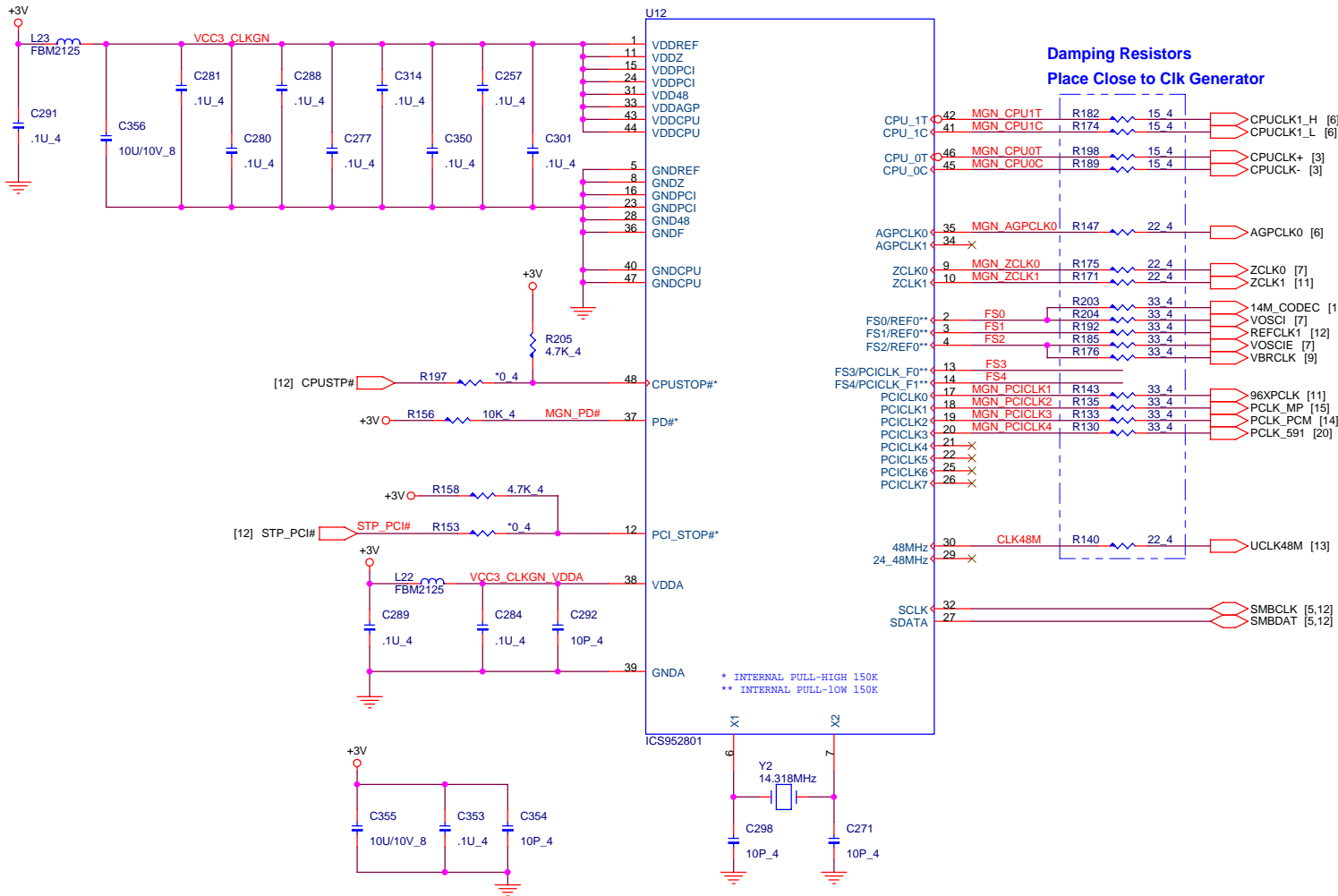
- +1.2V_HT
- +1.5V
- +1.8V

CPU CORE
Page 25

- VCC_CORE

BATTERY CHARGER
Page 26



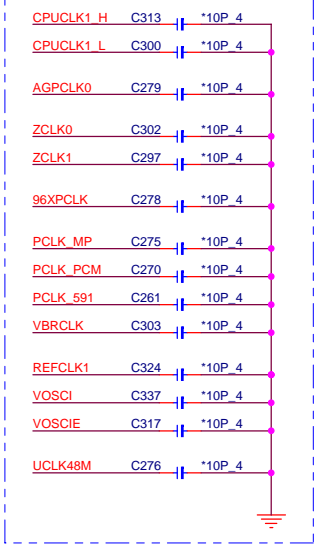


CLK Table for SiS M760 (Not For ICS ICS-952801)

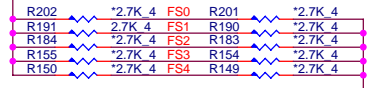
SiS 755/M760 CLOCK					CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)					
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

SiS 755/M760 CLOCK					CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)				
1	0	0	0	0	180	135	67.5	33.75
1	0	0	0	1	185	132.14	66.07	33.04
1	0	0	1	0	190	135.71	67.08	33.93
1	0	0	1	1	195	130	65	32.5
1	0	1	0	0	205	136.66	68.33	34.17
1	0	1	0	1	210	140	70	35
1	0	1	1	0	215	129	64.5	32.25
1	0	1	1	1	220	132	66	33
1	1	0	0	0	66.66	66.66	66.66	33.33
1	1	0	0	1	66.66	100	66.66	33.33
1	1	0	1	0	100	100	66.66	33.33
1	1	0	1	1	100	133.33	66.66	33.33
1	1	1	0	0	133	100	66.66	33.33
1	1	1	0	1	133	133.33	66.66	33.33
1	1	1	1	0	166	100	66.66	33.33
1	1	1	1	1	166	133.33	66.66	33.33

**By-Pass Capacitors
Place Close to Clock Generator**

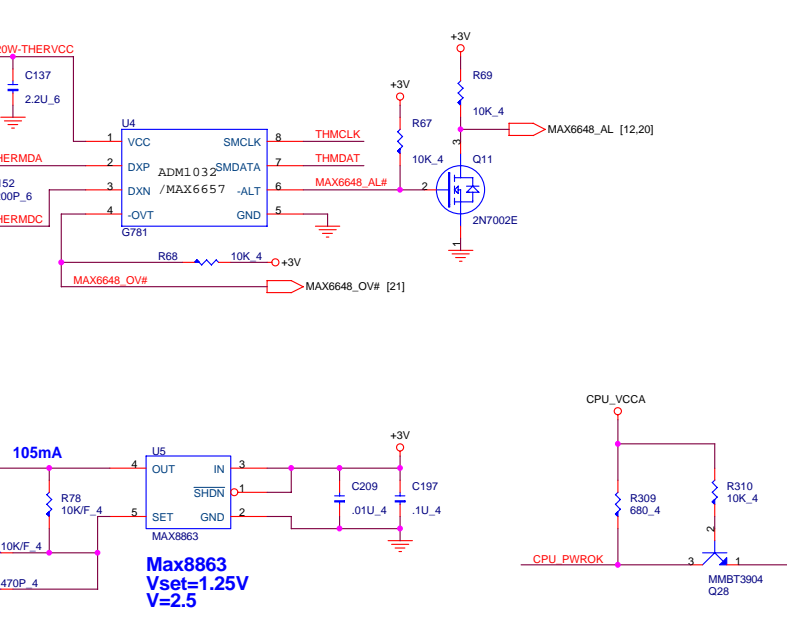
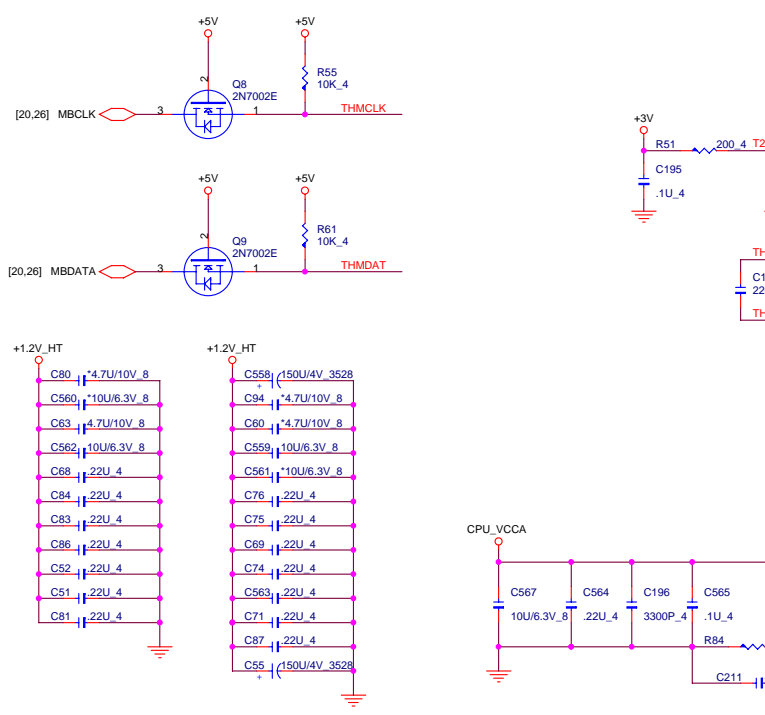
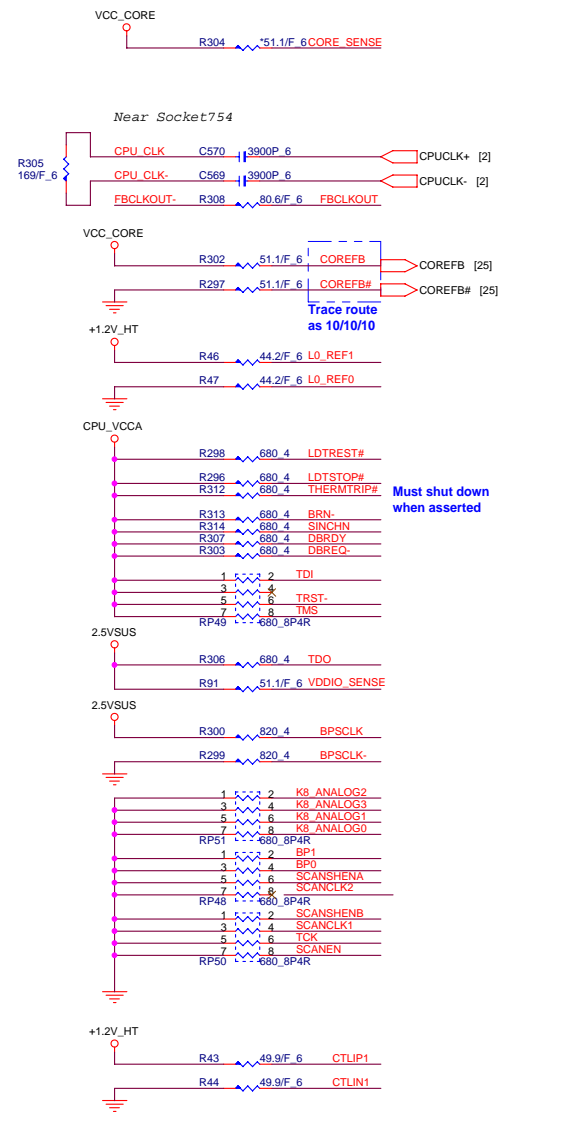
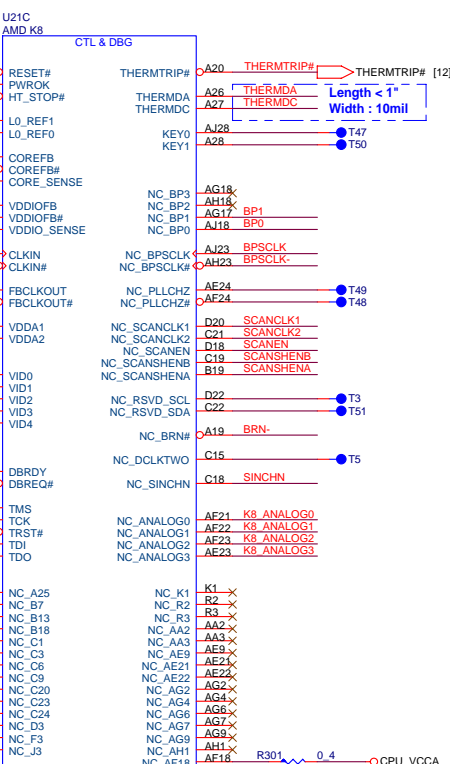
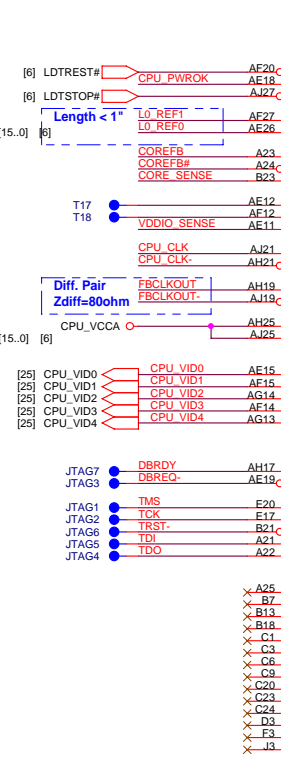
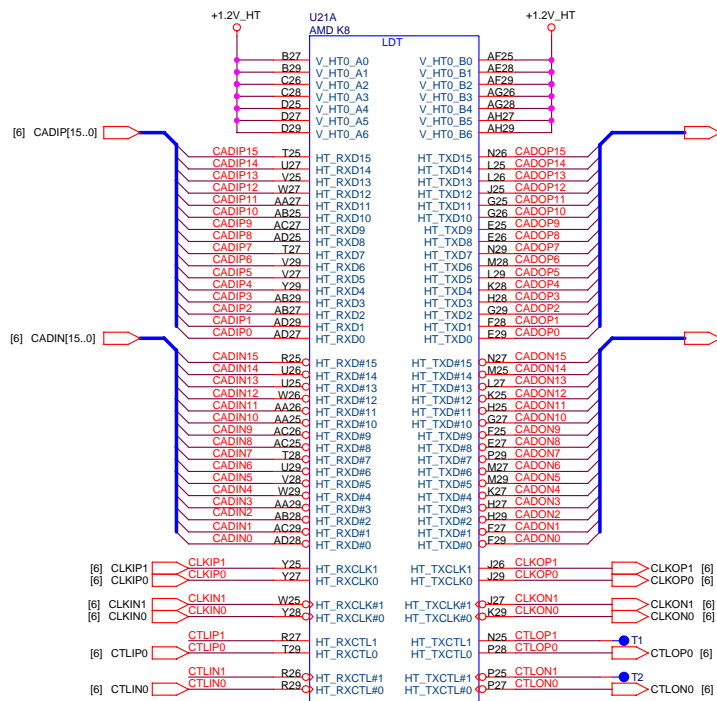


Frequency Selection

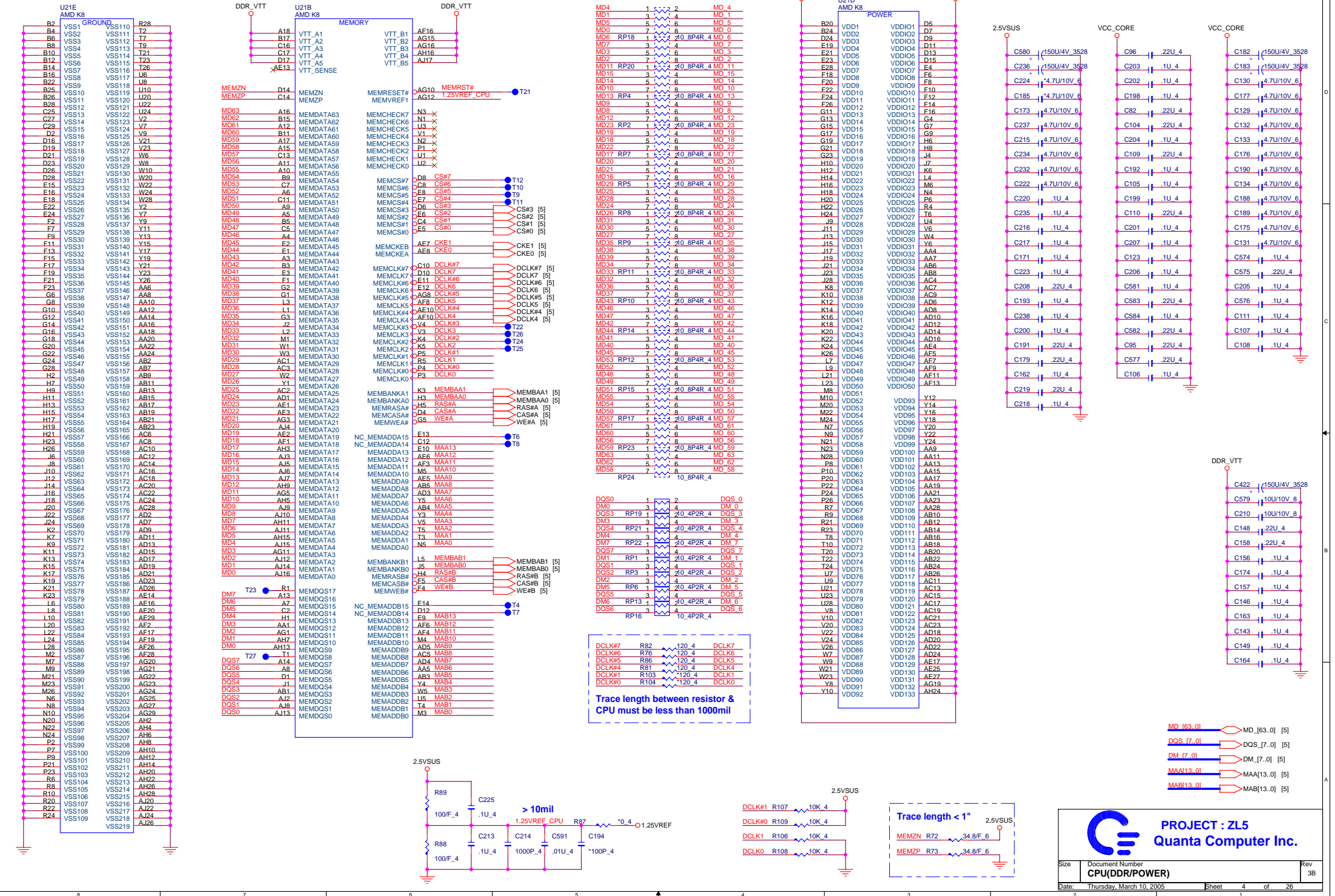


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
CLOCK GENERATOR		3B
Date:	Thursdays, March 10, 2005	Sheet 2 of 26



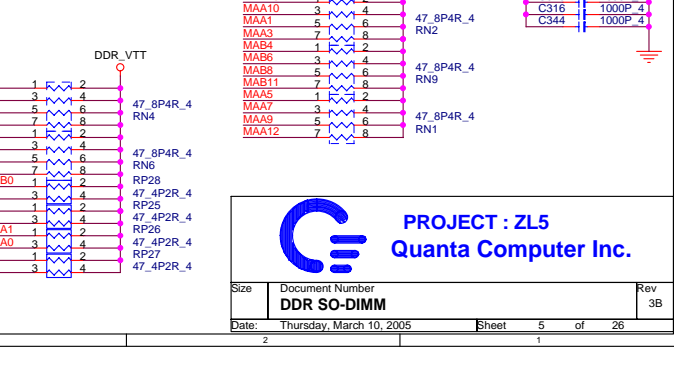
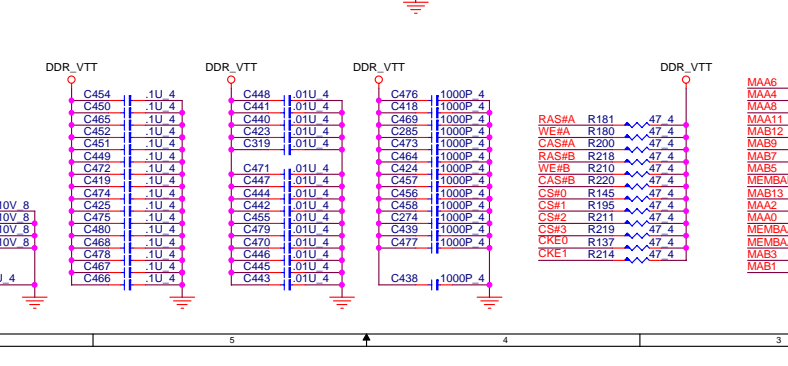
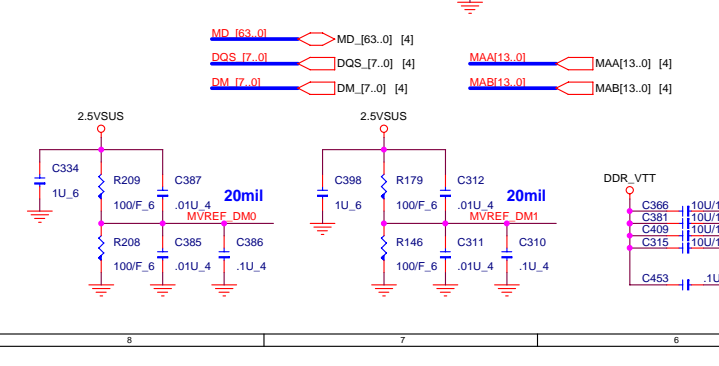
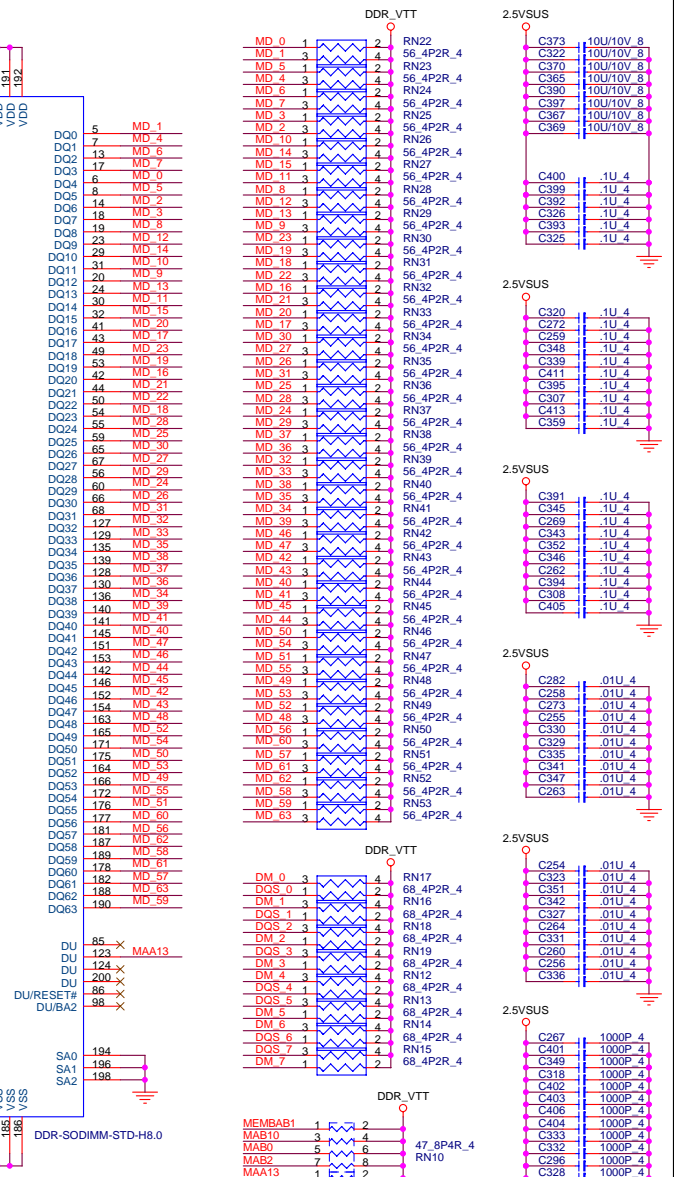
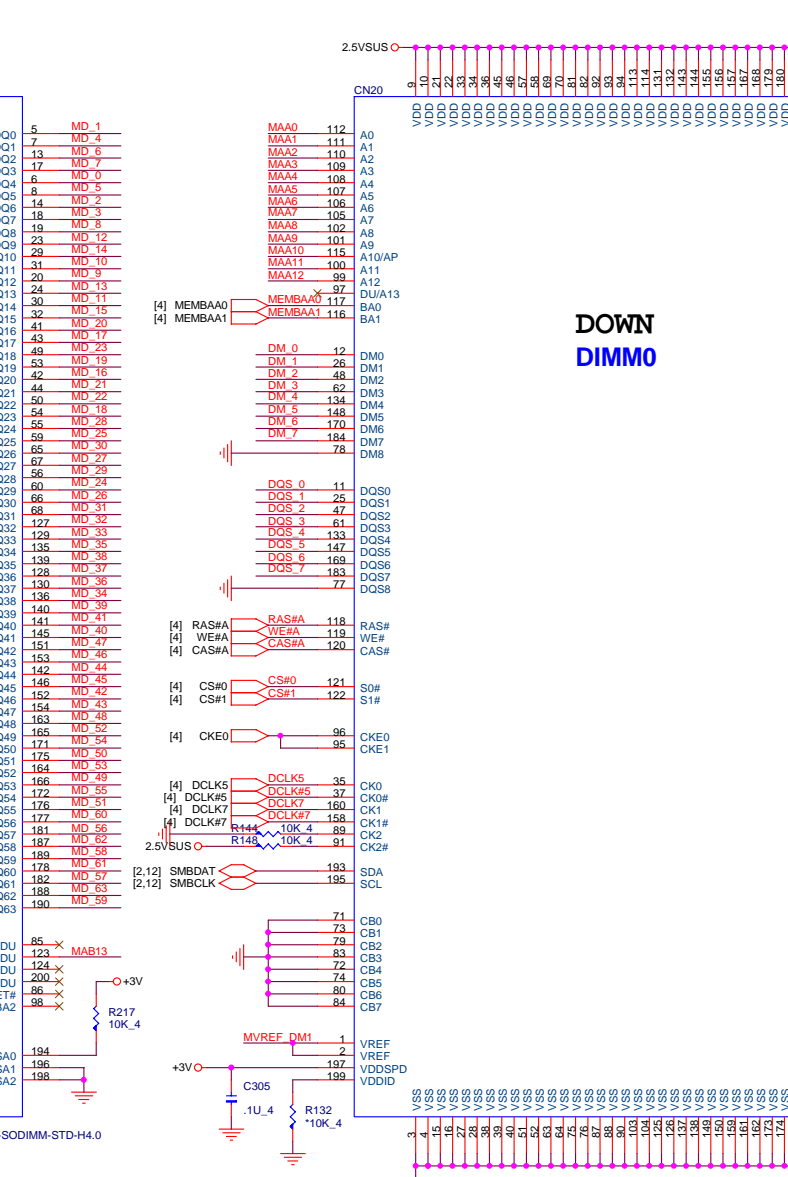
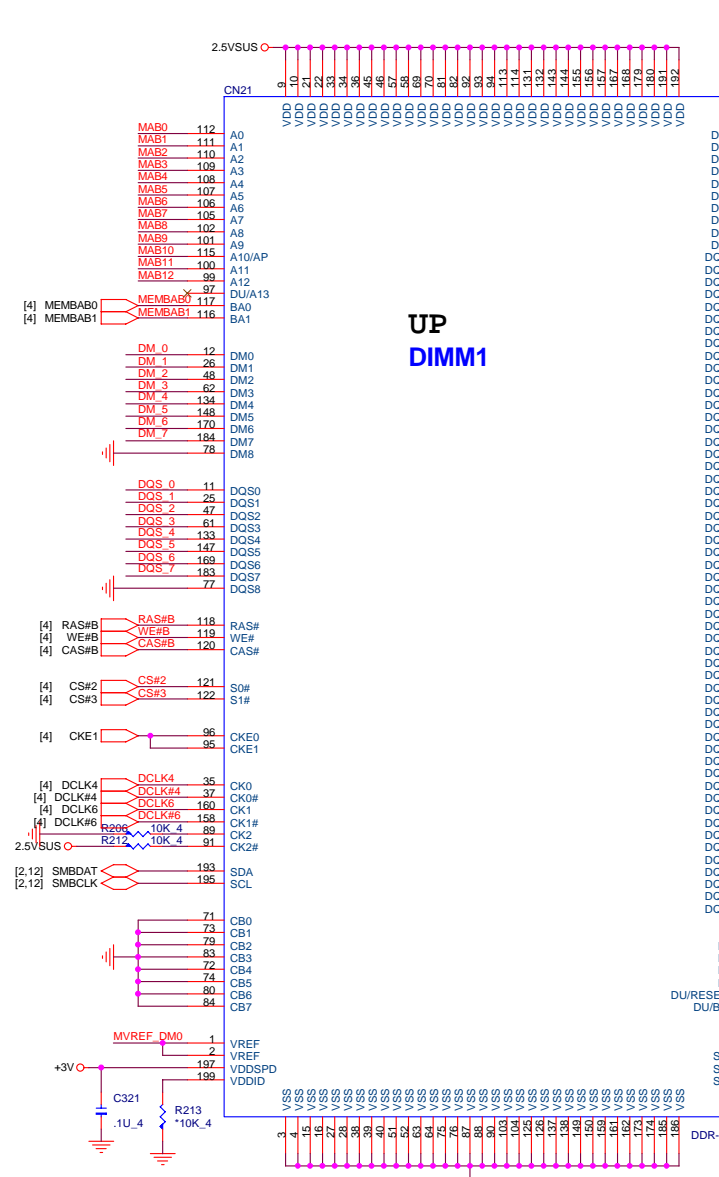
CPU DDR/POWER I/F

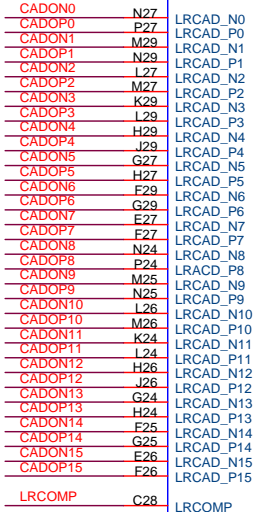
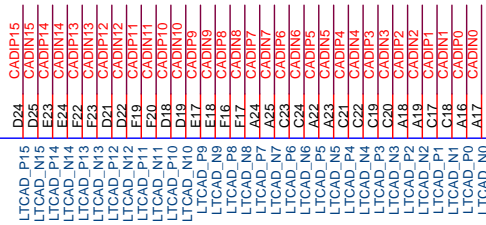


Trace length between resistor & CPU must be less than 1000mil

Trace length < 1"





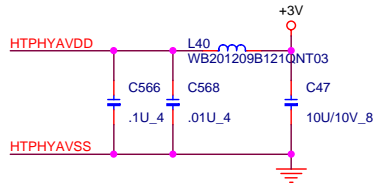
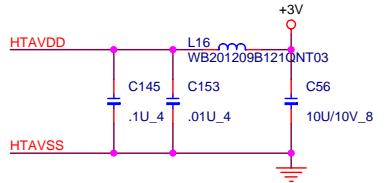
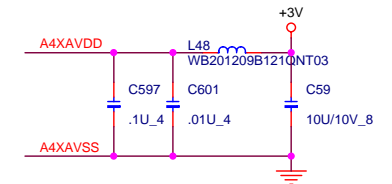
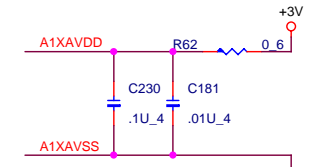
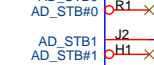
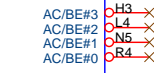
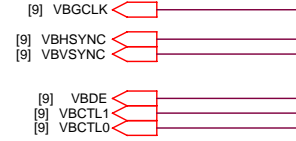
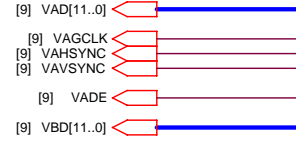
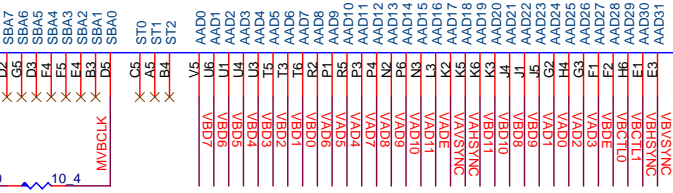
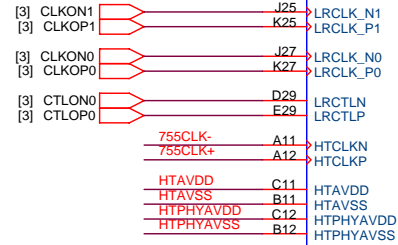


HOST_RX

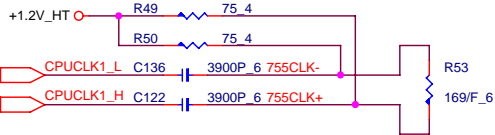
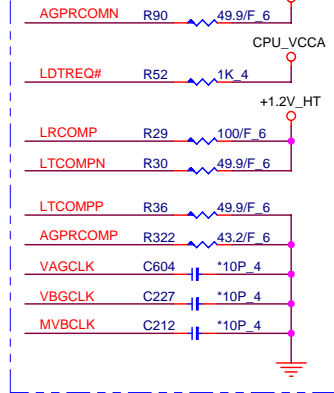
HOST_TX

M760-1

LVDS / AGP



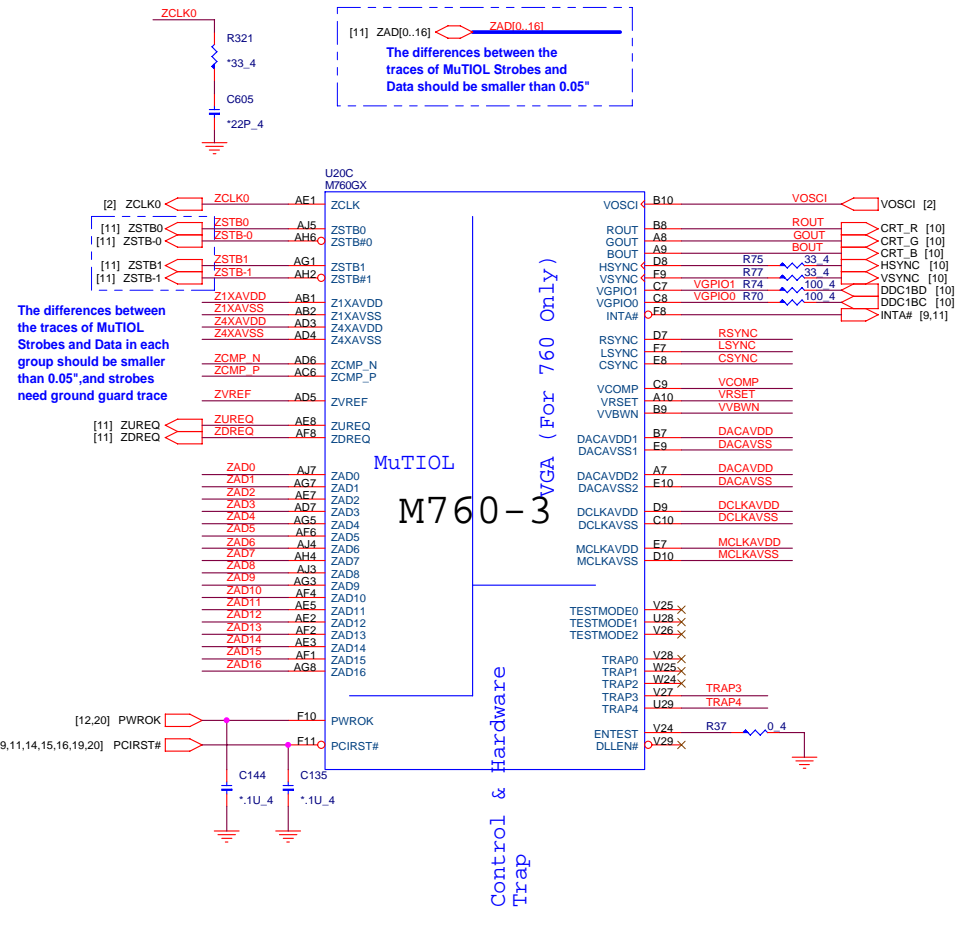
Place close to chip



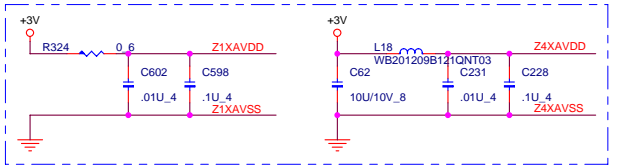
PROJECT : ZL5
 Quanta Computer Inc.

[11] ZAD[0..16] \leftrightarrow ZAD[0..16]

The differences between the traces of MuTIOL Strokes and Data should be smaller than 0.05"

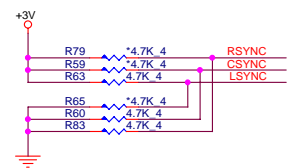


[9,11,14,15,16,19,20] PCIRST#

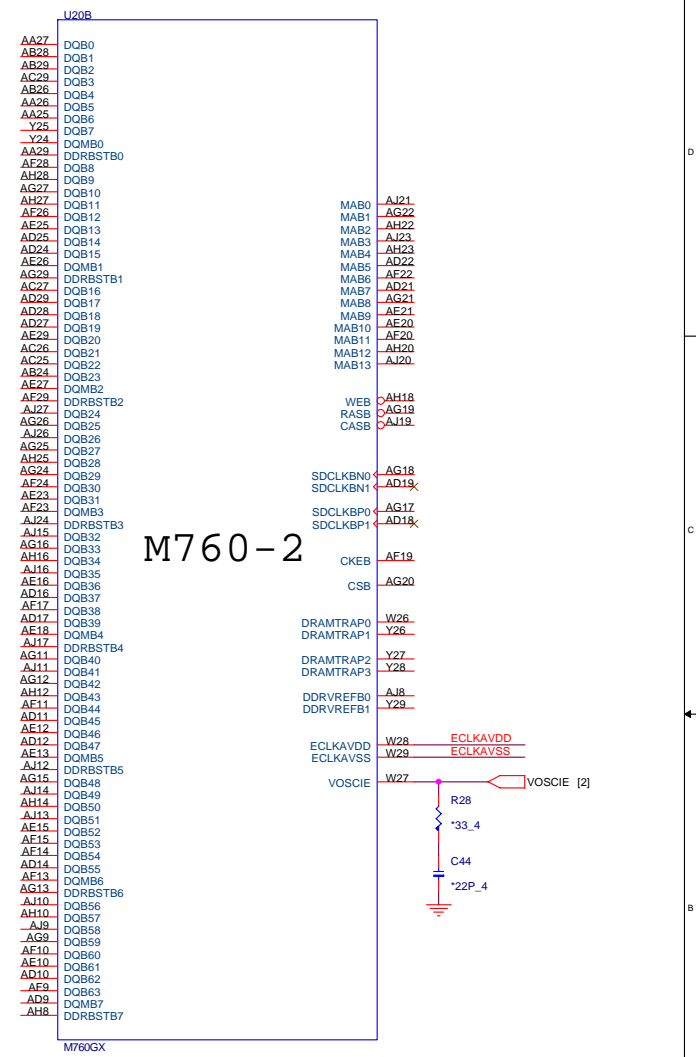
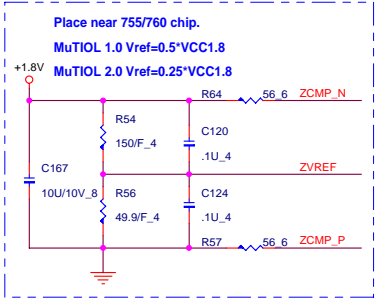
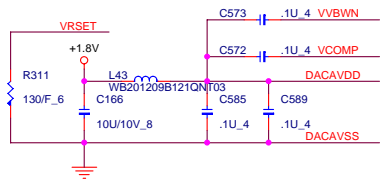
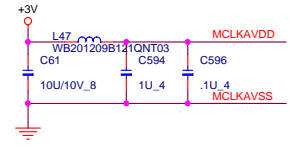
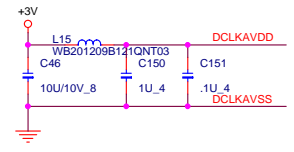


SIS755/760 NB Hardware Trap Table

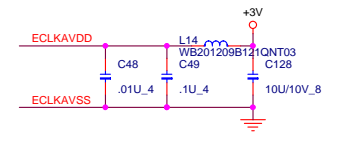
	755/760	ON/1	OFF/0	Internal	Default
DLLEN#	CPULCLK/ZCLK/AGPCLK PLL/DLL Circuit Enable	DISABLE	ENABLE	Pull Low	Low/0
TESTMODE0				Pull Low	
TESTMODE1	755 Test Mode Selection	1: Mode1	0: Mode0	Pull Low	
TESTMODE2	755 Test Mode Enable	ENABLE	DISABLE	Pull Low	Low/0
TRAP0	MuTIOL Verision 1, 2	Ver. 1	Ver. 2	Pull Low	Low/0
TRAP1	MuTIOL DBI Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP2	MuTIOLInitial Packet Series Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP3	Reserve			Pull Low	High/1
TRAP4	Reserve			Pull Low	High/1



NB Hardware Trap has internal pull-low in SIS M760 chip



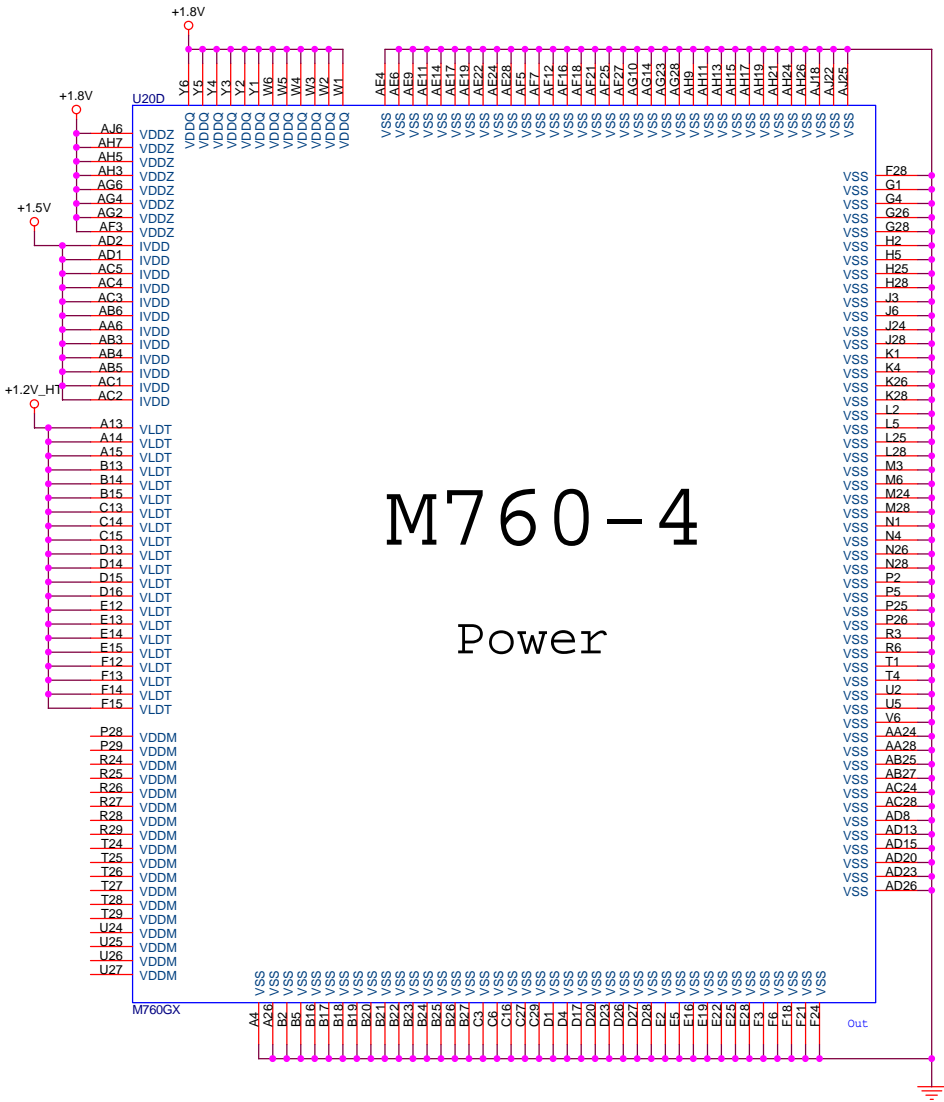
M760-2



PROJECT : ZL5
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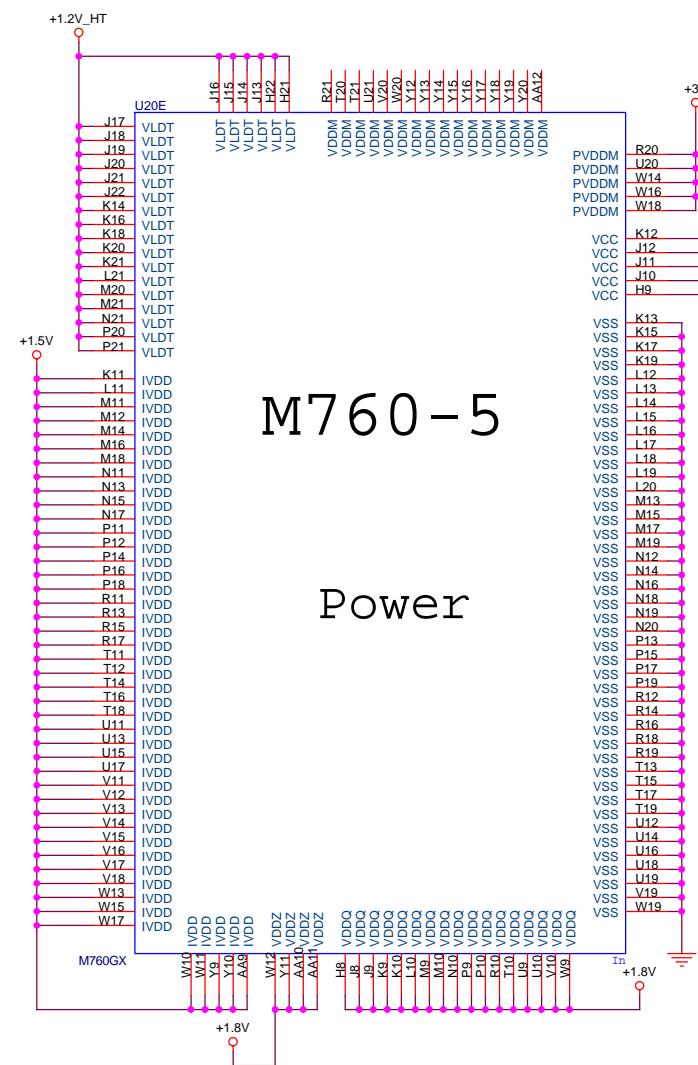
Size: Document Number
M760GX(MuTIOL/VGA)
Date: Thursday, March 10, 2005 Sheet 7 of 26 Rev 3B

If Support Sis M760LV IVDD=1.5V



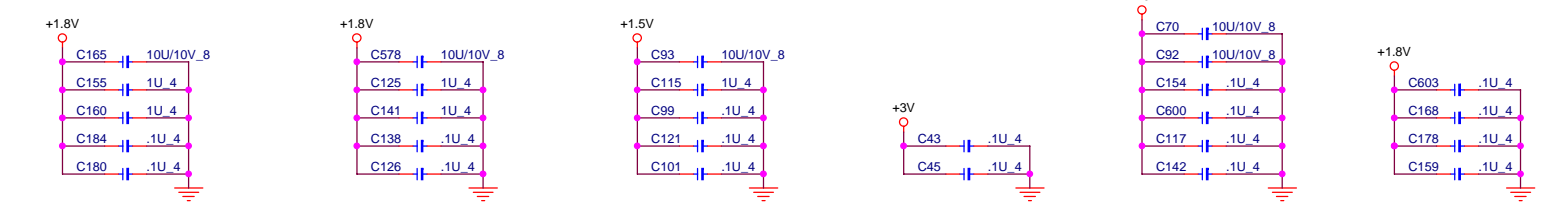
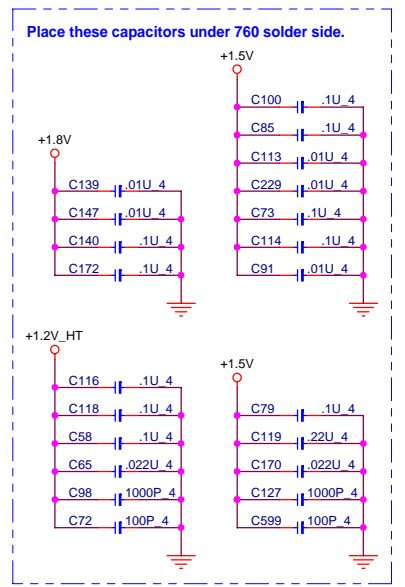
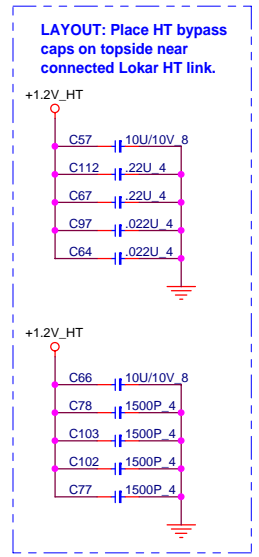
M760-4

Power



M760-5

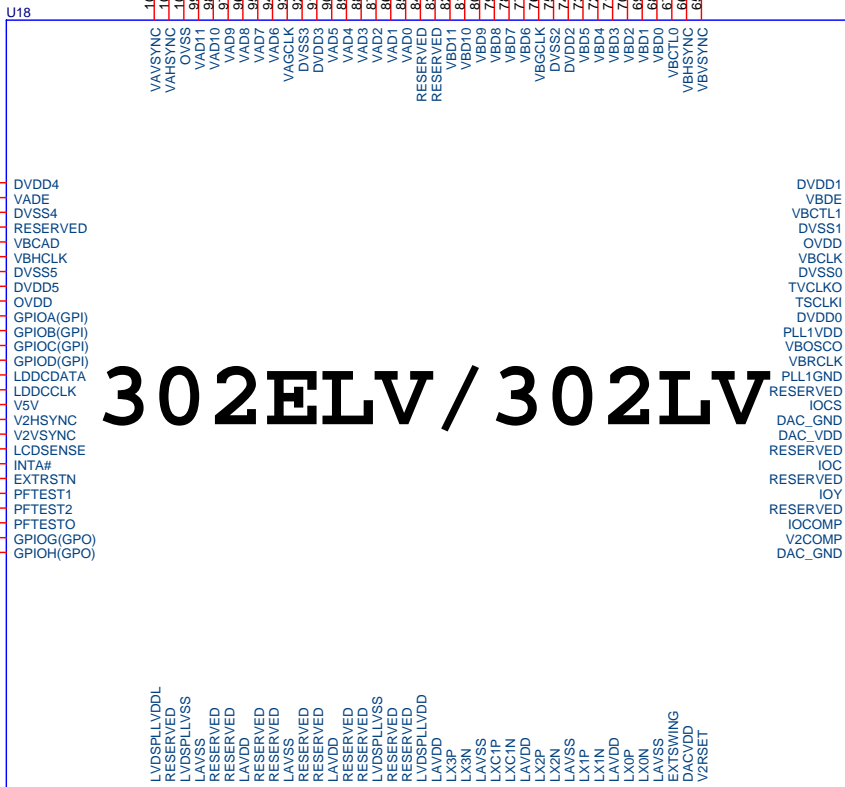
Power



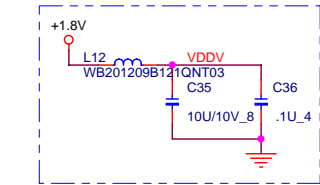
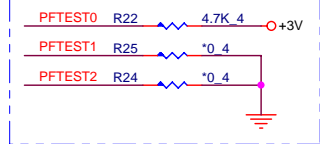
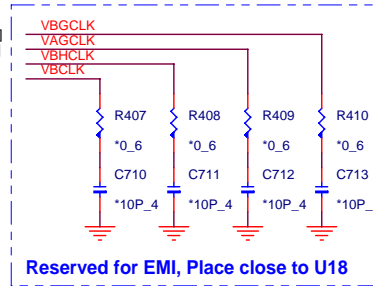
PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	M760GX(POWER)	3B
Date:	Thursday, March 10, 2005	Sheet 8 of 26

302ELV/302LV

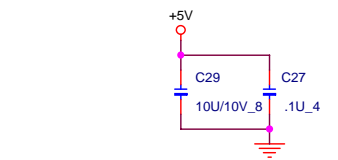
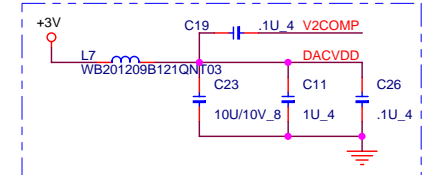
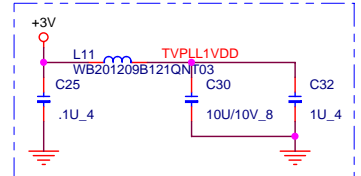
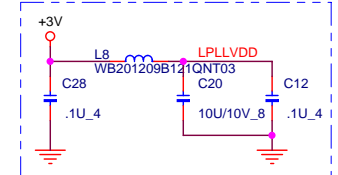
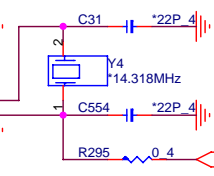


- [6] VAGCLK
- [6] VAHSYNC
- [6] VAVSYNC
- [6] VAD[11..0]
- [6] VBD[11..0]

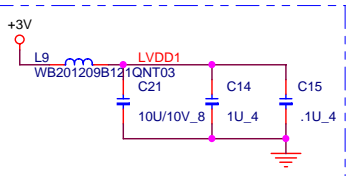
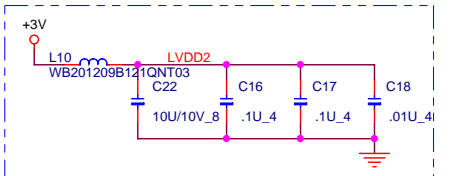
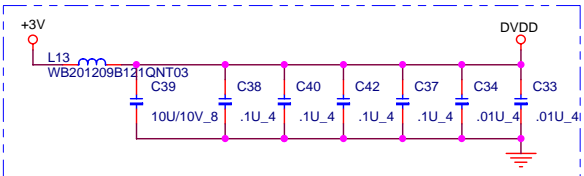


- [6] VADE
- [6] VBCAD
- [6] VBHCLK
- [10] LCDID0
- [10] LCDID1
- [10] LCDID2
- [10] PNL_DATA
- [10] PNL_CLK
- [7,11] INTA#
- [7,11,14,15,16,19,20] PCIRST#
- [10] LCDON
- [10] BKLON

- DVDD1
- VBDE
- VBCTL1
- DVSS1
- OVD
- VBCLK
- DVSS0
- TVCLKO
- TSCLKI
- DVDD0
- PLL1VDD
- VBOSCO
- R_VBRCLK
- PLL1GND
- RESERVED
- IOCS
- DAC_GND
- DAC_VDD
- RESERVED
- IOV
- RESERVED
- IOY
- RESERVED
- IOCOMP
- V2COMP
- DAC_GND

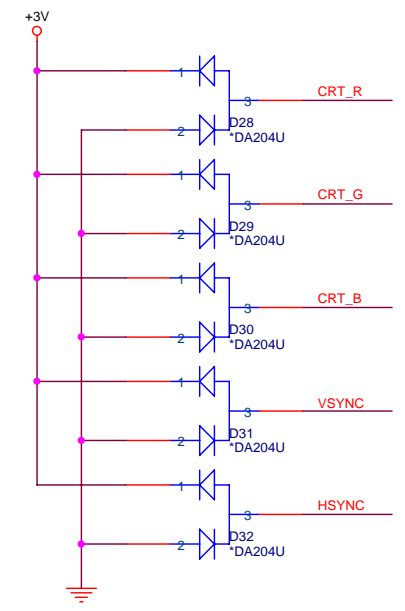
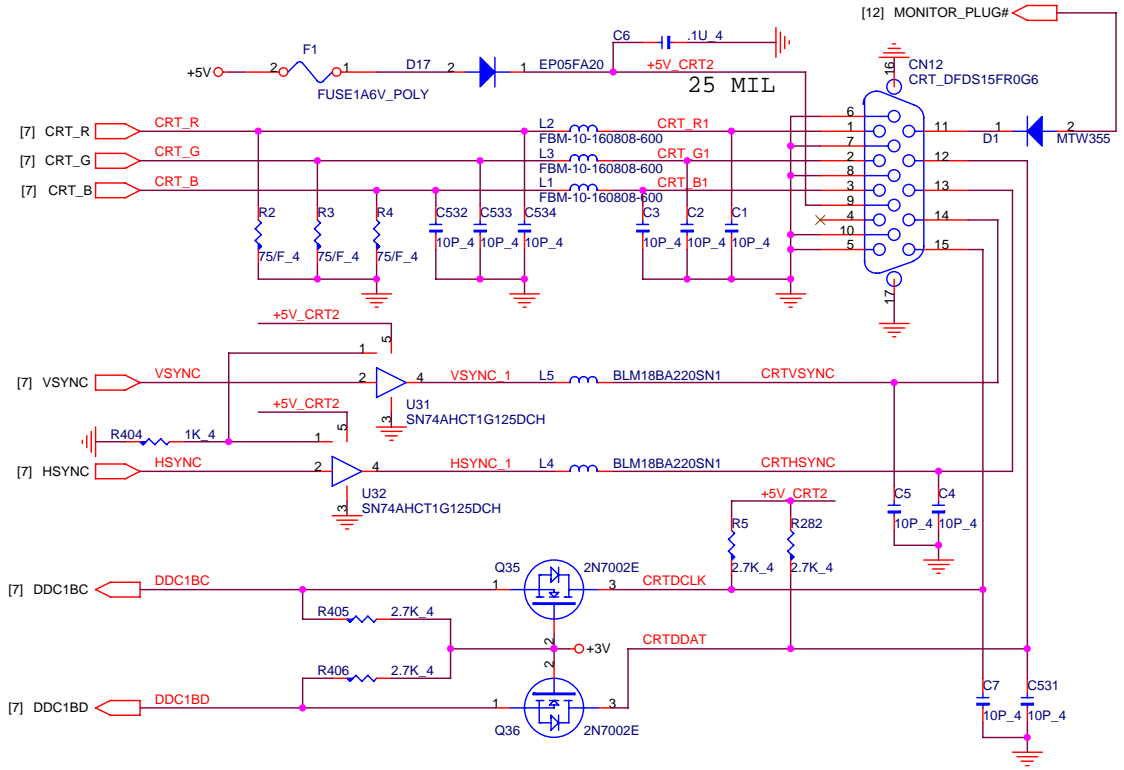
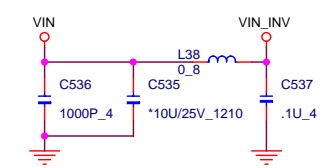
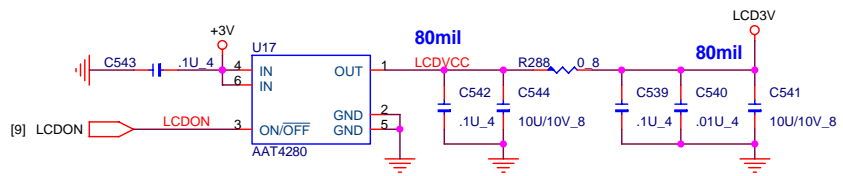
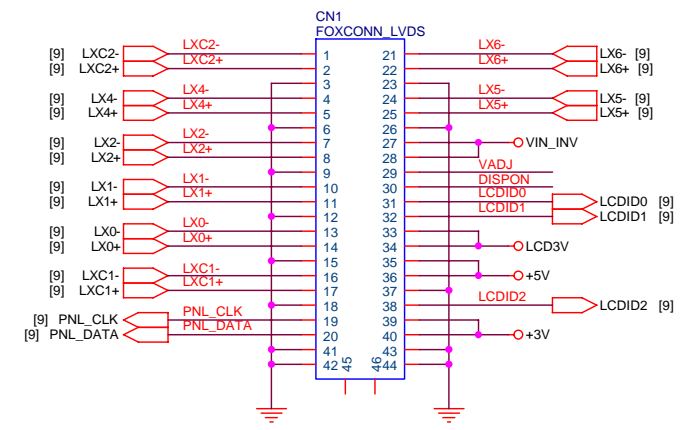
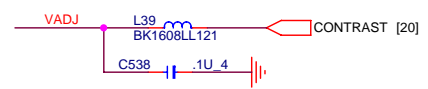
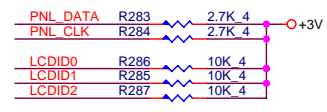
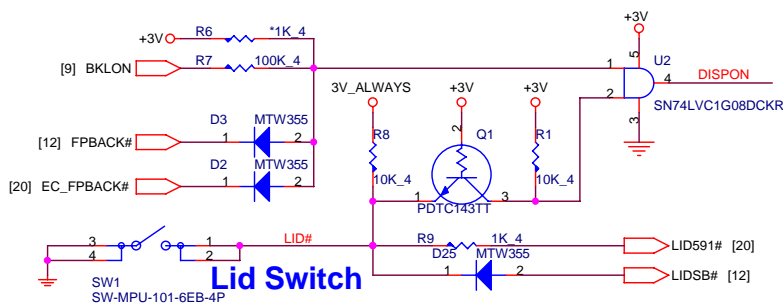


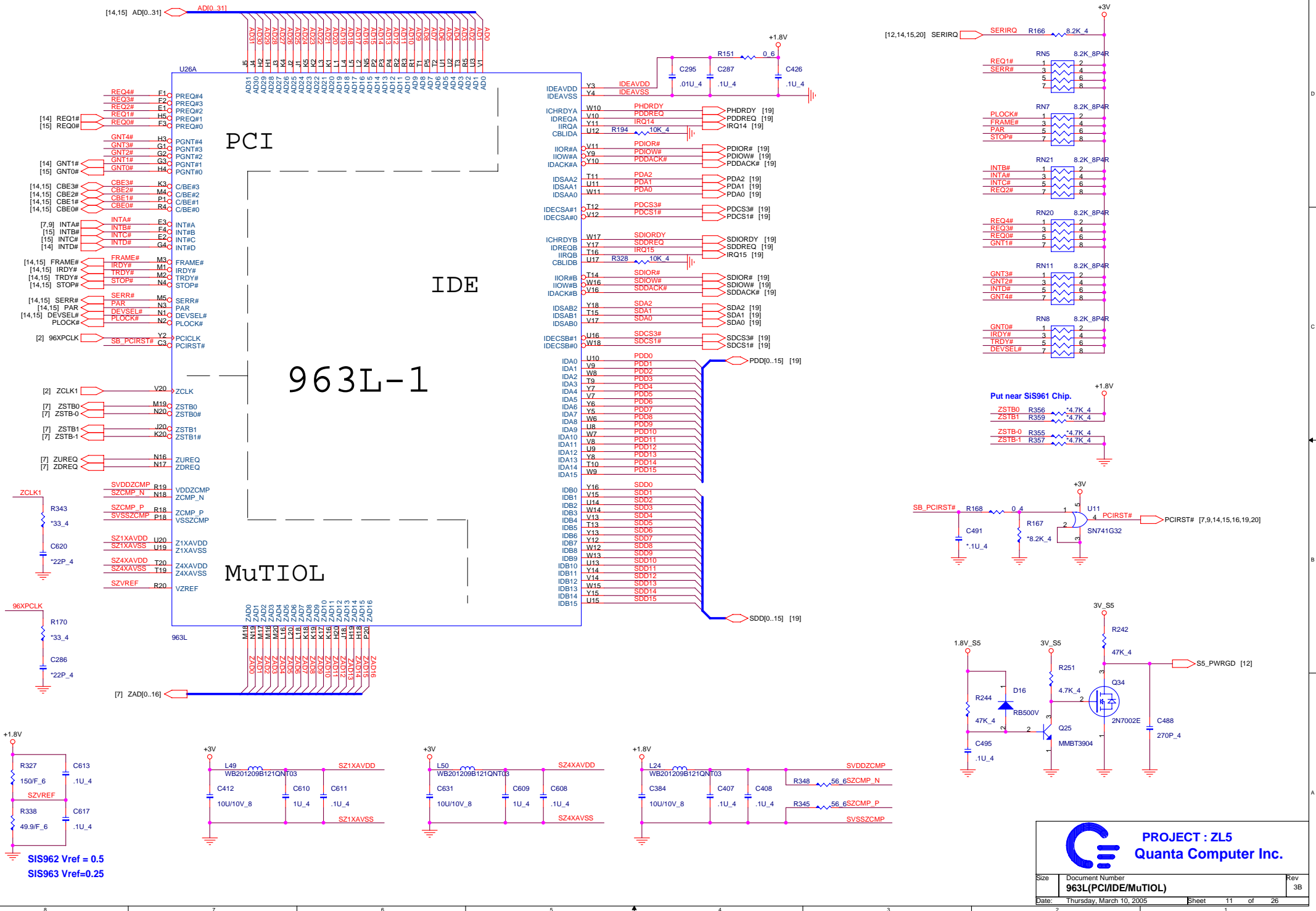
- [10] LXC2+
- [10] LXC2-
- [10] LX6+
- [10] LX6-
- [10] LX5+
- [10] LX5-
- [10] LX4+
- [10] LX4-
- [10] LXC1+
- [10] LXC1-
- [10] LX2+
- [10] LX2-
- [10] LX1+
- [10] LX1-
- [10] LX0+
- [10] LX0-

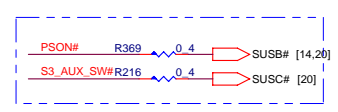
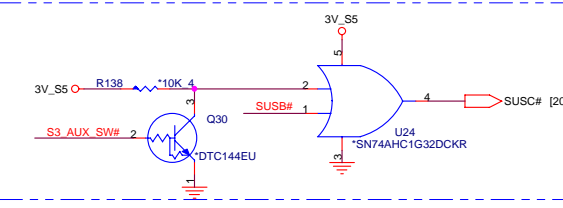
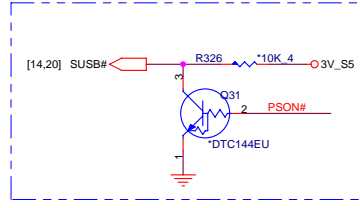
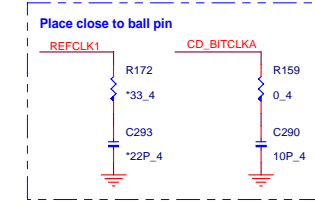
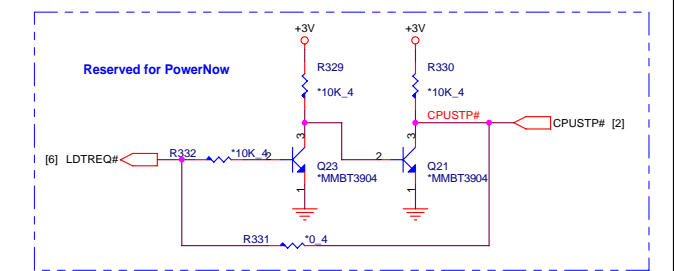
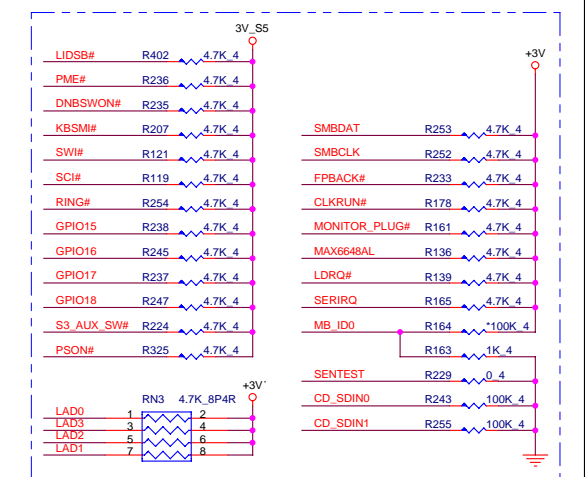
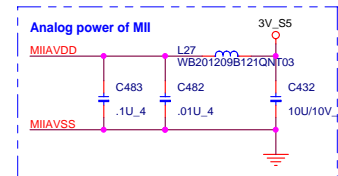
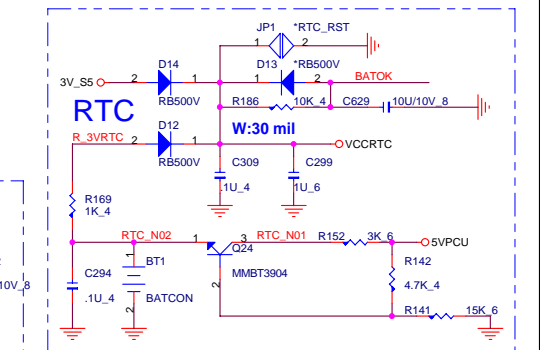
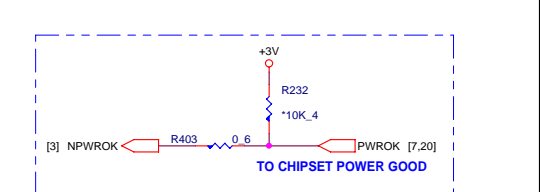
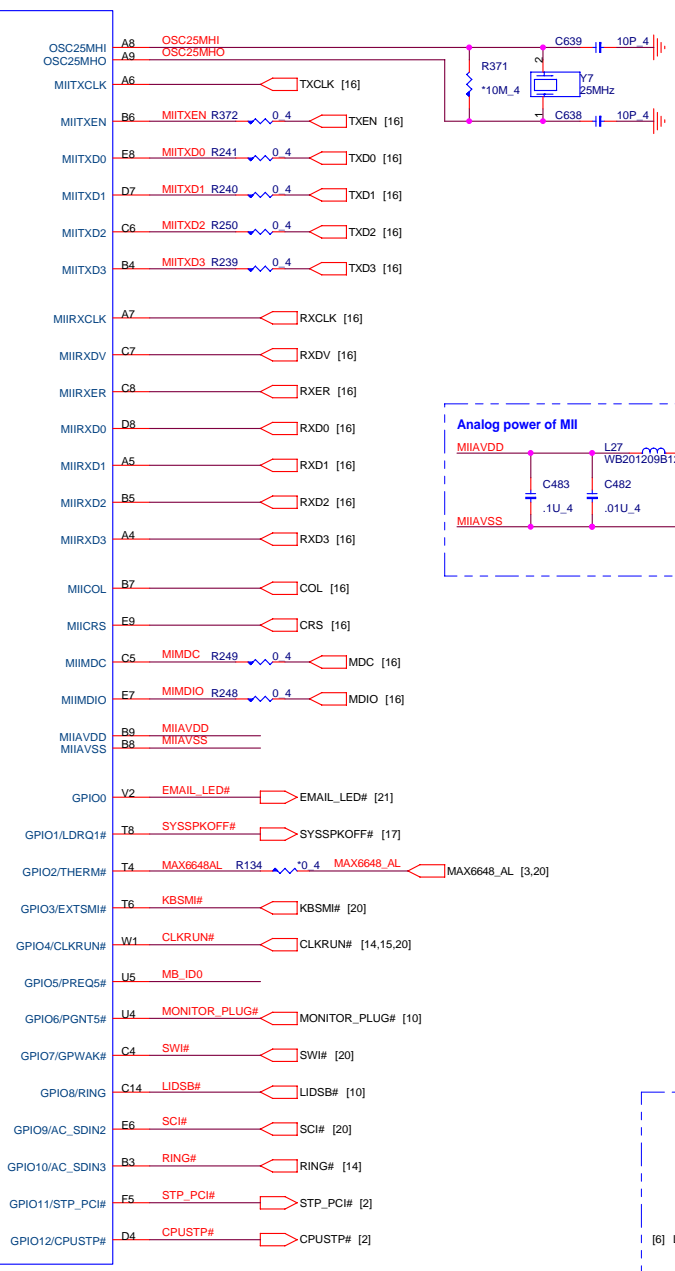
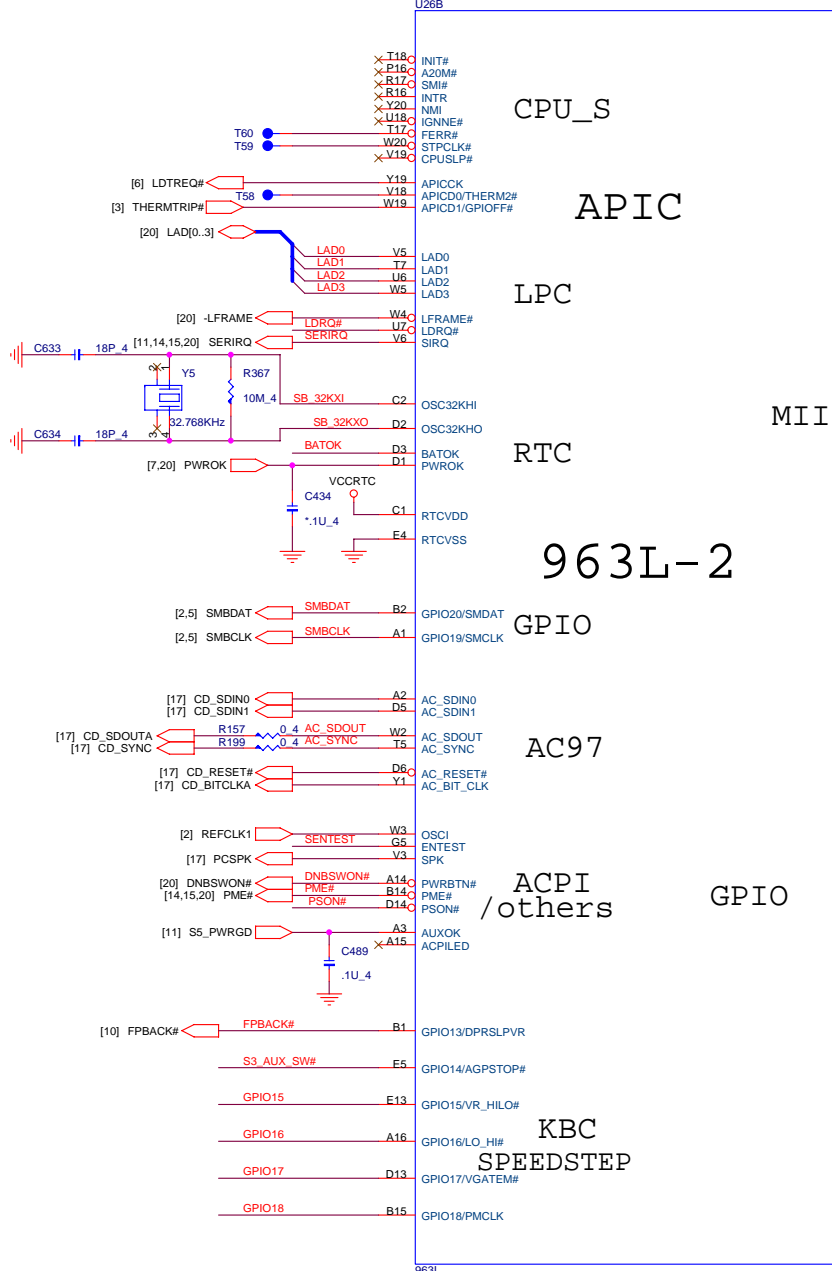


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Quanta Computer Inc.

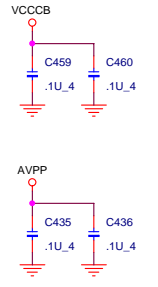
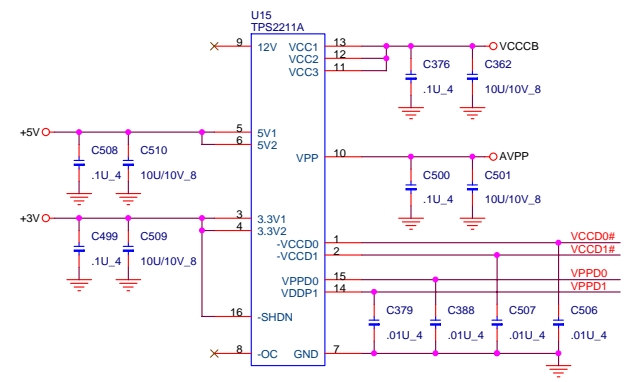
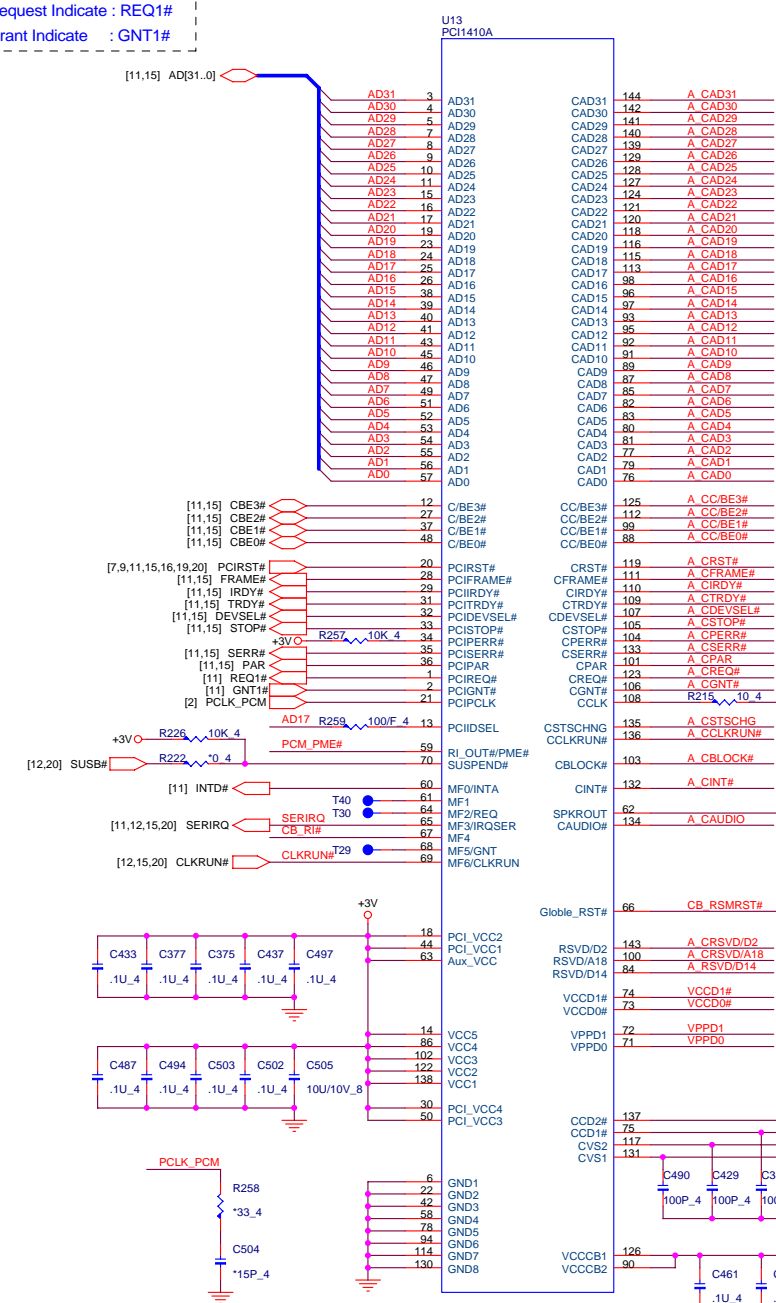
Size	Document Number 302ELV(LVDS)	Rev 3B
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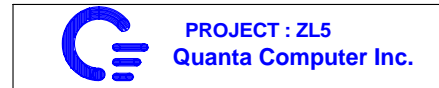
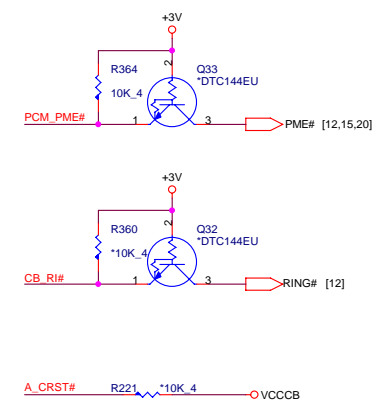
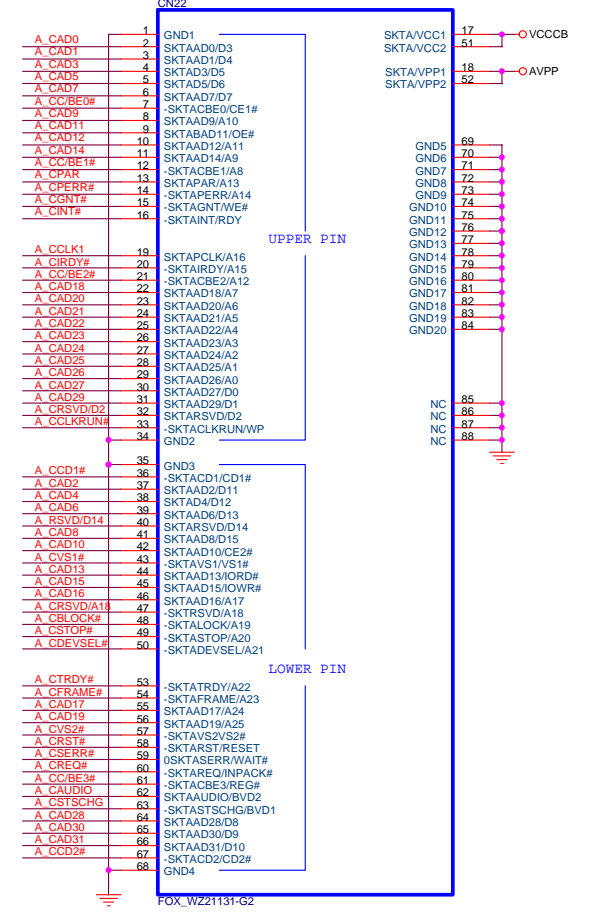




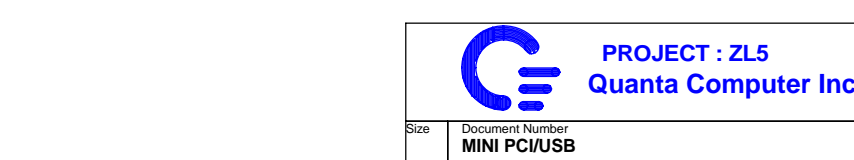
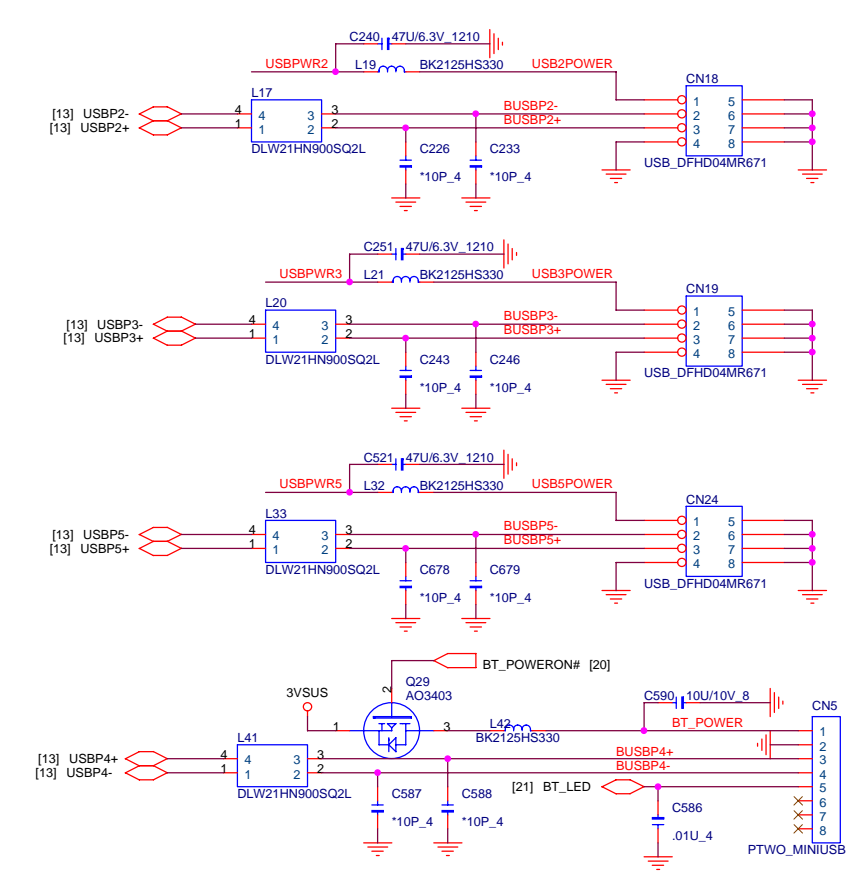
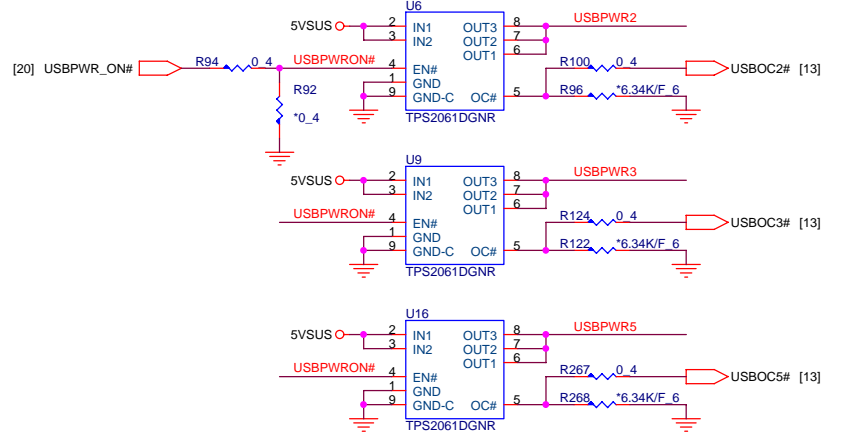
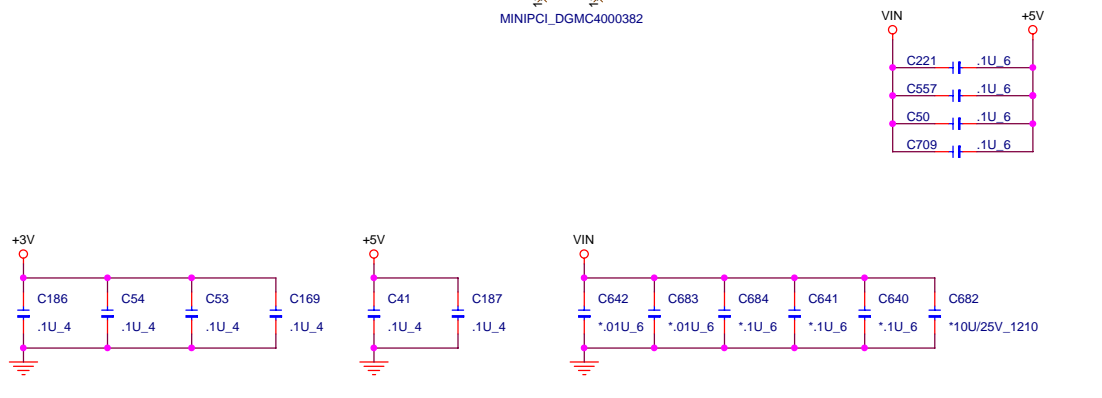
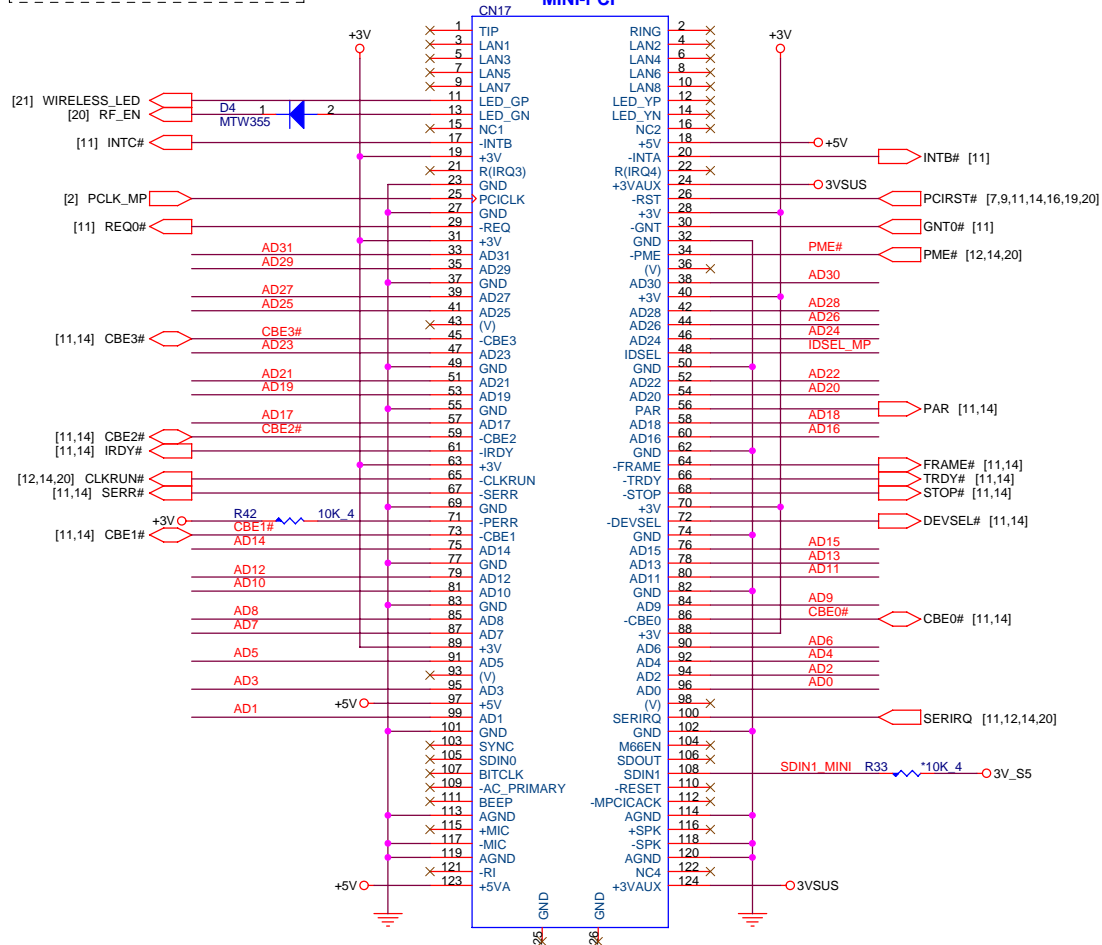
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 Interrupt Pin : INTD#
 Request Indicate : REQ1#
 Grant Indicate : GNT1#



CARBUS SLOT

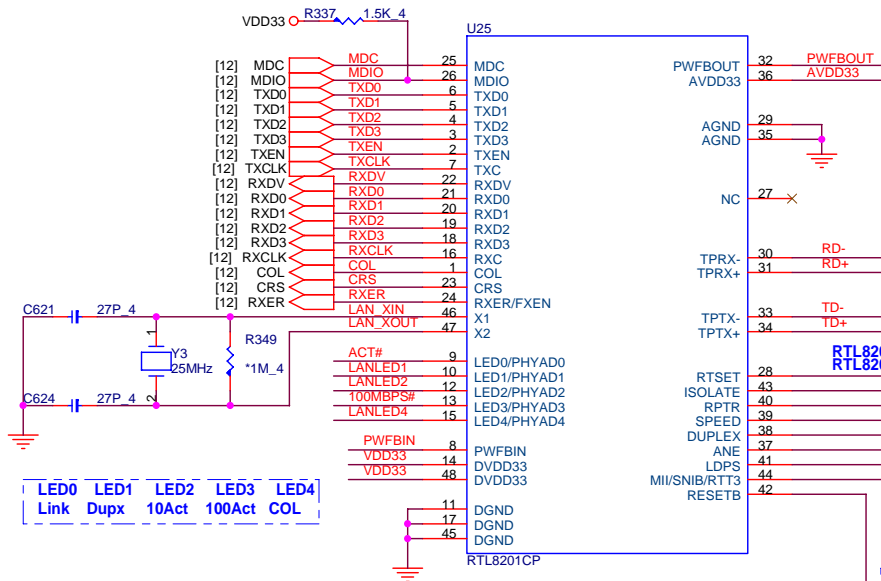


ID Select : AD22
 Interrupt Pin : INTB# , INTC#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#

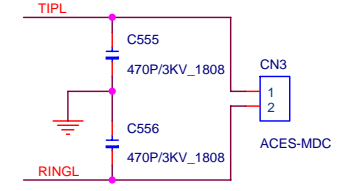
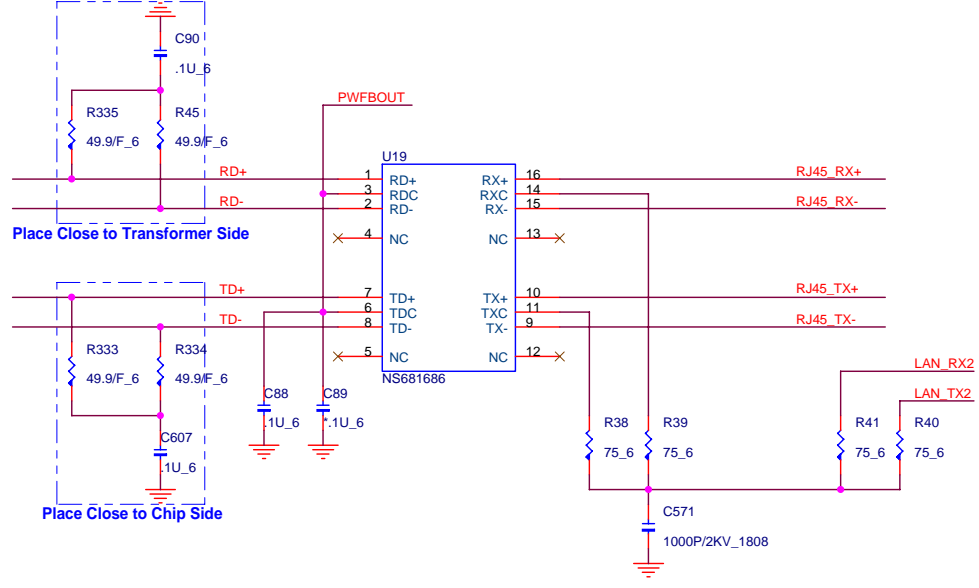
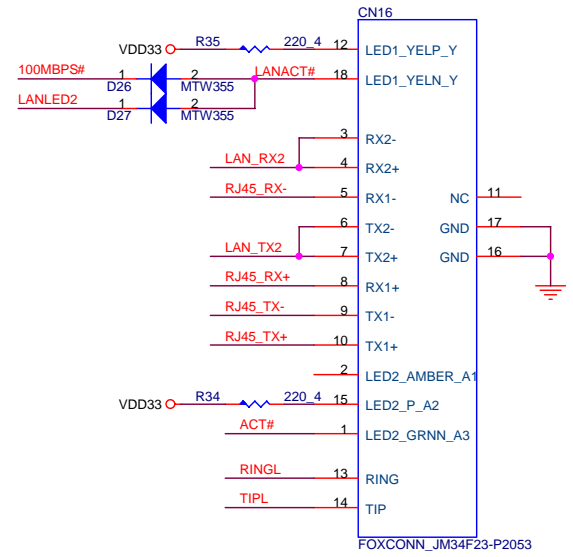
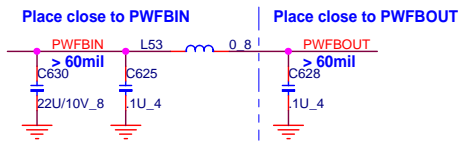
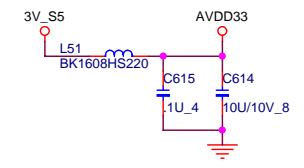
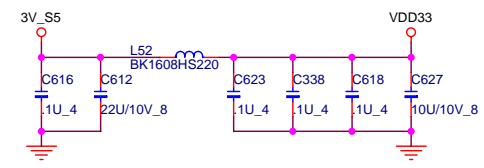
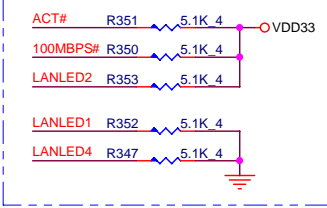
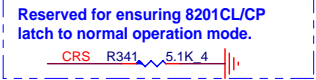
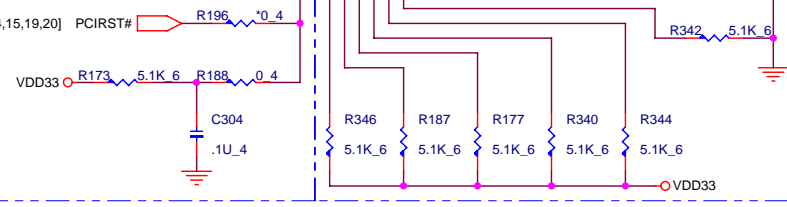


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	MINI PCI/USB	3B
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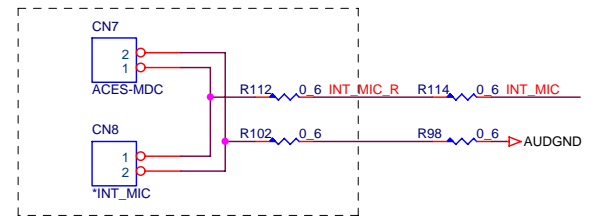
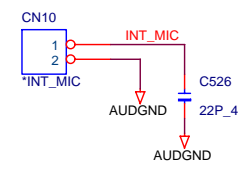
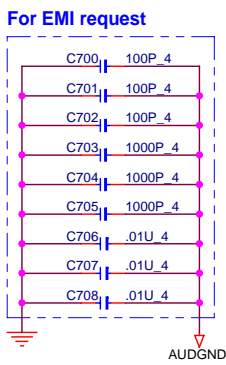
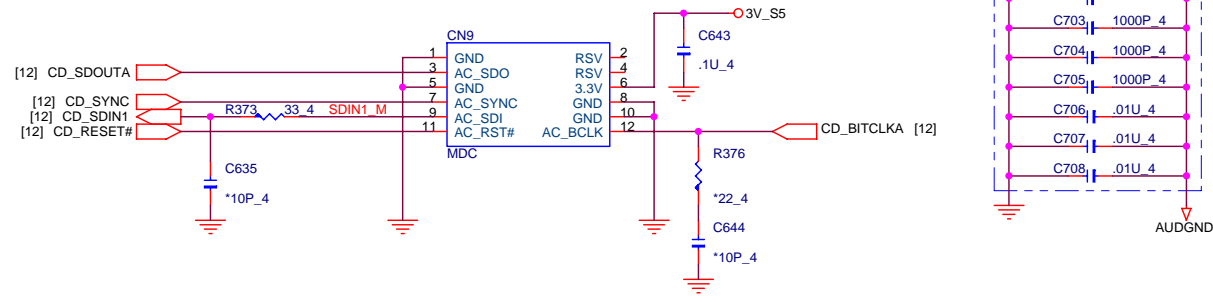
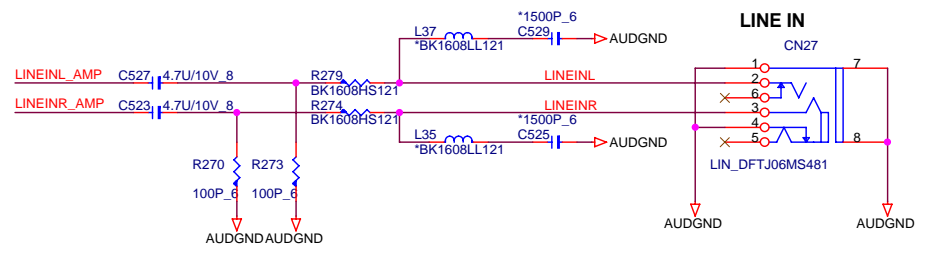
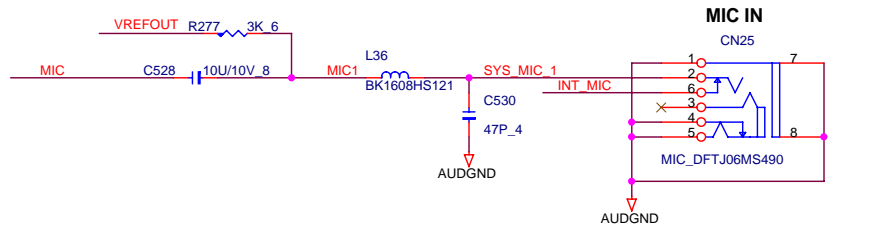
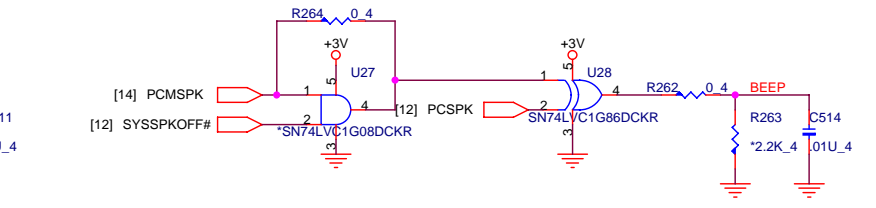
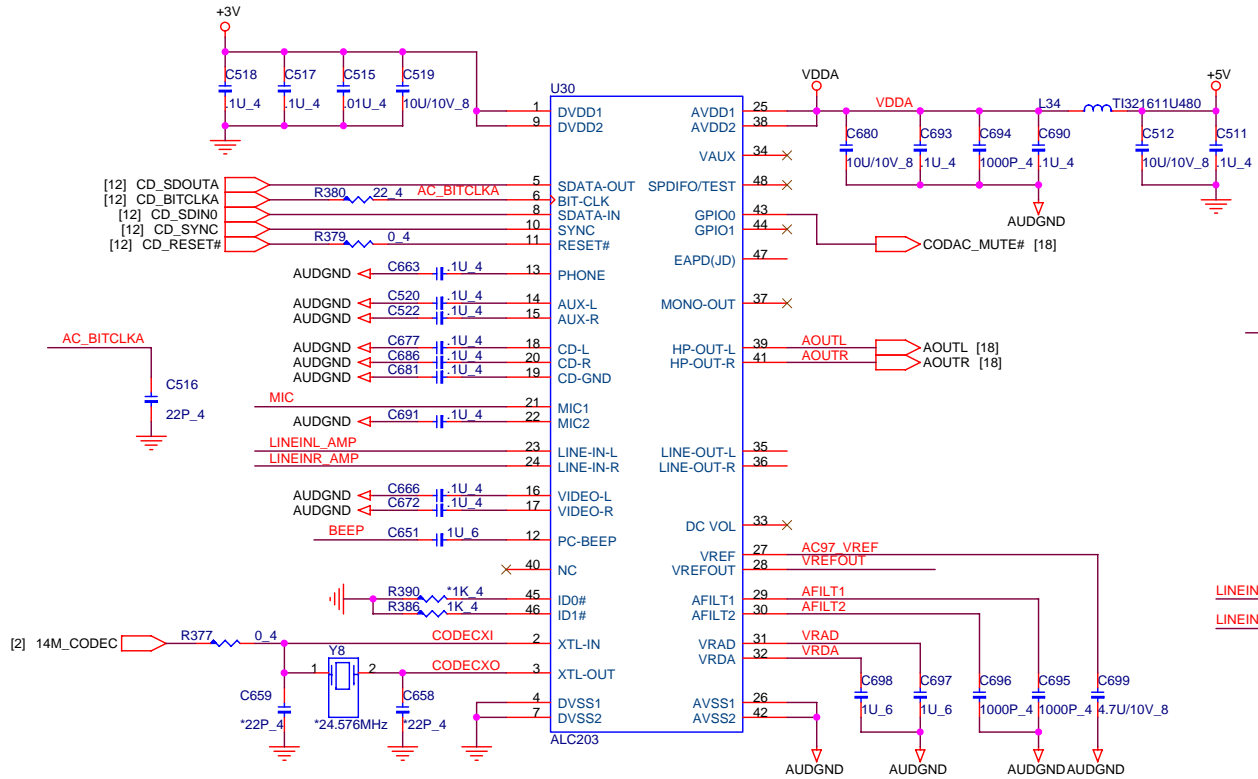



1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.



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LAN RTL8201CP Rev 3B

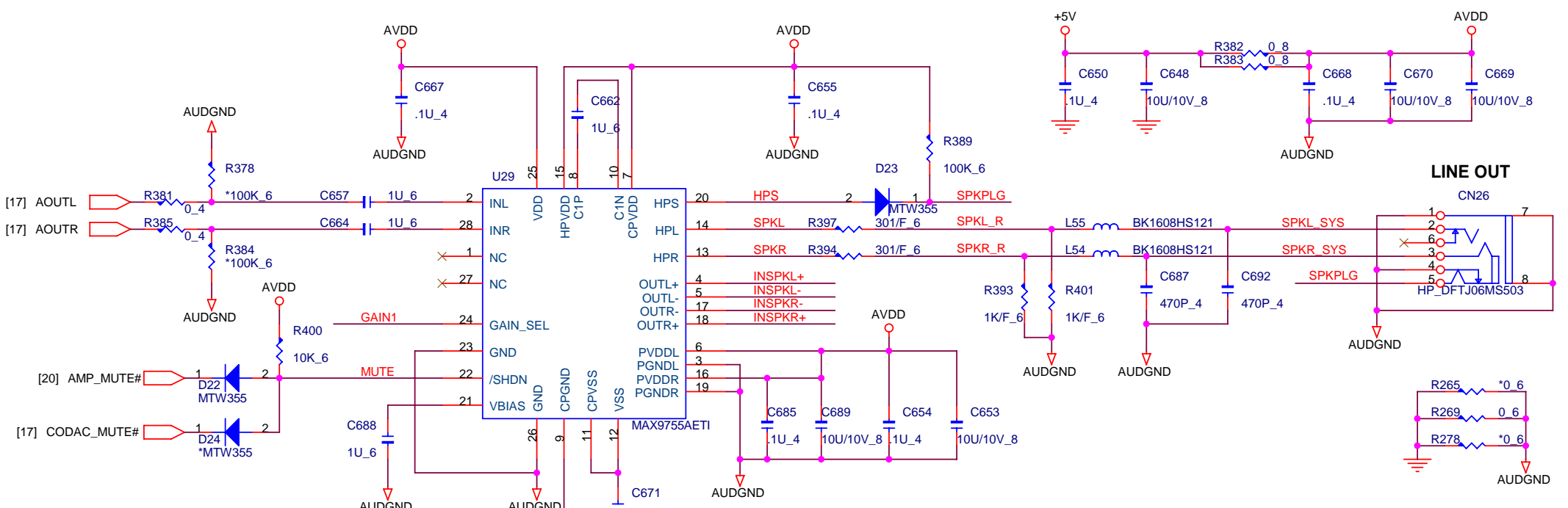
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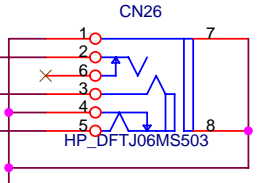


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Quanta Computer Inc.

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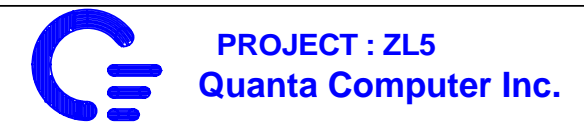
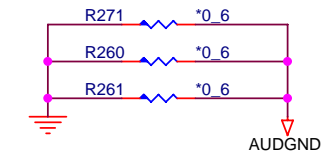
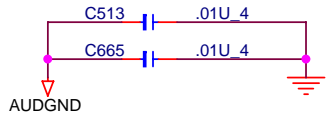
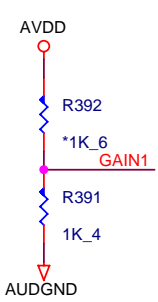
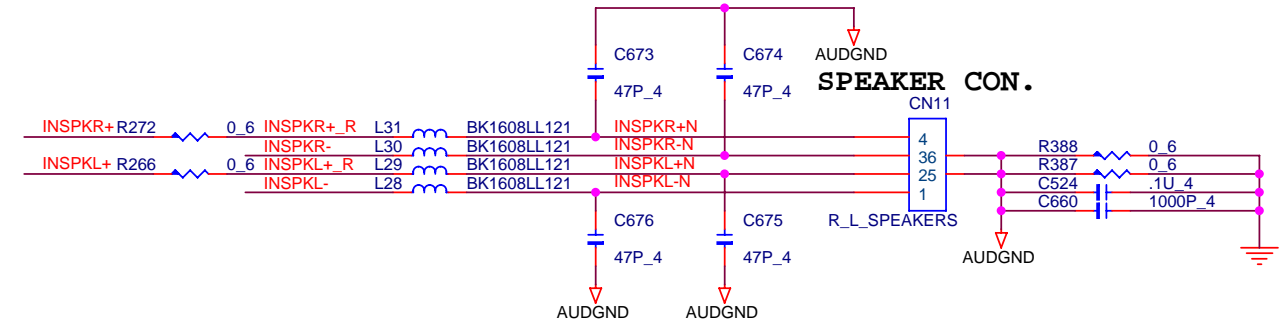


LINE OUT

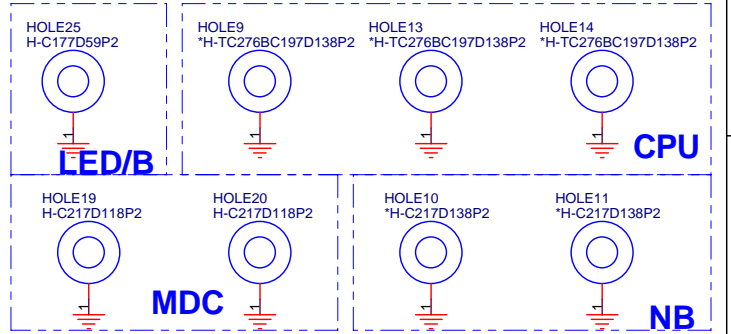
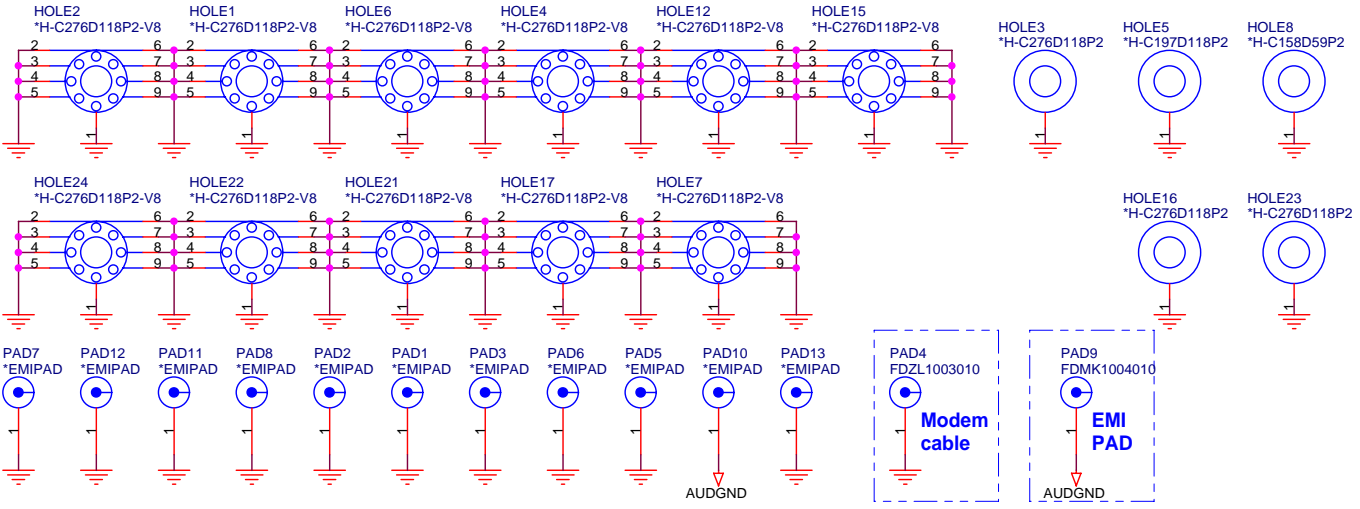
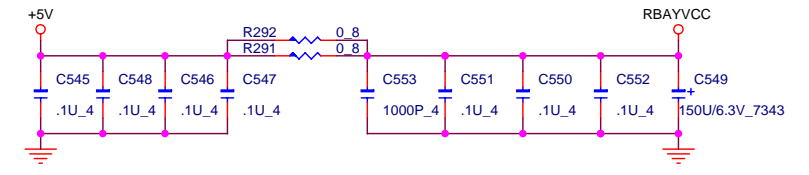
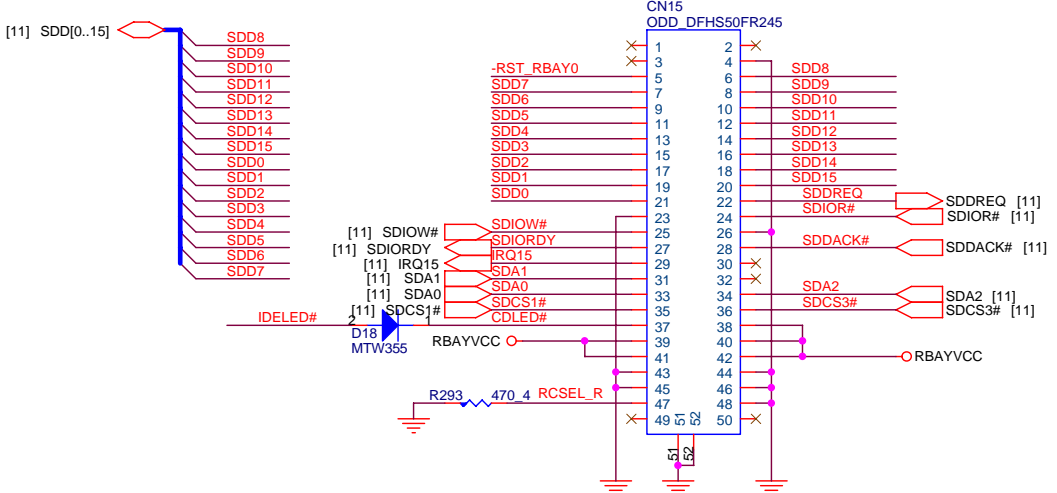
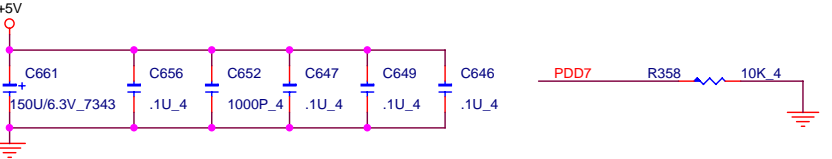
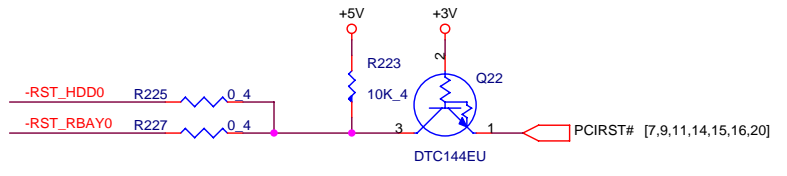
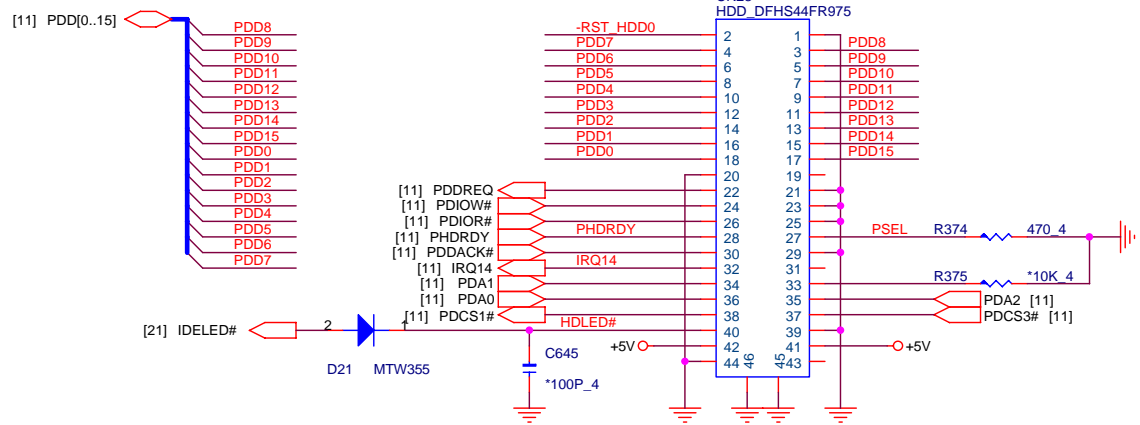


GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

SPEAKER CON.



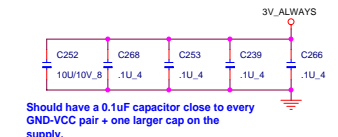
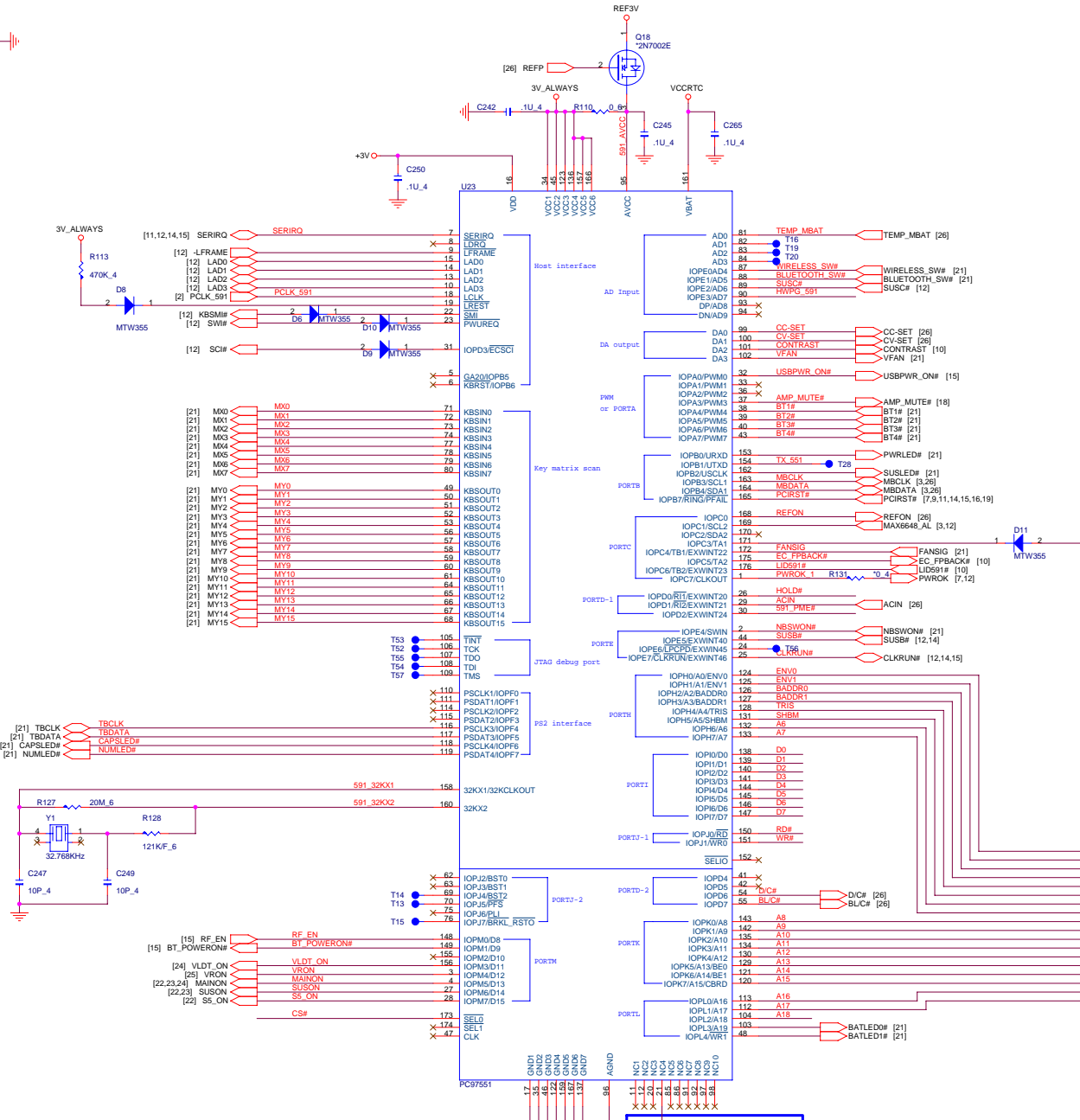
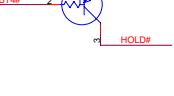
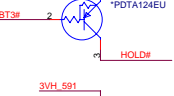
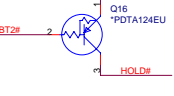
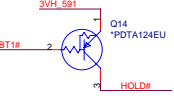
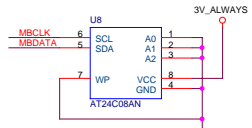
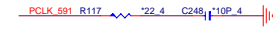
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	AUDIO AMP	3B
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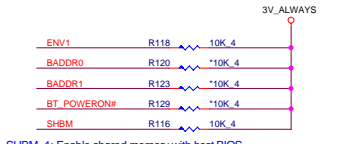
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	HDD/CDROM/SCREW	3B
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LDRQ#(pin 8) internal is no use

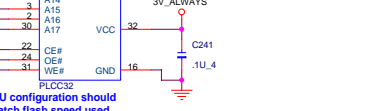
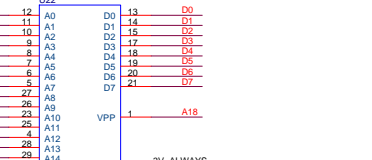
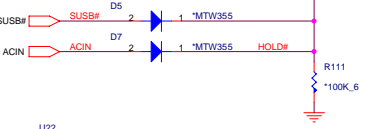
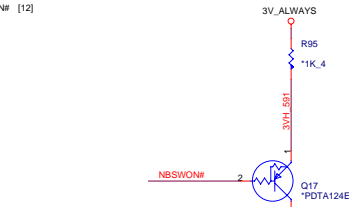
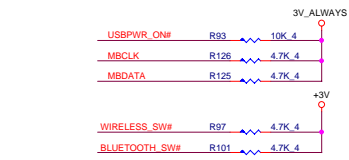


Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

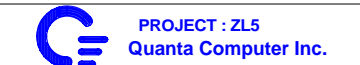


SHBM=1: Enable shared memory with host BIOS

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFG8AH, HCFG8AL)	(HCFG8BH, HCFG8BL)+1
1 1	Reserved	

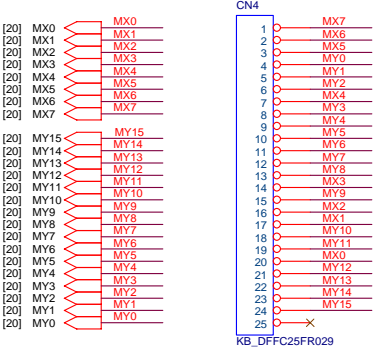


BIU configuration should match flash speed used

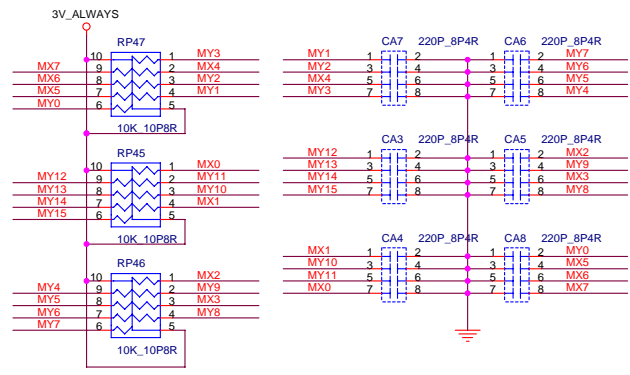


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	PC97551/FLASH	3B
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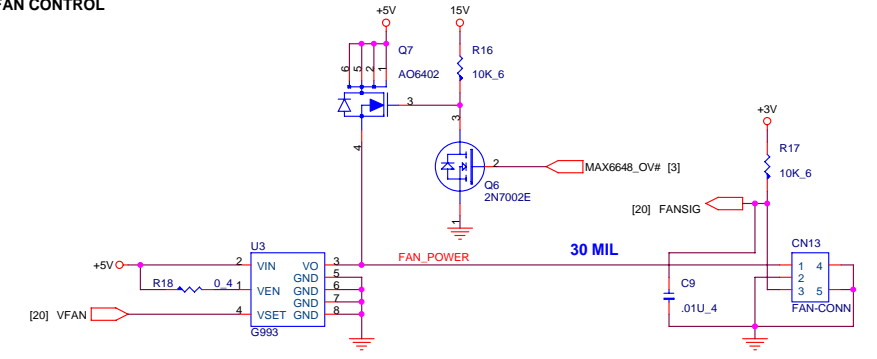
INT K/B



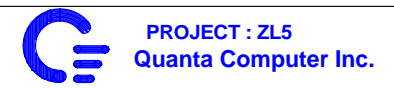
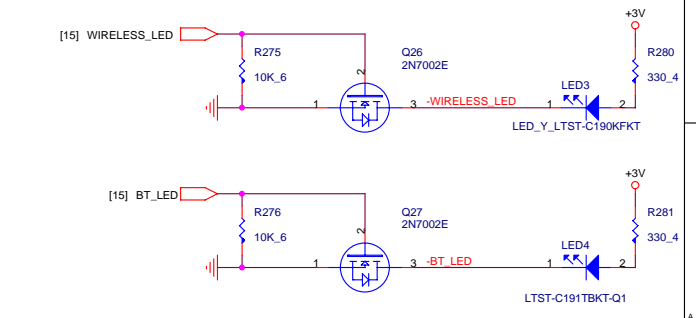
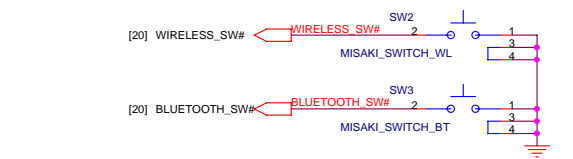
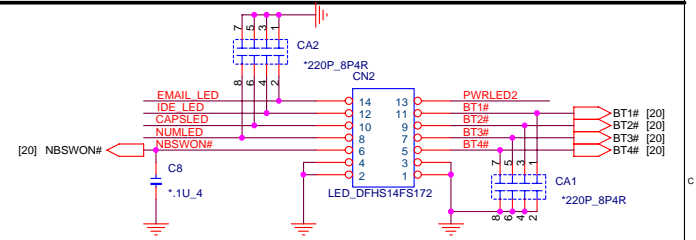
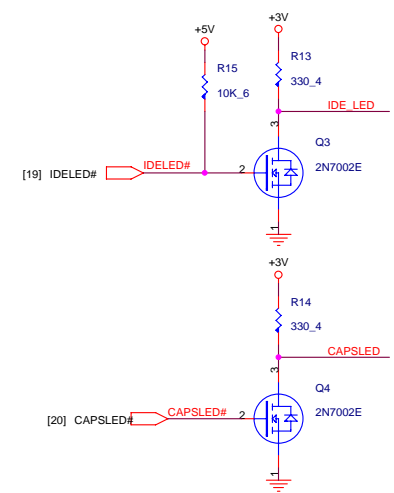
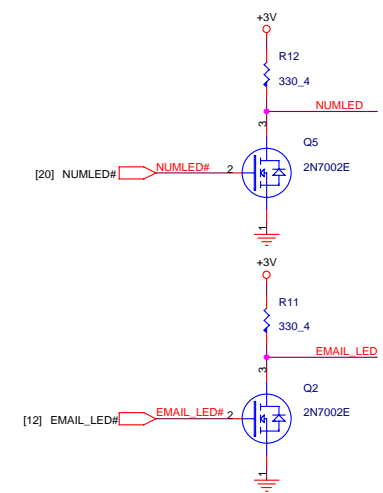
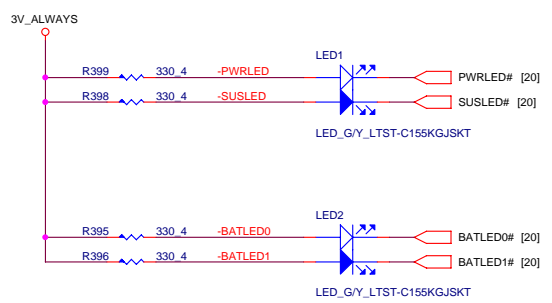
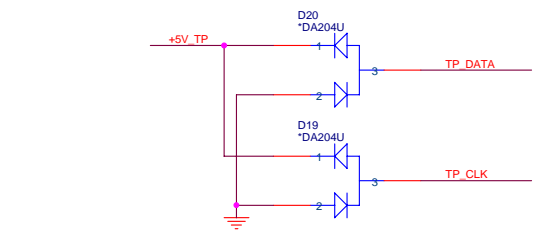
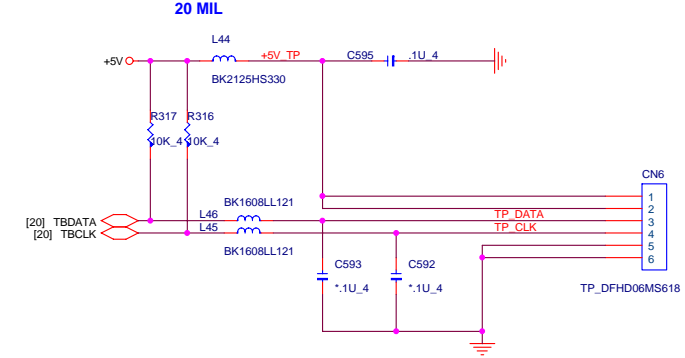
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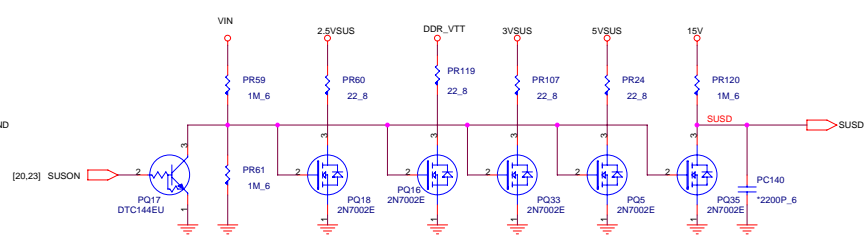
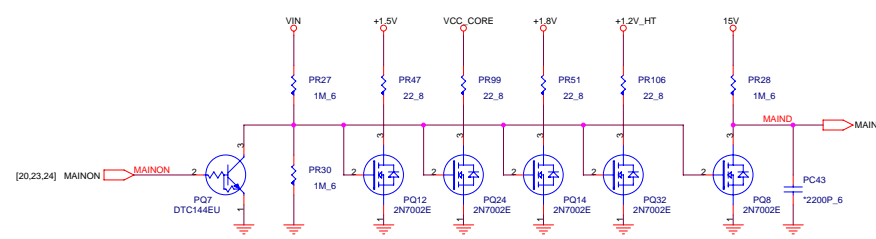
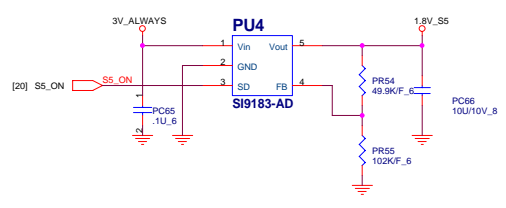
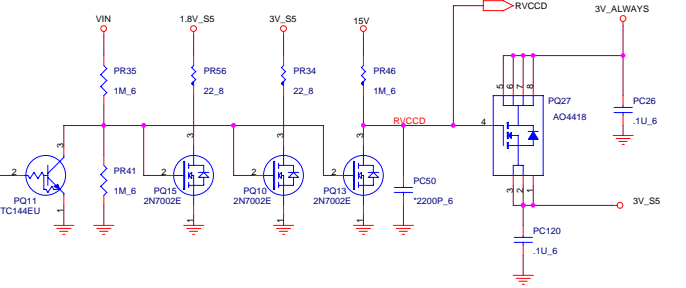
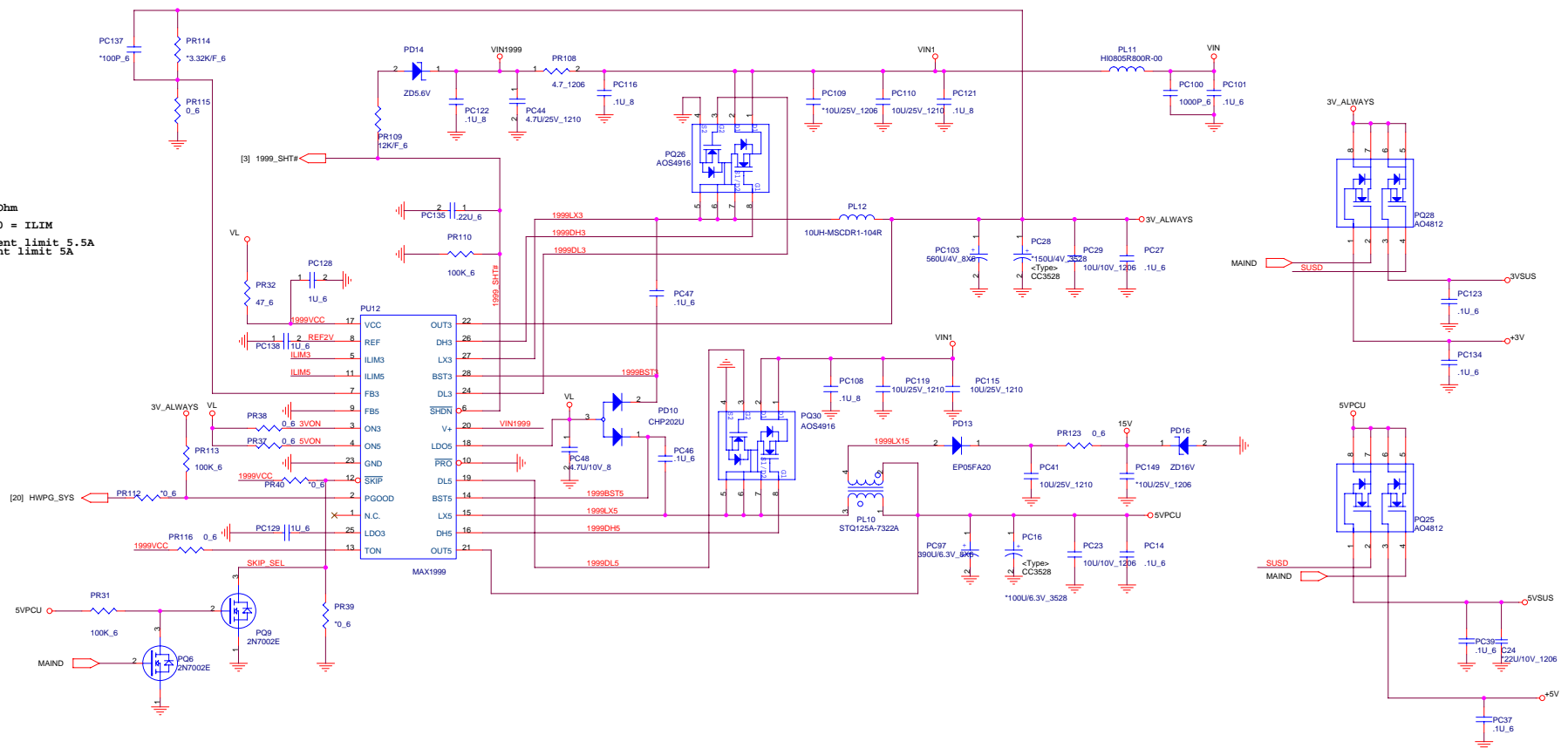
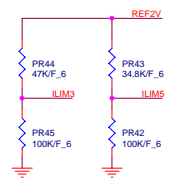
FAN CONTROL

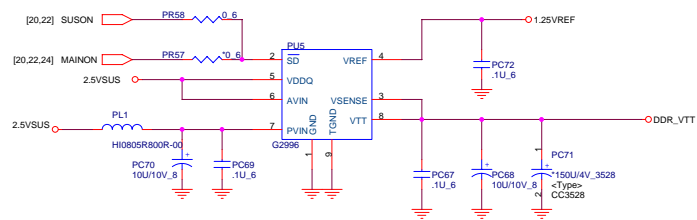
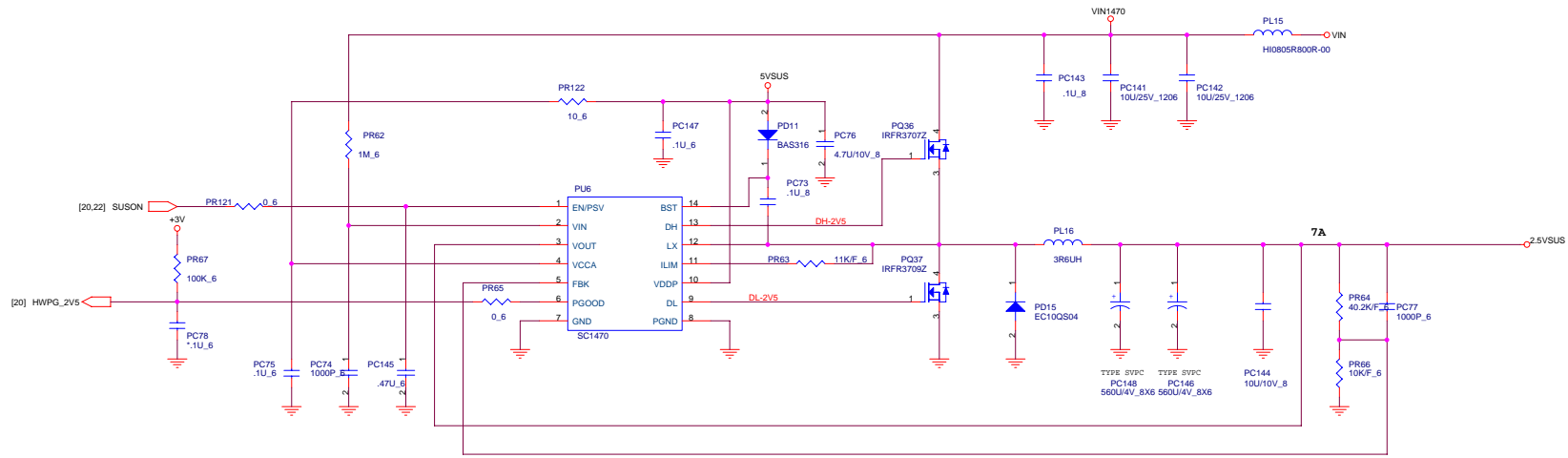


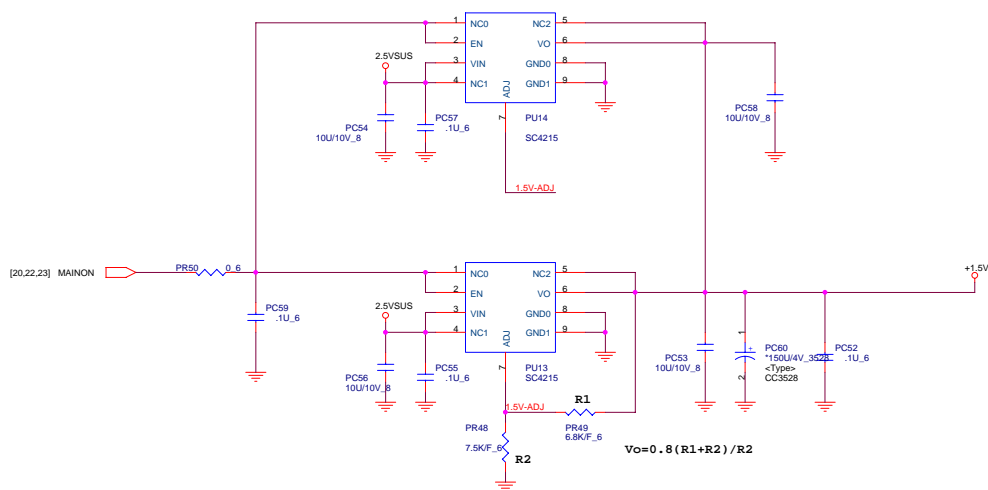
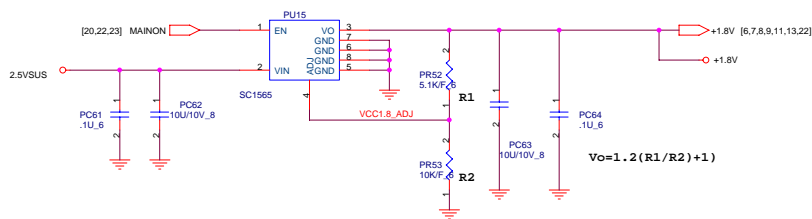
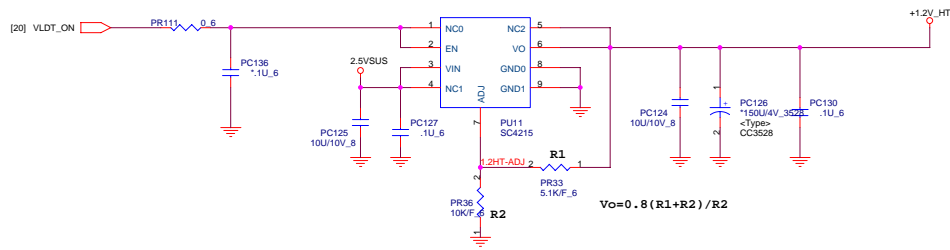
TOUCH PAD



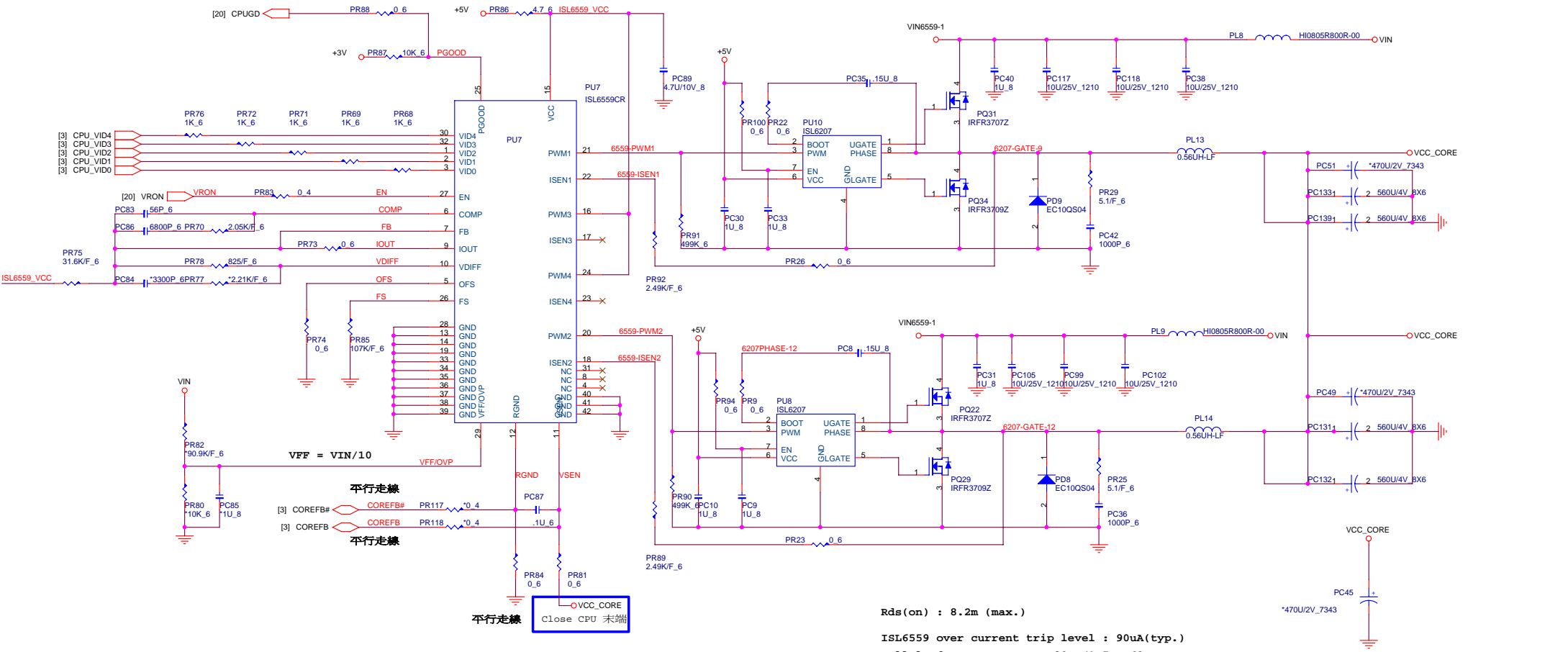
AO4916 Rds on = 27mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM5 = 1.485V Current limit 5.5A
 ILIM3 = 1.35V Current limit 5A







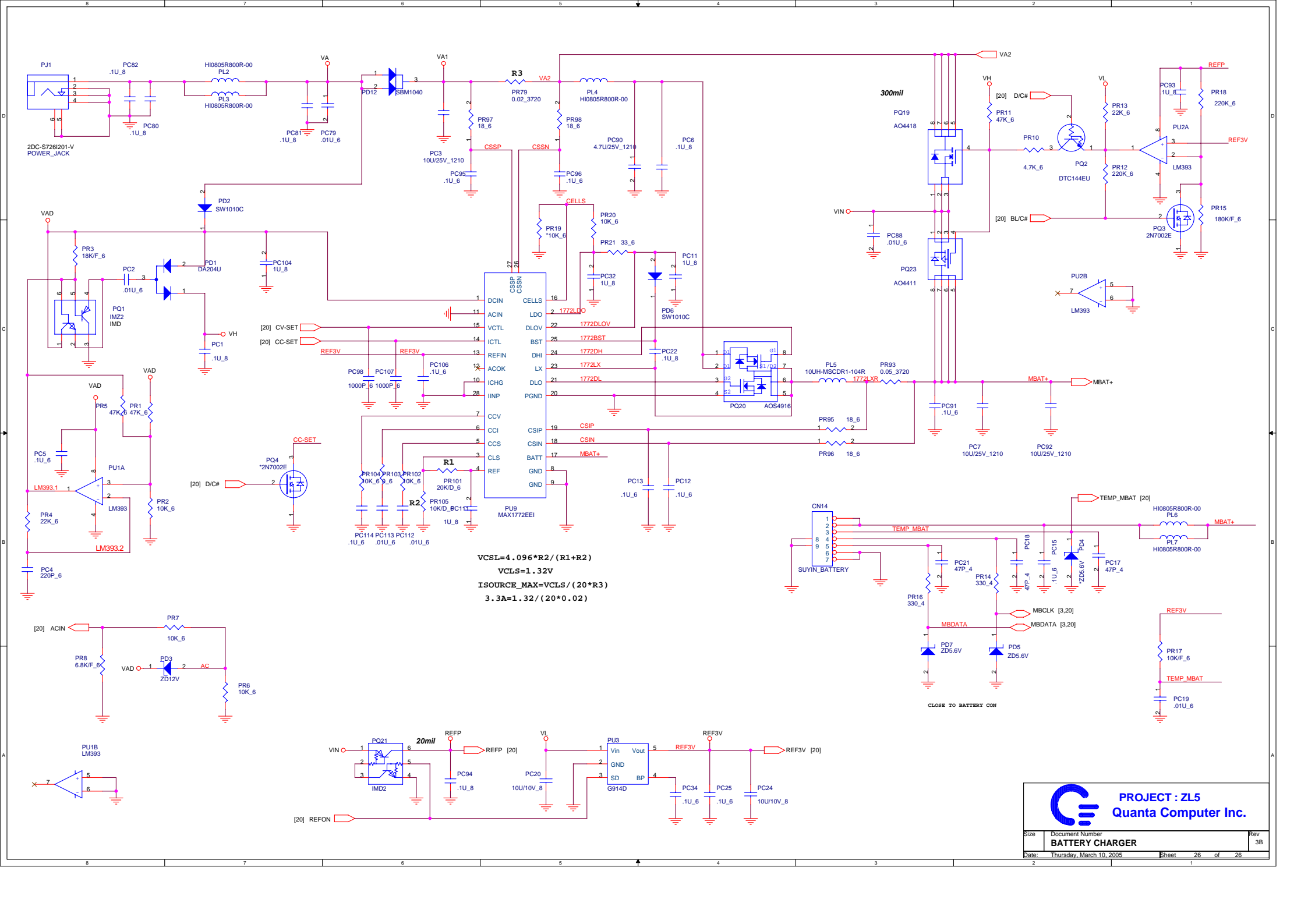
Vcore



$VFF = VIN/10$
 平行走線
 [3] COREFB# COREFB# PR117 10K 6
 [3] COREFB COREFB PR118 10K 6
 平行走線

平行走線
 VCC_CORE
 Close CPU 末端

Rds(on) : 8.2m (max.)
ISL6559 over current trip level : 90uA(typ.)
Full load Isen current : 90uA/1.5 ~ 60uA
AMD LPM 35W CORE
 $Rds(on) * Io(phase) = Rsen * Isen$
 $8.2m * 1.3 * (28A/2) = Rsen * 60uA$
Rsen = 2.48K ~ 2.49K
OCP : 28A * 1.5 = 42A



$$VCSL = 4.096 * R2 / (R1 + R2)$$

$$VCSL = 1.32V$$

$$ISOURCE_MAX = VCSL / (20 * R3)$$

$$3.3A = 1.32 / (20 * 0.02)$$