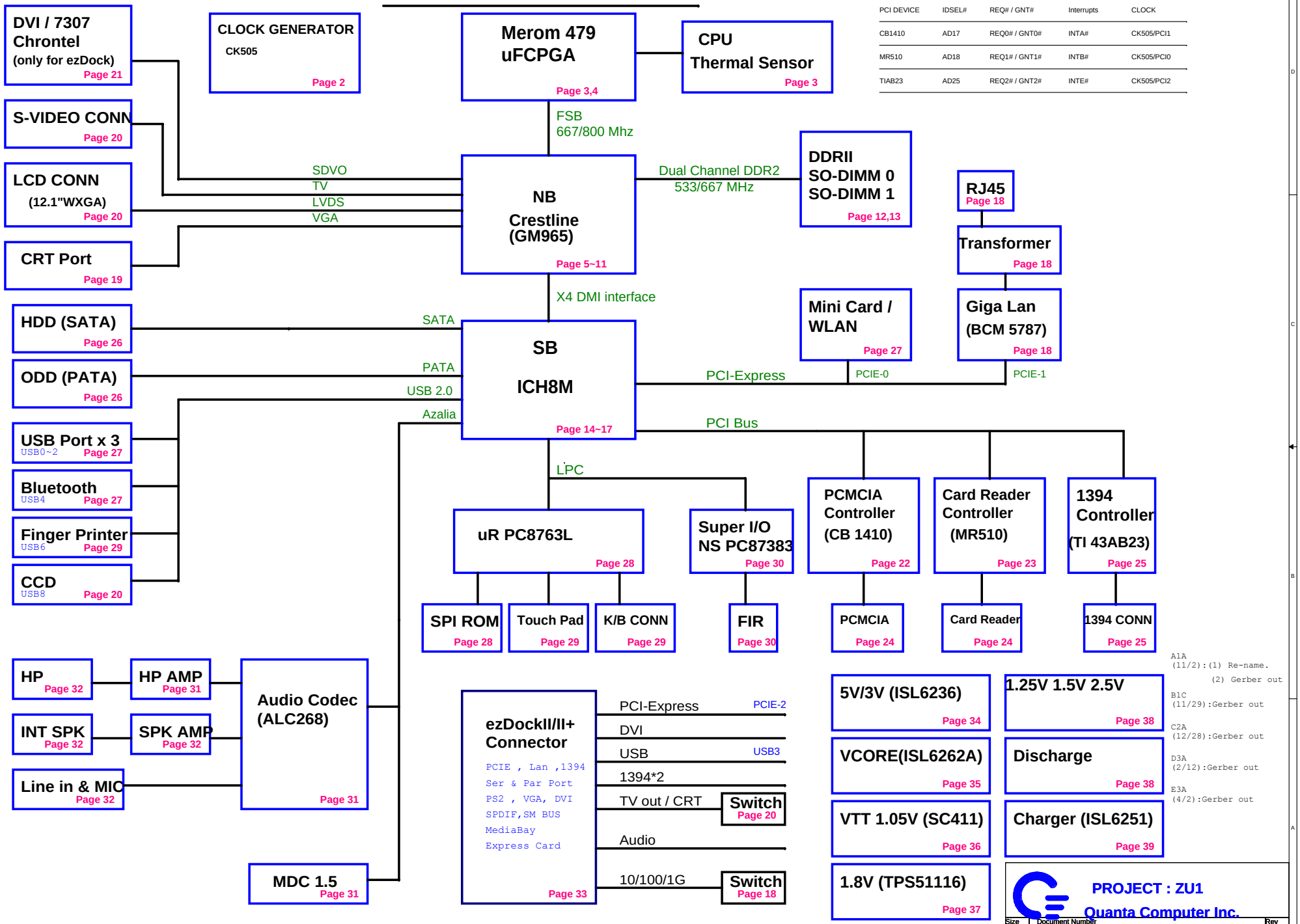
ZU1 SYSTEM BLOCK DIAGRAM



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTA#	CK505/PCI1
MR510	AD18	REQ1# / GNT1#	INTB#	CK505/PCI0
TIAB23	AD25	REQ2# / GNT2#	INTE#	CK505/PCI2

A1A
(11/2):(1) Re-name.
(2) Gerber out

B1C
(11/29):Gerber out

C2A
(12/28):Gerber out

D3A
(2/12):Gerber out

E3A
(4/2):Gerber out

PROJECT : ZU1
Quanta Computer Inc.

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	Block Diagram	3B
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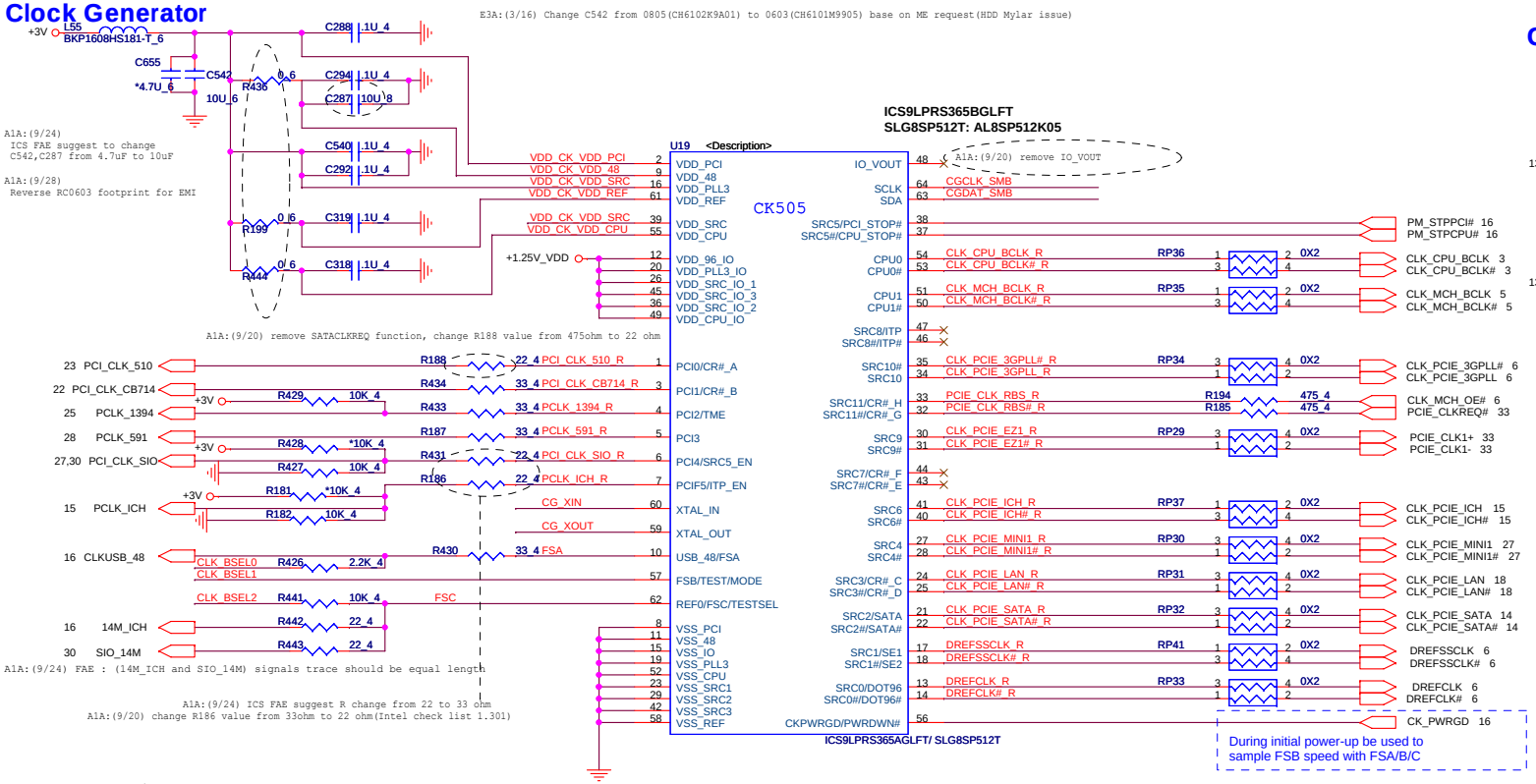
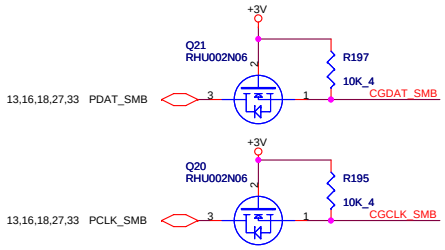
Clock Generator

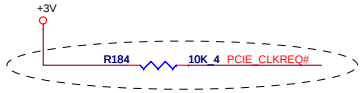


Clock Gen I2C

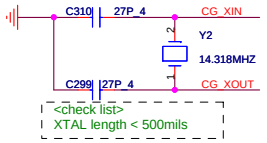


Pin	Active	Control signal
32	Low	SRC9/9#
33	Low	SRC10/10#

A1A:(9/24) Base on above table, SWAP SRC3 and SRC9



C2A:(12/26) Base on vendor-FCE suggestion, change C310/C299 from CH03306JBD7 (33p) to CH02706JB06(27p)



<check list>
(1)PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.

(2)PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock.
If PD be detect at powe-on,the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP
(Default is setting to PCI_STOP/CUP_SOTP)

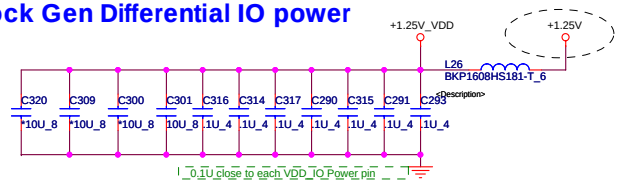
(3)PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock.
If PD be detect at powe-on,the CK505 will setting Pin 46/47 to SRC8
(Default is setting to SRC8)

(4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M ,
Pin 37, 38 will fixed be use CPU_Stop and PCI_Stop.

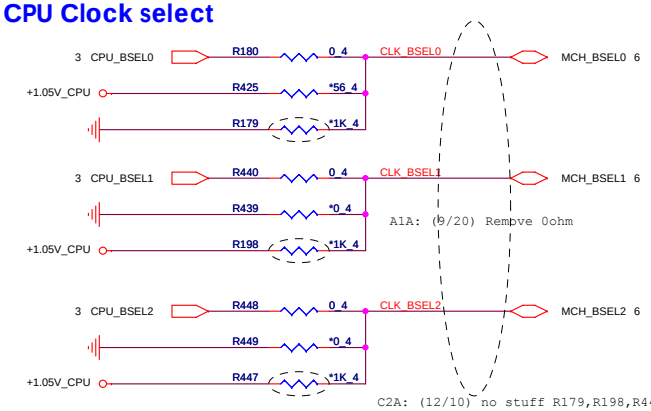
(5)SLG505YC64 CK505 Standar parts follow standar setting

C2A:(12/12)change from +1.05V to +1.25V.
Because VDD_IO will drop out when high loading

Clock Gen Differential IO power



CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

C2A: (12/10) no stuff R179,R198,R447 for auto CPU frequence selection (follow ZD1,ZO1)

PROJECT : ZU1

Quanta Computer Inc.

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	CLK. GEN./ CK505	3B
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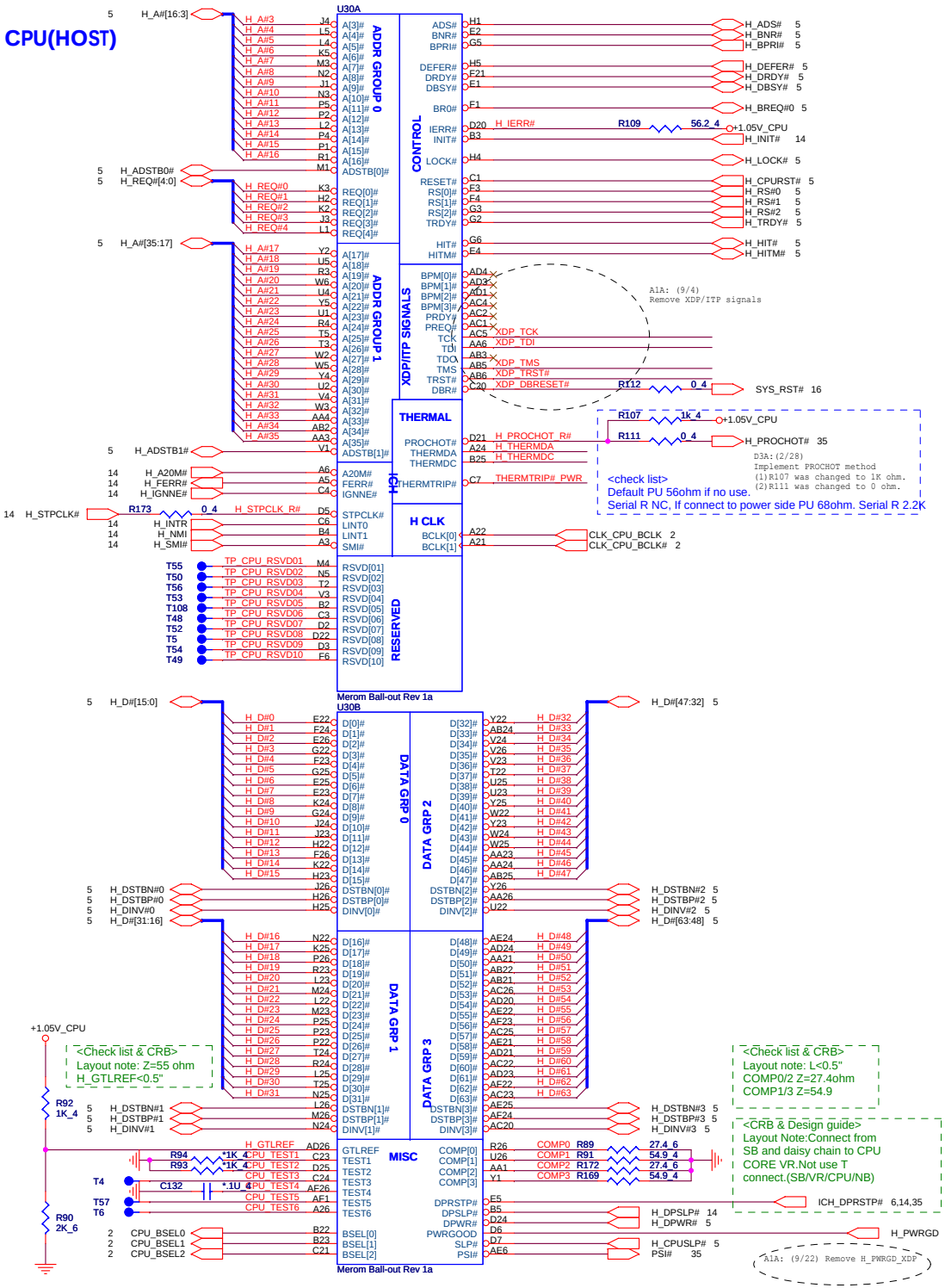
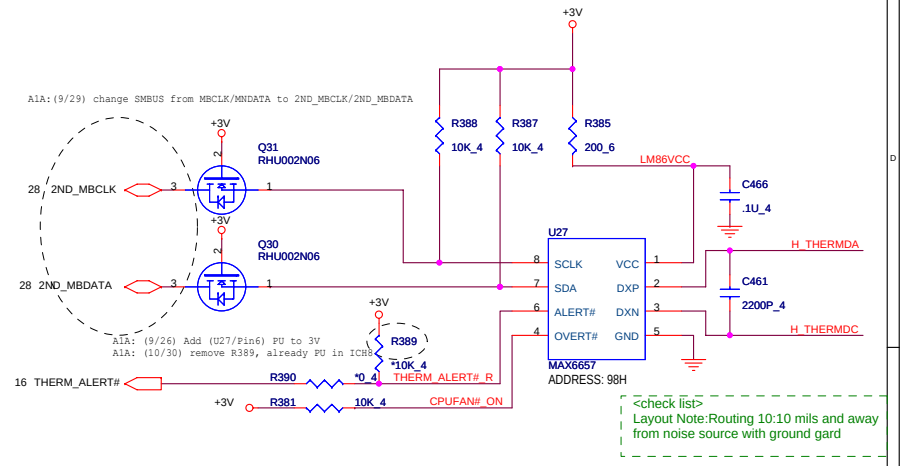
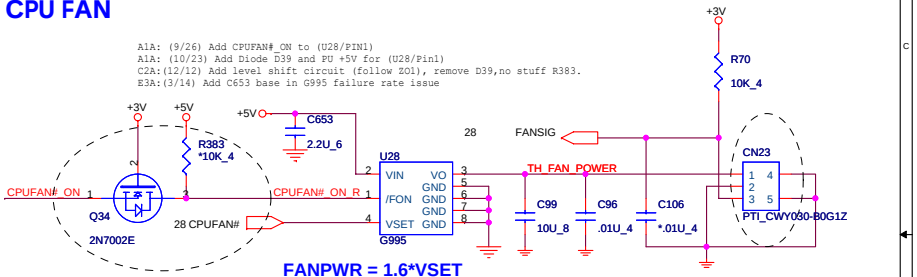
CPU(HOST)



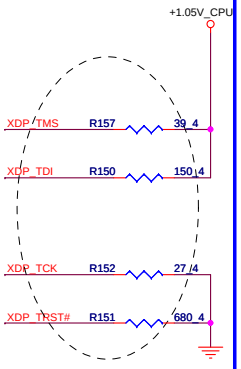
CPU Thermal monitor



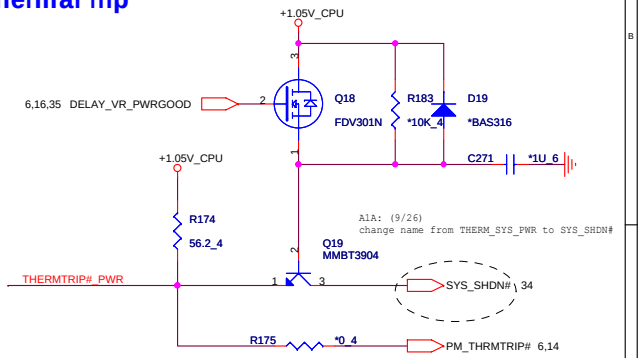
CPU FAN



PU/PD (ITP700)



Thermal Trip



PROJECT : ZU1

Quanta Computer Inc.

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CPU(Power)

VCC_CORE

C517 C222 C481 C483 C499 C479 C513 C515 C221 C498 — 10U_8

C478 C480 C482 C514 C502 C171 C191 C172 C512 C521 — 10U_8

C230 C223 C500 C503 C231 C501 — 10U_8

C516 C193 C504 C192 C173 C484 — 10U_8

CH61001ME96

<Description>

DESIGN GUIDE
CHANGE FROM 22UF *20 TO 10UF *32

C198 330U_7343

C217 *330U_7343

C197 330U_7343

A1A:(10/13) stuff C198, unstuff C217
(base on layout location)

<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

U30C

VCC[001] A7, VCC[002] A9, VCC[003] A10, VCC[004] A12, VCC[005] A13, VCC[006] A15, VCC[007] A17, VCC[008] A18, VCC[009] A20, VCC[010] B7, VCC[011] B9, VCC[012] B10, VCC[013] B12, VCC[014] B14, VCC[015] B15, VCC[016] B17, VCC[017] B18, VCC[018] B20, VCC[019] C9, VCC[020] C10, VCC[021] C12, VCC[022] C13, VCC[023] C15, VCC[024] C17, VCC[025] C18, VCC[026] D9, VCC[027] D10, VCC[028] D12, VCC[029] D14, VCC[030] D15, VCC[031] D17, VCC[032] D18, VCC[033] E7, VCC[034] E9, VCC[035] E10, VCC[036] E12, VCC[037] E13, VCC[038] E15, VCC[039] E17, VCC[040] E18, VCC[041] E20, VCC[042] F7, VCC[043] F9, VCC[044] F10, VCC[045] F12, VCC[046] F14, VCC[047] F15, VCC[048] F17, VCC[049] F18, VCC[050] F20, VCC[051] AA7, VCC[052] AA9, VCC[053] AA10, VCC[054] AA12, VCC[055] AA13, VCC[056] AA15, VCC[057] AA17, VCC[058] AA18, VCC[059] AA20, VCC[060] AB9, VCC[061] AC10, VCC[062] AB10, VCC[063] AB12, VCC[064] AB14, VCC[065] AB15, VCC[066] AB17, VCC[067] AB18

VCC[068] AB20, VCC[069] AB7, VCC[070] AC7, VCC[071] AC9, VCC[072] AC12, VCC[073] AC13, VCC[074] AC15, VCC[075] AC17, VCC[076] AC18, VCC[077] AD7, VCC[078] AD9, VCC[079] AD10, VCC[080] AD12, VCC[081] AD14, VCC[082] AD15, VCC[083] AD17, VCC[084] AD18, VCC[085] AE9, VCC[086] AE10, VCC[087] AE12, VCC[088] AE13, VCC[089] AE15, VCC[090] AE17, VCC[091] AE18, VCC[092] AE20, VCC[093] AF9, VCC[094] AF10, VCC[095] AF12, VCC[096] AF14, VCC[097] AF15, VCC[098] AF17, VCC[099] AF18, VCC[100] AF20

VCCP[01] G21, VCCP[02] V6, VCCP[03] J6, VCCP[04] K6, VCCP[05] M6, VCCP[06] J21, VCCP[07] K21, VCCP[08] M21, VCCP[09] N21, VCCP[10] N6, VCCP[11] R21, VCCP[12] R6, VCCP[13] T21, VCCP[14] T6, VCCP[15] V21, VCCP[16] W21

CPU_G21 — R108 0_4 — CPU_V6 — R159 0_4

<CRB>
R for test only

VCCA[01] B26, VCCA[02] C26 — +VCCA_PROC

VID[0] AD6, VID[1] AF5, VID[2] AE5, VID[3] AF4, VID[4] AE3, VID[5] AF3, VID[6] AE2

H_VID0 35, H_VID1 35, H_VID2 35, H_VID3 35, H_VID4 35, H_VID5 35, H_VID6 35

VCCSENSE AF7 — VCCSENSE 35

VSSSENSE AE7 — VSSSENSE 35

Merom Ball-out Rev 1a

<REV.NO. 0.5/REF.NO.19343>

Ivcc Max 52A

Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)

Ivcca Max 130mA

+1.05V_CPU

C250 C154 C153 C251 C249 C152 — .1U_6

+1.05V_CPU — R176 0_1210 — +1.05V

C280 330U_7343

<Check list>
ESR=12m ohm

<CRB>
.01U near to B26 ball

+1.5V — R386 0_6

VCC_CORE — C472 .01U_4 — C471 10U_8

R156 100_6

R160 100_6

<Demo board>
Routing 27.4ohm with 50mils spacing
PU/PD near to CPU 1"

U30D

VSS[001] A4, VSS[002] A8, VSS[003] A11, VSS[004] A14, VSS[005] A16, VSS[006] A19, VSS[007] A23, VSS[008] AF2, VSS[009] B6, VSS[010] B8, VSS[011] B11, VSS[012] B13, VSS[013] B16, VSS[014] B19, VSS[015] B21, VSS[016] B24, VSS[017] C5, VSS[018] C8, VSS[019] C11, VSS[020] C14, VSS[021] C16, VSS[022] C19, VSS[023] C2, VSS[024] C22, VSS[025] C25, VSS[026] D1, VSS[027] D4, VSS[028] D8, VSS[029] D11, VSS[030] D13, VSS[031] D16, VSS[032] D19, VSS[033] D23, VSS[034] D26, VSS[035] E3, VSS[036] E6, VSS[037] E8, VSS[038] E11, VSS[039] E14, VSS[040] E16, VSS[041] E19, VSS[042] E21, VSS[043] E24, VSS[044] F5, VSS[045] F8, VSS[046] F11, VSS[047] F13, VSS[048] F16, VSS[049] F19, VSS[050] F2, VSS[051] F22, VSS[052] F25, VSS[053] G4, VSS[054] G1, VSS[055] G23, VSS[056] G26, VSS[057] H3, VSS[058] H6, VSS[059] H21, VSS[060] H24, VSS[061] J2, VSS[062] J5, VSS[063] J22, VSS[064] J25, VSS[065] K1, VSS[066] K4, VSS[067] K23, VSS[068] K26, VSS[069] L3, VSS[070] L6, VSS[071] L21, VSS[072] L24, VSS[073] M2, VSS[074] M5, VSS[075] M22, VSS[076] M25, VSS[077] N1, VSS[078] N4, VSS[079] N23, VSS[080] N26, VSS[081] P3

VSS[082] P6, VSS[083] P21, VSS[084] P24, VSS[085] R2, VSS[086] R5, VSS[087] R22, VSS[088] R25, VSS[089] T1, VSS[090] T4, VSS[091] T23, VSS[092] T26, VSS[093] U3, VSS[094] U6, VSS[095] U21, VSS[096] U24, VSS[097] V2, VSS[098] V5, VSS[099] V22, VSS[100] V25, VSS[101] W1, VSS[102] W4, VSS[103] W23, VSS[104] W26, VSS[105] Y3, VSS[106] Y6, VSS[107] Y21, VSS[108] Y24, VSS[109] AA2, VSS[110] AA5, VSS[111] AA8, VSS[112] AA11, VSS[113] AA14, VSS[114] AA16, VSS[115] AA19, VSS[116] AA22, VSS[117] AA25, VSS[118] AB1, VSS[119] AB4, VSS[120] AB8, VSS[121] AB11, VSS[122] AB13, VSS[123] AB16, VSS[124] AB19, VSS[125] AB23, VSS[126] AB26, VSS[127] AC3, VSS[128] AC6, VSS[129] AC8, VSS[130] AC11, VSS[131] AC14, VSS[132] AC16, VSS[133] AC19, VSS[134] AC21, VSS[135] AC24, VSS[136] AD2, VSS[137] AD5, VSS[138] AD8, VSS[139] AD11, VSS[140] AD13, VSS[141] AD16, VSS[142] AD19, VSS[143] AD22, VSS[144] AD25, VSS[145] AE1, VSS[146] AE4, VSS[147] AE8, VSS[148] AE11, VSS[149] AE14, VSS[150] AE16, VSS[151] AE19, VSS[152] AE23, VSS[153] AE26, VSS[154] A2, VSS[155] AF6, VSS[156] AF8, VSS[157] AF11, VSS[158] AF13, VSS[159] AF16, VSS[160] AF19, VSS[161] AF21, VSS[162] A25, VSS[163] AF25

Merom Ball-out Rev 1a

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Quanta Computer Inc.

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NB(HOST)

D3A:(2/1) Change 965GM from ES sample to QS sample
Change U29 P/N from AJ0QN120T37 to AJ0QP200T09

U29A

HOST

CRESTLINE_1p0

+1.05V_GMCH

R86 221_4

H_SWING

R85 100_4

C137 .1U_4

<check list>
0.1U close to B3

H_RCOMP

R95 24.9_4

<check list>
10:20 mils(Width:Spacing)

R87 54.9_4

H_SCOMP

<check list>
Impedance 55ohm

R88 54.9_4

H_SCOMP#

<check list>
Impedance 55ohm

R392 1K_4

R391 2K_4

C473 .1U_4

<check list>
0.1U close to B9

H_AVREF
H_DVREF

H_CPURST#
H_CPUSLP#

H_D#[63:0]

H_A#[35:3]

H_A#[35:32] are not supported in
Calero Interposer
Crestline support 36 bit address

H_ADS#
H_ADSTB#_0
H_ADSTB#_1
H_BNR#
H_BPRI#
H_BREQ#
H_DEFER#
H_DBSY#
HPLL_CLK
HPLL_CLK#
H_DPWR#
H_DRDY#
H_HIT#
H_HITM#
H_LOCK#
H_TRDY#

H_DINV#[3:0]

H_DSTBN#[3:0]

H_DSTBP#[3:0]

H_REQ#[4:0]

H_RS#[2:0]

A1A:(9/20) remove R74 (0 ohm)

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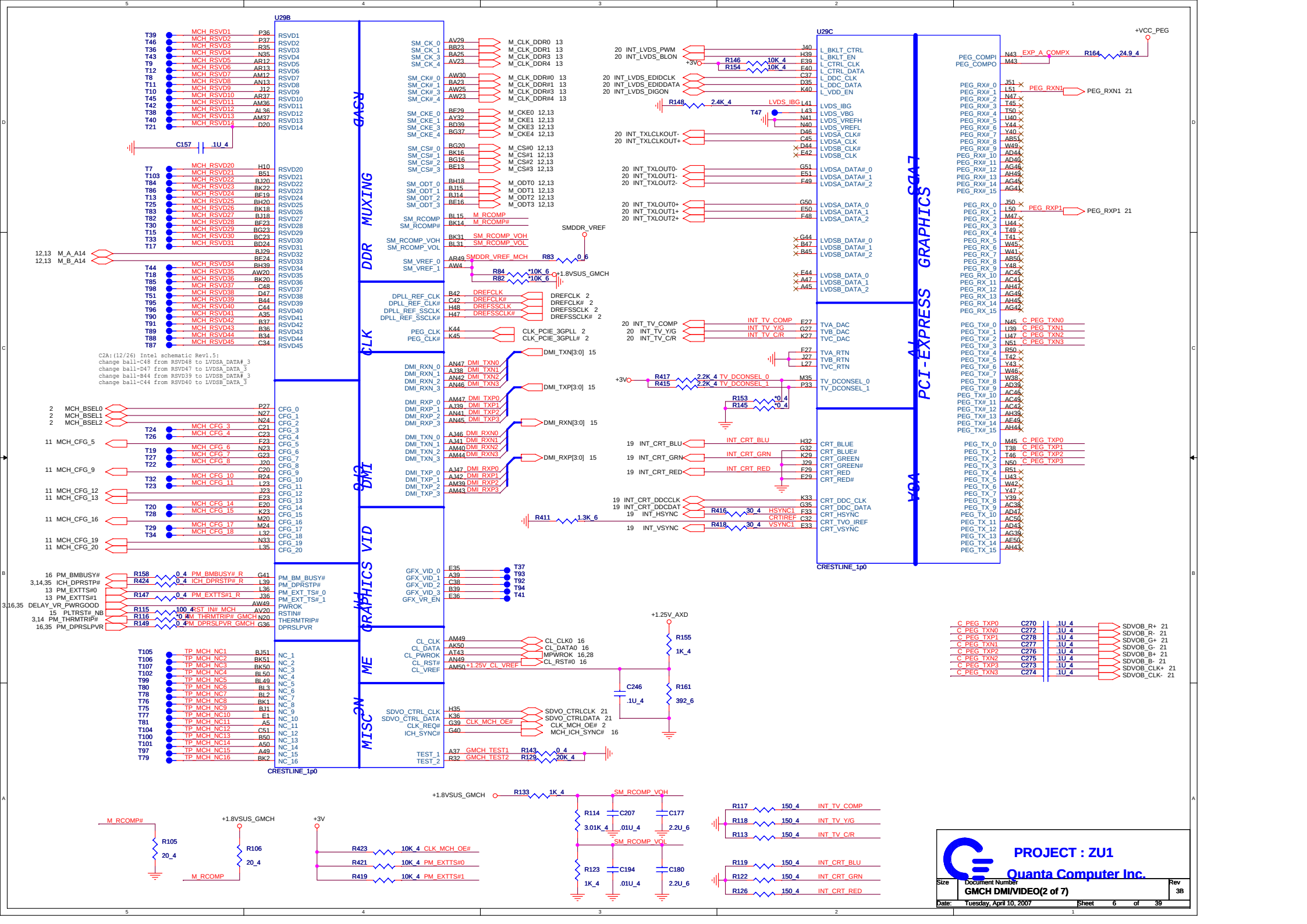
U29B
CRESTLINE_1p0
DMI
DDR MUXING
CLK
GRAPHICS VID
ME
MISC
U29C
CRESTLINE_1p0
PCI-EXPRESS GRAPHICS
SDVO
DMI_TXN[3:0] 15
DMI_TXP[3:0] 15
DMI_RXN[3:0] 15
DMI_RXP[3:0] 15
C2A:(12/26) Intel schematic Rev1.5:
change ball-C48 from RSVD48 to LVDSA_DATA#_3
change ball-D47 from RSVD47 to LVDSA_DATA_3
change ball-B44 from RSVD39 to LVDSB_DATA#_3
change ball-C44 from RSVD40 to LVDSB_DATA_3
+VCC_PEG
+1.25V_AXD
+1.8VSUS_GMCH
+3V
SMDDR_VREF
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Quanta Computer Inc.
GMCH DMI/VIDEO(2 of 7)
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Rev
3B
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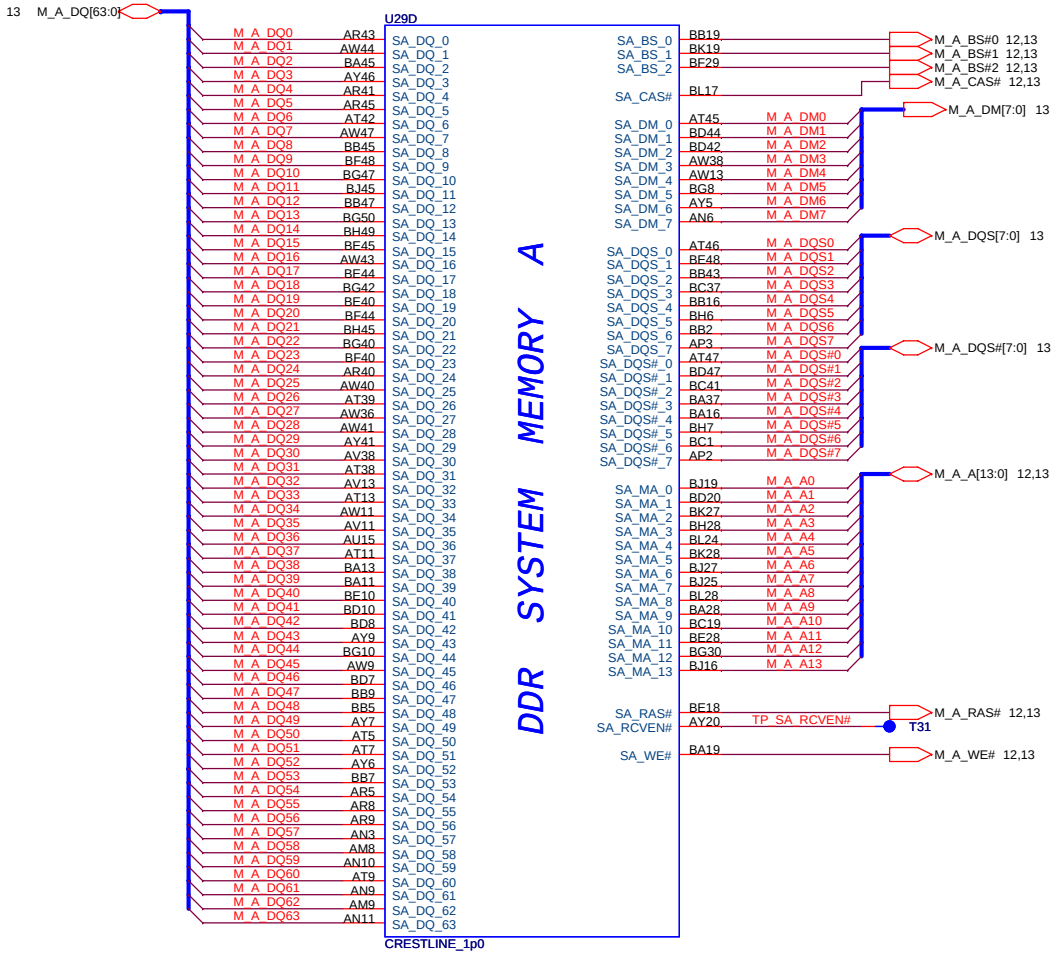
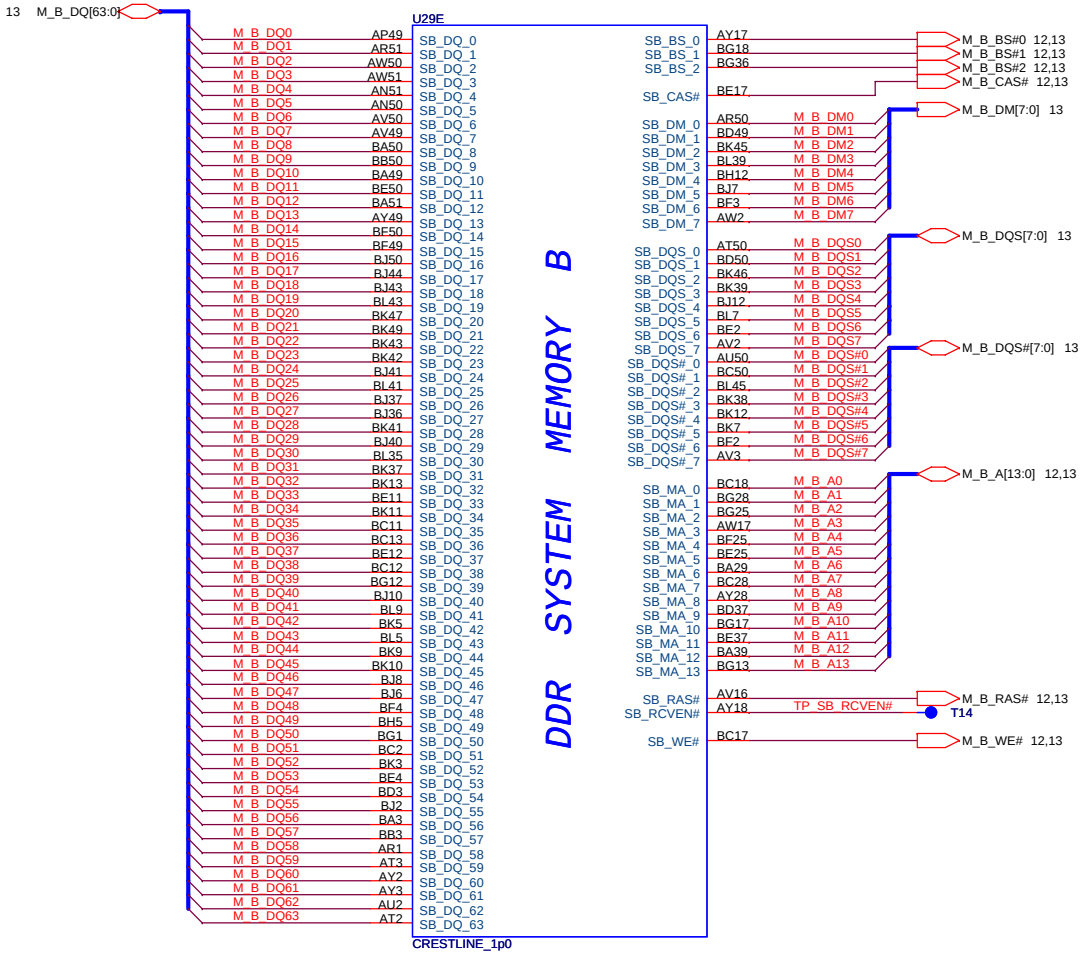
NB(Memory controller)





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Quanta Computer Inc.

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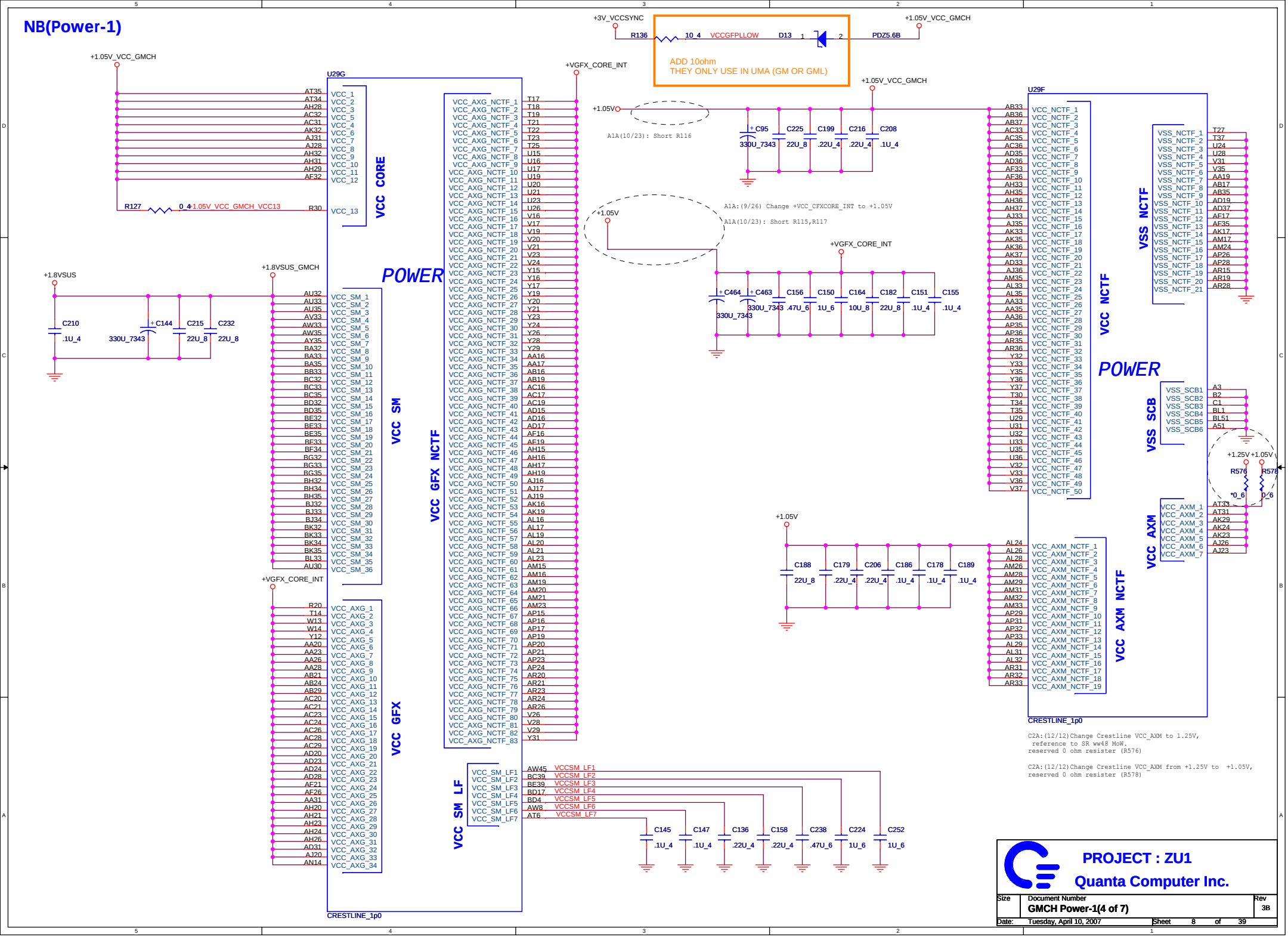
NB(Power-1)



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Quanta Computer Inc.		
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NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL INTERNAL

<Description>

+1.25V L53 10UH_8 C527 470U_7343 C262 .1U_4

+1.25V L25 10UH_8 C528 470U_7343 C264 .1U_4

+3V_VCCSYNC +3V R130 0_6 C205 .1U_4

<FAE>
INT VGA disable
VCCSYNC connect to GND

+3V L18 BKP1608HS181-T_6 C226 *22U_8 C522 .1U_4 C220 22N_4 R412 *0_4

+3V_TV_DAC R128 0_6 C505 .1U_4 C508 22N_4 R132 *0_4

<Description>

+1.25V L49 BKP1608HS181-T_6 C469 22U_8 C138 .1U_4

L50 BKP1608HS181-T_6 R384 0.5_6 C133 .1U_4

C465 22U_8 +1.25M_MPLL_RC

+1.25V R120 0_6 C143 100U_7343 C165 *22U_8 C159 4.7U_6 C176 22U_8 C168 1U_6

B1D:(12/9) change C143 from CH71002MJC8 to CH7102MT804 (Z-limit issue)

+1.25V R124 0_6 C200 *1U_6 C203 *1U_6 C213 22U_8 C201 .1U_4

+3V L51 BKP1608HS181-T_6 +3V_TV_DAC

C489 .1U_4 C487 22N_4 R404 *0_4

C488 .1U_4 C493 22N_4 R402 *0_4

C485 22U_8

C492 10U_8 C494 .1U_4 C495 22N_4 R401 *0_4

R131 *0_4

R138 0_6 +1.5V_VCCD_CRT +1.5V_VCCD_TVDAC

+1.5V_VCCD_QDAC

+1.25V R81 0_6 +1.25VM_MCH_VCCD_HPLL

C128 .1U_4 +1.25V_VCCD_PEG_PLL C259 .1U_4

+1.25V L24 BKP1608HS181-T_6

R168 1_8 C268 .1U_4

+V1.25S_PEGPLL_FB

C263 10U_8

+1.5V R137 0_6

C196 .1U_4 C214 22N_4

R125 100_6

C519 .1U_4 C511 22N_4 C507 1U_6

A1A:(10/18)
INTEL CRB VCCD_QDAC Filter Modification:
change L13 to R125(100ohm),
change R145(*0 ohm) to C507(1uF)

D3A:(01/02)
R125 shortage issue, Add 2nd source CS11003F953

D3A:(2/13)
Change R125 from CS11003B900 (100 ohm 0.1%) to CS11003J53(100 ohm 1%)

+1.8VSUS R163 0_6 +1.8V_VCCD_LVDS

C257 1U_6 C243 *10U_8

+3V_VCCA_CRT_DAC +3V_TV_DAC R128 0_6 C505 .1U_4 C508 22N_4 R132 *0_4

+3V_VCCA_DAC_BG

+1.25V_VCCA_DPLLA

+1.25V_VCCA_DPLLB

+1.25VM_VCCA_HPLL

+1.25VM_VCCA_MPLL

+1.8VSUS_VCC_TX_LVDS

+3V R166 0_8 C244 1000P_4 C266 .1U_4

+3V_VCCA_PEG_BG

+1.25V_VCCD_PEG_PLL

+1.25VM_VCCA_SM

+1.25VM_VCCA_SM_CK

+1.5V_VCCD_CRT

+1.5V_VCCD_TVDAC

+1.5V_VCCD_QDAC

+1.25VM_MCH_VCCD_HPLL

+1.25V_VCCD_PEG_PLL

U29H

CRESTLINE_1p0

J32	VCCSYNC		
A33	VCCA_CRT_DAC_1	CRT	
B33	VCCA_CRT_DAC_2		
A30	VCCA_DAC_BG		
B32	VSSA_DAC_BG		
B49	VCCA_DPLLA	PLL	
H49	VCCA_DPLLB		
AL2	VCCA_HPLL		
AM2	VCCA_MPLL		
A41	VCCA_LVDS	LVDS	
B41	VSSA_LVDS		
K50	VCCA_PEG_BG	PEG	
K49	VSSA_PEG_BG		
U51	VCCA_PEG_PLL		
AW18	VCCA_SM_1	SM	
AV19	VCCA_SM_2		
AU19	VCCA_SM_3		
AU18	VCCA_SM_4		
AU17	VCCA_SM_5		
AT22	VCCA_SM_7		
AT21	VCCA_SM_8		
AT19	VCCA_SM_9		
AT18	VCCA_SM_10		
AT17	VCCA_SM_11		
AR17	VCCA_SM_NCTF_1		
AR16	VCCA_SM_NCTF_2		
BC29	VCCA_SM_CK_1	CK	
BB29	VCCA_SM_CK_2		
C25	VCCA_TVA_DAC_1	TV	
B25	VCCA_TVA_DAC_2		
C27	VCCA_TVB_DAC_1		
B27	VCCA_TVB_DAC_2		
B28	VCCA_TVC_DAC_1		
A28	VCCA_TVC_DAC_2		
M32	VCCD_CRT	TV/CRT	
L29	VCCD_TVDAC		
N28	VCCD_QDAC		
AN2	VCCD_HPLL		
U48	VCCD_PEG_PLL		
J41	VCCD_LVDS_1	LVDS	
H42	VCCD_LVDS_2		
U13	VTT_1	VTT	
U12	VTT_2		
U11	VTT_3		
U9	VTT_4		
U8	VTT_5		
U7	VTT_6		
U5	VTT_7		
U3	VTT_8		
U2	VTT_9		
U1	VTT_10		
T13	VTT_11		
T11	VTT_12		
T10	VTT_13		
T9	VTT_14		
T7	VTT_15		
T6	VTT_16		
T5	VTT_17		
T3	VTT_18		
T2	VTT_19		
R3	VTT_20		
R2	VTT_21		
R1	VTT_22		
AT23	VCC_AXD_1	AXD	
AU28	VCC_AXD_2		
AU24	VCC_AXD_3		
AT29	VCC_AXD_4		
AT25	VCC_AXD_5		
AT30	VCC_AXD_6		
AR29	VCC_AXD_NCTF		
B23	VCC_AXF_1	AXF	
B21	VCC_AXF_2		
A21	VCC_AXF_3		
AJ50	VCC_DMI		
BK24	VCC_SM_CK_1	SM CK	
BK23	VCC_SM_CK_2		
BJ24	VCC_SM_CK_3		
BJ23	VCC_SM_CK_4		
A43	VCC_TX_LVDS		
C40	VCC_HV_1	HV	
B40	VCC_HV_2		
AD51	VCC_PEG_1	PEG	
W50	VCC_PEG_2		
W51	VCC_PEG_3		
V49	VCC_PEG_4		
V50	VCC_PEG_5		
AH50	VCC_RXR_DMI_1	DMI	
AH51	VCC_RXR_DMI_2		
A7	VTTLF1	VTTLF	
F2	VTTLF2		
AH1	VTTLF3		

+1.05V_GMCH

+1.25V_AXD

C142 4.7U_8 C126 4.7U_8 C148 2.2U_8 C134 .47U_6 C462 330U_7343

A1A(10/23): Short R122

+1.05V

R121 0_6 +1.25V

C187 1U_6 C195 *22U_8

R405 0_6 +1.25V

C477 1U_6 C475 10U_8

R165 0_6 +1.25V

C265 .1U_4

+1.25V_VCC_AXF

+1.25V_VCC_DMI

L19 1UH_8 +1.8VSUS_GMCH

C170 .1U_4 C211 22U_8

R134 1_6 +V1.8_SMCK_RC C233 22U_8

+1.8VSUS_VCC_SM_CK

+1.8VSUS_VCC_TX_LVDS

L21 1UH_8 +1.8VSUS

C239 1000P_4 C526 220U_7343

+3V_VCC_HV

+VCC_PEG

A1A: (9/20) Remove R138 0 ohm

L54 91nH +1.05V

C284 10U_8 C529 220U_7343

C129 .47U_4 C470 .47U_4 C146 .47U_4

<FAE>
VCC_RXR_DMI and VCC_PEG
connect to+1.05V

A1A: (9/20) Remove +VCC_RXR_DMI

+1.05V D8 2 1 PDZ5.6B1.05V_SD

R64 10_4

+3V R67 0_4

+3V_VCC_HV C112 .1U_4

<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

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Quanta Computer Inc.

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	GMCH Power-2(5 of 7)	3B
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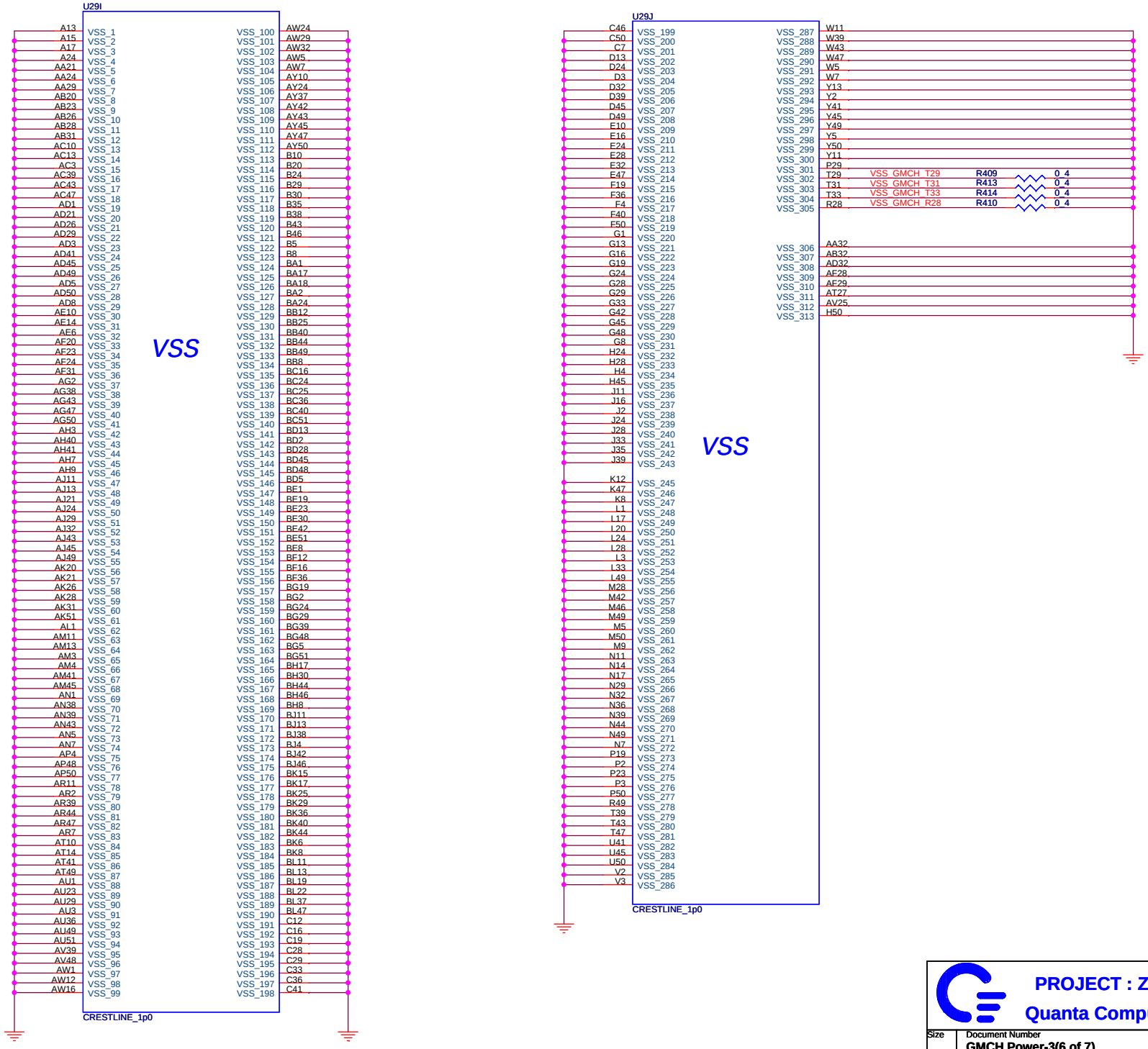
NB(Power-3)



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Strap table

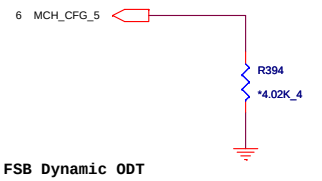
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

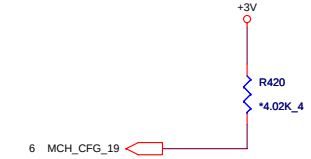
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

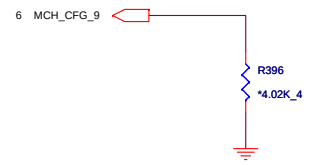


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

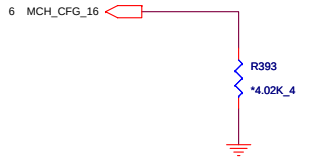


SDVO Present

Strap define at External DVI control page

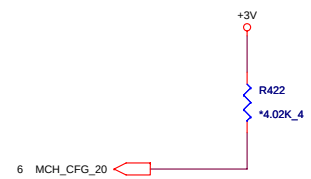
FSB Dynamic ODT

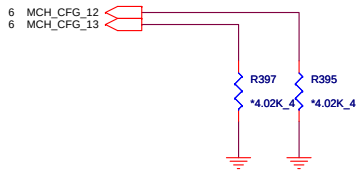
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





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DDR2 Dual channel A/B PU

M_A_A[13..0] → M_A_A[13..0] 7,13

M_B_A[13..0] → M_B_A[13..0] 7,13

DDRII A CHANNEL

SMDDR_VTERM

C160 .1U_4, C219 .1U_4, C163 .1U_4, C254 .1U_4, C212 .1U_4, C247 .1U_4, C162 .1U_4, C184 .1U_4, C241 .1U_4, C229 .1U_4, C260 .1U_4, C245 .1U_4, C161 .1U_4

DDRII B CHANNEL

SMDDR_VTERM

C255 .1U_4, C190 .1U_4, C166 .1U_4, C183 .1U_4, C167 .1U_4, C237 .1U_4, C248 .1U_4, C256 .1U_4, C209 .1U_4, C169 .1U_4, C253 .1U_4, C258 .1U_4, C204 .1U_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

M_A_A3	RP16	1	2	56X2	SMDDR_VTERM
M_A_A1		3	4		
M_A_A7	RP21	1	2	56X2	
M_A_A5		3	4		
M_A_A2	RP17	1	2	56X2	
M_A_A4		3	4		
M_A_A11	RP26	1	2	56X2	
6,13 M_CKE1		3	4		
M_A_A12	RP24	1	2	56X2	
M_A_A9		3	4		
	RP27	1	2	56X2	
7,13 M_A_BS#2		3	4		
6,13 M_CKE0					
M_A_A0	RP11	1	2	56X2	
7,13 M_A_BS#1		3	4		

M_B_A10	RP10	1	2	56X2	SMDDR_VTERM
7,13 M_B_BS#0		3	4		
M_B_A3	RP13	1	2	56X2	
M_B_A1		3	4		
M_B_A0	RP9	1	2	56X2	
7,13 M_B_BS#1		3	4		
M_B_A6	RP18	1	2	56X2	
M_B_A11		3	4		
M_B_A12	RP19	1	2	56X2	
M_B_A5		3	4		
M_B_A2	RP15	1	2	56X2	
M_B_A4		3	4		
M_B_A8	RP22	1	2	56X2	
M_B_A9		3	4		

M_A_A8	RP20	1	2	56X2	SMDDR_VTERM
M_A_A6		3	4		
	RP28	1	2	56X2	
6,13 M_CKE3		3	4		
7,13 M_B_BS#2					
	RP4	1	2	56X2	
7,13 M_A_BS#0		3	4		
6,13 M_ODT1					
	RP1	1	2	56X2	
6,13 M_ODT3		3	4		
6,13 M_CS#2					
M_A_A10	RP12	1	2	56X2	
7,13 M_A_CAS#		3	4		
	RP7	1	2	56X2	
7,13 M_A_WE#		3	4		
6,13 M_CS#1					
	RP8	1	2	56X2	
7,13 M_A_RAS#		3	4		
6,13 M_CS#0					
	RP5	1	2	56X2	
7,13 M_B_WE#		3	4		
7,13 M_B_CAS#					
M_B_A7	RP25	1	2	56X2	
6,13 M_CKE4		3	4		
	RP6	1	2	56X2	
6,13 M_CS#3		3	4		
7,13 M_B_RAS#					
	RP2	1	2	56X2	
6,13 M_ODT0	M_A_A13	3	4		
	RP3	1	2	56X2	
6,13 M_ODT2	M_B_A13	3	4		

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

6,13 M_A_A14	R144	56_4		SMDDR_VTERM
6,13 M_B_A14	R135	56_4		

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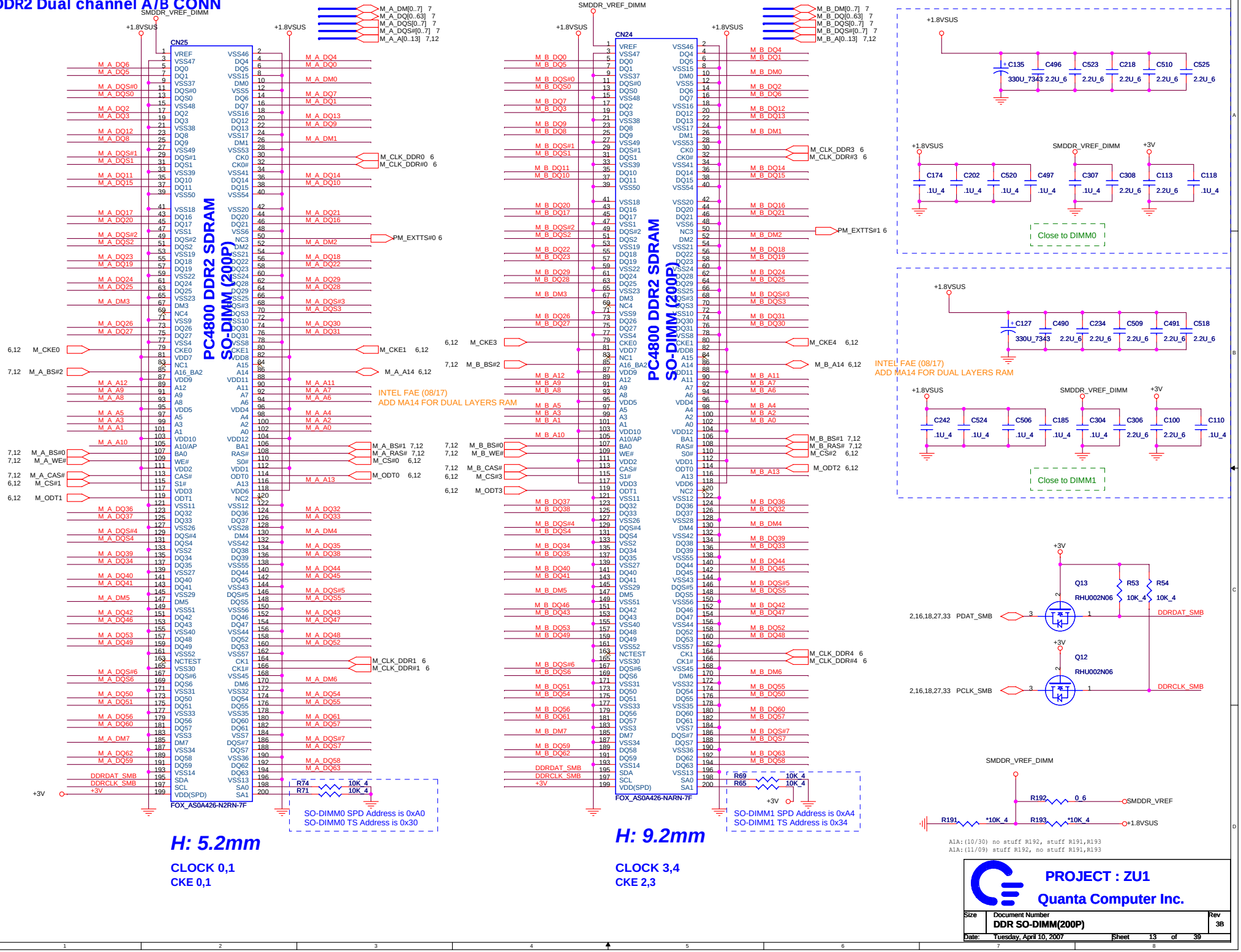
DDR2 Dual channel A/B CONN



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	DDR SO-DIMM(200P)	3B
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RTC

VCCRTC
+3VPCU
D23 CH500H-40 VCCRTC C328 1U_6
VCCRTC_4 D22 CH500H-40 R210 20K_6
<check list>
Delay 18~25ms
R205 1K_4
R246 1M_6
G1 *SHORT_PAD C363 1U_6
CN12 ACS_85204-0201
A1A: (9/24) change RTC CONN (follow ZC3)

CMOS Setting	G1
Clear CMOS	Short
Keep CMOS	Open

VCCRTC_3
+5VPCU
R201 1.2K_6 VCCRTC_1 R200 1K_4 VCCRTC_2
R202 4.7K_4
Q22 MMBT3904
R206 15K_4

CHANGE FROM 18PF TO 10PF
C548 10P_4
Y4 32.768KHZ
C547 10P_4
R231 10M_6

D3A:(2/1) Change ICH8M from ES sample to QS sample
Change U32 from AJ0QM740T31 to AJ0QN230T10

U32A

CLK_32KX1 AG25 RTCX1
CLK_32KX2 AF24 RTCX2
RTCRST# AF23 RTCRST#
SM_INTRUDER# AD22 INTRUDER#
ICH_INTVRMEN AF25 INTVRMEN
LAN100_SLP AD21 LAN100_SLP

A1A: 9/1 Remove GLAN

B24 GLAN_CLK
D22 LAN_RSTSYNC
C21 LAN_RXD0
B21 LAN_RXD1
C22 LAN_RXD2
D21 LAN_TXD0
E20 LAN_TXD1
C20 LAN_TXD2
AH21 GLAN_DOCK#/GPIO13
D25 GLAN_COMPI
C25 GLAN_COMPO

E3A:(3/30) Intel checklist Rev1.6
The GLAN_COMPO/GLAN_COMPI connection to 1.5-V rail through the resistor remains even if non-Intel LAN is used.
Stuff R232 (CS02492FB29)

+1.5V_PCIE R232 24.9_4 GLAN_COMP_SB

ACZ_BCLK AJ16 HDA_BIT_CLK
ACZ_SYNC AJ15 HDA_SYNC
ACZ_RST# AE14 HDA_RST#
31 ACZ_SDIN0 AJ17 HDA_SDIN0
31 ACZ_SDIN1 AH17 HDA_SDIN1
ACZ_SDIN2 AH15 HDA_SDIN2
T111 T63 ACZ_SDIN3 AD13 HDA_SDIN3
ACZ_SDOUT AE13 HDA_SDOUT
RST_RBAY# AE10 HDA_DOCK_EN#/GPIO33
RBAYON# AG14 HDA_DOCK_RST#/GPIO34

+3V +3V
R467 *10K_4 R289 *10K_4
RST_RBAY#
RBAYON#

29 SATA_LED# AF10 SATALED#

26 SATA_RXN0 C407 3900P_4 SATA_RXN0_C AF6 SATA0RXN
26 SATA_RXP0 C408 3900P_4 SATA_RXP0_C AF5 SATA0RXP
26 SATA_TXN0 C406 3900P_4 SATA_TXN0_C AH5 SATA0TXN
26 SATA_TXP0 C405 3900P_4 SATA_TXP0_C AH6 SATA0TXP

AG3 SATA1RXN
AG4 SATA1RXP
AJ4 SATA1TXN
AJ3 SATA1TXP

A1A: (9/20) Remove SATA1/SATA2

AF2 SATA2RXN
AF1 SATA2RXP
AE4 SATA2TXN
AE3 SATA2TXP

2 CLK_PCIE_SATA# AB7 SATA_CLKN
2 CLK_PCIE_SATA AC6 SATA_CLKP

R495 24.9_4 SATA_BIAS AG1 SATARBIAS#
AG2 SATARBIAS
<check list>
L<500mils

ICH8M REV 1.0

RTC: FWH0/LAD0 E5, FWH1/LAD1 F5, FWH2/LAD2 G8, FWH3/LAD3 F6, FWH4/LFRAME# C4, LDRQ0# G9, LDRQ1#/GPIO23 E6
LPC: A20GATE AF13, A20M# AG26, DPRSTP# AF26, DPSLP# AE26, FERR# AD24
GLAN / CPU: CPUPWRGD/GPIO49 AG29, IGNNE# AF27, INIT# AE24, INTR AC20, RCIN# AH14, NMI AD23, SMI# AG28, STPCLK# AA24, THRMTRIP# AE27, TP8 AA23
IHDA: DD0 V1, DD1 U2, DD2 V3, DD3 T1, DD4 V4, DD5 T5, DD6 AB2, DD7 T6, DD8 T3, DD9 R2, DD10 T4, DD11 V6, DD12 V5, DD13 U1, DD14 V2, DD15 U6
IDE: DA0 AA4, DA1 AA1, DA2 AB3, DCS1# Y6, DCS3# Y5, DIOR# W4, DIOW# W3, DDACK# Y2, IDEIRQ Y3, IORDY Y1, DDREQ W5

LAD0 27,28,30
LAD1 27,28,30
LAD2 27,28,30
LAD3 27,28,30
LFRAME# 27,28,30
LDRQ#0 30
LDRQ#1 T66
GATEA20 GATEA20 28
H_A20M# 3
H_DPRSTP# R R221 0_4 ICH_DPRSTP# 3,6,35
H_DPSLP# R R224 0_4 H_DPSLP# 3
H_FERR# 3
H_PWRGD_R R220 0_4 H_PWRGD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
RCIN# 28
H_SMI# R R219 0_4 H_NMI 3, H_SMI# 3
H_STPCLK# 3
H_THERMTRIP_R
ICH_TP8 T59
PDD[15:0] 26
PDA[2:0] 26
PDCS1# 26
PDCS3# 26
PDIOR# 26
PDIOW# 26
PDDACK# 26
IRQ14 26
PIORDY 26
PDDREQ 26

+1.05V_V_CPU_IO
R209 *56.2_4 R222 *56.2_4
R237 56.2_4
R212 56.2_4
R214 24_6 R211 *0_4 PM_THRMTRIP# 3,6
Placement close SB L<2"

E3A:(3/14)Change R214 from CS02403F908 to CS02403F916 (Lead free)

0810 UR FAE:
RCIN# DOESN'T NEED PU
R273 10K_4 R262 8.2K_4
RCIN#
GATEA20
A1A: (9/20) RCIN# PU 10K

SATA Disable

1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

VCCRTC
R227 332K_6
ICH_INTVRMEN
R228 *0_4
A1A: (9/20) Change INTVRMEN from PU to PD
B1C: (11/18) Change INTVRMEN from PD to PU

VCCRTC
R226 332K_6
LAN100_SLP
R241 *0_4
E3A:(4/3)Stuff R226(332K_6) and don't stuff R241 to enable Internal VR for VCCCL1_05 and VCCLAN1_05.
A1A: 9/1 Disable the internal VR powering VccLAN1_05, and VccCL1_05
D3A:(2/16)ICH8M Internal VR should not be disabled. no stuff R241, stuff R226
D3A:(2/28) Battery life issue. Disable ICH8M Internal VR (LAN) . stuff R241, no stuff R226 for C-build

+3V
R272 *1K_6
ACZ_SDOUT
ICH_TP3 16
R457 *1K_4

HDA

A1A: 9/6 base on Intel design guide, add it.

ACZ_SDOUT R282 33_4 ACZ_SDOUT_AUDIO 31
R283 33_4 ACZ_SDOUT_MDC 31
ACZ_SYNC R464 33_4 ACZ_SYNC_AUDIO 31
R465 33_4 ACZ_SYNC_MDC 31
ACZ_BCLK R462 33_4 BIT_CLK_AUDIO 31
R463 33_4 BIT_CLK_MDC 31
ACZ_RST# R268 33_4 ACZ_RST#_AUDIO 31,32
R267 33_4 ACZ_RST#_MDC 31

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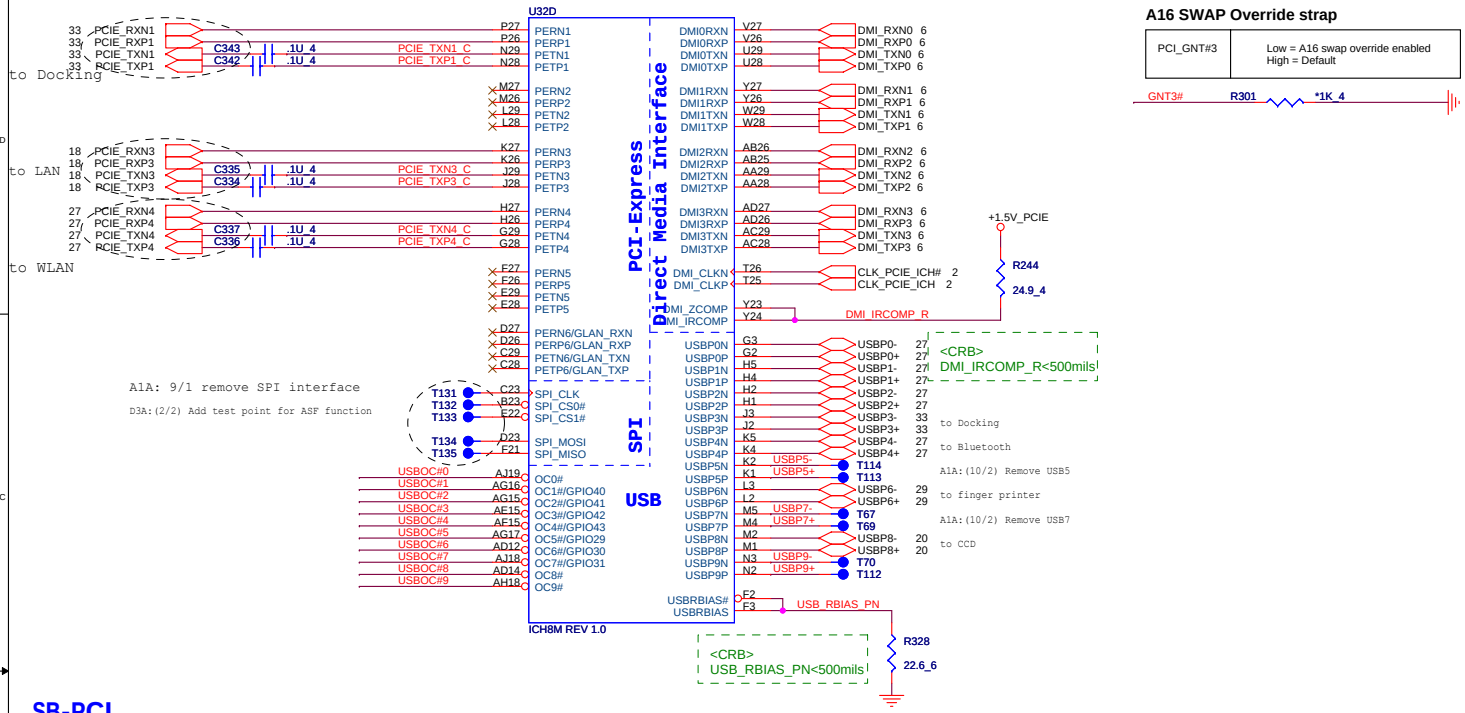
SB-PCIE/USB/DMI

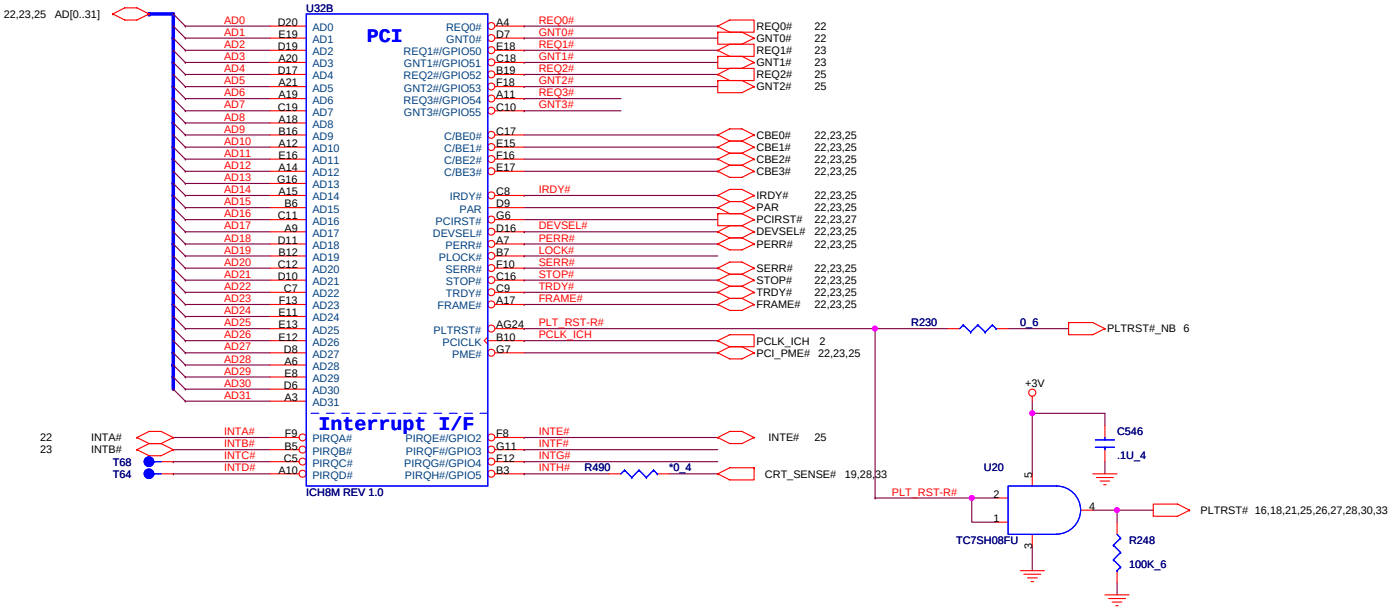


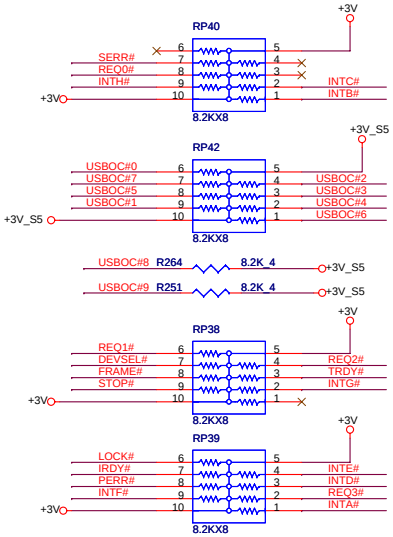
A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R301 *1K_4

SB-PCI





PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	3B

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SB-GPIO

D3A:(1/31) ASF issue:when iAMT is not implemented, ICH8M SMBus and SMLink should be connected together to support slave mode Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

A1A:(9/29) no support iAMT, remove SMB_CLK_ME,SMB_DATA_ME

U32C

ICH8M REV 1.0

SMB / SATA GPIO / Clocks / SYS GPIO / Power MGT / GPIO / Controller Link / MISC

SIO/ PC87383 DOES NOT NEED 32KHz

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

E3A:(3/26)
LAN_RST# should be terminated by 8.2-10 kΩ pull down resistor to GND if an Intelk 82566 MM/MC integrated LAN solution is not used.->
(1)Stuff 10k for R204
(2)Don't stuff R456
(3)Don't stuff R247

A1A:(9/16) Remove SUSM# used to control power planes to the Intel AMT sub-system

B1C:(11/20) short PWROK_EC to MPWROK

B1C:(11/29) no stuff R229,R233,C355

A1A:(9/11) Remove LAN_WOL_EN circuit

B1C:(11/24) add GPIO10 PU +3V,GPIO14 PD to GND

A1A:(9/26) Remove (1)ME_EC_ALERT# (2)EC_ME_ALERT

A1A:(9/26) change name from VR_PWRGD_CLKEN# to VR_PWRGD_CK410#

B1C:(11/24) add D43,D44 to stop leakage from EC to SB

B1C:(11/28) change DOCKIN# from GPIO7 to GPIO12

A1A:(9/26) Remove SATACLKREQ#

A1A:(9/11) Remove RI#

A1A:(9/26) Remove 2ND_MBCLK,2ND_MBDATA,Q11,Q12

A1A:(10/12) change from +3V to +3VSUS (Refer to ZC1)

A1A:(9/20) Refer to ZD1, Add ICH_PWROK circuit

A1A:(10/30) change DOCKIN#_ICH_R PU from +3V to +3V_S5

A1A:(9/29) no support iAMT, remove PU +3V_S5 circuit (R259/R258)

C2A:(12/21) no stuff R259 to prevent leakage issue

C2A:(12/12) Intel Suggest :ICH8M CPIO20 should not be pulled HIGH. Remove BOARD_ID3 circuit(remove R474,R475)

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

INTEL CRB: PU +3V

BIOS/ ERIC: UNSTUFF

ECN 2A
INTEL CRB V1.301
CL_RST# NO NEED PU.

INTEL CRB NEED THOSE PU & PD.

INTEL CRB SHOW IT

INTEL CRB SHOW IT

DISABLE LAN: STUFF

INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"

TO ICH8

FROM uR(EC)

Board ID	ID3	ID2	ID1	ID0
With EZ Dock	0	0	0	0
W/O EZ Dock	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

Size	Document Number ICH8M GPIO(3 of 4)		Rev 3B
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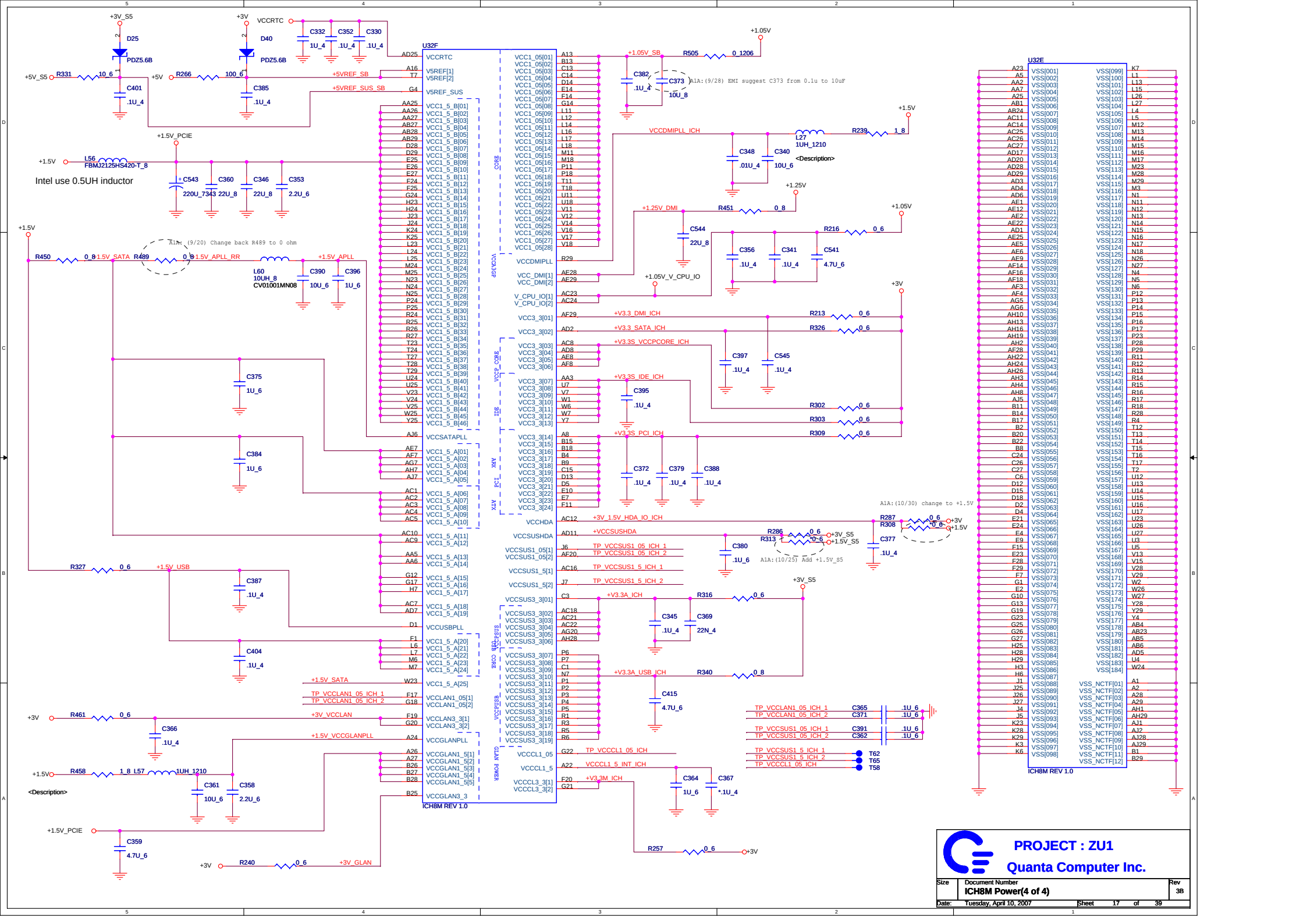
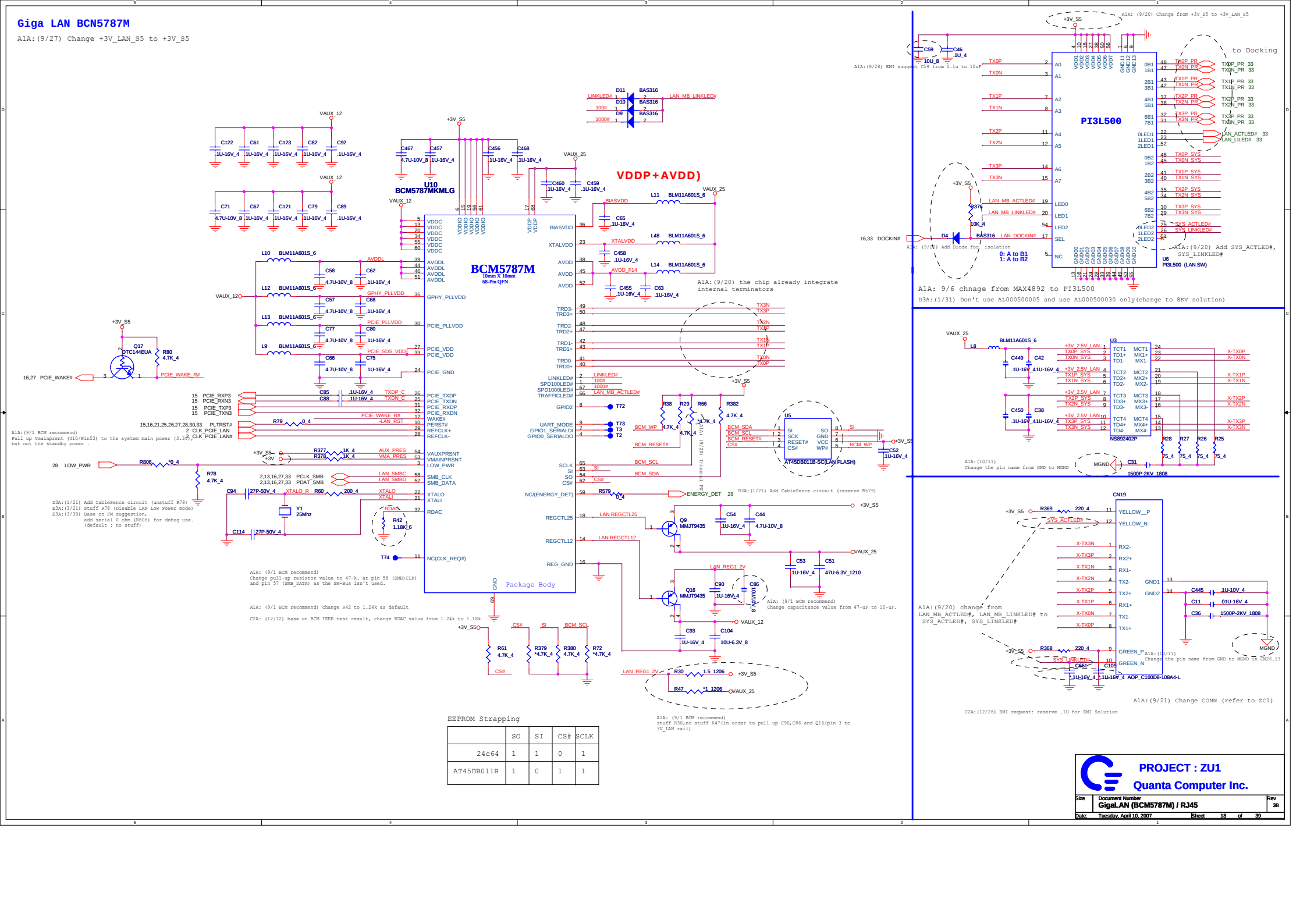

U32F
ICH8M REV 1.0
U32E
ICH8M REV 1.0
PROJECT : ZU1
Quanta Computer Inc.
ICH8M Power(4 of 4)
Rev 3B
Tuesday, April 10, 2007
Sheet 17 of 39
Intel use 0.5UH inductor
A1A: (9/20) Change back R489 to 0 ohm
A1A:(9/28) EMI suggest C373 from 0.1u to 10uF
A1A:(10/30) change to +1.5V
A1A:(10/25) Add +1.5V_S5
<Description>

Giga LAN BCN5787M

A1A:(9/27) Change +3V_LAN_S5 to +3V_S5



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GigaLAN (BCM5787M) / RJ45	3B

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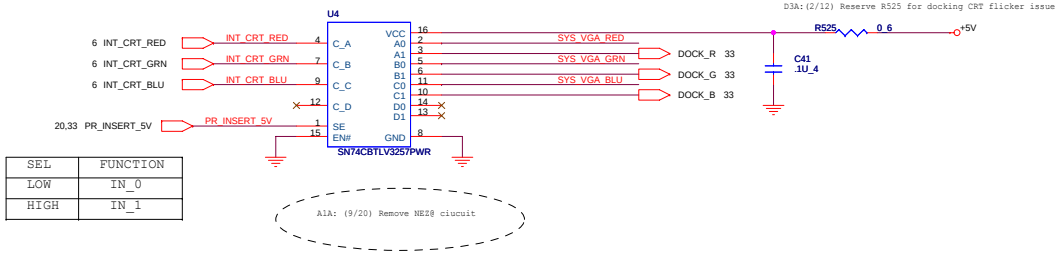
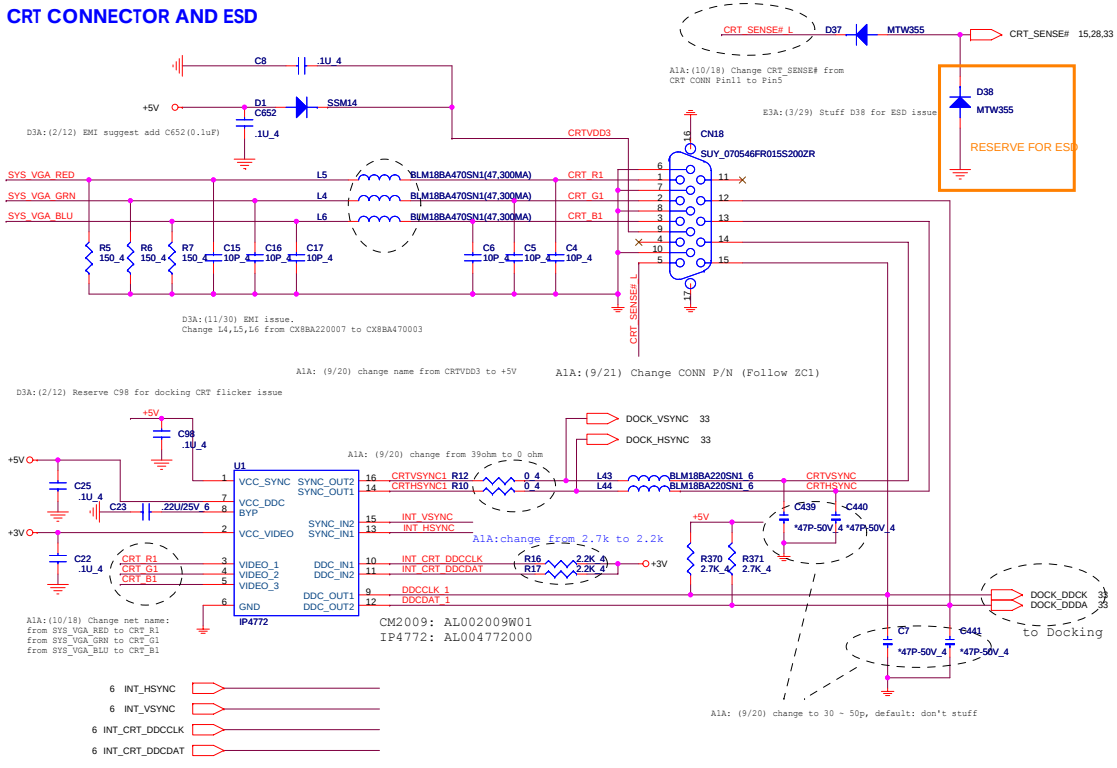
CRT Select



SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

CRT CONNECTOR AND ESD



PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	CRT	3B
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LVDS

B1C: (11/20)
(1) change PWM control from 965GM to EC
(2) Short L7, un-stuff C28 (L-C filter will impact PWM signal)
(3)stuff R13,no stuff R15

C2A:(12/28) EMI request: reserve L-C footprint for debug use (R52,C650)
D3A:(2/12) Stuff R15, Change PWM control from EC to 965GM
D3A:(2/14) Acer inform no support DPST in C build, remove R15

A1A:(10/2) change from USB7 to USB8

A1A: (9/20) Come from 965GM for PWM control

E3A:(3/15) Link C650 from DMIC-CLK to DMIC-CLK_1

A1A(10/5):Change C12 from CH6102M9900 to CH61004M3E5 (refer to ZC3)
E3A:(4/3) EOL issue change from CH61004M3E5 to CH61004M398

A1A: (9/20) Change LVDS CONN to 30pin
(9/21)change footprint to 88242-3000-30P-RUV

<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
8/27 change back to 100K

D3A:(2/12)
change U2 from AL004280000(AAT4280IGU-3-T1) to AL004280018(AAT4280IGU-1-T1).
rise time of LCDVCC is >0.5ms and <=10ms.
AL004280018 can meet this spec

E3A:(3/14)Change MB LCD connector pin define(CN2) and LCD cable pin define to cover production line issue
(Inverter short with signal to burn system)->ZR1 issue
(1)pin 27,29->NC
(2)pin 28,30->INVCC(VIN)->same as C build
(3)pin 8->INT_LVDS_EDIDDATA

CAMERA MODULE

BECAUSE UR'S SUGGESTION,
ACTICE CHANGE FROM LOW TO HIGH.

TV Out (SVHS) MiniDIN 7-pin

SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

A1A: (9/20) Remove "NEZ@" circuit

A1A:(9/21) Change CONN (Follow ZC1)

MR Sensor

D3A:(2/12) Follow ZO1 design,
Remove R24 footprint, DEL D3(BC000316Z07).
Add R73,Q36,Q37

D3A:(2/12) system sometimes will no backlight issue .
For short term solution:
change R22 from 10k(CS31002JB28) to 1K (CS21002FB24)

Project	PROJECT : ZU1
Company	Quanta Computer Inc.
Size	B
Document Number	LVDS/MR senseor/SVIDEO
Rev	3B
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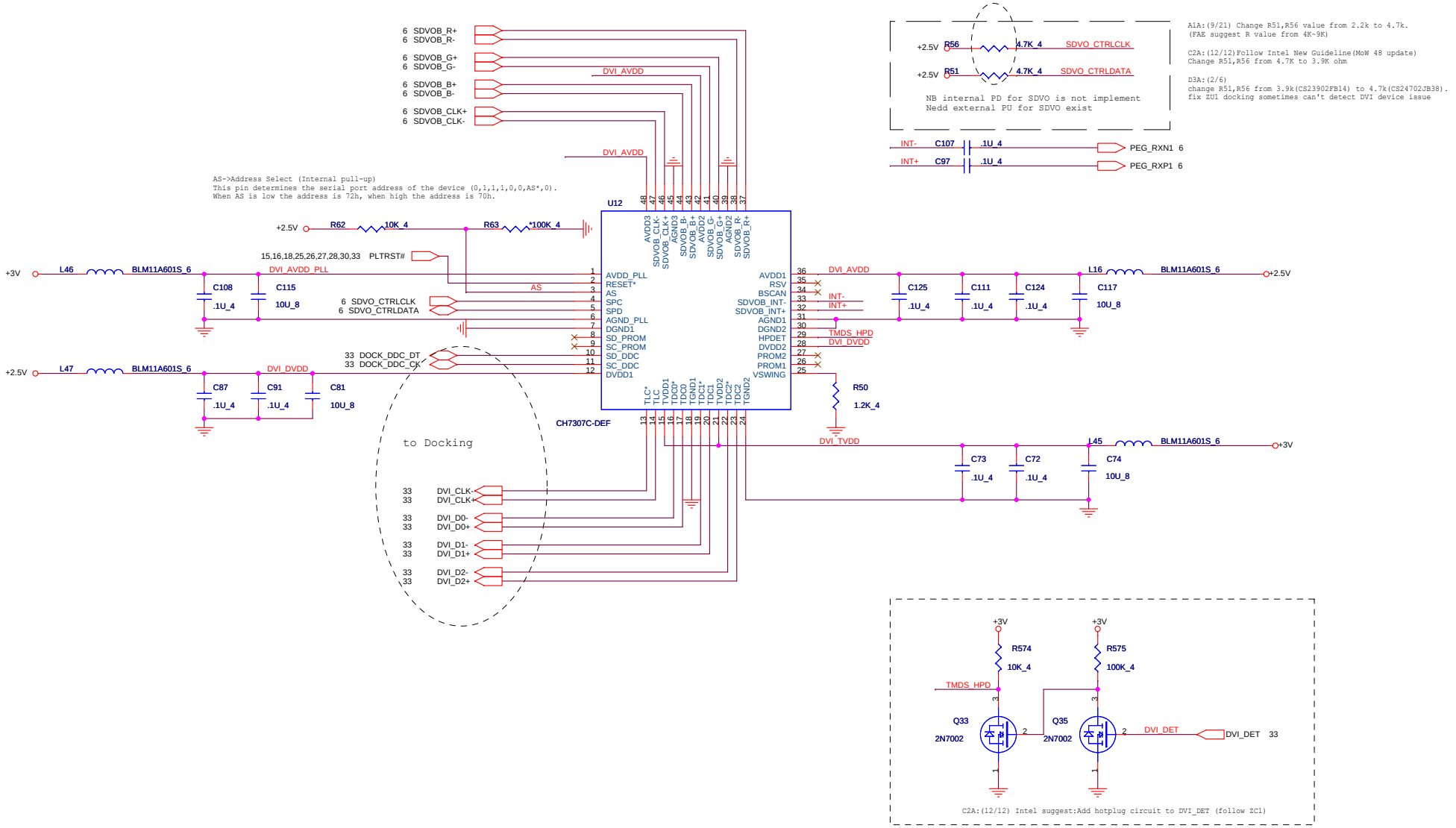
SDVO-DVI



D3A:(1/30) remove U13,R68,R75,R73,C98
1/16 confirm with CHRONTEL FAE,
he said we can remove CH9901 (U13),
If ZU1 need support HDCP,
just need change controller from CH7307 to CH7313.
CH7313 already integrated HDCP function, no need external EEPROM.

C2A:(12/22) confrim with FAE ->
Due to Intel VBIOS already integrate the EEPROM function.
ZU1 will remove the U11,R57,R52,C109 to save layout space.

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	DVI (CH7307)	3B
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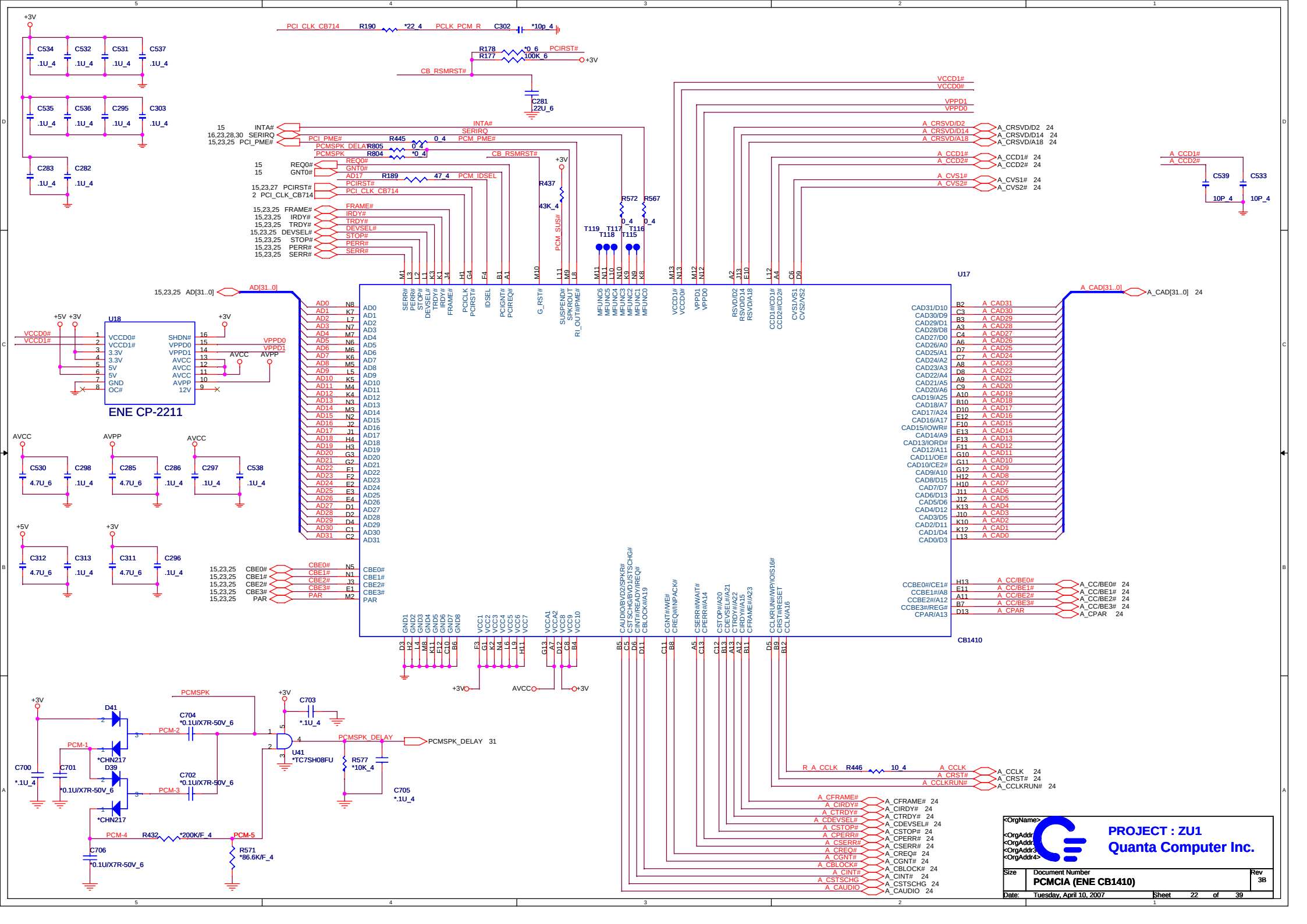
ENE CP-2211
U17
CB1410
U18
U41
*TC7SH08FU
PROJECT : ZU1
Quanta Computer Inc.
PCMCIA (ENE CB1410)
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ID Select : AD18
Interrupt Pin : INTB#
Request Indicate : REQ1#
Grant Indicate : GNT1#

GRST# should connect to Power On reset if support S3

A1A:(9/22) no stuff R496,R522

48MHz Clock

A1A:(9/26) Add 22ohm for R490 and 10p for C839
Change Y7 from 50MHz to 48MHz

A1A:(9/28) base on EMI suggest: remove R490,C839

A1A:(9/22) XMDAT4B is for 8 bit MMC,remove it.

D3A:(2/12)
(1)no stuff 43K(CS34302JB19):
R562,R527,R533,R538,R539,R565,R561,R540,R498,R497,R500,R552,R555
(2)no stuff 10k(CS31002JB28) : R560
(3) Change R547 from 43k (CS34302JB19) to 8.2k (CS28202JB14)
(4)Change R528 from 10K(CS31002JB28) to 43K(CS34302JB19)

A1A:(9/22) FAE suggest R value under 47 ohm.

A1A:(9/22) Add PU/PD resister

A1A:(9/26) For EMI solution
(close to MR510)

A1A:(9/26) For EMI solution

Size	Document Number		Rev
	Card Reader (MR510)		3B
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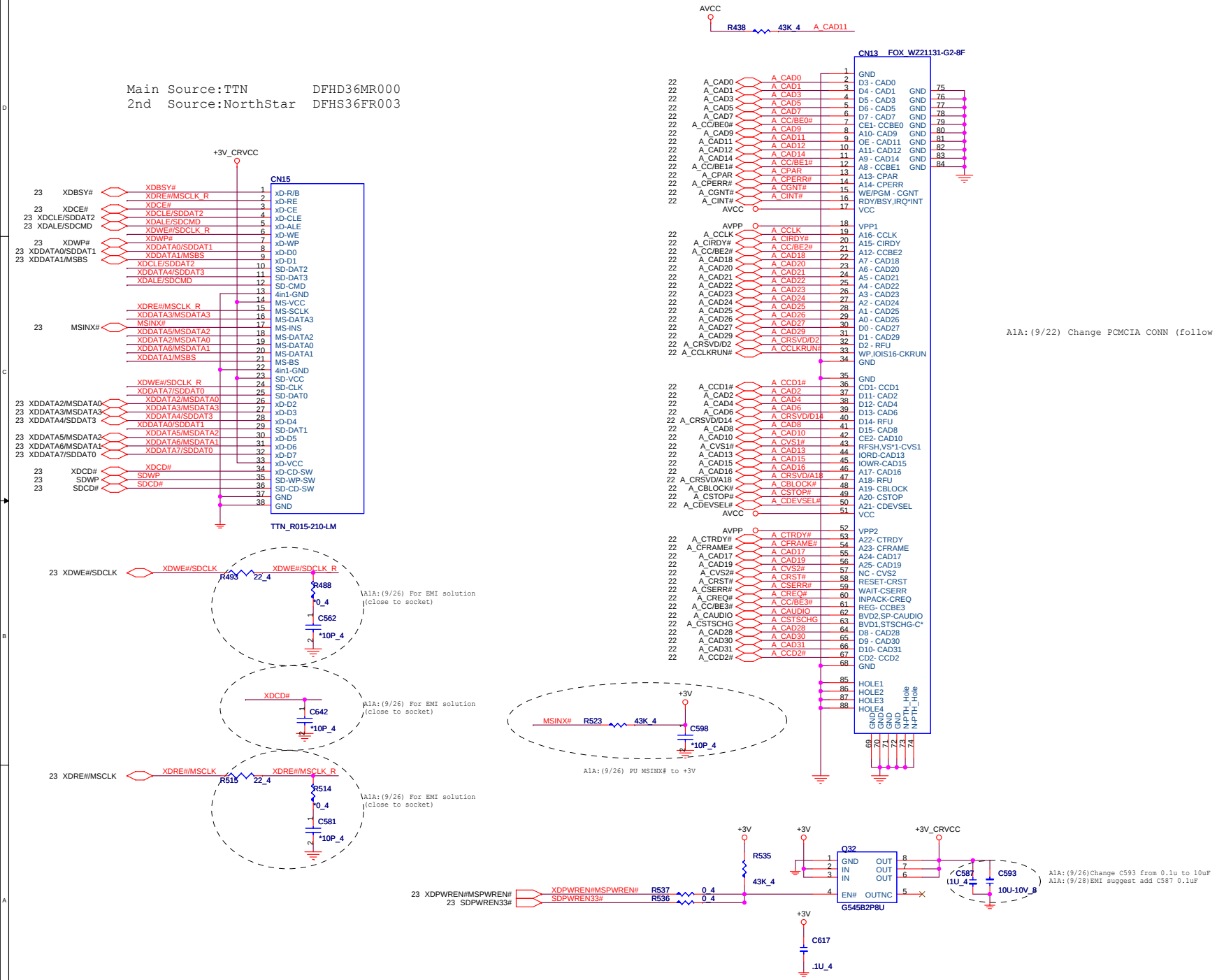
PROJECT : ZU1
Quanta Computer Inc.

Main Source:TTN DFHD36MR000
2nd Source:NorthStar DFHS36FR003



PROJECT : ZU1		
Quanta Computer Inc.		
Size	Document Number: CARD Reader & PCMCIA SLOT	Rev: 3B
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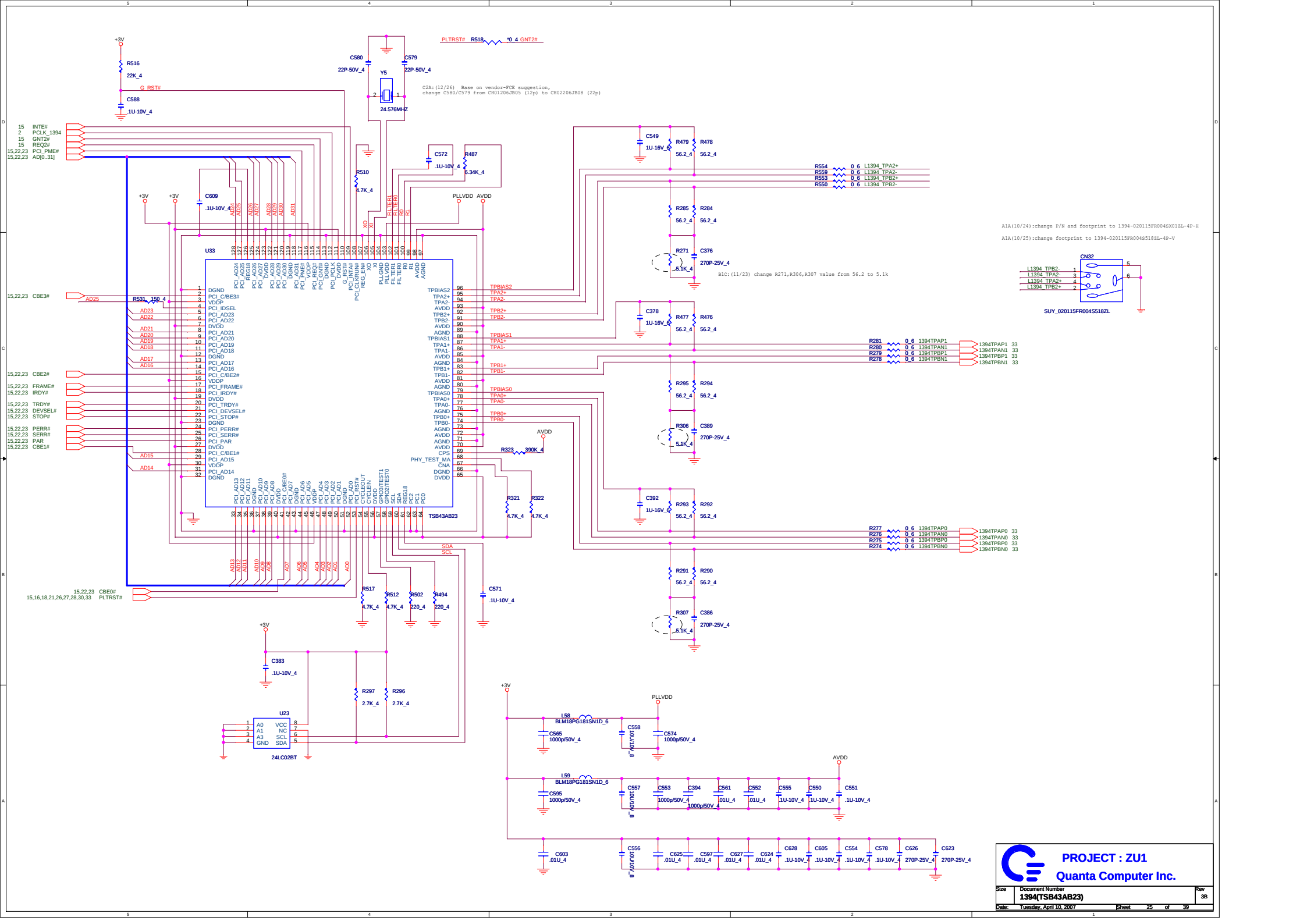
U33
TSB43AB23
U23
24LC02BT
Y5
24.576MHZ
CN32
SUY_020115FR004S518ZL
PROJECT : ZU1
Quanta Computer Inc.
1394(TSB43AB23)
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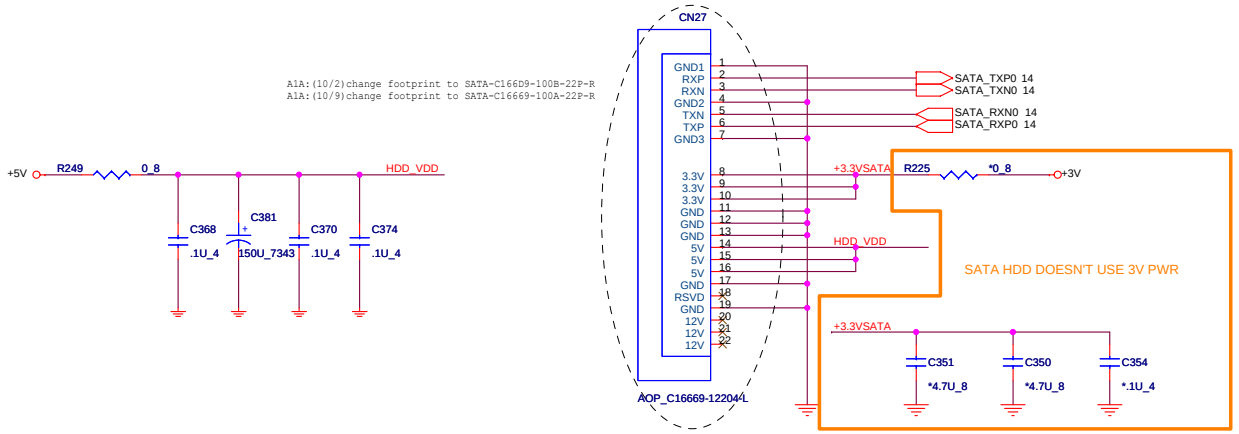
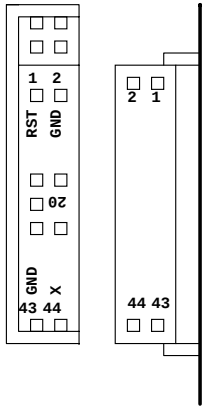
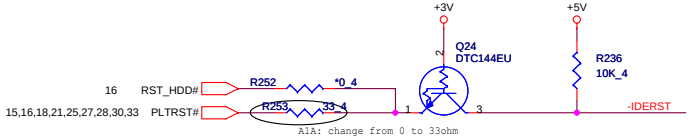
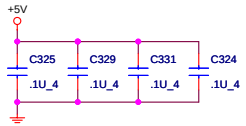
SATA HDD





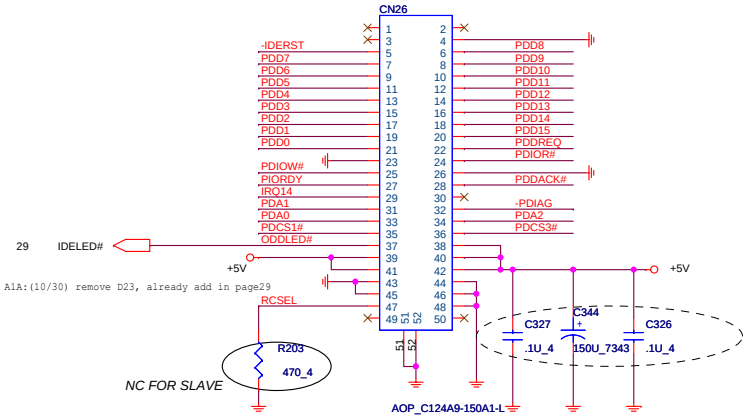
PATA ODD

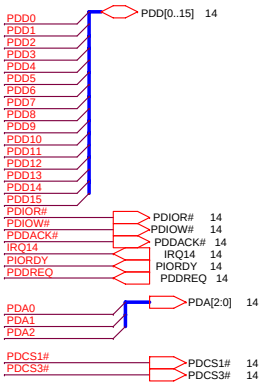


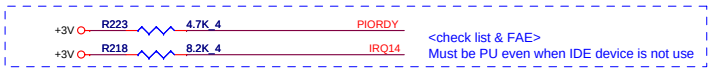


A1A:(9/29) change footpint: CDR-C124A9-100C-50P

ODD Connector







PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD & PATA-ODD	3B
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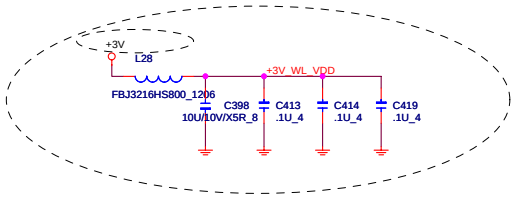
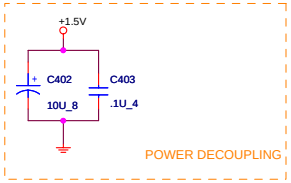
MINI-Card

A1A: (9/20) Change from +3V to +3V_WL_VDD
A1A: (10/23)change +3V to +3VSUS
B1C: (10/23)change from +3VSUS to +3V





D3A:(1/21) Stuff R349,R350 for debug use

A1A:9/4 Reserved for debug only

15,22,23 PCIRST#
2,30 PCI_CLK_SIO
PCIRST# R349 0_4 CL_DATA1_CN
PCLK_SIO R350 0_4 CL_CLK1_CN

B1C:(11/29) no stuff R353,R348,R356

16 CL_RST#1 R353 *0_4 CL_RST#0_CN
16 CL_DATA1 R348 *0_4 CL_DATA1_CN
16 CL_CLK1 R356 *0_4 CL_CLK1_CN
R354 0_4 KEDRON_GND_43
R351 0_6 KEDRON_VCC
+3V_WL_VDD R352 R355 0_4 KEDRON_GND_37

A1A(10/30): Add (CN28/Pin39,41) to +3V_WL_VDD (follow ZO1)

15 PCIE_TXP4
15 PCIE_TXN4
15 PCIE_RXP4
15 PCIE_RXN4
PCIE_RXP4
PCIE_RXN4
A1A:(10/20) Remove 0.1uF *2pcs
28 uR_SOUT_CR
28 uR_SWD

+3VSUS
2 CLK_PCIE_MINI1
2 CLK_PCIE_MINI1#
Q25
*DTC144EU
R357
*4.7K_4
16,18 PCIE_WAKE#
PCIE_WAKE#_MINI-Card

E3A:(3/16) Base on Acer demand, remove wake on lan for Mini PCIE function. no stuff Q25,R357

+1.5V
0_4 R336 +1.5V_MINI-Card
+3V_WL_VDD +3V_WL_VDD
A1A:(10/30)change form +3VSUS to +3V_WL_VDD
C424 10U_8
C422 .1U_4

CN28
Reserved 51
Reserved 49
Reserved 47
Reserved 45
Reserved 43
Reserved 41
Reserved 39
Reserved 37
Reserved 35
GND
PETp0
PETn0
GND
GND
PERp0
PERn0
GND
Reserved 21
Reserved 19
Reserved 17
GND 15
REFCLK+ 13
REFCLK- 11
GND 9
CLKREQ# 7
Reserved 5
Reserved 3
WAKE# 1
+3.3V 52
GND 50
+1.5V 48
LED_WPAN# 46
LED_WLAN# 44
LED_WWAN# 42
GND 40
USB_D+ 38
USB_D- 36
GND 34
SMB_DATA 32
SMB_CLK 30
+1.5V 28
GND 26
+3.3Vaux 24
PERST# 22
Reserved 20
GND 18
Reserved 16
Reserved 14
Reserved 12
Reserved 10
Reserved 8
+1.5V 6
GND 4
+3.3V 2
ACS_88911-5204

A1A: (9/26) Remove (CN28/Pin46)BT_LED
WIRELESS_LED# 29
B1C:(11/13) Robson ES1 to ES2 change. PIN 37 => GND
A1A: (9/20) Remove USB circuit
B1C:(11/20) need support BCM module PIN 40 => GND
MINI_DAT_SMB
MINI_CLK_SMB
RF_EN_RR R343 0_4 PLTRST# 15,16,18,21,25,26,28,30,33
RF_EN 28
R337 0_4 LFRAME# 14,28,30
R345 0_4 LAD3 14,28,30
R341 0_4 LAD2 14,28,30
R338 0_4 LAD1 14,28,30
R339 0_4 LAD0 14,28,30
A1A:9/4 Reserved for debug only

B1D:(12/9) change from 9.0mm to 9.9mm (ME request)

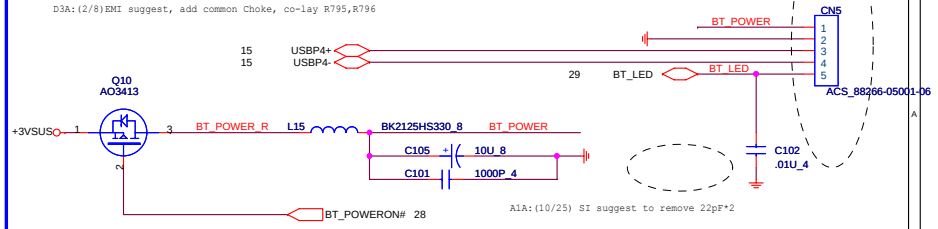
+3V
Q14 RHU002N06
R48 10K_4
2,13,16,18,33 PDAT_SMB
MINI_DAT_SMB

+3V
Q15 RHU002N06
R58 10K_4
2,13,16,18,33 PCLK_SMB
MINI_CLK_SMB

BLUETOOTH MODULE CONNECTOR

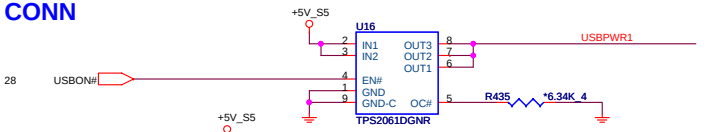
A1A: (9/25) change CONN (follow ZH3)

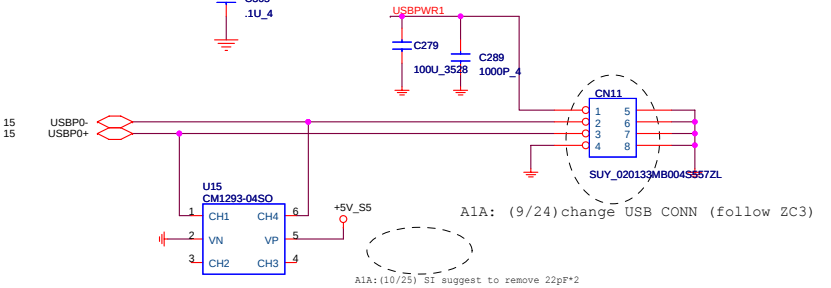
D3A:(2/8)EMI suggest, add common Choke, co-lay R795,R796



A1A:(10/25) SI suggest to remove 22pF*2

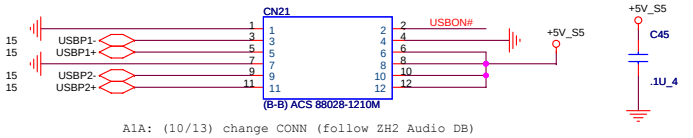
USB CONN





A1A: (9/24)change USB CONN (follow ZC3)

A1A:(10/25) SI suggest to remove 22pF*2



A1A: (10/13) change CONN (follow ZH2 Audio DB)

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Mini card/USB/Bluetooth	3B
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A1A:(9/16)Change from WPC8769 to WPC8763

A1A: (9/25) change VBAT from +3VPCU to +A3VPCU

1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC

1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick!
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.

A1A: (9/25) place the above capacitors as close to the pins as possible

08/10 FAE: SMI DOESN'T NEED DIODE

FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.

08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.

A1A: (9/25)
FAE: PUT Y6 with EC in the same side

A1A:(9/27)change C130,C131 from 6.8p to 5.6p

1/13 Comfirm by vendor mail :
Connect to AGND

C2A:(12/26) Base on vendor-FCE suggestion,
change C130/C131 from CH-5606TB01 (5.6p) to CH01006JBD1 (10p)

A1A: (9/26) Add HWPG_CPUIO

C2A:(12/25) Steven:D16 not necessary if 3V/5V fail, EC can't work.
This monitor circuit is't necessary.

E3A:(3/16)PE request move D15~D18 location for FFC cable issue.Remove D16 footprint and net (HWPG_3/5VPCU) to save layout space.

A1A: (9/26) Add it. Capacitors as close to EC as possible

E3A:(3/15) ICMNT connect to EC pin100(AD pin for power control) , reserve R570 0ohm for debug use

B1C:(10/20)SWAP GPIO1 & GPIO3 (follow EC team)
A1A:(9/29)SWAP GPIO3 & GPIO6 (follow EC team)

A1A: (9/26) Remove BL/C#

08/10 FAE: ADD TP FOR DEBUG

CCD_POWERON ACITVE LO => HI

A1A: (9/26) Remove MY16

A1A: (9/26) Remove LAN_WOL_EN

A1A: (9/26) Remove REAYINS#

A1A: (9/26) Remove LAN_ON
A1A: (9/26) Remove EC_ME_ALERT

C2A:(12/12)FAE suggest add 22 Ohm dumping resistors on SPI flash interface F_SCK(pin92) and F_SDO(pin87) to avoid potential EMI problem

0~AVCC power for DA pin power reference

08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.

SM BUS PU

MBCLK	R98	4.7K_4	+3VPCU
MBDATA	R99	4.7K_4	
2ND_MBCLK	R102	4.7K_4	
2ND_MBDATA	R100	4.7K_4	
EC_GPIO42	R139	4.7K_4	+3V
CRT_SENSE#	R398	4.7K_4	

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0	CCD_POWERON#	R408	10K_4
BADDR1	SOUT_CR_DEBUG	R407	*10K_4
SHBM	RF_EN	R399	10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ACER ID

A1A:(9/29) change from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA

U7 24LC08 — SCL, SDA, A0, A1, A2, WP, VCC, GND — +3VPCU — C69 .1U_4

D3A:(1/21) Add CableSence circuit

D3A:(1/31) Anda inform: change LAN Low power pin from GPIO47 to GPIO52

SPI FLASH

U26 W25X80VSSIG — SO, SI, SCK, CE, VDD, HOLD, WP, VSS — +3VPCU — R45 10K_4 — C454 .1U_4

SPI_SDI_uR	
SPI_SDO_uR_R	
SPI_SCK_uR_R	
SPI_CS0#_uR	

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

BUTTON ON KEYBOARD MATRIX

MX0	MX0 29
MX1	MX1 29
MX2	MX2 29
MX3	MX3 29
MX4	WIRELESS_SW# 29
MX5	BLUETOOTH_SW# 29
MY16	MY16 29

DEBUG PORTS

B1C:(11/28) change CN10/pin1 from +3V to +3VPCU

EC Debug Port

+3VPCU — SOUT_CR_DEBUG, SWD_DEBUG — CN10 *ACS_88231-04001

LPC debug card

A1A(10/5):Change LPC debug CONN to DFFC10FR103

E3A:(3/22) confirm with BIOS-CM, no need LPC dedug CONN, Remove CN6,R432 footprint to save space for layout.

INTERNAL KEYBOARD STRIP SET

+3VPCU — MY0 — R110 10K_4

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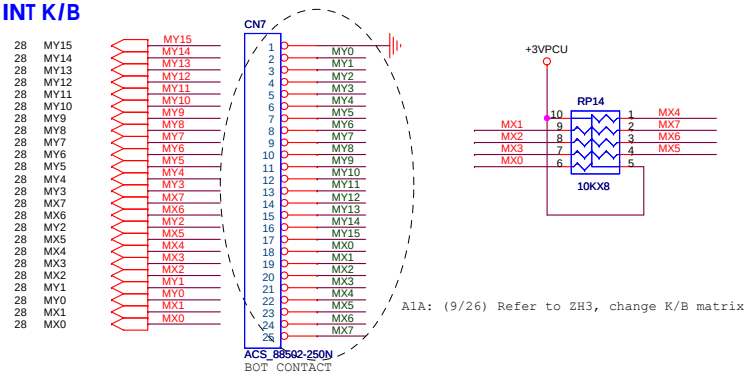
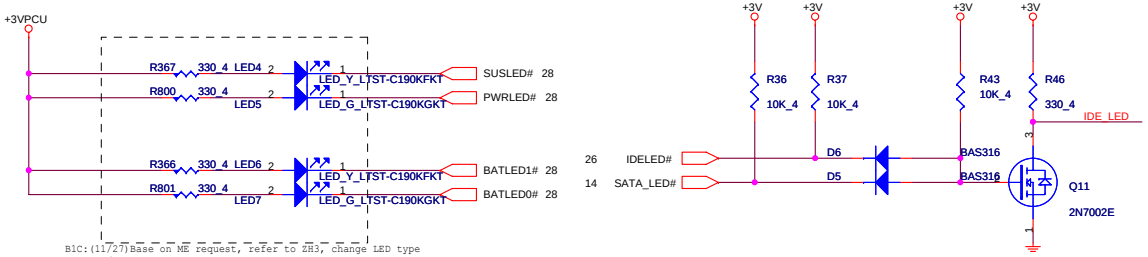
INT K/B

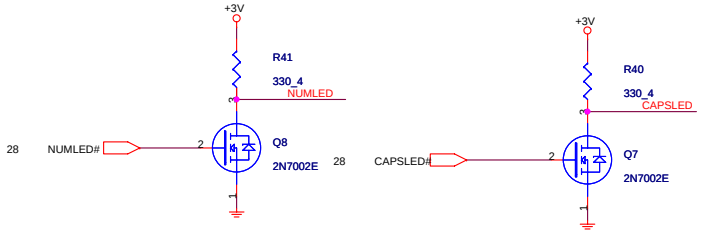


A1A: (9/26) Refer to ZH3, change K/B matrix

LED



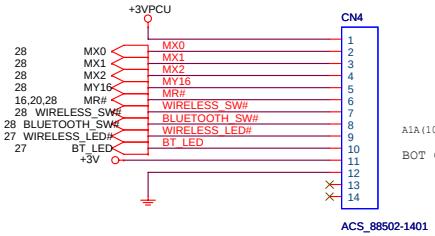
B1C:(11/27)Base on ME request, refer to ZH3, change LED type
B1C:(11/28)Base on ME request, change LED type
D3A:(1/24) Base on SMT-ME request, change LED type to 2 in 1
DEL LED4,LED5,LED6,LED7,R570,R571,Add LED2,LED3
E3A:(3/16)Change LED2, LED3 type base on ME request, Add R800,R801
E3A:(3/30) ESD issue, change LED type (follow B stage)



A1A:(10/30) no stuff (ZU1 no support EMAIL LED)

E3A:(3/30)Remove Q27,R1 footprint to save space for layout
ZU1 no support E-Mail LED

Function Board



A1A(10/5):Change Pin define (Base on Acer ID)

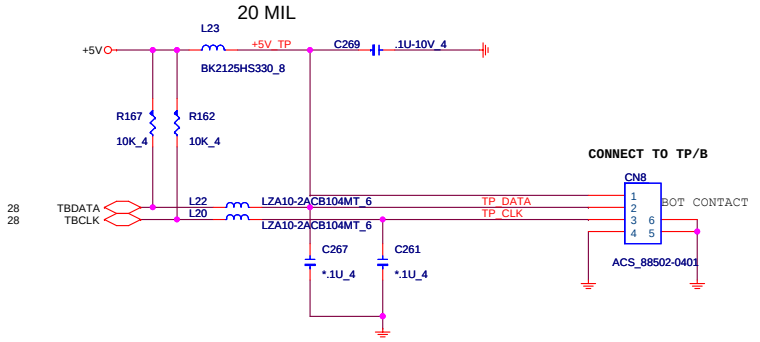
BOT CONTACT

A1A:(9/27) Add Function Board CONN (14pin)

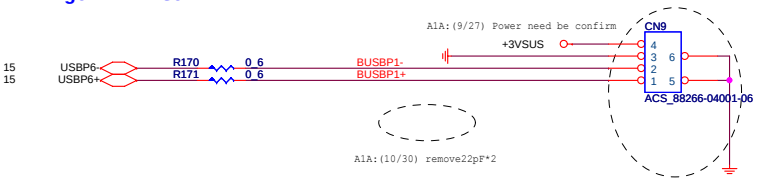
A1A:(10/30) add +3V for Daughter Board use

Keyboard Matrix	Button
MX0/MY16	acer EAP Buttton
MX1/MY16	acer EMAIL Buttton
MX2/MY16	acer WWW Buttton
MX3/MY16	acer EPM Buttton
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button

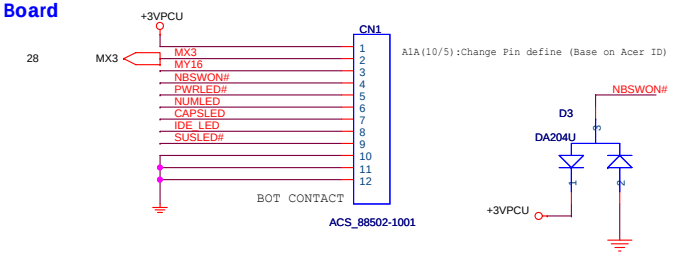
TOUCH PAD



Finger Printer



LED Board

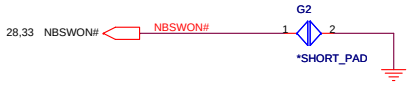


A1A(10/5):Change Pin define (Base on Acer ID)

A1A:(9/27) Add LED Board CONN (10pin)

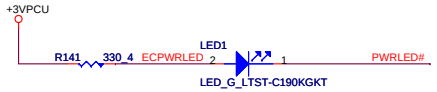
A1A:(10/26) Add SUSLED#

E3A:(3/30) change ESD protect Diode location from LED/B to MB
(Add D3)



A1A: (9/24) change SW CONN (follow ZC3)

D3A: (1/29) remove SW1, add G2 footprint



A1A: (10/30) Reserved LED for debug use

+3VPCU

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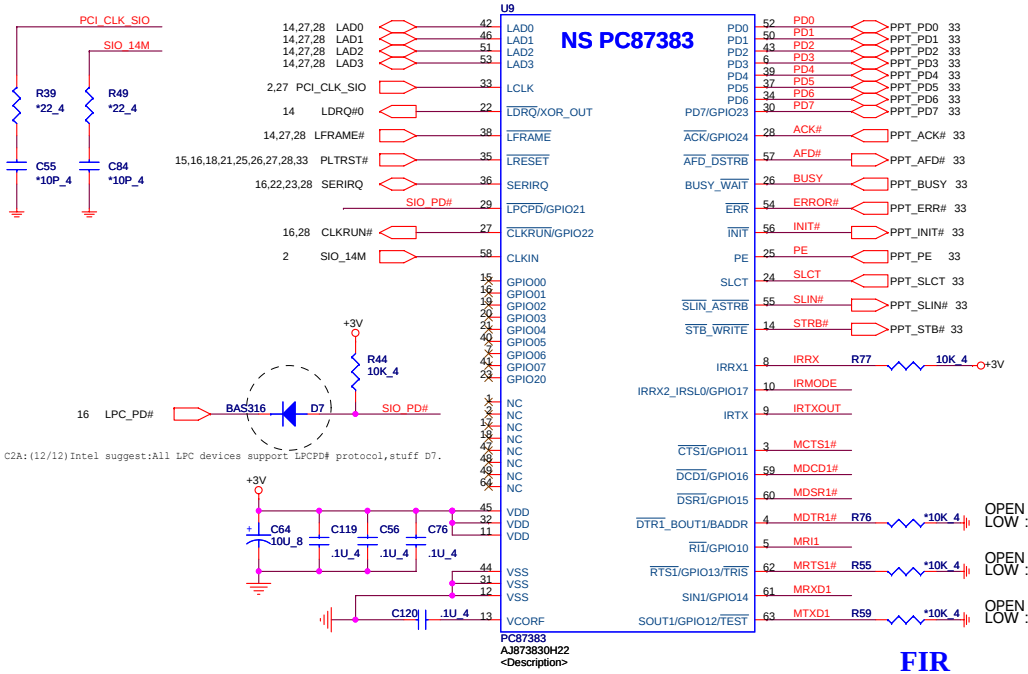
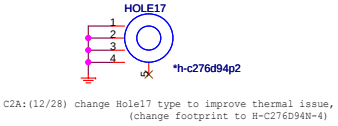
NS SIO PC87383



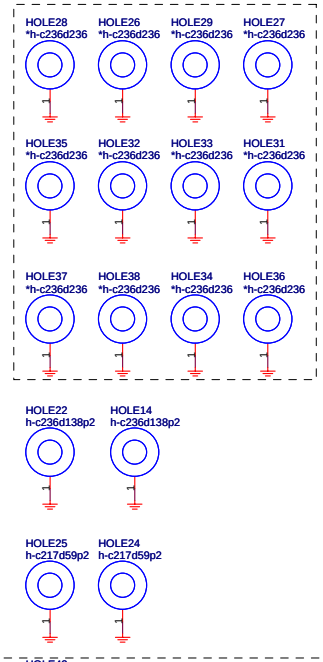
A1A:(9/20) PPT PU 4.7k circuit exist in Docking. remove it.



C2A:(12/28) change Hole17 type to improve thermal issue, (change footprint to H-C276D94N-4)

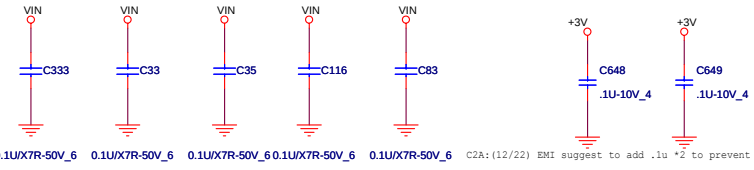
C2A:(12/12)Intel suggest:All LPC devices support LPCPD# protocol,stuff D7.

HOLE

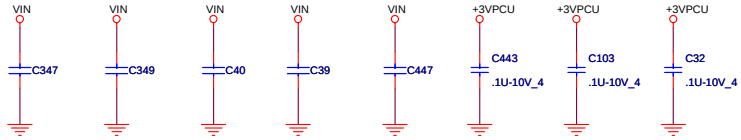


EMI Cap

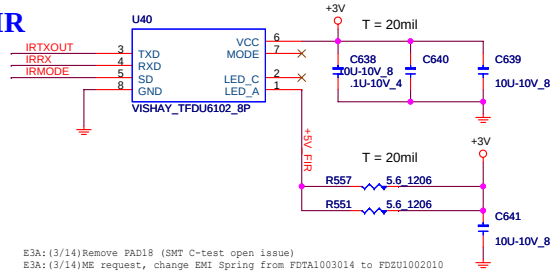
A1A:(10/19) EMI suggest :Add the VIN power shape bypass cap 0.1uF x 10pcs
Add the +3VPCU power traces bypass cap 0.1uF x 3pcs



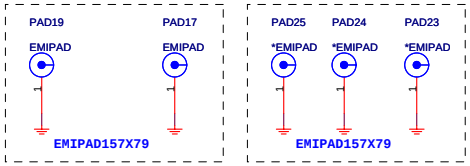
C2A:(12/22) EMI suggest to add .1u *2 to prevent noise (+3V)



FIR



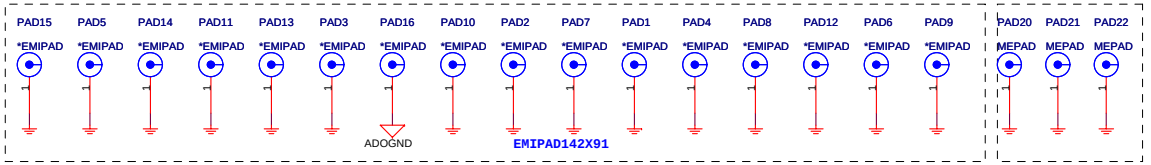
E3A:(3/14)Remove PAD18 (SMT C-test open issue)
E3A:(3/14)ME request, change EMI Spring from FDTA1003014 to FDZU1002010
D3A:(2/14)EMI request add two of clip(FDTA1003014) in PAD17 and PAD19 for EMI issue

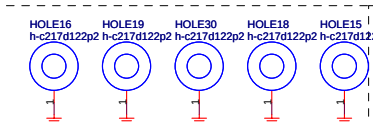


C2A:(12/22) EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)

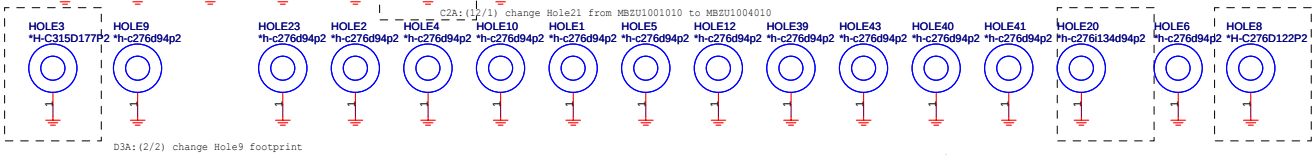
B1C:(11/27)change Hole42 footprint
B1C:(11/23)remove Hole7
D3A:(2/8)Remove hole13

ESDPad





C2A:(12/1) change Hole21 from MBZU1001010 to MBZU1004010



D3A:(2/2) change Hole9 footprint

C2A:(12/22) change Hole20 footprint to h-c276i134d94p2

C2A:(12/22) Add theree PAD per ME request (fix wire)
D3A:(2/2) change PAD20.PAD21.PAD22 footprint
D3A:(2/12) Add PAD20.PAD21.PAD22 P/N (FDZU1001010)

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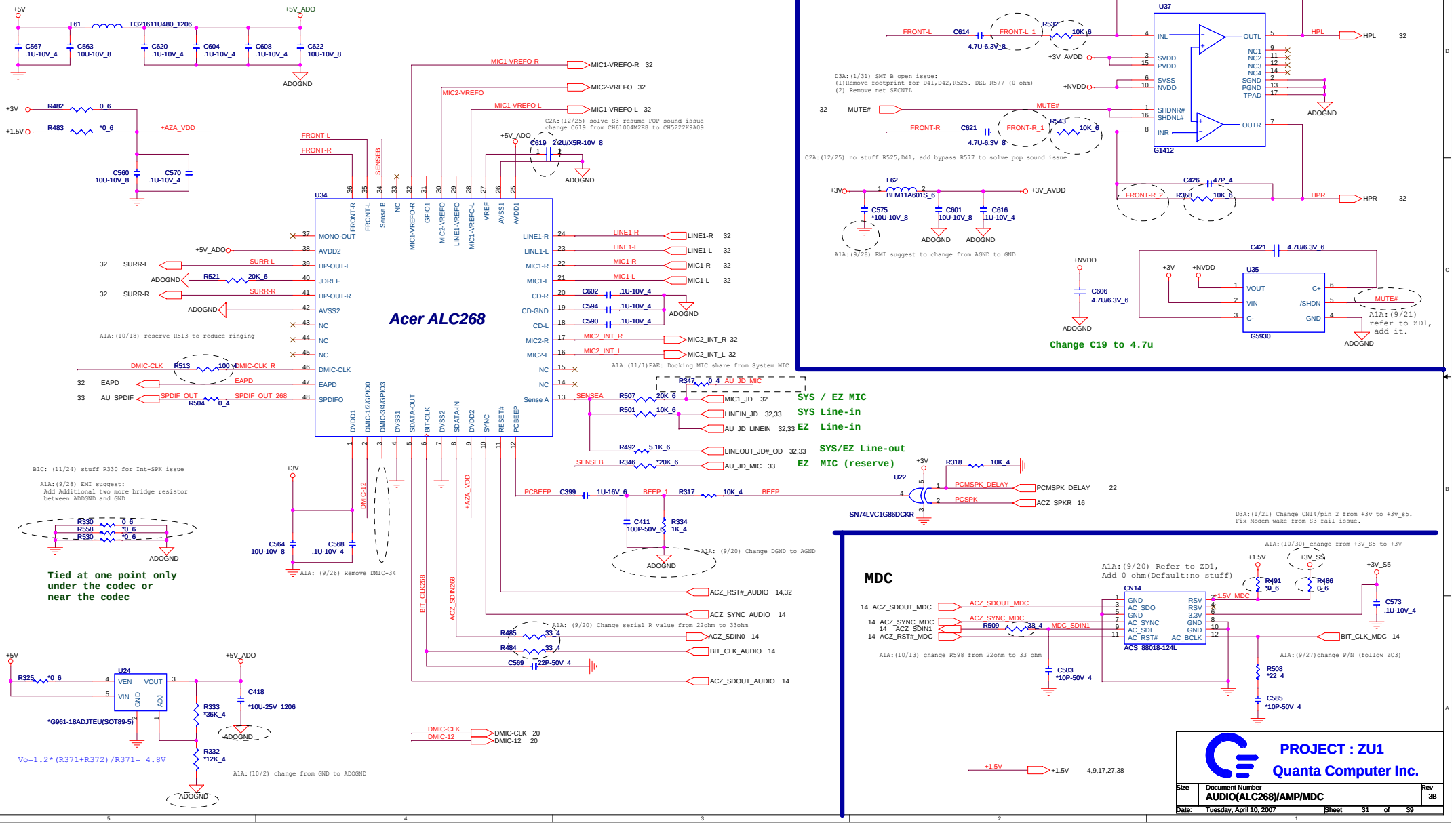
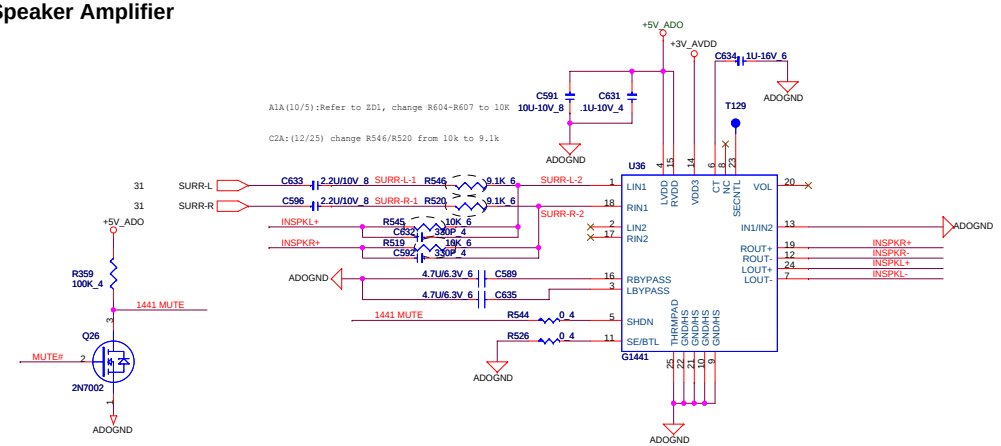
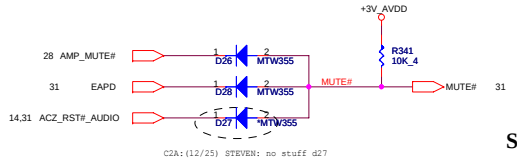
CODEC(ALC268)

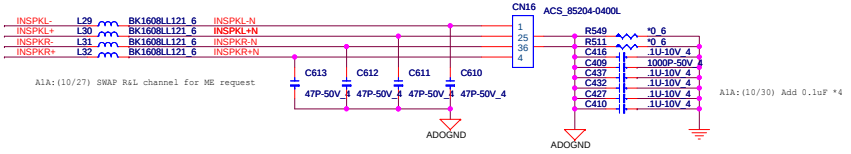


Speaker Amplifier

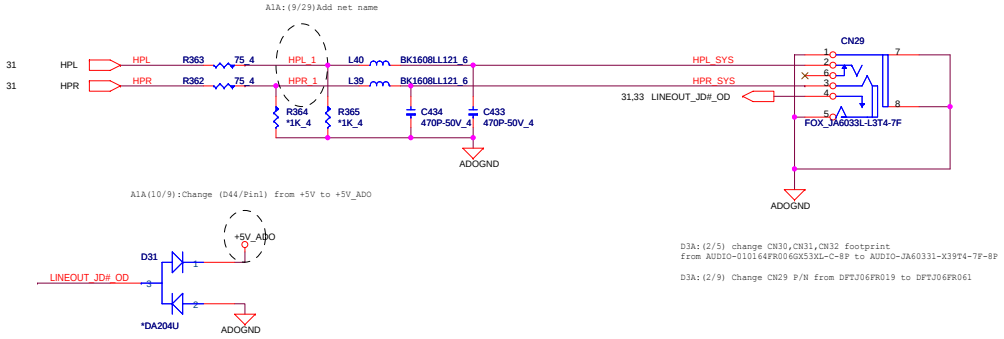




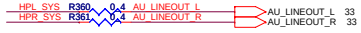
SPEAKER



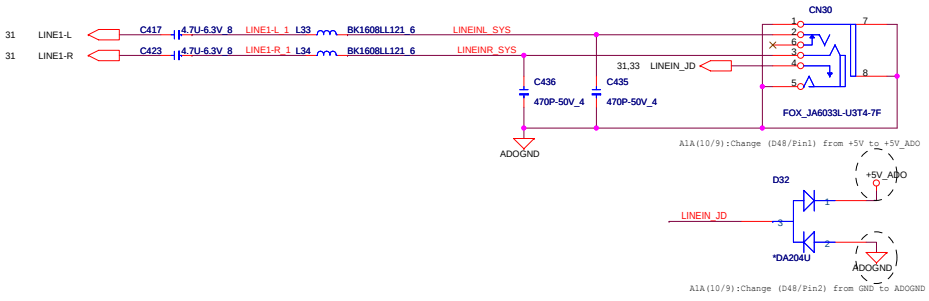
SYSTEM LINE OUT



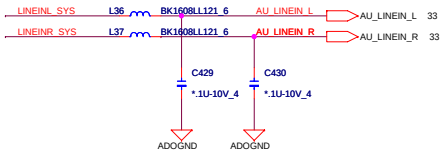
Docking LINE OUT/SPDIF



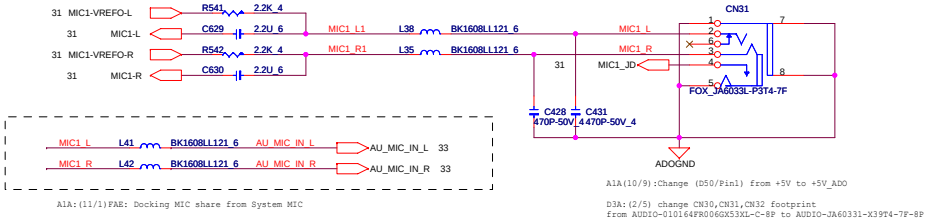
SYSTEM LINE IN



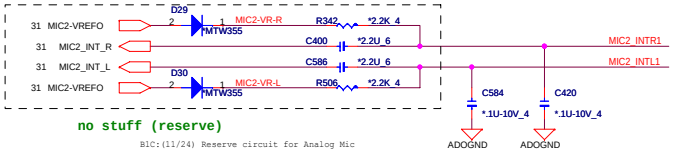
Docking LINE IN

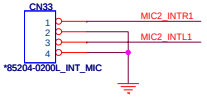


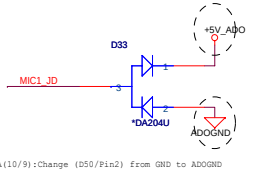
SYSTEM MIC



Analog MIC







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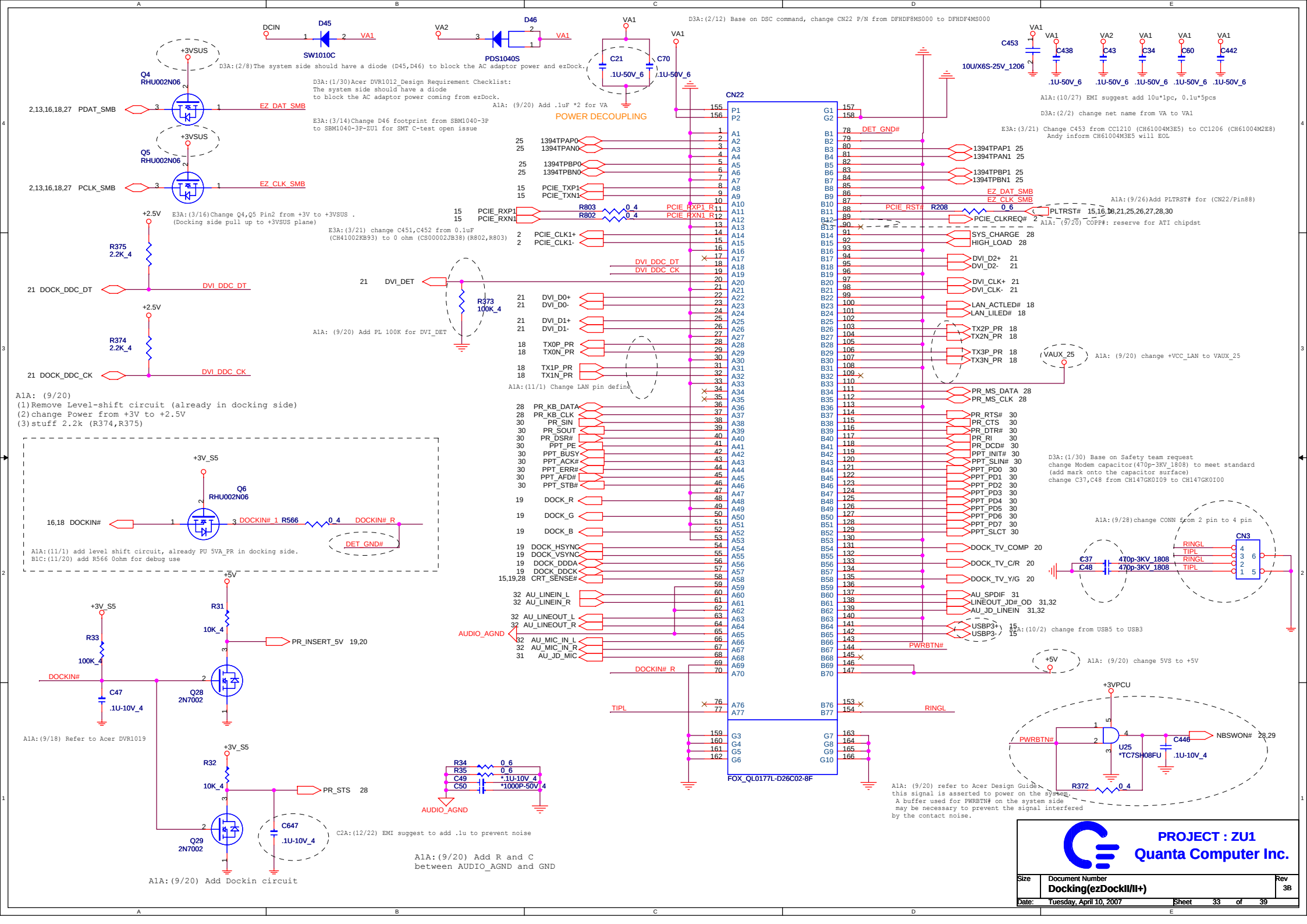
D3A:(2/12) Base on DSC command, change CN22 P/N from DFHDF8MS000 to DFHDF4MS000
DCIN
D45
SW1010C
VA1
D46
PDS1040S
VA2
C21
.1U-50V_6
C70
.1U-50V_6
POWER DECOUPLING
D3A:(2/8)The system side should have a diode (D45,D46) to block the AC adaptor power and ezDock.
D3A:(1/30)Acer DVR1012_Design Requirement Checklist:
The system side should have a diode
to block the AC adaptor power coming from ezDock.
A1A: (9/20) Add .1uF *2 for VA
E3A:(3/14)Change D46 footprint from SBM1040-3P
to SBM1040-3P-ZU1 for SMT C-test open issue
+3VSUS
Q4
RHU002N06
Q5
RHU002N06
2,13,16,18,27 PDAT_SMB
EZ_DAT_SMB
2,13,16,18,27 PCLK_SMB
EZ_CLK_SMB
E3A:(3/16)Change Q4,Q5 Pin2 from +3V to +3VSUS .
(Docking side pull up to +3VSUS plane)
+2.5V
R375
2.2K_4
R374
2.2K_4
21 DOCK_DDC_DT
DVI_DDC_DT
21 DOCK_DDC_CK
DVI_DDC_CK
A1A: (9/20)
(1)Remove Level-shift circuit (already in docking side)
(2)change Power from +3V to +2.5V
(3)stuff 2.2k (R374,R375)
E3A:(3/21) change C451,C452 from 0.1uF
(CH41002KB93) to 0 ohm (CS00002JB38)(R802,R803)
21 DVI_DET
R373
100K_4
A1A: (9/20) Add PL 100K for DVI_DET
A1A:(11/1) Change LAN pin define
CN22
FOX_QL0177L-D26C02-8F
1394TPAP0
1394TPAN0
1394TPBP0
1394TPBN0
PCIE_TXP1
PCIE_TXN1
PCIE_RXP1
PCIE_RXN1
R803 0_4 PCIE_RXP1_R
R802 0_4 PCIE_RXN1_R
PCIE_CLK1+
PCIE_CLK1-
DVI_DDC_DT
DVI_DDC_CK
DVI_D0+
DVI_D0-
DVI_D1+
DVI_D1-
TX0P_PR
TX0N_PR
TX1P_PR
TX1N_PR
PR_KB_DATA
PR_KB_CLK
PR_SIN
PR_SOUT
PR_DSR#
PPT_PE
PPT_BUSY
PPT_ACK#
PPT_ERR#
PPT_AFD#
PPT_STB#
DOCK_R
DOCK_G
DOCK_B
DOCK_HSYNC
DOCK_VSYNC
DOCK_DDDA
DOCK_DDCK
CRT_SENSE#
AU_LINEIN_L
AU_LINEIN_R
AU_LINEOUT_L
AU_LINEOUT_R
AUDIO_AGND
AU_MIC_IN_L
AU_MIC_IN_R
AU_JD_MIC
DOCKIN#_R
TIPL
RINGL
DET_GND#
PCIE_RST#
R208 0_6
PCIE_CLKREQ#
PLTRST# 15,16,18,21,25,26,27,28,30
A1A:(9/26)Add PLTRST# for (CN22/Pin88)
A1A:(9/20) COPP#: reserve for ATI chipdst
SYS_CHARGE 28
HIGH_LOAD 28
1394TPAP1 25
1394TPAN1 25
1394TPBP1 25
1394TPBN1 25
EZ_DAT_SMB
EZ_CLK_SMB
DVI_D2+ 21
DVI_D2- 21
DVI_CLK+ 21
DVI_CLK- 21
LAN_ACTLED# 18
LAN_LILED# 18
TX2P_PR 18
TX2N_PR 18
TX3P_PR 18
TX3N_PR 18
VAUX_25
A1A: (9/20) change +VCC_LAN to VAUX_25
PR_MS_DATA 28
PR_MS_CLK 28
PR_RTS# 30
PR_CTS 30
PR_DTR# 30
PR_RI 30
PR_DCD# 30
PPT_INIT# 30
PPT_SLIN# 30
PPT_PD0 30
PPT_PD1 30
PPT_PD2 30
PPT_PD3 30
PPT_PD4 30
PPT_PD5 30
PPT_PD6 30
PPT_PD7 30
PPT_SLCT 30
DOCK_TV_COMP 20
DOCK_TV_C/R 20
DOCK_TV_Y/G 20
AU_SPDIF 31
LINEOUT_JD#_OD 31,32
AU_JD_LINEIN 31,32
USBP3+ 15
USBP3- 15
A1A:(10/2) change from USB5 to USB3
PWRBTN#
+5V
A1A: (9/20) change 5VS to +5V
C453
10U/X6S-25V_1206
C438
C43
C34
C60
C442
.1U-50V_6
A1A:(10/27) EMI suggest add 10u*1pc, 0.1u*5pcs
D3A:(2/2) change net name from VA to VA1
E3A:(3/21) Change C453 from CC1210 (CH61004M3E5) to CC1206 (CH61004M2E8)
Andy inform CH61004M3E5 will EOL
D3A:(1/30) Base on Safety team request
change Modem capacitor(470p-3KV_1808) to meet standard
(add mark onto the capacitor surface)
change C37,C48 from CH147GK0I09 to CH147GK0I00
A1A:(9/28)change CONN from 2 pin to 4 pin
CN3
C37
C48
470p-3KV_1808
470p-3KV_1808
RINGL
TIPL
RINGL
TIPL
+3V_S5
Q6
RHU002N06
16,18 DOCKIN#
DOCKIN#_1
R566
0_4
DOCKIN#_R
DET_GND#
A1A:(11/1) add level shift circuit, already PU 5VA_PR in docking side.
B1C:(11/20) add R566 0ohm for debug use
+5V
R31
10K_4
PR_INSERT_5V 19,20
R33
100K_4
DOCKIN#
C47
.1U-10V_4
Q28
2N7002
A1A:(9/18) Refer to Acer DVR1019
R32
10K_4
PR_STS 28
Q29
2N7002
C647
.1U-10V_4
C2A:(12/22) EMI suggest to add .1u to prevent noise
A1A:(9/20) Add Dockin circuit
R34 0_6
R35 0_6
C49 *1U-10V_4
C50 *1000P-50V_4
AUDIO_AGND
A1A:(9/20) Add R and C
between AUDIO_AGND and GND
+3VPCU
PWRBTN#
U25
*TC7SH08FU
C446
.1U-10V_4
NBSWON# 28,29
R372 0_4
A1A: (9/20) refer to Acer Design Guide,
this signal is asserted to power on the system.
A buffer used for PWRBTN# on the system side
may be necessary to prevent the signal interfered
by the contact noise.
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
Docking(ezDockII/II+)
Rev
3B
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MAIND — MAIND 38

SUSD — SUSD 38

3 SYS_SHDN#

PR121 0_4

PL20 HI0805R800R-00_8

PL7 HI0805R800R-00_8

VIN

PC77 0.1U/X7R-50V_6

PC79 2200P/X7R-50V_4

PC72 10U/X6S-25V_1206

PC84 10U/X6S-25V_1206

VL

PR122 39K_4

3V5V_EN

ISL6236_3V

PR97 390K_4

PC74 0.1U/X7R-50V_6

PR95 150K_4

PC71 4.7U/X7R-10V_8

PR102 0_4

PC75 1U/10V_6

PR107 0_4

PC76 .01U/X7R-16V_4

PC73 0.1U/X7R-50V_6

PR103 *0_4

PR109 *0_4

PL10 HI0805R800R-00_8

PC94 0.1U/X7R-50V_6

PC87 2200P/X7R-50V_4

PC86 10U/X6S-25V_1206

PC83 10U/X6S-25V_1206

3V_DL

PQ23 FDS6900AS

3V_DH

PL12 2.5uH_7.5A

3VPCU

+3VPCU

OCP : 6.25A

Change PL12 part number from (CV-2575MZ02) to (CV-2575TZ51)

Change PL11 part number from (DC-15A00036) to (DC-15A00010)

OCP: 10A

D3A:(2/15)Andy inform change PR116 from CS42102FB00 to CS42102FB12

+5VPCU

5VPCU

PL11 1.5uH_10A

5V_LX

5V_DH

PQ18 FDS8884

5V_DL

PQ17 FDS6690AS

PR114 *0_4

PR113 0_4

PC95 10U/X6S-25V_1206

PC143 330U/6.3V_6X5.7

PC92 0.1U/X7R-50V_6

PR116 210K_4

DDPWRGD_R

3V5V_EN

PC97 0.1U/X7R-50V_6

PR124 1_6

PR112 287K_4

PC90 0.1U/X7R-50V_6

PR123 1_6

PR118 0_6

PR115 *0_6

PC103 0.1U/X7R-50V_6

PC142 330U/6.3V_6X5.7

PU7 ISL6236

BYP, OUT1, FB1, ILIM1, PGOOD1, EN1, DH1, LX1, PAD, PAD, PAD, PAD

DDREFIN, LDO, VIN, RTC, ONOFF, VCC, TON, REF

REFIN2, ILIM2, OUT2, SKIP#, PGOOD2, EN2, DH2, LX2

BST1, DL1, VDD, SECFB, GND, PGND, DL2, BST2

PD6 CHN217

PD8 CHN217

PD7 BAT54-7-F

PC82 0.1U/X7R-50V_6

PC81 0.1U/X7R-50V_6

PC78 0.1U/X7R-50V_6

PC99 1U/10V_6

PR125 0_6

DDPWRGD_R

T144

OCP:10A

L(ripple current)
=(19-5)*5/(1.5u*0.4M*19)
~6A

Iocp=10-(6/2)=7A
Vth=7A*15mOhm=105mV
R(Ilim)=(105mV*10)/5uA
~210K

OCP:6.25A

L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A

Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K

PR117 22_8

15V

+15V_ALWP

PC80 0.1U/X7R-50V_6

PR128 200K_4

PR126 39K_4

VIN

15V

+5VPCU

PR159 1M_6

PR127 1M_6

S5D

PQ24 DTC144EU

28,38 S5_ON

PR160 1M_6

PQ44 2N7002E

PC108 0.1U/X7R-50V_6

PQ26 FDS8884

+5V_S5

PC101 0.1U/X7R-50V_6

+5VPCU

PC91 0.1U/X7R-50V_6

MAIND

PQ21 FDC653N_NL

+5V

PC93 0.1U/X7R-50V_6

+3VPCU

PC105 0.1U/X7R-50V_6

MAIND

PQ29 FDC653N_NL

+3V

PC107 0.1U/X7R-50V_6

+3VPCU

PC102 0.1U/X7R-50V_6

S5D

PQ27 FDC653N_NL

+3V_S5

PC104 0.1U/X7R-50V_6

+3VPCU

PC96 0.1U/X7R-50V_6

SUSD

PQ22 FDC653N_NL

+3VSUS

PC100 0.1U/X7R-50V_6

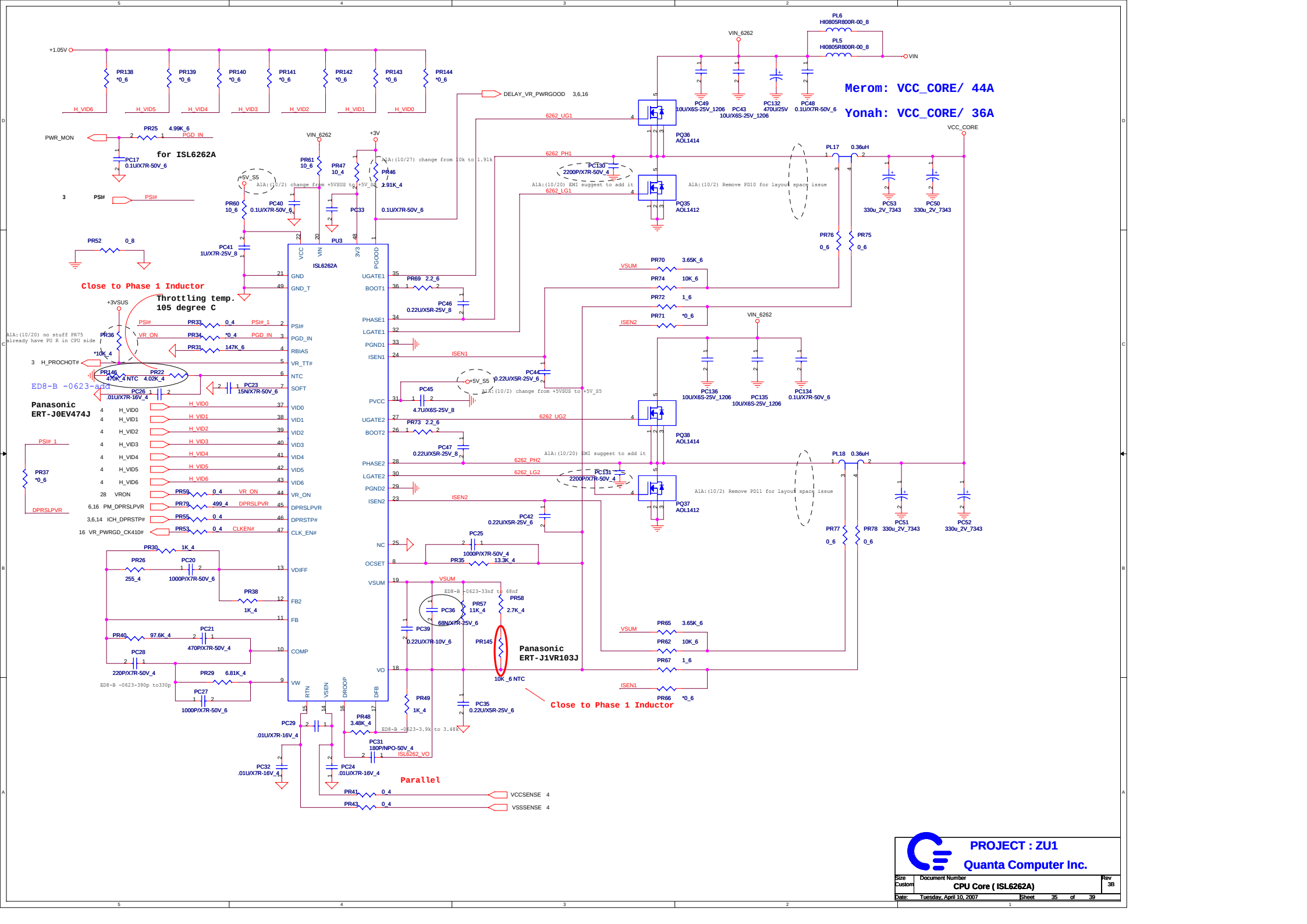
C2A:(12/10) change S5_ON control circuit

B1C:(11/29)Change PQ26 from FDS6690AS (BAM66900022) to FDS8884 (BAM88840006)

Quanta Computer Inc.

PROJECT : ZU1

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6236)	3B
Date: Tuesday, April 10, 2007	Sheet 34 of 39	


Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
ISL6262A
PROJECT : ZU1
Quanta Computer Inc.
CPU Core (ISL6262A)
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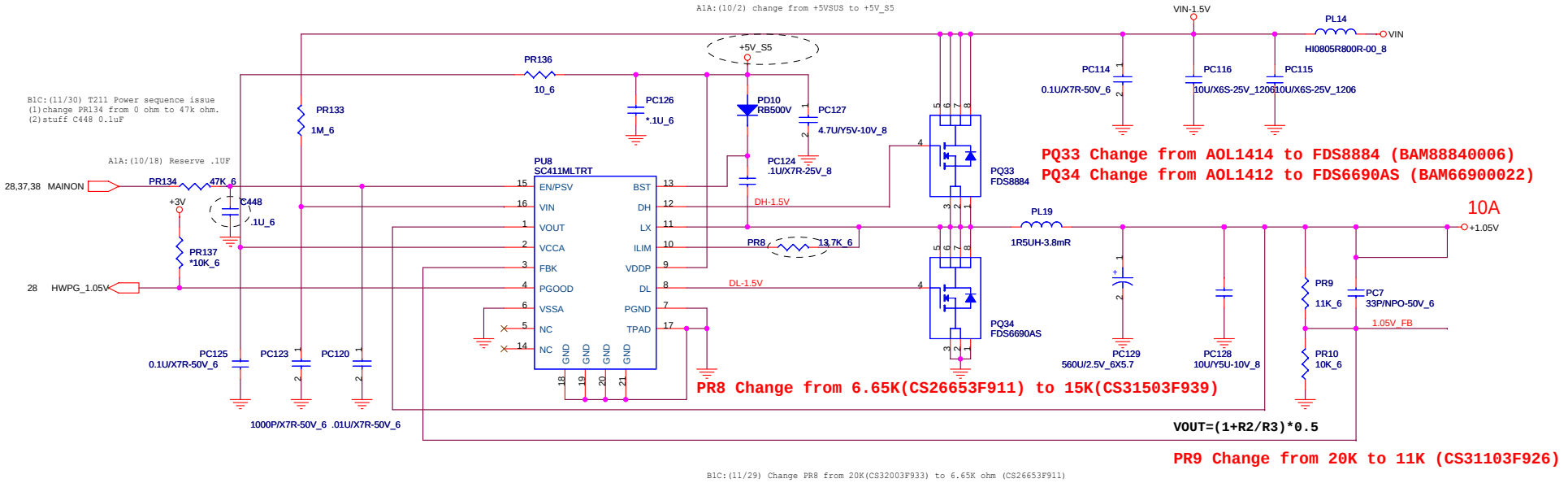
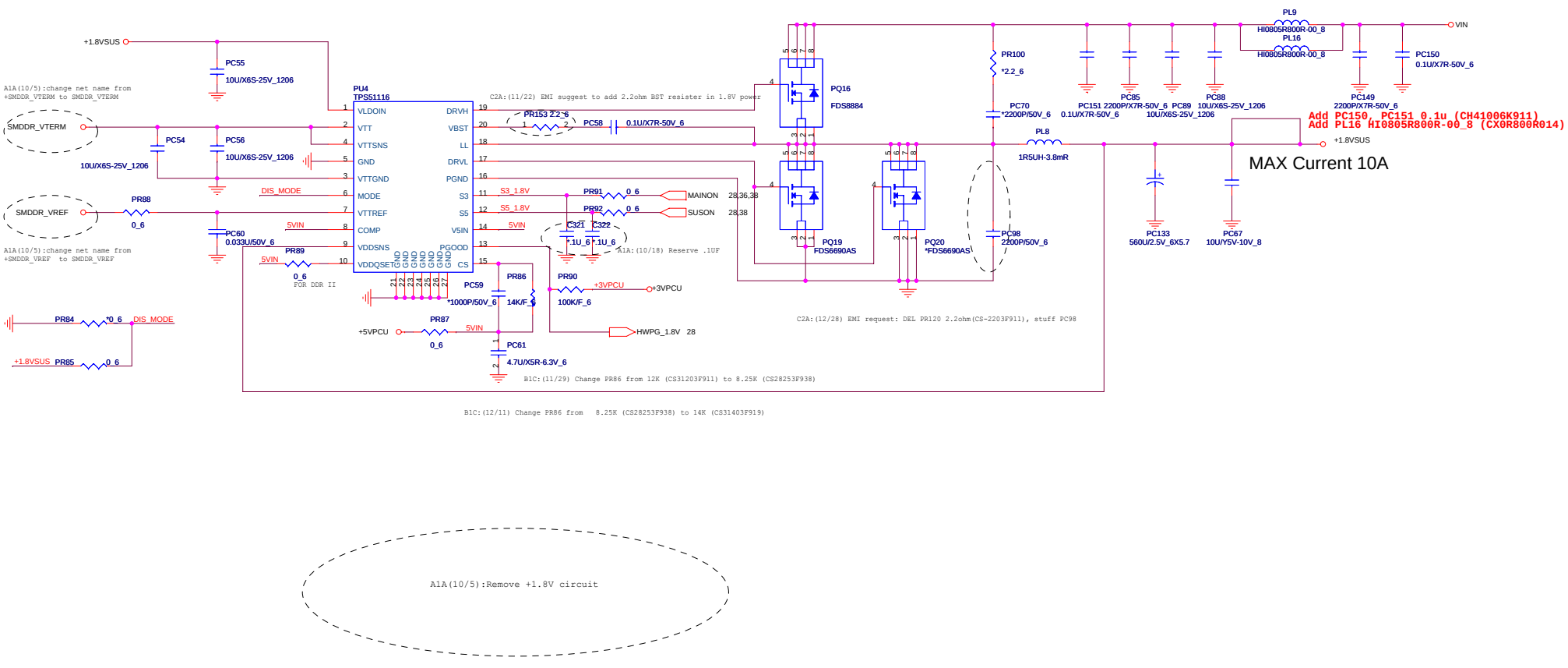


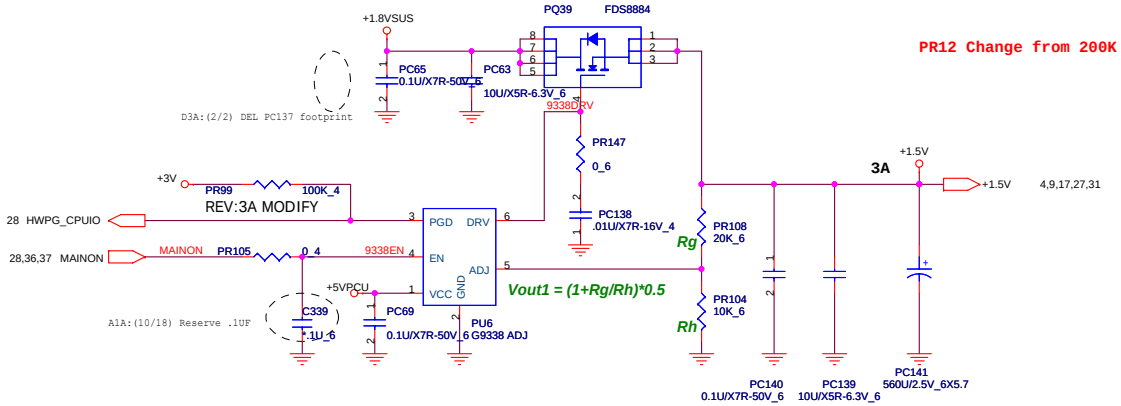
PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	VTT 1.05V (SC411)	3B
Date: Tuesday, April 10, 2007	Sheet 36 of 39	

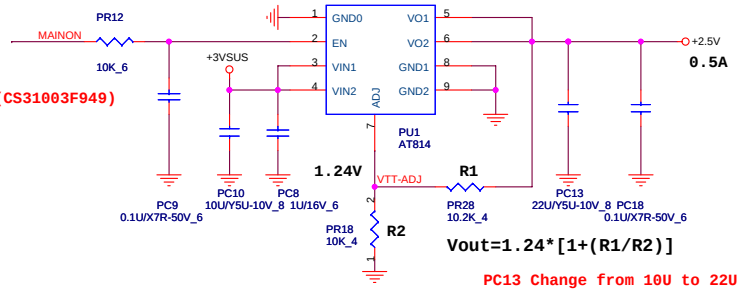


Size	Document Number: DDR 1.8V(TPS51116)	Rev: 3B
Date: Tuesday, April 10, 2007	Sheet 37 of 39	

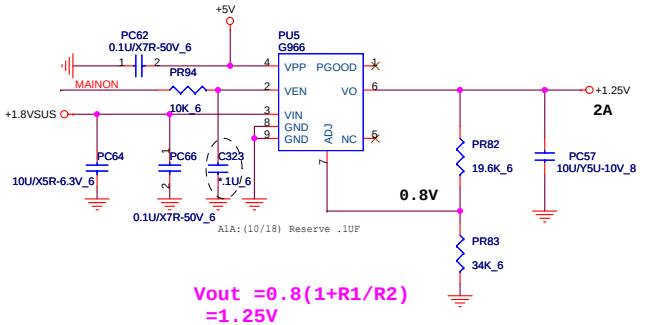
PROJECT : ZU1
Quanta Computer Inc.



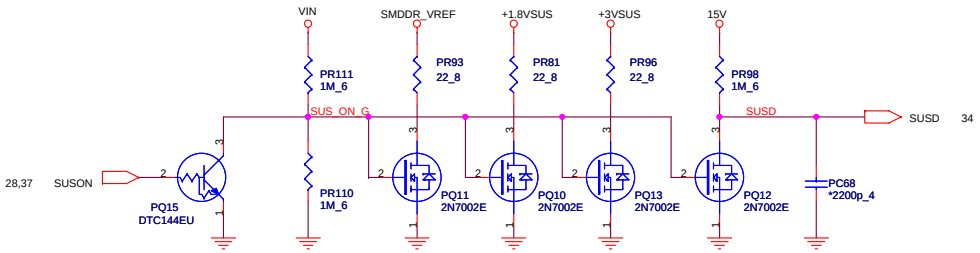
PR12 Change from 200K to 10K (CS31003F949)

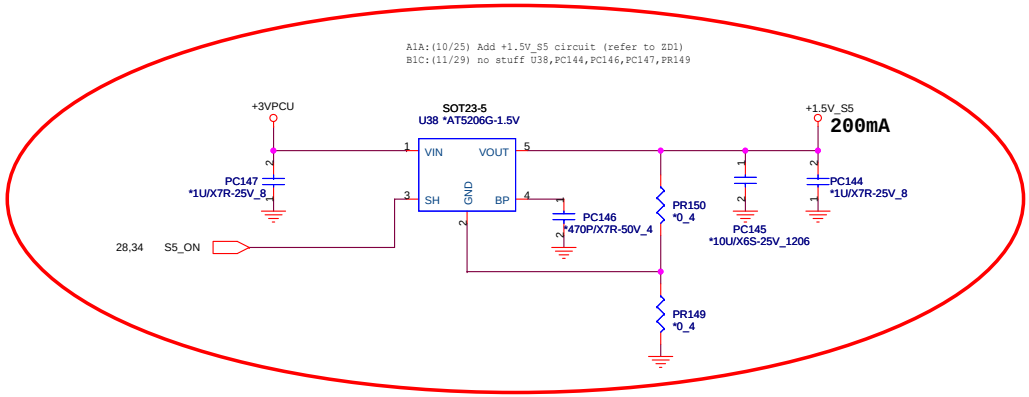


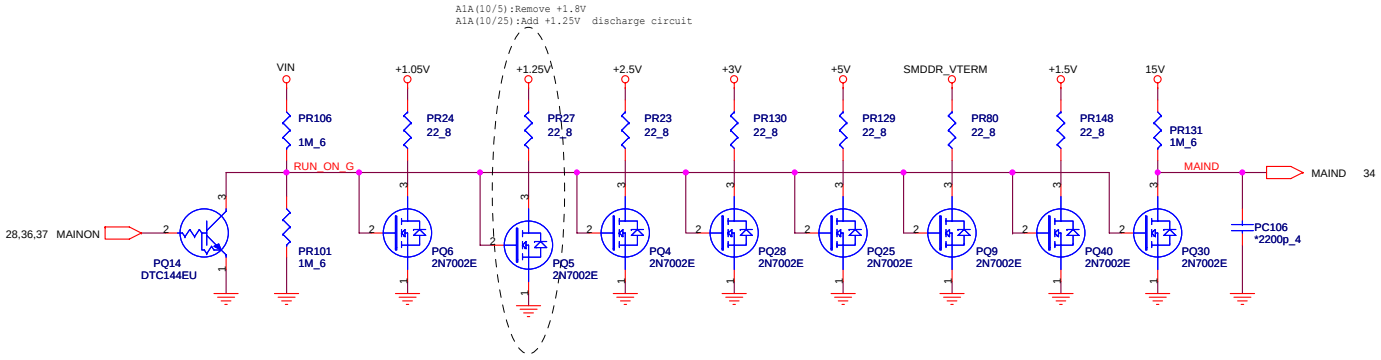
PC13 Change from 10U to 22U (CH6221M9A07)



Vout =0.8(1+R1/R2)
=1.25V







PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	3B
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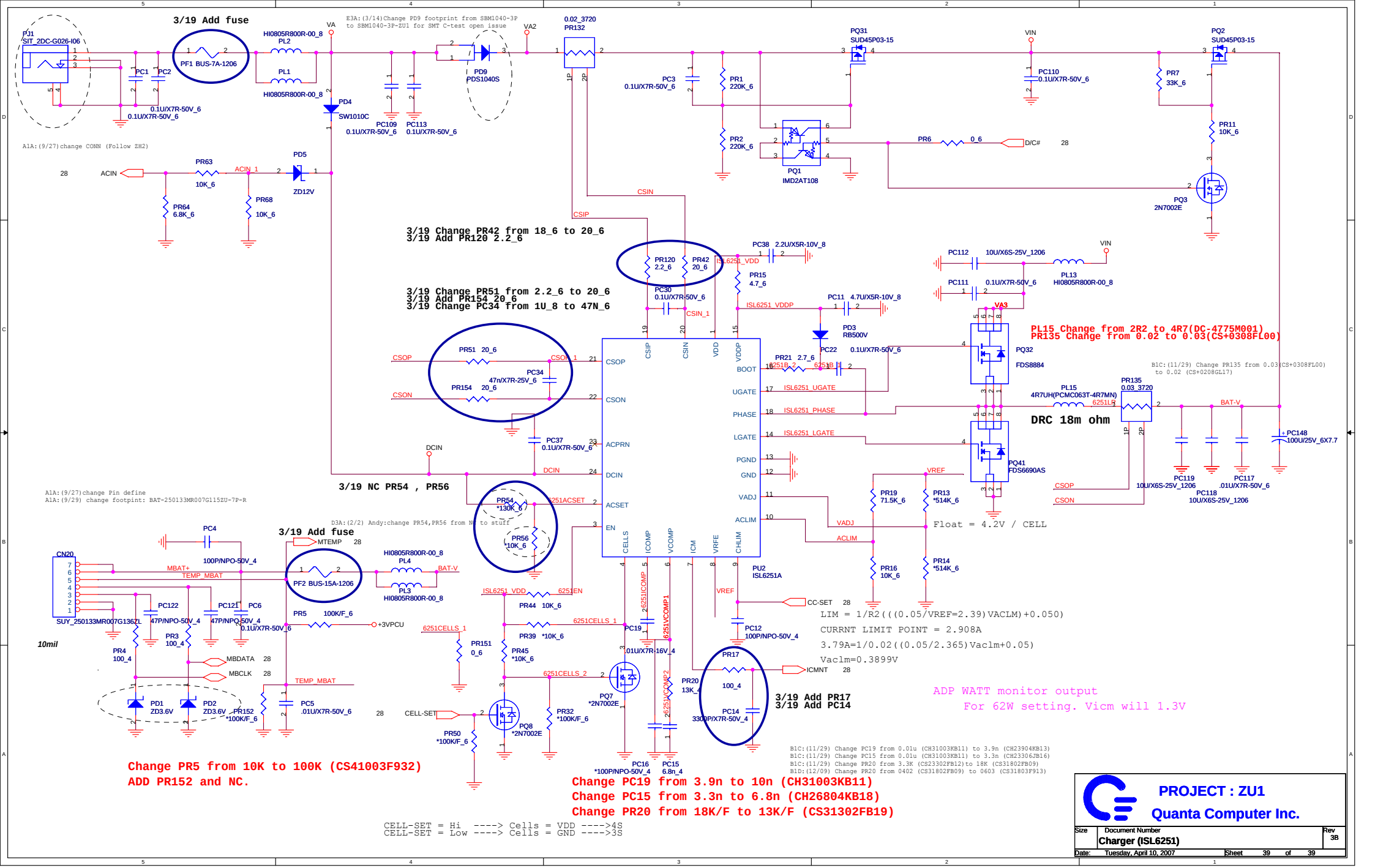
3/19 Add fuse
PF1 BUS-7A-1206
HI0805R800R-00_8
PL2
PL1
HI0805R800R-00_8
PD4
SW1010C
PD9
PDS1040S
0.02_3720
PR132
PQ31
SUD45P03-15
PQ2
SUD45P03-15
PQ1
IMD2AT108
PQ3
2N7002E
PR6
0_6
D/C#
28
ACIN
PR63
10K_6
PR64
6.8K_6
PR68
10K_6
PD5
ZD12V
3/19 Change PR42 from 18_6 to 20_6
3/19 Add PR120 2.2_6
3/19 Change PR51 from 2.2_6 to 20_6
3/19 Add PR154 20_6
3/19 Change PC34 from 1U_8 to 47N_6
PR120
2.2_6
PR42
20_6
PR51 20_6
PR154 20_6
PC34
47n/X7R-25V_6
PC37
0.1U/X7R-50V_6
DCIN
3/19 NC PR54 , PR56
PR54
*130K_6
PR56
*10K_6
PU2
ISL6251A
CSOP
CSON
CSIP
CSIN
VDD
VDDP
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM
ACPRN
DCIN
ACSET
EN
CELLS
ICOMP
VCOMP
ICM
VFRE
CHLIM
PC38 2.2U/X5R-10V_8
PR15
4.7_6
PC30
0.1U/X7R-50V_6
PC11 4.7U/X5R-10V_8
PD3
RB500V
PC22 0.1U/X7R-50V_6
PR21 2.7_6
PC112 10U/X6S-25V_1206
PC111 0.1U/X7R-50V_6
PL13
HI0805R800R-00_8
PQ32
FDS8884
PQ41
FDS6690AS
PL15 Change from 2R2 to 4R7(DC-4775M001)
PR135 Change from 0.02 to 0.03(CS+0308FL00)
PL15
4R7UH(PCMC063T-4R7MN)
PR135
0.03_3720
DRC 18m ohm
PC148
100U/25V_6X7.7
PC119
10U/X6S-25V_1206
PC117
.01U/X7R-50V_6
PC118
10U/X6S-25V_1206
PR19
71.5K_6
PR13
*514K_6
PR16
10K_6
PR14
*514K_6
Float = 4.2V / CELL
LIM = 1/R2(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT = 2.908A
3.79A=1/0.02((0.05/2.365)Vaclm+0.05)
Vaclm=0.3899V
PC12
100P/NPO-50V_4
CC-SET
ICMNT
3/19 Add fuse
PF2 BUS-15A-1206
CN20
SUY_250133MR007G136ZL
PC4
100P/NPO-50V_4
PC122
47P/NPO-50V_4
PC121
47P/NPO-50V_4
PC6
0.1U/X7R-50V_6
PR4
100_4
PR3
100_4
PR5
100K/F_6
+3VPCU
MBDATA
MBCLK
TEMP_MBAT
PD1
ZD3.6V
PD2
ZD3.6V
PR152
*100K/F_6
PC5
.01U/X7R-50V_6
10mil
PR151
0_6
PR45
*10K_6
PR44
10K_6
PR39
*10K_6
PR32
*100K/F_6
PR50
*100K/F_6
PQ7
*2N7002E
PQ8
*2N7002E
PC19
.01U/X7R-16V_4
PC16
*100P/NPO-50V_4
PC15
6.8n_4
PR17
100_4
PR20
13K_4
PC14
3300P/X7R-50V_4
3/19 Add PR17
3/19 Add PC14
ADP WATT monitor output
For 62W setting. Vicm will 1.3V
Change PR5 from 10K to 100K (CS41003F932)
ADD PR152 and NC.
Change PC19 from 3.9n to 10n (CH31003KB11)
Change PC15 from 3.3n to 6.8n (CH26804KB18)
Change PR20 from 18K/F to 13K/F (CS31302FB19)
CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S
PROJECT : ZU1
Quanta Computer Inc.
Charger (ISL6251)
Tuesday, April 10, 2007
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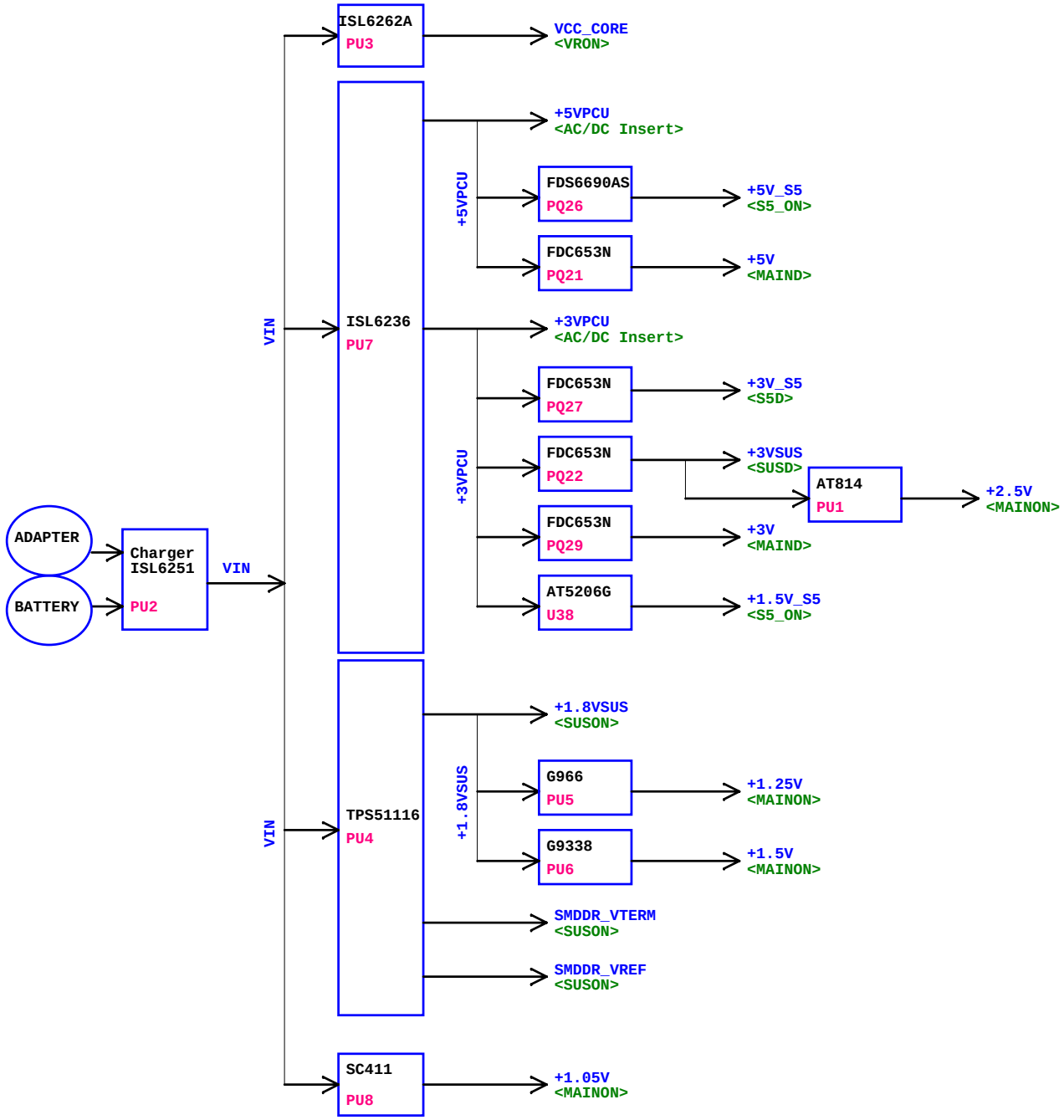
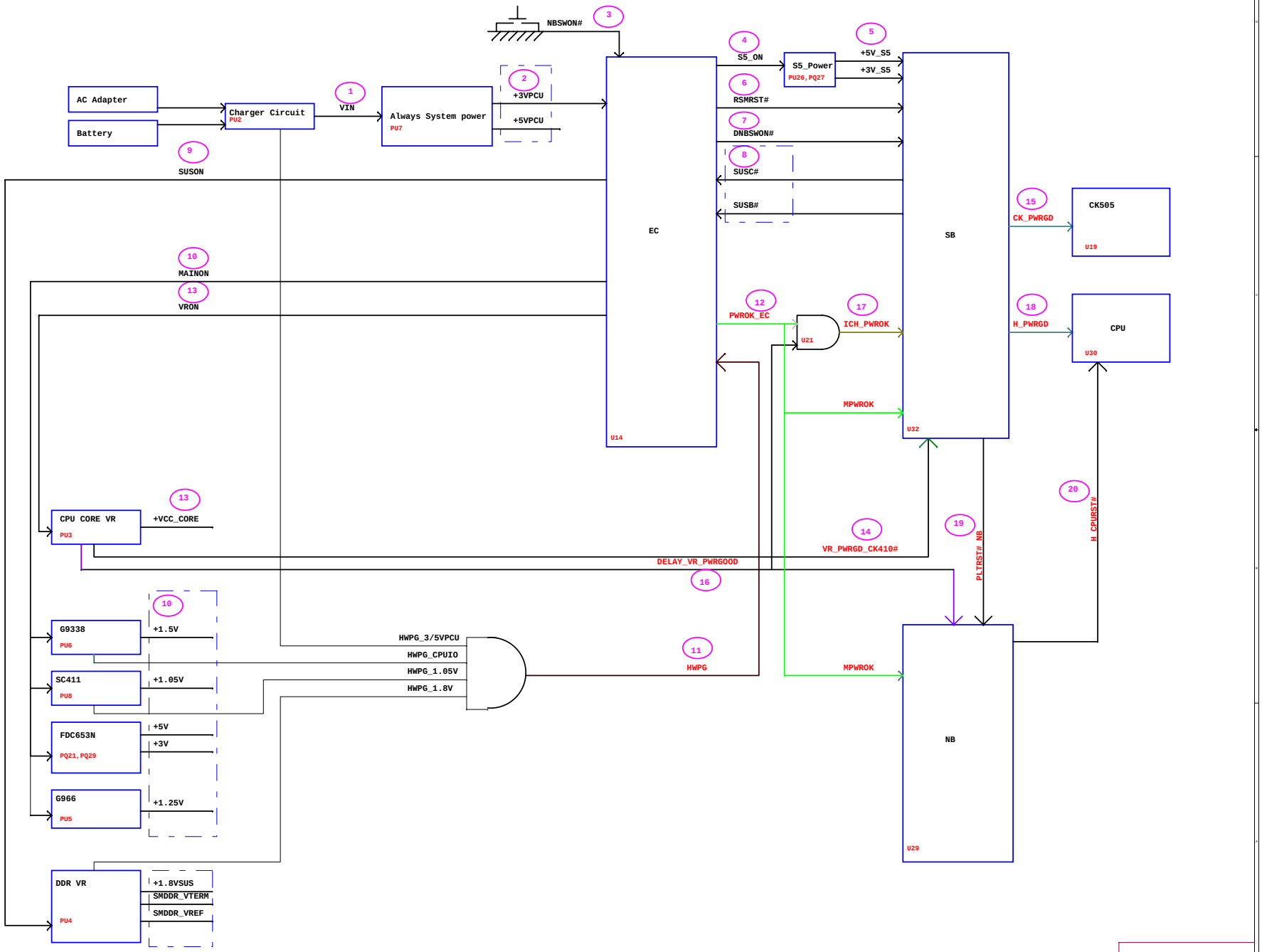


ZU1 Power Table

SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



ZU1 Power Sequence

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
1	CPU Clock select issue	Stuff R179,R198,R447 for CPU Clock select issue	A1A	2
2	PCI Clock issue	change R186 value from 33ohm to 22 ohm (refer to Intel check list 1.301)	A1A	2
3	CK505 issue	ICS FAE suggest to change C542,C287 from 4.7u to 10u	A1A	2
4	EMI issue	EMI suggest to reserve R436,R199,R444 for EMI test	A1A	2
5	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2
6	CK505 issue	SWAP SRC3 and SRC9	A1A	2
7	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2
8	CK505 issue	Remove U19/Pin48 (no use)	A1A	2
9	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2
10	CK505 issue	remove SATACLKREQ function, change R188 value from 475ohm to 22 ohm	A1A	2
11	CK505 issue	FAE : (14M_ICH and SIO_14M) signals trace should be equal length	A1A	3
12	CPU issue	Remove XDP/ITP signals (no use)	A1A	3
13	CPU issue	Retain the termination resistors (R157,R150~R152) on these signals even when ITP700 not implemented.	A1A	3
14	Thermal Trip issue	change Q19/Pin3 net name from THERM_SYS_PWR to SYS_SHDN#	A1A	3
15	CPU FAN issue	change CPU FAN CONN (follow ZC3)	A1A	3
16	CPU FAN issue	Add CPUFAN#_ON to (U28/PIN1)	A1A	3
17	CPU FAN issue	Add Diode D39 and PU +5V for (U28/Pin1)	A1A	3
18	CPU Thermal monitor issue	Add (U27/Pin6) PU to 3V	A1A	3
19	CPU Thermal monitor issue	remove R389, already PU in ICH8	A1A	3
20	CPU Thermal monitor issue	change SMBUS from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA (Q30,Q31)	A1A	3
21	CPU Power issue	stuff C198, unstuff C217 (base on layout location)	A1A	4
22	GMCH Power issue	Short R115~R117,change +VCC_CFXCORE_INT to +1.05V	A1A	8
23	GMCH Power issue	Short R122,R138, remove VCC_RXR_DMI circuit (connect to +VCC_PEG directly)	A1A	9
24	GMCH Power issue	INTEL CRB VCCD_QDAC Filter Modification:change L13 to R125(100ohm), change R145(*0 ohm) to C507(1uF)	A1A	9
25	DDR Power issue	stuff R192, no stuff R191,R193 for SMDDR_VREF_DIMM	A1A	13
26	RTC BAT issue	Change RTC BATTERY CONN CN12(follow to ZC3)	A1A	14
27	ICH8-M Strap issue	Stuff R241, no stuff R266 (Disable Internal VR powering VccLAN1_05, VccCL1_05)	A1A	14
28	ICH8-M HDA issue	add R283,R465,R463,R267 for MDC module (base on Intel Design Giude)	A1A	14
29	ICH8-M issue	PU RCIN# to +3V	A1A	14
30	ICH8-M issue	Remove ICH8-M GLAN/SATA1/SATA2 circuit (no use)	A1A	14
31	ICH8-M issue	change net name (U31/Pin2) from VR_PWRGD_CLKEN# to VR_PWRGD_CK410#	A1A	16
32	ICH8-M issue	Remove SATACLKREQ#(U32/Pin:AG13),RI# (U32/Pin:AF17) ;{no use}	A1A	16
33	ICH8-M issue	no support iAMT, remove SMB_CLK_ME,SMB_DATA_ME	A1A	16
34	ICH8-M issue	change DOCKIN#_ICH_R PU from +3V to +3V_S5	A1A	16

PROJECT : ZU1
Quanta Computer Inc.

PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: A1
MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09

CHANGE LIST SHEET 1

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
35	Power sequence issue	change (U21/Pin5) from +3V to +3VSUS (refer to ZC1)	A1A	16
36	ICH8-M issue	Remove WOL_EN (U32/Pin:AG19) -no use	A1A	16
37	ICH8-M issue	Remove SUSM# (used to control power planes to the Intel AMT sub-system)	A1A	16
38	ICH8-M issue	Remove (1)ME_EC_ALERT# (2)EC_ME_ALERT (no use)	A1A	16
39	ICH8-M issue	connect LAN_RST#(U32/Pin:AH20) to PLTRST# (If no use internal LAN MAC connect LAN_RST# to PLTRST#)	A1A	16
40	ICH8-M issue	change DOCKIN#_ICH_R PU from +3V to +3V_S5	A1A	16
41	EMI issue	EMI suggest C373 from 0.1u to 10uF	A1A	17
42	ICH8-M Power issue	Reserve R308,R313 for +1.5V MDC module	A1A	17
43	LAN Power issue	change LAN power from +3V_LAN_S5 to +3V_S5	A1A	18
44	LAN Power issue	BCM FAE: Pull up Vmainprsnt (U10/Pin53) to the system main power (3.3v), but not the standby power	A1A	18
45	LAN Power issue	BCM FAE: Change capacitance value from 47-uF to 10-uF.	A1A	18
46	LAN Power issue	BCM FAE:stuff R30,no stuff R47(in order to pull up C90,C86 and Q16/pin 3 to 3V_LAN rail)	A1A	18
47	LAN Switch issue	EMI suggest C59 from 0.1u to 10uF	A1A	18
48	LAN Switch issue	Add Diode D4 for isolation (Dockin#)	A1A	18
49	LAN Switch issue	change LAN Switch from MAX4892 to PI3L500	A1A	18
50	LAN Transformer issue	change TRANSFORMER GND(U3/Pin15,18,21,24) to MGND	A1A	18
51	LAN CONN issue	Change CONN P/N (follow ZC1)	A1A	18
52	LAN CONN issue	change CONN GND(CN19/Pin13,14) to MGND	A1A	18
53	CRT issue	change C439, C440,C7,C441 to 30~50pF(default :no stuff)	A1A	19
54	CRT issue	Change CRT_SENSE# from CRT CONN Pin11 to Pin5 (follow Acer define)	A1A	19
55	CRT issue	Change CRT CONN P/N(follow ZC1)	A1A	19
56	CRT issue	change R16,R17 from 2.7k to 2.2k ; R10,R12 from 39 to 0 ohm	A1A	19
57	CRT issue	change U1 from CM2009 to IP4772	A1A	19
58	LVDS issue	change CCD function from USB7 to USB8	A1A	20
59	LVDS issue	Change C12 from CH6102M9900 to CH61004M3E5 (refer to ZC3)	A1A	20
60	TV issue	Change CN17 CONN P/N (follow ZC1)	A1A	20
61	SDVO issue	Change R51,R56 value from 2.2k to 4.7k (FAE suggest R value from 4K~9K)	A1A	21
62	PCMCIA issue	refer to BL3. Add G_RST# circuit.	A1A	22
63	PCMCIA issue	FAE suggest R189's value under 47 ohm.	A1A	22
64	Card reader issue	no stuff R496,R522	A1A	23
65	Card reader issue	FAE suggest R503's value under 47 ohm.	A1A	23
66	Card reader issue	Remove U39/Pin99, no use (XMDAT4B is for 8 bit MMC,remove it.)	A1A	23
67	Card reader issue	Change C593 from 0.1u to 10uF,EMI suggest add C587 0.1uF	A1A	24
68	PCMCIA issue	change PCMCIA CONN (follow BH1)	A1A	24

PROJECT : ZU1
Quanta Computer Inc.

PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: A1
MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09

CHANGE LIST SHEET 2

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
69	PATA ODD issue	change R253 from 0 to 33ohm	A1A	26
70	PATA ODD issue	Add C326,C327,C344 for +5V	A1A	26
71	PATA ODD issue	Remove D23, already add in page29	A1A	26
72	Mini Card issue	Reserve R349,R350,R337,R345,R344,R338,R339 for debug card use	A1A	27
73	Mini Card issue	Add (CN28/Pin39,41) to +3V_WL_VDD (follow ZO1)	A1A	27
74	Mini Card issue	Remove (CN28/Pin36,38) USB circuit	A1A	27
75	Mini Card issue	Remove (CN28/Pin46) BT LED	A1A	27
76	Mini Card issue	Remove 0.1uF (CN28/Pin23,25), already in WL module	A1A	27
77	Bluetooth issue	SI suggest to remove 22pF*2 (CN5/Pin3,4)	A1A	27
78	USB CONN issue	SI suggest to remove 22pF*2 (CN11/Pin2,3)	A1A	27
79	EC issue	Change EC from WPC8769 to WPC8763	A1A	28
80	EC issue	change U7/Pin5,6 from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA	A1A	28
81	EC issue	Remove ME_EC_ALERT#	A1A	28
82	EC issue	FAE:Change U14/Pin80 from +3VPCU to +A3VPCU	A1A	28
83	EC issue	change C130,C131 from 6.8p to 5.6p	A1A	28
84	EC issue	Add D18 for HWPG_CPUIO	A1A	28
85	Finger Printer issue	SI suggest to remove 22pF*2 (CN9/Pin2,3)	A1A	29
86	SuperIO issue	Remove PPT PU 4.7K circuit (already in docking)	A1A	30
87	Audio issue	Change Serial resister R484,R485 value from 22 ohm to 33 ohm	A1A	31
88	Audio issue	reserve R513 to reduce ringing	A1A	31
89	Audio issue	Refer to ZD1, change R546,R520,R545,R519 to 10k	A1A	32
90	Docking issue	(CN22/Pin18,Pin19):(1)Remove Level-shift circuit (2)change Power from +3V to +2.5V (3)stuff 2.2k	A1A	33
91	Docking Power issue	Add .1u*7 , 10U*1 for VA	A1A	33
92	Docking issue	Reserve U25 for docking PWRBTN#	A1A	33
93	Docking issue	Change Docking Pin141/142 from USB5 to USB3	A1A	33
94	Docking issue	PL DVI_DET 100k to GMD (CN22/Pin20)	A1A	33
95	Docking issue	Change LAN pin define	A1A	33
96	Audio issue	Change CN29,CN30,CN31 P/N (Base on Acer request)	A1B	32
97	ICH8-M Strap issue	Change INTVRMEN from PD to PU	B1C	14
98	Leakage issue	add D43,D44 to stop leakage from EC to SB	B1C	16
99	ICH8-M issue	change DOCKIN# from GPIO7 to GPIO12	B1C	16
100	Power sequence issue	short PWROK_EC to MPWROK	B1C	16
101	ICH8-M issue	PU GPIO10 to +3V, PD GPIO14 to GND	B1C	16
102	ICH8-M issue	remove R229,R233,C355	B1C	16

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
103	PCMCIA issue	Reserve R572 for debug use	B1C	22
104	1394 issue	Change R271,R306,R307 from 56.2 to 5.1k ohm (fix 1394 can't detect issue)	B1C	25
105	Mini Card issue	no stuff R353,R348,R356	B1C	27
106	Mini Card issue	need support BCM WL Module, Connect CN28/Pin40 to GND	B1C	27
107	EC issue	SWAP GPIO1 and GPIO3	B1C	28
108	EC issue	Change CN10/Pin1 from +3V to +3VPCU	B1C	28
109	LED issue	Base on Me request, change PWR/SUS/BAT LED type	B1C	29
110	Audio issue	Stuff R330 to fix Internal SPK issue (floating GND issue)	B1C	27
111	Docking issue	Add R566 for Debug use	B1C	33
112	Mini Card issue	ME request :change CN28 P/N from DFHD52MS049 to DFHS52FR082 (9.0mm to 9.9mm)	B1D	27
113	GMCH Power issue	Change C143 from CH71002MJC8 to CH7102MT804 (Z-limit issue,H2.9mm to H1.5mm)	B1D	9
114	CPU Clock issue	Set CPU Frequency to auto selection (no stuff R179,R198,R447)	C2A	2
115	S5_ON issue	Change S5_ON control circuit (follow ZO1/ZD1)	C2A	34
116	CK505 issue	change CK505 VDD_IO from +1.05V to +1.25V. Because VDD_IO will drop out when high loading	C2A	2
117	G995 issue	Add level shift circuit (follow ZO1), remove D39,no stuff R383.	C2A	3
118	BIOS EMI issue	FAE suggest add 22 Ohm dumping resistors R596,R597 to avoid potential EMI problem	C2A	28
119	LAN issue	Base on BCM IEEE test result, change RDAC value (R42) from 1.24k to 1.18k	C2A	18
120	Audio issue	Acer change internal Mic solution to Fortemedia,Remove CN33,D29,D30,R342,R506,C400,C586	C2A	32
121	DVI Detect issue	Intel suggest:Add hotplug circuit to DVI_DET (follow ZC1)	C2A	21
122	ICH8M issue	Intel Suggest :ICH8M CPIO20 should not be pulled HIGH.Remove BOARD_ID3 circuit(remove R474,R475)	C2A	16
123	SDVO issue	Intel Suggest :Follow Intel New Guideline(MoW 48 update) Change R51,R56 from 4.7K to 3.9K ohm	C2A	21
124	GMCH Power issue	Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW.reserved 0 ohm resister (R576)	C2A	8
125	SuperIO issue	Intel Suggest :All LPC devices support LPCPD# protocol, stuff D7	C2A	30
126	ICH8M issue	no stuff R259 to prevent leakage issue	C2A	16
127	EMI issue	EMI suggest add C647 to prevent noise for PR_STS	C2A	33
128	EMI issue	EMI suggest to add .1u *2 to prevent noise (+3V)	C2A	30
129	EMI issue	EMI suggest to add 2.2ohm BST resister (PR153) in 1.8V power	C2A	37
130	EMI issue	EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)	C2A	30
131	ME issue	ME request add three pad for fix wire (PAD20,21,22)	C2A	30
132	DVI issue	remove the U11,R57,R52,C109 to save layout space.	C2A	21
133	Power monitor issue	D16 not necessary if 3V/5V fail, EC can't work.	C2A	28
134	S3 resume POP sound issue	change C619 from CH61004M2E8 to CH5222K9A09 to solve S3 resume POP sound issue	C2A	31
135	POP sound issue	no stuff R525,D41, add bypass R577 to solve pop sound issue	C2A	31
136	AUDIO issue	no stuff D27	C2A	32

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
137	Audio issue	change R546/R520 from 10k to 9.1k	C2A	32
138	GMCH POWER issue	Change Crestline VCC_AXM from +1.25V to +1.05V, reserved 0 ohm resister (R578)	C2A	8
139	XTAL issue	Base on vendor-FCE suggestion, change C580/C579 from CH01206JB05 (12p) to CH02206JB08 (22p)	C2A	25
140	XTAL issue	Base on vendor-FCE suggestion, change C310/C299 from CH03306JBD7 (33p) to CH02706JB06 (27p)	C2A	2
141	XTAL issue	Base on vendor-FCE suggestion, change C130/C131 from CH-5606TB01 (5.6p) to CH01006JBD1 (10p)	C2A	28
142	EMI issue	EMI request: DEL PR120 2.2ohm(CS-2203F911), stuff PC98	C2A	37
143	EMI issue	EMI request: reserve .1U for (CN19/pin9,10)	C2A	18
144	EMI issue	EMI request: reserve L-C footprint for debug use (R52,C650)	C2A	20
145	debug issue	Stuff R349 , R350 for debug use	D3A	27
146	Modem wake from S3 fail issue	Change CN14/pin 2 from +3v to +3v_s5.	D3A	31
147	CableSence circuit issue	Add CableSence circuit (unstuff R78)	D3A	18
148	CableSence circuit issue	Add CableSence circuit (reserve R579)	D3A	18
149	LED type issue	Base on SMT-ME request, change LED type to 2 in 1,DEL LED4,LED5,LED6,LED7,R570,R571,Add LED2,LED3	D3A	29
150	SW button issue	Base on ASSEMBLY -Line request, remove SW1, add G2 footprint	D3A	29
151	change Modem capacitor to meet safety standard	change C37,C48 from CH147GK0I09 to CH147GK0I00	D3A	33
152	Power issue	The system side should have a diode (D45,D46) to block the AC adaptor power and ezDock.	D3A	33
153	EMI issue	Change L4,L5,L6 from CX8BA220007 to CX8BA470003	D3A	19
154	DVI issue	remove U13,R68,R75,R73,C98 for layout space issue	D3A	21
155	ASF issue	Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)	D3A	16
156	SMT B open issue	(1)Remove footprint for D41,D42,R525. DEL R577 (0 ohm) (2) Remove net SECNTL	D3A	31
157	CableSence circuit issue	change LAN Low power pin from GPIO47 to GPIO52	D3A	28
158	LAN switch issue	Change U6 from AL000500005 to AL000500030 (change to 8KV solution)	D3A	18
159	Change 965GM from ES sample to QS sample	Change U29 P/N from AJ0QN120T37 to AJ0QP200T09	D3A	5~11
160	Change ICH8M from ES sample to QS sample	Change U32 from AJ0QM740T31 to AJ0QN230T10	D3A	14~17
161	Audio Jack issue	change CN30,CN31,CN32 footprint from AUDIO-010164FR006GX53XL-C-8P to AUDIO-JA60331-X39T4-7F-8P	D3A	32
162	docking sometimes can't detect DVI device issue	change R51,R56 from 3.9k(CS23902FB14) to 4.7k(CS24702JB38).	D3A	21
163	EMI issue	EMI suggest, add common Choke, co-lay R795,R796	D3A	27
164	Audio Jack issue	Change CN30 P/N from DFTJ06FR017 to DFTJ06FR059	D3A	32
165	Audio Jack issue	Change CN29 P/N from DFTJ06FR019 to DFTJ06FR061	D3A	32
166	Audio Jack issue	Change CN31 P/N from DFTJ06FR018 to DFTJ06FR060	D3A	32
167	backlight control issue	Follow ZO1 design,Remove R24 footprint, DEL D3(BC000316Z07).Add R73,Q36,Q37	D3A	20
168	docking CRT flicker issue	Reserve C98,R525 for docking CRT flicker issue	D3A	19
169	EMI issue	EMI suggest add C652(0.1uF)	D3A	19
170	system sometimes will no backlight issue .	For short term solution:change R22 from 10k(CS31002JB28) to 1K (CS21002FB24)	D3A	

PROJECT : ZU1
Quanta Computer Inc.

PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: B/C
MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Kin Wang	DOCUMENT NO:	DATE :2006/12/09

CHANGE LIST SHEET 5

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
171	Quanta DSC Team issue	Base on DSC command, change CN22 P/N from DFHDF8MS000 to DFHDF4MS000	D3A	33
172	rise time of LCDVCC is >0.5ms and <=10ms.	change U2 from AL004280000(AAT4280IGU-3-T1) to AL004280018(AAT4280IGU-1-T1).	D3A	23
173	Card reader issue	no stuff 43K(CS34302JB19):R562,R527,R533,R538,R539,R565,R561,R540,R498,R497,R500,R552,R555	D3A	23
174	Card reader issue	no stuff 10k(CS31002JB28) : R560	D3A	23
175	Card reader issue	Change R547 from 43k (CS34302JB19) to 8.2k (CS28202JB14)	D3A	23
176	Card reader issue	Change R528 from 10K(CS31002JB28) to 43K(CS34302JB19)	D3A	23
177	Shortage issue	Change R125 from CS11003B900 (100 ohm 0.1%) to CS11003F953(100 ohm 1%)	D3A	9
178	EMI issue	EMI request add two of clip(FDTA1003014) in PAD17 and PAD19 for EMI issue	D3A	30
179	DPST issue	Acer inform no support DPST in C build, remove R15	D3A	20
180	Shortage issue	Andy inform change PR116 from CS42102FB00 to CS42002FB12	D3A	34
181	ICH8M Power issue	ICH8M Internal VR should not be disabled.no stuff R241, stuff R226	D3A	14
182	implement it for CPU protect in C build.	Change R111 from *2.2k to 0ohm,Change R107 from 56.2(CS05622FB22) to 1k(CS21002FB24)	D3A	3
183	Battery life issue.	Battery life issue. Disable ICH8M Internal VR (LAN). stuff R241, no stuff R226 for C-build	D3A	14
184	Change EMI Spring Material	ME request, change EMI Spring from FDTA1003014 to FDZU1002010	E3A	30
185	C-Test SMT open issue	C-test SMT open issue, remove PAD18	E3A	30
186	ZR1 issue	Change CN2 Pin define to cover production line issue(Inverter short with signal to burn system)	E3A	20
187	C-Test SMT open issue	Change PD9,D46 footprint from SBM1040-3P to SBM1040-3P-ZU1 for SMT C-test open issue	E3A	33 & 39
188	Change NB P/N for RAMP	Change U29 P/N form AJ0QP200T09 to AJSLA5T0T05	E3A	5~11
189	Change SB P/N for RAMP	Change U32 P/N from AJ0QN230T10 to AJSLA5Q0T05	E3A	14~17
190	Material Lead issue	Change R214 from CS02403F908 to CS02403F916 (Lead free)	E3A	14
191	G995 failure rate issue	Add C653 base on G995 failure rate issue	E3A	3
192	Run-in auto shot down issue	ICMNT connect to EC pin100 , reserve R570 0ohm for debug use, Add C654 to avoid noise	E3A	28 & 39
193	remove wake on lan for Mini PCIE function.	Base on Acer demand, remove wake on lan for Mini PCIE function.no stuff Q25,R357	E3A	27
194	move D15~D18 location for FFC cable issue	Remove footprint (D16), Remove net (HWPG_3/5VPCU),no stuff PR119	E3A	28 & 34
195	LED issue	Change LED2, LED3 type base on ME request, Add R800,R801	E3A	29
196	HDD Mylar issue	Change C542 from 0805(CH6102K9A01) to 0603(CH6101M9905) base on ME request(HDD Mylar issue)	E3A	2
197	Docking issue	Change Q4,Q5 Pin2 from +3V to +3VSUS .(Docking side pull up to +3VSUS plane)	E3A	33
198	Docking issue	change C451,C452 from 0.1uF (CH41002KB93) to 0 ohm (CS00002JB38)(R802,R803)	E3A	33
199	Disable LAN Low Power mode	Stuff R78(CS24702JB38)	E3A	18
200	EOL issue	Change C453 from CC1210 (CH61004M3E5) to CC1206 (CH61004M2E8)	E3A	33
201	LPC CONN issue	confirm with BIOS-CM, no need LPC dedug CONN,Remove CN6,R432 footprint to save space for layout.	E3A	28
202	LAN_RST# issue	(1)Stuff 10k for R204(2)Don't stuff R456(3)Don't stuff R247	E3A	16
203	PO" sounds when insert PCMCIA card	Add 0 ohm (R804) for PCMSPK	E3A	22
204	ESD issue	Stuff D38 for CRT port	E3A	19

PROJECT : ZU1 Quanta Computer Inc.	PROJECT : ZU1	APPROVE BY : Kin Wang	DRAWING BY:Barry Lee	Stage: C / Ramp
	MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09

CHANGE LIST SHEET 6

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
205	PCMCIA POP SOUND issue	Refer to BU1, add circuit for POP sound issue	E3A	24
206	GLAN issue	Stuff R232 (CS02492FB29), The GLAN_COMPO/GLAN_COMPI connection to 1.5-V rail through the resistor remains	E3A	14
207	ESD issue	change LED type (follow B stage) DEL LED2,LED3, Add LED4~7	E3A	29
208	ESD issue	change ESD protect Diode from location LED/B to MB	E3A	29
209	Disable LAN Low power mode	Base on PM suggestion, add serial 0 ohm (R806) for debug use.(no stuff)	E3A	18
210			E3A	
211			E3A	
212			E3A	
213			E3A	
214			E3A	
215			E3A	
216			E3A	
217			E3A	
218			E3A	
219			E3A	
220			E3A	
221			E3A	
222			E3A	
223			E3A	
224			E3A	
225			E3A	
226			E3A	
227			E3A	
228			E3A	
229			E3A	
230			E3A	
231			E3A	
232			E3A	
233			E3A	
234			E3A	
235			E3A	
236			E3A	
237			E3A	
238			E3A	

PROJECT : ZU1
Quanta Computer Inc.

PROJECT : ZU1	APPROVE BY : Kin Wang	DRAWING BY:Barry Lee	Stage: Ramp
MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2007/03/29

CHANGE LIST SHEET 7