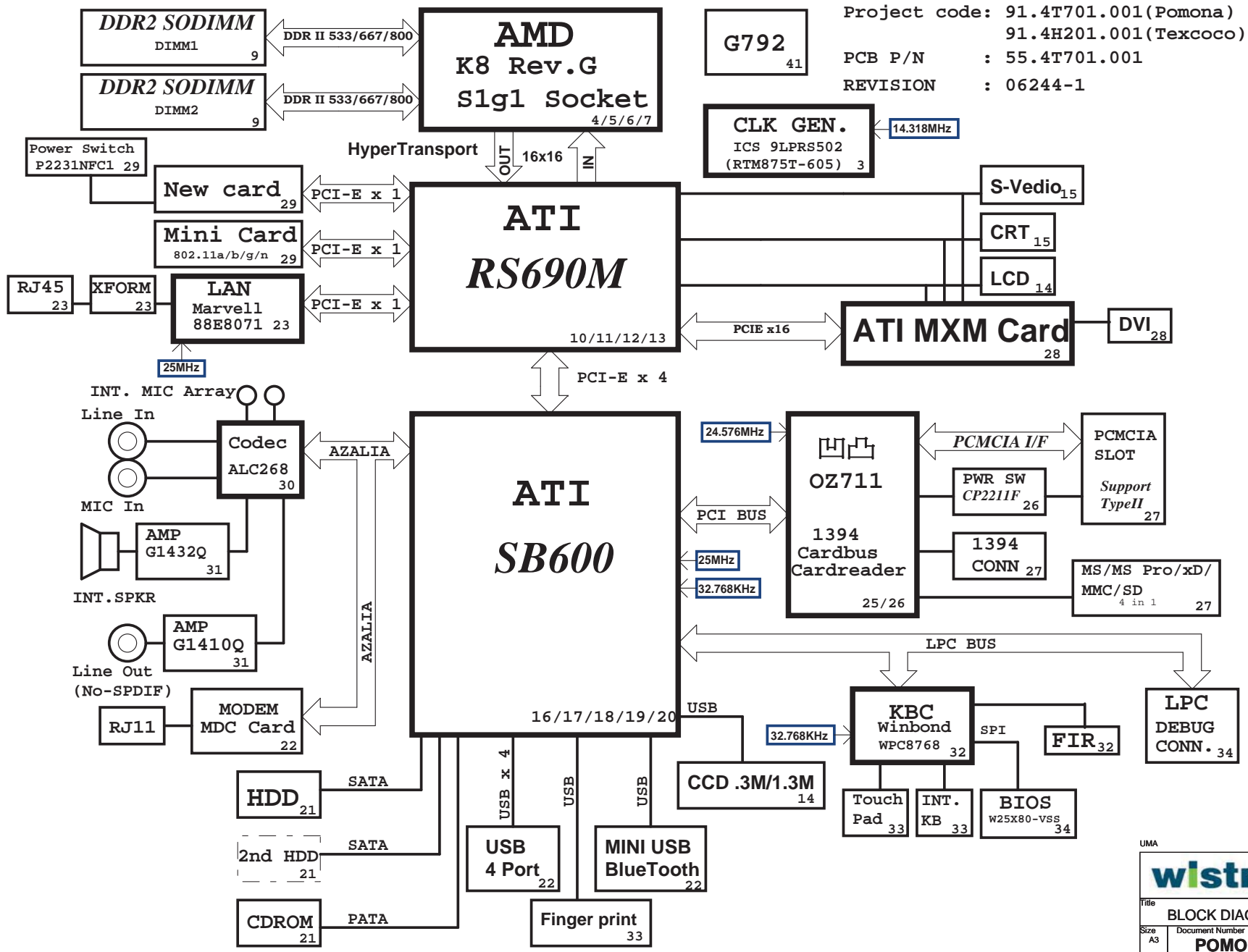


Pomona/Texcoco Block Diagram

<http://hobi-elektronika.net> Ver. -1

Project code: 91.4T701.001 (Pomona)
91.4H201.001 (Texcoco)
PCB P/N : 55.4T701.001
REVISION : 06244-1



PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE
ISL6264 38/39

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC
TPS51124 47

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

SYSTEM DC/DC
ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO
TPS51100 48

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO
APL5915 48

INPUT	OUTPUT
3D3V_S5	1D2V_S5
3D3V_S0	2D5V_S0
3D3V_S0	1D5V_S0

SYSTEM LDO
ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger
ISL6255 42

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

UMA

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Hsichih, Taipei

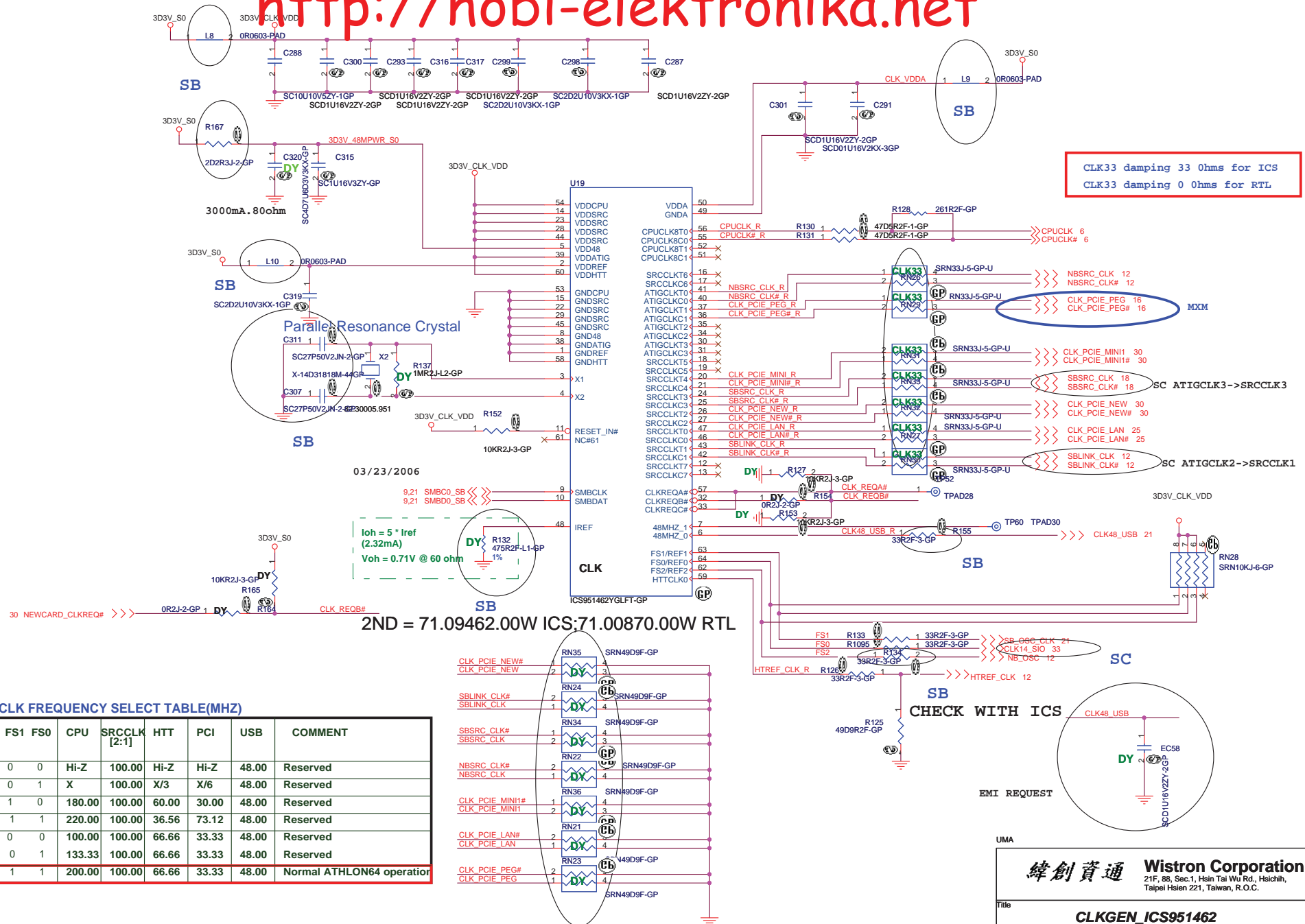
Title: BLOCK DIAGRAM
Size: A3, Document Number: POMONA/TEXCOCO, Rev: 1
Date: Thursday, March 29, 2007, Sheet: 1 of 49

<http://hobi-elektronika.net>

SA: 07/31/06 Start

UMA

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CHANGE HISTORY					
Title					Rev
Size	Document Number	Pomona/Texcoco			Rev
A3					1
Date: Thursday, March 29, 2007					
				Sheet	2 of 49



CLK33 damping 33 Ohms for ICS
CLK33 damping 0 Ohms for RTL

03/23/2006
Ioh = 5 * Iref (2.32mA)
Voh = 0.71V @ 60 ohm
2ND = 71.09462.00W ICS:71.00870.00W RTL

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

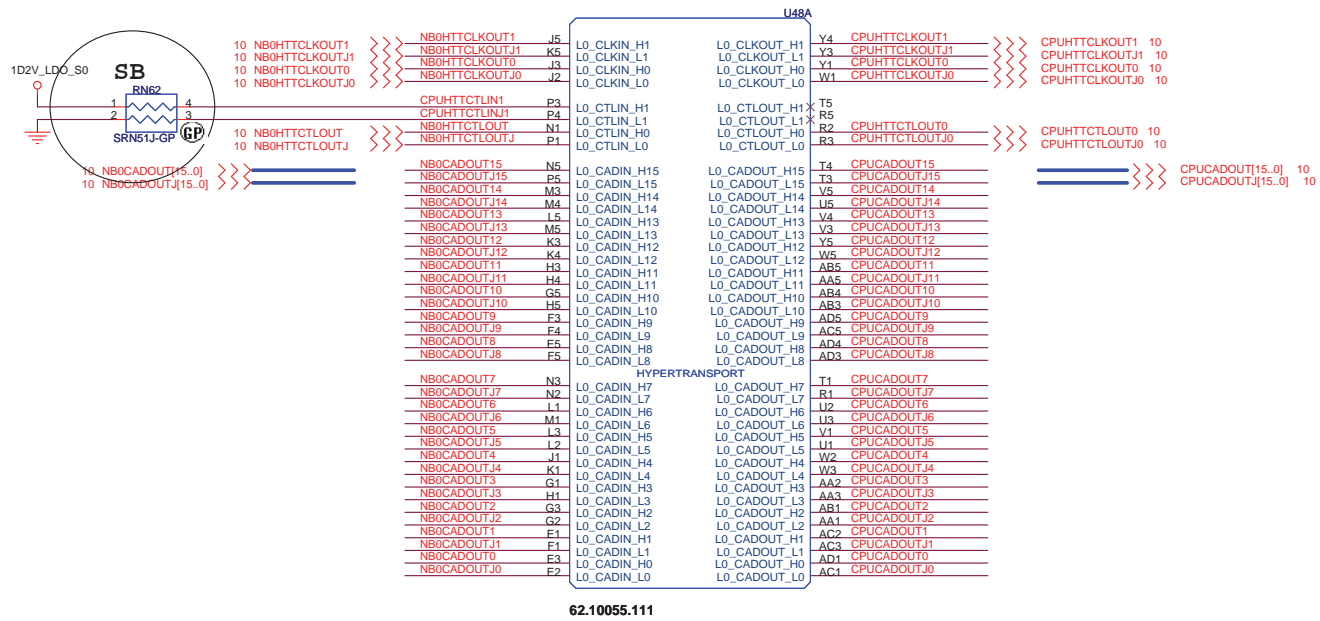
UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN_ICS951462**

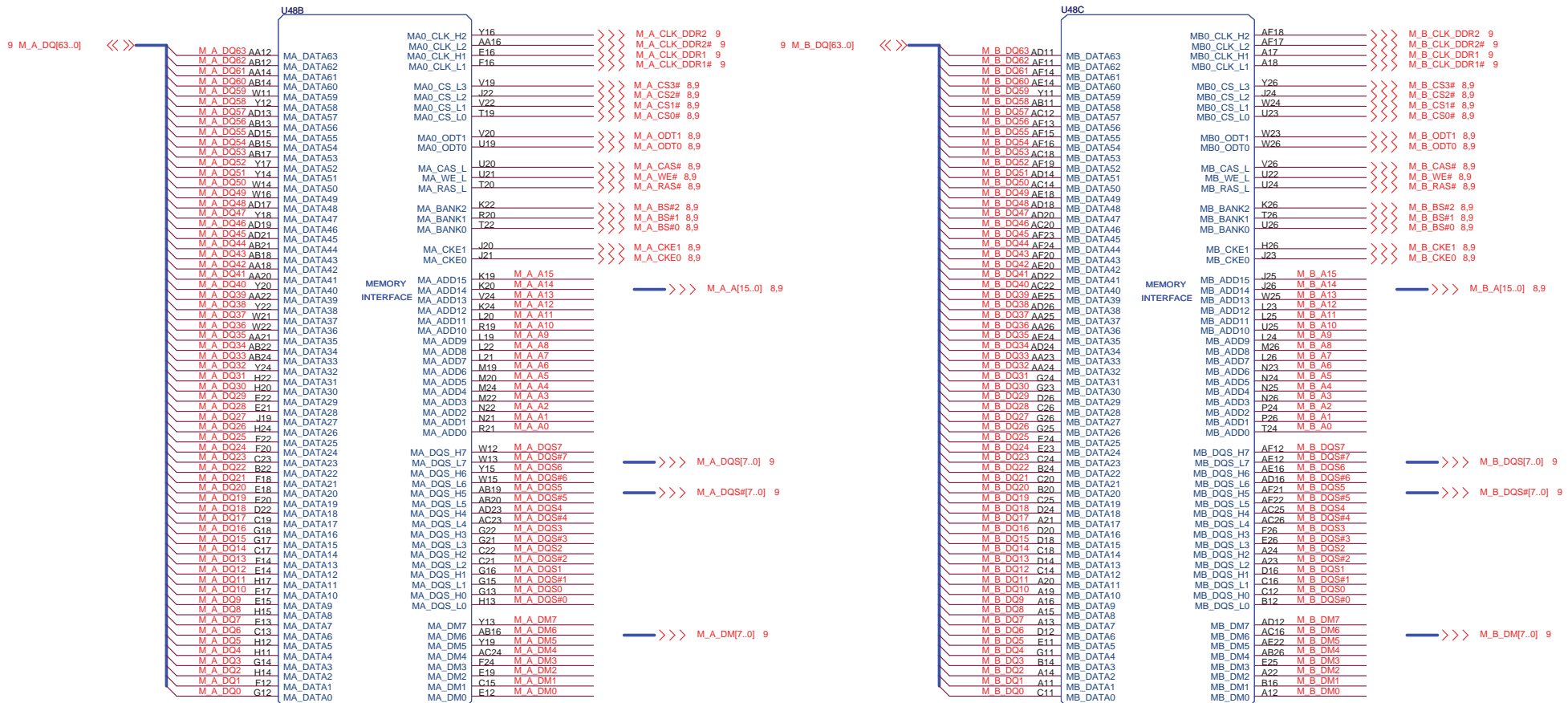
Size A3 Document Number **Pomona/Textcoco** Rev 1

Date: Thursday, March 29, 2007 Sheet 3 of 49



UMA

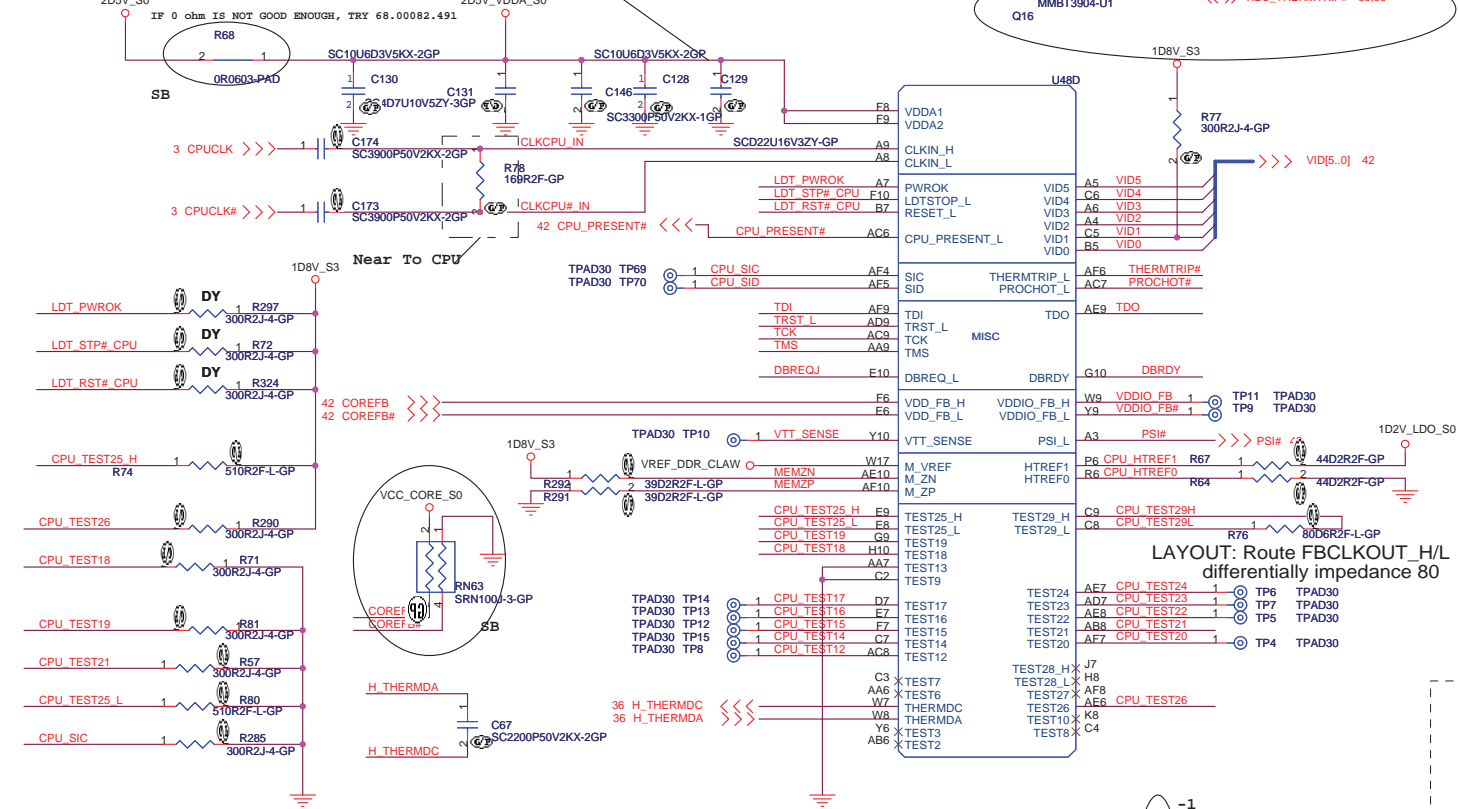
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU(1/4)_HyperTransport I/F			
Size A3	Document Number Pomona/Textcoco	Rev 1	
Date: Thursday, March 29, 2007		Sheet 4	of 49



UMA

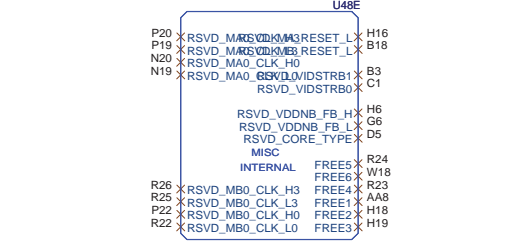
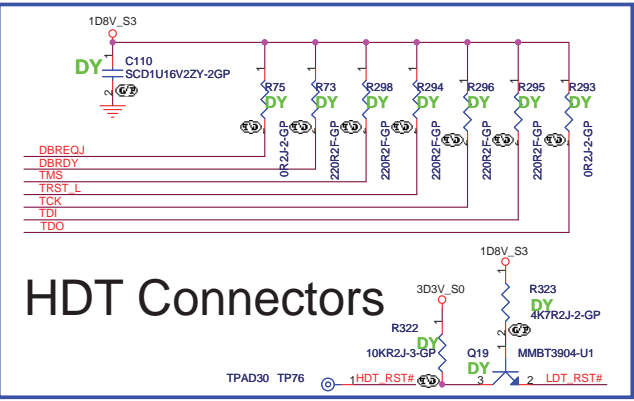
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU(2/4)_DDR2	
Title	Rev 1
Size A3	Document Number
Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 5 of 49

LAYOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



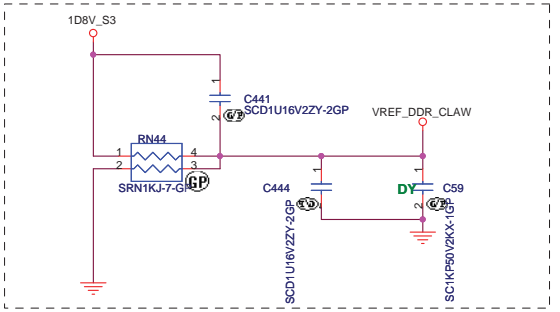
SC

SC CHANGE TO 680



LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

VREF_DDR2_CPU

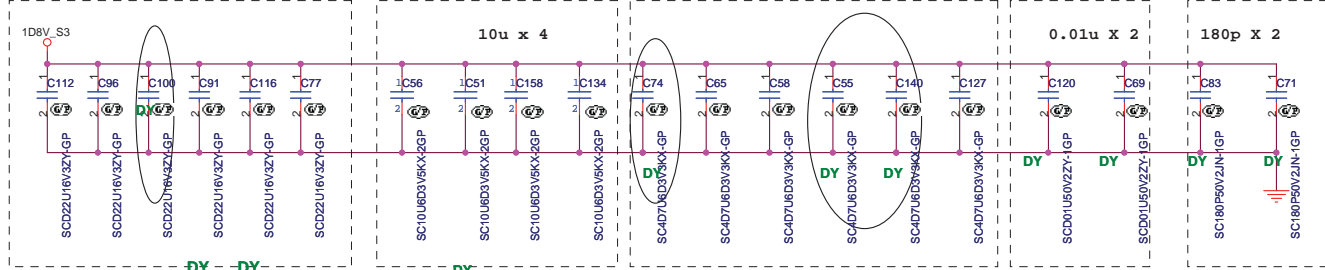


LAYOUT: Locate close to CPU.

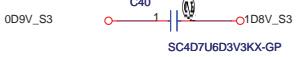
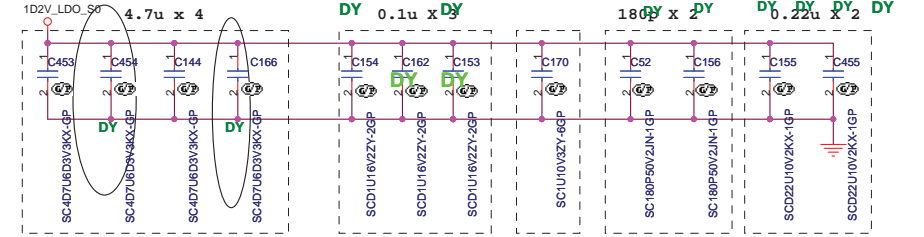
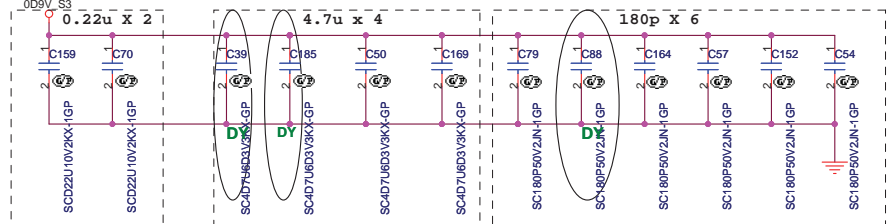
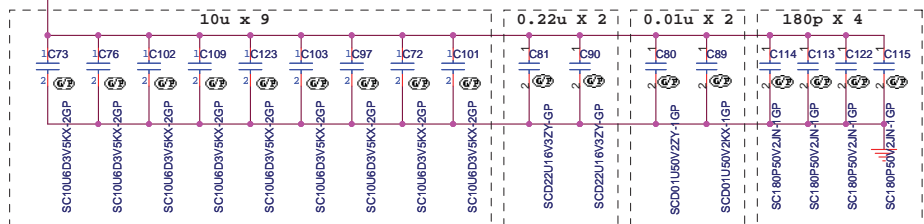
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(3/4)_Control & Debug		
Size	A3	Document Number	Pomona/Texcoco
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VCC_CORE_S0 LAYOUT: Place on backside of processor.



UMA

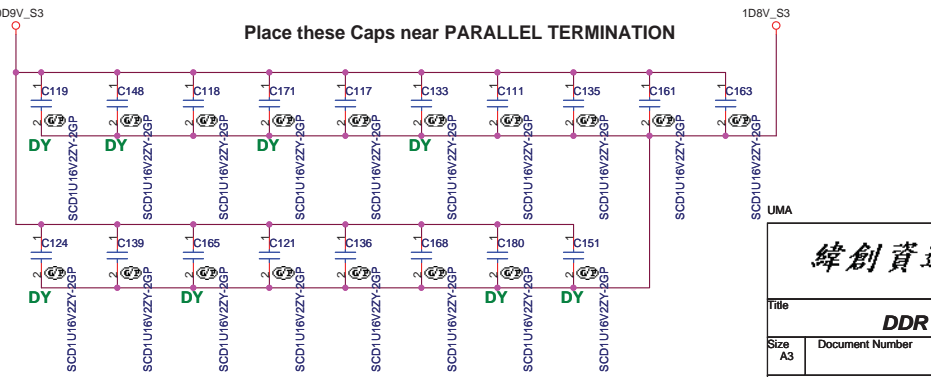
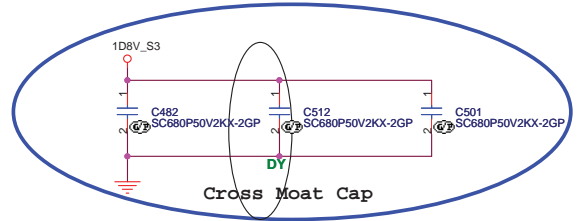
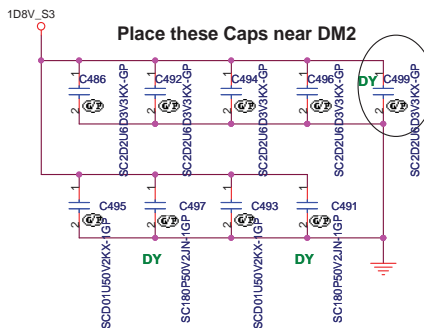
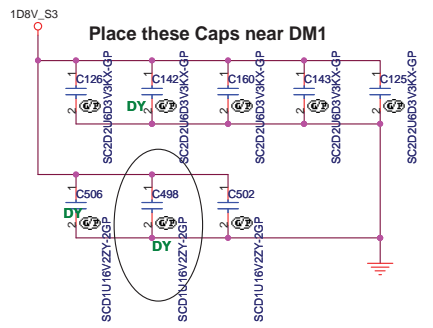
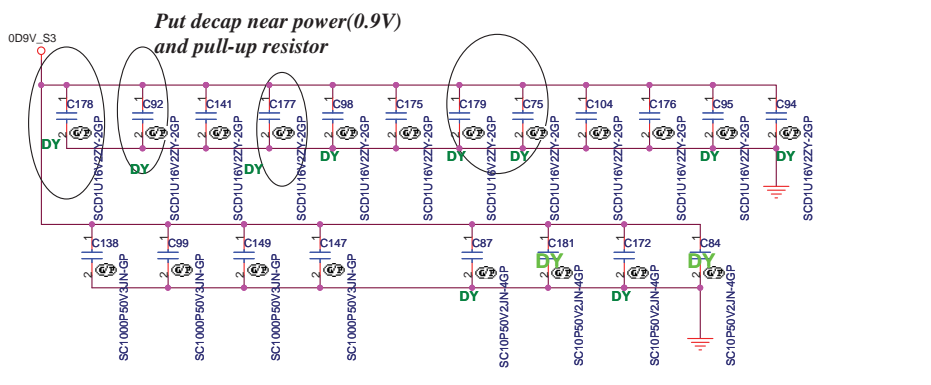
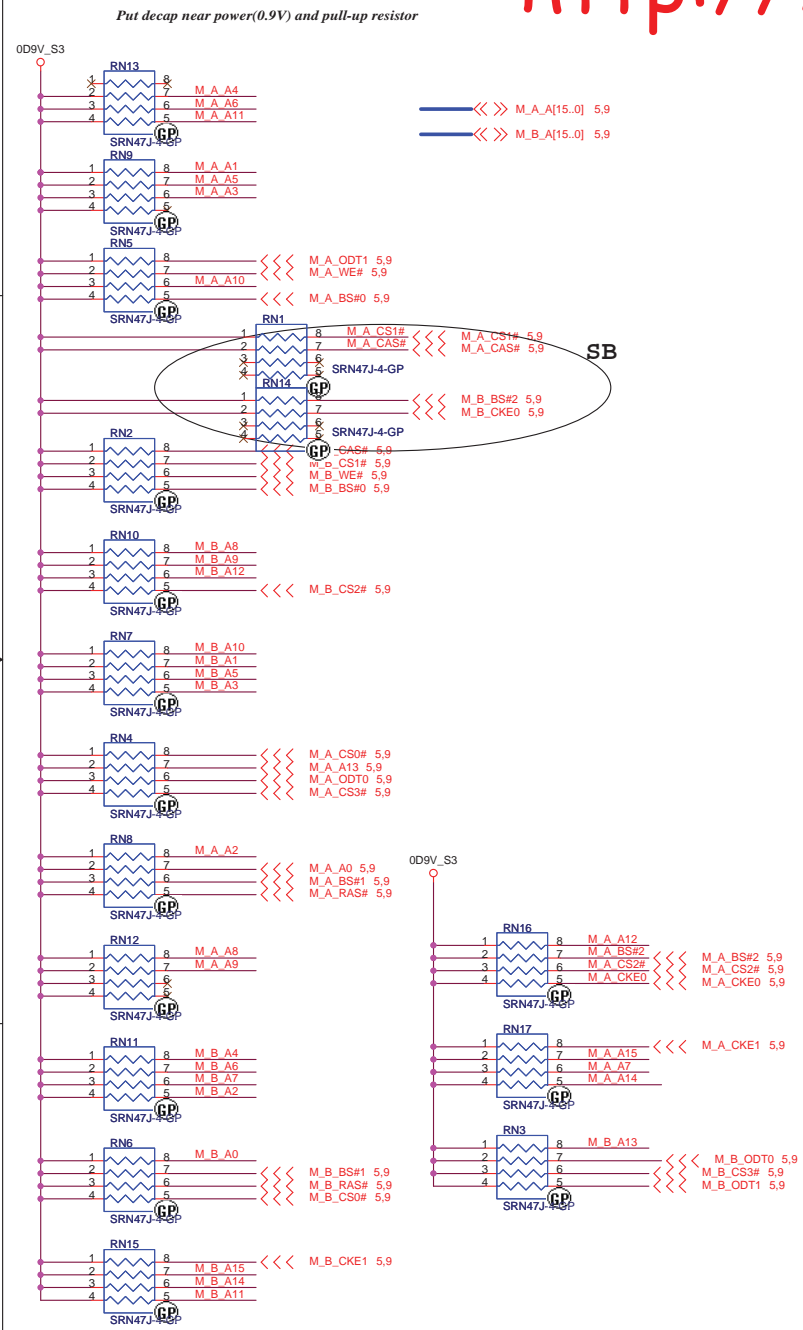
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4)_Power**

Size: A3 Document Number: **Pomona/Textcoco** Rev: 1

Date: Thursday, March 29, 2007 Sheet 7 of 49

PARALLEL TERMINATION

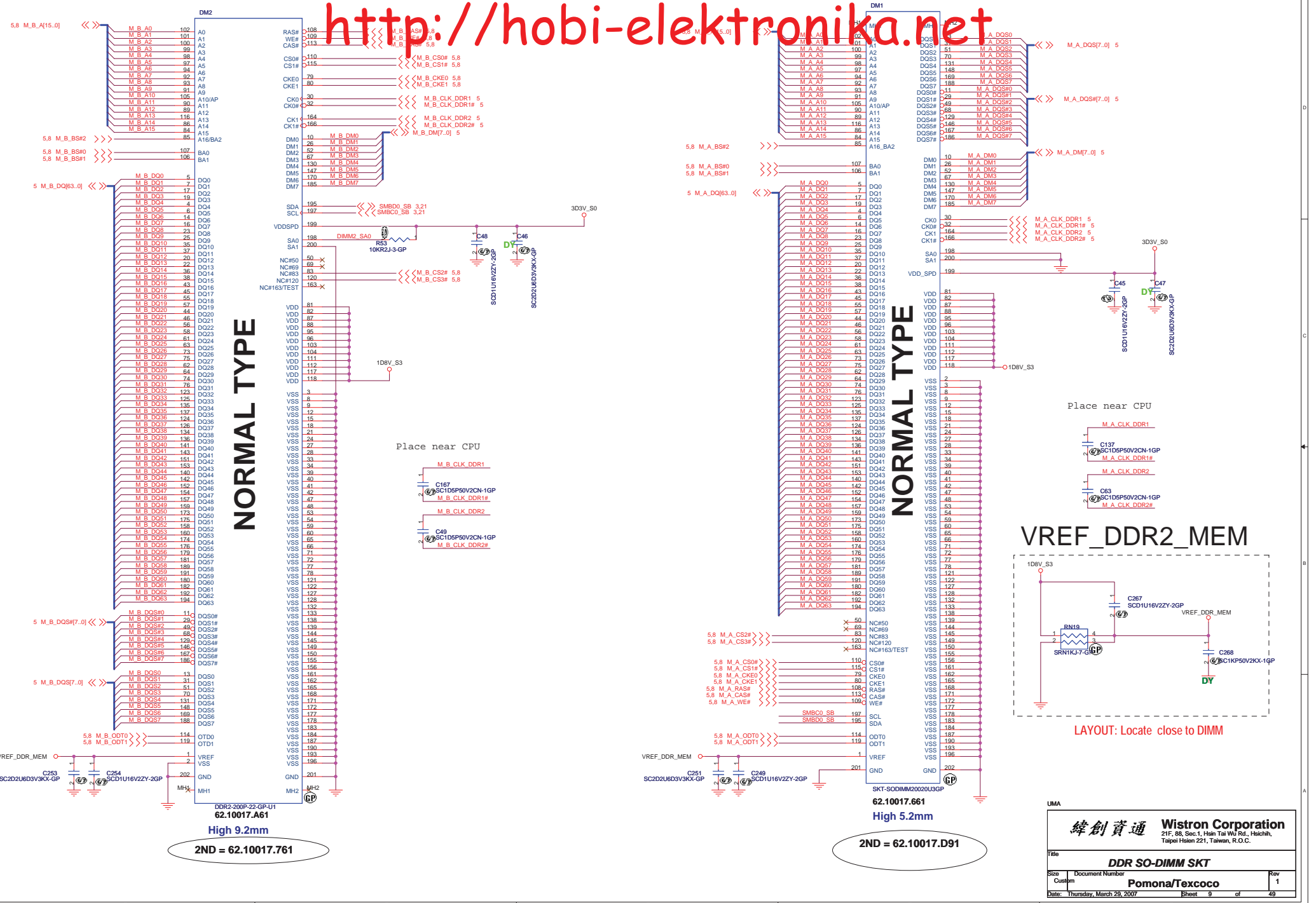


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DAMPING & TERMINATION**

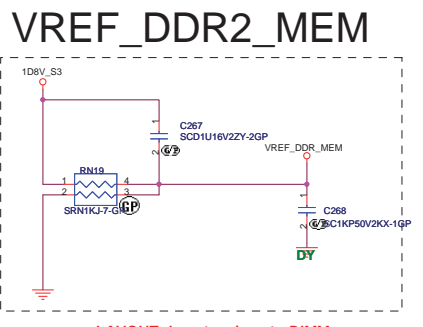
Size A3 Document Number: **Pomona/Textcoco** Rev 1

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2ND = 62.10017.761

2ND = 62.10017.D91



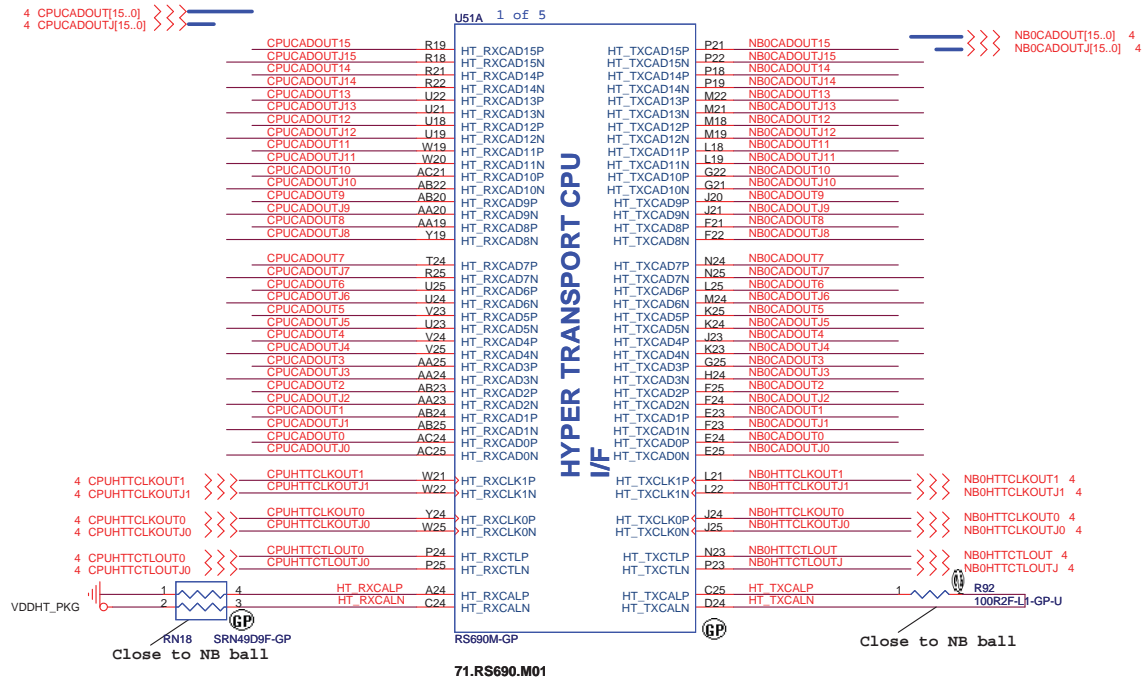
LAYOUT: Locate close to DIMM

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DDR SO-DIMM SKT		
Docu	Document Number	Rev
Custom	Pomona/Texcoco	1
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CPU TO NB

NB TO CPU



UMA

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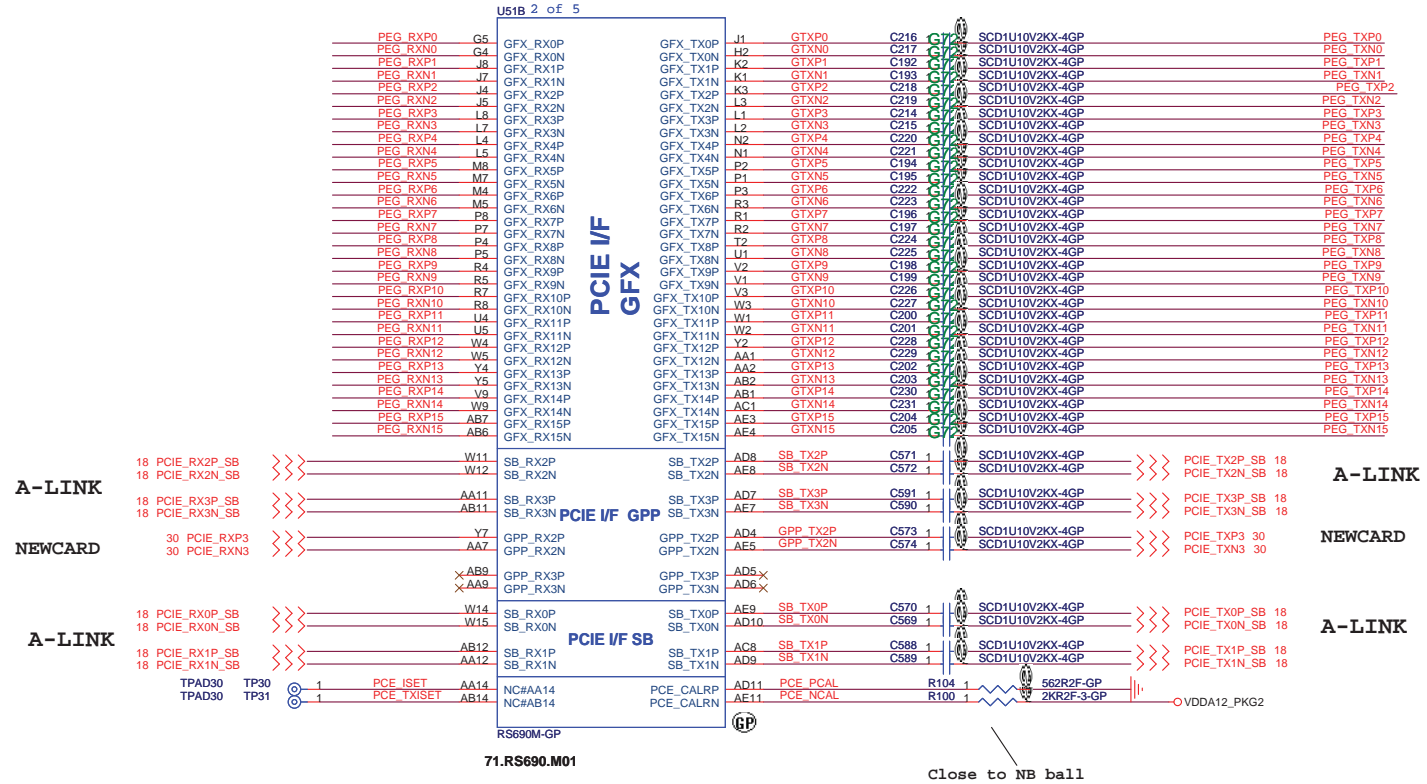
Title: **NB-RS690M HT**

Size A3 Document Number **Pomona/Textcoco** Rev 1

Date: Thursday, March 29, 2007 Sheet 10 of 49

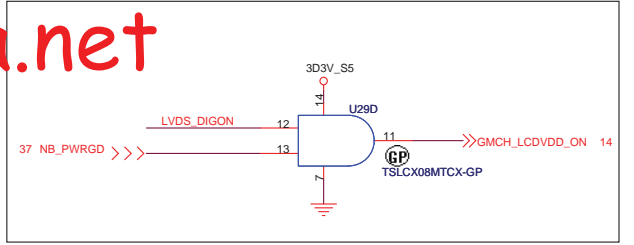
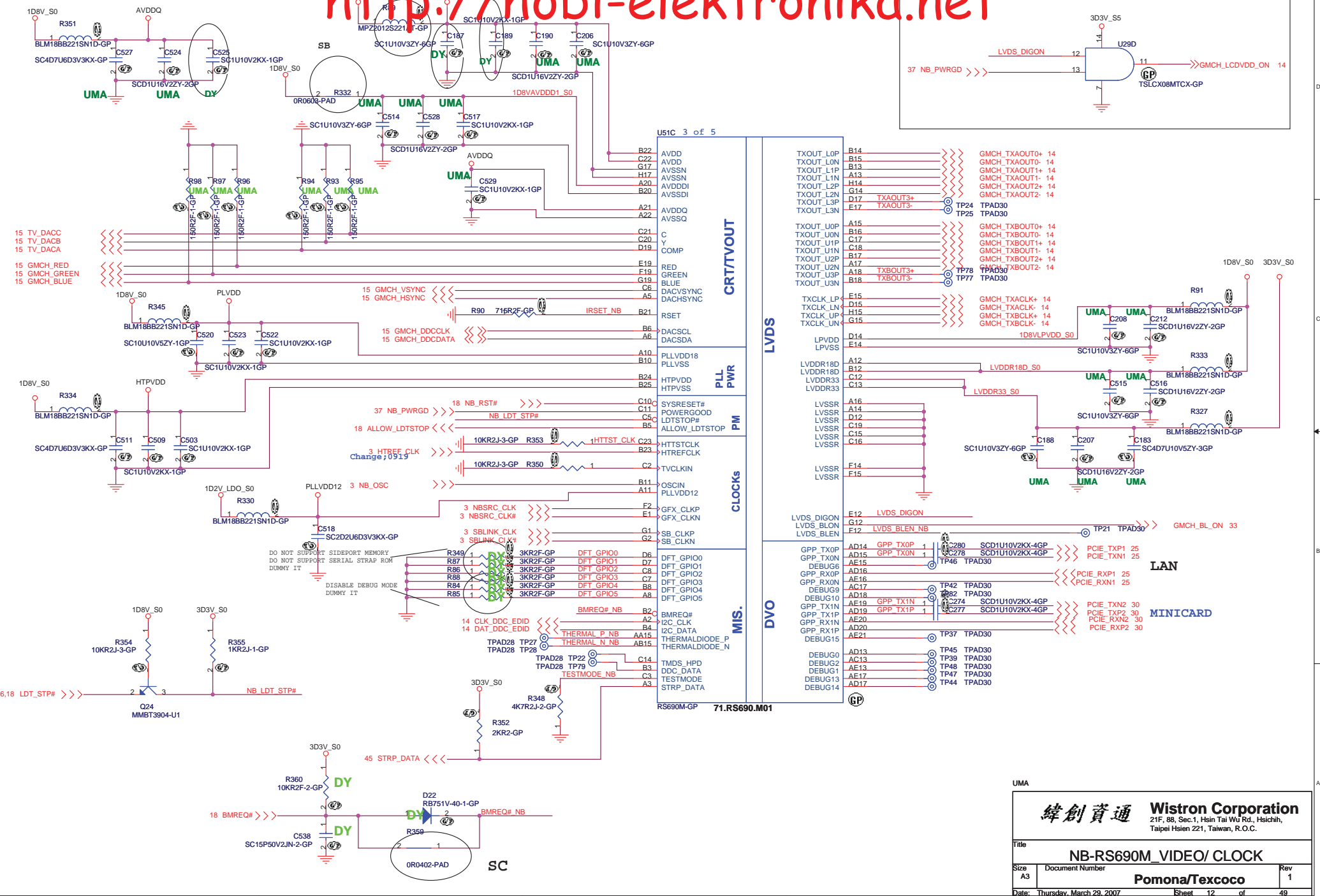
16 PEG_RXN[15..0] >>>
16 PEG_RXP[15..0] >>>

>>> PEG_TXN[15..0] 16
>>> PEG_TXP[15..0] 16



UMA

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Title NB-RS690M_MEM/PCIE_LINK I/F			
Size A3	Document Number	Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 11	of	49

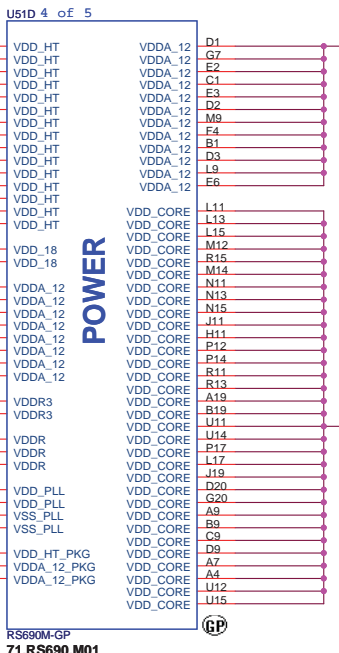
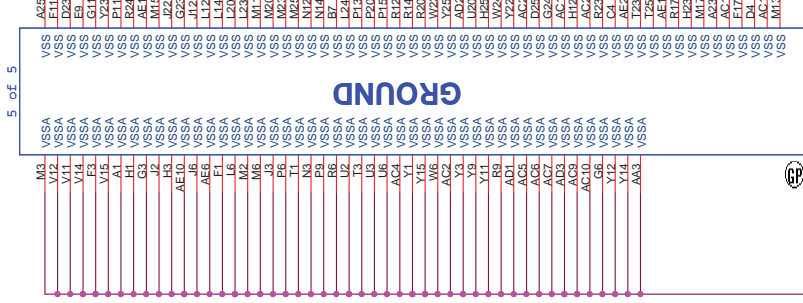
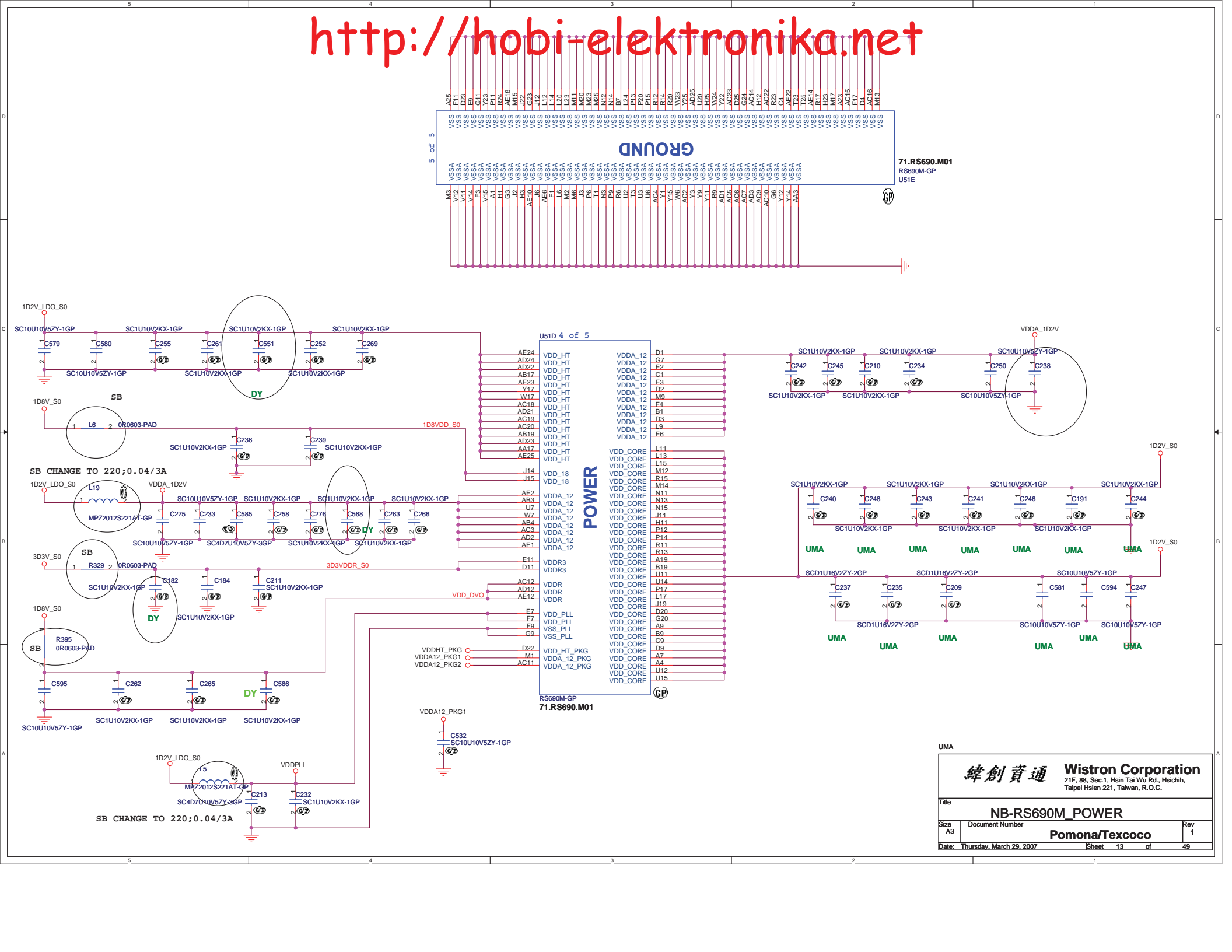


緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **NB-RS690M_VIDEO/ CLOCK**

Size A3 Document Number **Pomona/Texcoco** Rev 1

Date: Thursday, March 29, 2007 Sheet 12 of 49



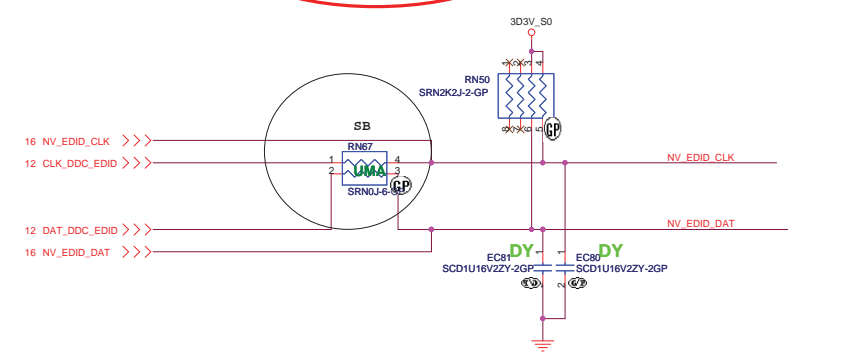
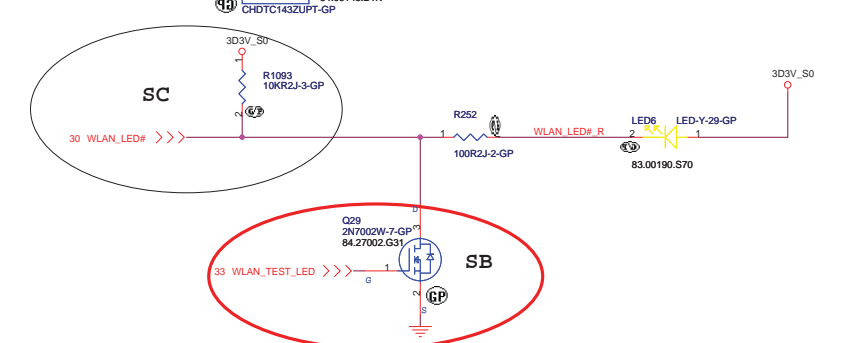
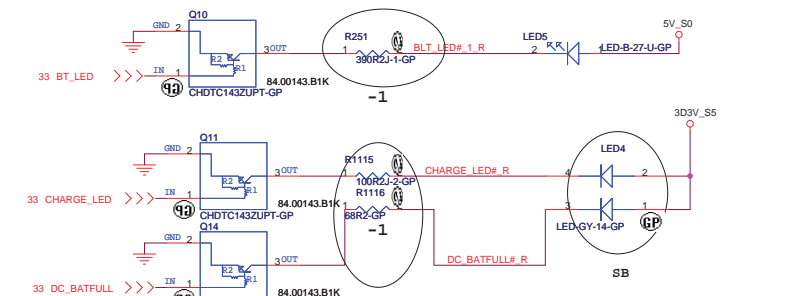
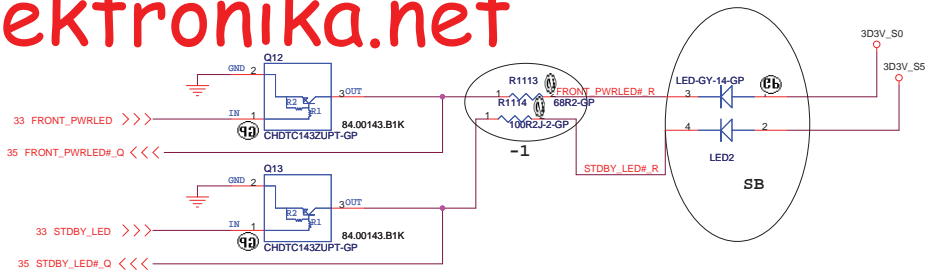
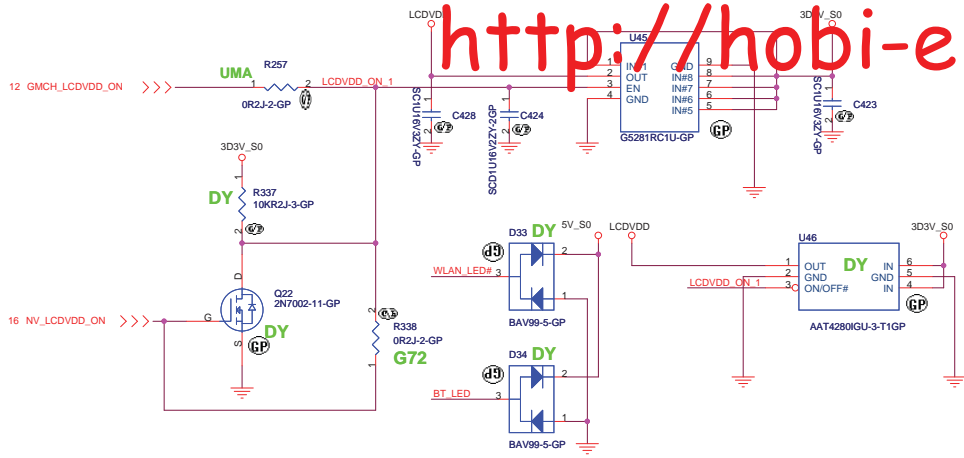
UMA

緯創資通 **Wistron Corporation**
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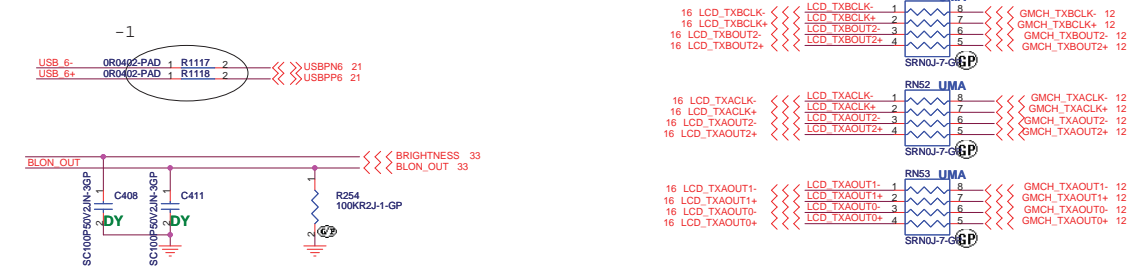
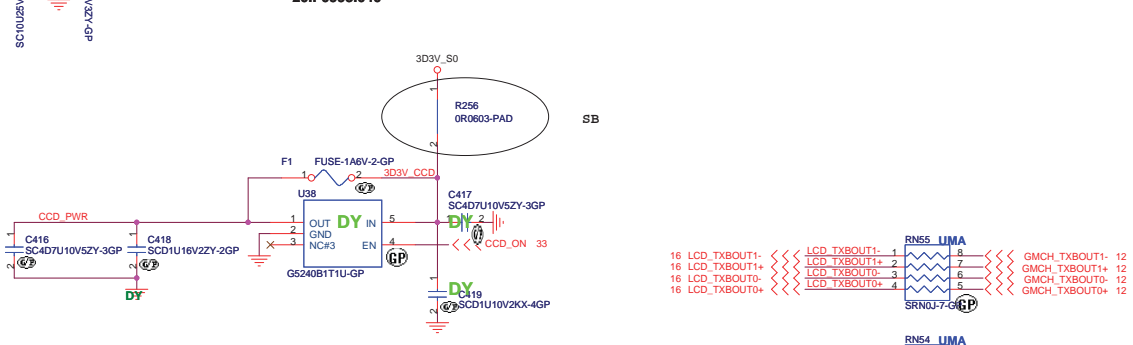
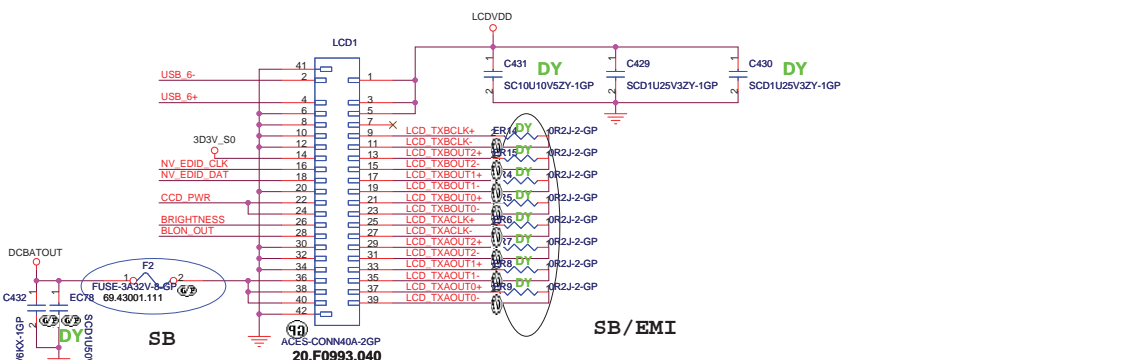
Title: **NB-RS690M_POWER**

Size: A3 Document Number: **Pomona/Textcoco** Rev: 1

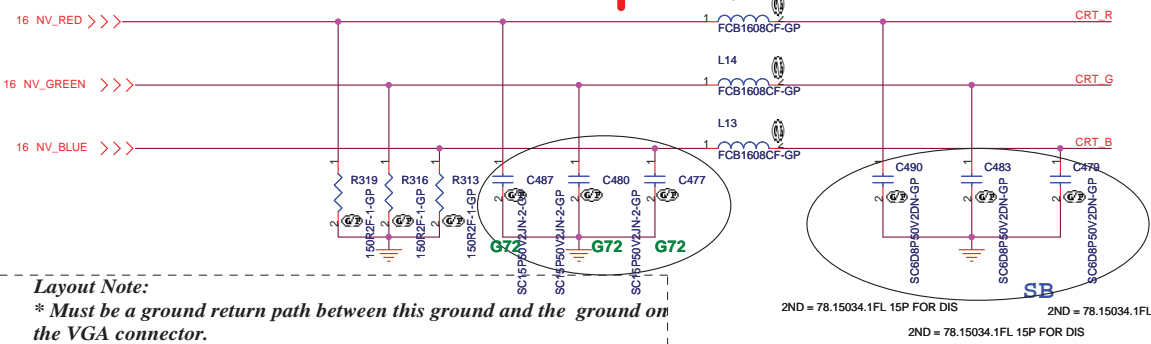
Date: Thursday, March 29, 2007 Sheet 13 of 49



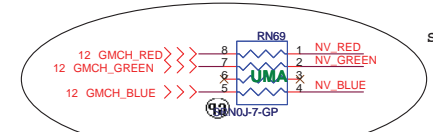
LCD/INVERTER CONN



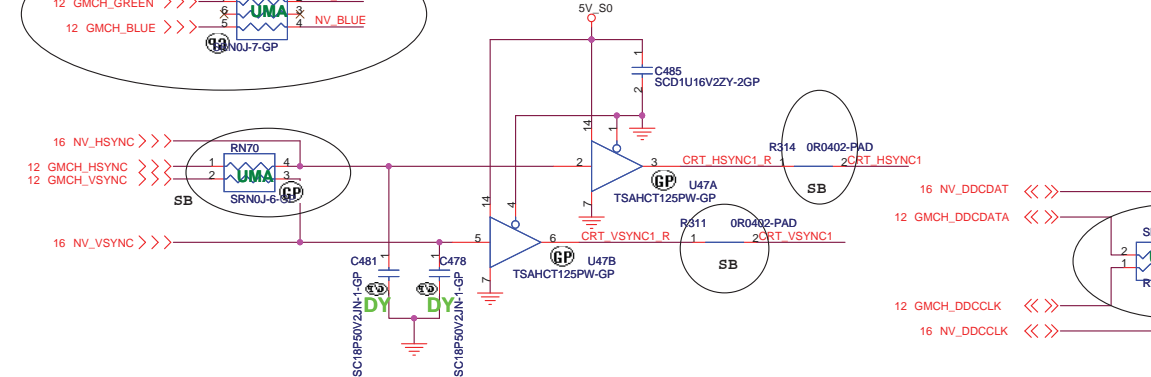
Layout Note:
Place these resistors close to the CRT-out connector



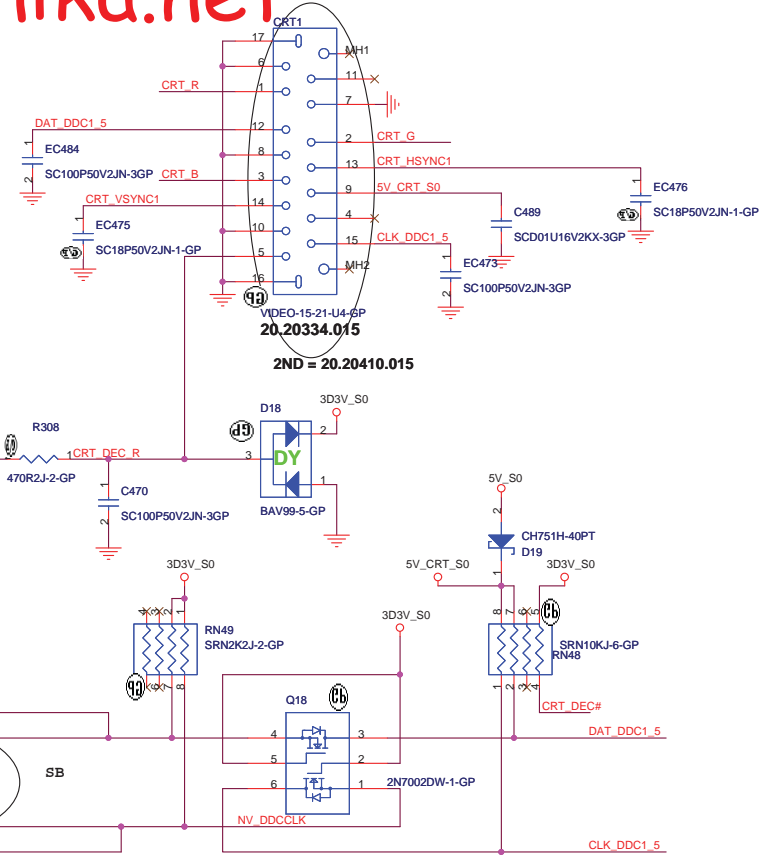
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



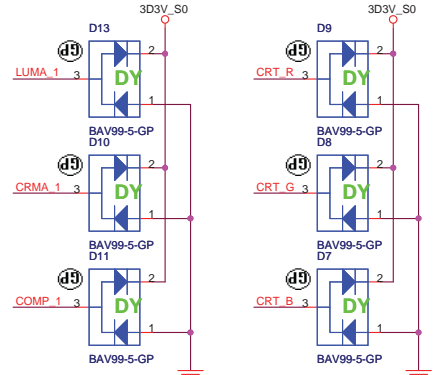
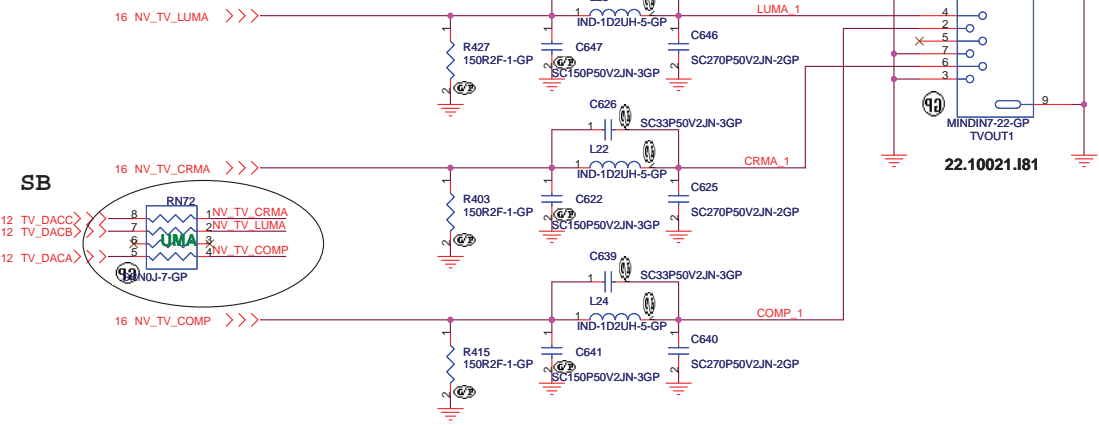
SB Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV CONN



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Title		CRT/TV Connector	
Size	Document Number	Rev 1	
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ENG MUST STUFF FOR ATI

Put near graphic connector

- 11 PEG_TXP[15..0] <<<
- 11 PEG_TXN[15..0] <<<
- 11 PEG_RXP[15..0] <<<
- 11 PEG_RXN[15..0] <<<

- 14 LCD_TXBOUT0+
- 14 LCD_TXBOUT0-
- 14 LCD_TXBOUT1+
- 14 LCD_TXBOUT1-
- 14 LCD_TXBOUT2+
- 14 LCD_TXBOUT2-

- 15 NV_BLUE
- 15 NV_GREEN
- 15 NV_RED

- 15 NV_TV_COMP
- 15 NV_TV_LUMA
- 15 NV_TV_CRMA

19 UMA_DIS <<<

- LCD_TXACLK- 14
- LCD_TXACLK+ 14
- LCD_TXAOUT2- 14
- LCD_TXAOUT2+ 14
- LCD_TXAOUT1- 14
- LCD_TXAOUT1+ 14
- LCD_TXAOUT0- 14
- LCD_TXAOUT0+ 14

>>> NV_EDID_DAT 14

>>> NV_EDID_CLK 14

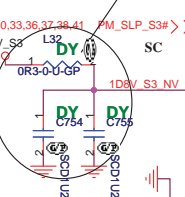
>>> NV_LCDVDD_ON 14

>>> NV_BLON 33

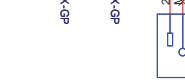
>>> NV_DVI_DAT 17

>>> NV_DVI_CLK 17

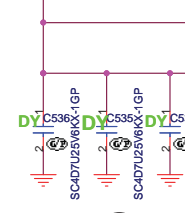
POWER-ON



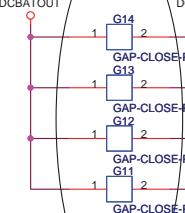
SB/NV



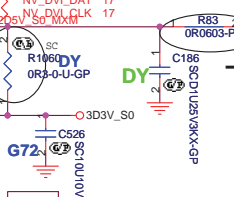
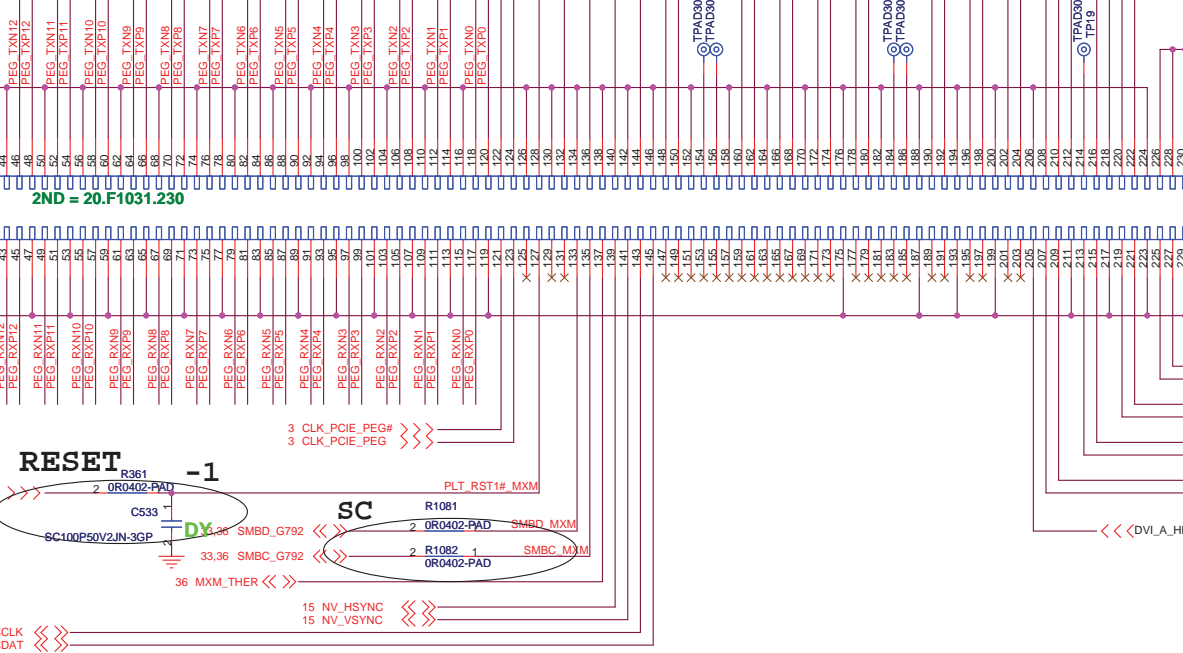
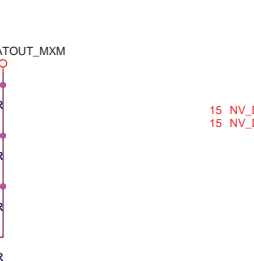
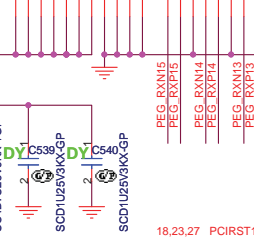
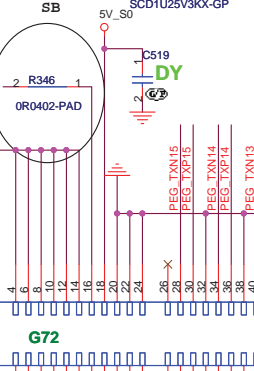
RESET



DCBATOUT



SB



EMI REQUEST

- <<< MDS_A_TX0+ 17
- <<< MDS_A_TX0- 17
- <<< MDS_A_TX1+ 17
- <<< MDS_A_TX1- 17
- <<< MDS_A_TX2+ 17
- <<< MDS_A_TX2- 17
- <<< MDS_A_TXC+ 17
- <<< MDS_A_TXC- 17
- <<< DVI_A_HPD 17

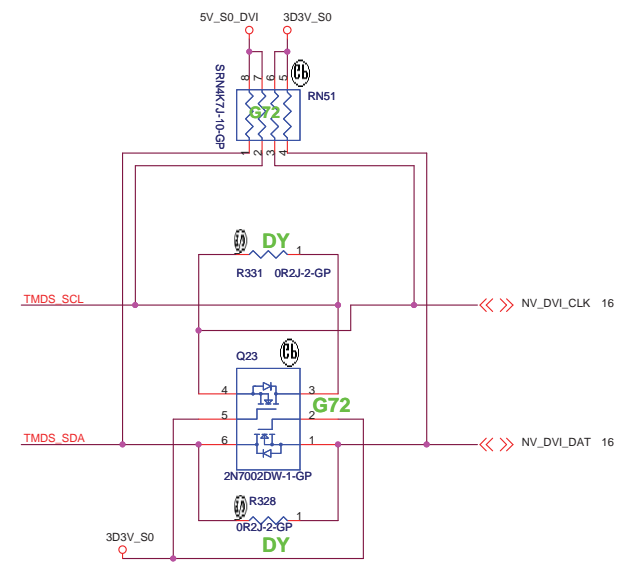
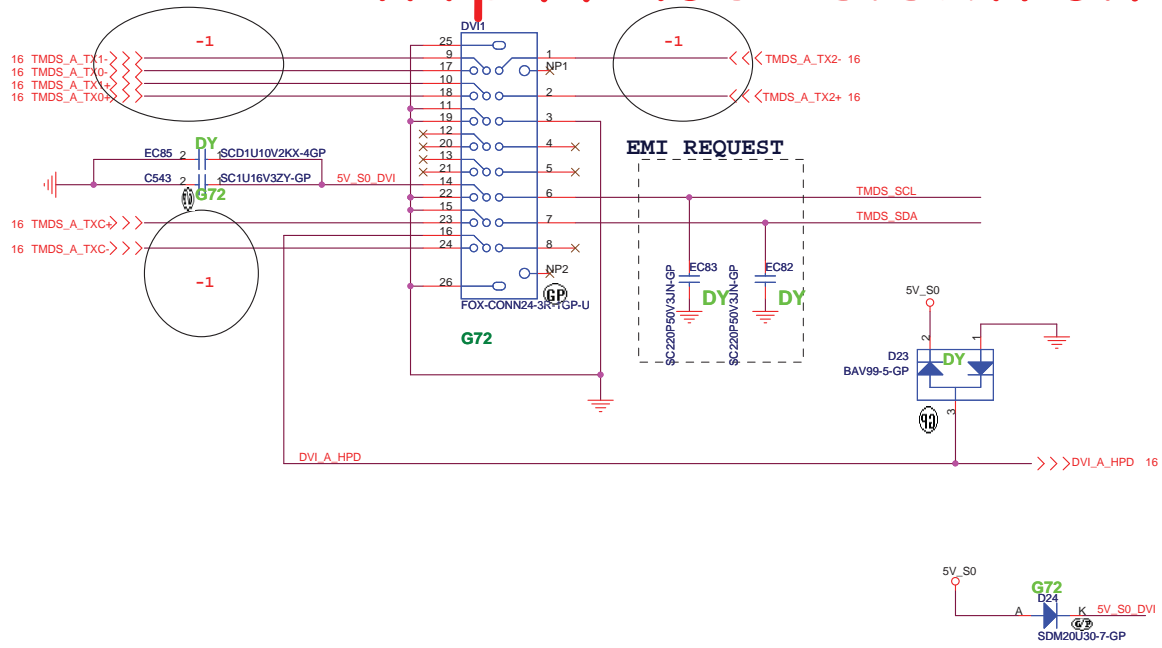
UMA

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

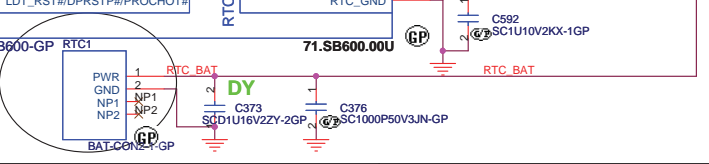
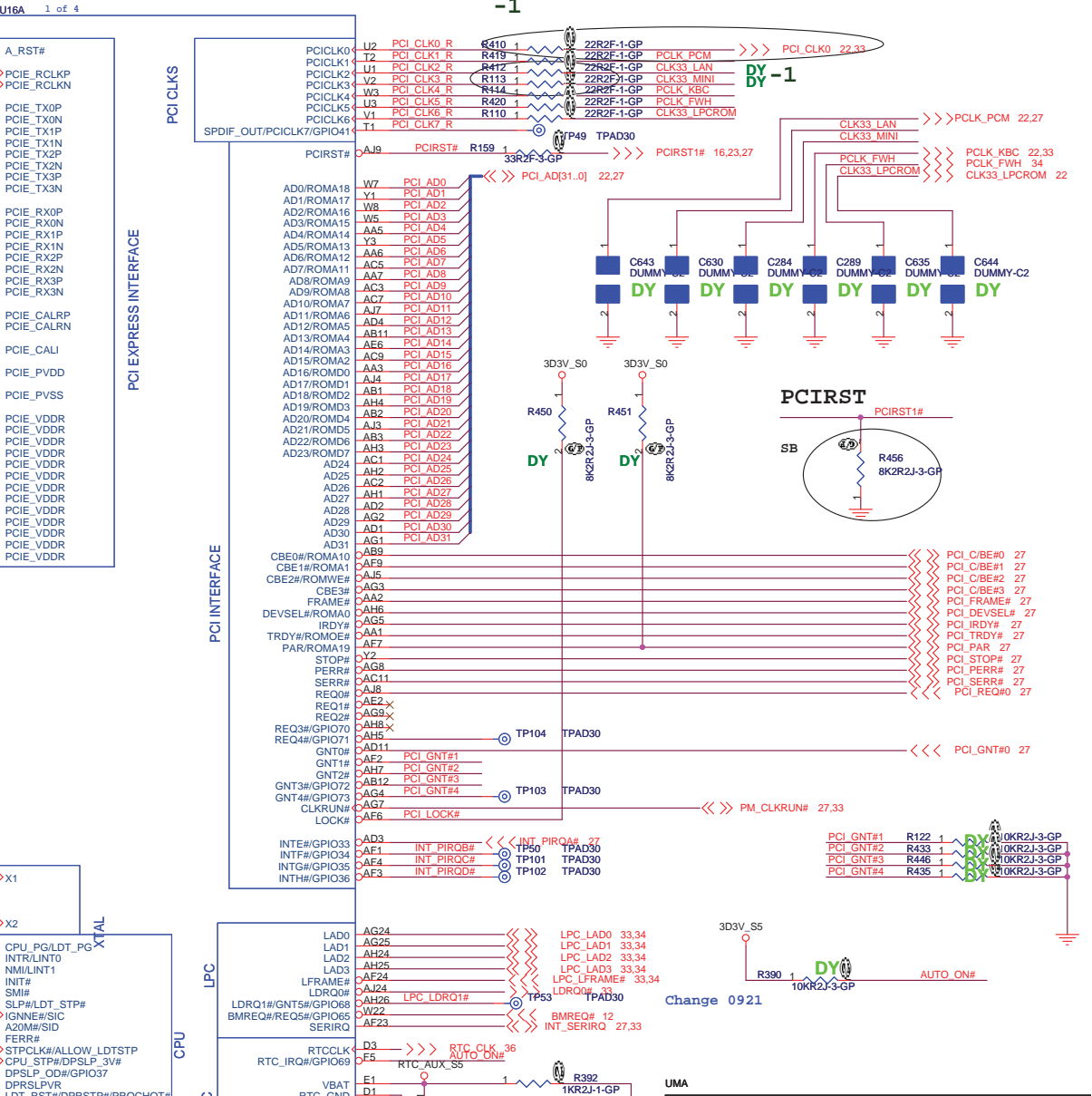
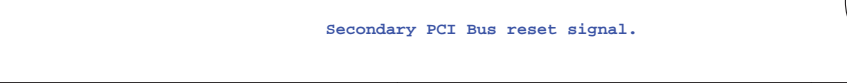
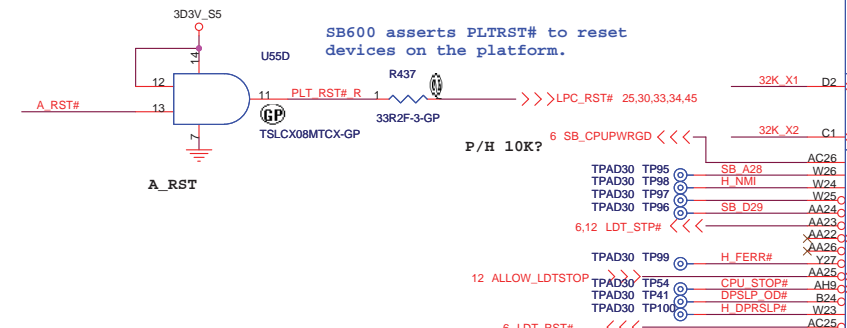
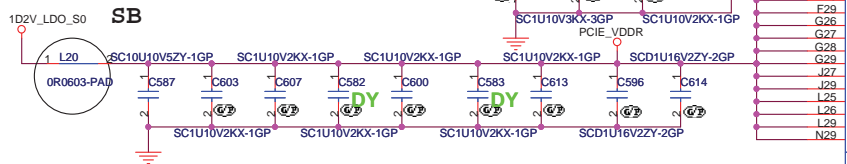
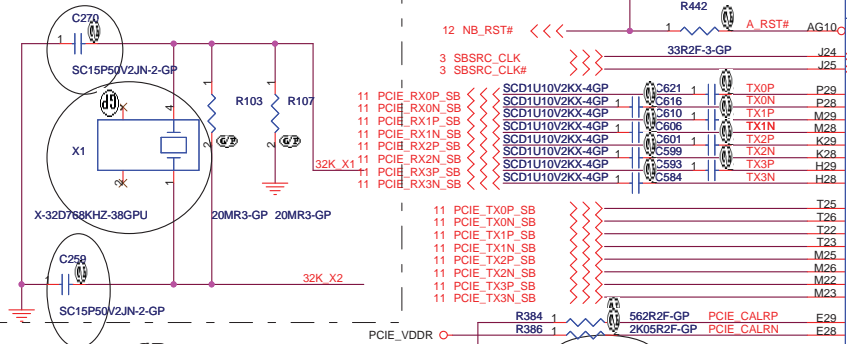
Size: A3 Document Number: **Pomona/Texcoco** Rev: **1**

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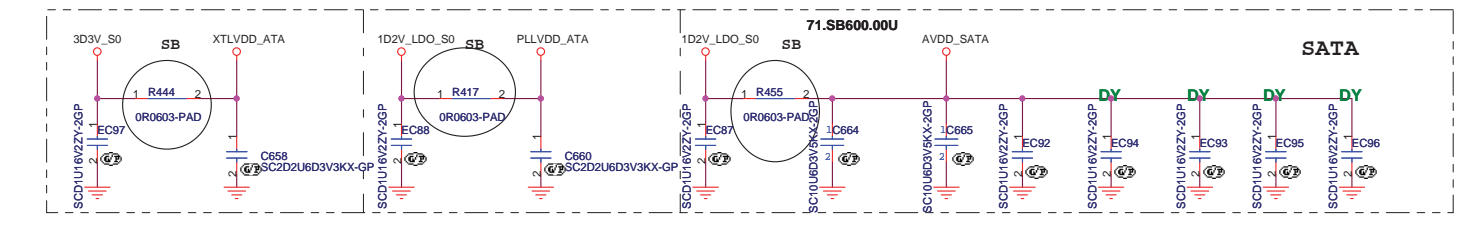
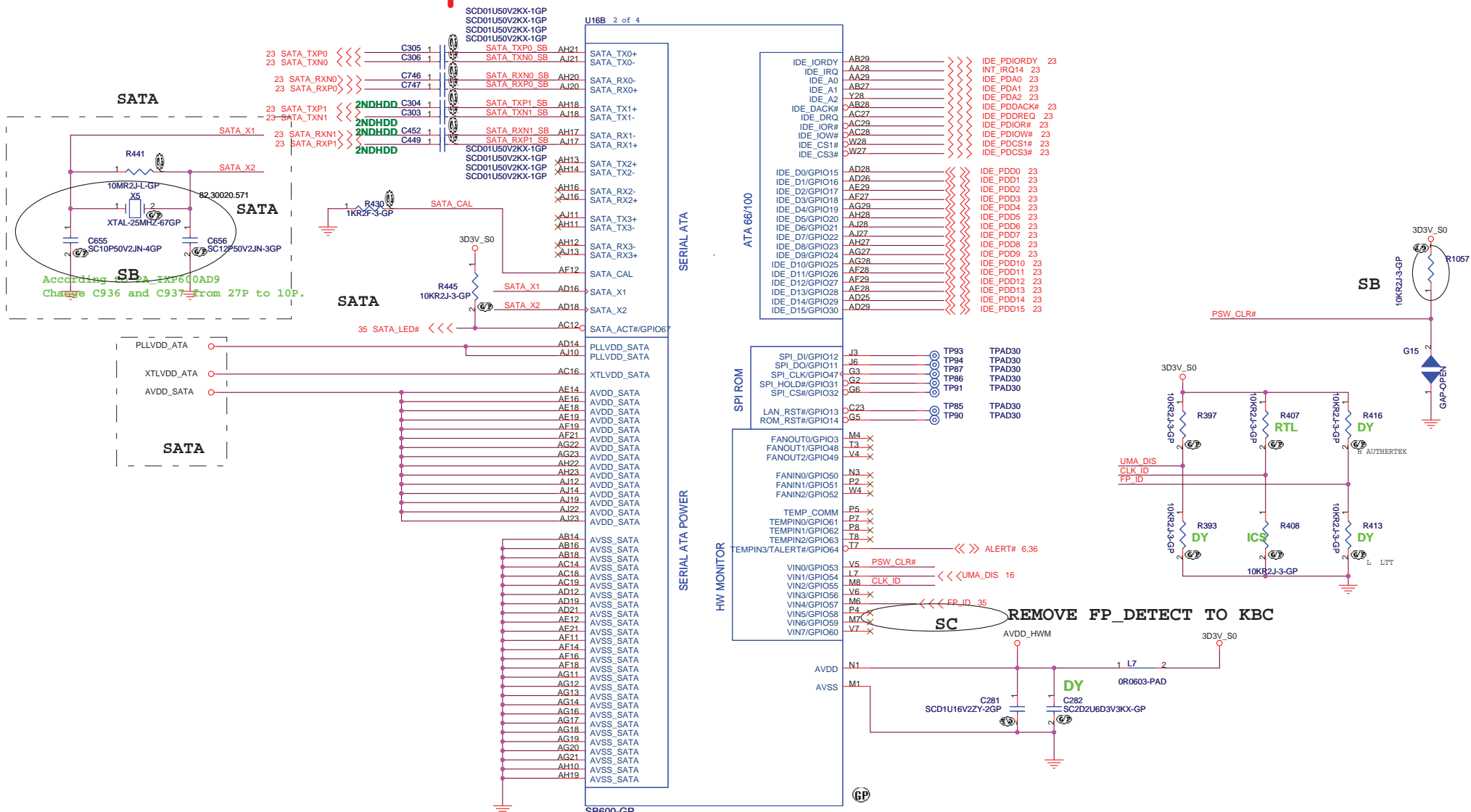
UMA		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DVI CONNECTOR		
Size: A3	Document Number: Pomona/Textcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet: 17	of 49

Place these components close to U13 and use ground guard for 32K_X1 and 32K_X2.



緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: SB600 PCI/CPU/LPC/RTC (1 of 5)			
Size A3	Document Number	Pomona/Texcoco	
Date: Thursday, March 29, 2007	Sheet	18	of 49

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB60

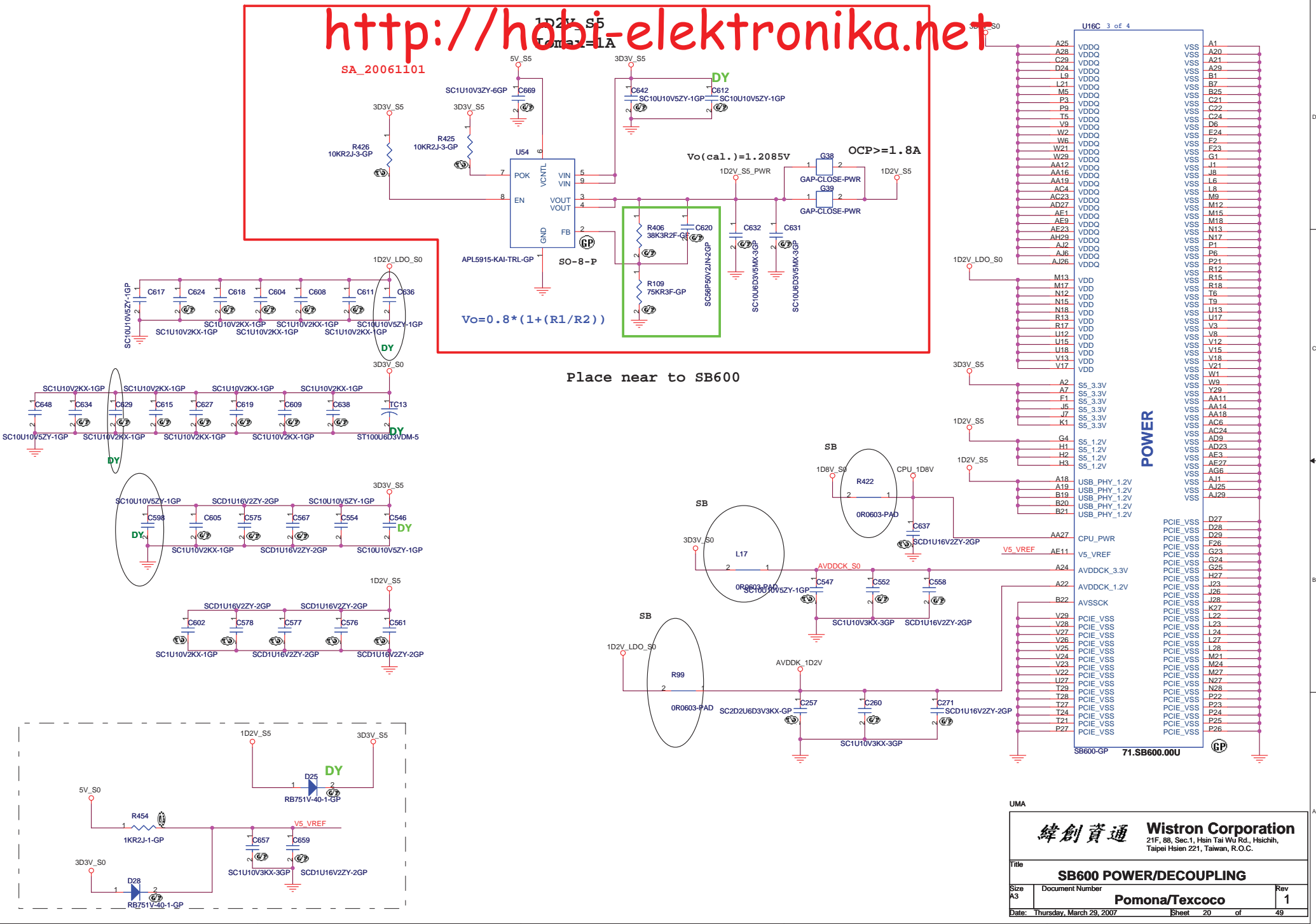


UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title SB600 ACPI/GPIO/SATA/IDE (2 of 5)
Size A3 Document Number Pomona/Texcoco Rev 1
Date: Thursday, March 29, 2007 Sheet 19 of 49

SA_20061101



Place near to SB600

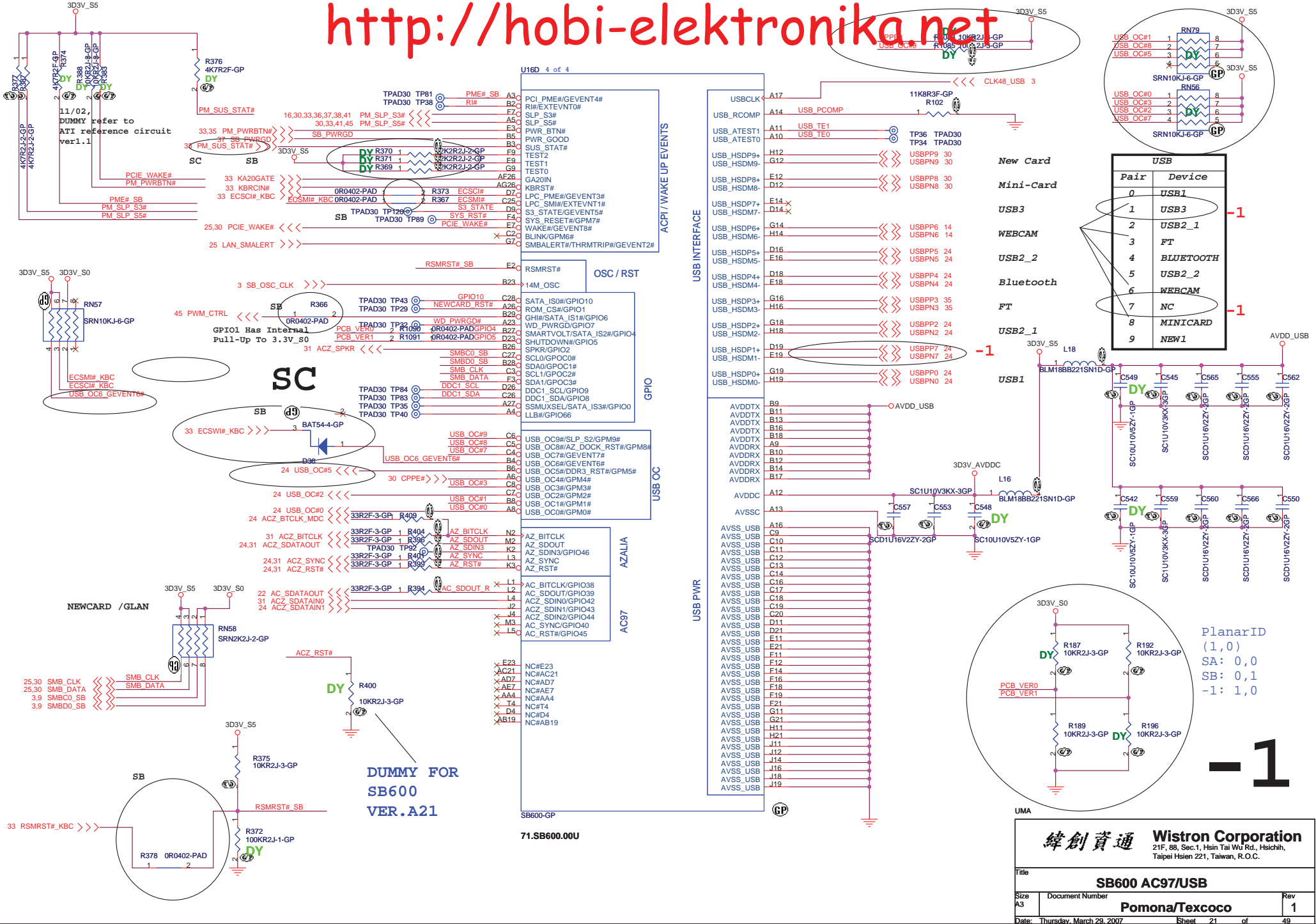
POWER

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

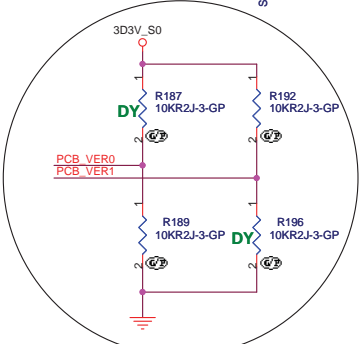
Title: **SB600 POWER/DECOUPLING**

Size A3 Document Number: **Pomona/Textcoco** Rev: **1**

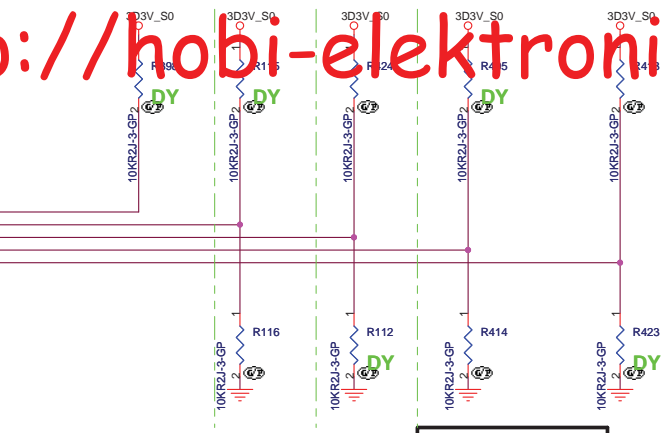
Date: Thursday, March 29, 2007 Sheet 20 of 49



Pair	Device
0	USB1
1	USB3
2	USB2_1
3	FT
4	BLUETOOTH
5	USB2_2
6	WEBCAM
7	NC
8	MINICARD
9	NEW1



21 AC_SDATAOUT
 18.33 PCLK_KBC
 18 CLK33 LPCROM
 18.33 PCLK_CLK0
 18.27 PCLK_PCM

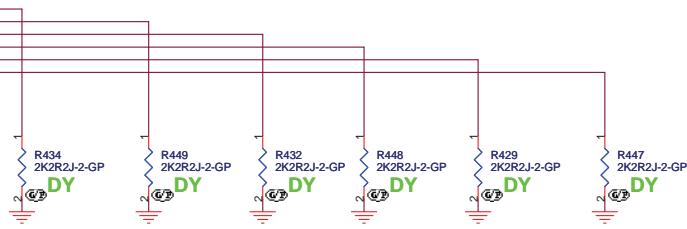


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4			

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

18.27 PCI_AD28
 18.27 PCI_AD27
 18.27 PCI_AD26
 18.27 PCI_AD25
 18.27 PCI_AD24
 18.27 PCI_AD23



DEBUG STRAPS

STRAP	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

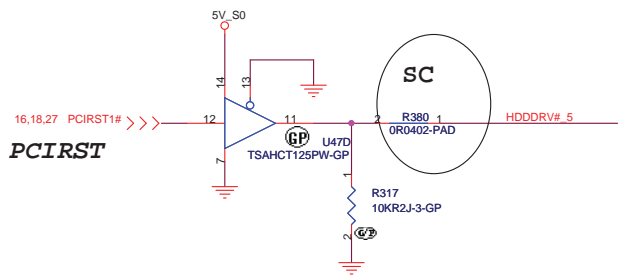
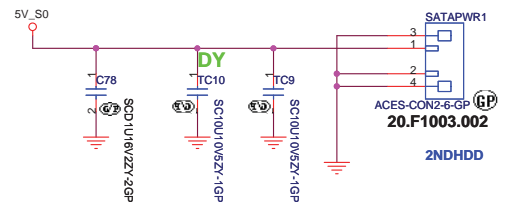
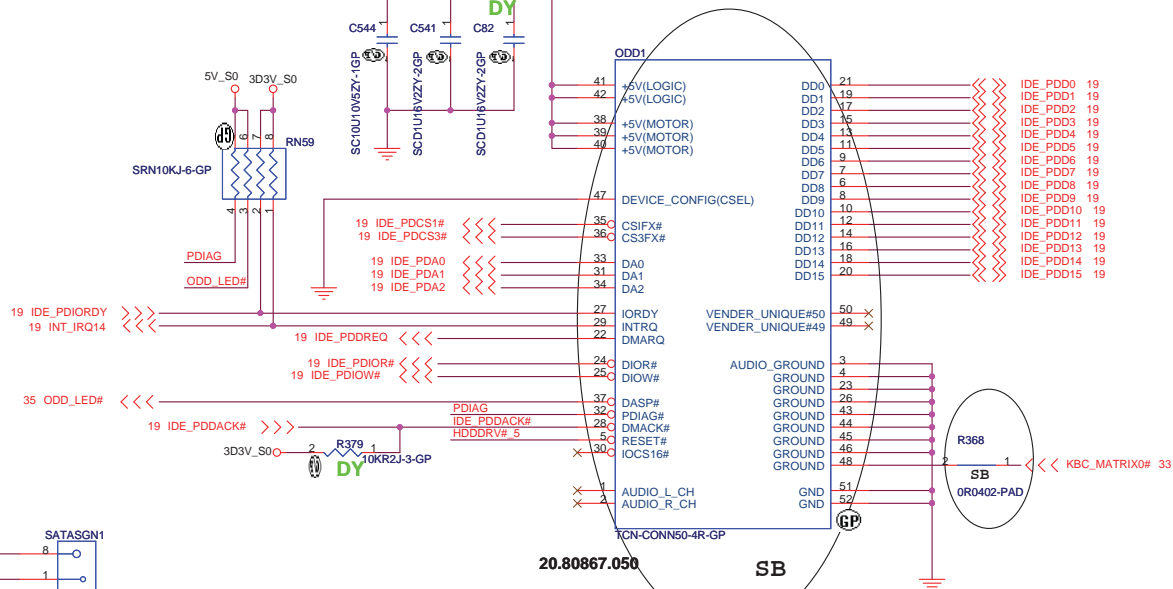
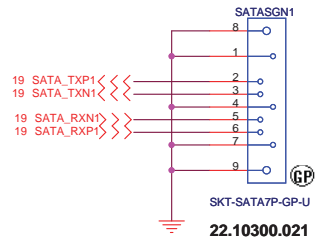
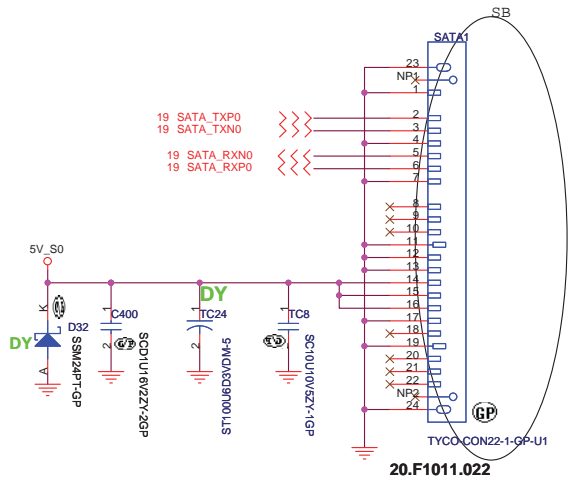
UMA

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
SB600 STRAPPING PIN	
Title	
Size A3	Document Number
	Pomona/Texcoco
Date: Thursday, March 29, 2007	Sheet 22 of 49
	Rev 1

SATA HD Connector

<http://hobi-elektronika.net>

ODD Connector



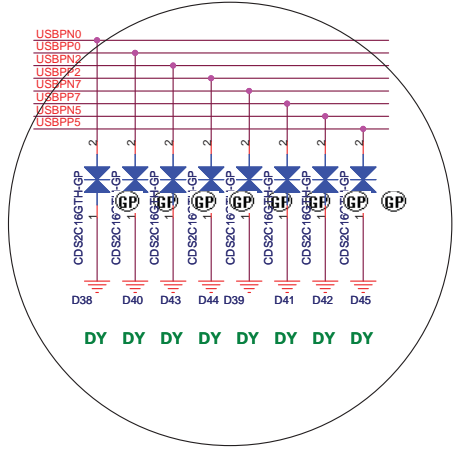
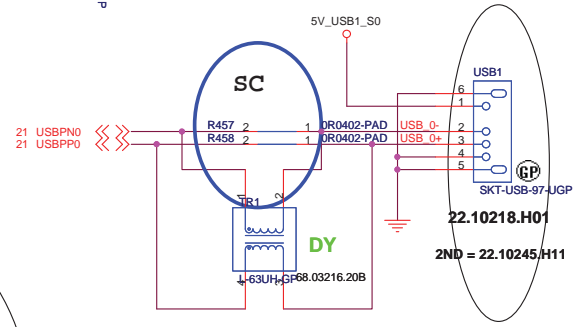
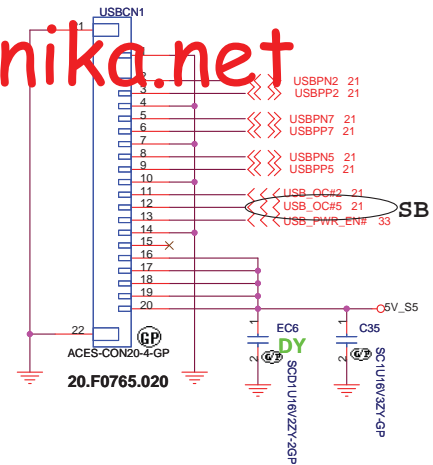
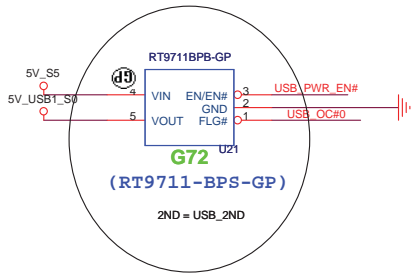
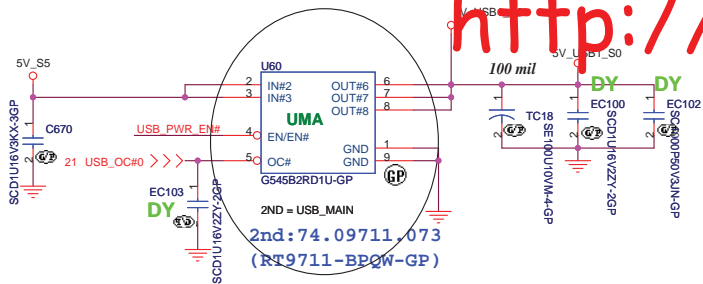
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD and CDROM**

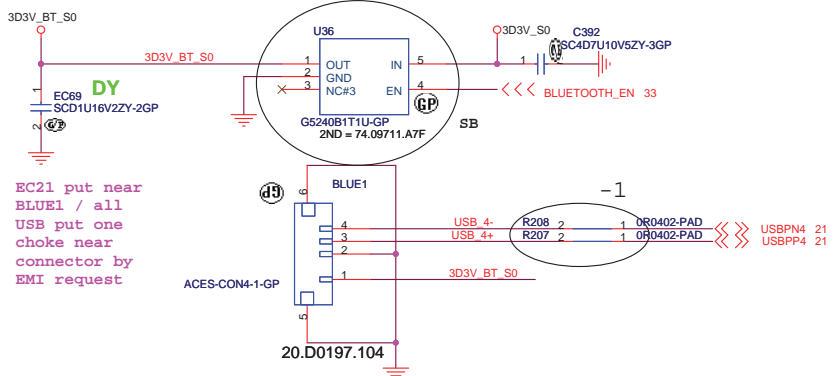
Size: Document Number **Pomona/Textcoco** Rev: **1**

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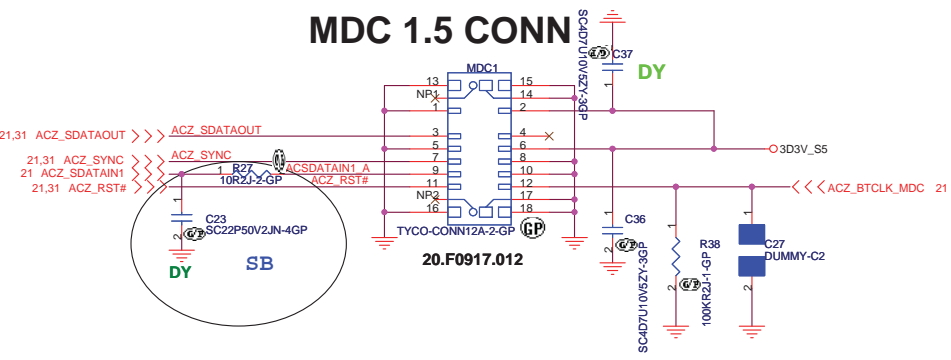
SC

BLUETOOTH MODULE

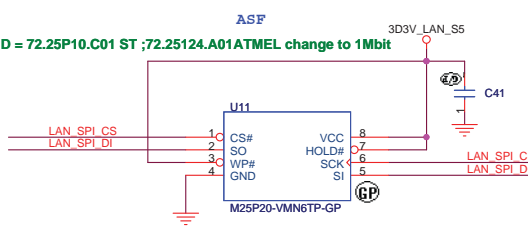
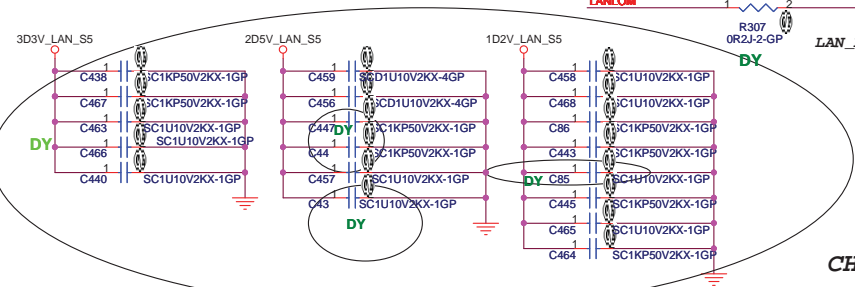
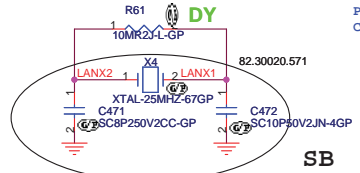
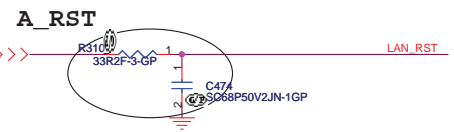
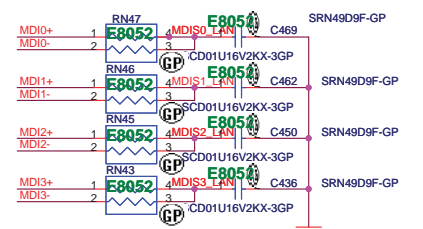
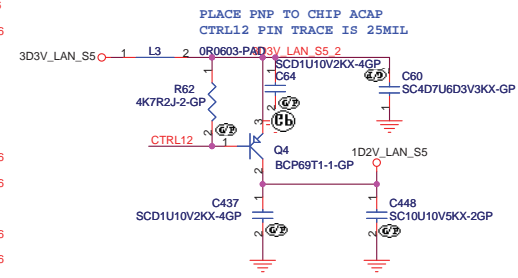
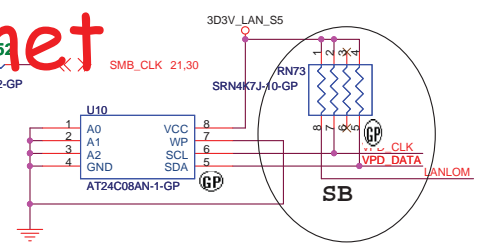
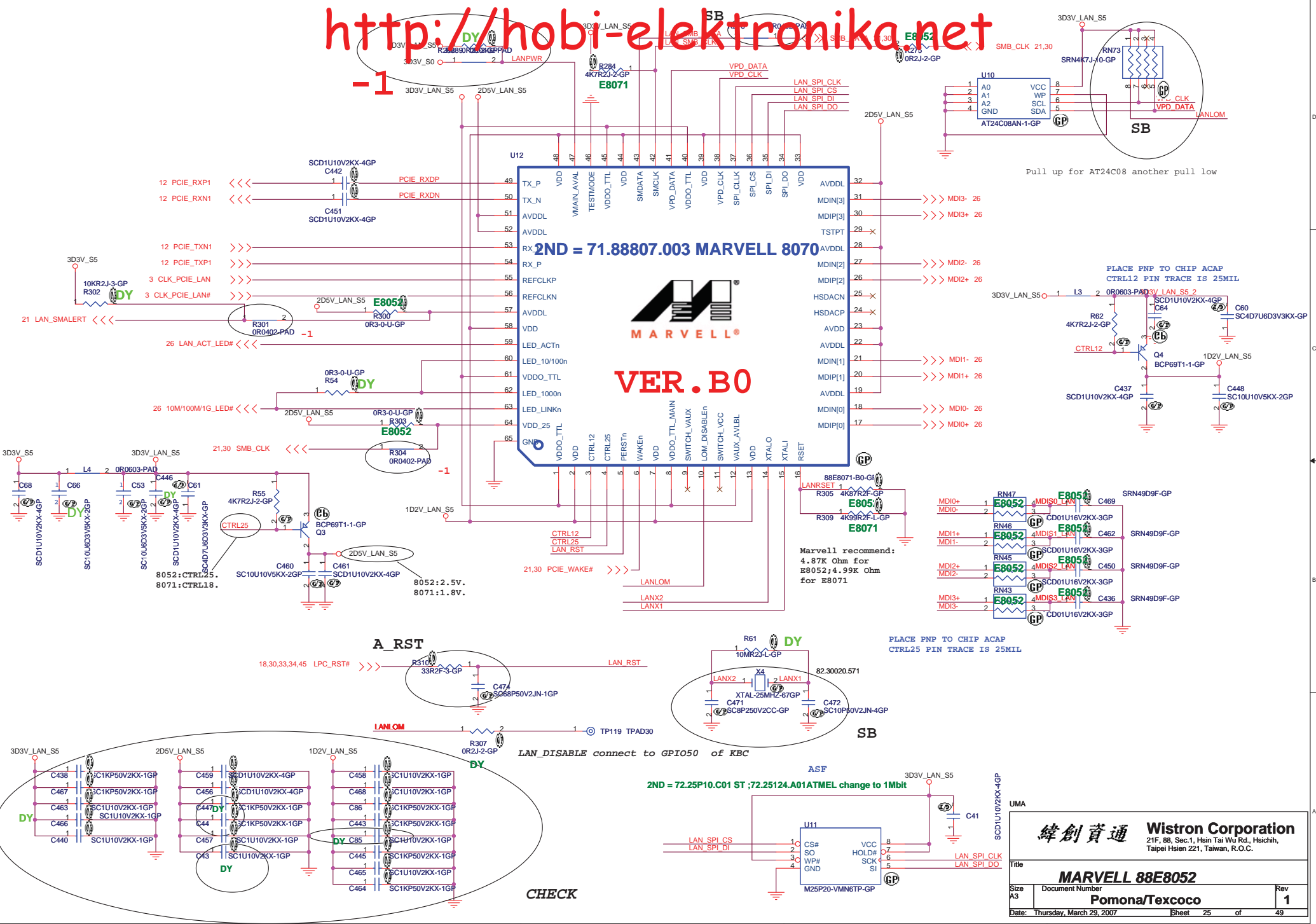


EC21 put near BLUE1 / all USB put one choke near connector by EMI request

MDC 1.5 CONN

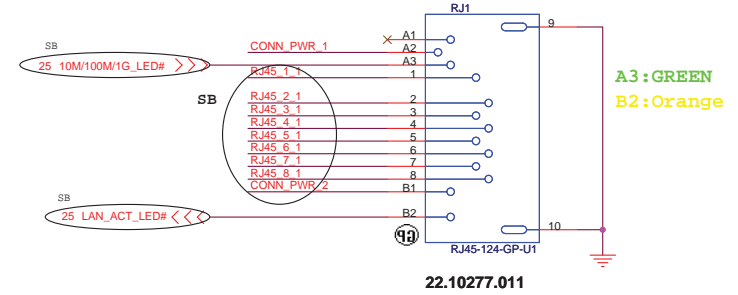


-1



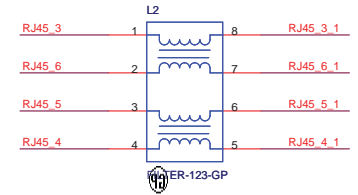
UMA		Title	
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Rev 1	
MARVELL 88E8052		Document Number	
Pomona/Textcoco		Date: Thursday, March 29, 2007	
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http://hobi-elektronika.net LAN Connector

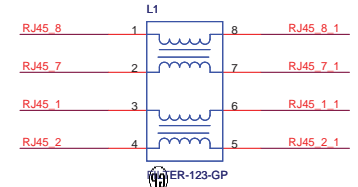


LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
 LAN Data: Yellow(B2), when LAN is transferring data.

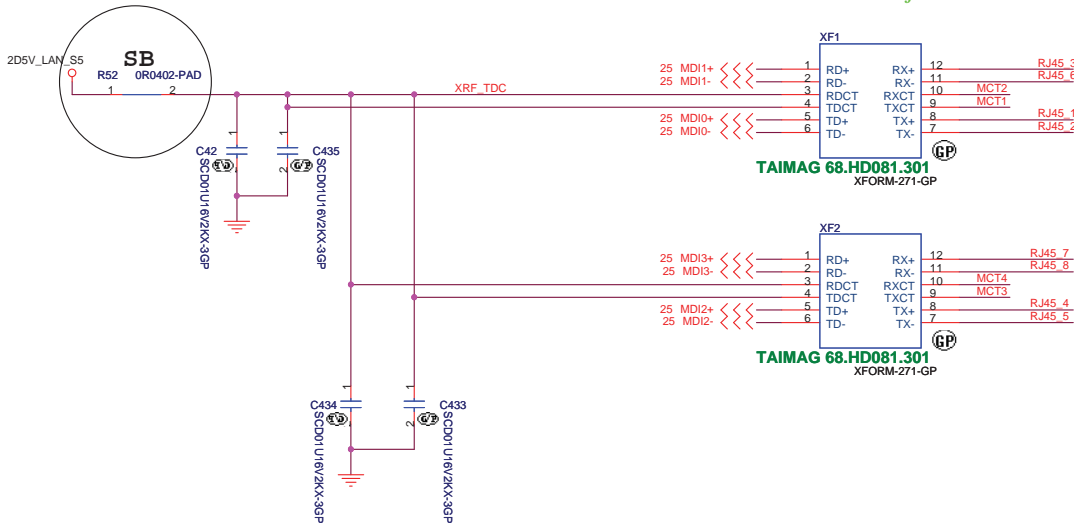
For EMI



-1



SC CHANGE 69.10106.021 TO 69.10106.011



GIGA Lan Transformer

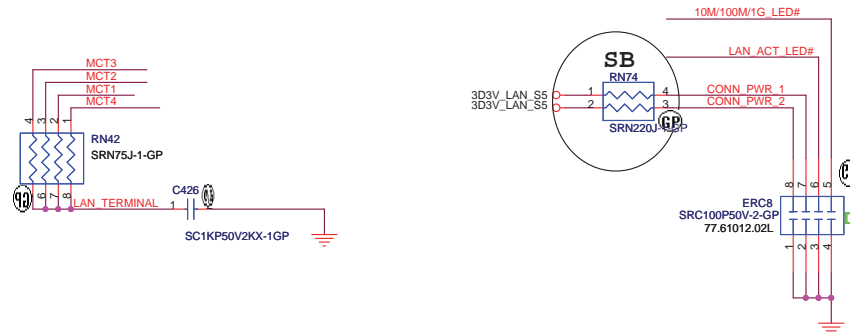
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP, DOC_RING, TIP_RING:

W/S : 10/100 @ Surface layers
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



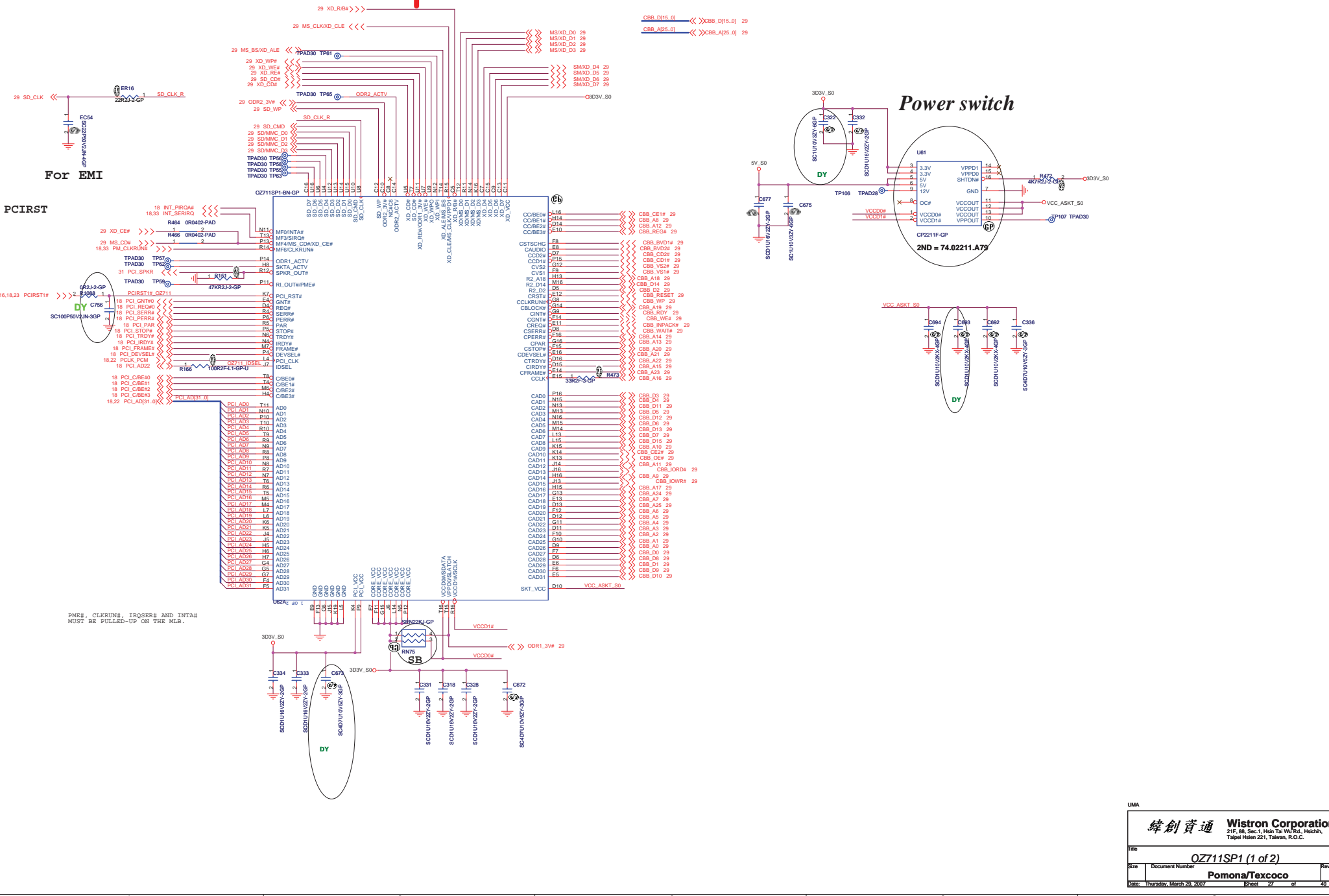
UMA

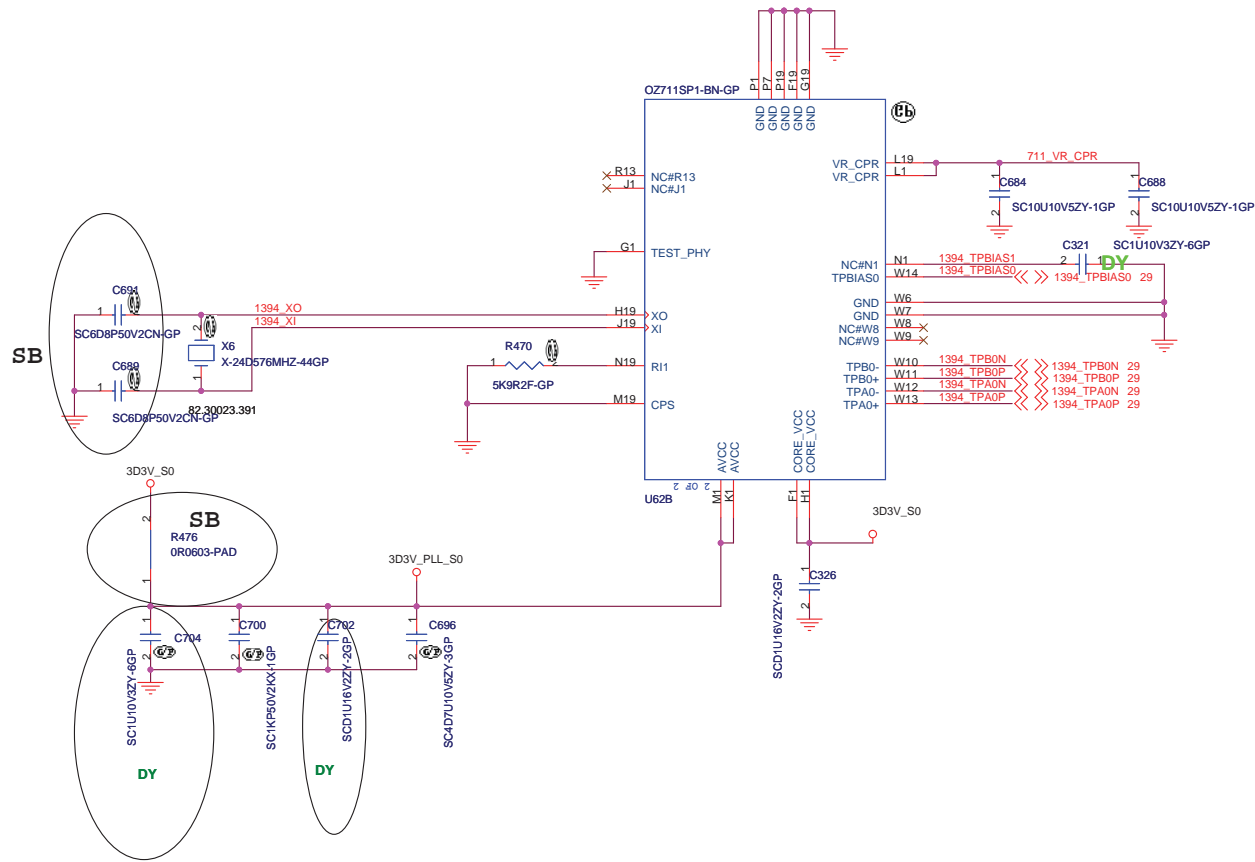
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size A3 Document Number **Pomona/Textcoco** Rev **1**

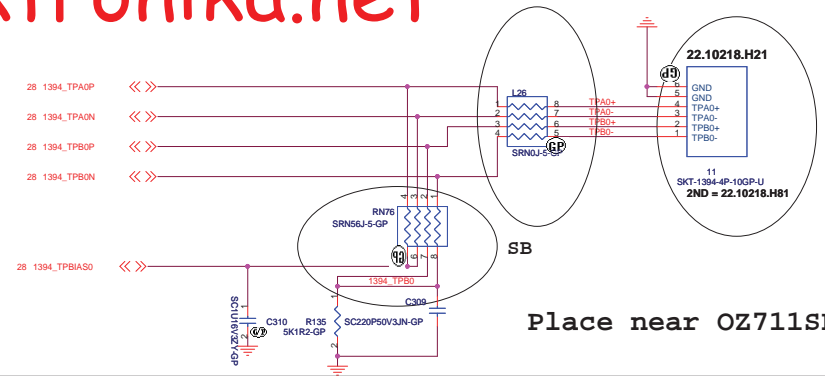
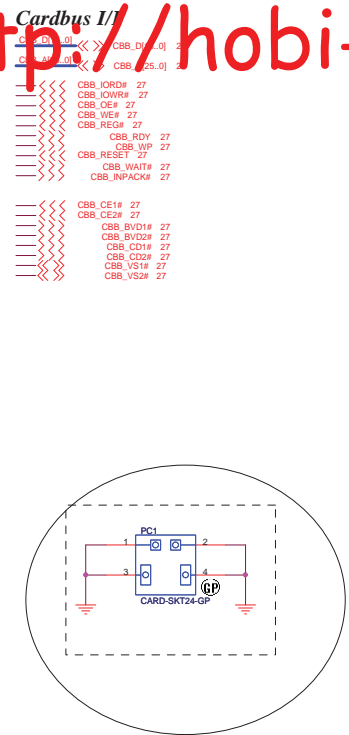
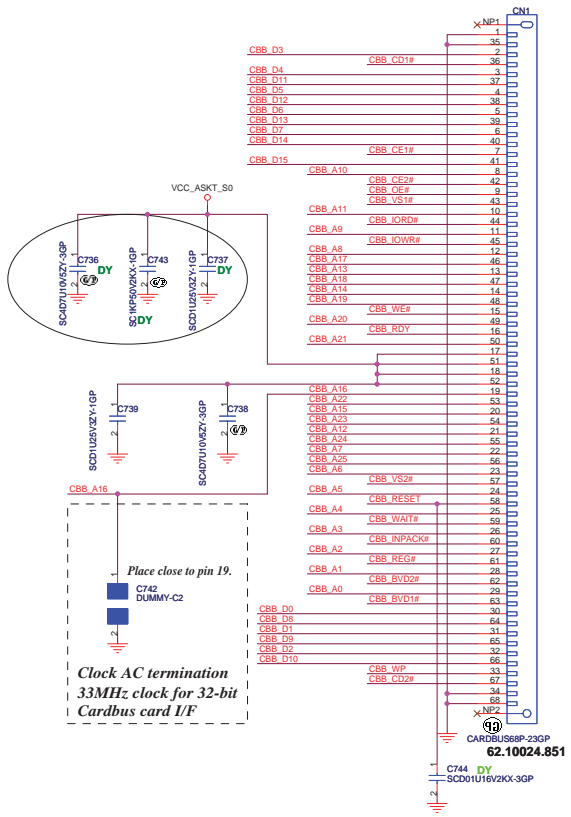
Date: Thursday, March 29, 2007 Sheet 26 of 49



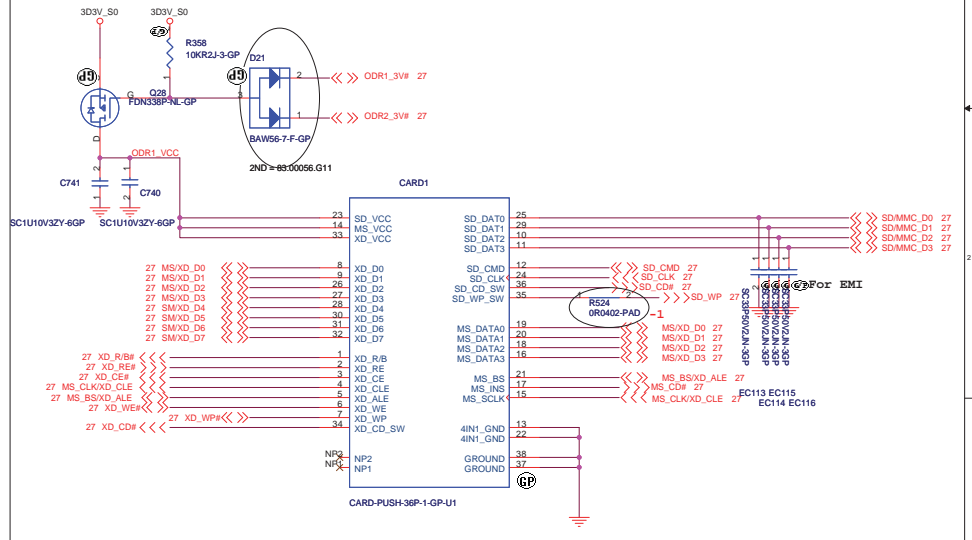


UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
OZ711SP1 (2 of 2)			
Size	Document Number	Pomona/Textcoco	
			Rev 1
Date: Thursday, March 29, 2007		Sheet 28	of 49



Place near OZ711SP1



XD
MS / MS PRO
SD / SD IO / MMC

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsin 221, Taiwan, R.O.C.

Title PCMCIA / 1394 / CARD READER

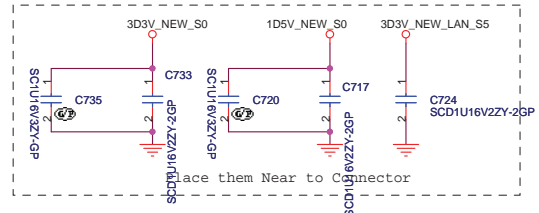
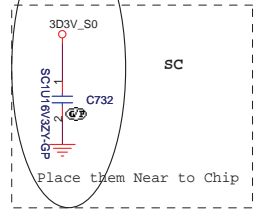
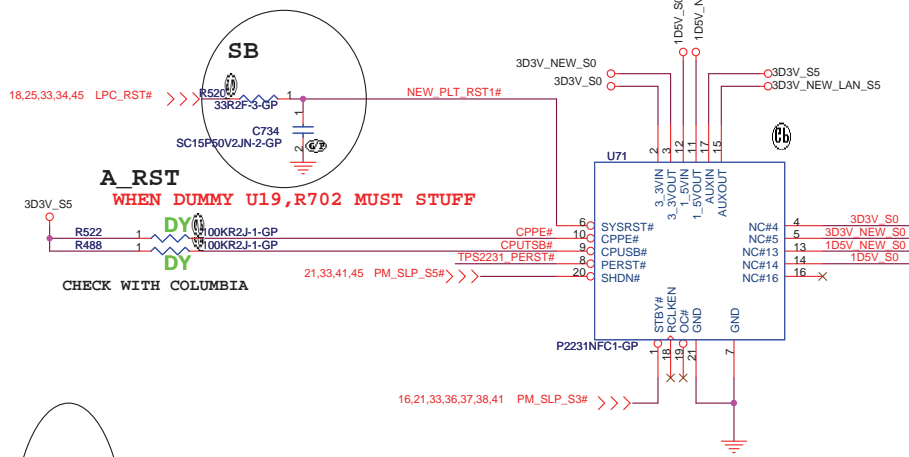
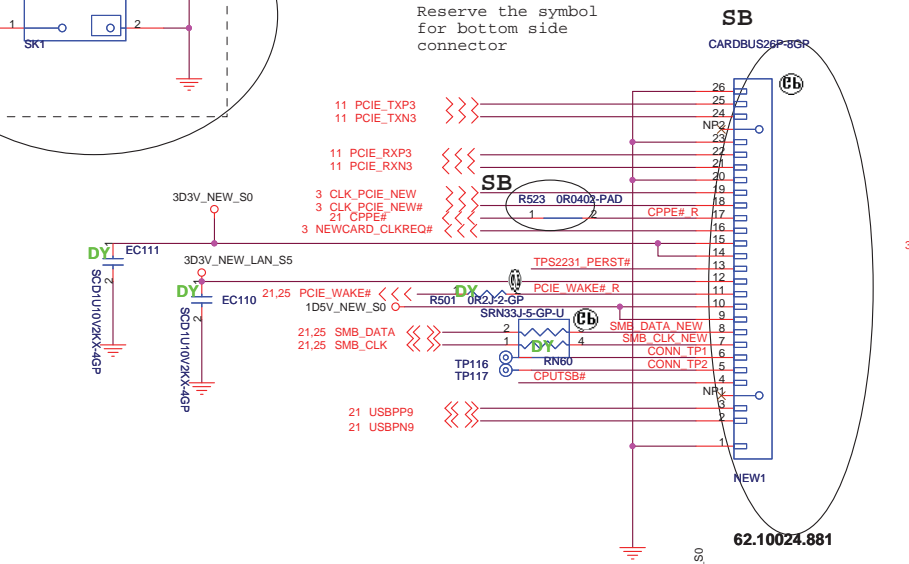
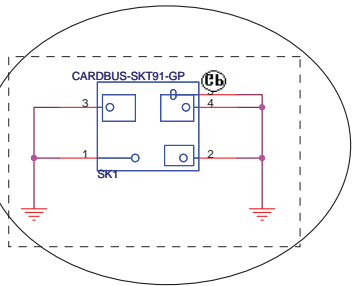
Size Document Number Rev 1

Pomona/Textcoco

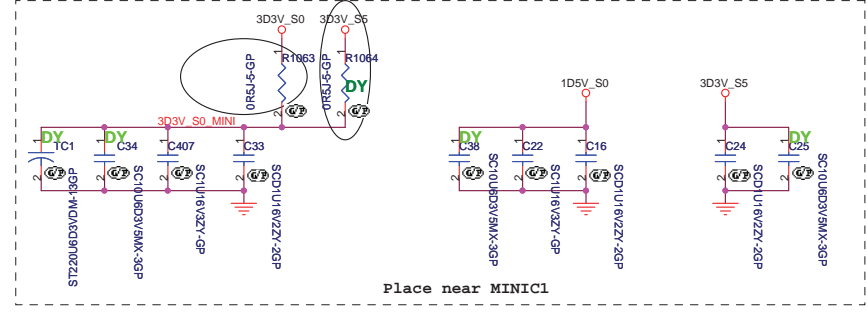
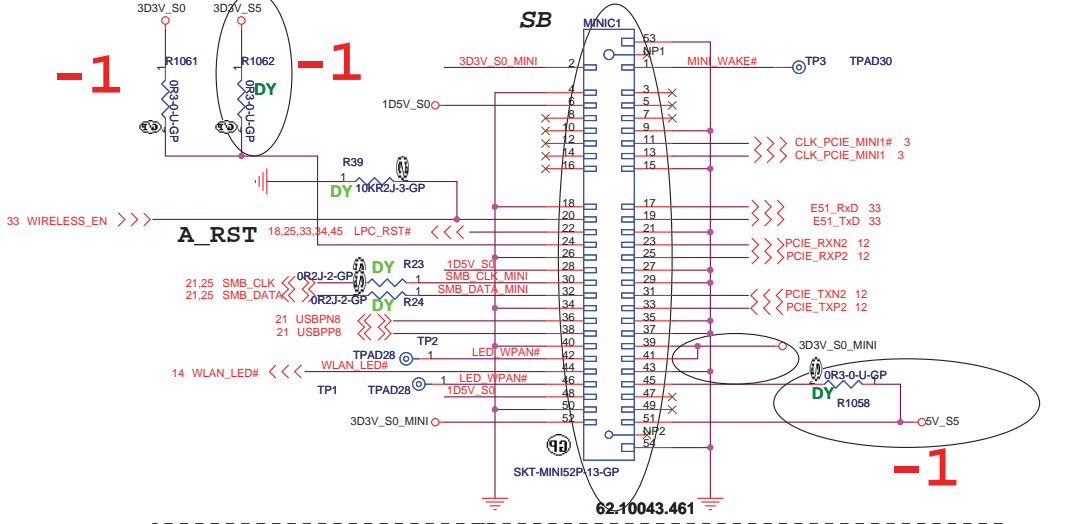
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NEWCARD Connector

Reserve the symbol for bottom side connector



CHECK / POWER PIN



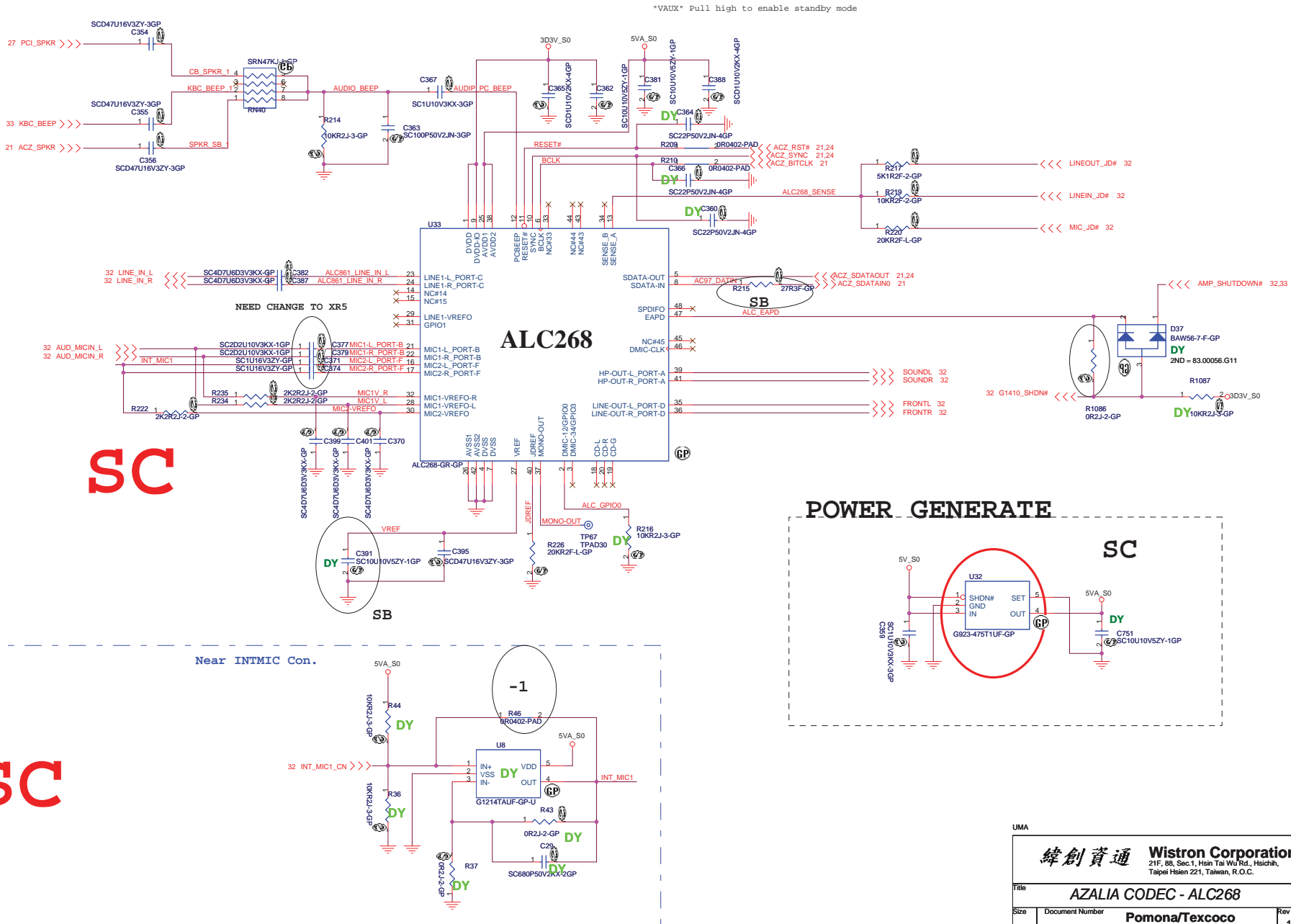
UMA

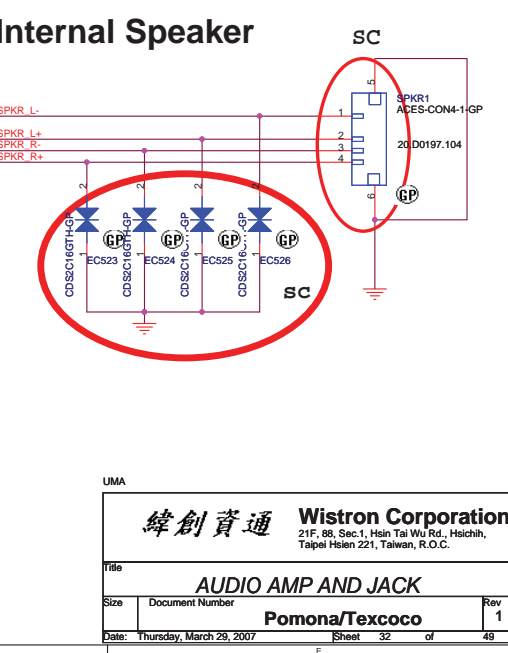
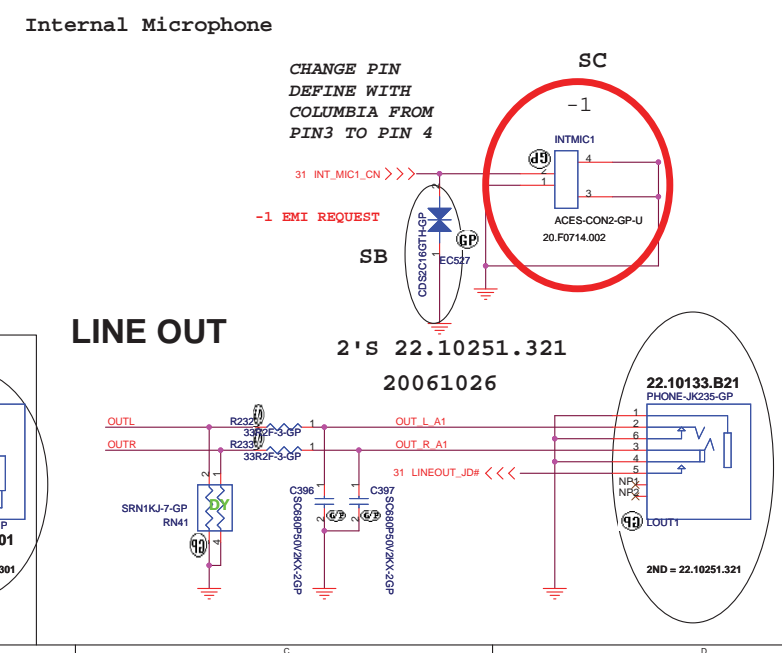
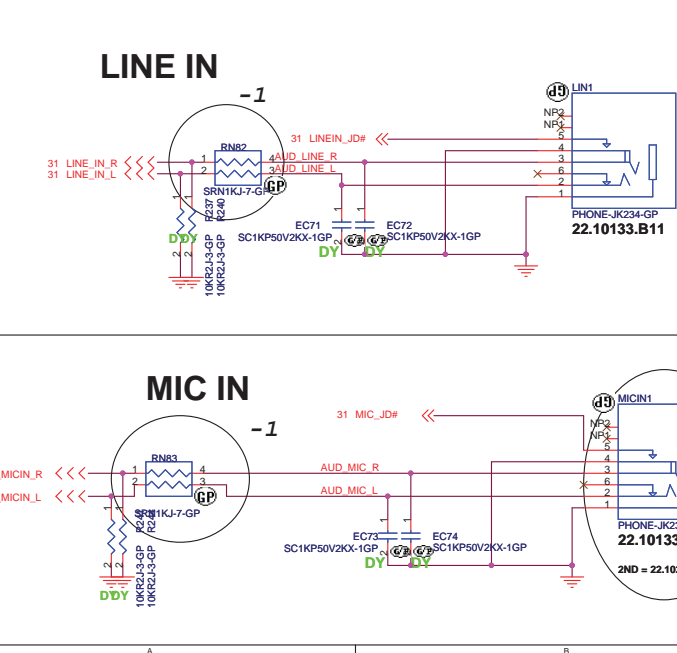
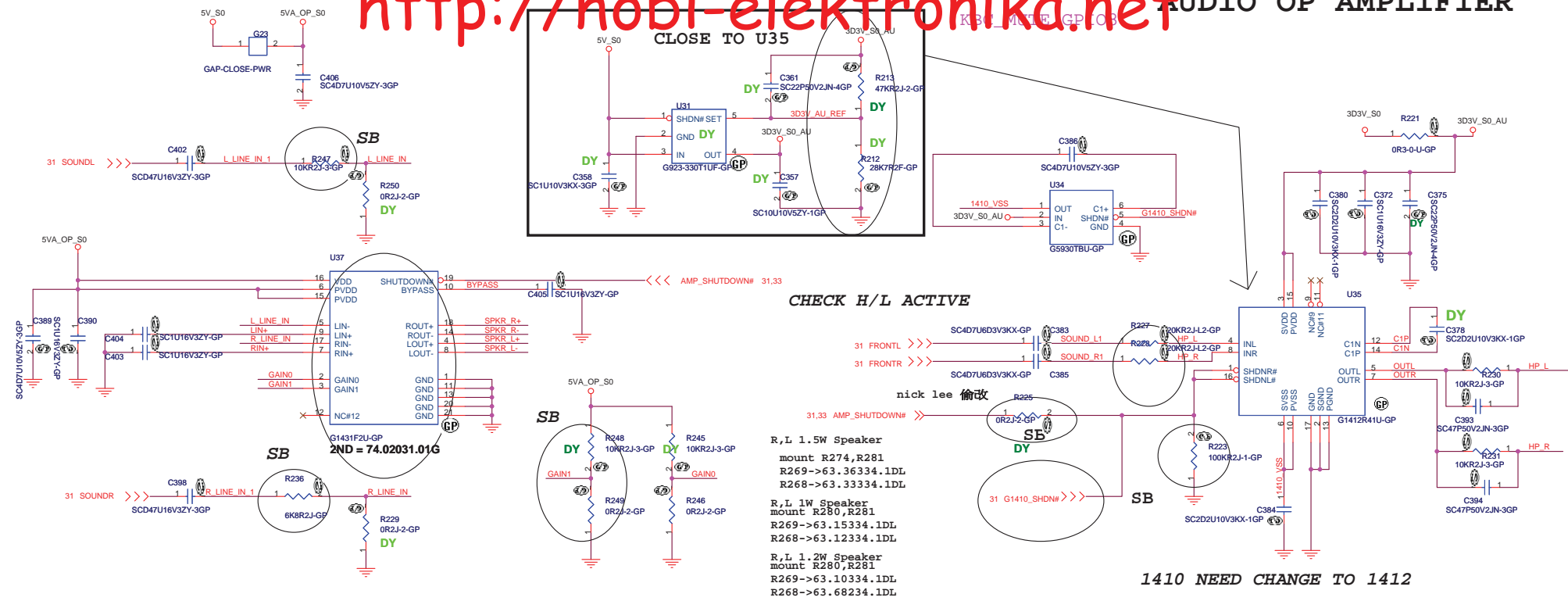
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / NEW CARD**

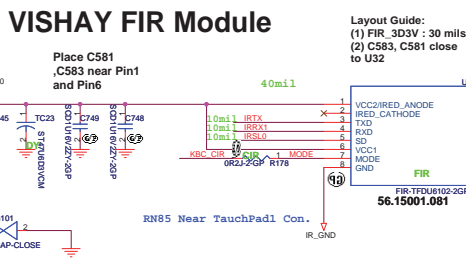
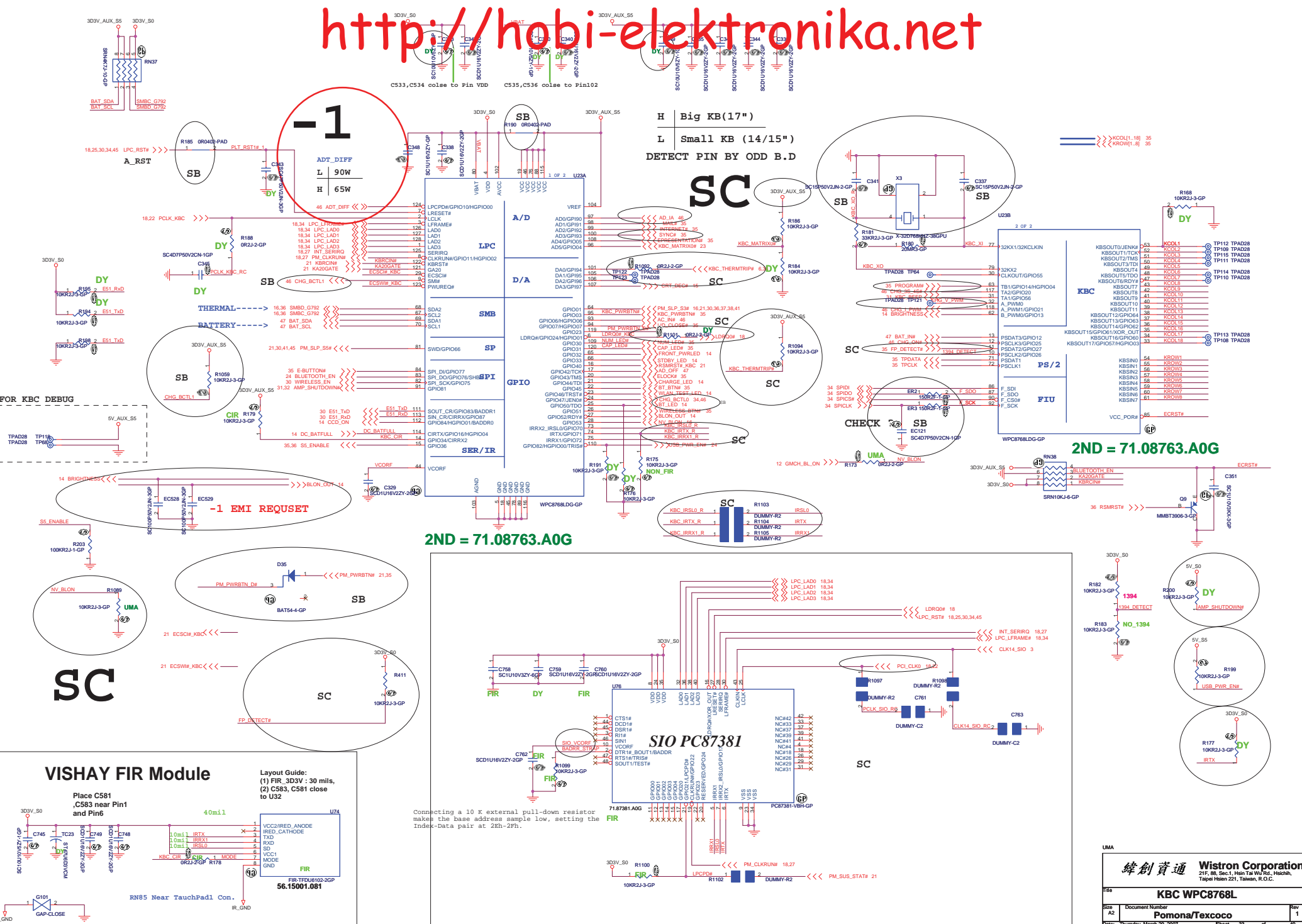
Size: Document Number **Pomona/Textcoco** Rev: 1

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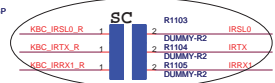


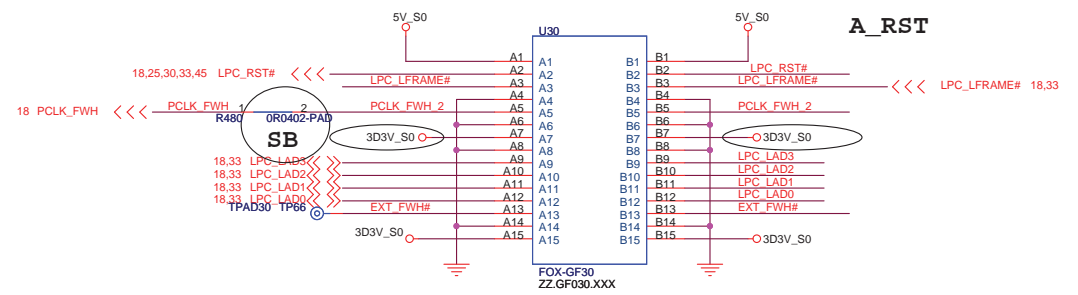
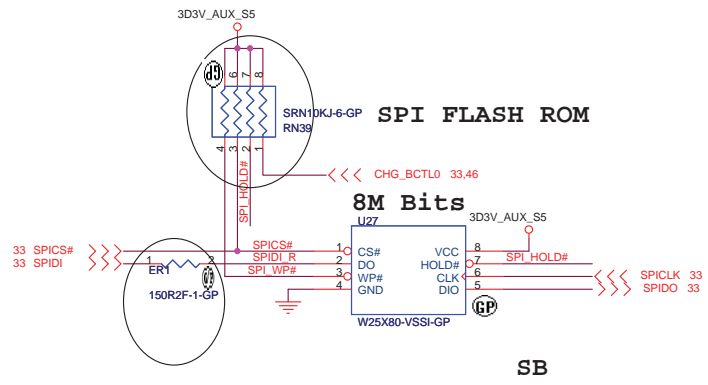


C533, C534 close to Pin VDD C535, C536 close to Pin102



2N2 = 71.08763.A0G

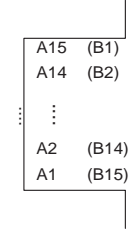




GOLDEN FINGER FOR DEBUG BOARD
Check;MYALL M

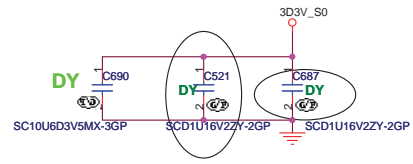
1. Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
2. Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
3. Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)

TOP VIEW

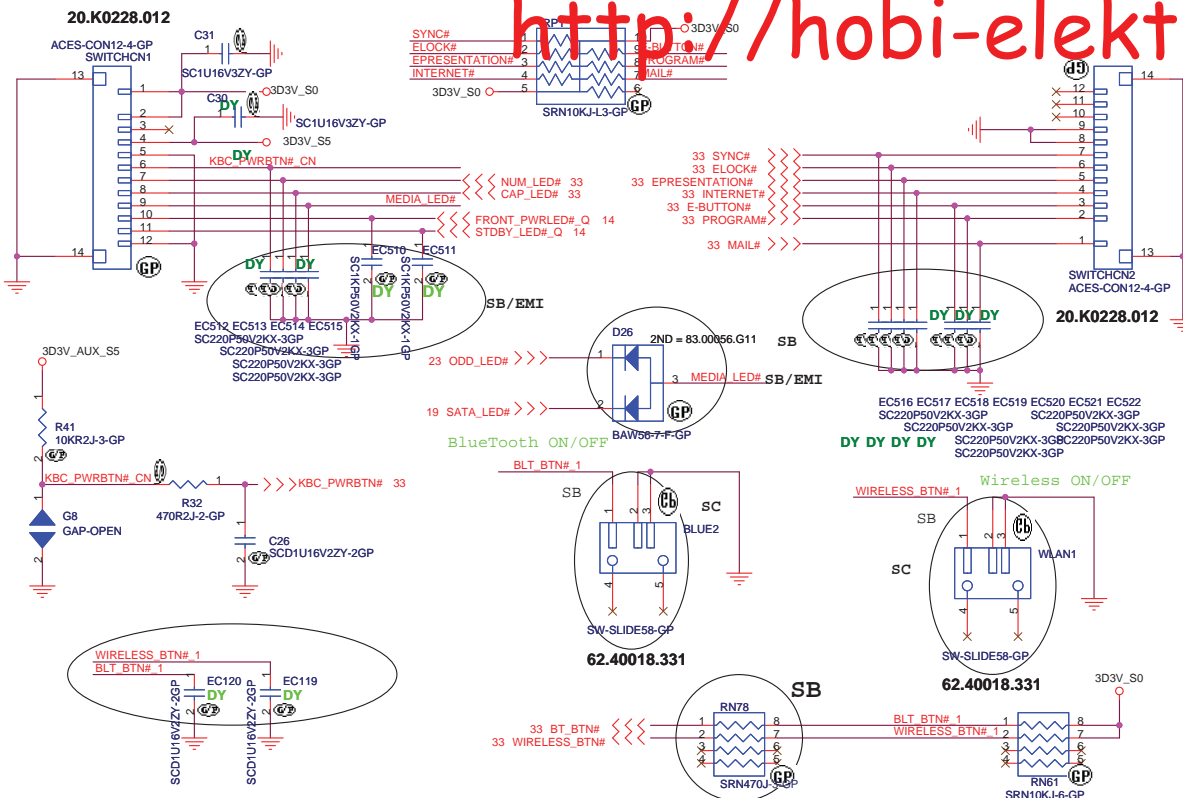


(BOTTOM VIEW)

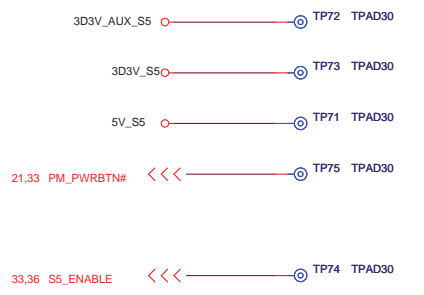
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



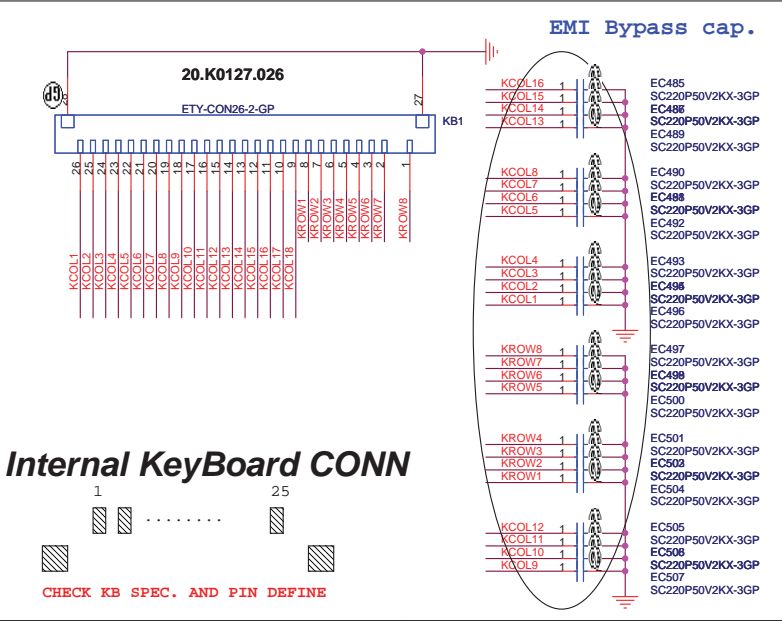
UMA			
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
BIOS			
Title			
Size A3	Document Number	Rev	
	Pomona/Texcoco	1	
Date:	Thursday, March 29, 2007	Sheet	34 of 49



Check test point

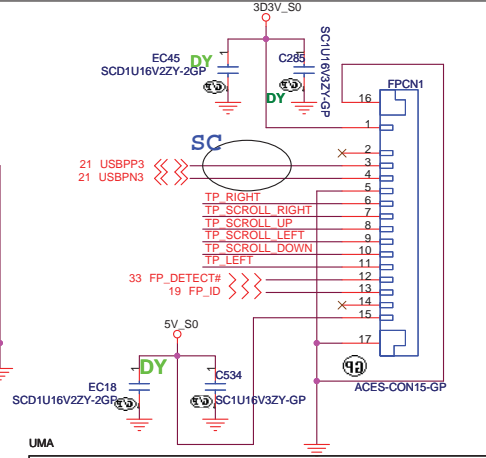
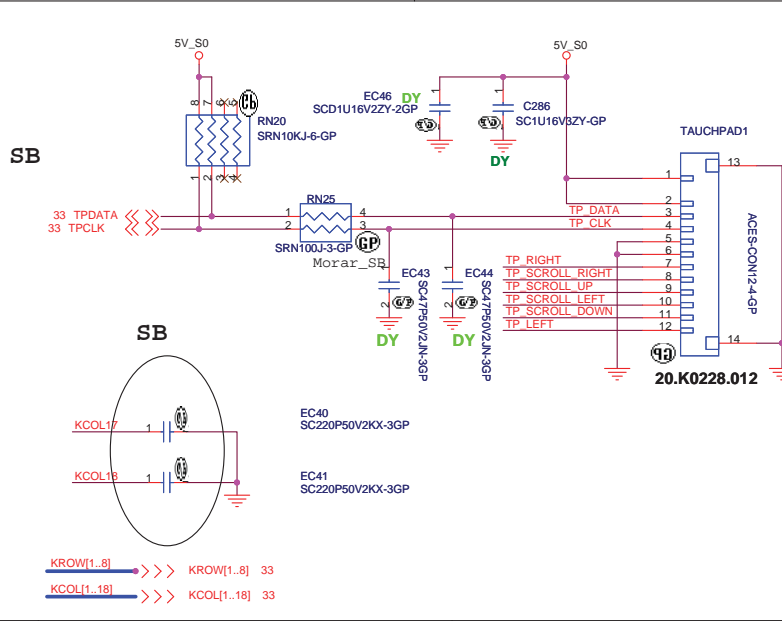


Test Point放在Dimm Door打開可量測處



Internal Keyboard CONN

CHECK KB SPEC. AND PIN DEFINE



UMA

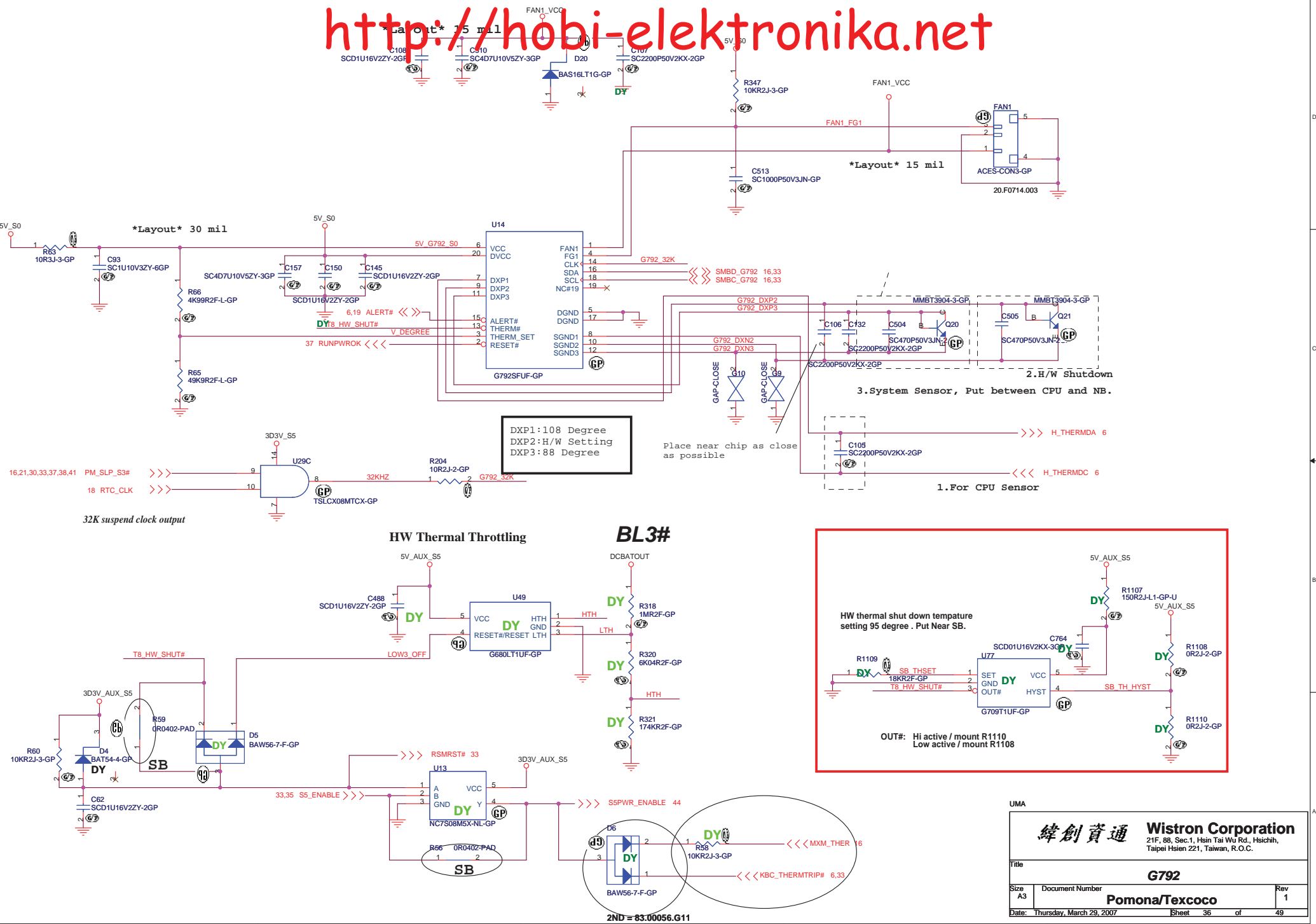
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONs / KB / TOUCHPAD**

Size: Document Number

Pomona/Textcoco

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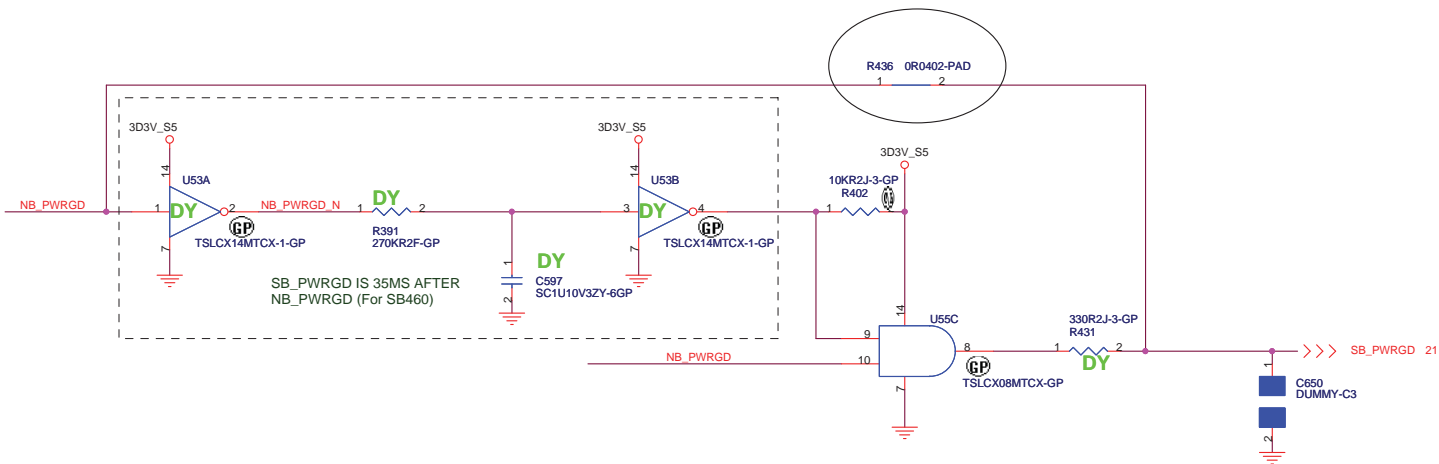
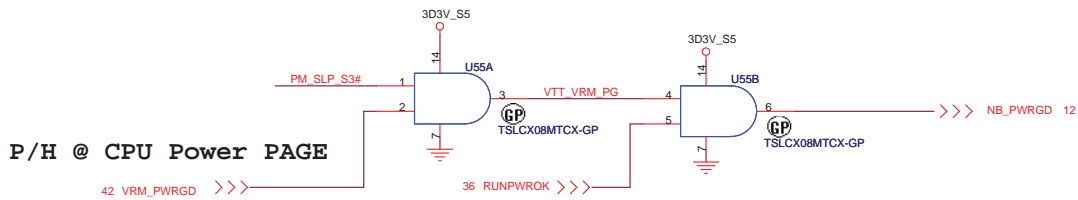
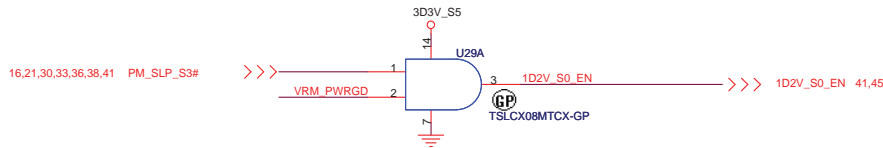
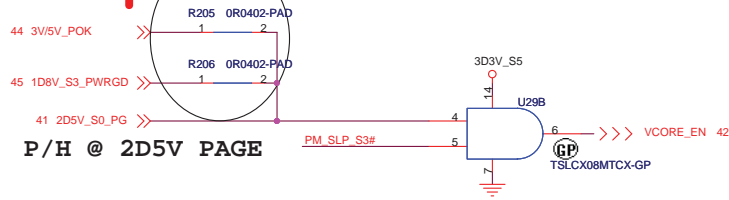
UMA

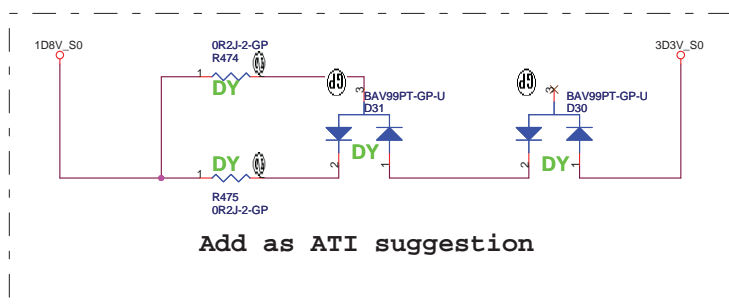
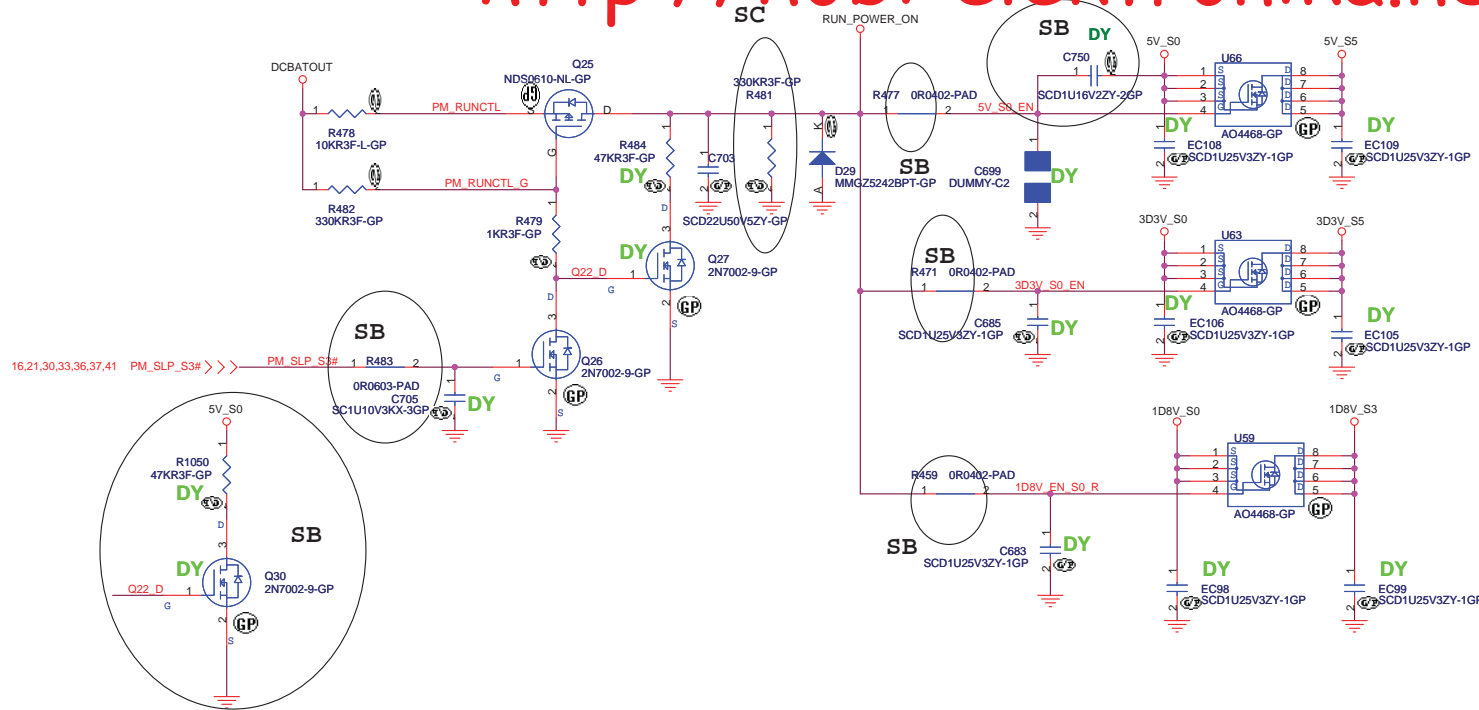
緯創資通 Wistron Corporation
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Title: **G792**

Size A3 Document Number **Pomona/Textcoco** Rev 1

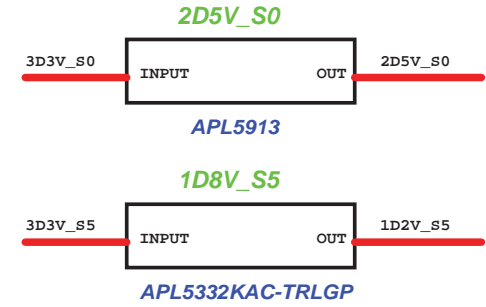
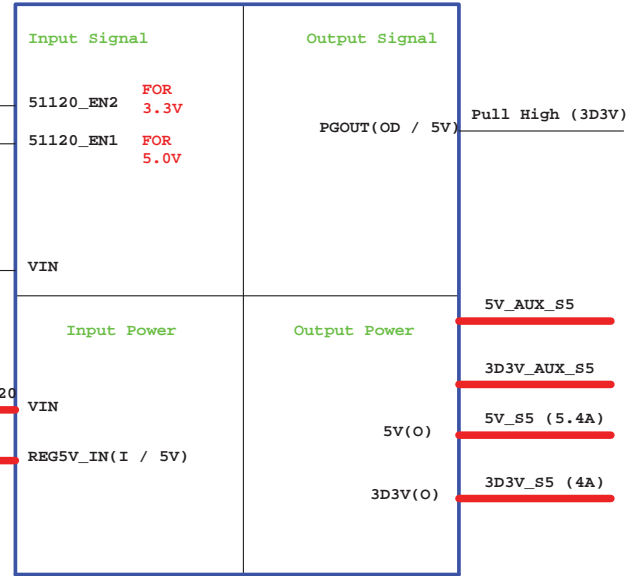
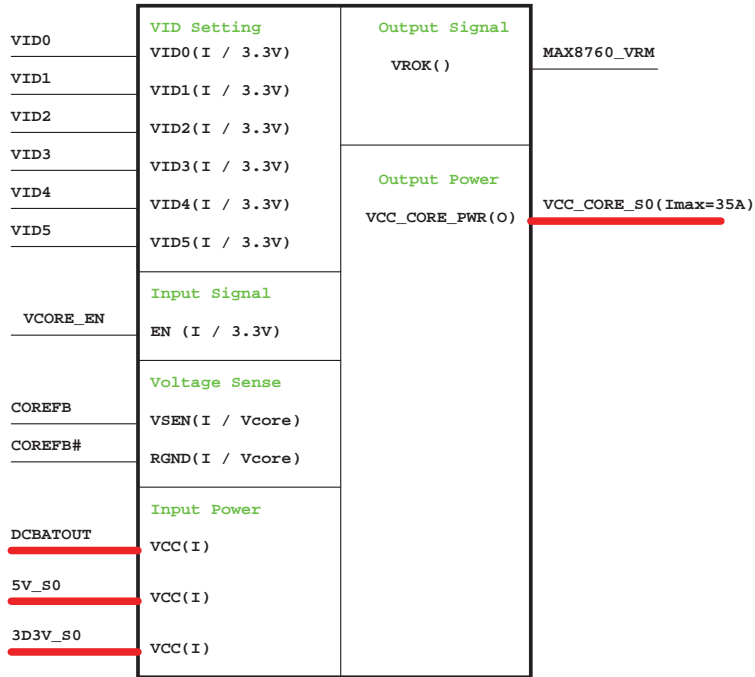
Date: Thursday, March 29, 2007 Sheet 36 of 49



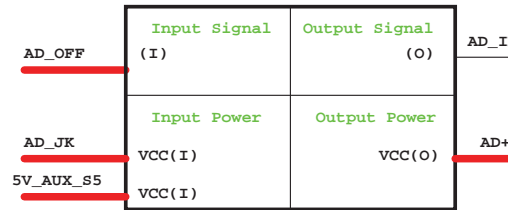


UMA		
緯創資通		Wistron Corporation
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Title PWR CTL LOGIC / PWR PLANE		
Size A3	Document Number Pomona/Textcoco	Rev 1
Date: Thursday, March 29, 2007	Sheet 38 of	49

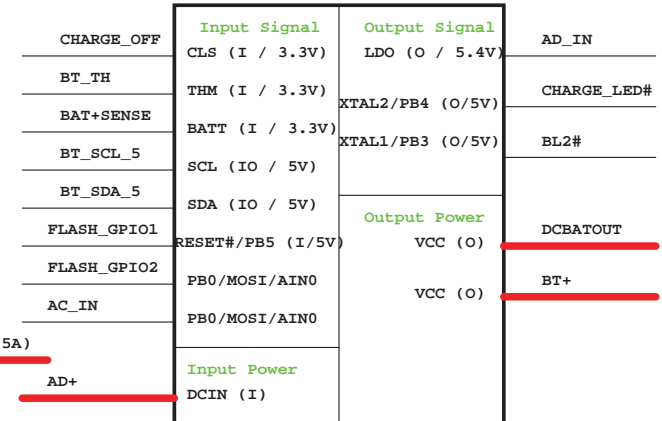
CPU_CORE ISL6264CRZ



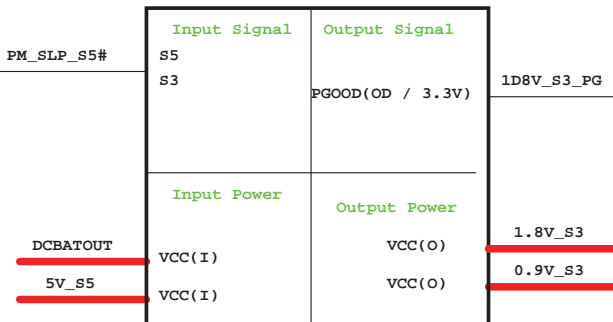
Adapter



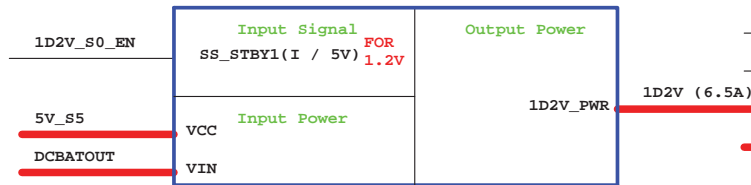
Charger_ISL6255



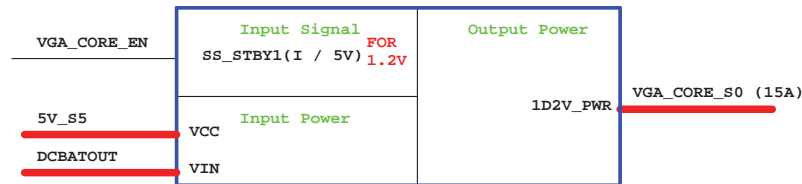
TI TPS51116 1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



UMA

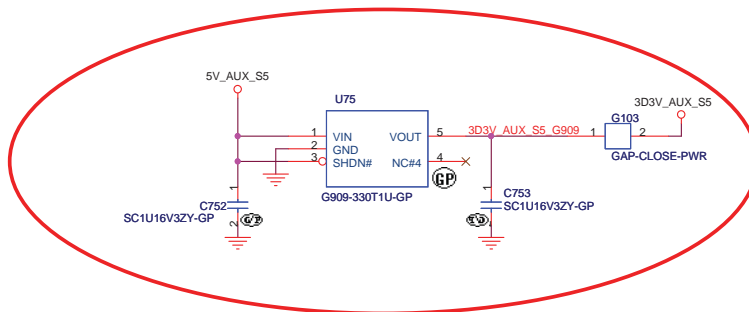
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size A3 Document Number: **Pomona/Texcoco** Rev: **1**

Date: Thursday, March 29, 2007 Sheet 39 of 49

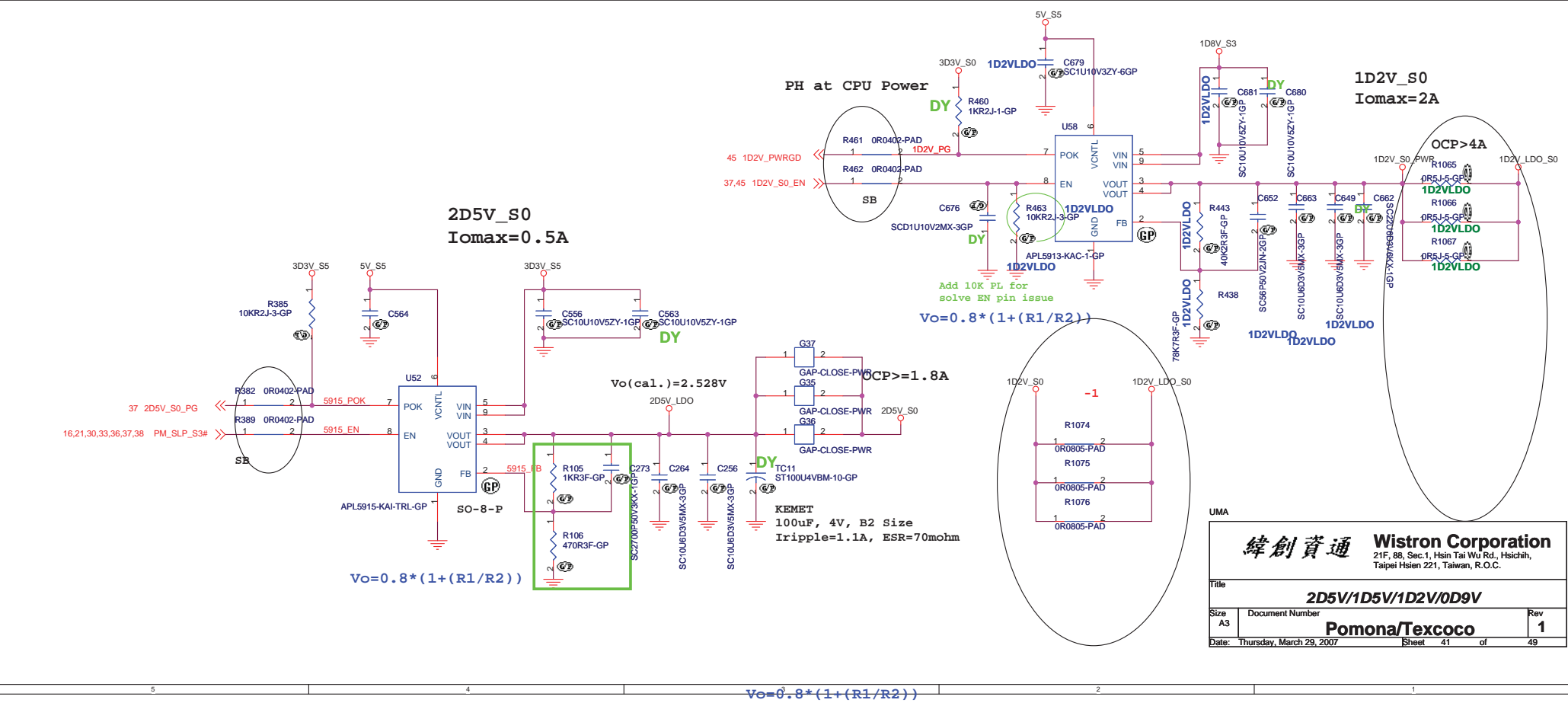
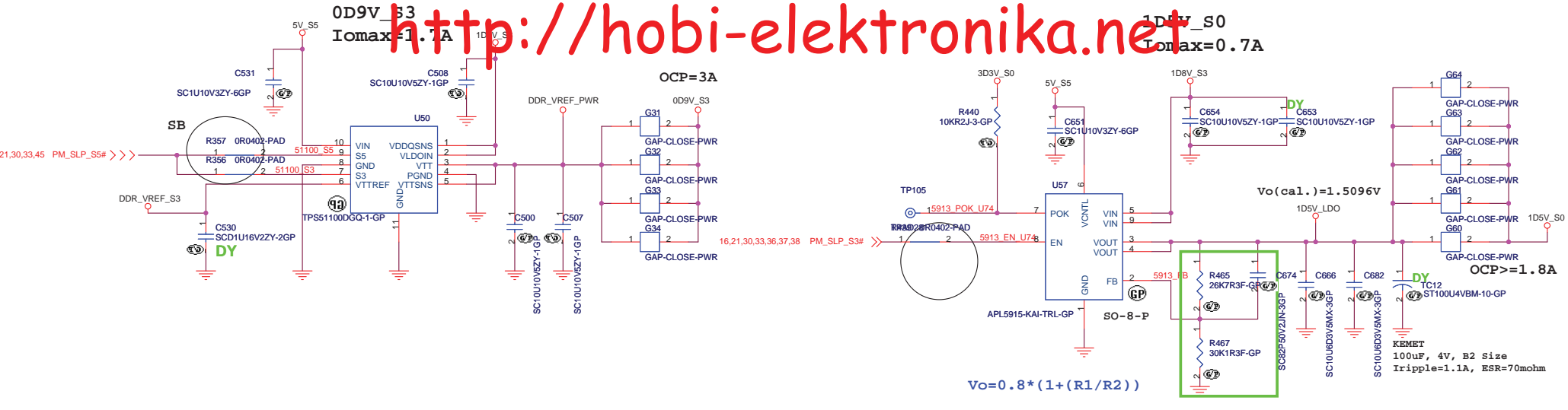
Aux Power 3D3V_AUX_S5



SB modify

UMA

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		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
3D3V AUX			
Size	Document Number	Rev	
A3	Pomona/Textcoco	1	
Date: Thursday, March 29, 2007		Sheet 40	of 49



UMA

緯創資通 Wistron Corporation
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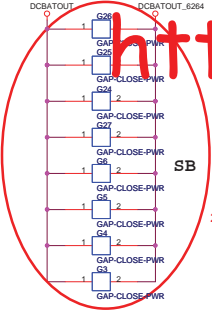
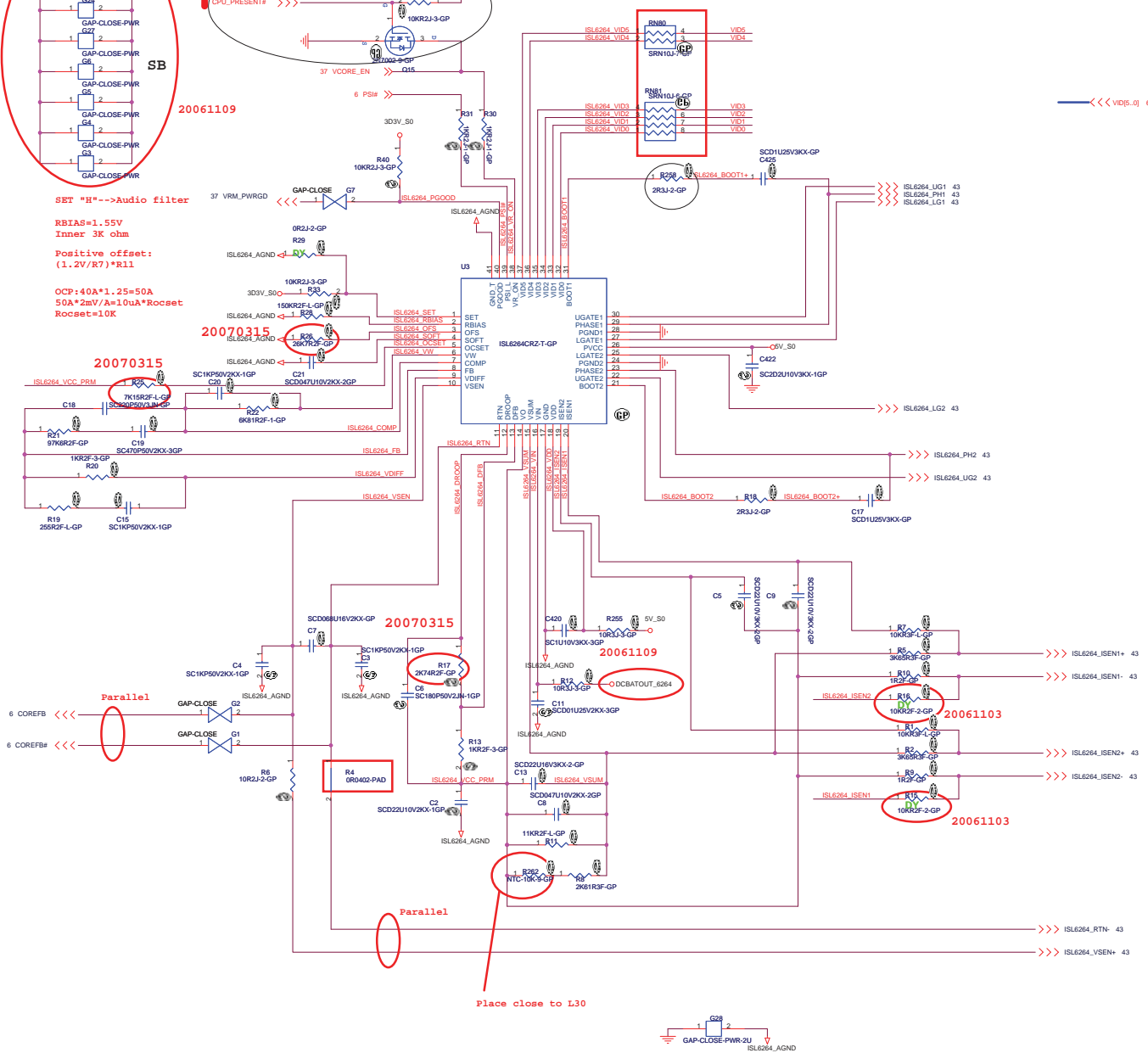
Title		
2D5V/1D5V/1D2V/0D9V		
Size	Document Number	Rev
A3	Pomona/Textcoco	1
Date:	Thursday, March 29, 2007	Sheet 41 of 49

High(3D3V)=> Vout=1.2V
Low(0V) => Vout=1.0V

CPU_VCORE
 VID=1.20V(25W)/1.15V(35W)
 I_{omax}=21A(25W)/35A (35W)
 OCP=40A~45A

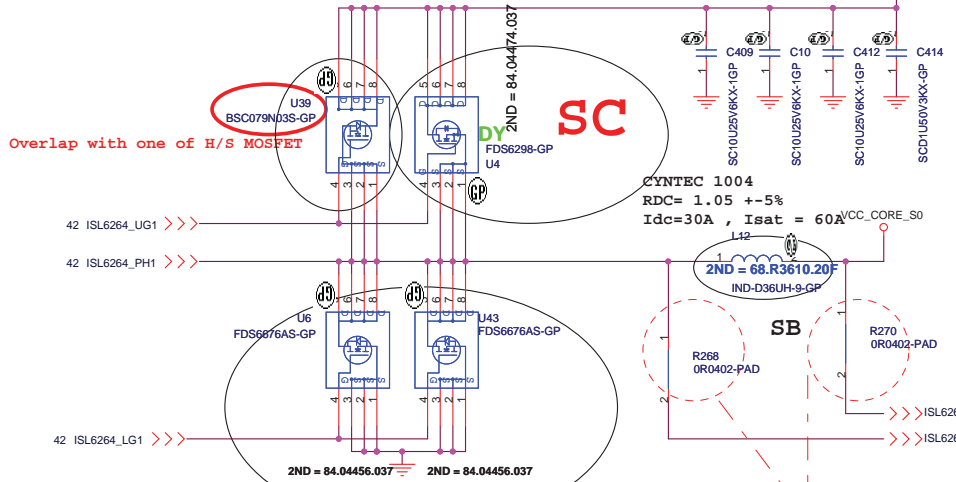
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.500
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



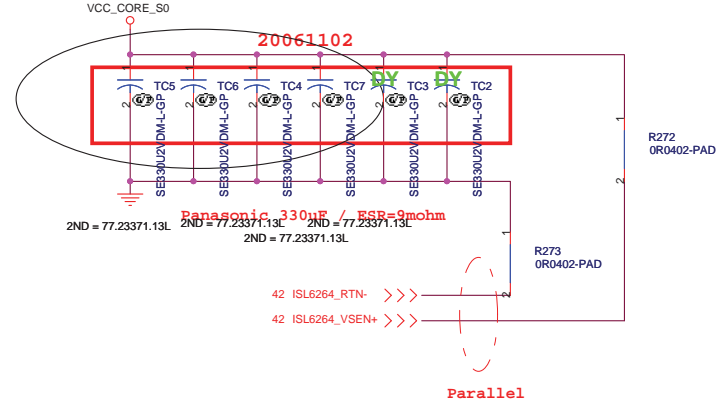
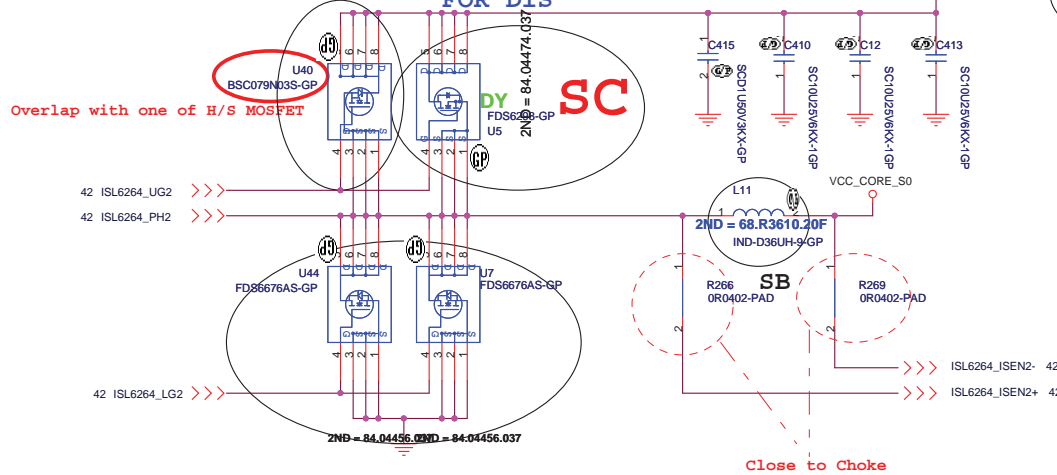
SET "R" --> Audio filter
 RBIAS=1.55V
 Inner 3K ohm
 Positive offset:
 (1.2V/R7)*R11
 OCP=40A*1.25=50A
 50A*2mV/A=10uA*Rocset
 Rocset=10K

SB 2ND SOURCE FOR DIS



VCC_CORE_S0

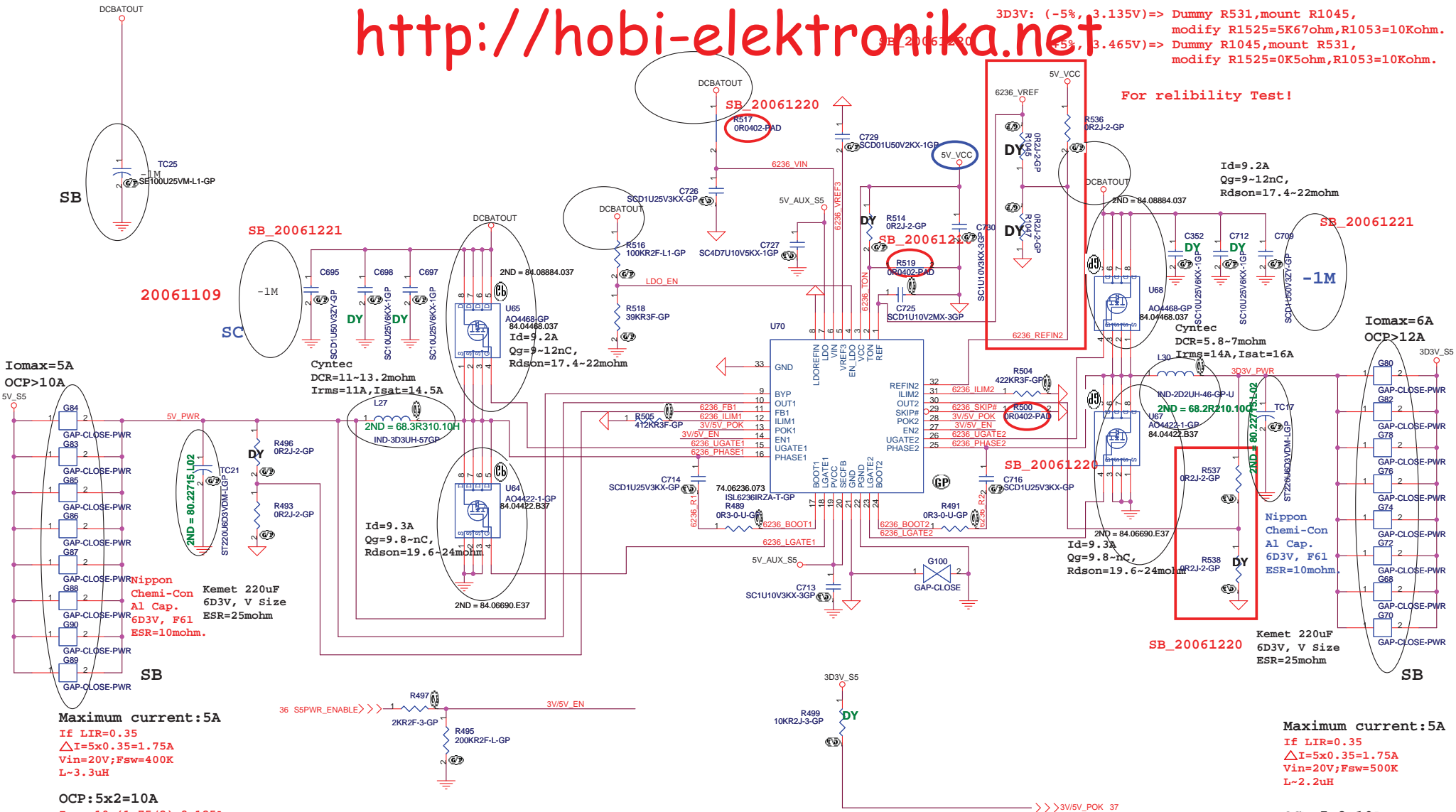
SB 2ND SOURCE SB 2ND FOR DIS



CYNTEC 1004
RDC= 1.05 +-5% , Idc=30A , Isat = 60A

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Title CPU Vcore Power_2	
Size A3	Document Number Pomona/Texcoco
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3D3V: (-5%, 3.135V) => Dummy R531, mount R1045, modify R1525=5K67ohm, R1053=10Kohm.
 3D3V: (-5%, 3.465V) => Dummy R1045, mount R531, modify R1525=0K5ohm, R1053=10Kohm.



Iomax=5A
 OCP>10A

SB

Maximum current: 5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 400K$
 $L \sim 3.3\mu H$
 OCP: $5 \times 2 = 10A$
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5\mu A$
 $\sim 438K \rightarrow 442K$

Nippon Chemi-Con Al Cap.
 6D3V, F61
 ESR=10mohm.

Kemet 220uF
 6D3V, V Size
 ESR=25mohm

Id=9.3A
 Qg=9.8-nC,
 Rdson=19.6-24mohm

SB_20061221
 -1M
 SC
 20061109
 -1M

Cyntec
 DCR=11-13.2mohm
 Irms=11A, Isat=14.5A

U65
 AQ4468-GP
 84.04468.037
 Id=9.2A
 Qg=9-12nC,
 Rdson=17.4-22mohm

U70
 LD0REFIN
 LDO
 VIN
 VREF
 EN
 LDO
 TON
 REF

U64
 AQ4422-1-GP
 84.04422.B37

U68
 AQ4468-GP
 84.04468.037

Cyntec
 DCR=5.8-7mohm
 Irms=14A, Isat=16A

Id=9.2A
 Qg=9-12nC,
 Rdson=17.4-22mohm

Iomax=6A
 OCP>12A

For reliability Test!

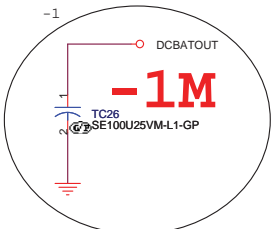
Nippon Chemi-Con Al Cap.
 6D3V, F61
 ESR=10mohm.

Kemet 220uF
 6D3V, V Size
 ESR=25mohm

Maximum current: 5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 500K$
 $L \sim 2.2\mu H$

OCP: $5 \times 2 = 10A$
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5\mu A$
 $\sim 438K \rightarrow 442K$

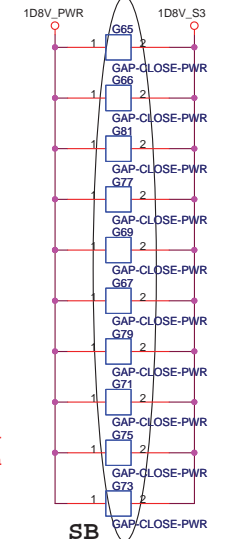
UMA			
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ISL6236 5V 3D3V			
Size A3	Document Number	Pomona/Textcoco	Rev 1
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Id=9.6A
Qg=18-nC,
Rdson=13.5-16.5mohm

-1M

1D8V Iomax=8A
OCP>16A



Id=13.2A
Qg=27nC,
Rdson=6.8-8.2mohm

SC remove TC19

Nippon Chemi-Con Al Cap.
390uF/2D5V
ESR=15mohm

PH at 2D5V Power Page

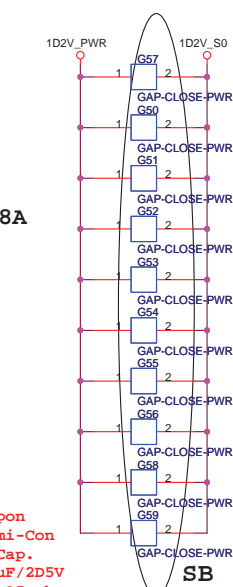
>>>1D8V_S3_PWRGD 37

PH at CPU Power Page

SB_20061220

$V_{out} = 0.758V * (R1 + R2) / R2$

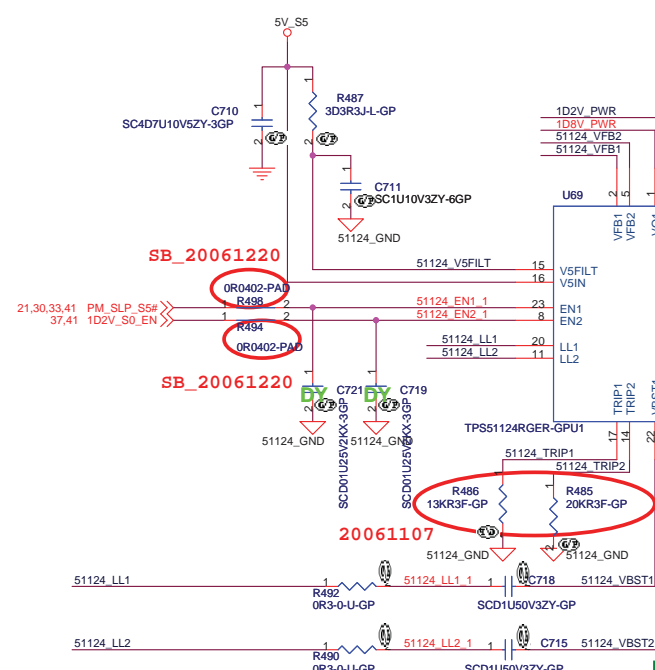
SC



Id=9.2A
Qg=9-12nC,
Rdson=17.4-22mohm

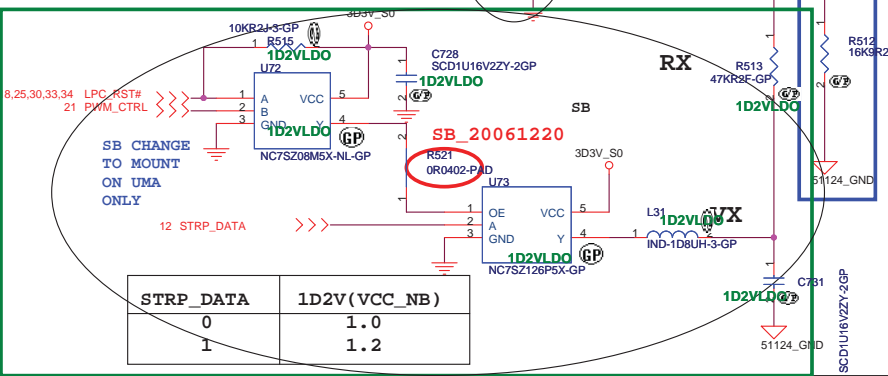
-1M

1D2V Iomax=8A
OCP>16A



$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2



STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

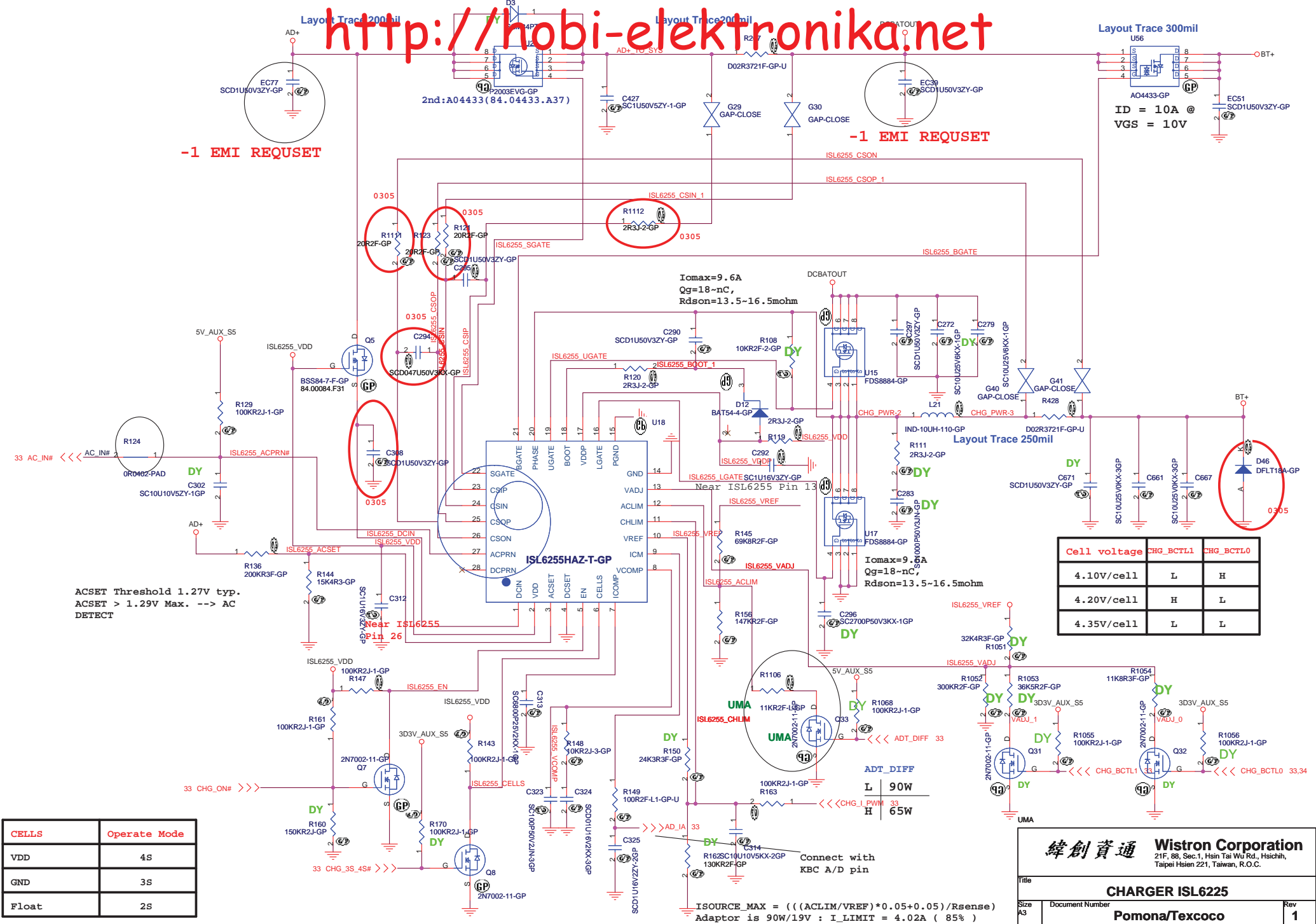
UMA

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Title: **TPS51124 1D8V 1D2V**

Size A3 Document Number: **Pomona/Texcoco** Rev: **1**

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-1 EMI REQUSET

-1 EMI REQUSET

ID = 10A @
VGS = 10V

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. ---> AC
DETECT

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

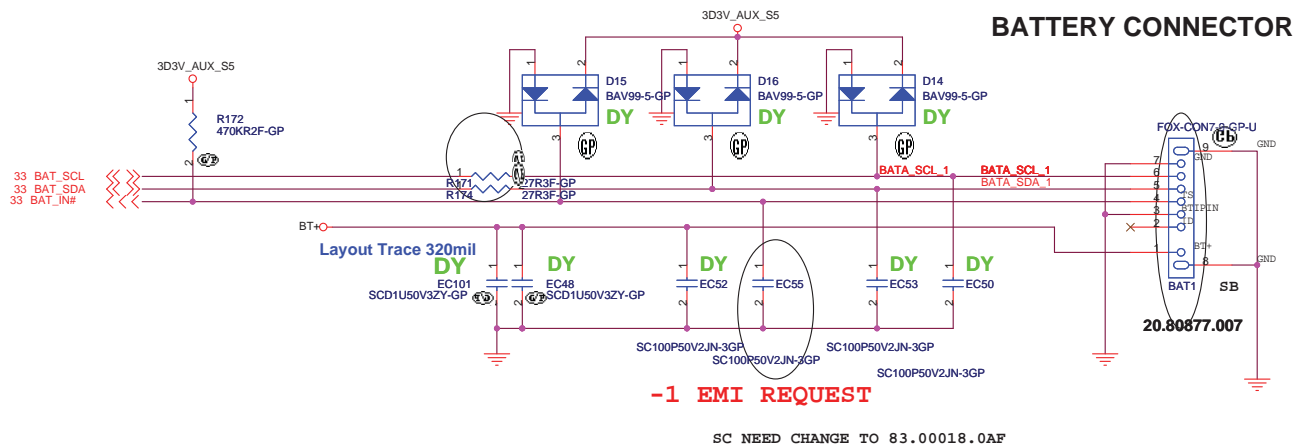
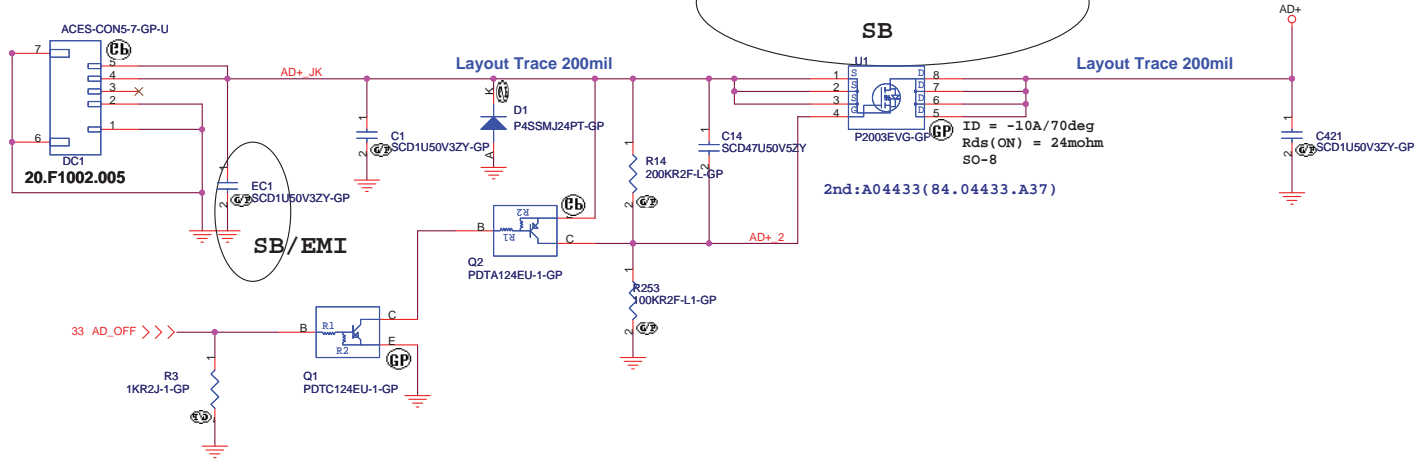
ISOURCE_MAX = ((ACLIM/VREF)*0.05+0.05)/Rsense
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

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Taipei Hsien 221, Taiwan, R.O.C.

CHARGER ISL6225

Size A3 Document Number **Pomona/Texcoco** Rev **1**

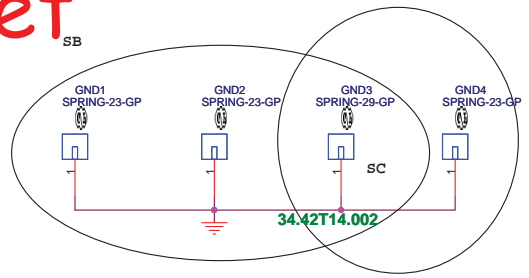
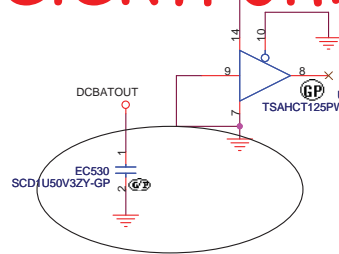
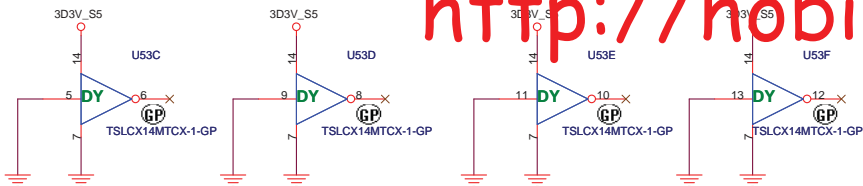
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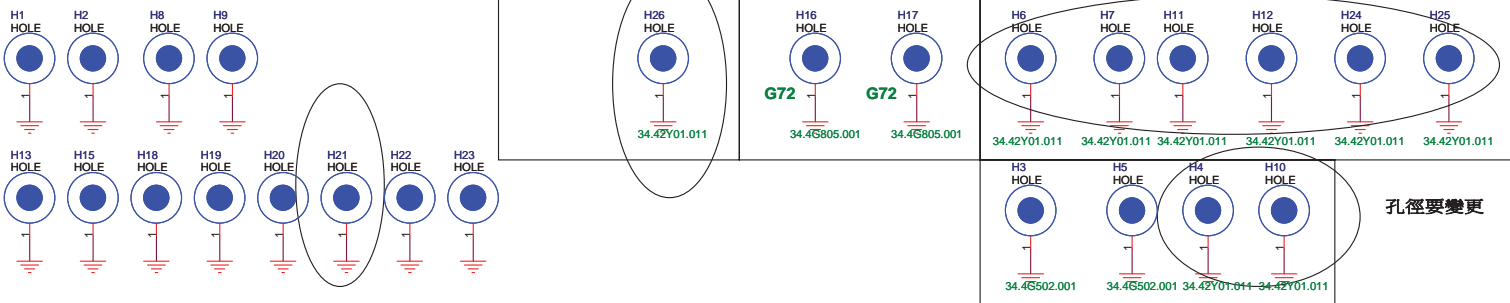
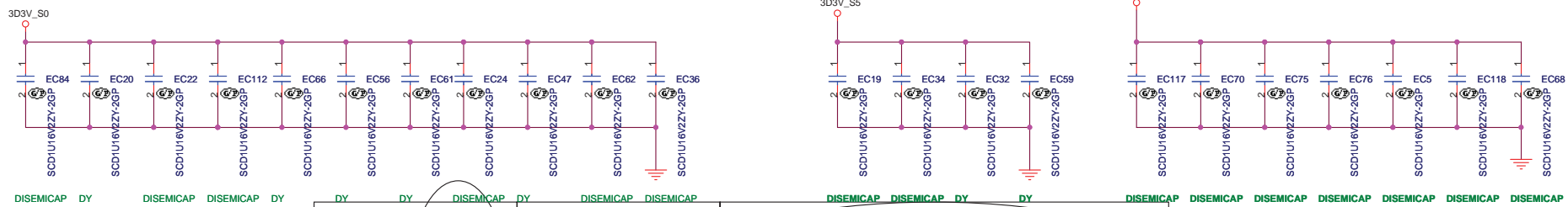
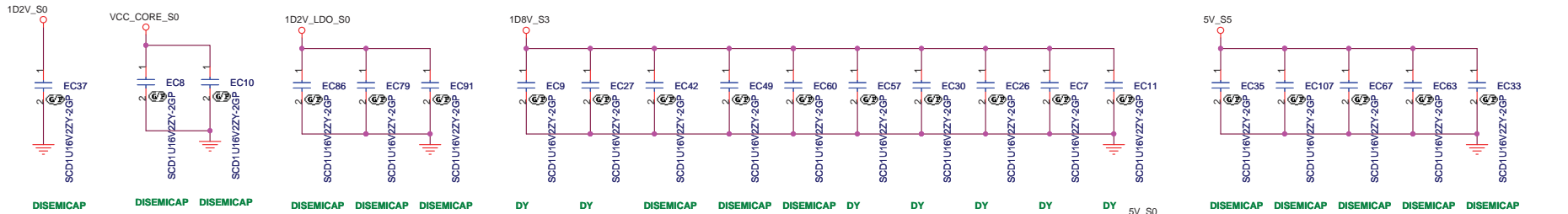
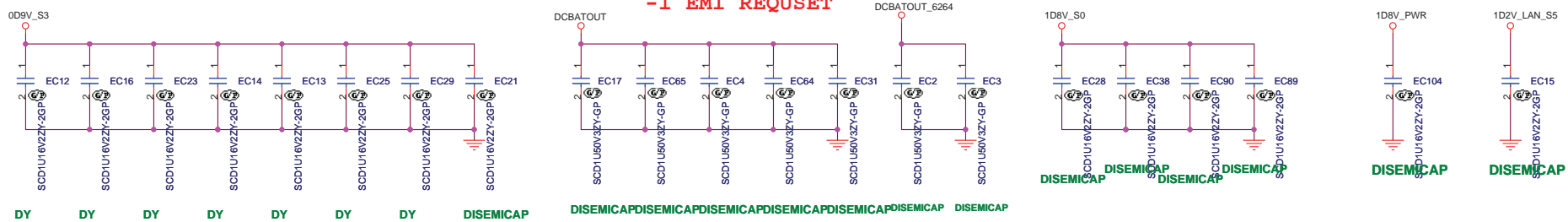
SC

UMA

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Title AD/BATT CONN	
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-1 EMI REQUSET



孔徑要變更

UMA

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Title: **EMI/Spring/Boss**

Size: Document Number: **Pomona/Textcoco** Rev: 1

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PAGE3 BY RN21-24,RN34-RN36,R132,9LPR462AGLF INTERNAL P/D.
PAGE3 CHANGE X2,C307,C311 BY KDS SUGGESTION
PAGE14 ADD F2 BETWEEN DCBATOUT AND LCD CONN.
PAGE14 CHANGE LED2 TO DUAL COLOR LED FOR POWER LED AND STANDBY LED.
PAGE14 CHANGE LED4 TO DUAL COLOR LED FOR CHARGER LED AND DC_BATT_FULL_LED
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C479,483,490 TO 15P FROM 6.8P FOR SOLVE SIV ISSUE.DIS ONLY;UMA WILL KEEP 6.8P
PAGE18 CHANGE X1,C259,C270 BY KDS SUGGESTION
PAGE19 CHANGE X5,C655,C656 BY KDS SUGGESTION
PAGE19 PSW_CLK# P/U 10K TO 3D3V_S5
PAGE21 CHANGE R101 TO DY FOR ECSWI#_KBC AND CHANGE TO R531 THAT CONNECT TO USB_OC6#(GEVENT6#)
PAGE23 CHANGE SATAL CONN.
PAGE23 CHANGE ODD1 CONN.
PAGE24 CHANGE R27 TO 10R FOR SOLVE ACZ_SDATAIN1 OF SIV FAIL ITEM
PAGE25 CHANGE X4,C471,C472 BY KDS SUGGESTION
PAGE26 CHANGE RJ1 CONN.AND LAN_ACT_LED# TO B2 FROM A1,10M/100M/1G_LED# FROM B2 TO A3
PAGE26 CHANGE LAN_ACT_LED# TO B2 FROM A1
PAGE26 CHANGE 10M/100M/1G_LED# FROM B2 TO A3
PAGE28 CHANGE C631,C689 TO 6.8P BY KDS SUGGESTION
PAGE30 CHANGE NEW1 CONN.
PAGE30 CHANGE MINIC1 CONN.
PAGE30 ADD R537 AND SET TO DY
PAGE31 CHANGE R215 TO 27R FOR SOLVE ACZ_SDATAIN0 OF SIV FAIL ITEM
PAGE31 ADD R538 OR AND SET INTERNAL MIC TO LEFT CHANNEL,DY R224,D17 AND ADD D36
PAGE31 SET C391 TO DY FOR POP SOUND
PAGE31 CHANGE R247 TO 10K;R236 TO 6.8K;R248 TO DY;249 TO STUFF FOR SET GAIN TO 1.2W
PAGE31 CHANGE R238,239,242,243 TO 0R
PAGE31 CHANGE R223 TO STUFF
PAGE31 CHANGE INTMIC1 CONN.
PAGE31 CHANGE SPKR1 CONN.
PAGE33 ADD D35 BETWEEN KBC AND PM_PWRBTN#
PAGE33 DY R197 AND STUFF R193 FOR SET PCB VER. TO 001
PAGE33 CHANGE X3,C337,C341 BY KDS SUGGESTION
PAGE34 Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)
PAGE33 CHANGE WLAN1,BLUE2 CONN.
PAGE37 SET R453 TO DY
PAGE38 ADD C750

-1

- 1.Change U19 ATIGLCK3 to SRCCLK3.PAGE3
- 2.Change U19 ATIGLCK2 to SRCCLK1.PAGE3
- 3.Add CLK14_SIO of U19;PIN62 FOR Super I/O.PAGE3
- 4.Change THERMTRIP# TO KBC GPI94.PAGE6
- 5.Change LDT_RST#;LDT_STP#;SB_CPUPWRGD P/L resistor to 680 ohms by AMD reccommand.PAGE6
- 6.Adjust current limit resistor for FRONT_PWRLED.R1113 change to 68 ohms.PAGE14
- 7.Adjust current limit resistor for BT_LED.R251 change to 390 ohms.PAGE14
- 8.Adjust current limit resistor for DC_BATFULL_LED.R1116 change to 68 ohms.PAGE14
- 9.Add R1093 P/H 10K ohms TO 3D3V_S0 for solve WLAN_LED light leak in dos mode.PAGE14
- 10.Remove damping resistor of TMDS signal.PAGE16
- 11.Remove bridge resistor of TMDS signal.PAGE17
- 12.Change FP_DETECT TO KBC GPIO27.PAGE19
- 13.Change USB7 from PORT7 to PORT1 of U19.PAGE21
- 14.Change PCB_VER0/1 form KBC to GPIO4/5 of U19.PAGE21
- 15.Add ESD diode D38-D45 for USB signal.PAGE23
- 16.Add damping resistor 22 ohms and P/L CAP 22P for SD_CLK for EMI.PAGE27
- 17.Add P/L CAP 33P for SD/MMC_D0-D3 for EMI.PAGE29
- 18.Dummy R1062,R1058 and mount R1061 for MINICARD.PAGE30
- 19.Remove MIC array design.PAGE31
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