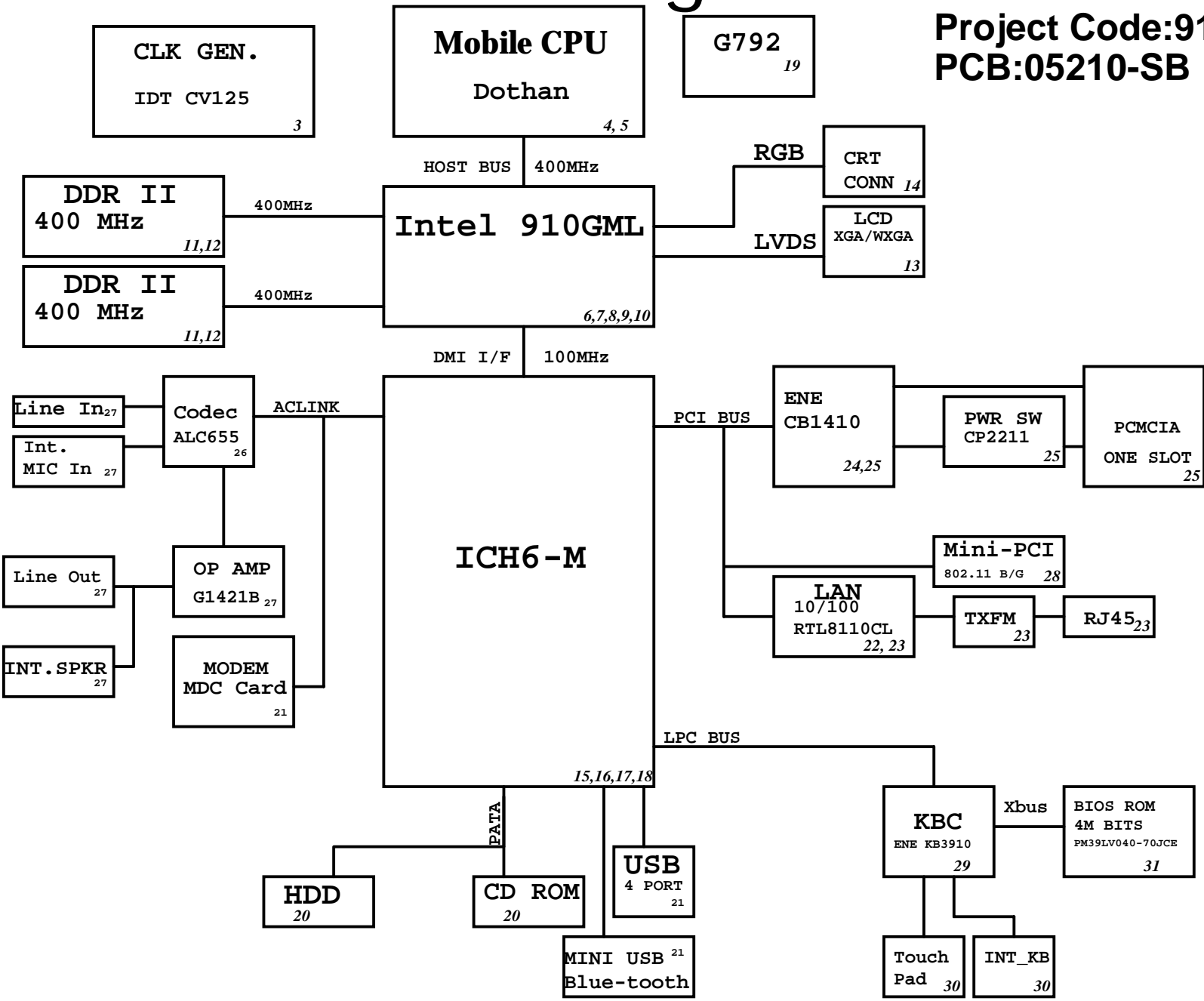


# Morar Block Diagram 2005/05/28

Project Code:91.4E101.001  
PCB:05210-SB



SYSTEM DC/DC TPS5130 35,36	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5 1D05V_S0 2D5V_S0 (LDO)

SYSTEM DC/DC ISL6227 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DQ 37	
INPUTS	OUTPUTS
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER ISL6255 38	
INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

CPU DC/DC ISL6218CV-T 34	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

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Taipei Hsien 221, Taiwan, R.O.C.

# Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = <b>DMI x4</b> (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = <b>Dothan</b> (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = <b>Normal Operation</b> (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = <b>Dynamic ODT Enabled</b> (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = <b>1.05V</b> (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = <b>1.05V</b> (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = <b>No SDVO device present</b> (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH FWORK In signal.

## PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

# ICH6-M Integrated Pull-up and Pull-down Resistors

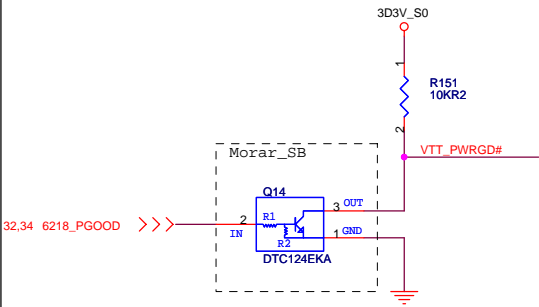
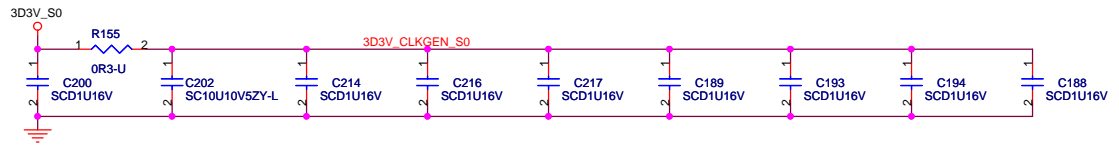
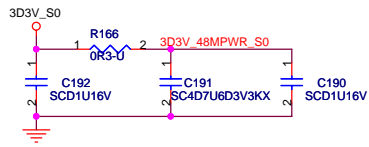
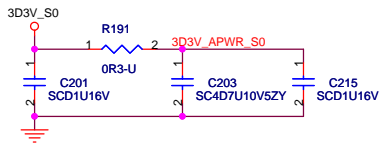
ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

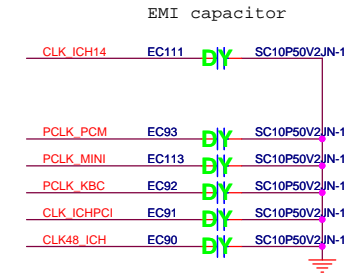
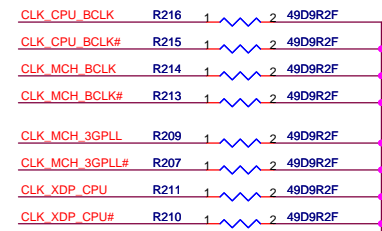
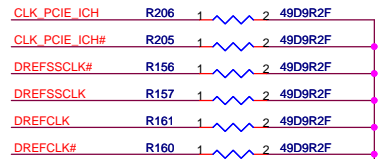
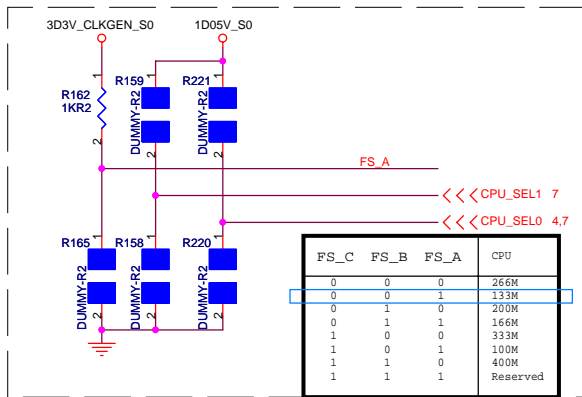
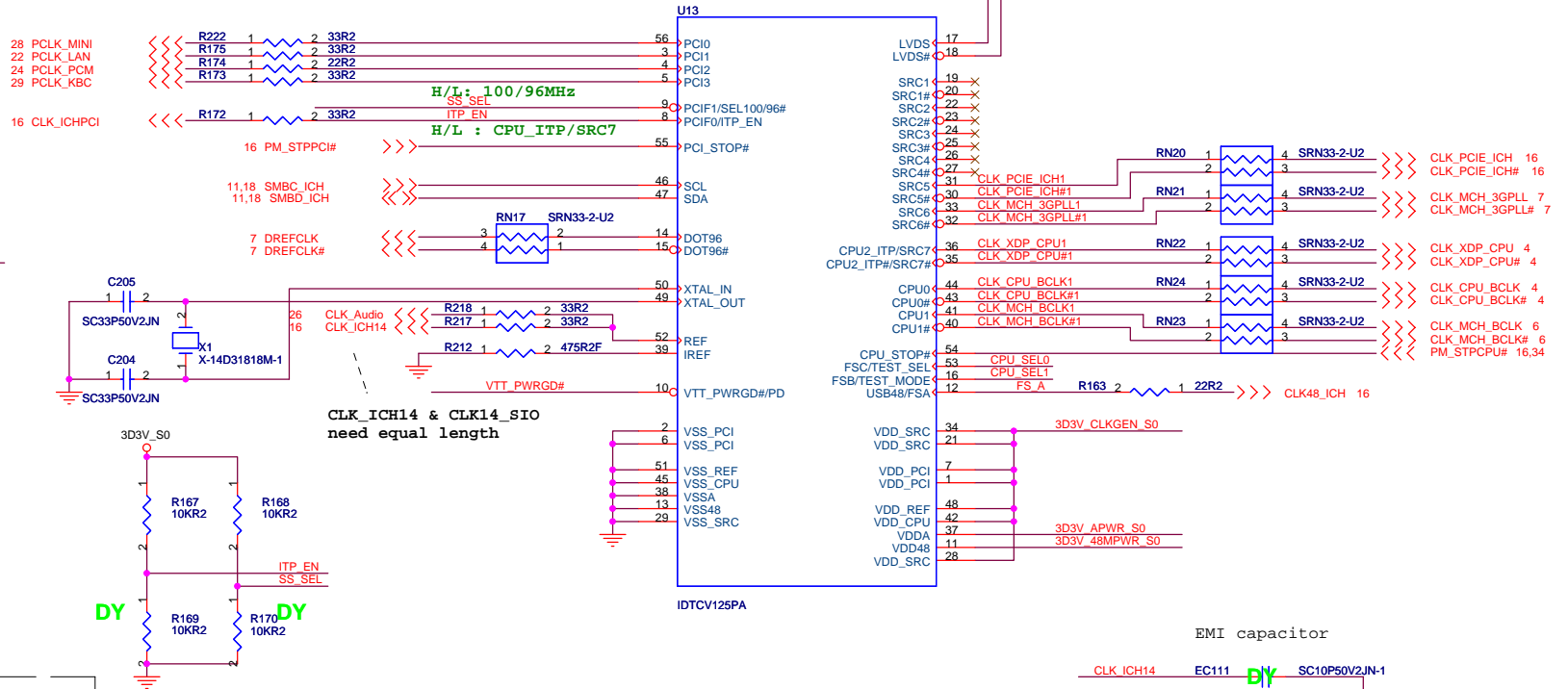
## ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

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<b>Memo</b>	
Size A3	Document Number
Date: Saturday, May 28, 2005	Sheet 2 of 40
<b>MORAR</b>	<b>SB</b>



IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z



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Title: **Clock Generator - IDT125**

Size A3 Document Number **MORAR** Rev **SB**

Date: Friday, June 24, 2005 Sheet 3 of 40

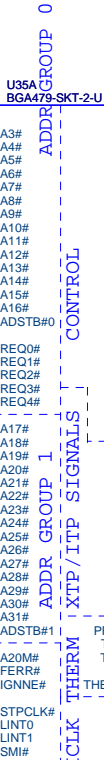
6 H\_A#[31..3]

6 H\_ADSTB#0  
6 H\_REQ#[4..0]

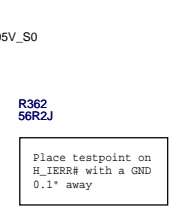
6 H\_ADSTB#1

15 H\_A20M#  
15 H\_FERR#  
15 H\_IGNNE#

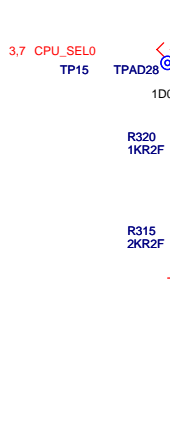
H\_STPCLK#  
15 H\_NMI#  
15 H\_SMI#



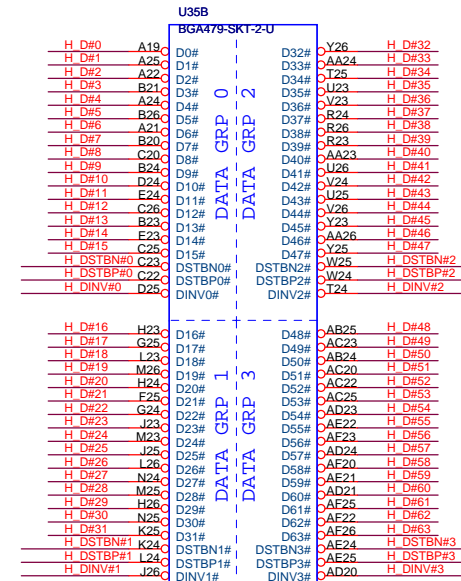
connector  
62.10053.061  
Morar\_SA:62.10053.061  
Morar\_SB:62.10053.061  
Morar\_SB:62.10055.011(2nd)



PM\_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)

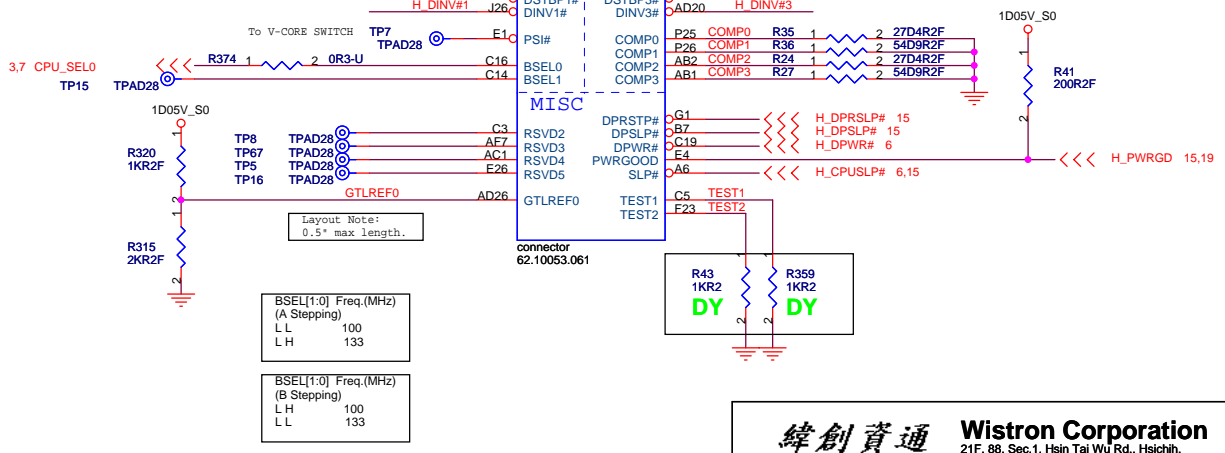


All place within 2" to CPU



H\_D#[63..0] 6  
H\_DINV#[3..0] 6  
H\_DSTBN#[3..0] 6  
H\_DSTBP#[3..0] 6

Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

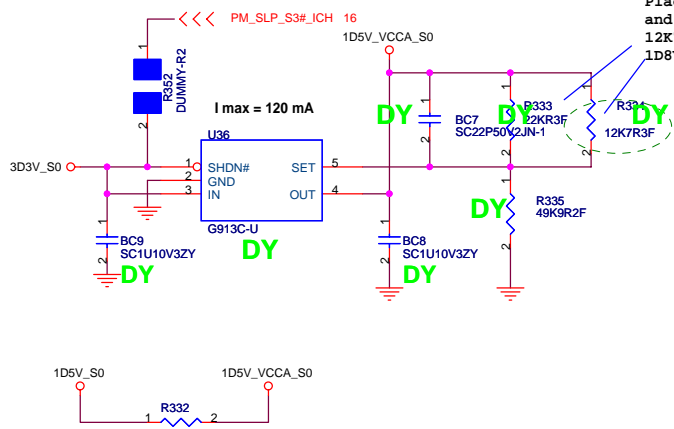
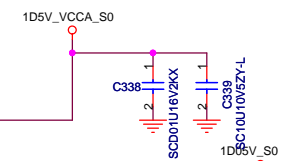
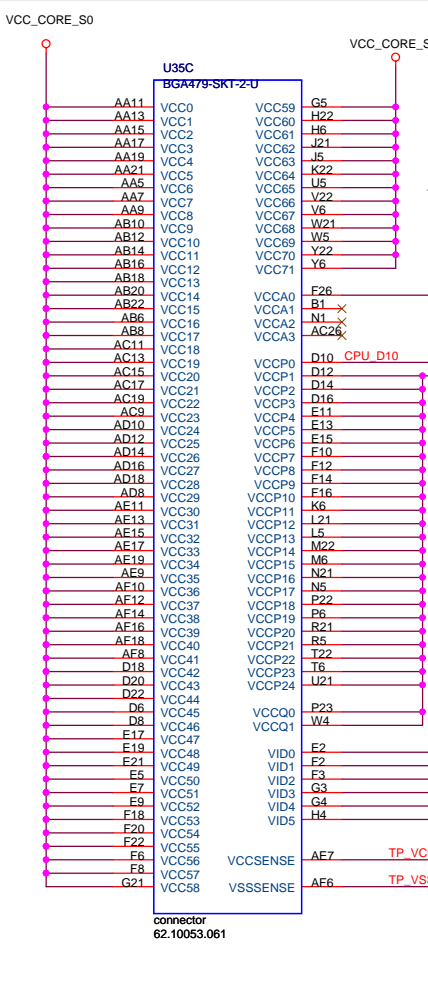


Layout Note:  
0.5" max length.

BSEL1[1:0] Freq.(MHz)	
L L	100
L H	133

BSEL1[1:0] Freq.(MHz)	
L H	100
L L	133

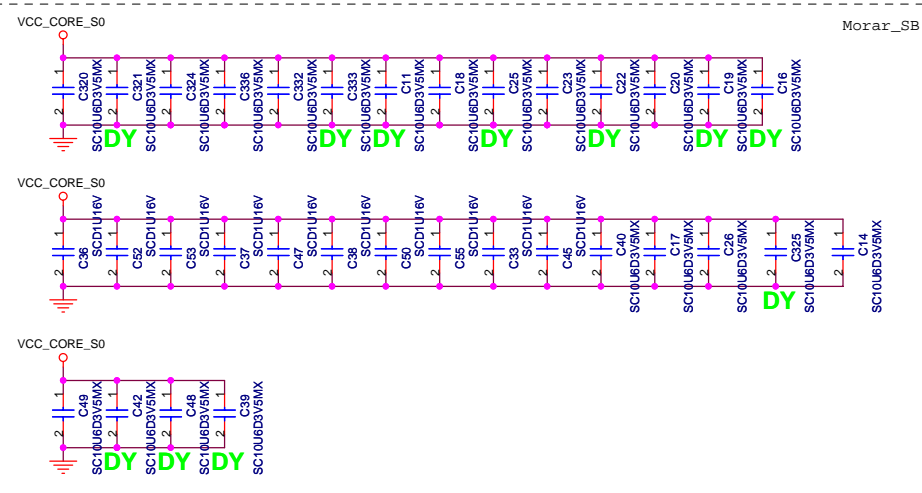
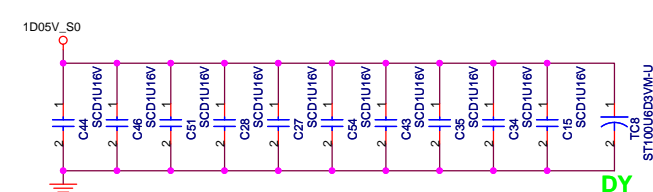
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Place these and dummy 12K7R3F for 1D8V\_VCCA\_S0

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.



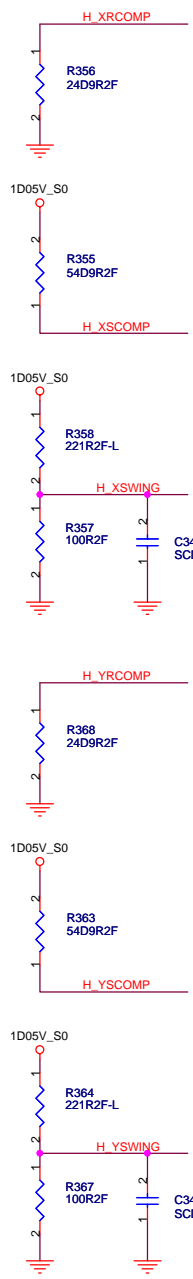
U35D	BGA479-SKT-2-U	D13
VSS0	VSS97	D13
VSS1	VSS98	D15
VSS2	VSS99	D17
VSS3	VSS100	D19
VSS4	VSS101	D21
VSS5	VSS102	D23
VSS6	VSS103	D26
VSS7	VSS104	F3
VSS8	VSS105	E8
VSS9	VSS106	E10
VSS10	VSS107	E12
VSS11	VSS108	E14
VSS12	VSS109	E16
VSS13	VSS110	E18
VSS14	VSS111	E20
VSS15	VSS112	E22
VSS16	VSS113	E25
VSS17	VSS114	F1
VSS18	VSS115	F4
VSS19	VSS116	F5
VSS20	VSS117	F7
VSS21	VSS118	F9
VSS22	VSS119	F11
VSS23	VSS120	F13
VSS24	VSS121	F15
VSS25	VSS122	F17
VSS26	VSS123	F19
VSS27	VSS124	F21
VSS28	VSS125	F24
VSS29	VSS126	G2
VSS30	VSS127	G6
VSS31	VSS128	G22
VSS32	VSS129	G23
VSS33	VSS130	G26
VSS34	VSS131	H3
VSS35	VSS132	H5
VSS36	VSS133	H21
VSS37	VSS134	H25
VSS38	VSS135	J1
VSS39	VSS136	J4
VSS40	VSS137	J6
VSS41	VSS138	J22
VSS42	VSS139	J24
VSS43	VSS140	K2
VSS44	VSS141	K5
VSS45	VSS142	K21
VSS46	VSS143	K23
VSS47	VSS144	K26
VSS48	VSS145	L3
VSS49	VSS146	L6
VSS50	VSS147	L22
VSS51	VSS148	L25
VSS52	VSS149	M1
VSS53	VSS150	M4
VSS54	VSS151	M5
VSS55	VSS152	M21
VSS56	VSS153	M24
VSS57	VSS154	N3
VSS58	VSS155	N6
VSS59	VSS156	N22
VSS60	VSS157	N23
VSS61	VSS158	N26
VSS62	VSS159	P2
VSS63	VSS160	P5
VSS64	VSS161	P21
VSS65	VSS162	P24
VSS66	VSS163	R1
VSS67	VSS164	R4
VSS68	VSS165	R6
VSS69	VSS166	R22
VSS70	VSS167	R25
VSS71	VSS168	T3
VSS72	VSS169	T5
VSS73	VSS170	T21
VSS74	VSS171	T23
VSS75	VSS172	T26
VSS76	VSS173	U2
VSS77	VSS174	U6
VSS78	VSS175	U22
VSS79	VSS176	U24
VSS80	VSS177	V1
VSS81	VSS178	V4
VSS82	VSS179	V5
VSS83	VSS180	V21
VSS84	VSS181	V25
VSS85	VSS182	W2
VSS86	VSS183	W6
VSS87	VSS184	W22
VSS88	VSS185	W23
VSS89	VSS186	W26
VSS90	VSS187	Y2
VSS91	VSS188	Y5
VSS92	VSS189	Y21
VSS93	VSS190	Y24
VSS94	VSS191	
VSS95		
VSS96		

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Title: **CPU (2 of 2)**

Size: A3 Document Number: **MORAR** Rev: **SB**

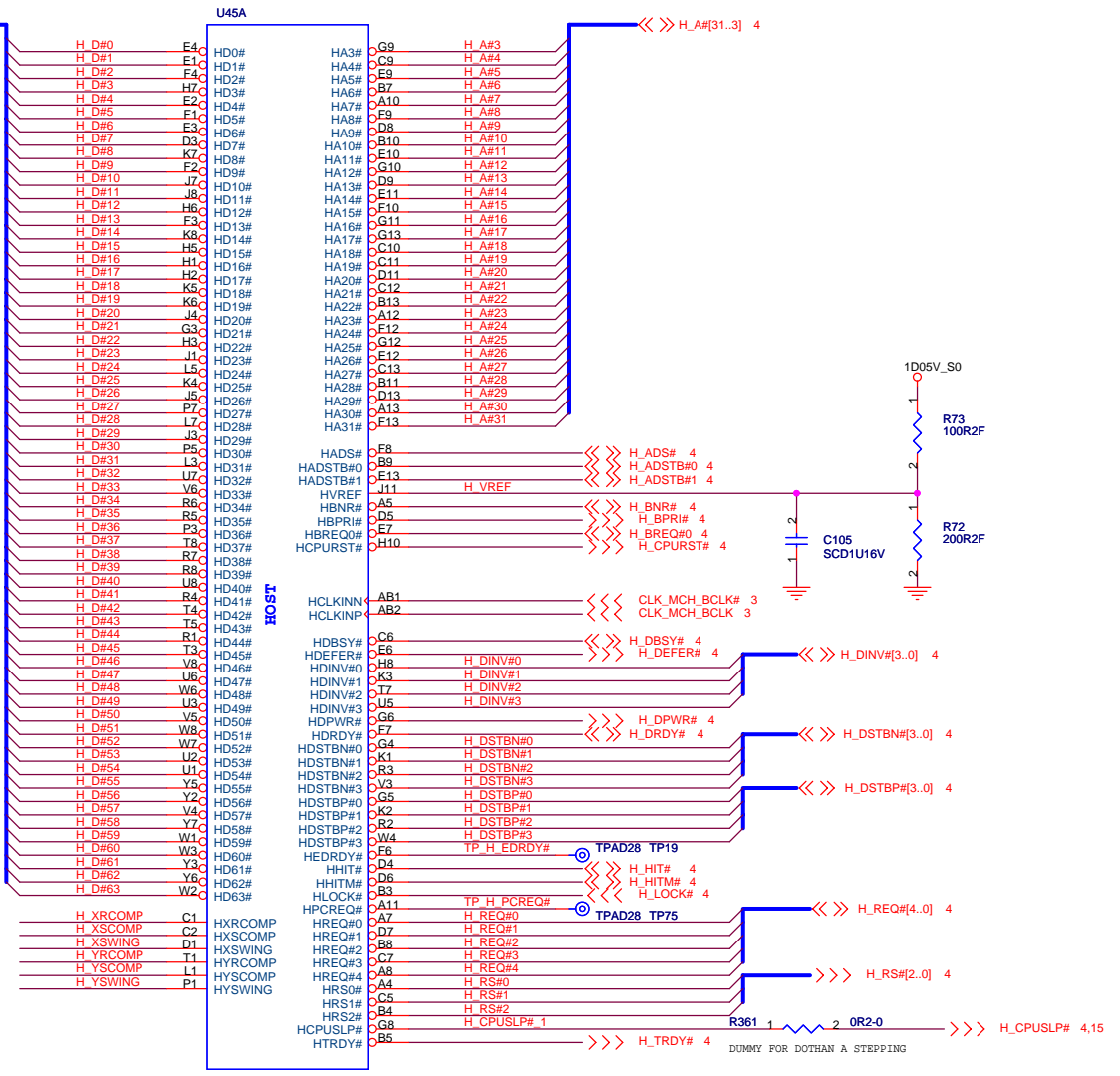
Date: Thursday, May 26, 2005 Sheet 5 of 40



Place them near to the chip

4 H\_D#[63.0]

4 H\_A#[31..3]



71.0GMCH.08U

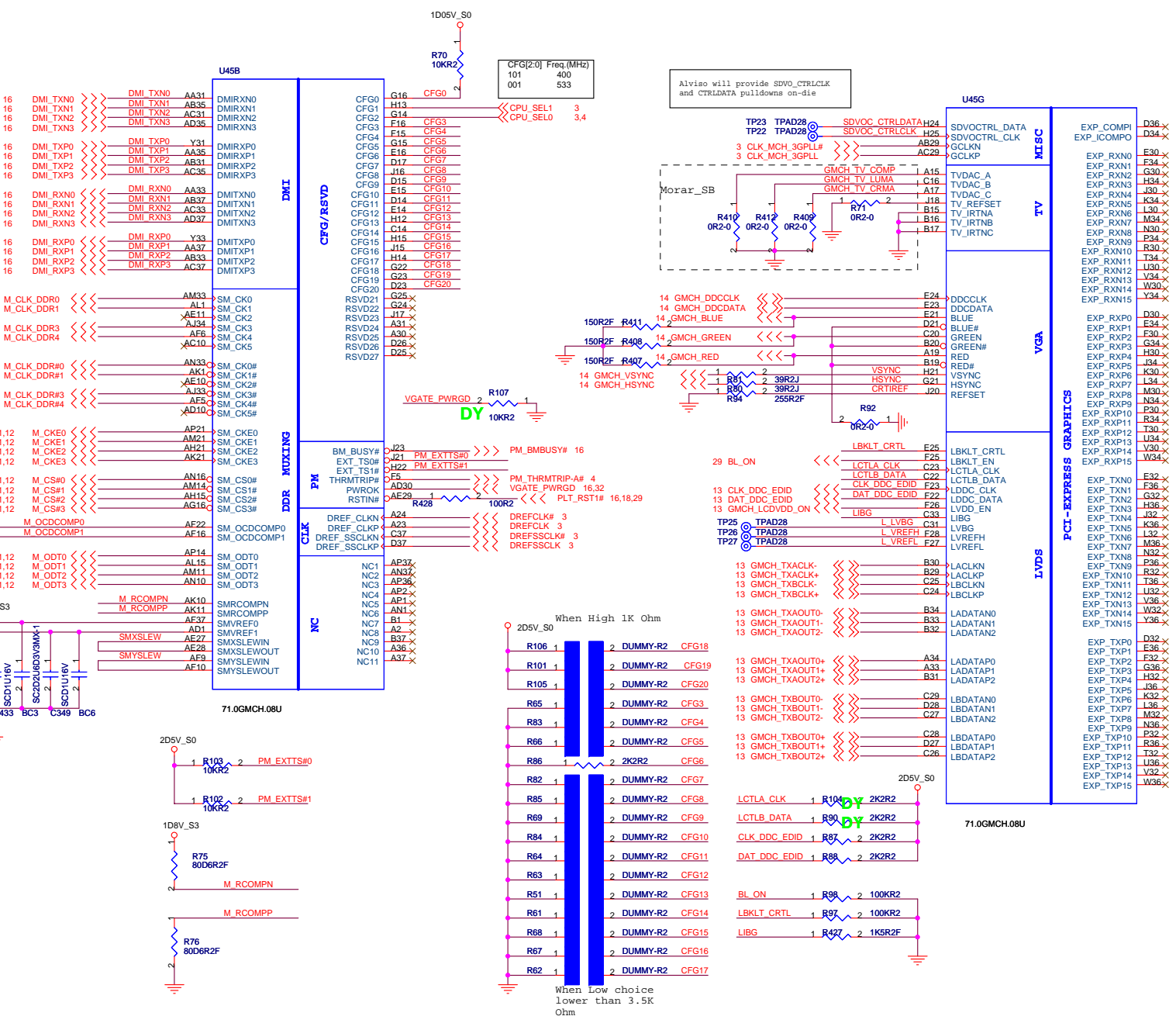
<Core Design>

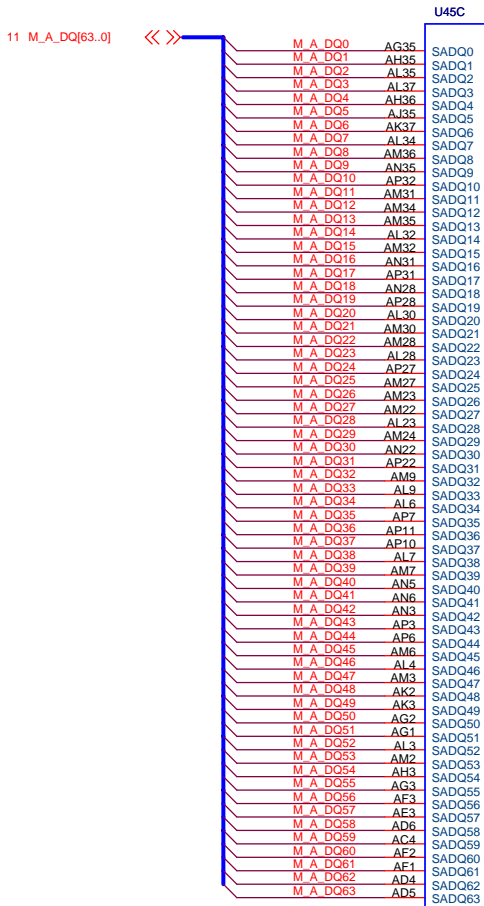
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Title: **GMCH (1 of 5)**

Size: A3	Document Number: MORAR	Rev: SB
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Date: Friday, June 24, 2005 Sheet 6 of 40

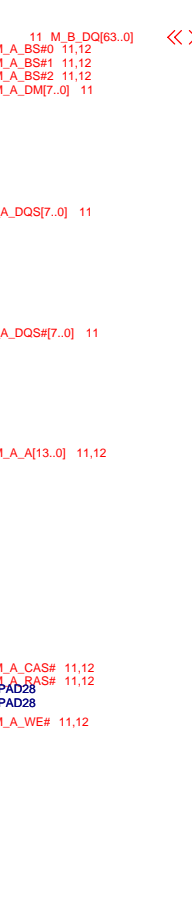




71.0GMCH.08U

DDR SYSTEM MEMORY A

Place Test PAD Near to Chip as could as possible



71.0GMCH.08U

DDR SYSTEM MEMORY B

Place Test PAD Near to Chip as could as possible

<Core Design>

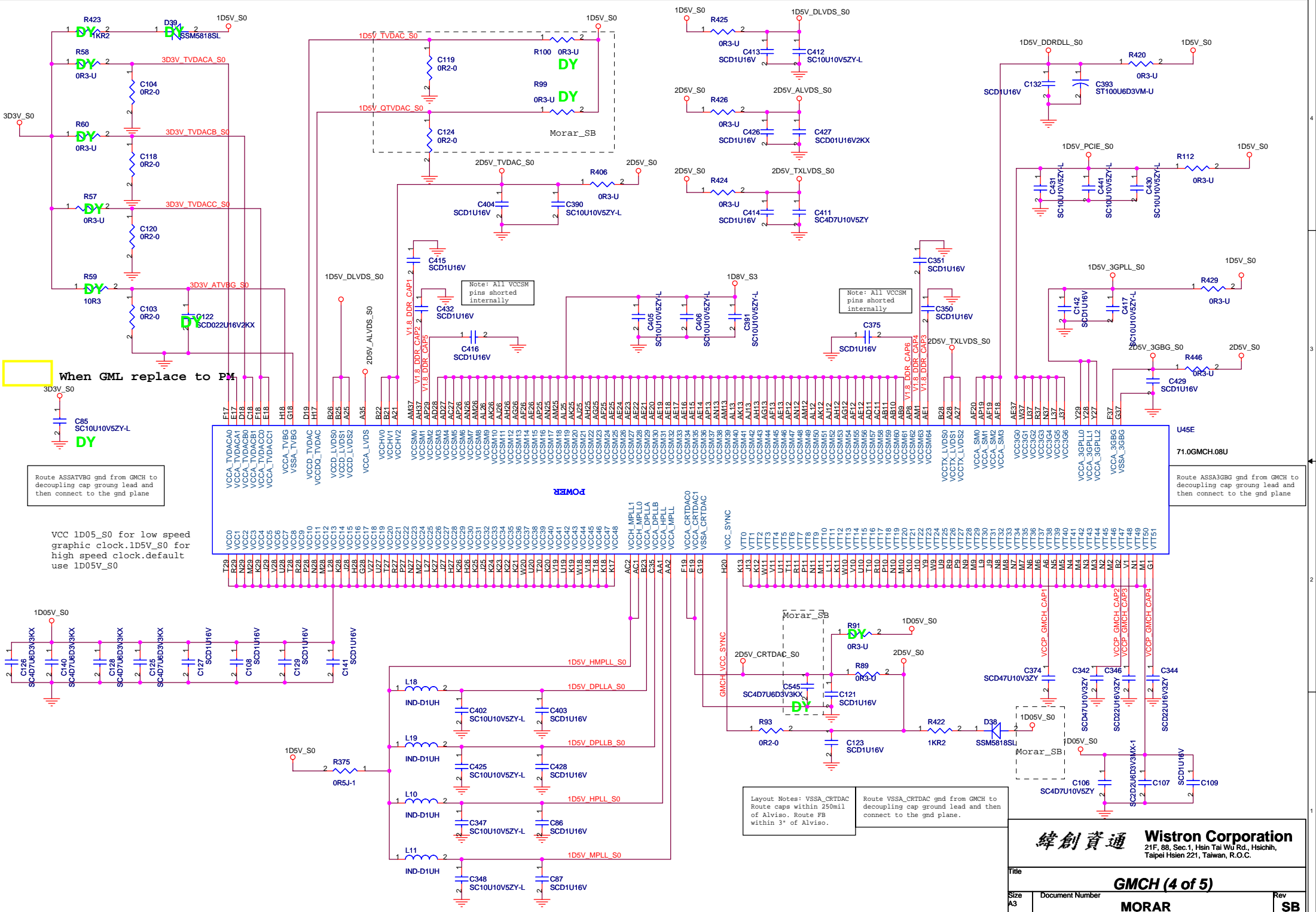
**緯創資通** Wistron Corporation  
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Title: **GMCH (3 of 5)**

Size A3	Document Number	Rev
	<b>MORAR</b>	<b>SB</b>

Date: Friday, June 24, 2005 Sheet 8 of 40

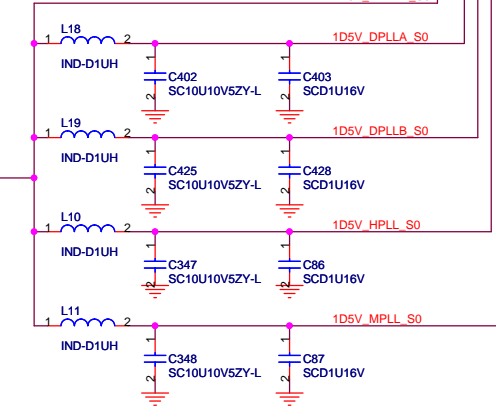
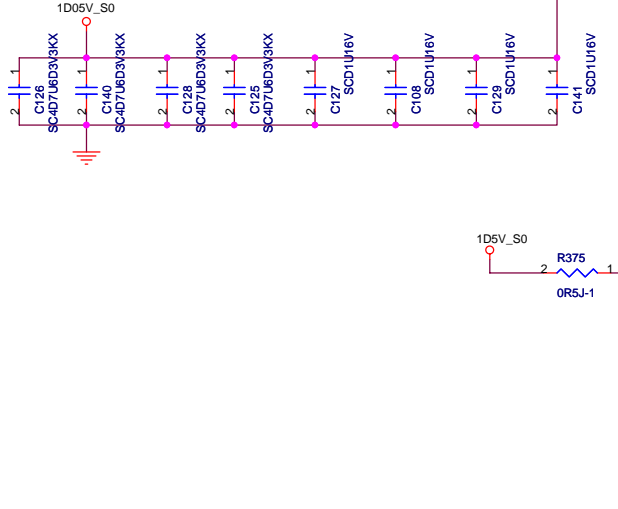




When GML replace to PM  
 3D3V\_S0  
 C85  
 SC10U10V5ZY-L  
 DY

Route ASSA3ATVBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane

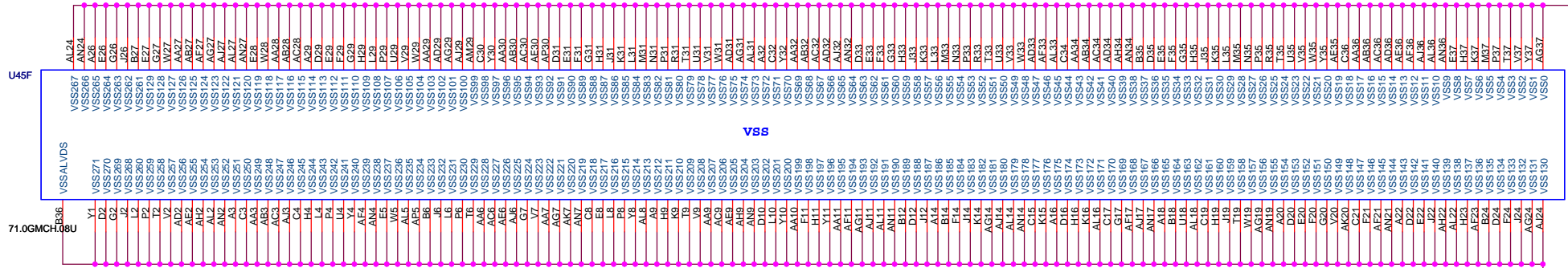
VCC 1D05\_S0 for low speed graphic clock. 1D5V\_S0 for high speed clock. default use 1D05V\_S0



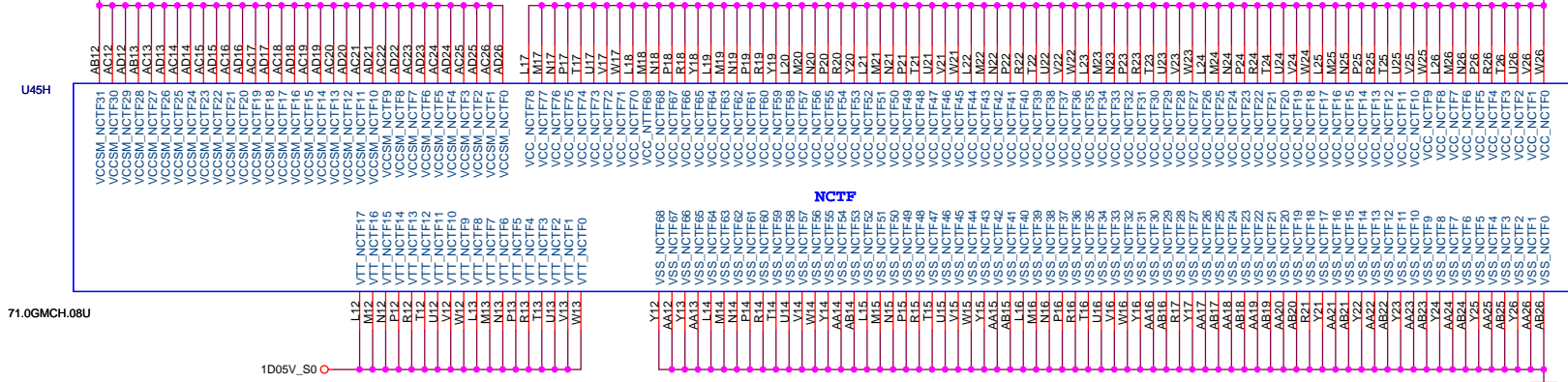
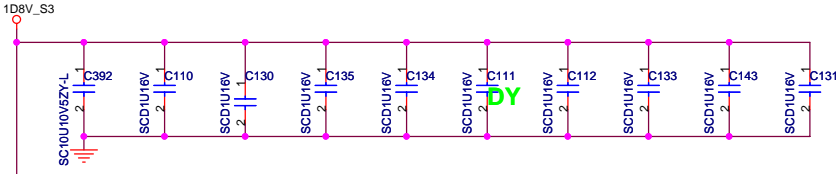
Layout Notes: VSSA\_CRTDAC  
 Route caps within 25mm1 of Alviso. Route FB within 3" of Alviso.

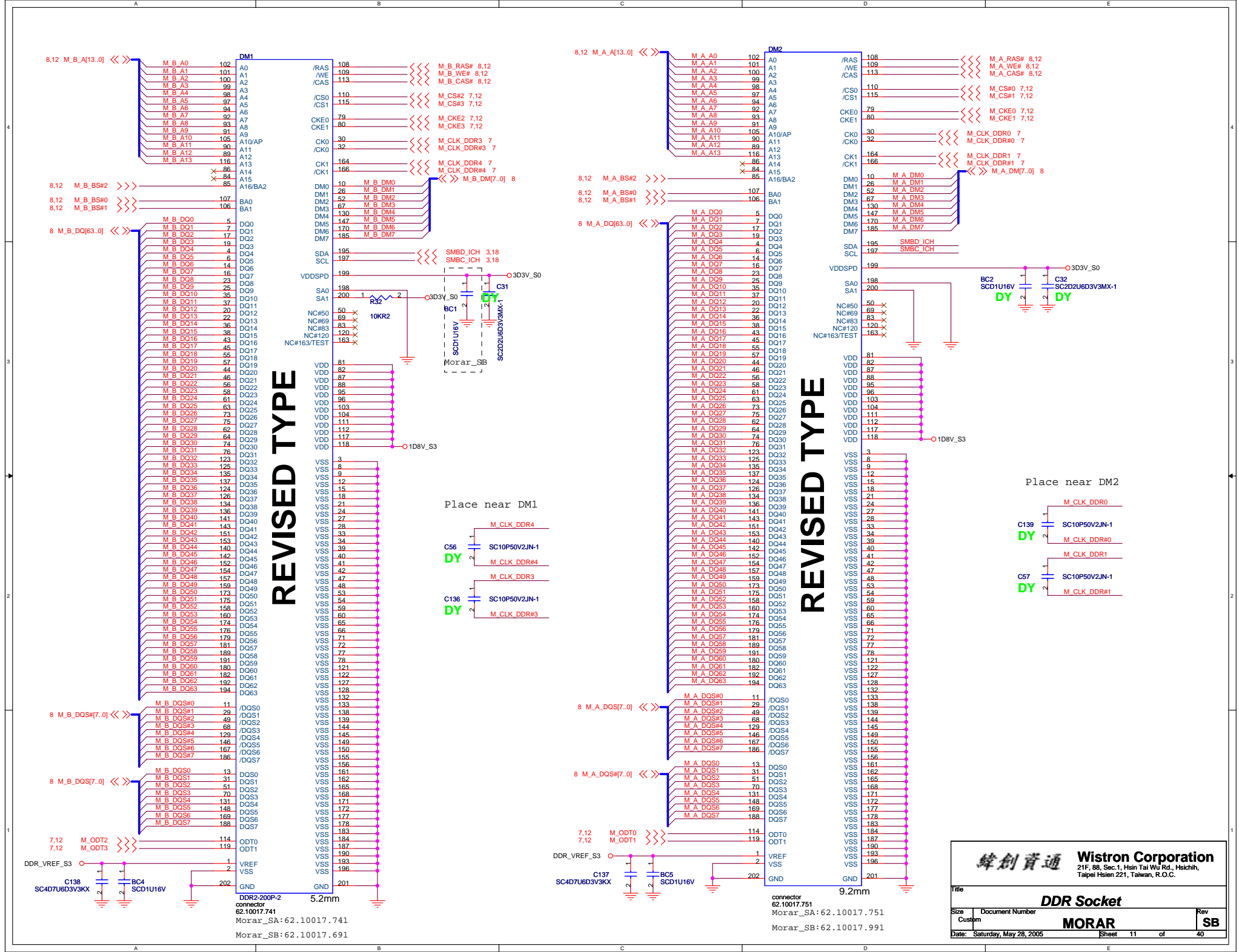
Route VSSA\_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

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Place these Hi-Freq decoupling caps near GMCH





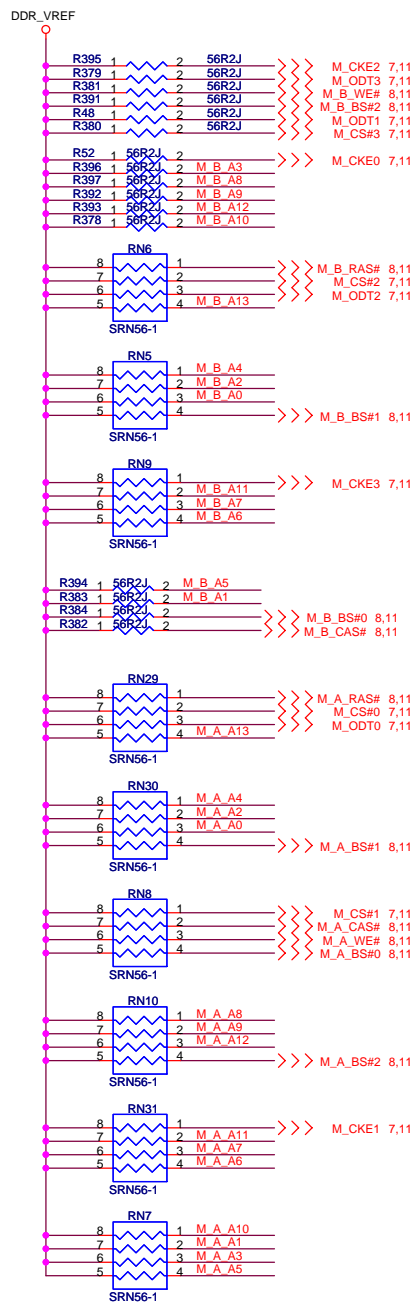
**緯創資通** **Wistron Corporation**  
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**DDR Socket**

File	Document Number	Rev
Size	Custpm	SB
Date: Saturday, May 28, 2005	<b>MORAR</b>	Sheet 11 of 40

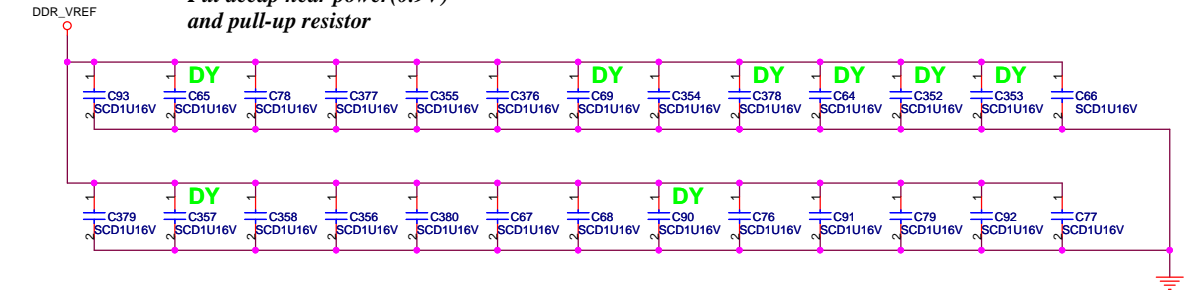
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

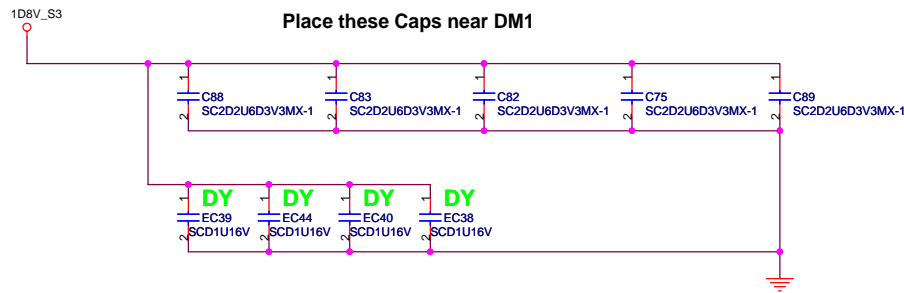


# Decoupling Capacitor

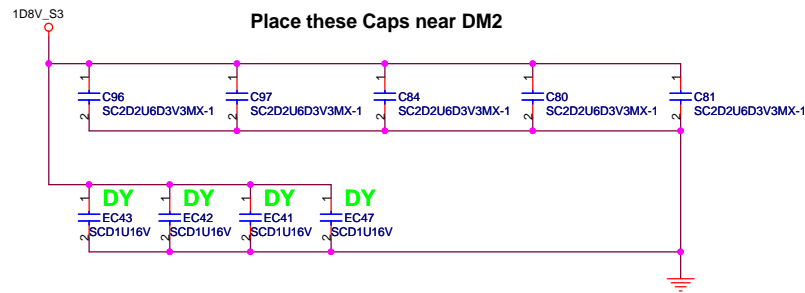
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



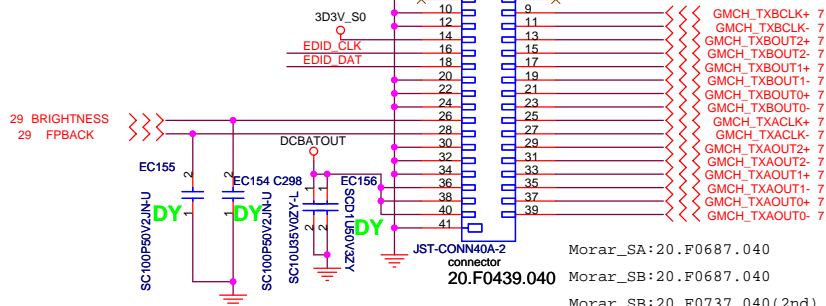
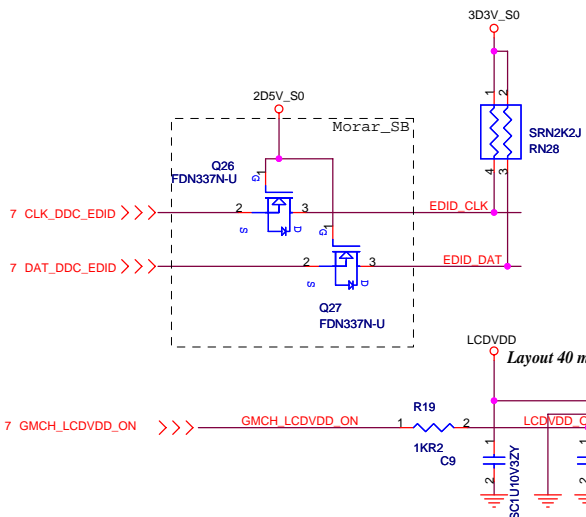
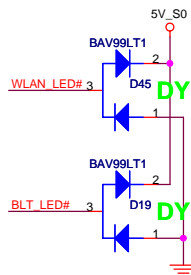
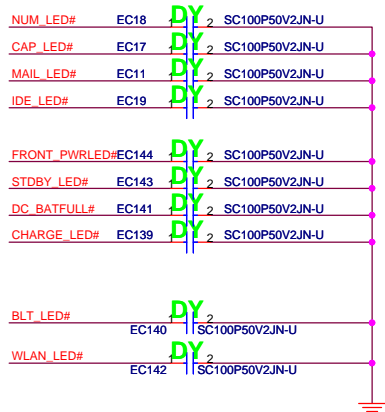
Place these Caps near DM2



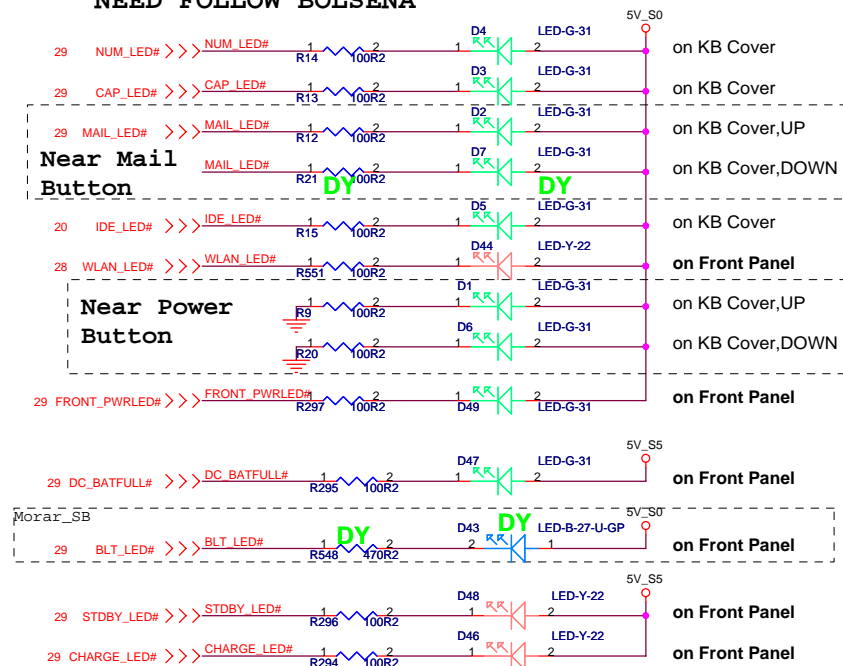
緯創資通 Wistron Corporation  
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Title		DDR2 Termination Resistor	
Size	A3	Document Number	MORAR
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Rev	SB		

# LED



# NEED FOLLOW BOLSENA



## on KB cover

LED	V	V	V	V	V	V
Button	V	V	V	V	V	V
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS
						NUM
						HDD

## Front panel

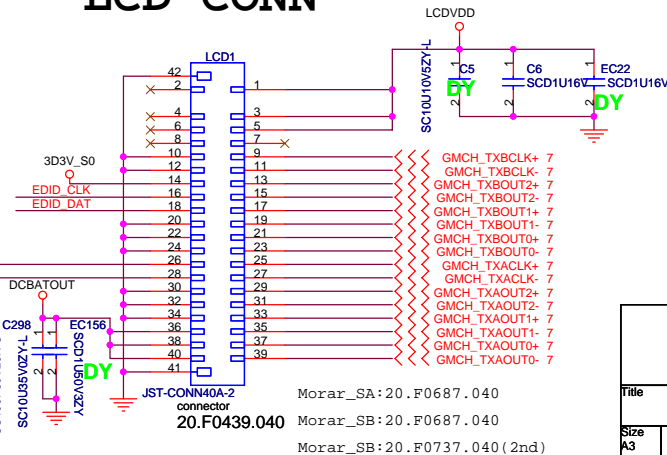
LED	V	V	V	V
Button	V	V	V	V
	Bluetooth	Wireless	Charger	Power2

Charger:  
Green : DC only or Battery full with DC  
Orange : Charging  
Orange Blink : Battery low

Power2:  
Green : S0  
Orange : S3  
Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

# LCD CONN

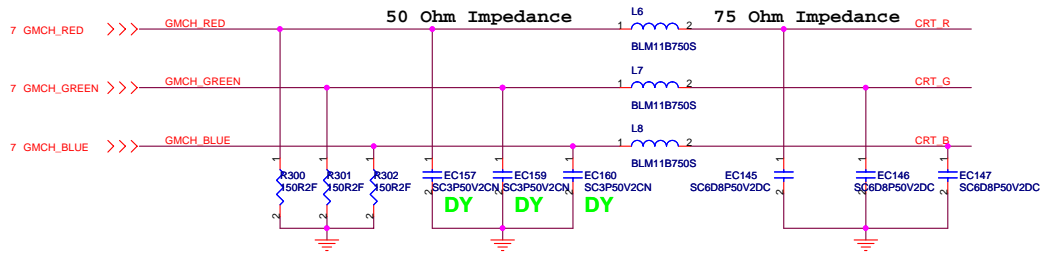


**緯創資通** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

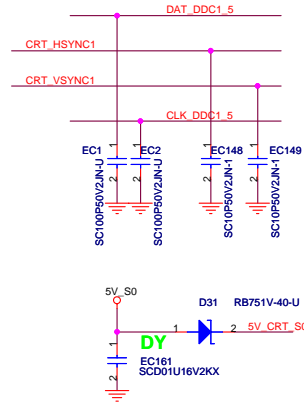
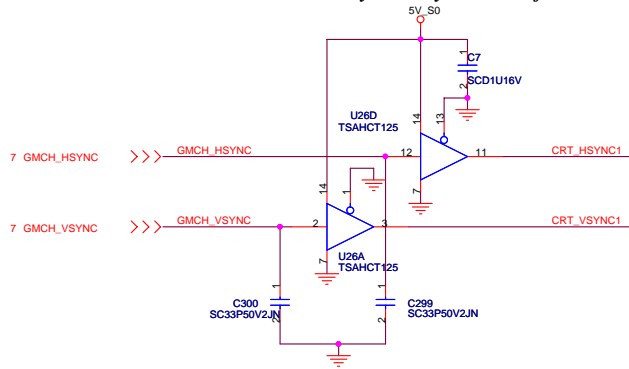
Title		
<b>LCD CONN &amp; LED</b>		
Size	Document Number	Rev
A3	<b>MORAR</b>	<b>SB</b>
Date: Saturday, May 28, 2005		
Sheet		of
13		40

# CRT CONNECTOR

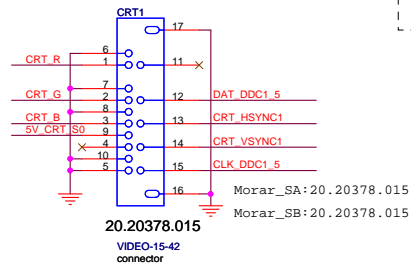
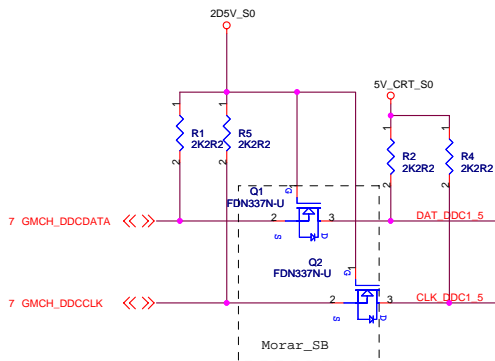
Ferrite bead impedance: 75ohm@100MHz



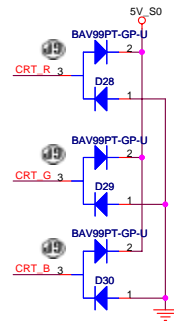
## Hsync & Vsync level shift




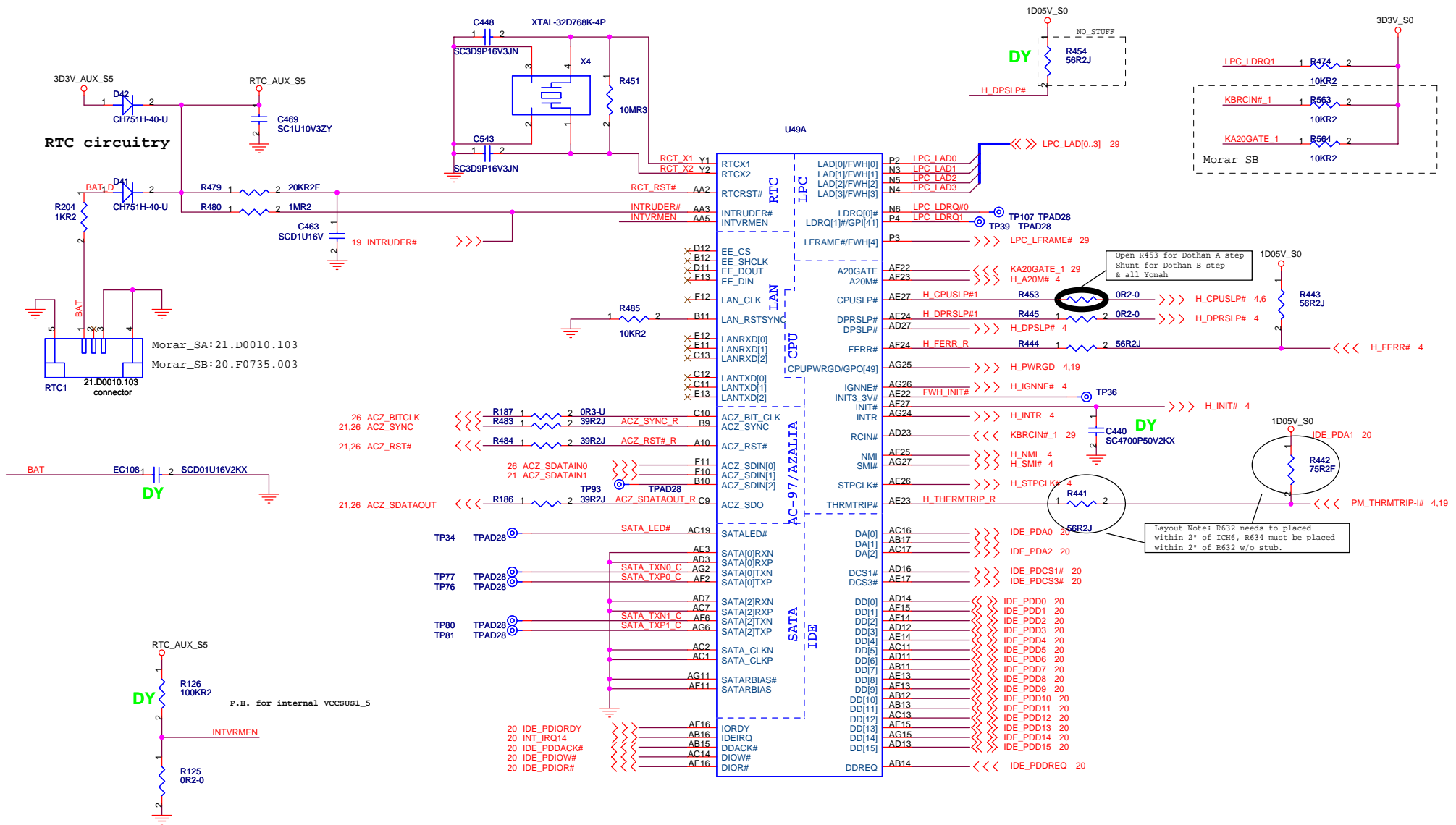
## DDC\_CLK & DATA level shift

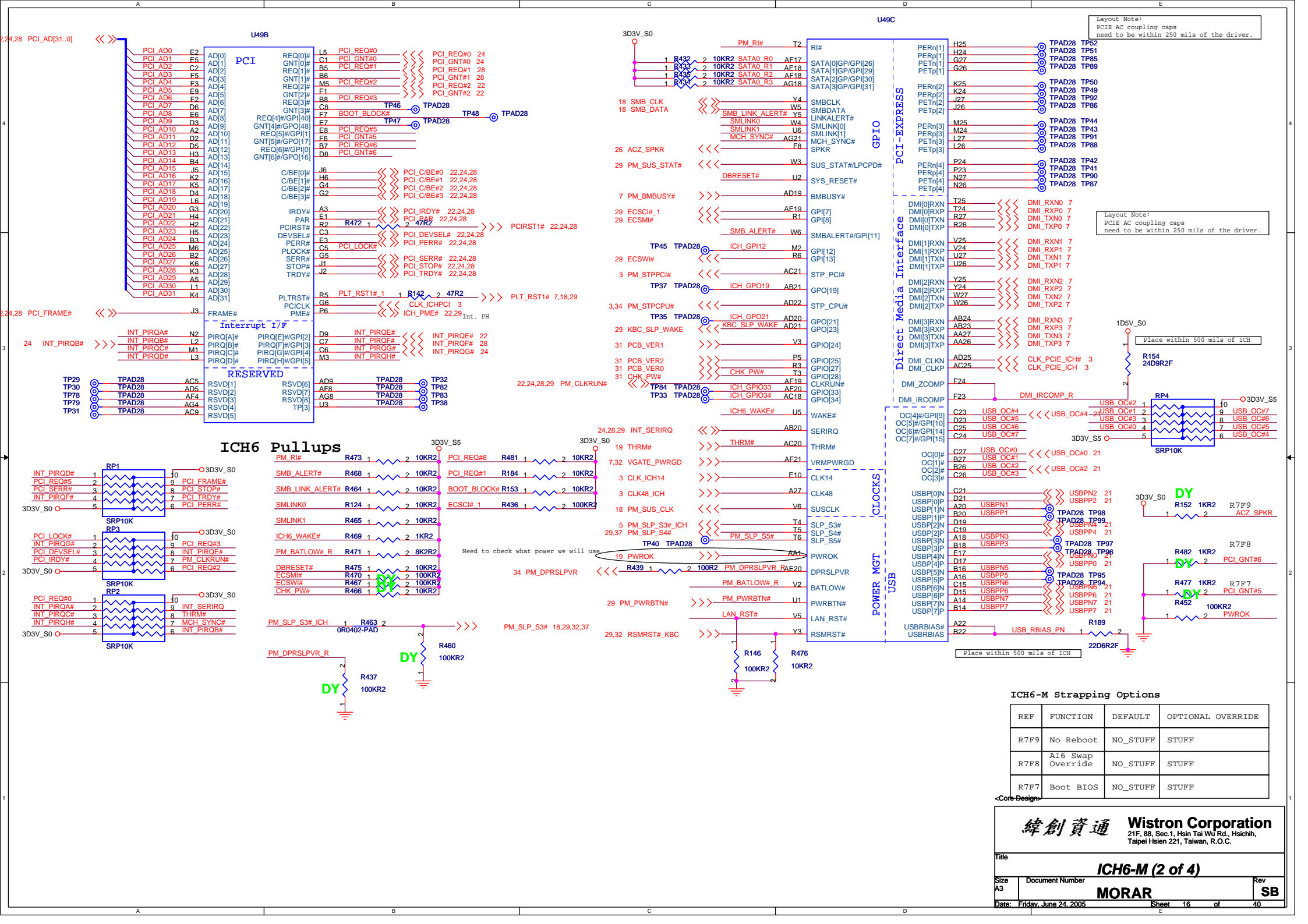


## ESD Protection Diode



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<b>Title</b> <b>CRT Connector</b>	
<b>Size</b> Custom	<b>Document Number</b> <b>MORAR</b>
<b>Date:</b> Saturday, May 28, 2005	<b>Rev</b> <b>SB</b>
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Layout Note:  
PCI AC coupling caps  
need to be within 250 mils of the driver.

Layout Note:  
PCI AC coupling caps  
need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500 mils of ICH

**ICH6-M Strapping Options**

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

<Core Design>

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Title: **ICH6-M (2 of 4)**

Size A3 Document Number **MORAR** Rev **SB**

Date: Friday, June 24, 2005 Sheet 16 of 40



Layout Note:  
Place above caps within  
100 mils of ICH near F27, P27, AB27

Layout Note:  
IDE decoupling

Layout Note:  
PCI decoupling

Place within 100  
mils of ICH  
near pin AG5

Place within 100  
mils of ICH  
near pin AG9

Place within 100  
mils of ICH

Place within 100  
mils of ICH  
near E26, E27

Place within 100  
mils of ICH  
pin AB1

Place within 100  
mils of ICH  
pin AG10

Place within 100  
mils of ICH  
pin A13

Place within 100  
mils of ICH  
pin V7

Layout Note:  
Place near pin AA19

ALL NO\_STUFF Caps do  
not have layout  
requirements but if  
layout allows then place  
next to ICH6

\*Within a given well, 5VREF needs to be up before the  
corresponding 3.3V rail

Layout Note:  
Place near ICH6

Place within 100  
mils of ICH

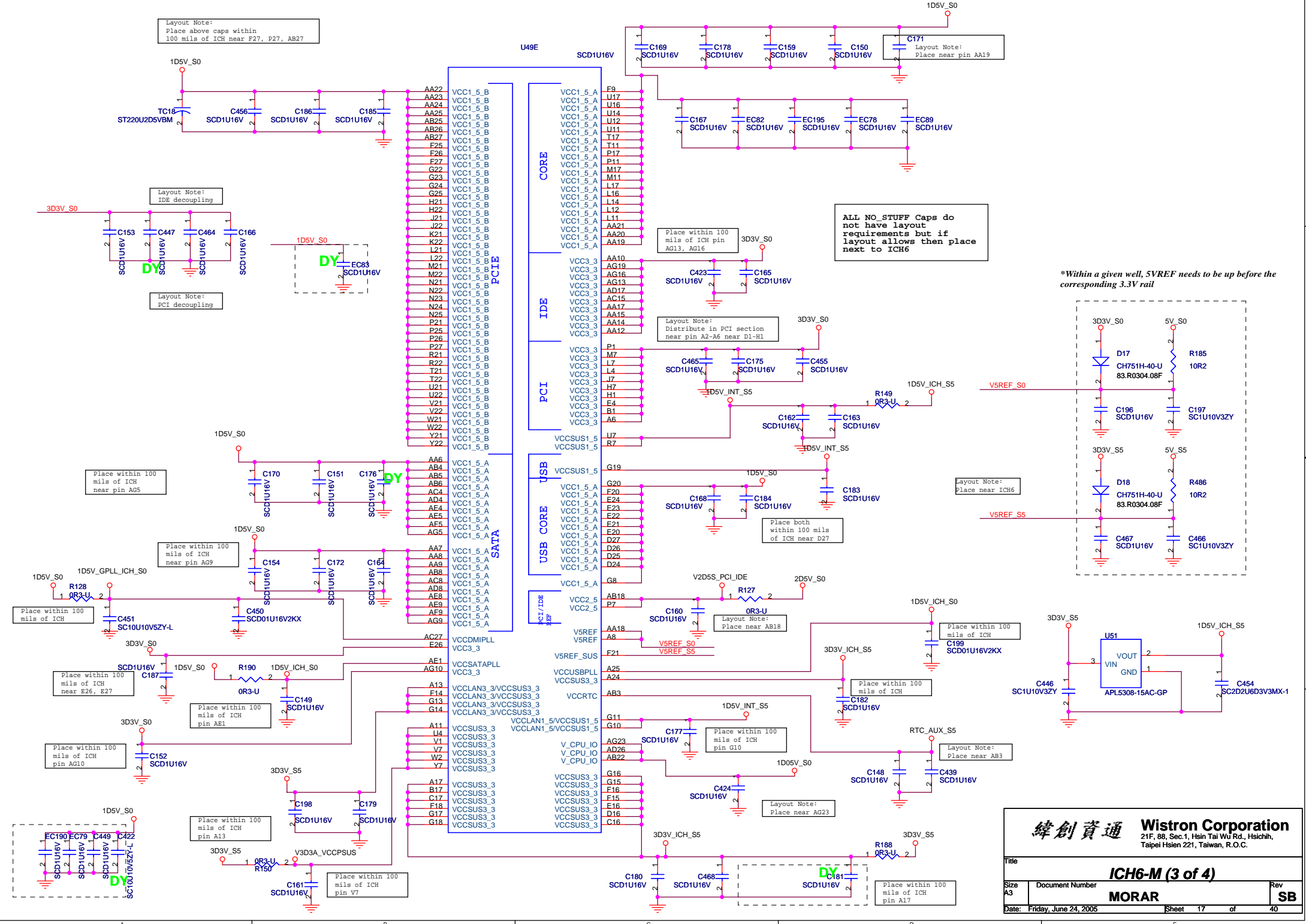
Layout Note:  
Place near AB3

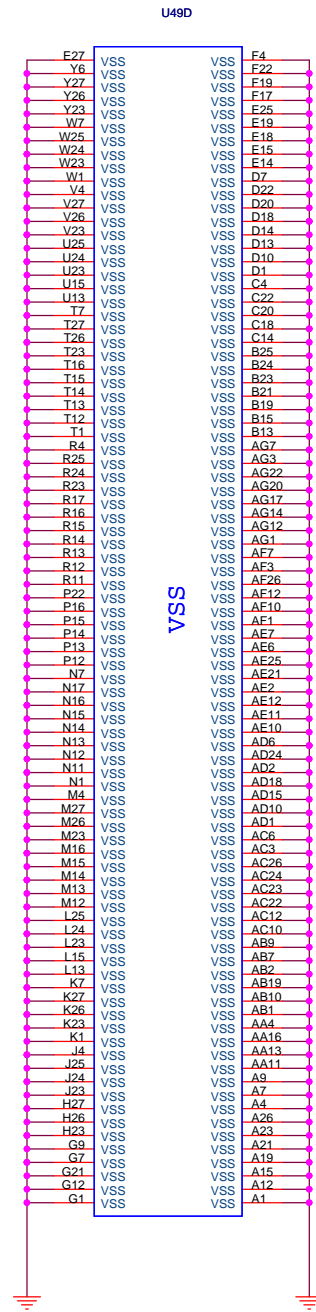
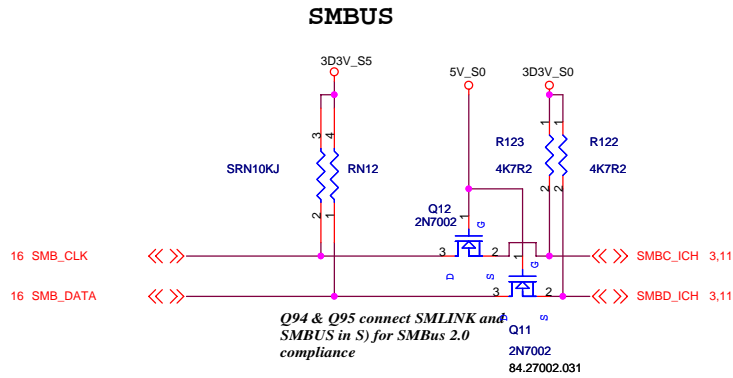
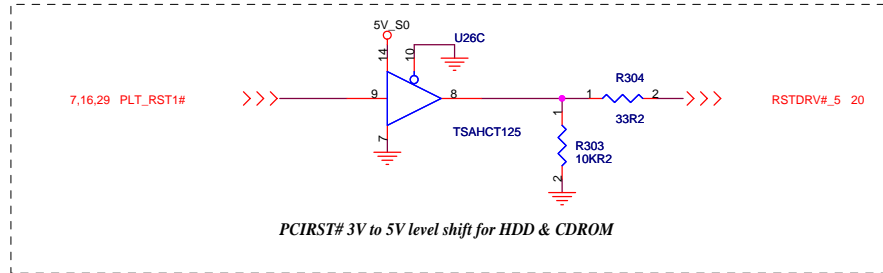
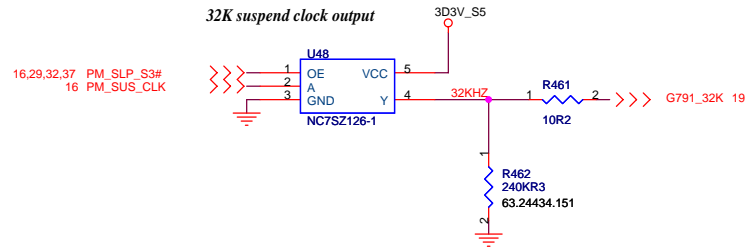
Layout Note:  
Place near AG23

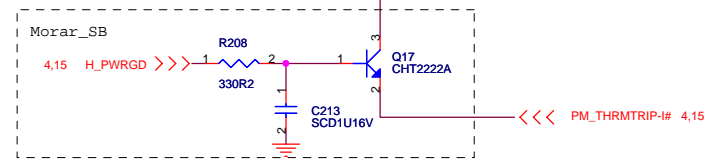
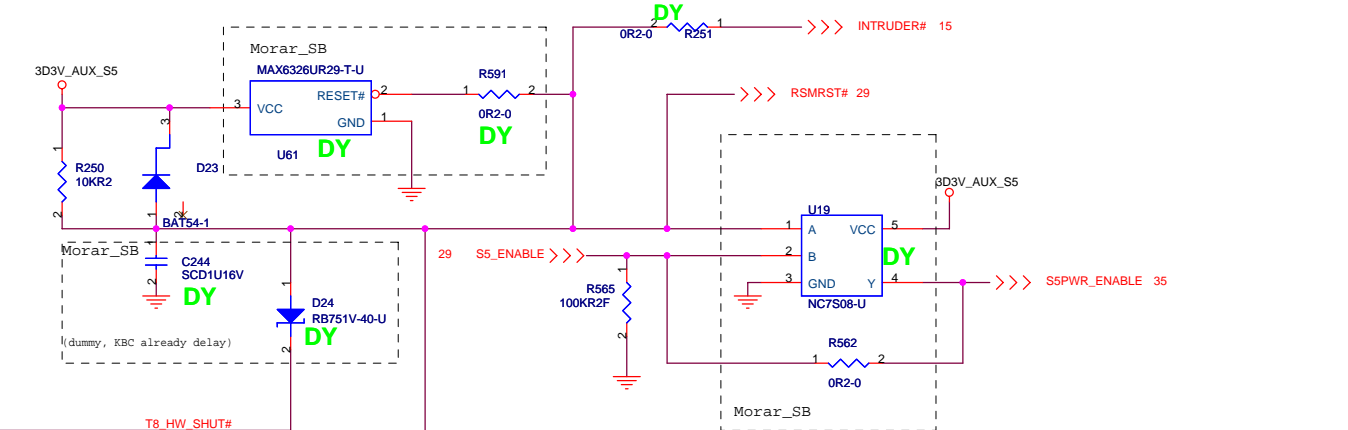
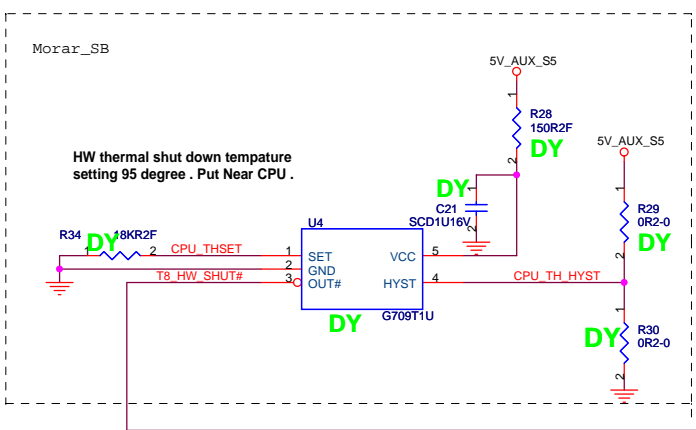
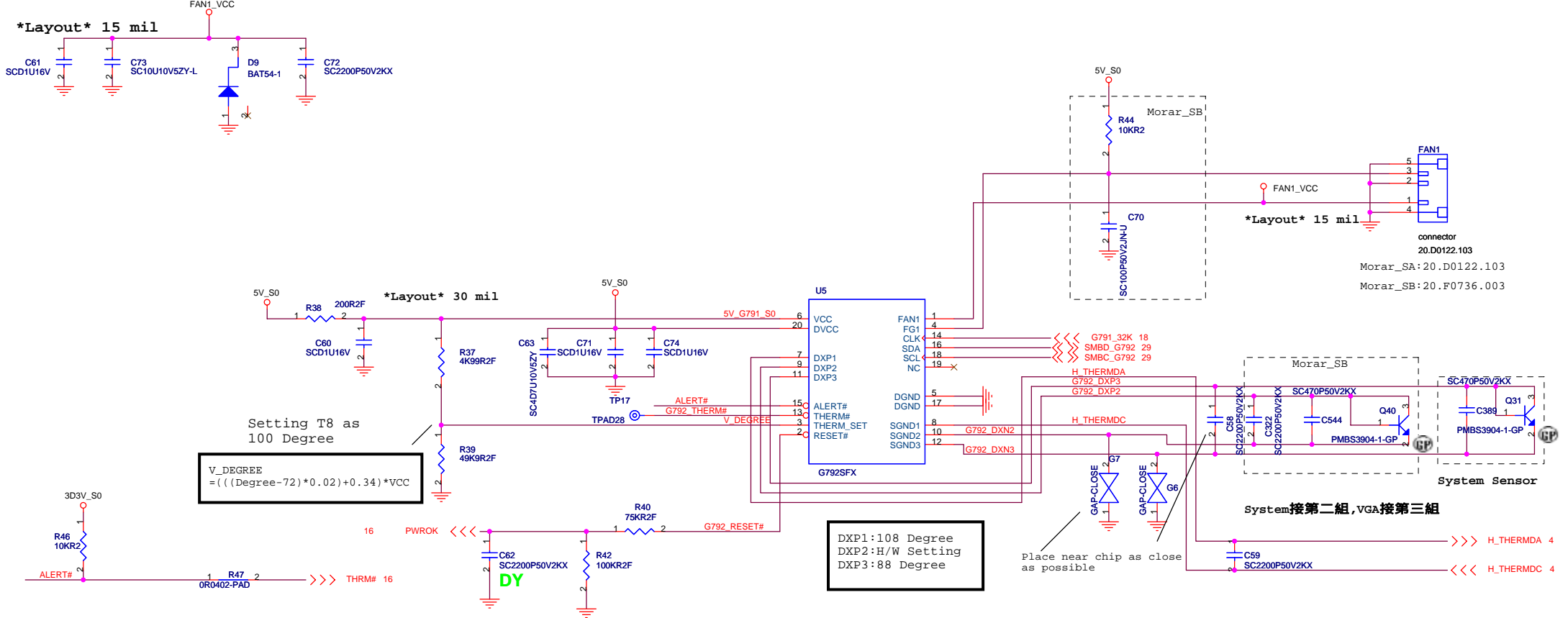
Place within 100  
mils of ICH  
pin A17

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>ICH6-M (3 of 4)</b>			
Size	Document Number	Rev	
A3	<b>MORAR</b>	SB	
Date: Friday, June 24, 2005	Sheet 17	of 40	

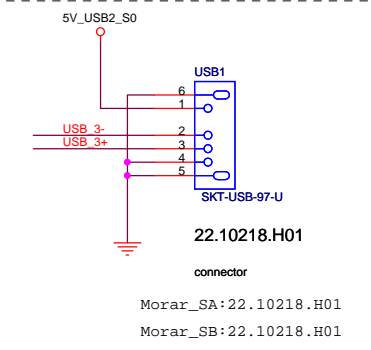
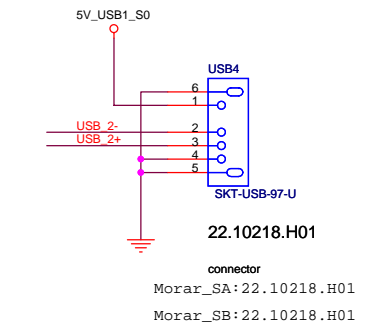
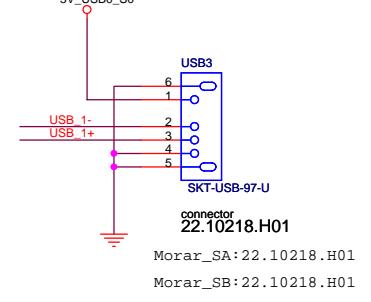
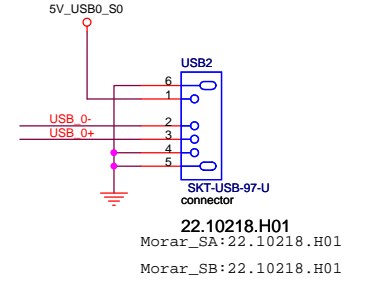
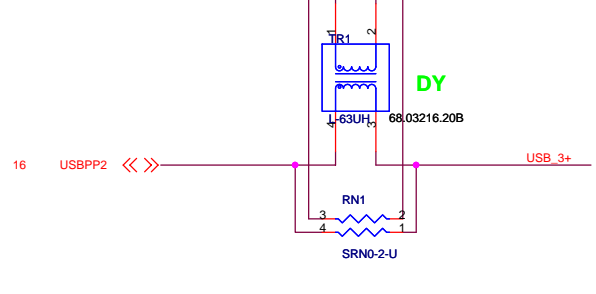
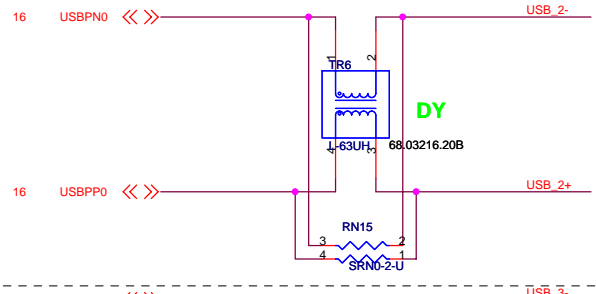
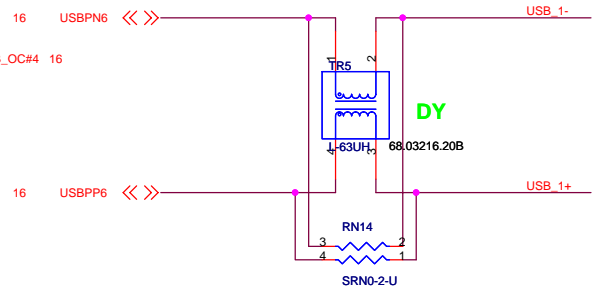
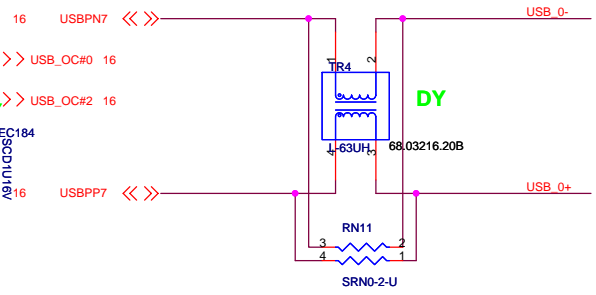
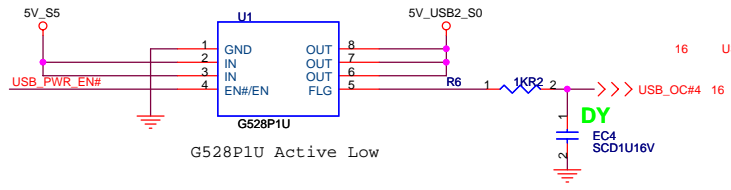
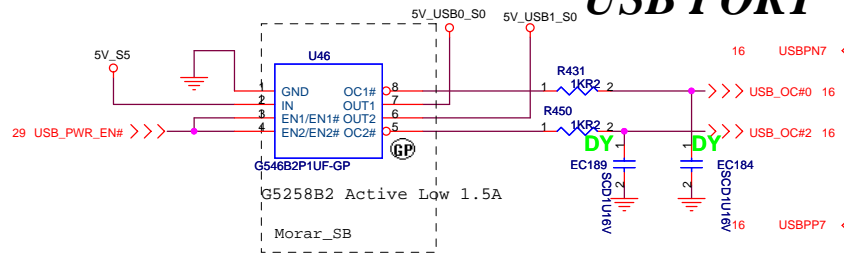
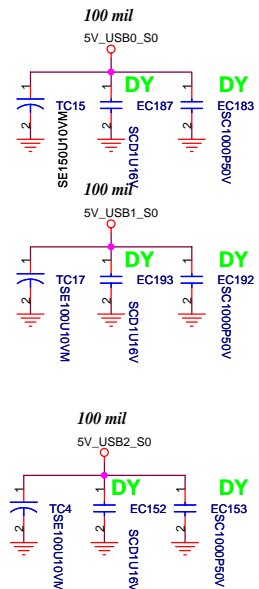




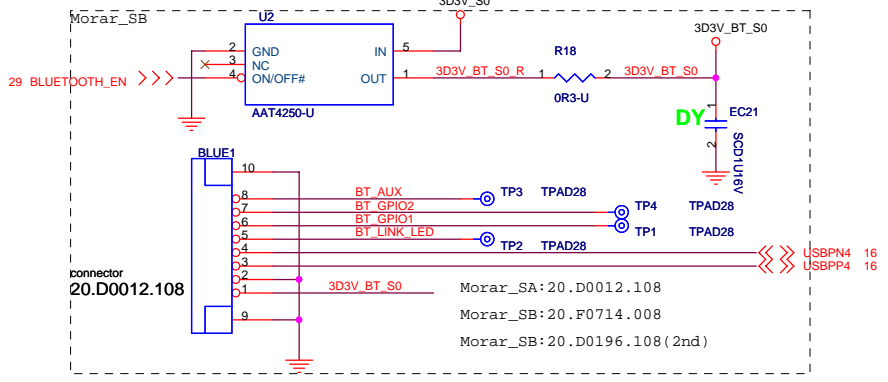




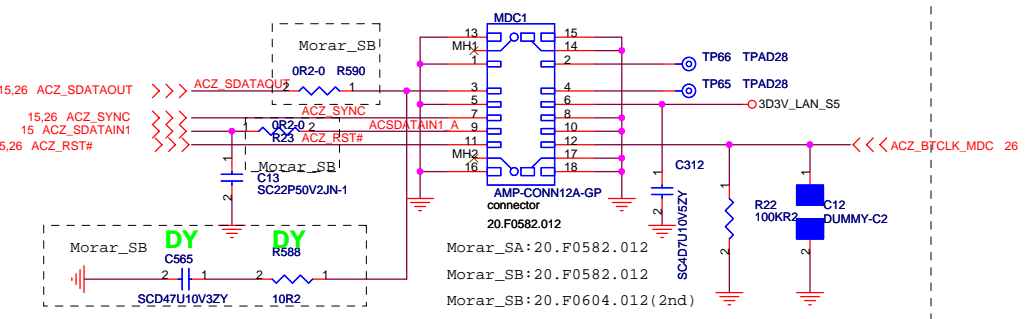
# USB PORT



# BLUETOOTH MODULE

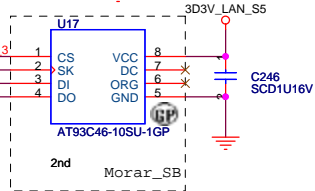
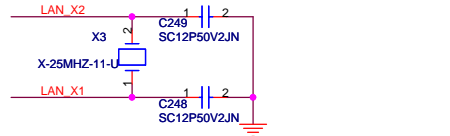
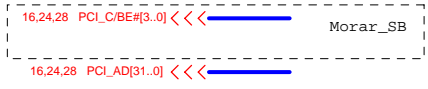
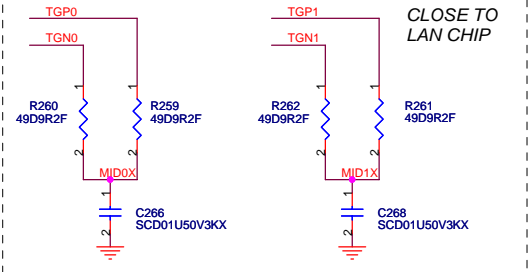


# MDC 1.5 CONNECTOR

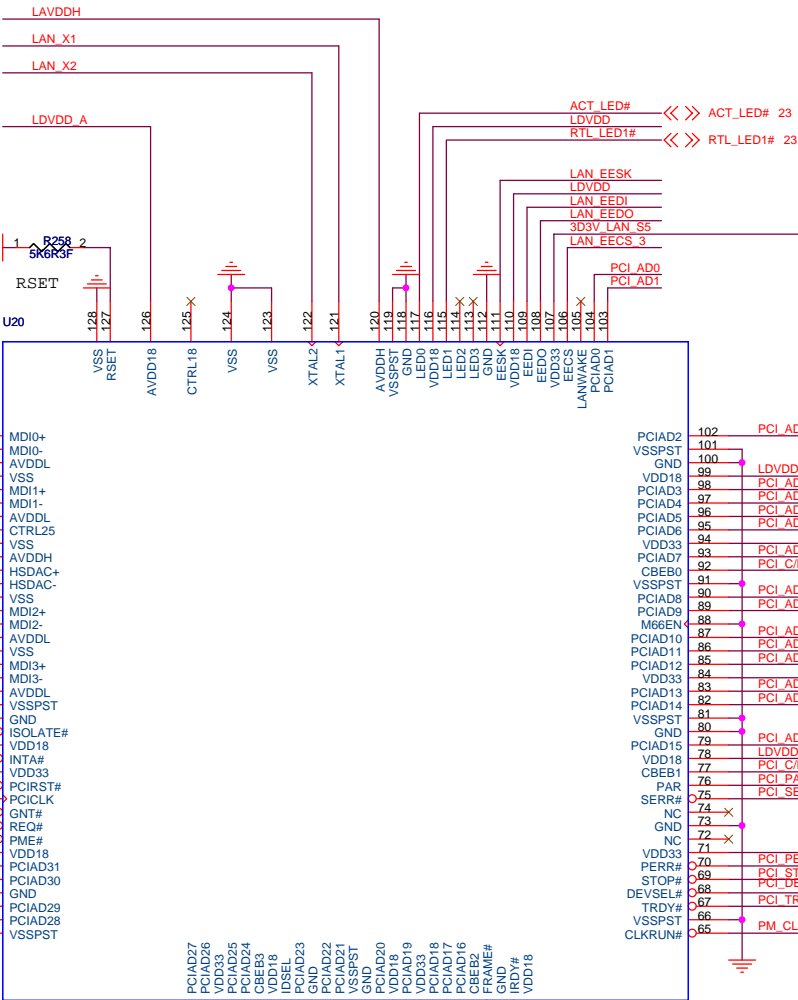


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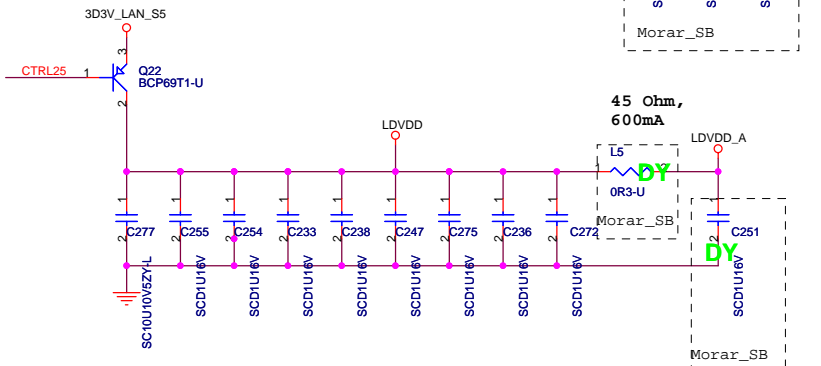
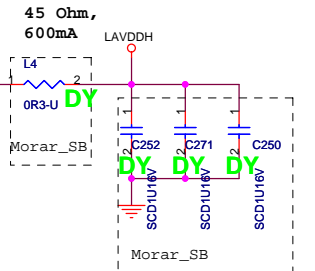
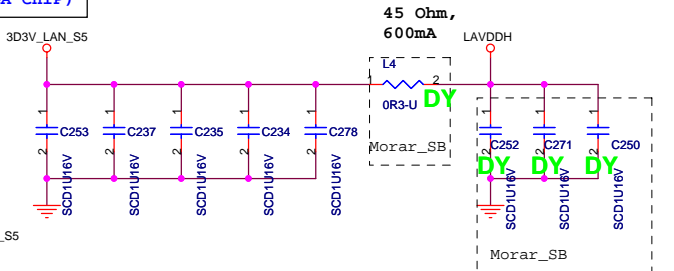
<b>USB / MDC / BLUETOOTH</b>		
Size A3	Document Number <b>MORAR</b>	Rev <b>SB</b>
Date: Saturday, May 28, 2005		
Sheet	21	of 40



EEPROM LED OPTION USE '01'  
(DEFINED IN SPEC)  
=> LED0 : ACT  
=> LED1 : LINK  
(BOTH 10/100 AND GIGA CHIP)



3D3V\_LAN\_S5



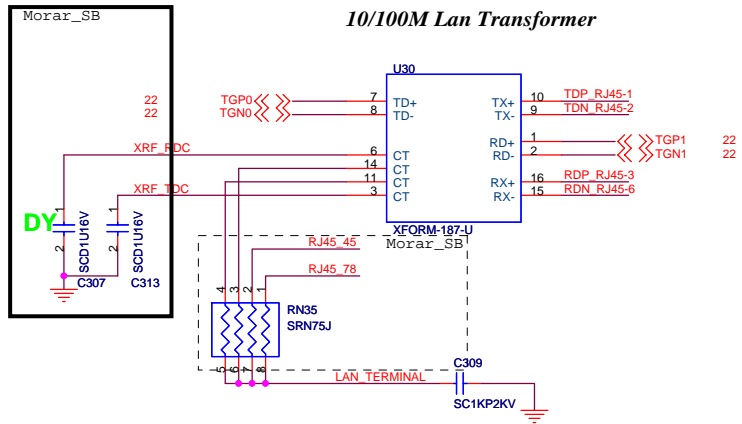
GIGALAN: RTL810SBL  
10/100 LAN: RTL810C

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8100CL**

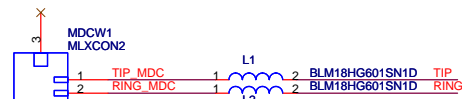
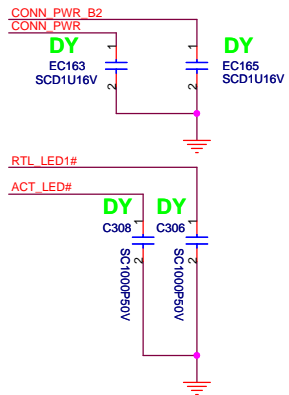
Size: A3 Document Number: **MORAR** Rev: **SB**

Date: Saturday, May 28, 2005 Sheet: 22 of 40

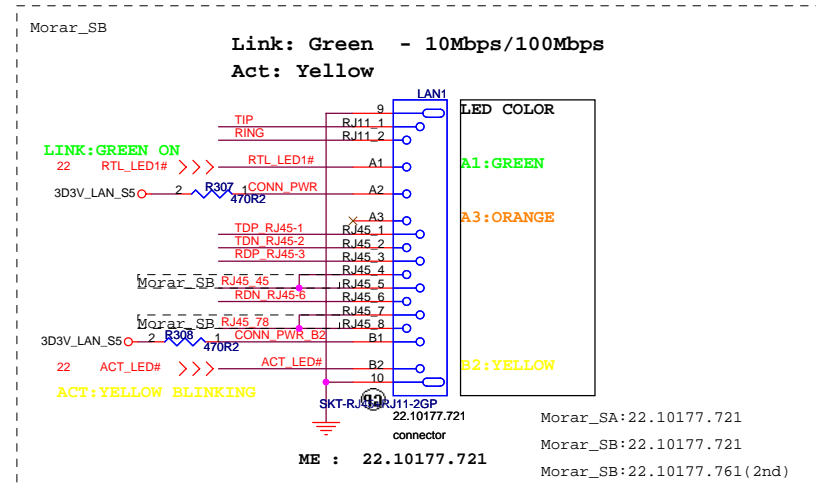


10/100M Lan Transformer

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

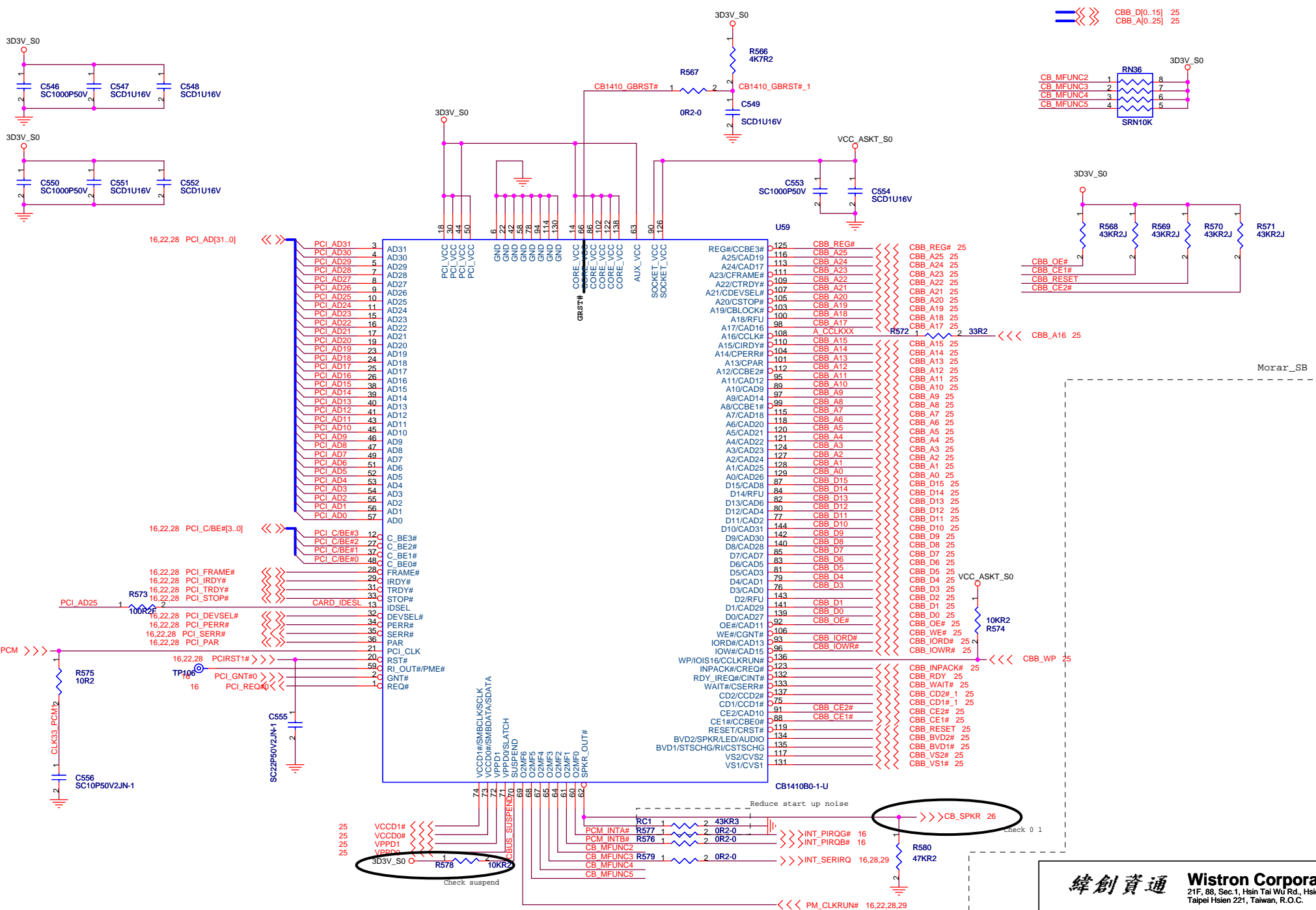


21.D0010.102  
connector  
Morar\_SA:21.D0010.102  
Morar\_SB:20.F0714.002  
Morar\_SB:20.D0196.102(2nd)



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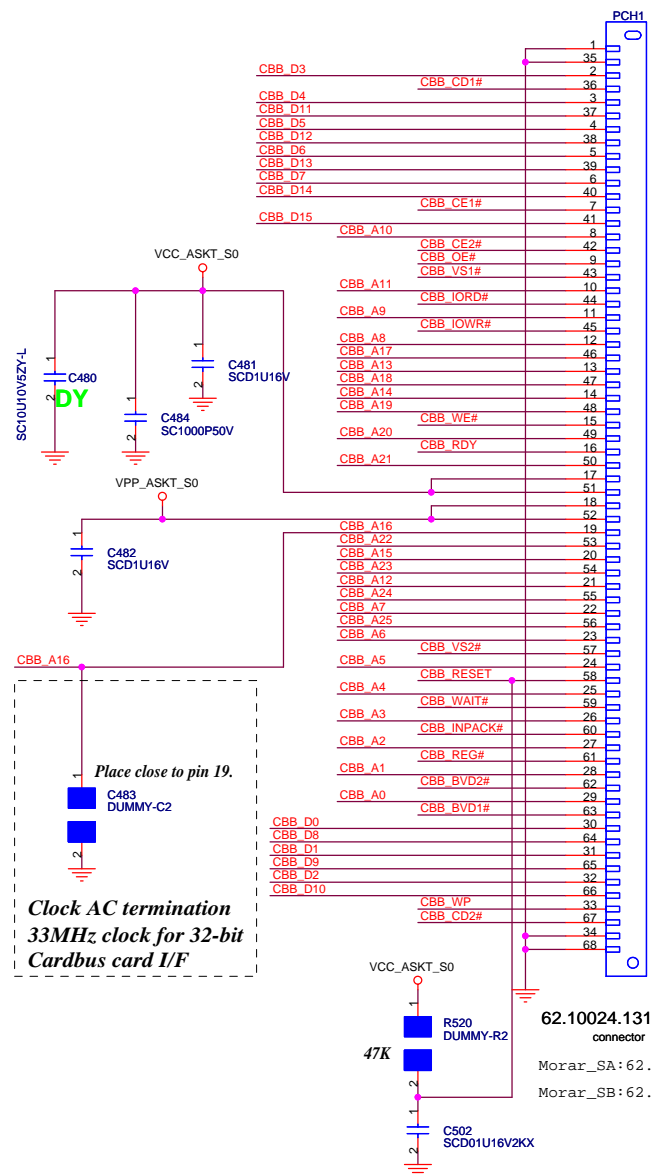
Title: LAN CONN  
Size: A3 Document Number: MORAR Rev: SB  
Date: Saturday, May 28, 2005 Sheet: 23 of 40



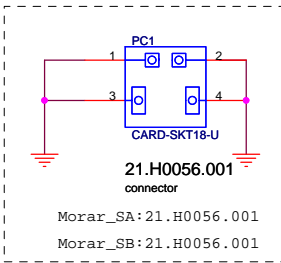
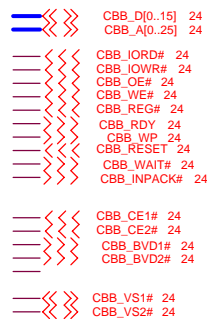
緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.



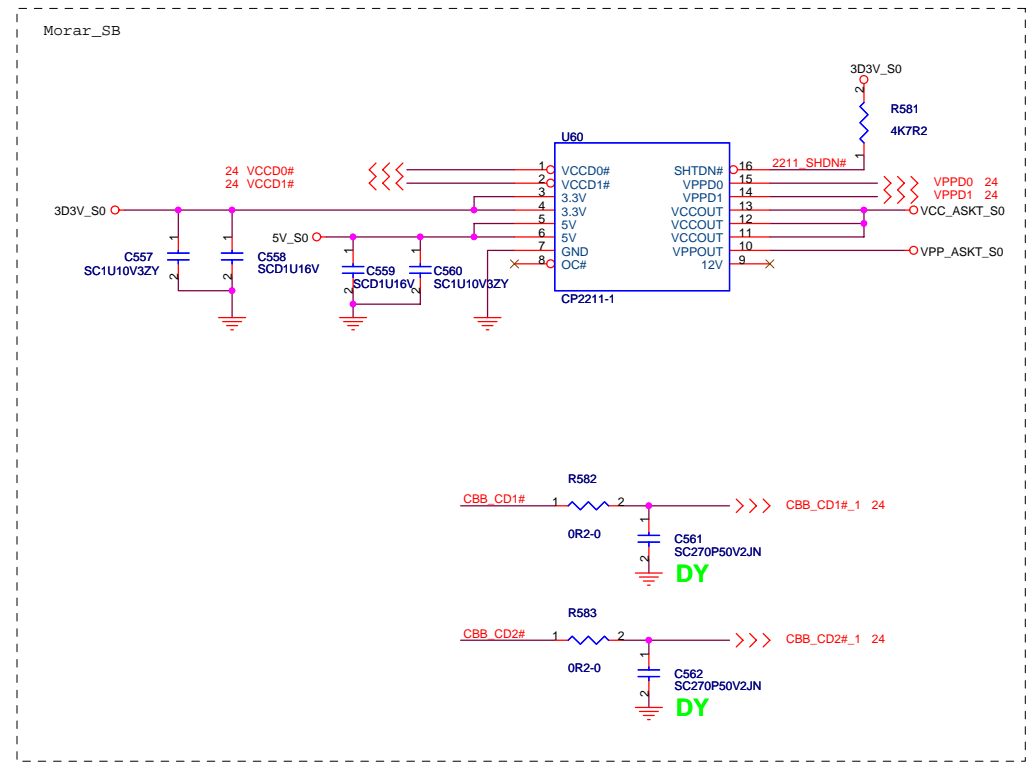
# PCMCIA Socket



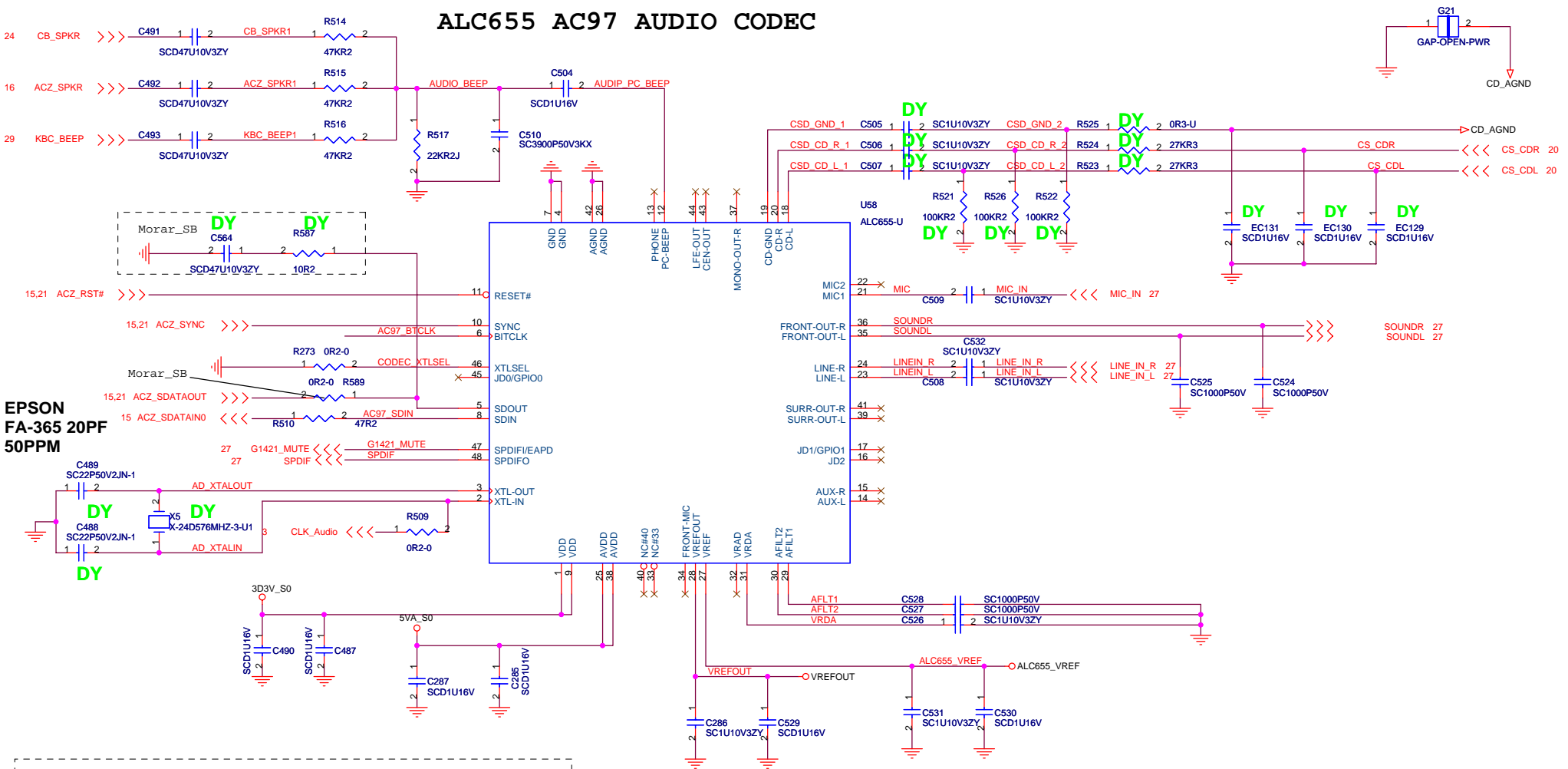
# Cardbus I/F



# Power switch



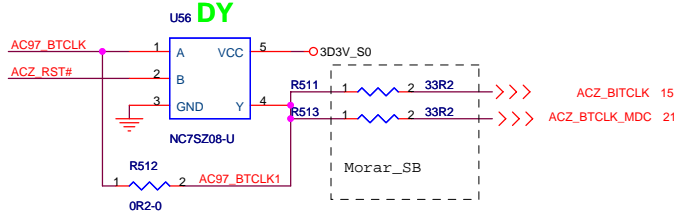
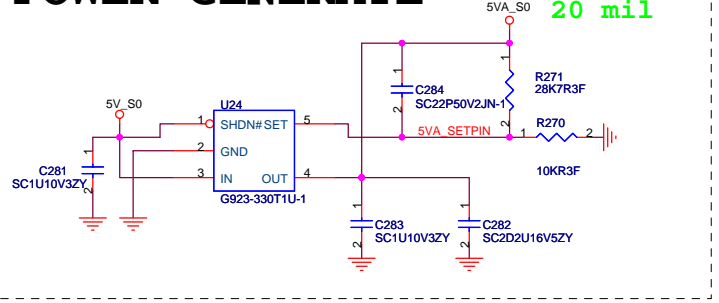
# ALC655 AC97 AUDIO CODEC



**EPSON  
FA-365 20PF  
50PPM**

## POWER GENERATE

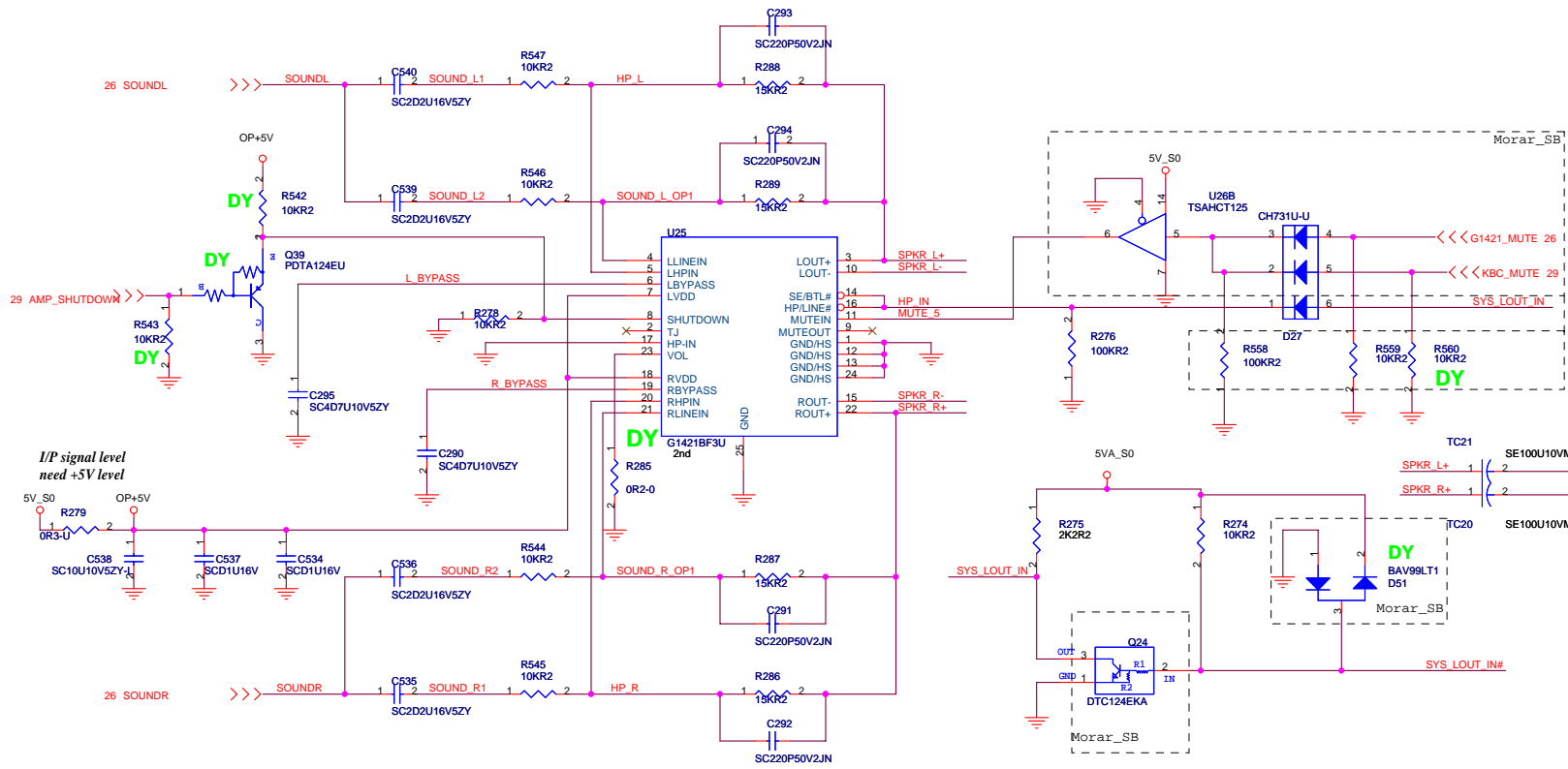
**\*Layout\*  
20 mil**



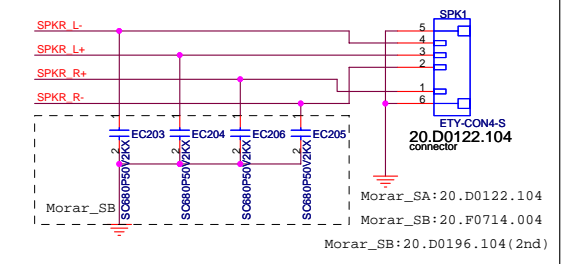
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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>AC'97 CODEC - ALC655</b>		
Size A3	Document Number <b>MORAR</b>	Rev <b>SB</b>
Date: Saturday, May 28, 2005	Sheet 26	of 40

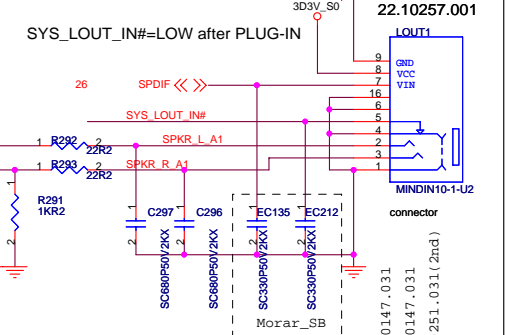
# AUDIO OP AMPLIFIER



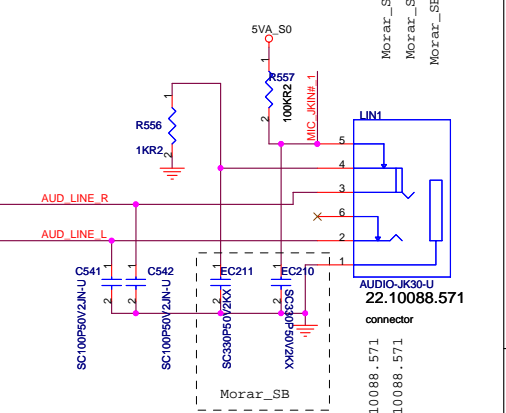
## Internal Speaker



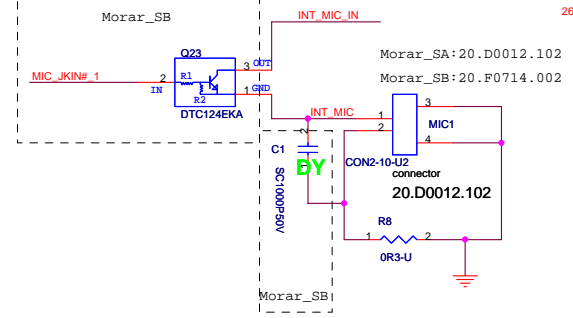
## LINE OUT



## LINE IN/MIC IN

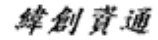


## Internal Mic

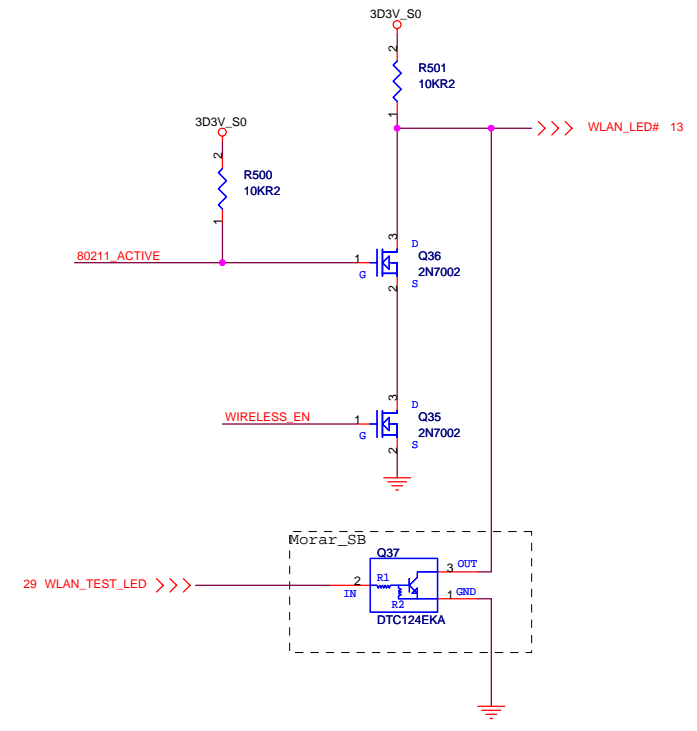
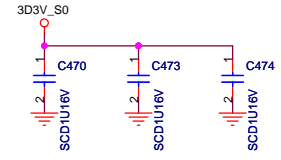
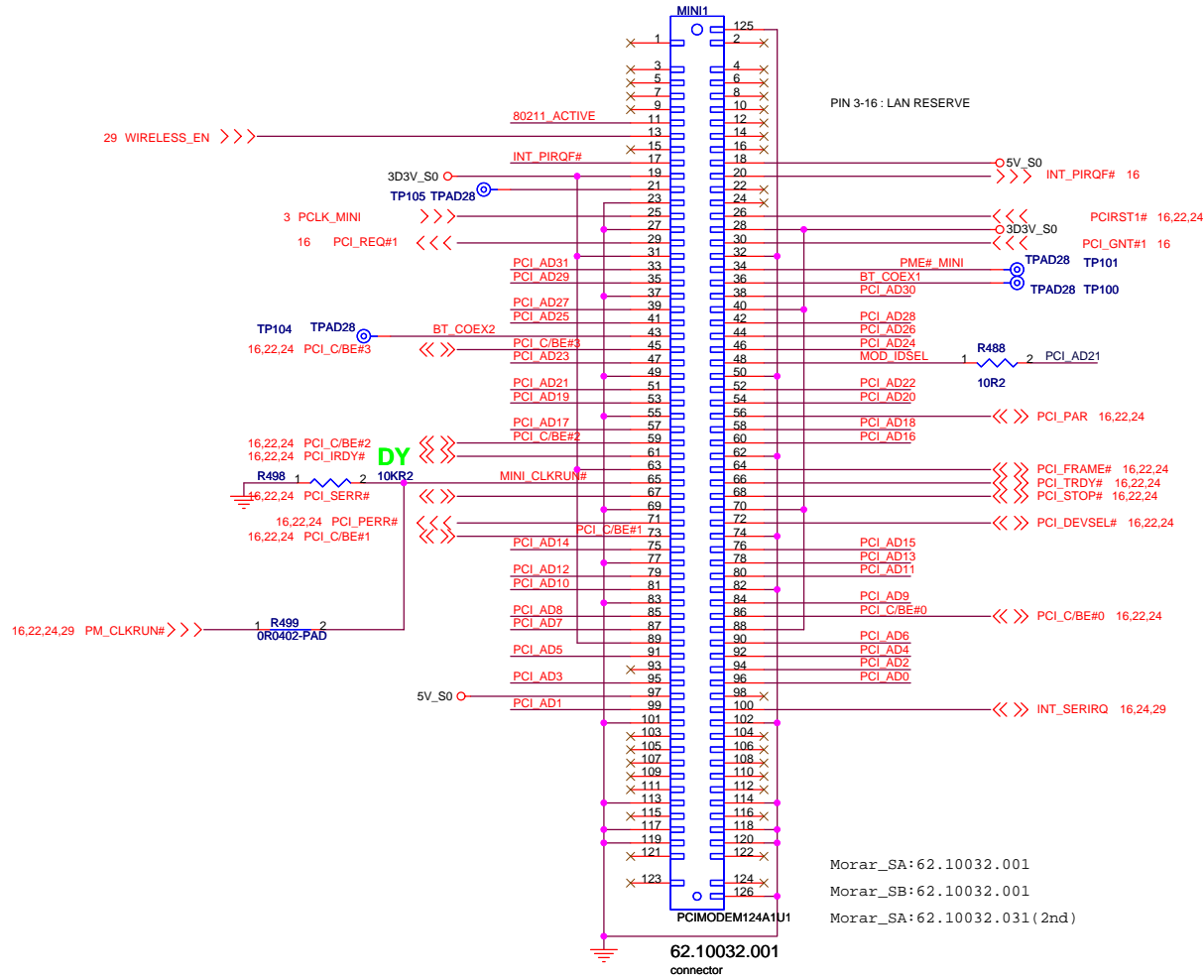


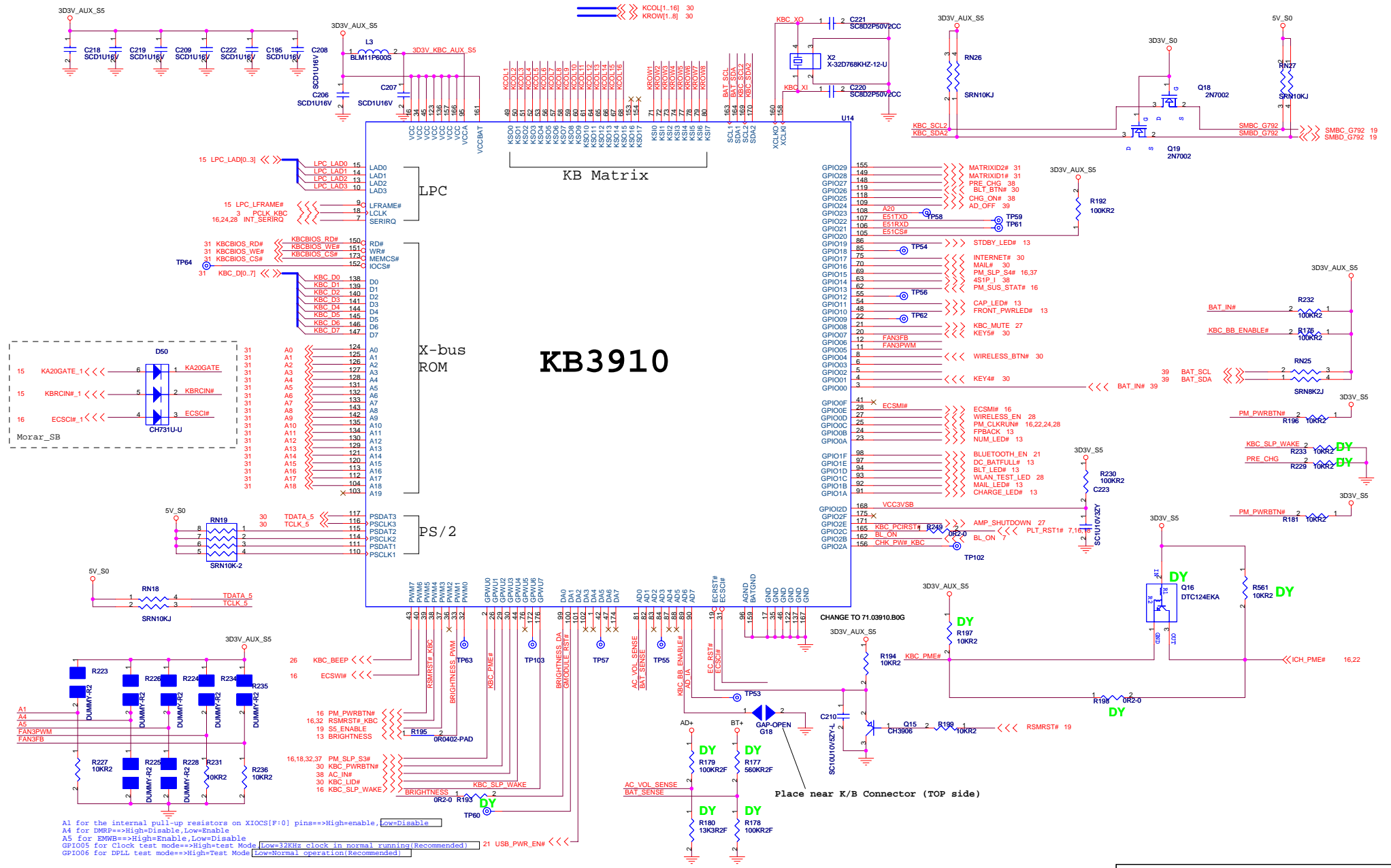
I/P signal level need +5V level

<Core Design>

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<b>Audio AMP and Jack</b>	
Title	Rev
Size	Document Number
<b>MORAR</b>	
Date: Saturday, May 28, 2005	Sheet 27 of 40

16,22,24 PCI\_AD[31..0] <<<

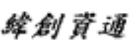




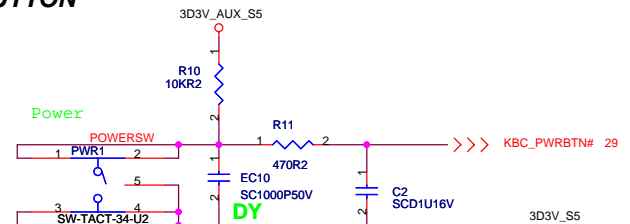
# KB3910

A1 for the internal pull-up resistors on XIOCS[P:0] pins==>High=enable, Low=Disable  
 A4 for DMW==>High=Disable, Low=Enable  
 A5 for EMWB==>High=Enable, Low=Disable  
 GPIO05 for Clock test mode==>High=test Mode, Low=32KHz clock in normal running (Recommended)  
 GPIO06 for DPLL test mode==>High=test Mode, Low=Normal operation (Recommended)

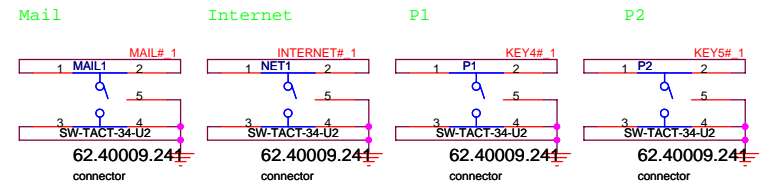
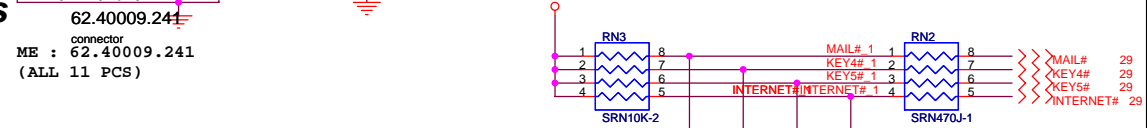
Place near K/B Connector (TOP side)

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<b>KBC ENE</b>	
<b>MORAR</b>	
Title: _____ Size: Custom Date: Friday, June 24, 2005	Document Number: _____ Rev: SB Sheet: 29 of 40

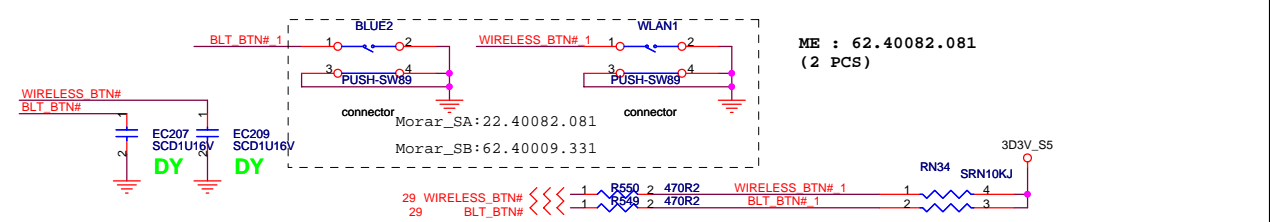
# POWER BUTTON



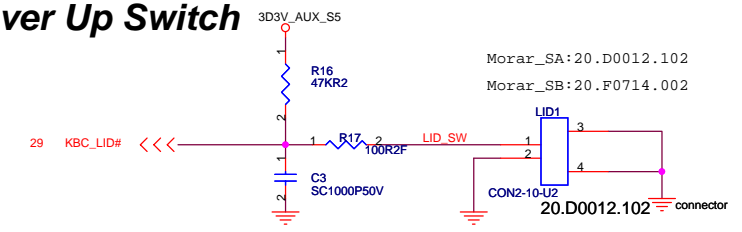
# Buttons



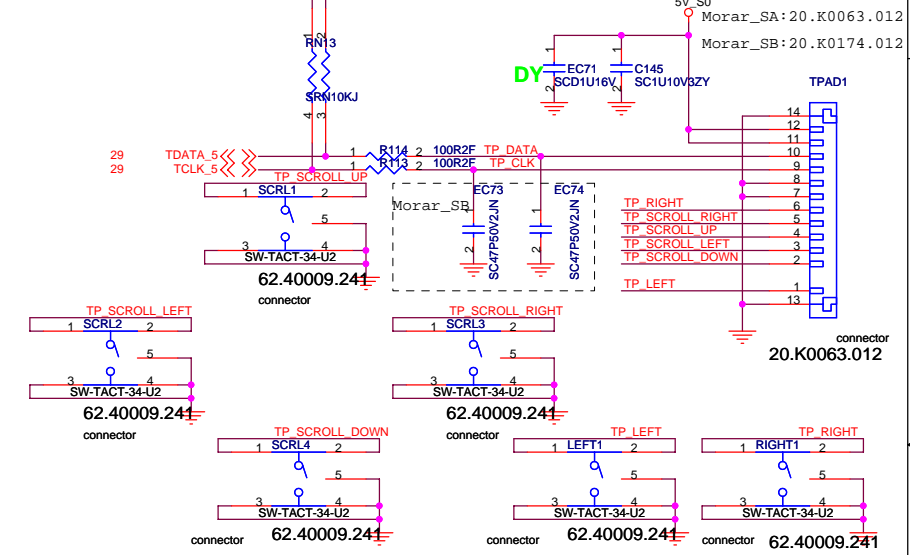
# BlueTooth ON/OFF Wireless ON/OFF



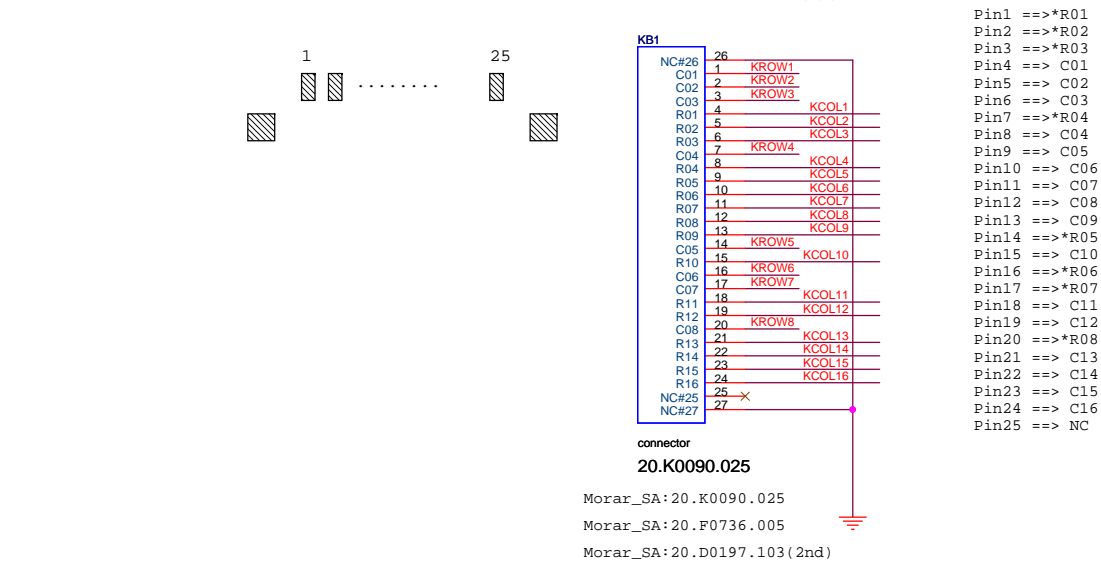
# Cover Up Switch



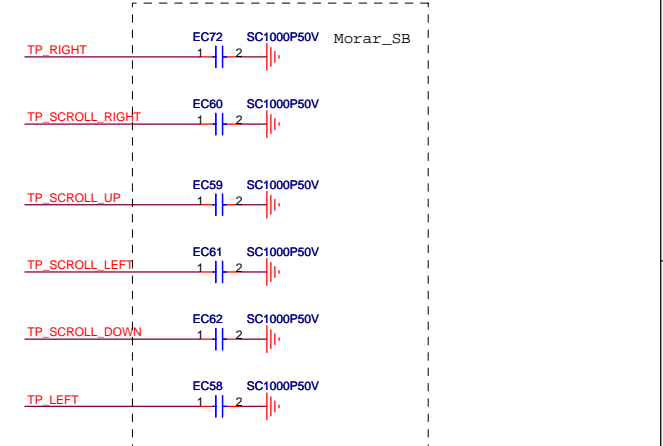
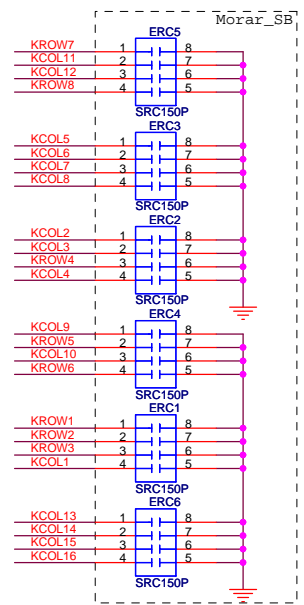
# TOUCH PAD



# Internal KeyBoard CONN



# EMI Bypass cap.



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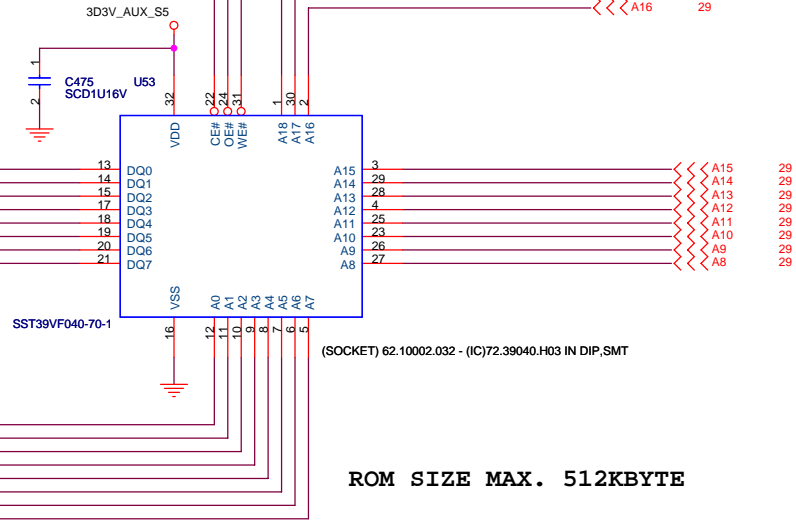
Title: **BUTTONS / KB / TOUCHPAD**  
 Size: A3 Document Number: **MORAR** Rev: **SB**  
 Date: Saturday, May 28, 2005 Sheet 30 of 40

>>> KBC\_D[0..7] 29

29 KBCBIOS\_WE#  
29 KBCBIOS\_RD#  
29 KBCBIOS\_CS#

29 KBC\_D0  
29 KBC\_D1  
29 KBC\_D2  
29 KBC\_D3  
29 KBC\_D4  
29 KBC\_D5  
29 KBC\_D6  
29 KBC\_D7

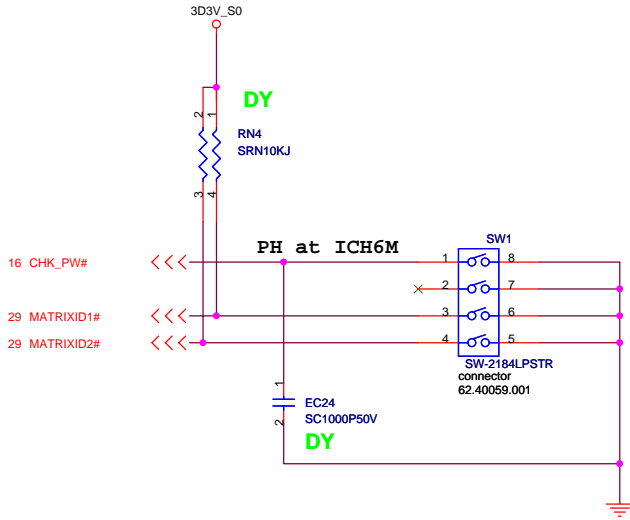
29 A0  
29 A1  
29 A2  
29 A3  
29 A4  
29 A5  
29 A6  
29 A7



(SOCKET) 62.10002.032 - (IC)72.39040.H03 IN DIP,SMT

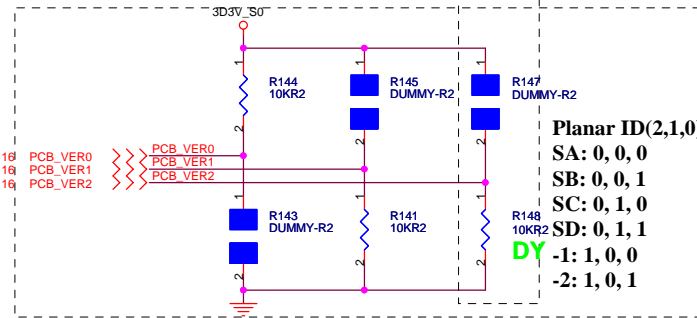
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:  
SSKT3262.10002.032  
SSKT32 62.10005.032



Morar\_SB1 Can not use in Board ID

Board ID



Keyboard matrix ( from vendor )

	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0

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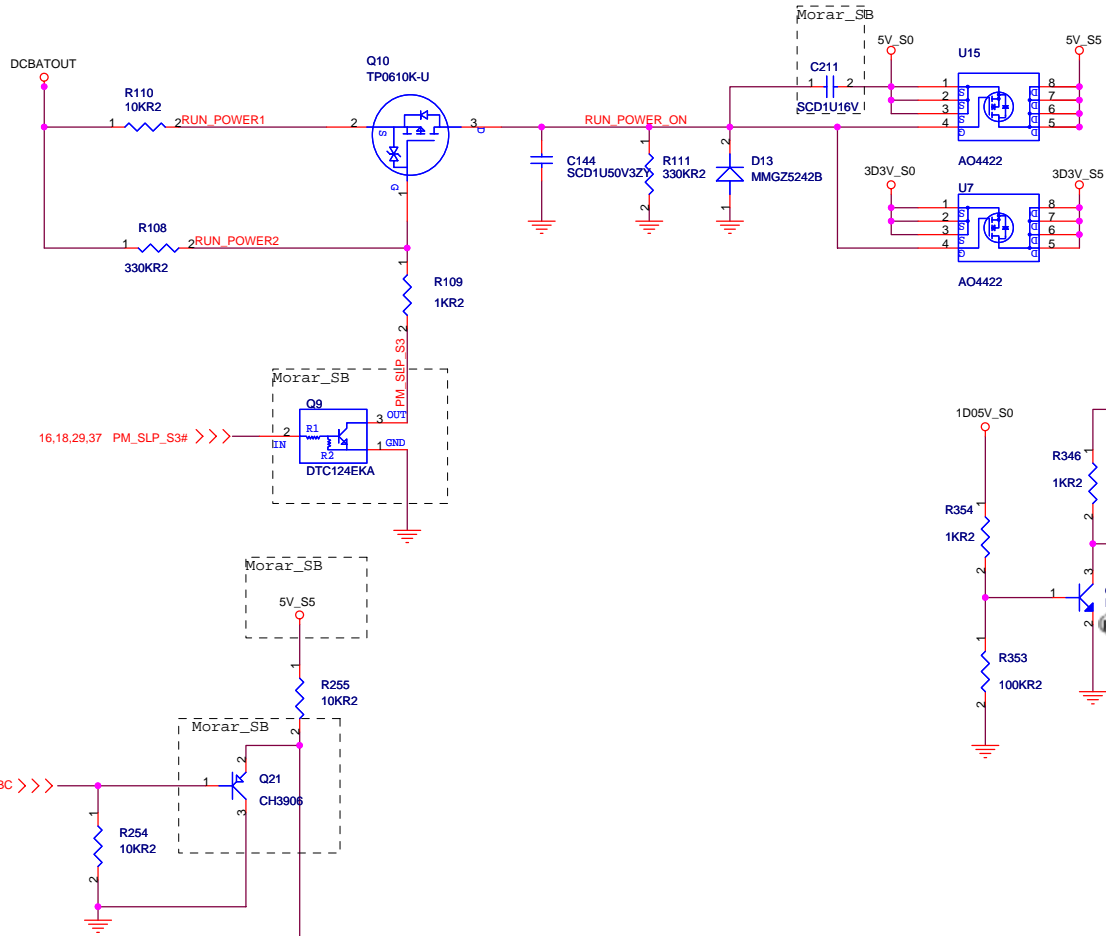
**BIOS ROM**

Title: **MORAR**

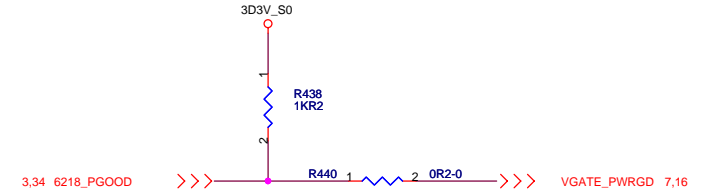
Size A3 Document Number Rev  
**SB**

Date: Saturday, May 28, 2005 Sheet 31 of 40

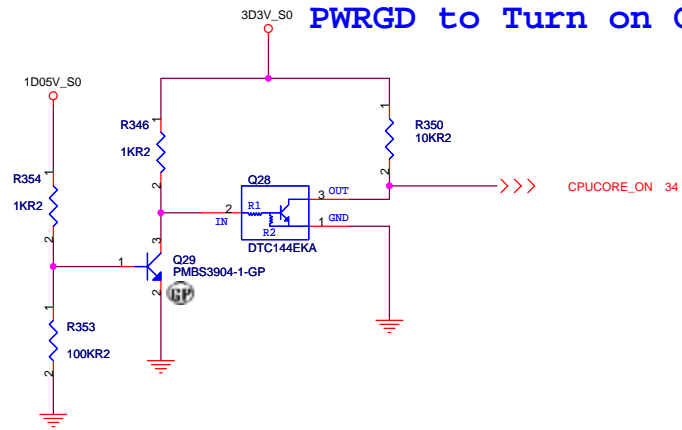
# Run Power



## PWRGD for NB and SB

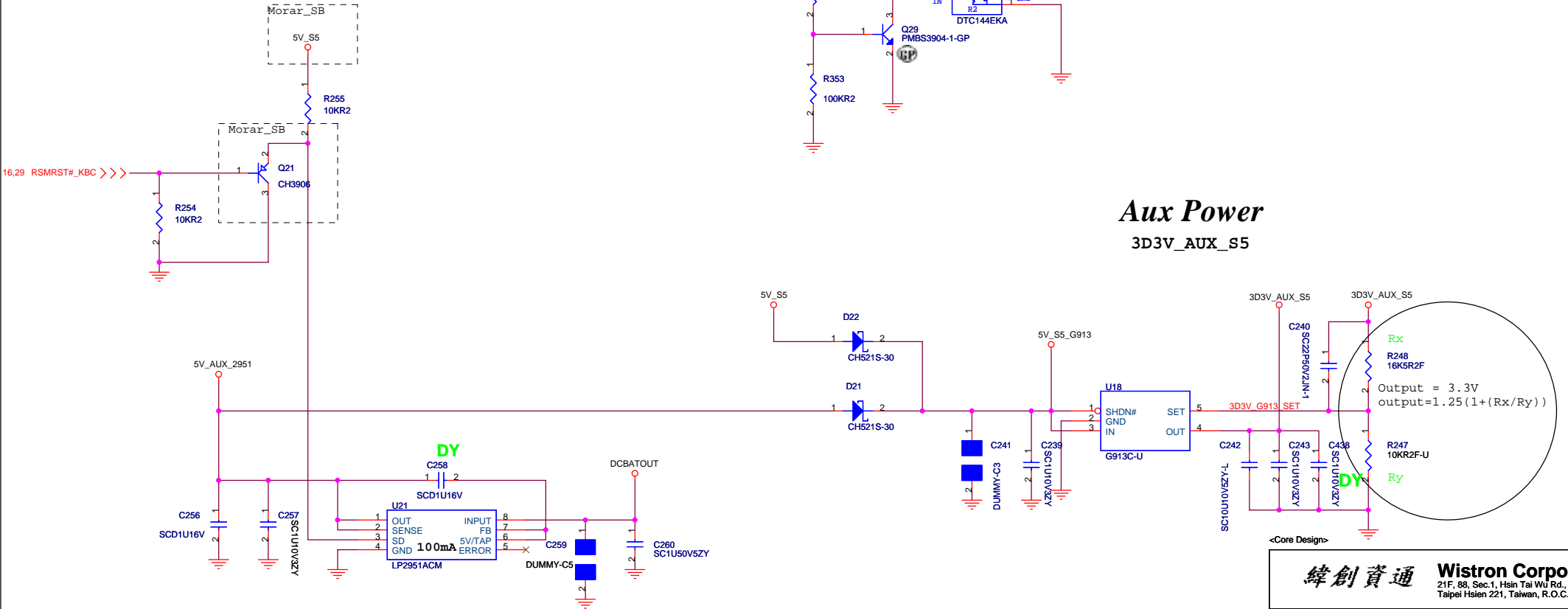


## PWRGD to Turn on CPU\_Core\_Power



## Aux Power

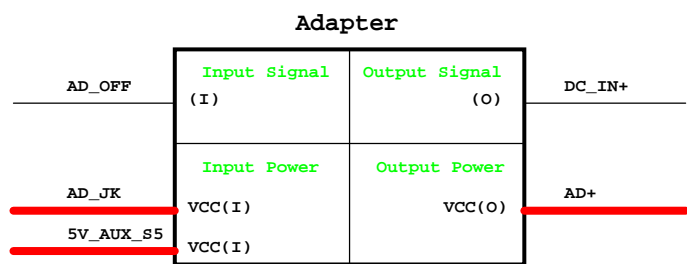
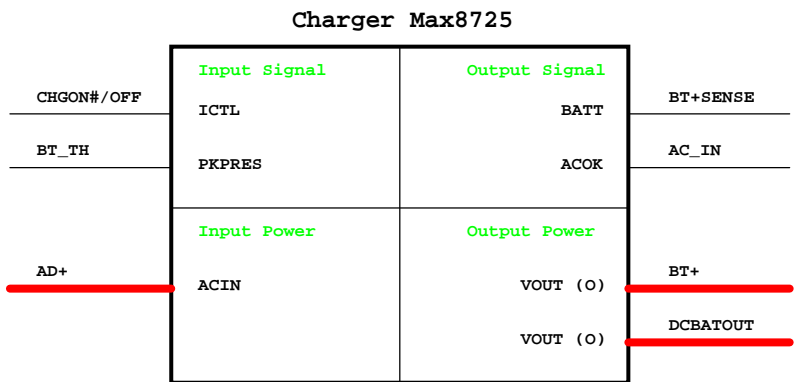
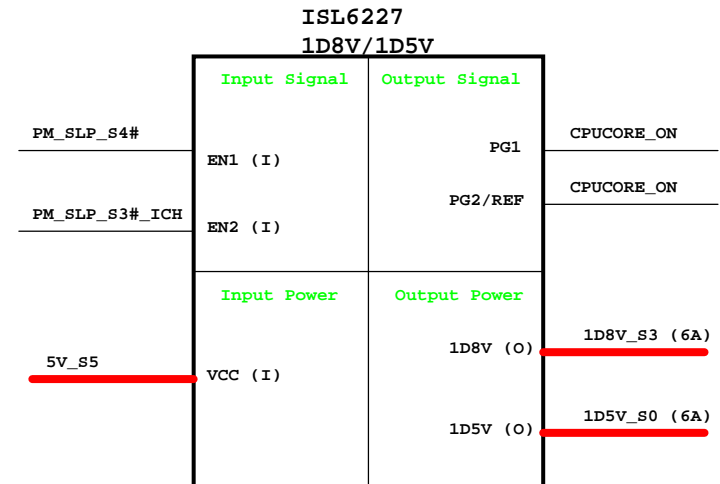
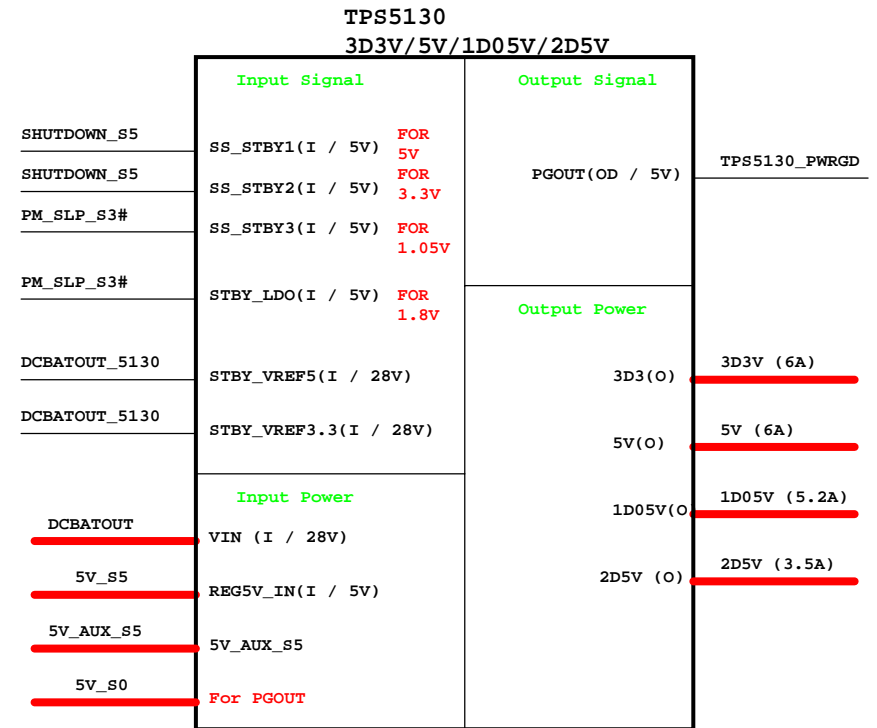
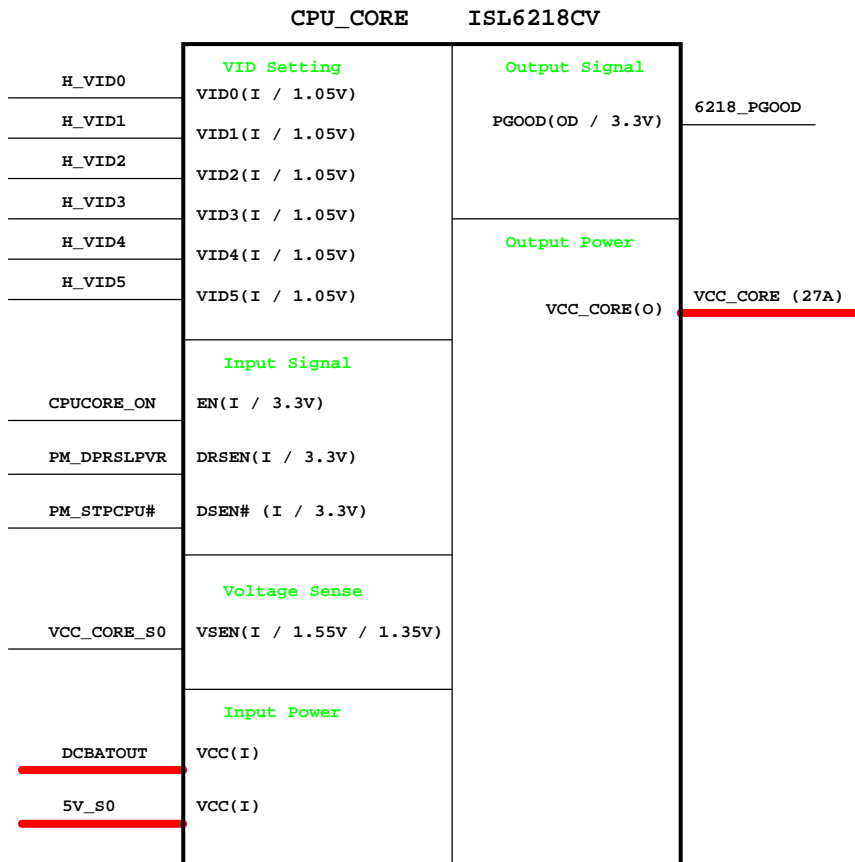
3D3V\_AUX\_S5



<Core Design>

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Title		
<b>RUN POWER and 3D3V AUX S5</b>		
Size	Document Number	Rev
A3	<b>MORAR</b>	<b>SB</b>
Date: Saturday, May 28, 2005		Sheet 32 of 40





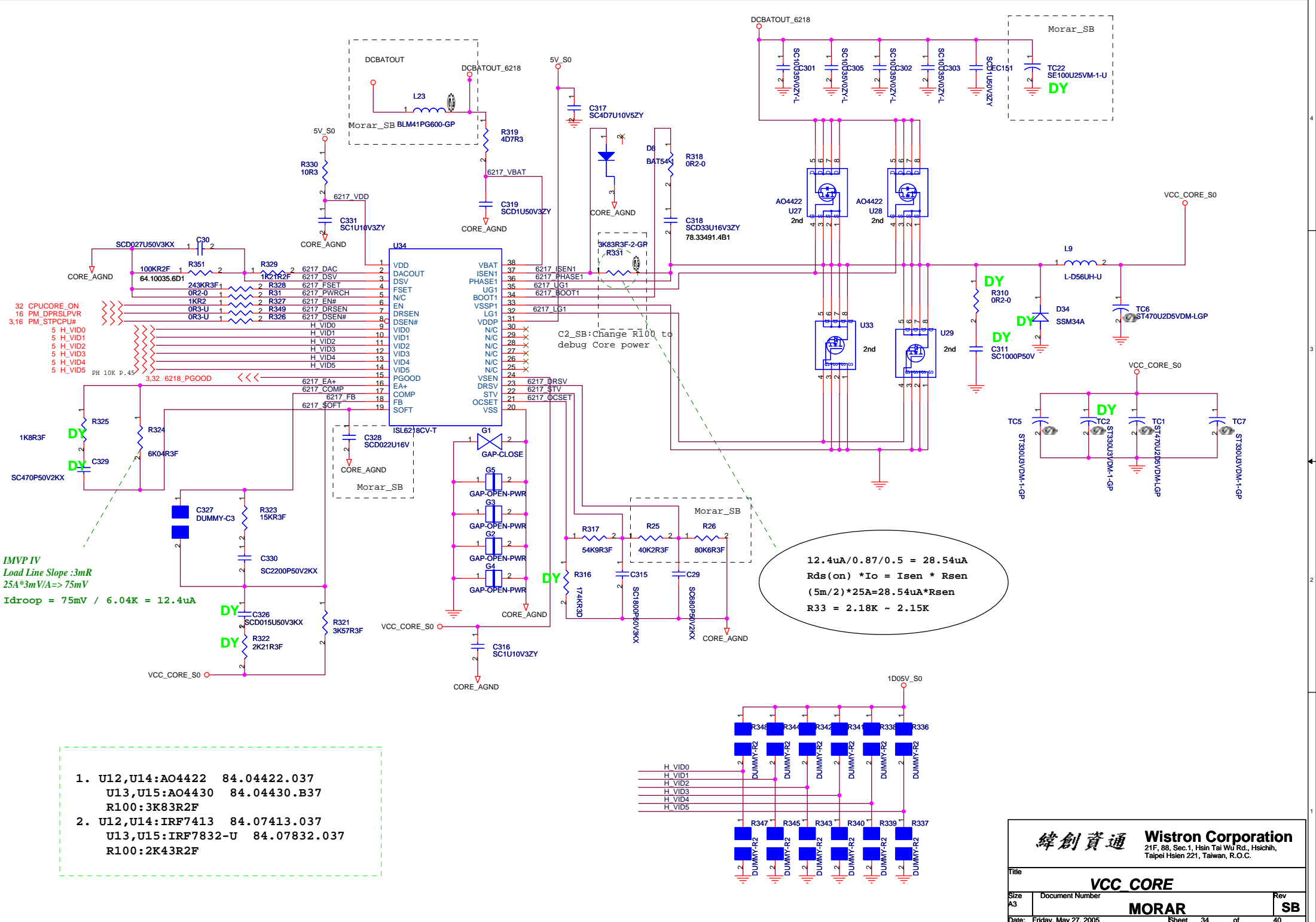
<Core Design>

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Title: **Power Diagram**

Size: A3 Document Number: **MORAR** Rev: **SB**

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32 CPU CORE\_ON  
 16 PM\_DPRS L\_PVR  
 3,16 PM\_STPCPU#  
 5 H\_VID0  
 5 H\_VID1  
 5 H\_VID2  
 5 H\_VID3  
 5 H\_VID4  
 5 H\_VID5  
 PH 10K P.45

IMVP IV  
 Load Line Slope :3mR  
 25A\*3mV/A => 75mV  
 Idroop = 75mV / 6.04K = 12.4uA

$$12.4\mu A / 0.87 / 0.5 = 28.54\mu A$$

$$R_{ds(on)} * I_o = I_{sen} * R_{sen}$$

$$(5m/2) * 25A = 28.54\mu A * R_{sen}$$

$$R_{33} = 2.18K \sim 2.15K$$

- U12,U14:AO4422 84.04422.037  
 U13,U15:AO4430 84.04430.B37  
 R100:3K83R2F
- U12,U14:IRF7413 84.07413.037  
 U13,U15:IRF7832-U 84.07832.037  
 R100:2K43R2F

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Title: **VCC CORE**

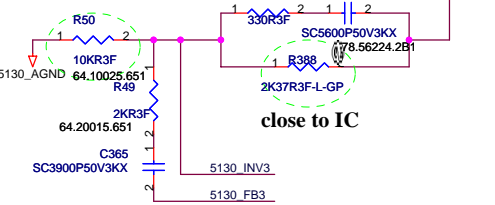
Size: A3 Document Number: MORAR Rev: SB

Date: Friday, May 27, 2005 Sheet: 34 of 40

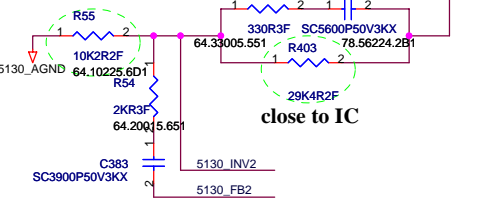
# TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(5V=>CH1 , 3D3V=>CH2 , 1D05V =>CH3)

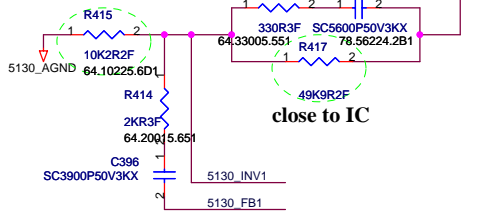
For 1.05V  
SETTING=1.0515V



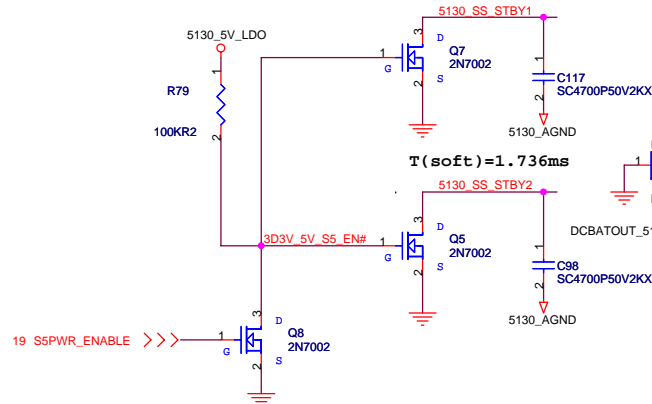
For 3V  
SETTING=3.3V



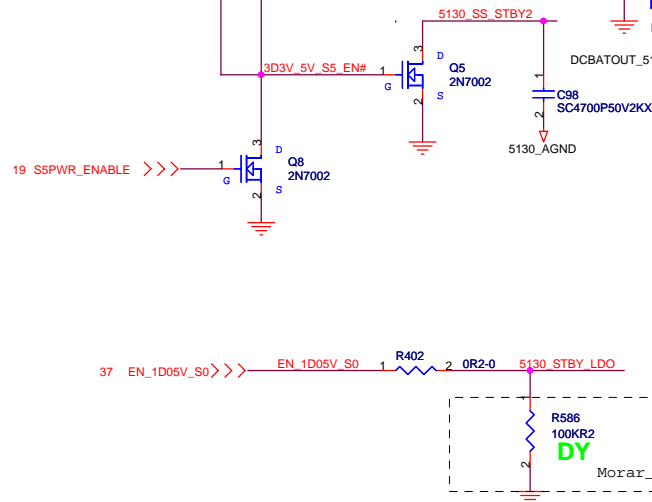
For 5V  
SETTING=5.008V



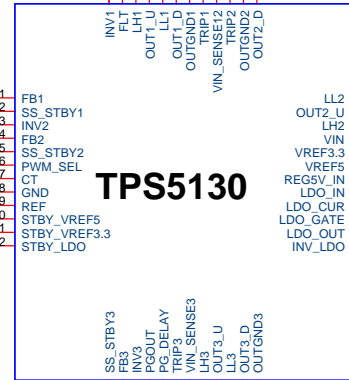
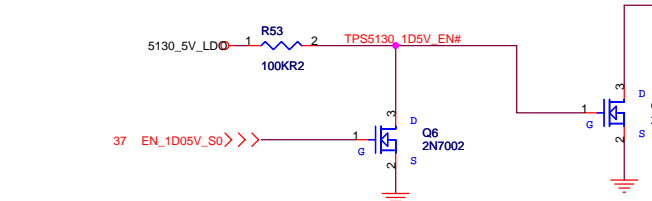
T(soft)=1.736ms



T(soft)=1.736ms

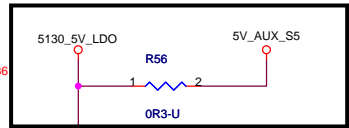
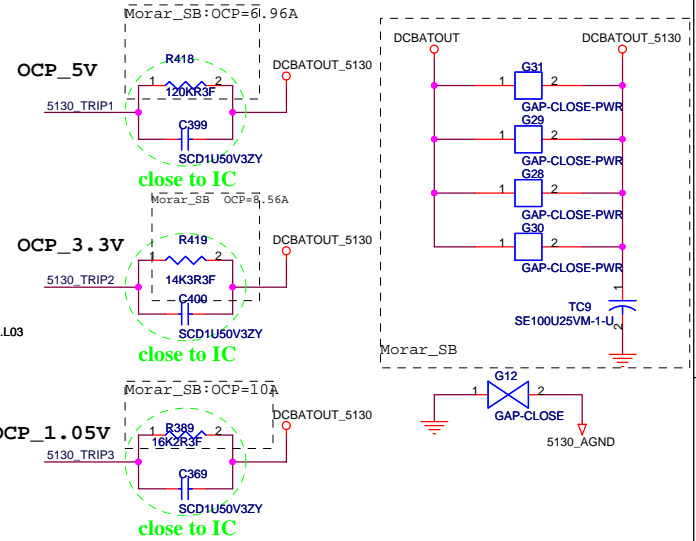


T(soft)=1.736ms



TPS5130

LDO SETTING  
For 2.5V  
SETTING=2.516V



	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

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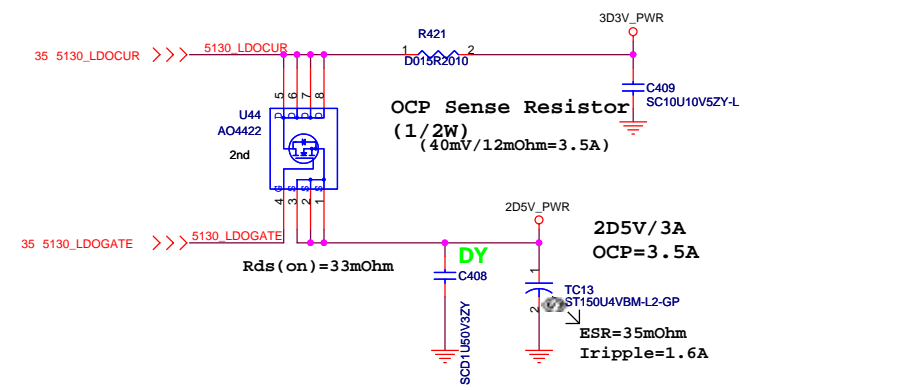
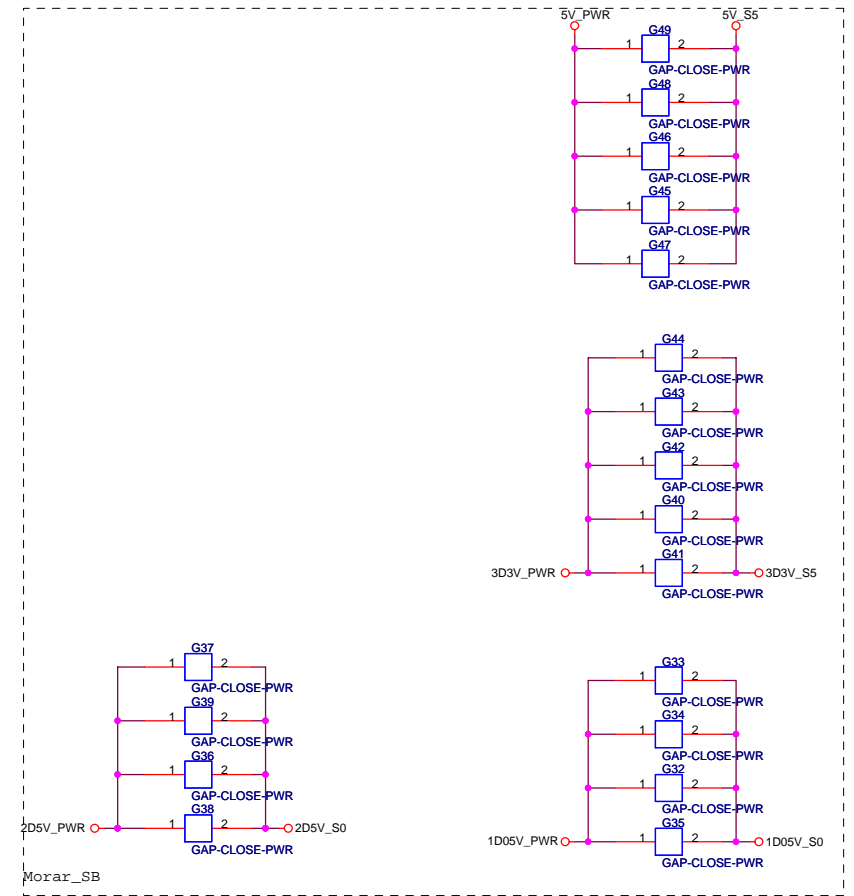
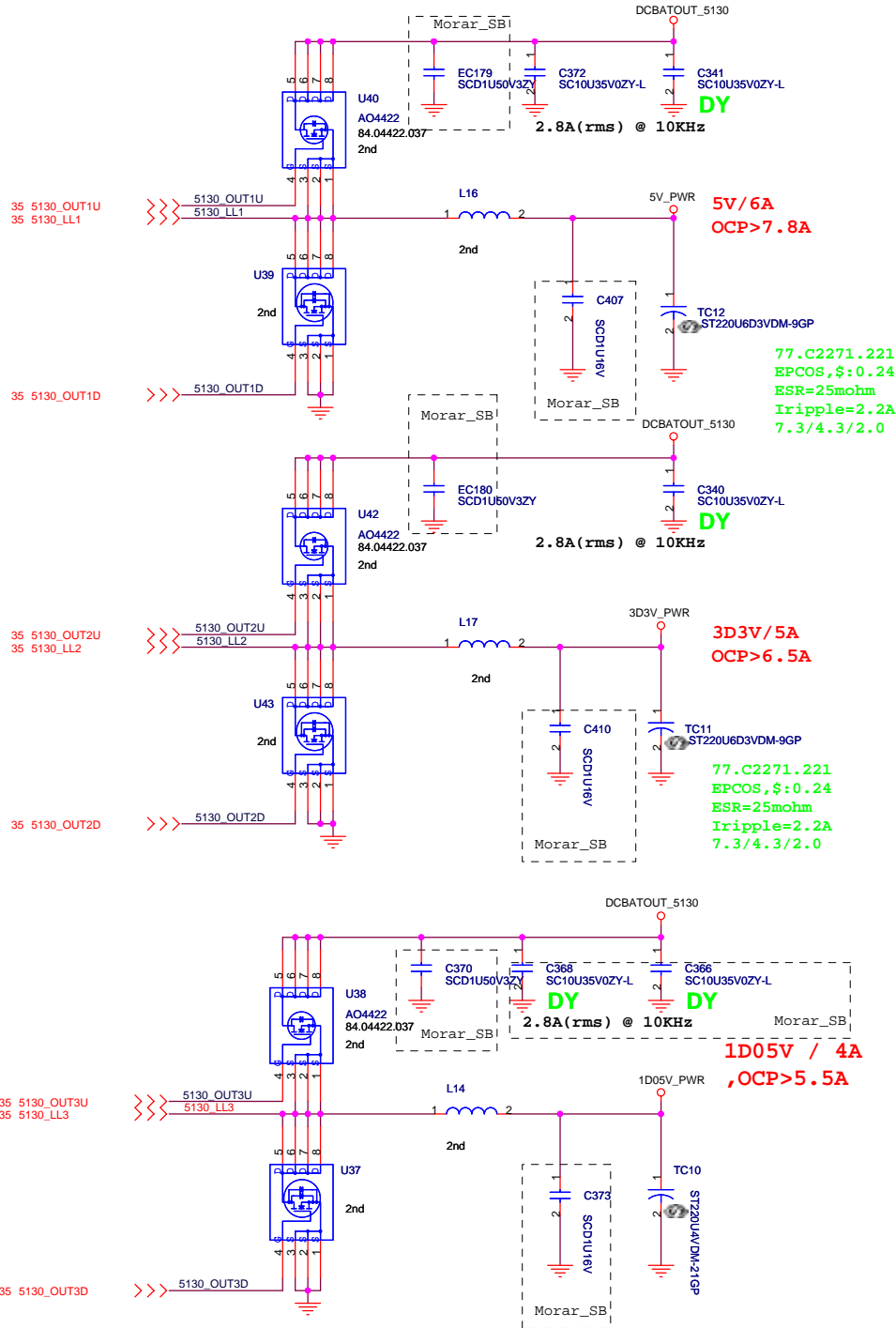
Title: **TI TPS5130 --- 5V/3.3V/1.05V,2.5(LDO)**

Size: A3 Document Number: **MORAR** Rev: **SB**

Date: Friday, May 27, 2005 Sheet 35 of 40

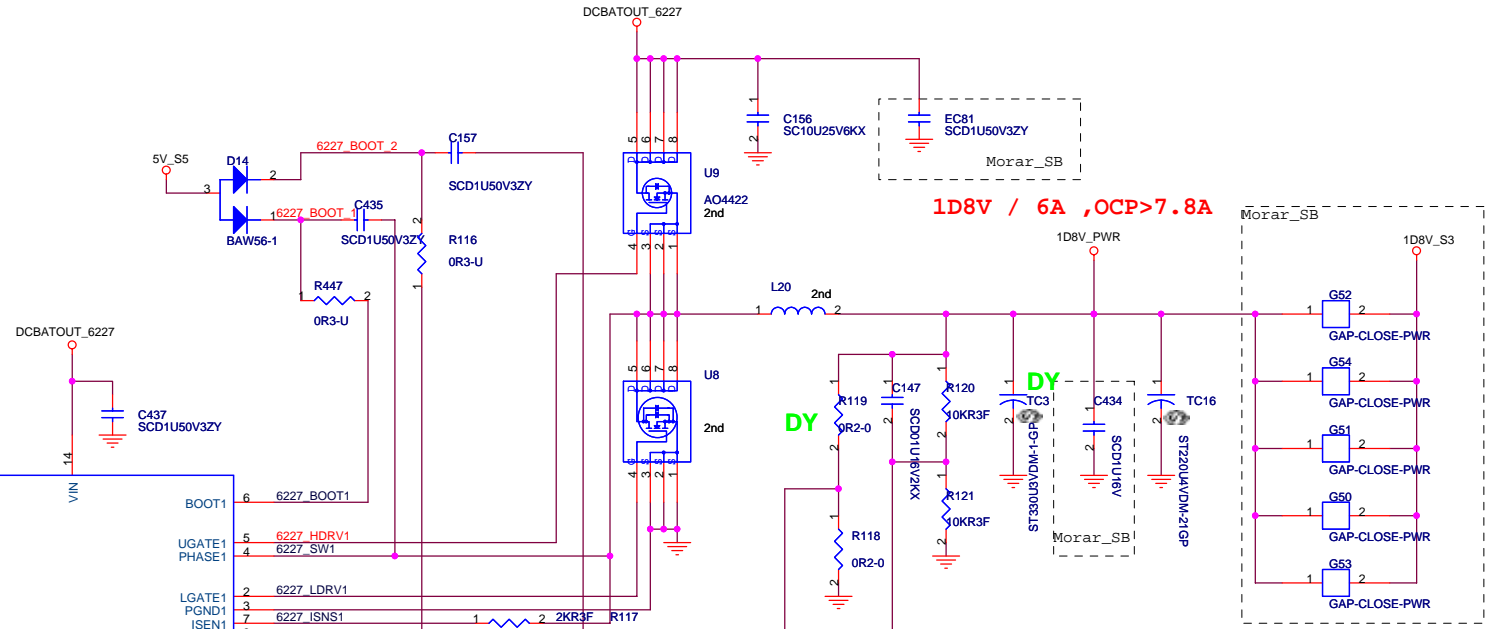
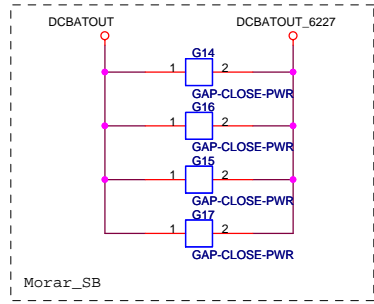
# TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(5V=>CH1 , 3D3V=>CH2 , 1D05V =>CH3)

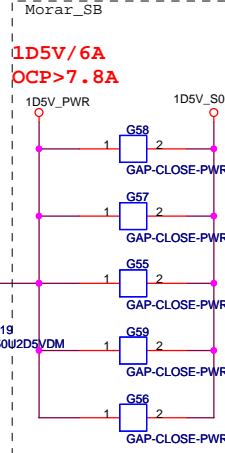
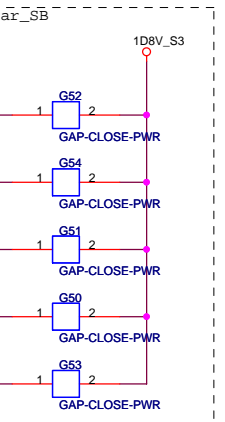


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Title <b>TI TPS5130 --- 5V/3.3V/1.05V,2.5(LDO)</b>		
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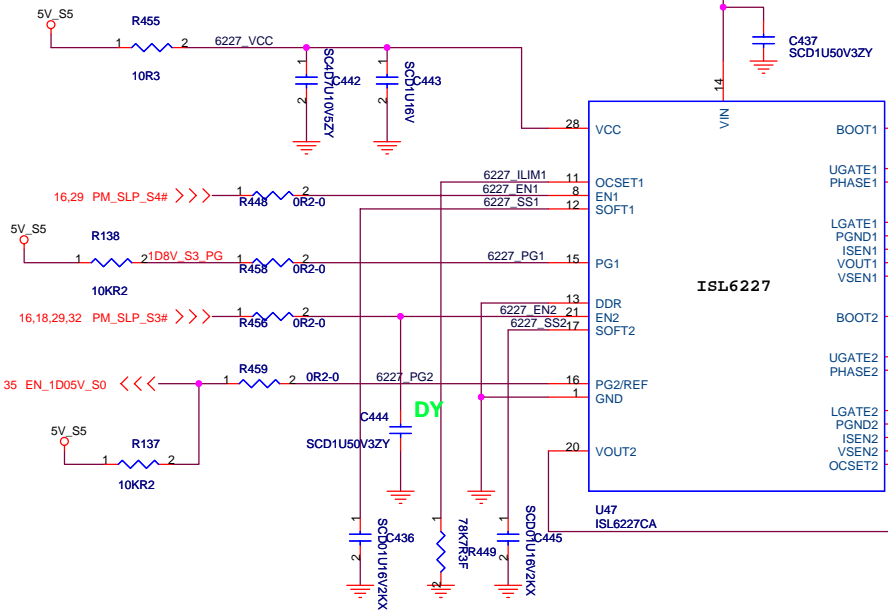


1D8V / 6A , OCP > 7.8A



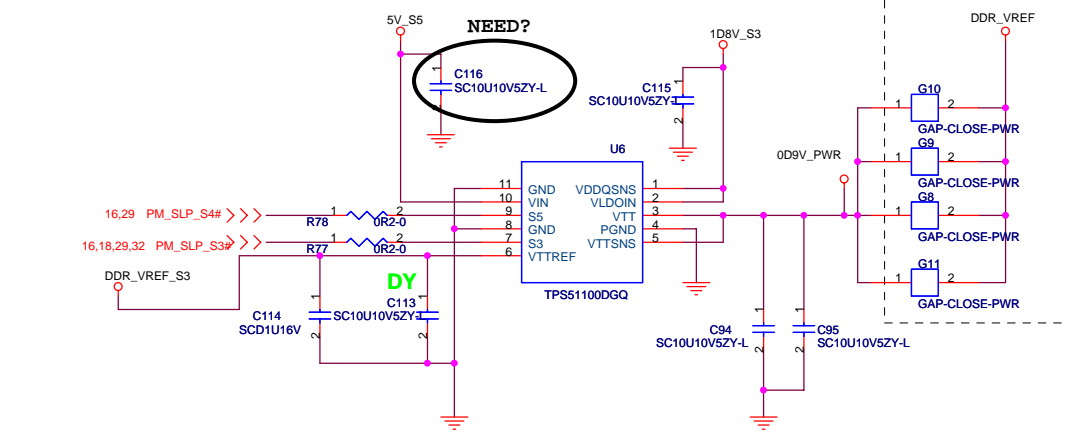
1D5V/6A  
OCP > 7.8A

77.C2271.191  
EPCOS, \$: 0.243  
ESR=15mohm  
Tripple=2.9A  
7.3/4.3/2.0

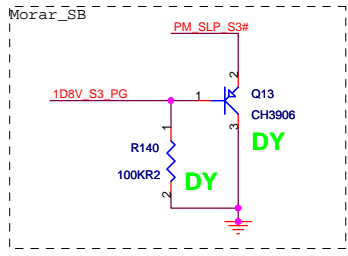


OCP  
7.8A=>R169=151K  
9.0A=>R169=133K

0D9V



NEED?

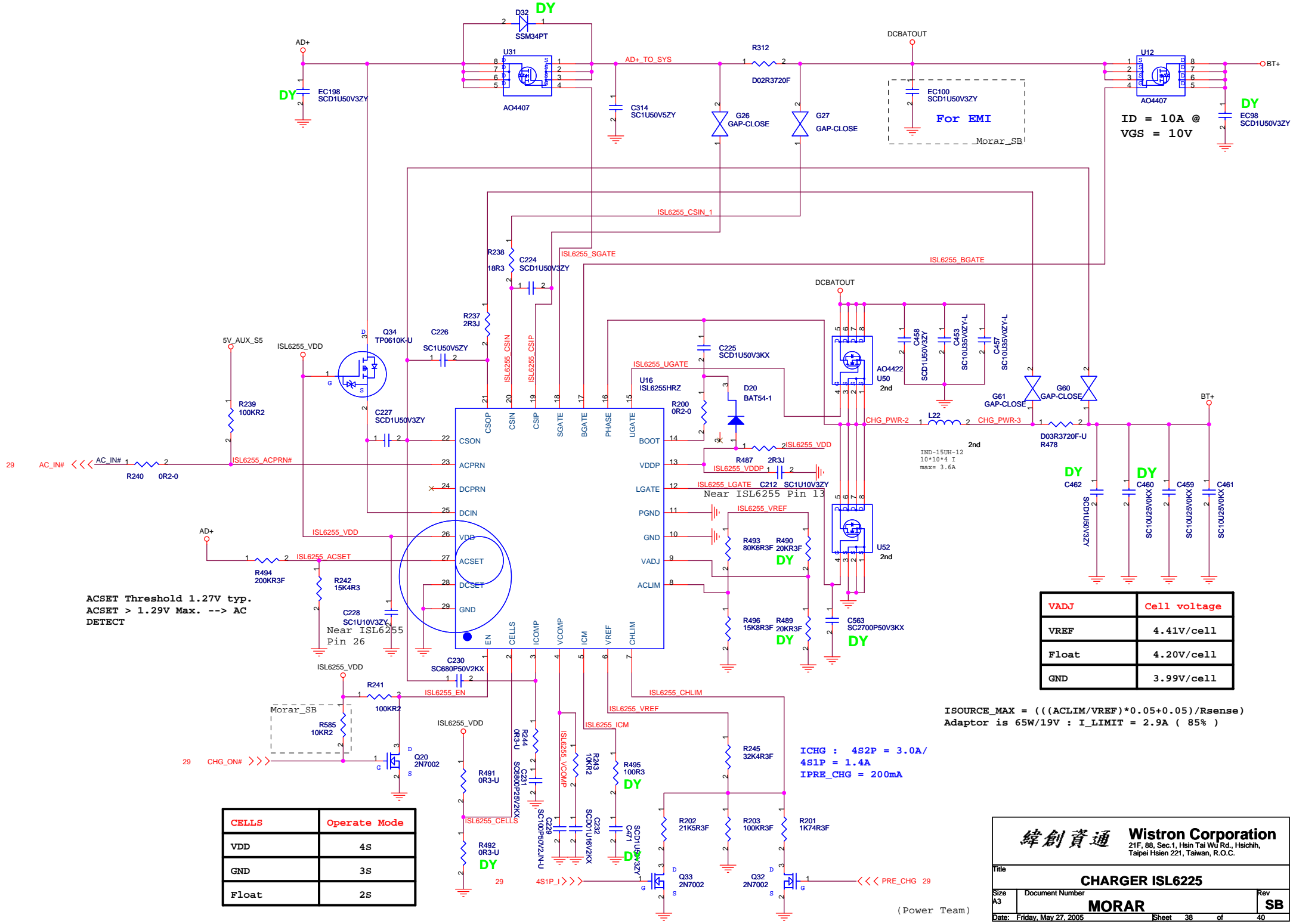


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Title: 1D8V/1D5V/0D9V

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ACSET Threshold 1.27V typ.  
 ACSET > 1.29V Max. --> AC  
 DETECT

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE\_MAX = (((ACLIM/VREF)\*0.05+0.05)/Rsense)  
 Adaptor is 65W/19V : I\_LIMIT = 2.9A ( 85% )

ICHG : 4S2P = 3.0A/  
 4S1P = 1.4A  
 IPRE\_CHG = 200mA

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Title: **CHARGER ISL6225**

Size A3 Document Number: **MORAR** Rev: **SB**

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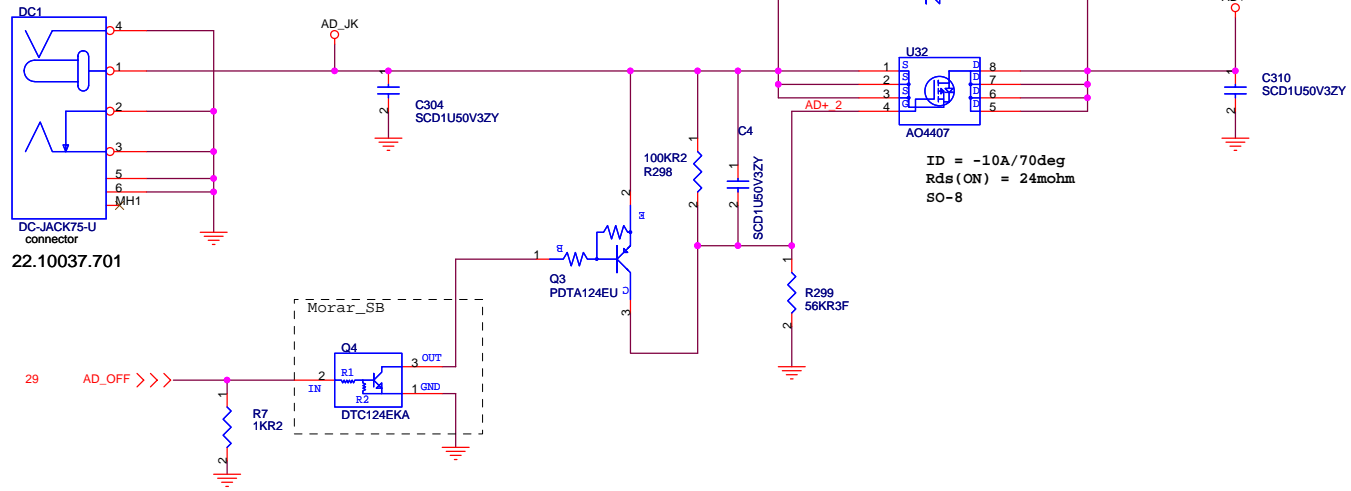
(Power Team)

### Adaptor in to generate DCBATOUT

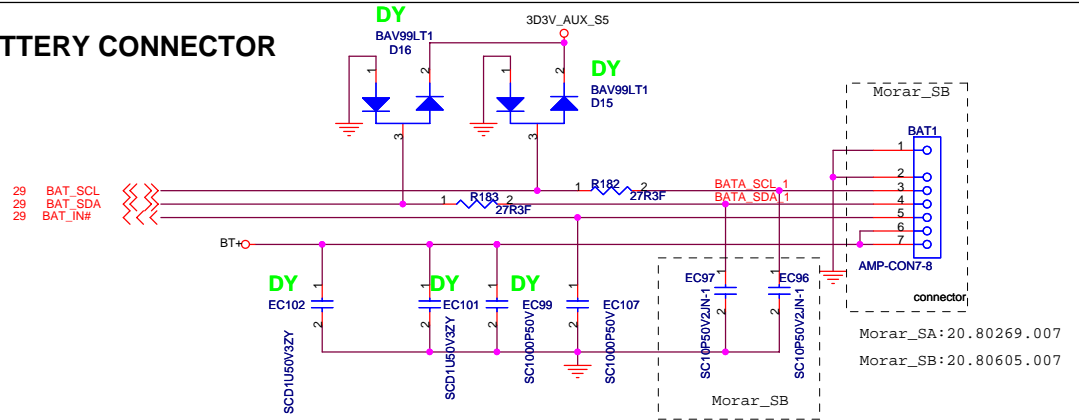
Morar\_SA: 22.10037.701

Morar\_SB: 22.10037.701

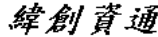
Morar\_SB: 22.10037.B02(2nd)

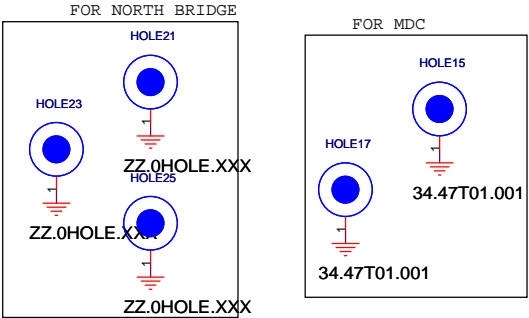
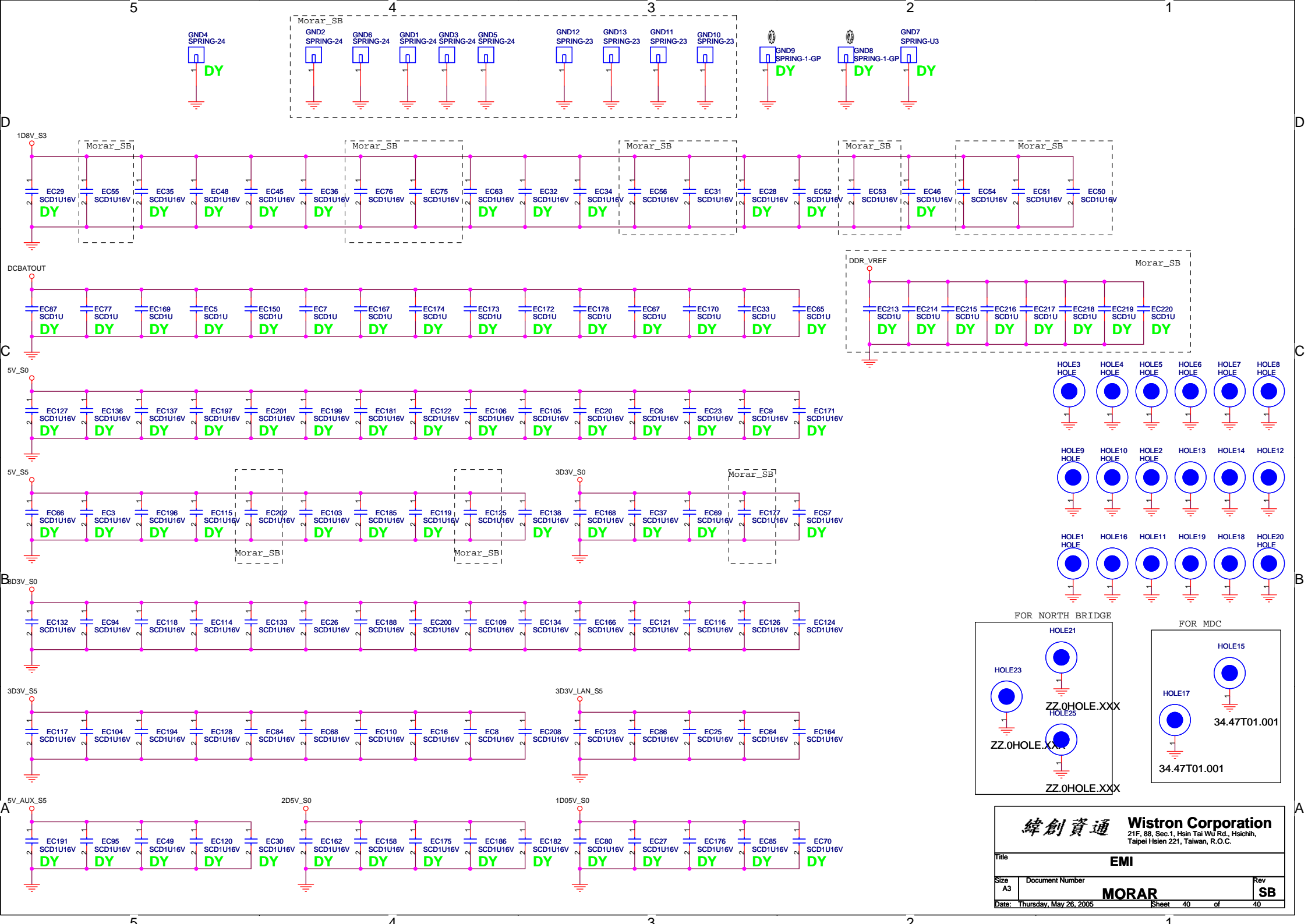


### BATTERY CONNECTOR



<Variant Name>

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<b>AD/BATT CONN</b>		
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Title: **EMI**

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