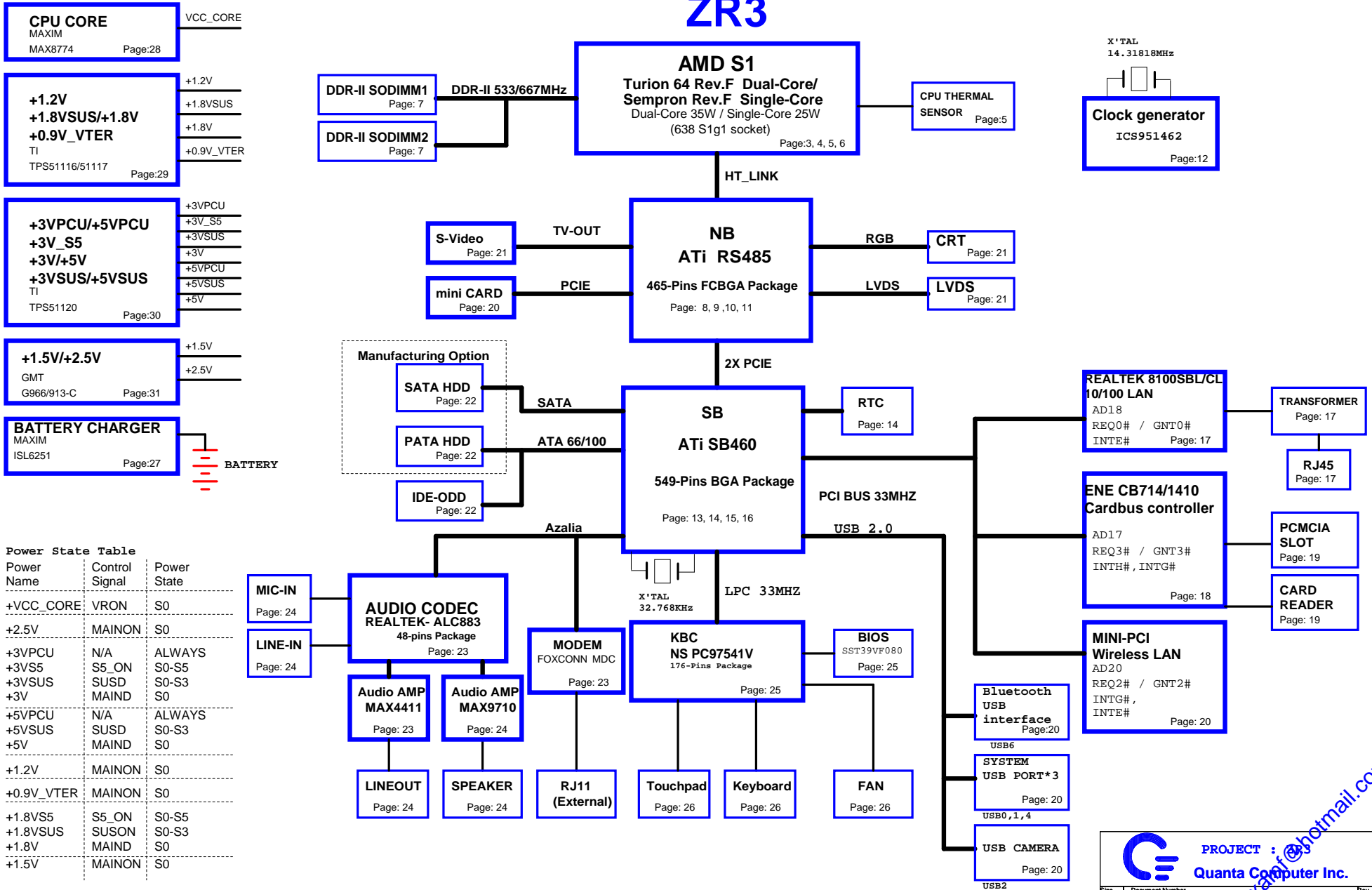


ZR3



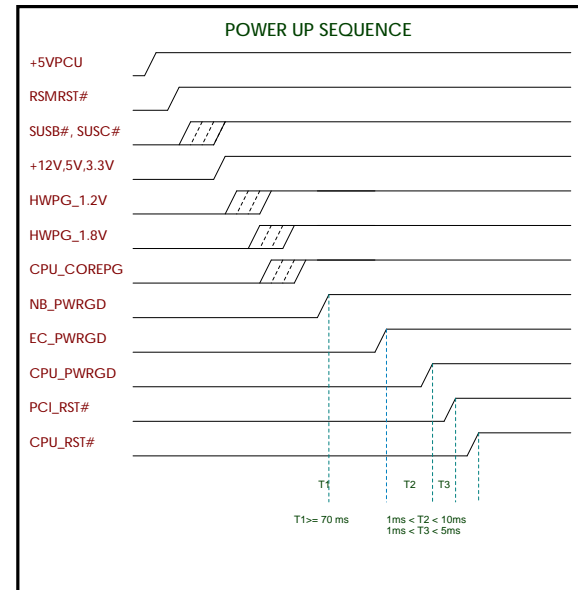
Power State Table

Power Name	Control Signal	Power State
+VCC_CORE	VRON	S0
+2.5V	MAINON	S0
+3VPCU	N/A	ALWAYS
+3VS5	S5_ON	S0-S5
+3VSUS	SUSD	S0-S3
+3V	MAIND	S0
+5VPCU	N/A	ALWAYS
+5VSUS	SUSD	S0-S3
+5V	MAIND	S0
+1.2V	MAINON	S0
+0.9V_VTER	MAINON	S0
+1.8VS5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAIND	S0
+1.5V	MAINON	S0

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 Page 04 : ATHLON64 DDRII MEMORY I/F
 Page 05 : ATHLON64 CTRL & DEBUG
 Page 06 : ATHLON64 PWR & GND
 Page 07 : DDRII SODIMMX2
 Page 08 : RS485-HT LINK0 I/F
 Page 09 : RS485-PCIE LINK I/F
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 Page 11 : RS485-POWER
 Page 12 : External CLOCK GENERATOR
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 Page 15 : SB460M HDD/POWER/DECOUPLING
 Page 16 : SB460M STRAPS
 Page 17 : LAN RTL8110SBL/CL
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 Page 21 : CRT & LVDS & S-Video
 Page 22 : HDD & CDROM & HOLES
 Page 23 : ALC883 & MDC & HP AMP
 Page 24 : SPEAKER AMP / JACK
 Page 25 : 97551 & FLASH
 Page 26 : T/P,FAN,SWITCH,LED,K/B
 Page 27 : BATTERY CHARGER
 Page 28 : VCORE MAX8774
 Page 29 : TPS51116/51117 1.8V/1.2V
 Page 30 : TPS51120 3/5V
 Page 31 : +1.5V / 2.5V

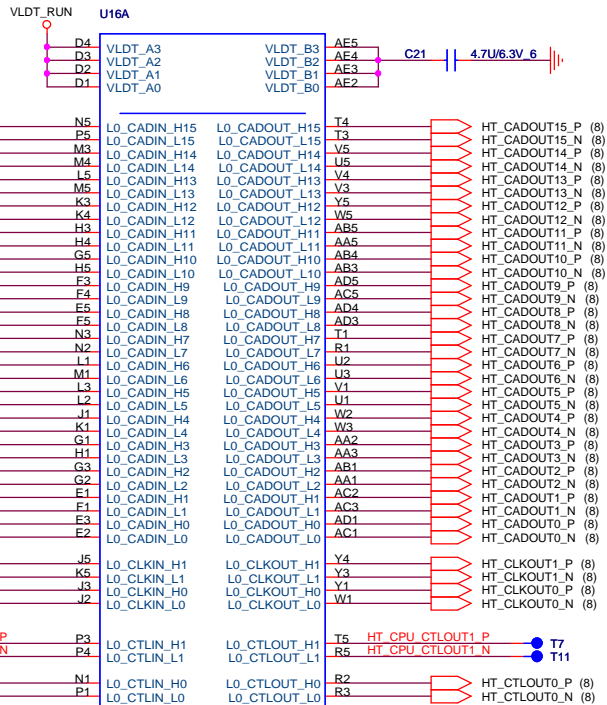
	POWER	VOLTAGE	ACTIVE SCOPE	PAGE
SYSTEM	+12V	+12V	S0	
	+5V	+5V	S0	
	+3V	+3.3V	S0	
	+5VPCU	+5V	ALWAYS	
	+3VPCU	+3.3V	ALWAYS	
	+5VSUS	+5V	S0-S3	
	+3VSUS	+3.3V	S0-S3	
	+3V_S5	+3.3V	S0	
	CPU	VCCCORE	VID[0..5]	S0
VDDA_RUN		+2.5V	S0	
VLDT_RUN		+1.2V	S0	
+0.9V_VTER		+0.9V	S0	
+1.8V		+1.8V	S0	
DDR2	+1.8VSUS	+1.8V	S0-S3	
	+0.9V_VTER	+0.9V	S0	
	+1.8V	+1.8V	S0	
RC485 NB	+1.8VSUS	+1.8V	S0-S3	
	+3V	+3.3V	S0	
	VDDC	+1.2V	S0	
	VDD_HT	+1.2V	S0	
	VDDA12	+1.2V	S0	
	VDD18	+1.8V	S0	
	VDDA18	+1.8V	S0	
	VDD_DVO	+1.8V	S0	
	VDDR3	+3.3V	S0	
	AVDD_NB	+3.3V	S0	
	AVDDQ	+1.8V	S0	
	PLLVDD	+1.8V	S0	
	LPVDD	+1.8V	S0	
	LPVDD18A	+1.8V	S0	
	SB460 SB	+3V	+3.3V	S0
+1.8V		+1.8V	S0	
+3V_S5		+3.3V	S0	
+1.8V_S5		+1.8V	S0	
VDD		+1.8V	S0	
AVDD_CK		+1.8V	S0	
AVDD_SATA		+1.8V	S0	
XTLVDD_ATA		+1.8V	S0	
PLLVDD_ATA		+1.8V	S0	
PCIE_PVDD		+1.8V	S0	
PCIE_VDDR		+1.8V	S0	
CPU-PWR		+1.2V	S0	
VDDQ		+3.3V	S0	
V5_VREF		+5V	S0	
+1.8V_SUB_PHY		+1.8V	S0	
+3VSUS	+3.3V	S0-S3		
+SB_S5_3V	+3.3V	S0		
+SB_S5_1.8V	+1.8V	S0		



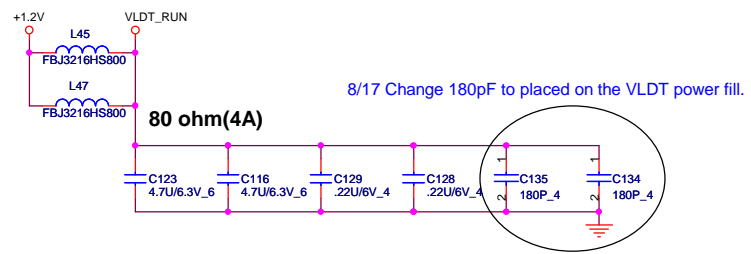


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1 Processor Socket



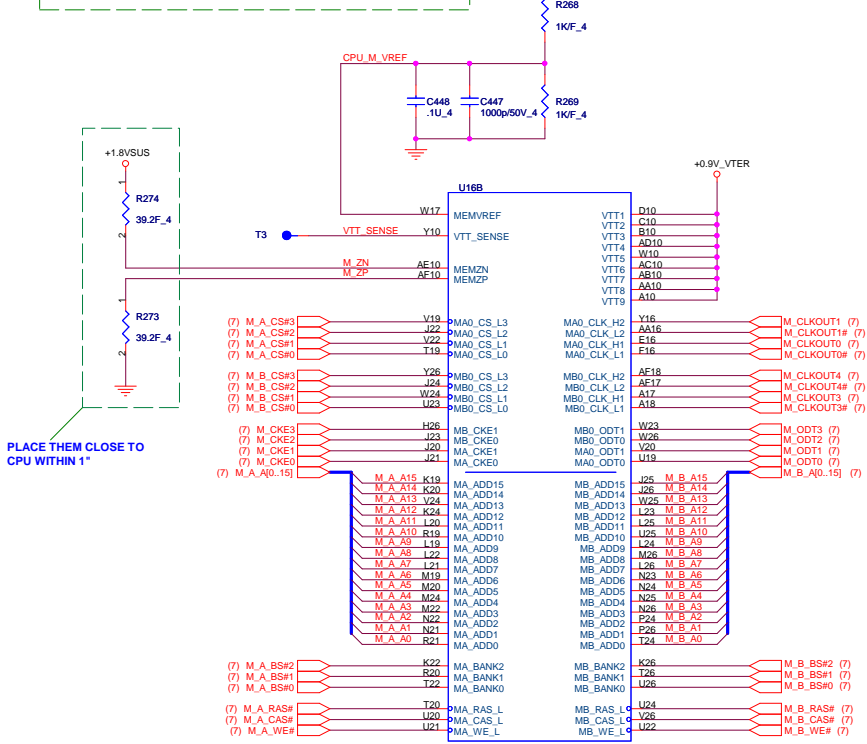
LAYOUT: Place bypass cap on topside of board
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDT0 POWER PINS

PROJECT : ZR3
Quanta Computer Inc

Size	Document Number	Rev
	ATHLON64 HT I/F	1A
Date:	Wednesday, October 18, 2006	Sheet of 31

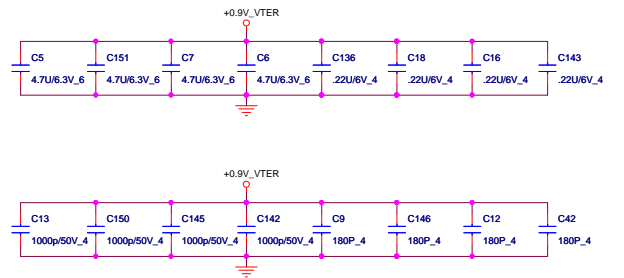
hexainfo@hotmail.com

VDD_VTT_SUS_CPU is CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

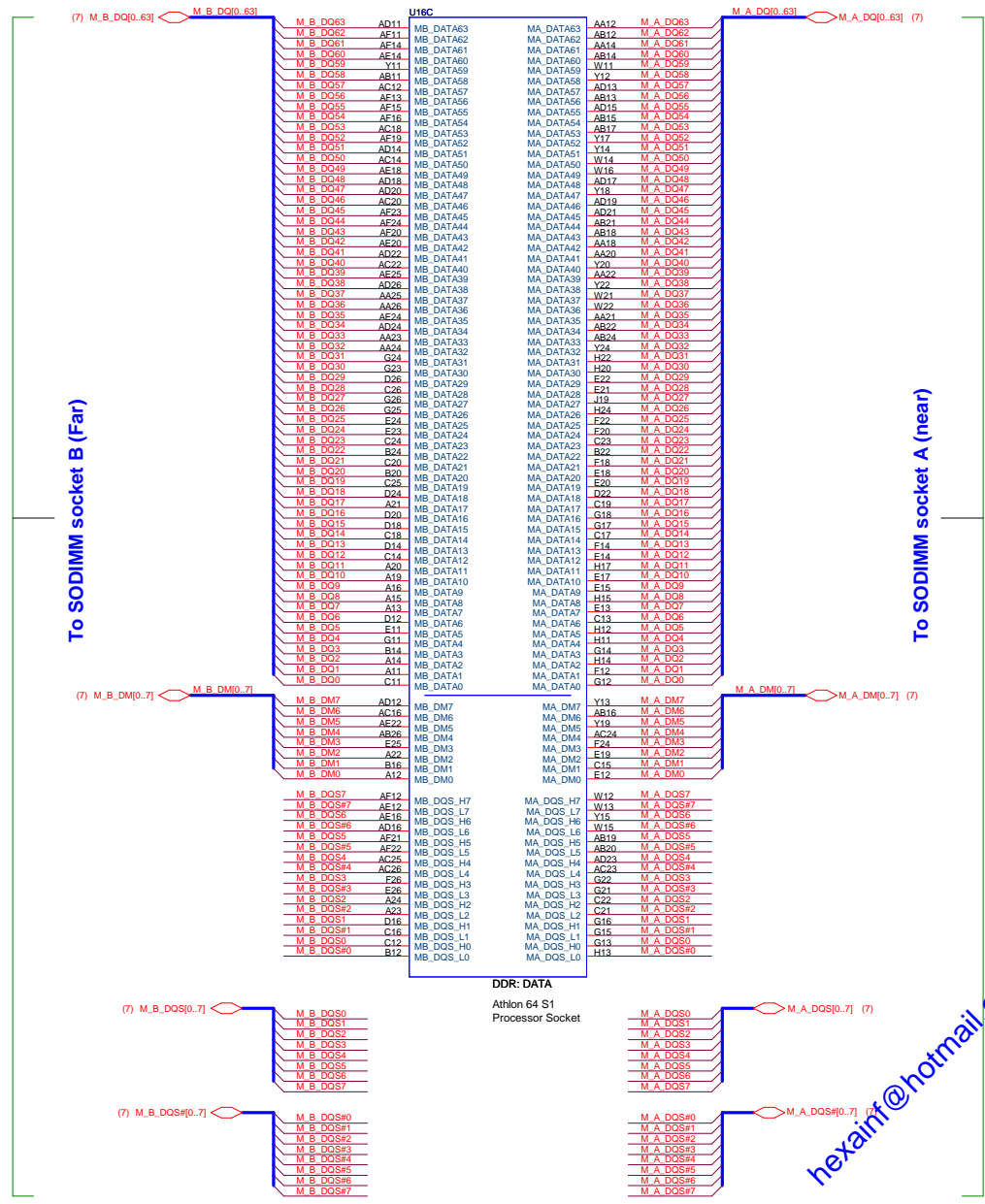


PLACE THEM CLOSE TO CPU WITHIN 1"

DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket



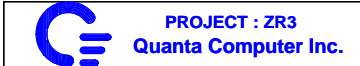
Processor DDR2 Memory Interface



To SODIMM socket B (Far)

To SODIMM socket A (near)

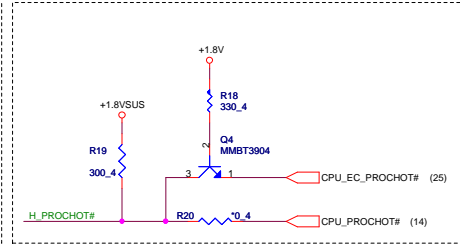
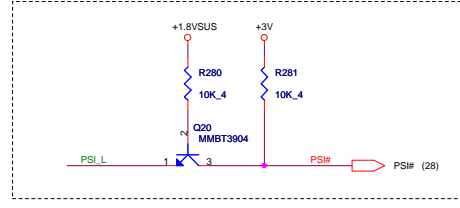
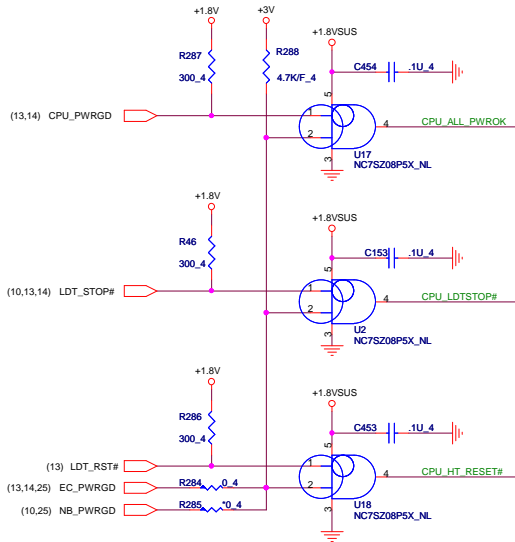
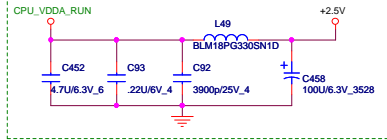
Athlon 64 S1
Processor Socket



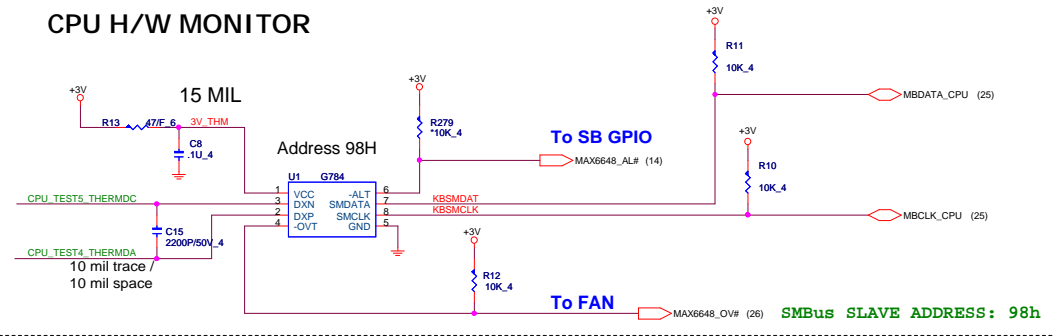
hexairf@hotmail.com

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN



CPU H/W MONITOR

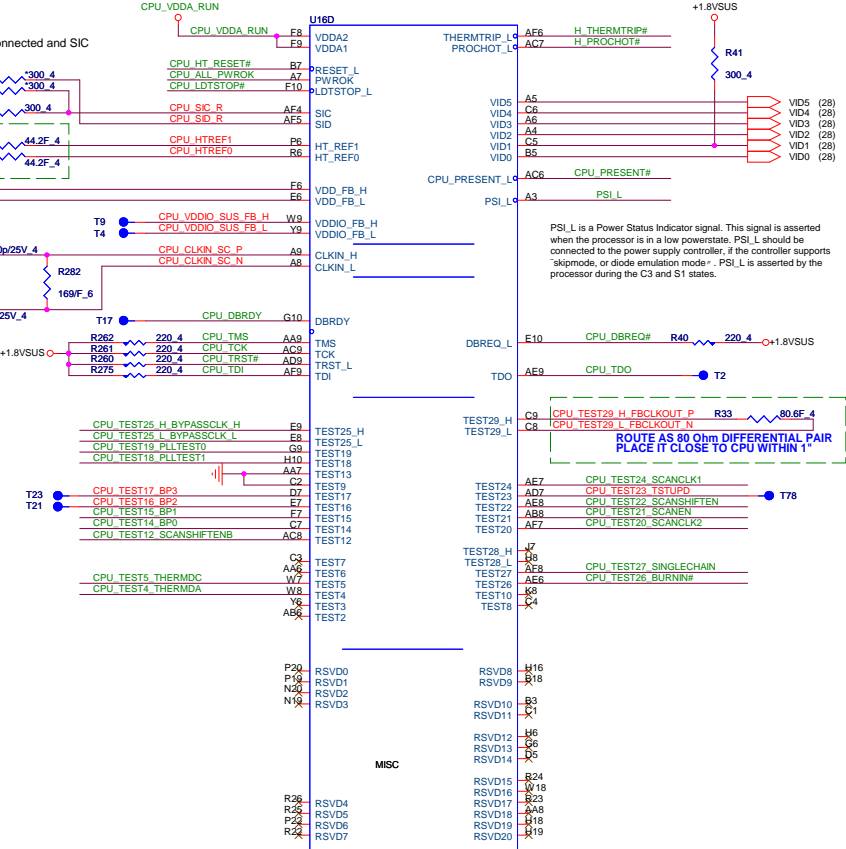


ATHLON Control and Debug

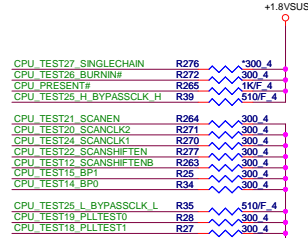
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- (± 5%) pull-down to VSS.

Place them to CPU within 1"

To Power (28) COREFB+V (28) COREFB-

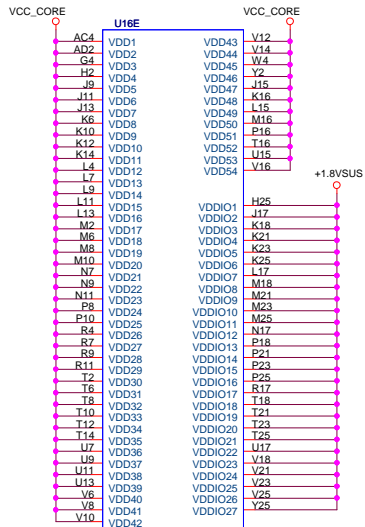


AMD NPT S1 SOCKET Processor Socket

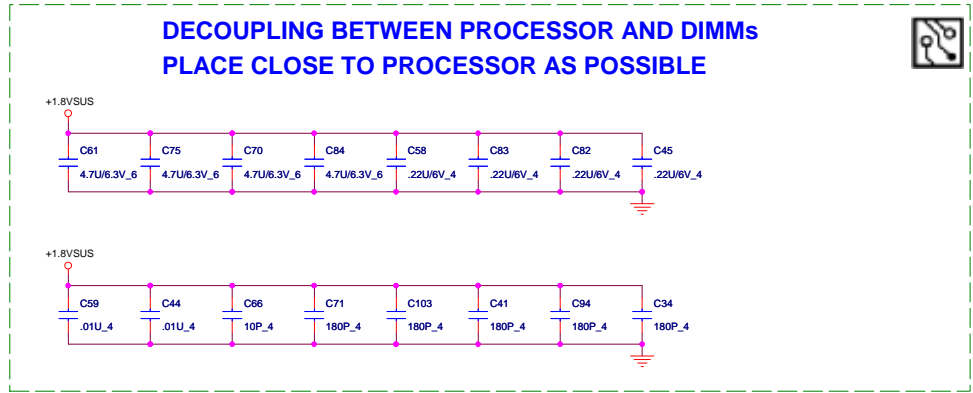
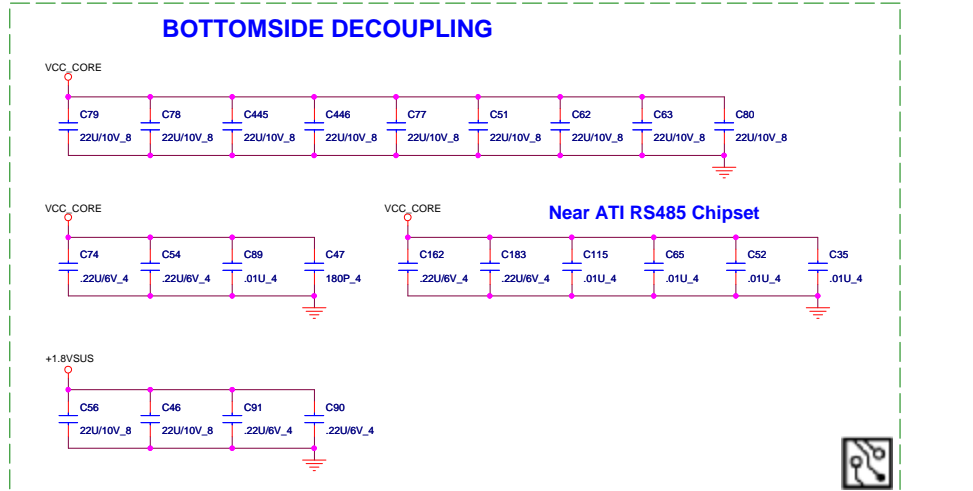
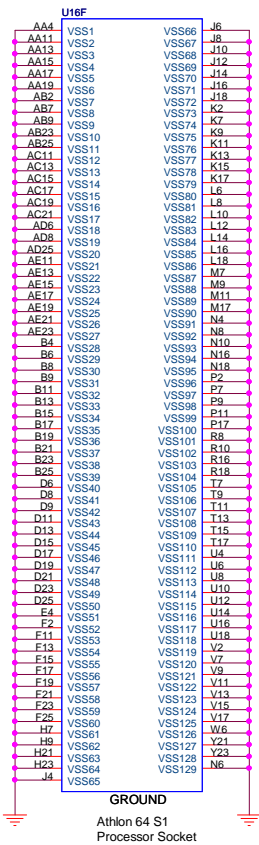


If no use which Net need pull-up or down

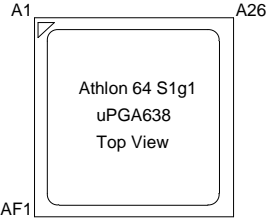
hexainf@hotmail.com

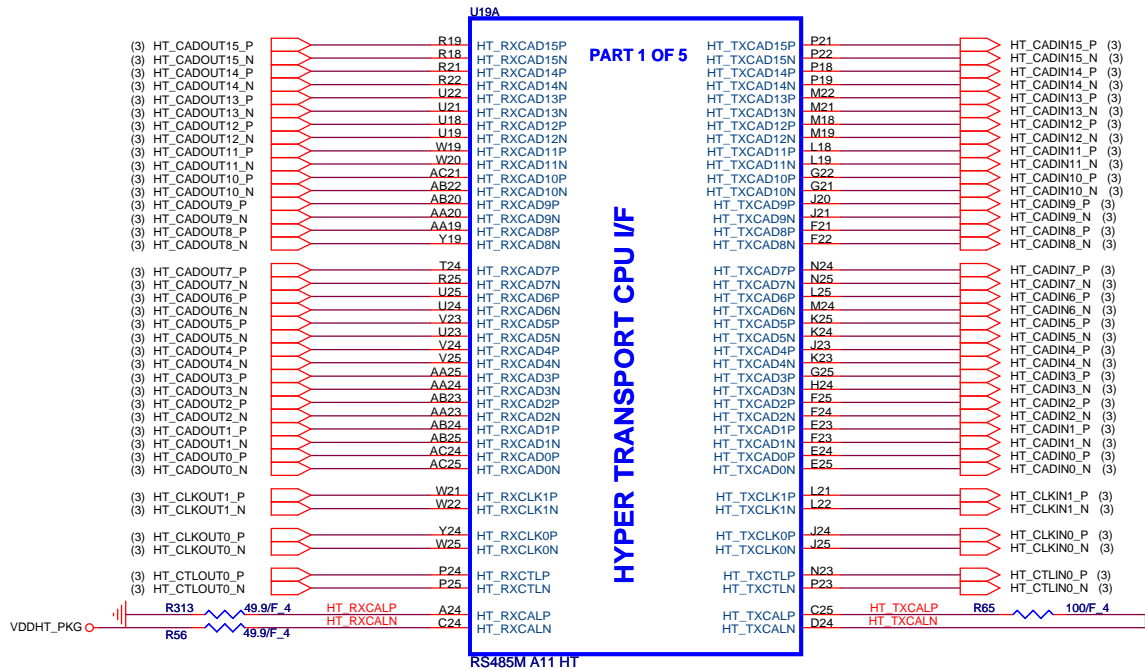



POWER
Athlon 64 S1
Processor Socket



PROCESSOR POWER AND GROUND






PROJECT : ZR3
Quanta Computer Inc.

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	RS485-HT LINK0 I/F	1A
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WLAN MINI CARD

(20) MINI_PCIE_RXP0
(20) MINI_PCIE_RXN0

T31

T83

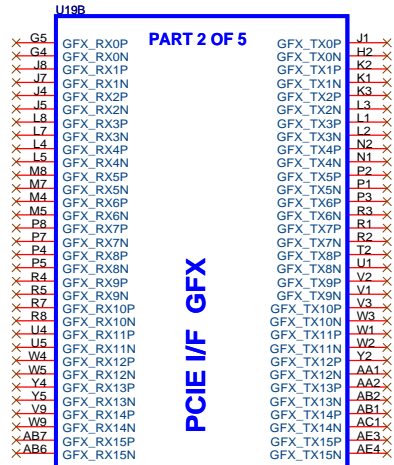
(13) A_RX0P
(13) A_RX0N

(13) A_RX1P
(13) A_RX1N

R43 10K 6
R37 8.25K/F 6

R27: 10KOhm FOR RS485
1.47KOhm FOR RS690

R29: 8.25KOhm FOR RS485
DNI FOR RS690



PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB



Place these caps close to connector

AD8 GPP_TX0P C C126 .1U 4
AE8 GPP_TX0N C C122 .1U 4

AD7 GPP_TX1P T84
AE7 GPP_TX1N T82

~~AD4~~ GPP_TX2P
~~AE5~~ GPP_TX2N

~~AD5~~ GPP_TX3P
~~AD6~~ GPP_TX3N

AE9 A_TX0P C C120 .1U 4
AD10 A_TX0N C C121 .1U 4

AC8 A_TX1P C C139 .1U 4
AD9 A_TX1N C C140 .1U 4

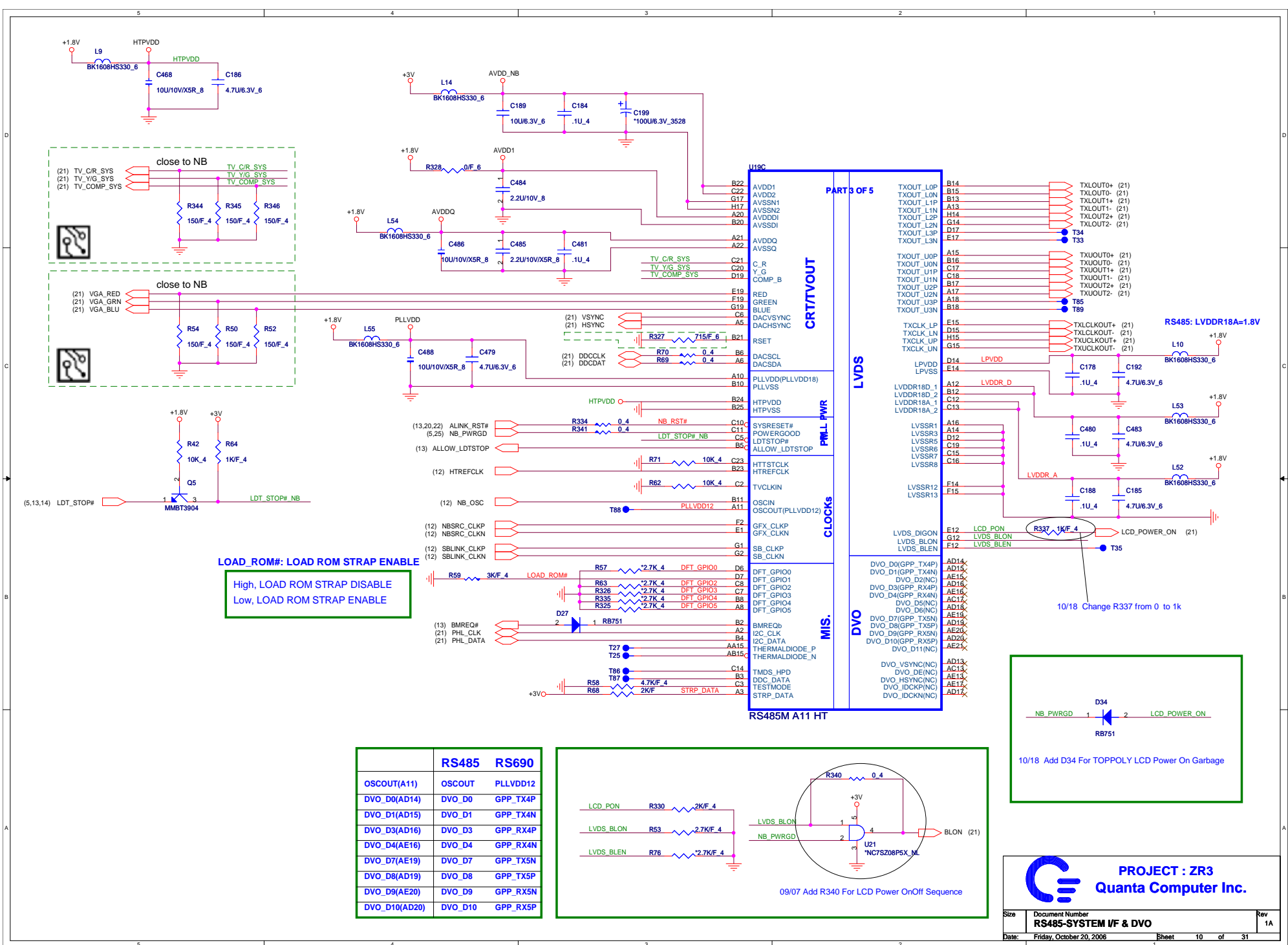
AD11 PCE_PCAL R36 150F 6
AE11 PCE_NCAL R38 100F 6

R28: 150 Ohm FOR RS485
562 Ohm FOR RS690
R26: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690

RS485M A11 HT

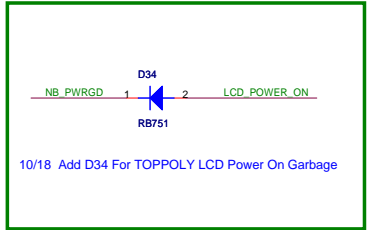
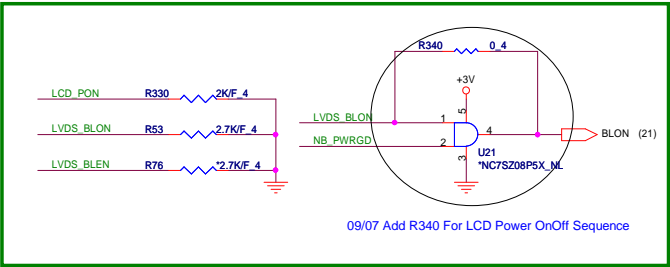
PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-PCIE LINK I/F	1A
Date:	Wednesday, October 18, 2006	Sheet 9 of 31



LOAD_ROM#: LOAD ROM STRAP ENABLE
 High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

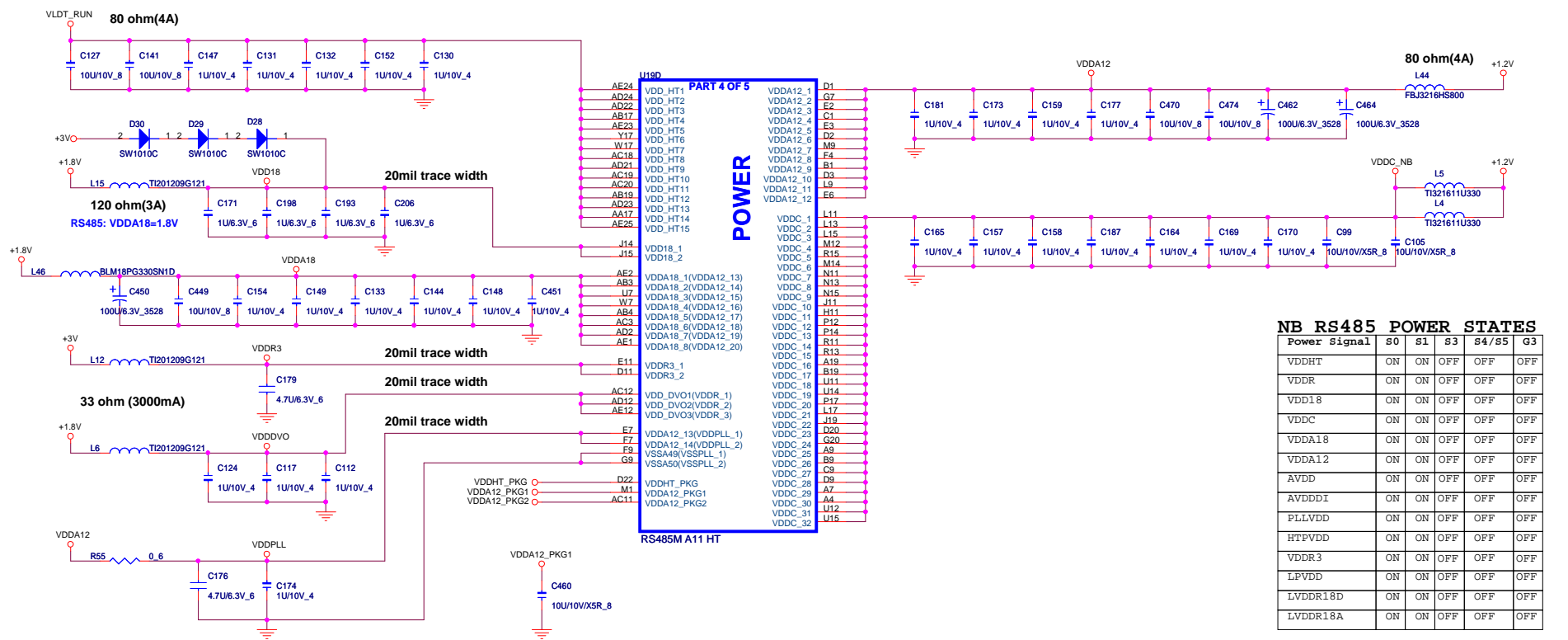
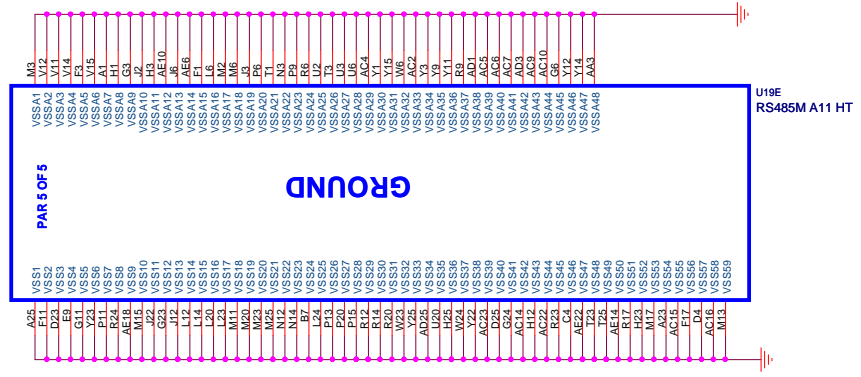
	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P



PROJECT : ZR3
Quanta Computer Inc.

Size: Document Number
RS485-SYSTEM I/F & DVO Rev: 1A

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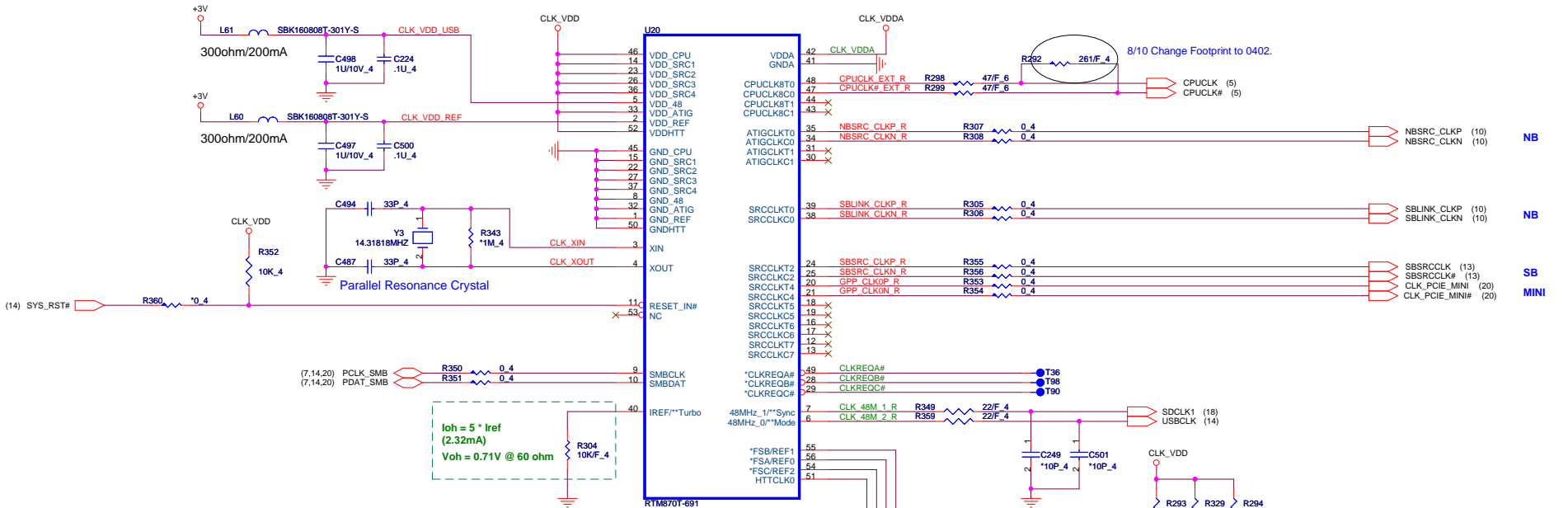
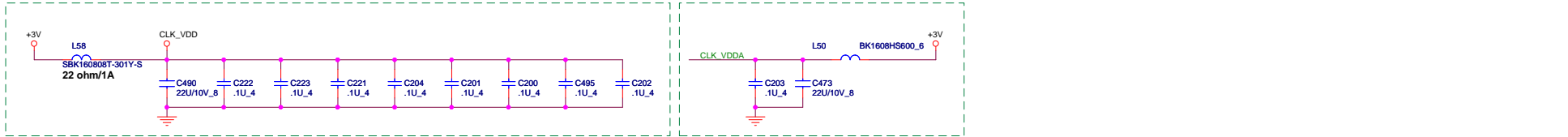


NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

PROJECT : ZR3
Quanta Computer Inc.

Size: Document Number **RS485-POWER** Rev: 1A
 Date: Wednesday, October 18, 2006 Sheet: 11 of 31

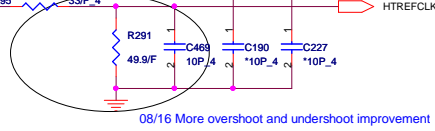
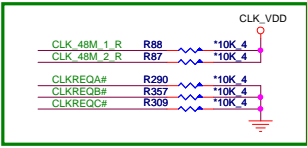


Note: * internal 150K pull up ,
** internal 150K pull down

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	HTT	SRC	ATIG	USB1	SSC
0	0	0	266.67	66.66	100	100	48.00	+/- 0.25%
0	0	1	133.33	66.66	100	100	48.00	+/- 0.25%
0	1	0	200.00	66.66	100	100	48.00	+/- 0.25%
0	1	1	166.67	66.66	100	100	48.00	+/- 0.25%
1	0	0	333.33	66.66	100	100	48.00	+/- 0.25%
1	0	1	100.00	66.66	100	100	48.00	+/- 0.25%
1	1	0	400.00	66.66	100	100	48.00	+/- 0.25%
1	1	1	200.00	66.66	100	100	48.00	+/- 0.25%

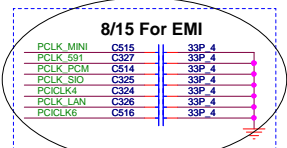
Check AMD clock



08/16 More overshoot and undershoot improvement

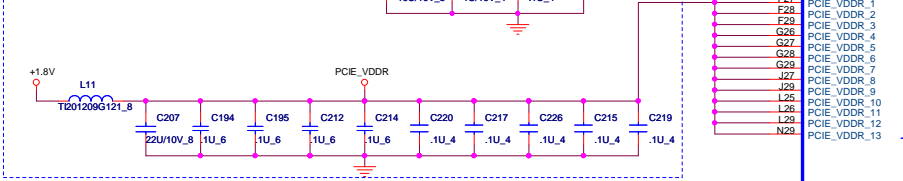
PROJECT : ZR3
Quanta Computer Inc.

Size Document Number
EXTERNAL CLOCK GENERATOR
 Date: Wednesday, October 18, 2006 Sheet 12 of 31 Rev 1A



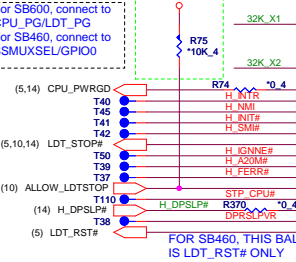
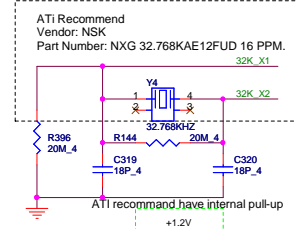
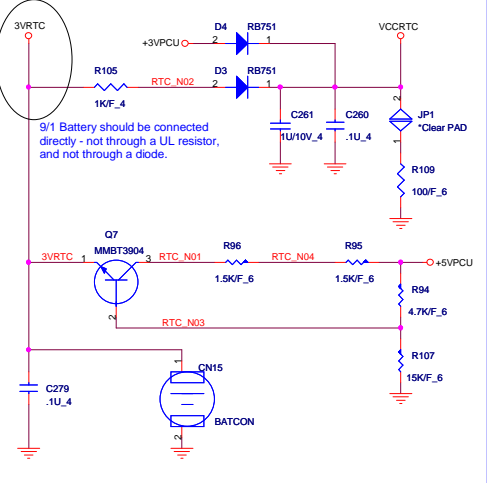
SB CALIBRATION RESISTOR VALUE			
R?	SB600	SB460	
R?	562 OHM 1%	150 OHM 1%	
R?	2.05K 1%	150 OHM 1%	
R?	0 ohm	4.12K 1%	

PCI Express Power



CLG

RTC



SB460 SB 27x27mm Part 1 of 4

PCI CLKS

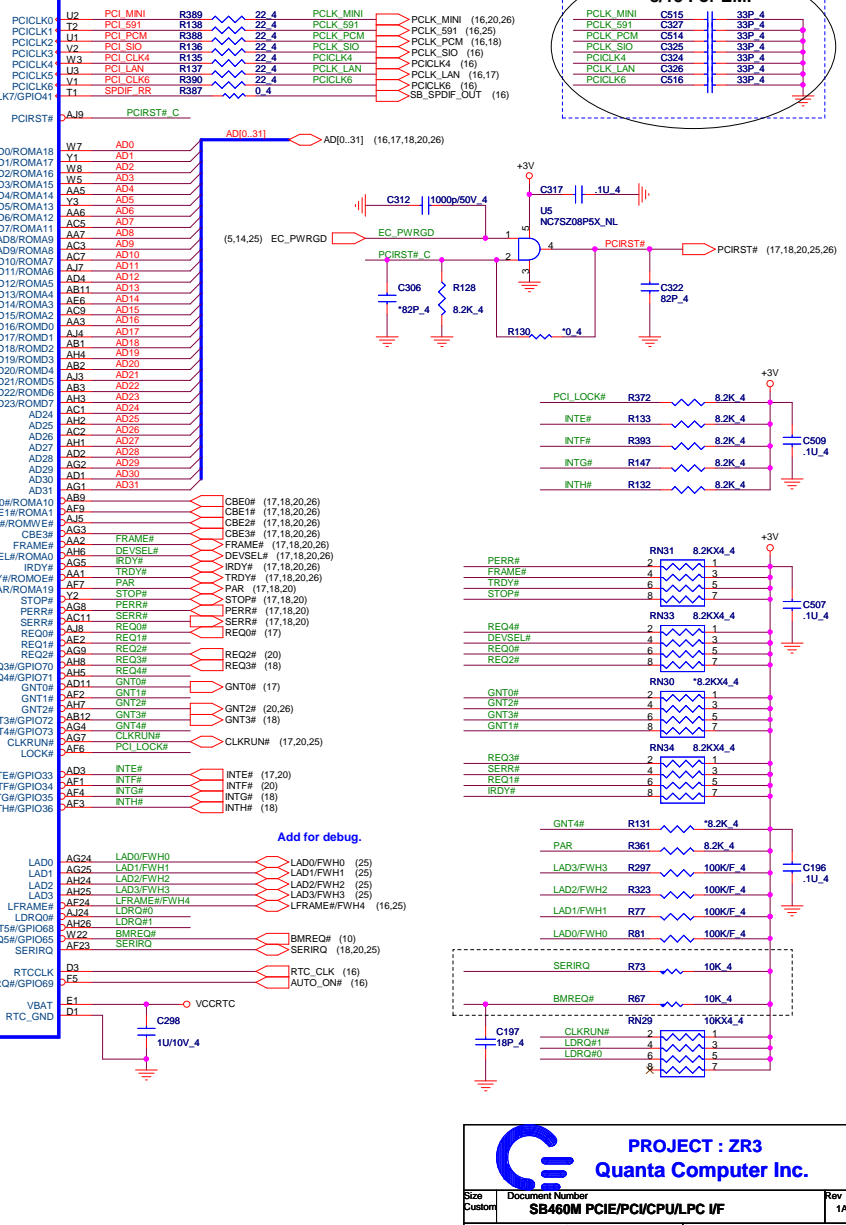
PCI EXPRESS INTERFACE

PCI INTERFACE

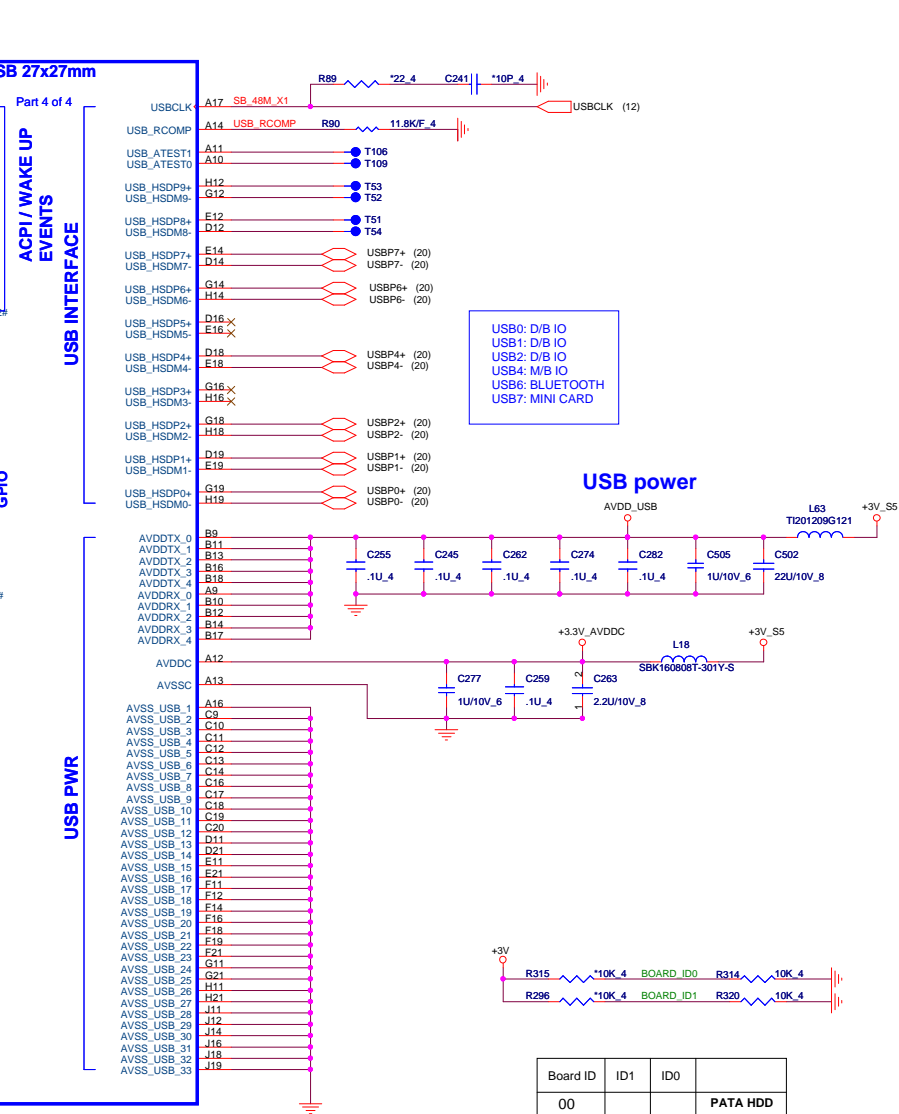
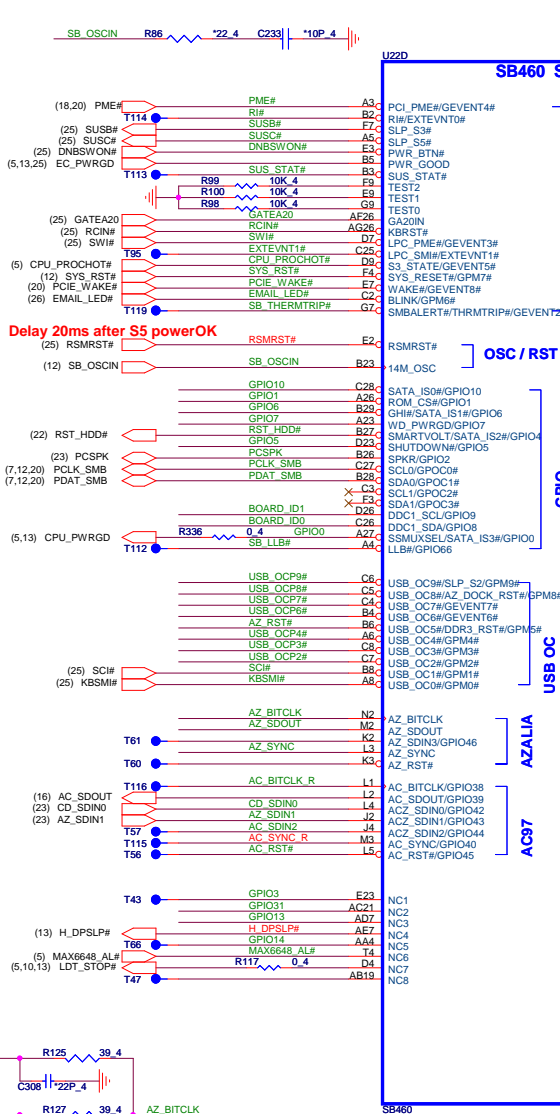
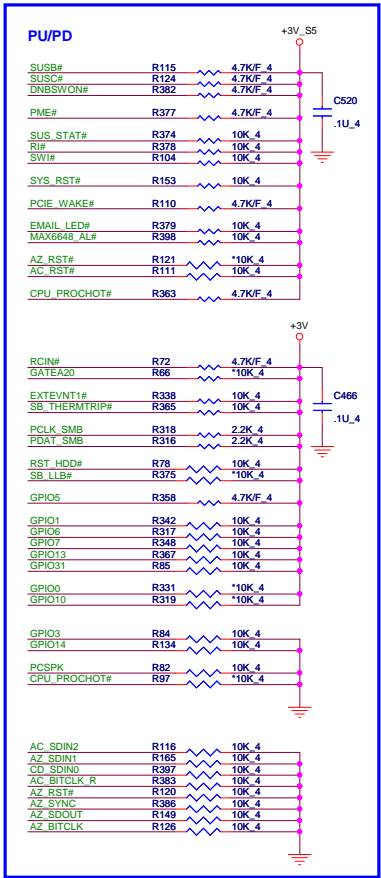
LPC

CPU

RTC

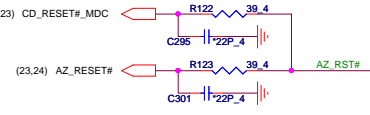
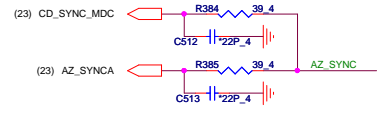
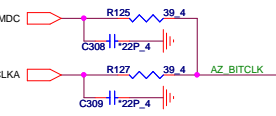
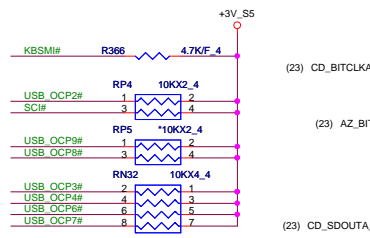


PROJECT : ZR3
Quanta Computer Inc.



USB0: D/B IO
 USB1: D/B IO
 USB2: D/B IO
 USB4: M/B IO
 USB6: BLUETOOTH
 USB7: MINI CARD

USB power use S3 power, But Over current signal datasheet is S5 only, But ATI FAE say use S3 is ok



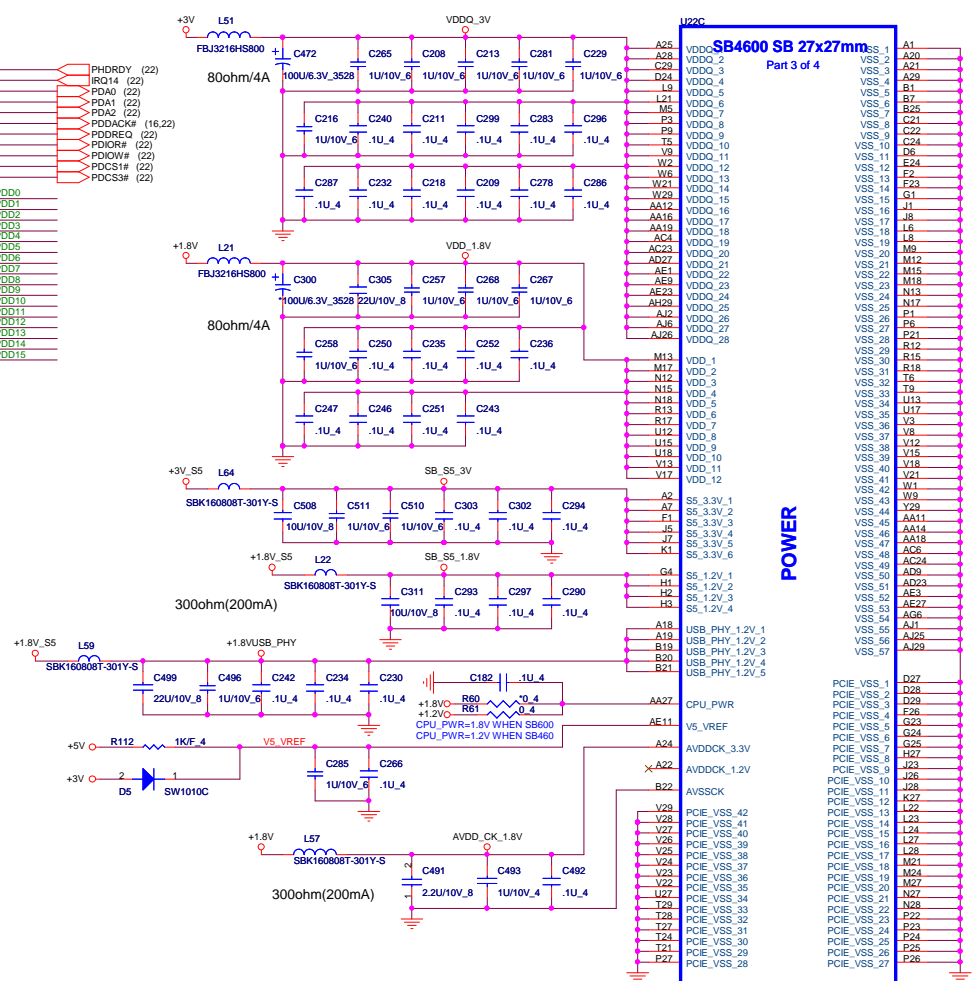
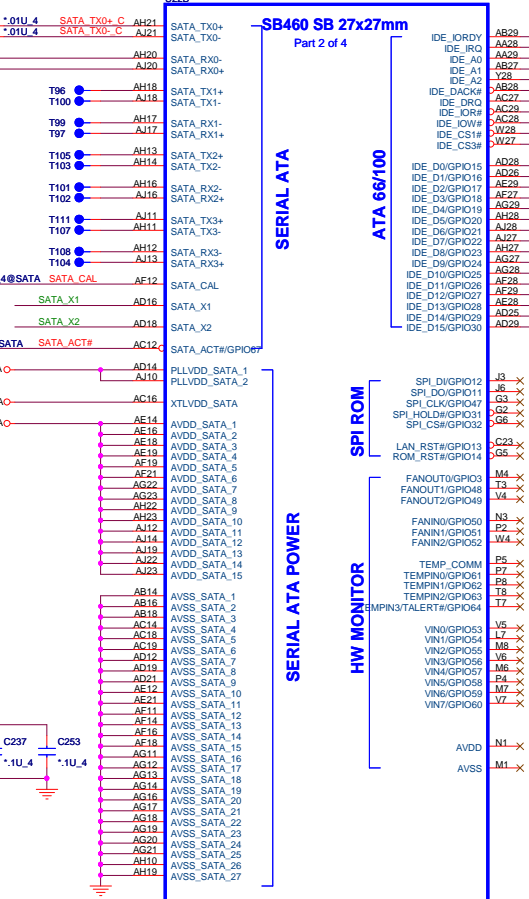
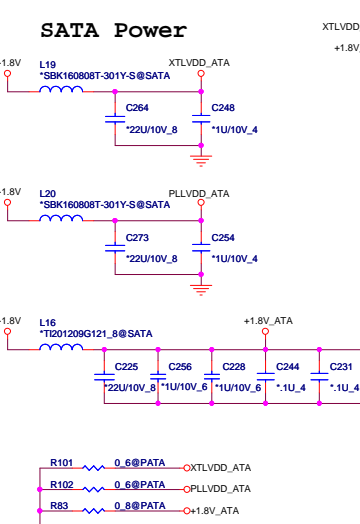
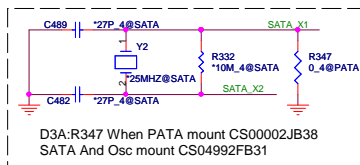
Board ID	ID1	ID0	
00			PATA HDD
01			SATA HDD
10			
11			



09/07 Stuff C329,C328 to 33P For EMI Situation.

PROJECT : ZR3
Quanta Computer Inc.

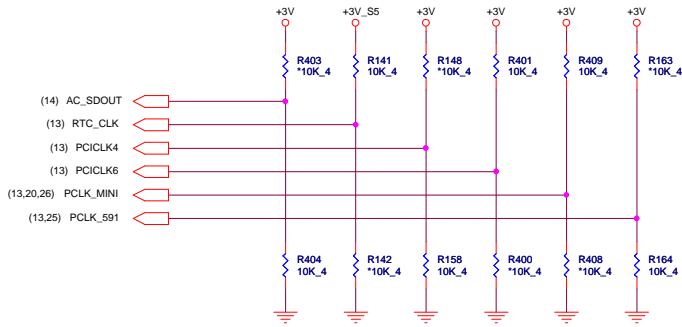
Size: Document Number
 Custom: SB460M ACPI/GPIO/USB/AC97
 Date: Wednesday, October 18, 2006 Sheet 14 of 31



CLG

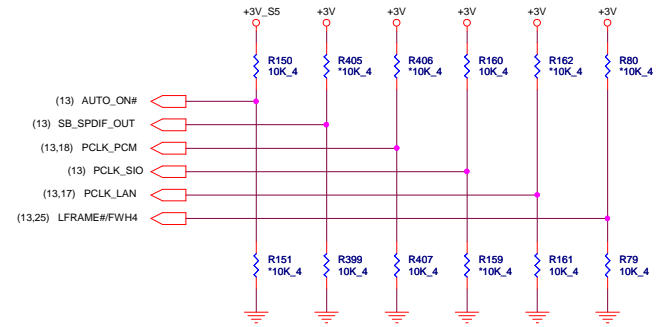
PROJECT : ZR3
Quanta Computer Inc.

Size Custom	Document Number SB460M HDD/POWER/DECOUPLING	Rev 1A
Date:	Wednesday, October 18, 2006	Sheet 15 of 31



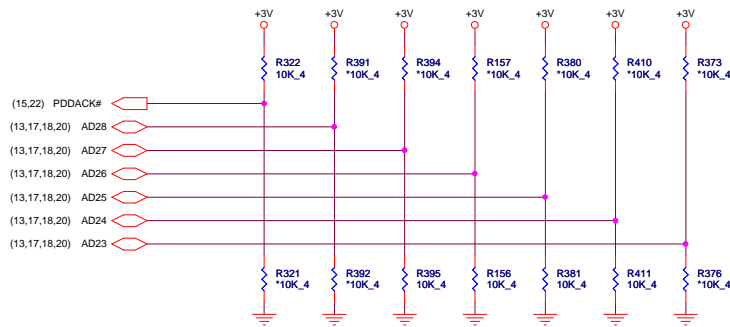
REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI	PCLK_591
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	L, L = FWH ROM NOTE: FOR SB460, PCI_CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]	



	AUTO_ON#	SB_SPDIF_OUT	TPCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET HIGH	ENABLE THERMTRIP#
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HLOW DEFAULT	DISABLE THERMTRIP# DEFAULT

BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

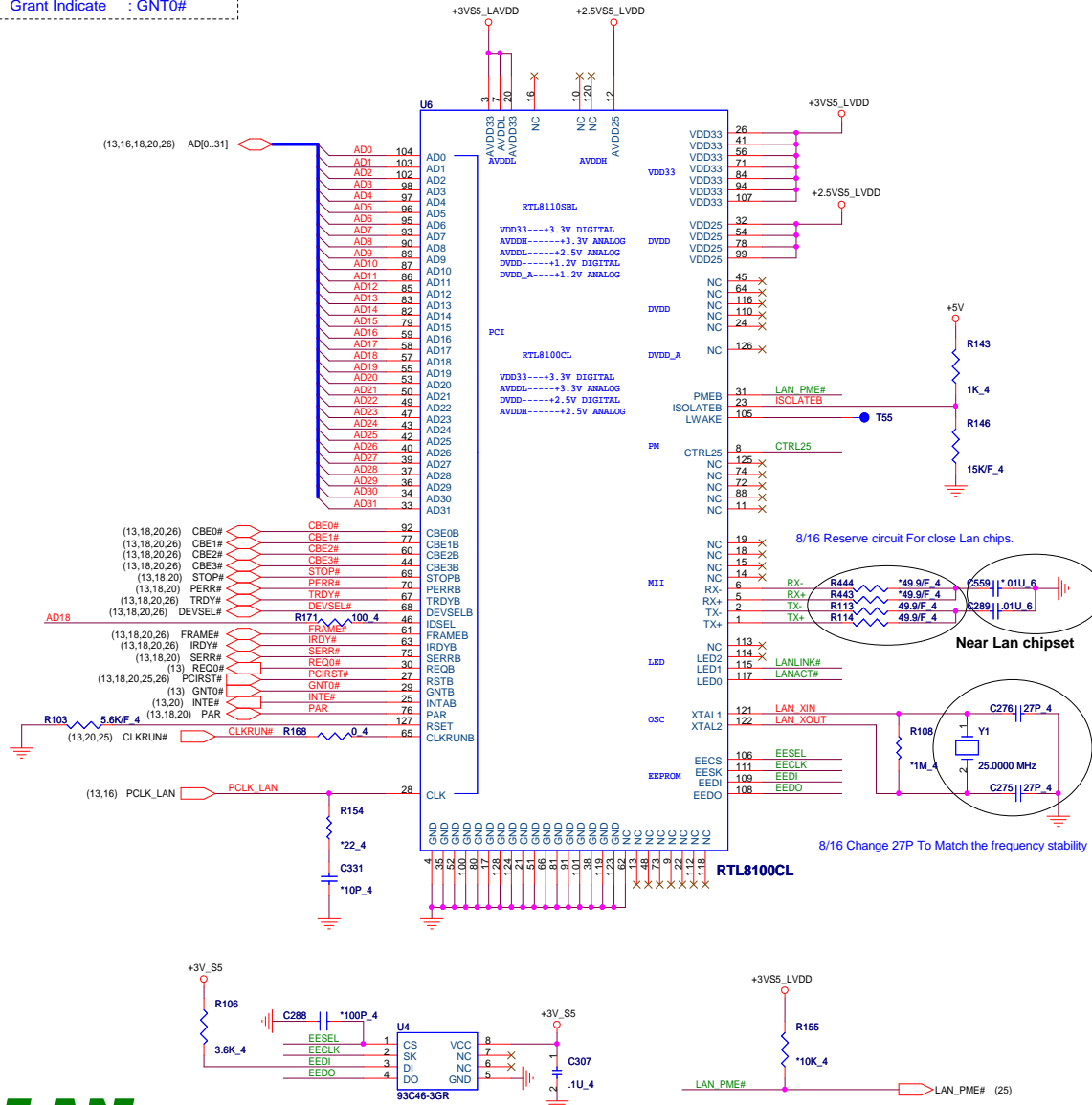
	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

CLG

PROJECT : ZR3
Quanta Computer Inc.

Size Custom	Document Number SB460M STRAPS	Rev 1A
Date: Wednesday, October 18, 2006 Sheet 16 of 31		

ID Select : AD18
 Interrupt Pin : INTF#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#

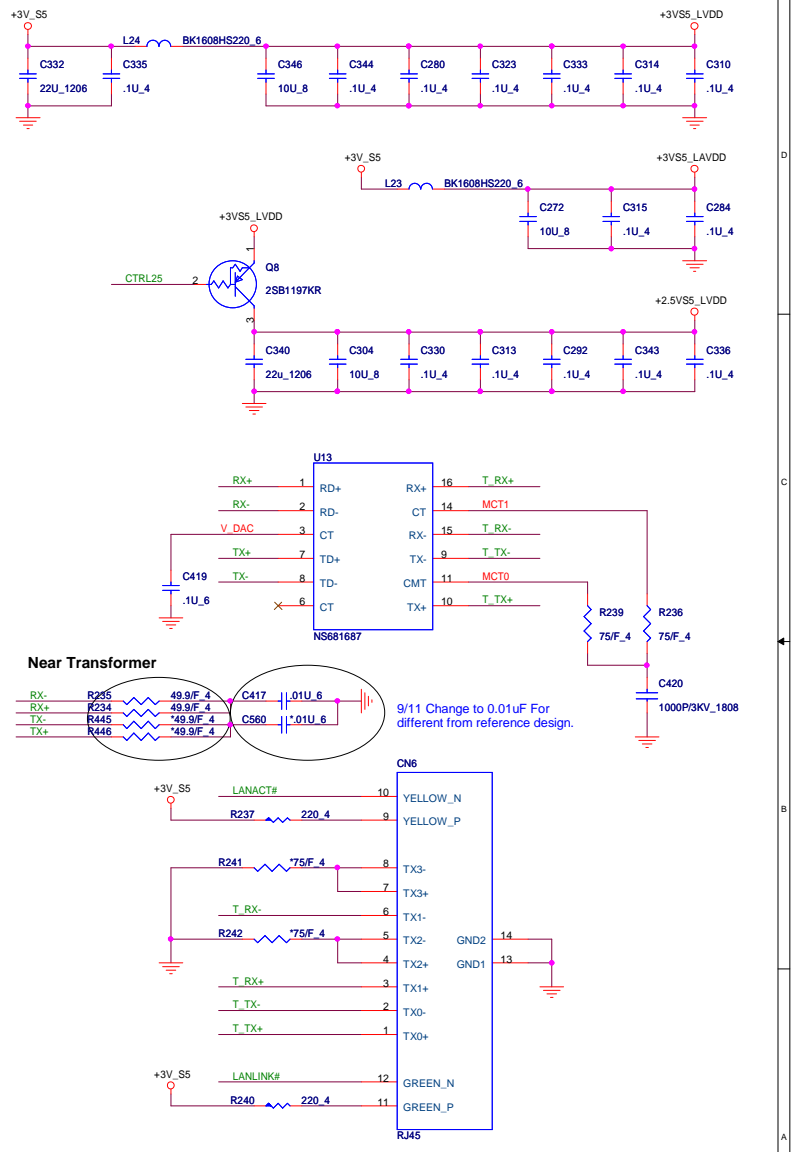


8/16 Reserve circuit for Close Lan chips.

Near Lan chipset

8/16 Change 27P To Match the frequency stability

LAN



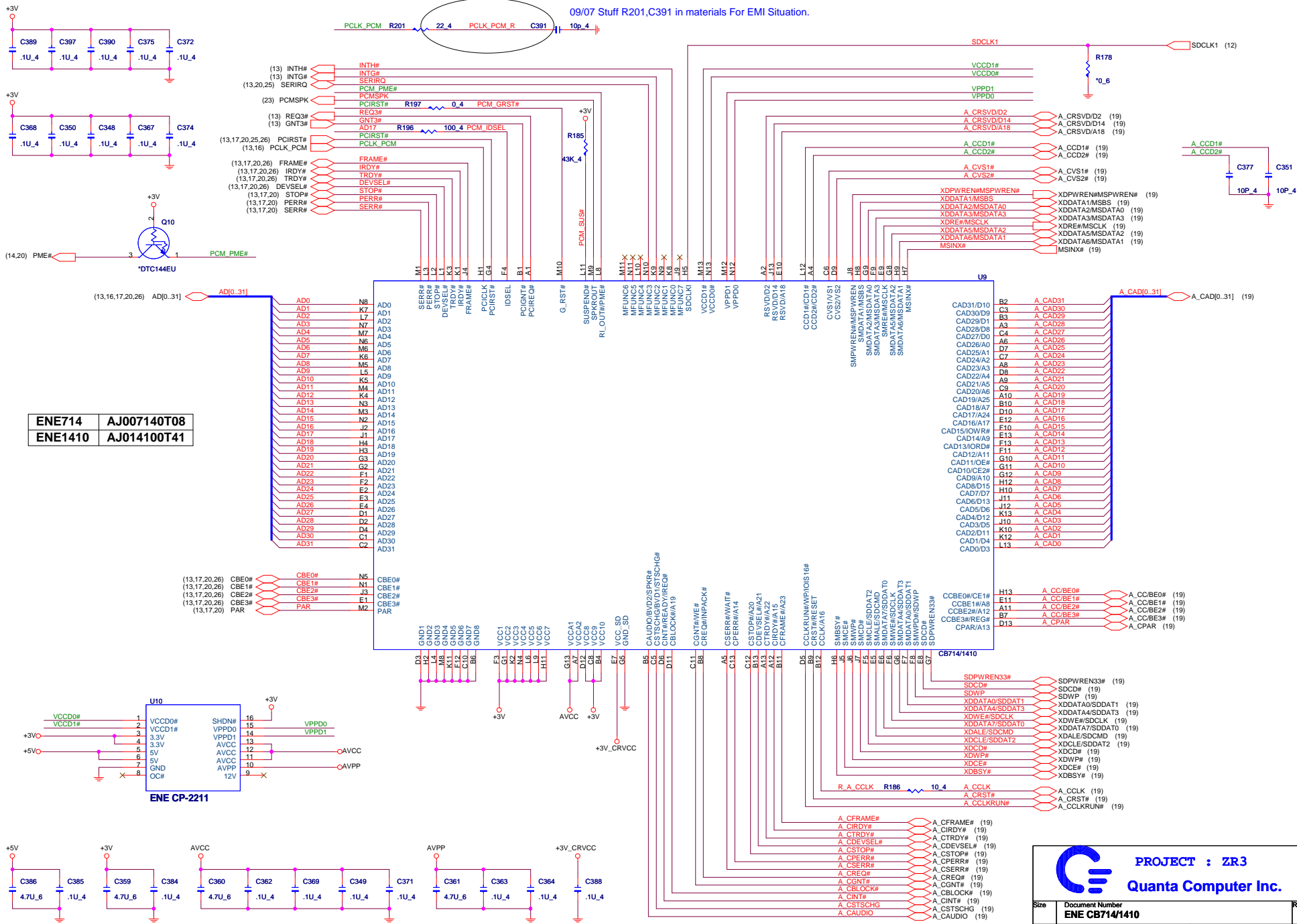
Near Transformer

9/11 Change to 0.01uF For different from reference design.

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
Date:	LAN RTL810SBL/8100CL	1A
Date:	Wednesday, October 18, 2006	Sheet 17 of 31

09/07 Stuff R201,C391 in materials For EMI Situation.

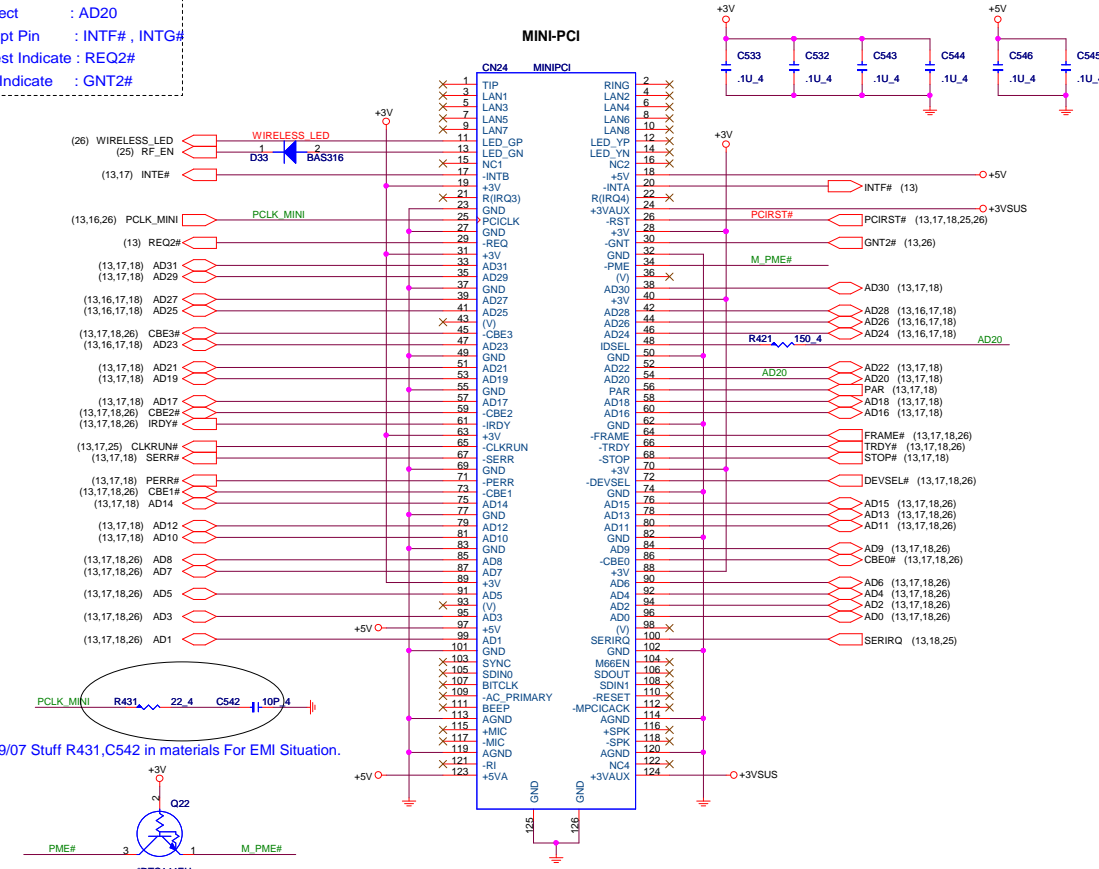


ENE714	AJ007140T08
ENE1410	AJ014100T41

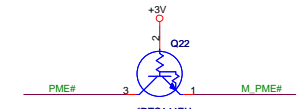
PROJECT : ZR3
Quanta Computer Inc.

Size: Document Number: **ENE CB714/1410** Rev 1A
 Date: Wednesday, October 18, 2006 Sheet 18 of 31

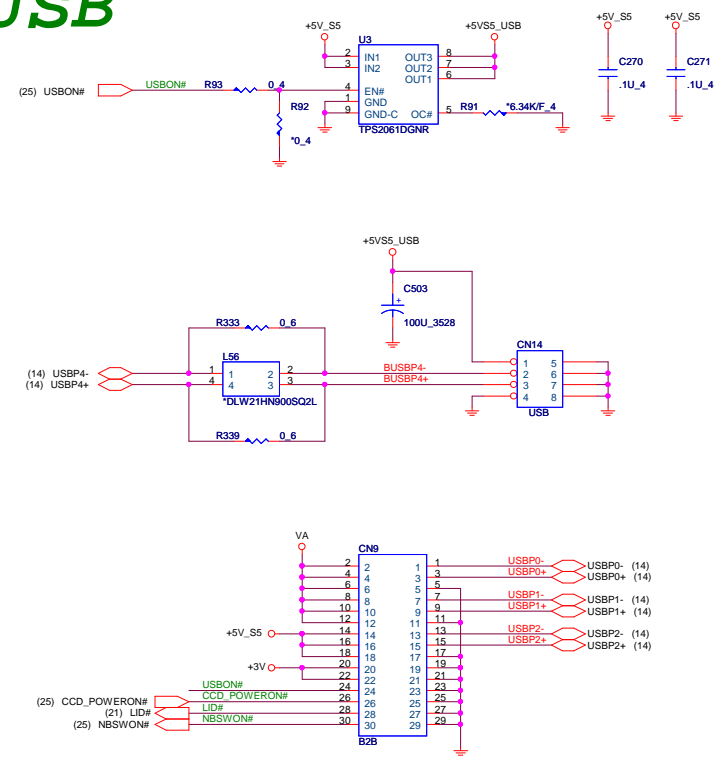
ID Select : AD20
 Interrupt Pin : INTF#, INTG#
 Request Indicate : REQ2#
 Grant Indicate : GNT2#



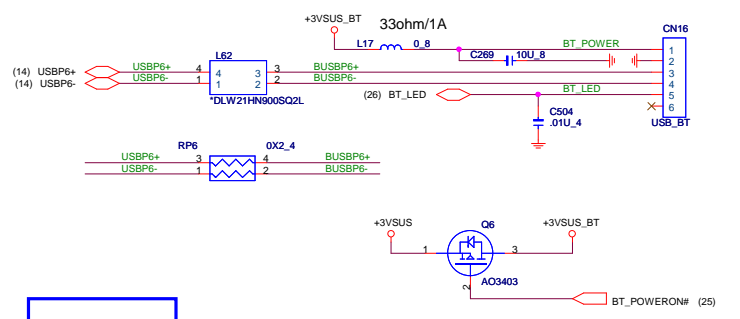
09/07 Stuff R431,C542 in materials For EMI Situation.



USB

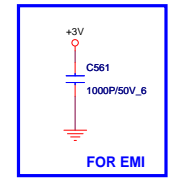


BLUETOOTH MODULE CONNECTOR



MPC

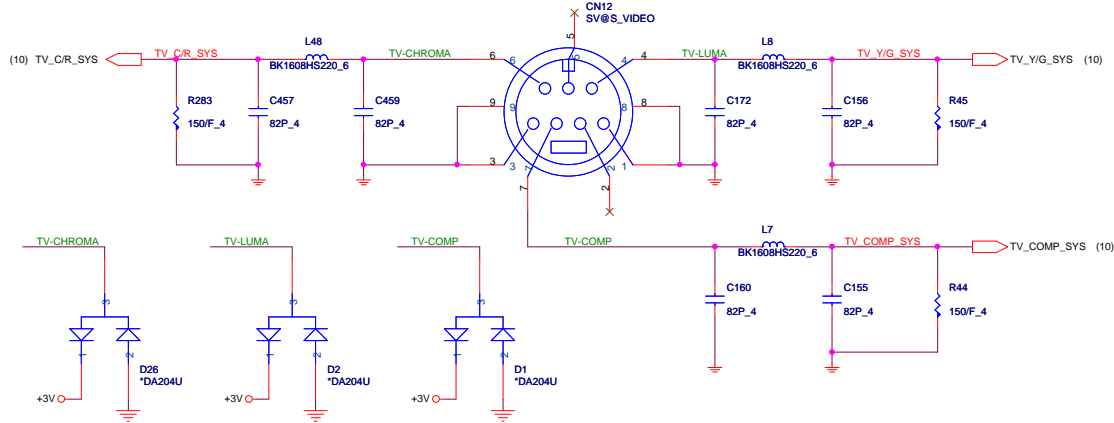
Close Minicard connector



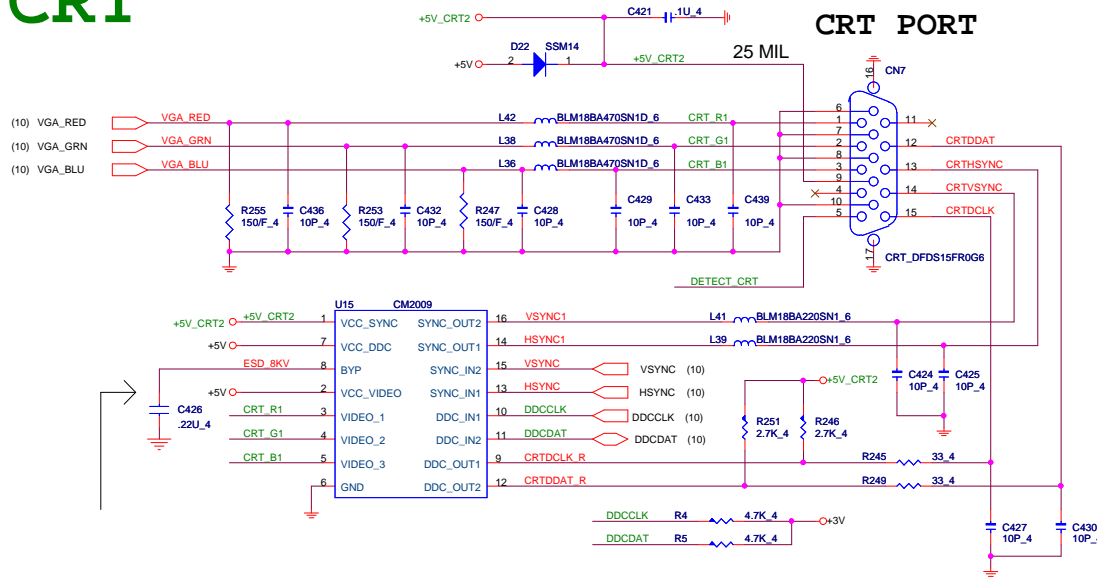
PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI&PCI-E,USB PORT	1A
Date:	Wednesday, October 18, 2006	Sheet 20 of 31

S-VIDEO



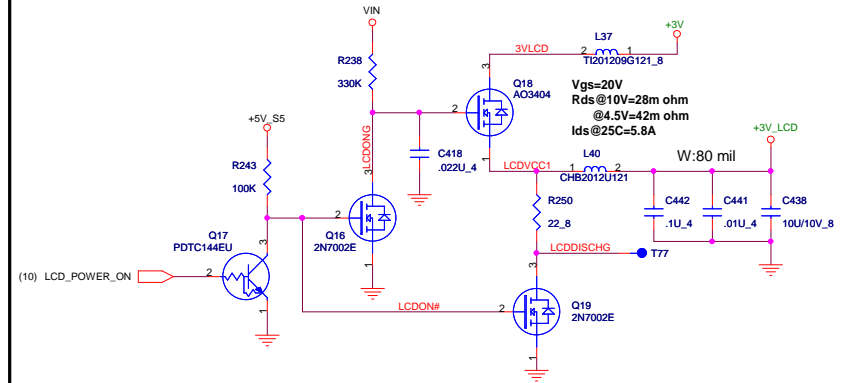
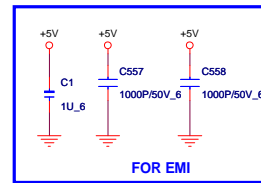
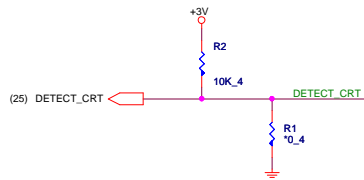
CRT



increase capability of ESD, from +4KV improve to +8KV.

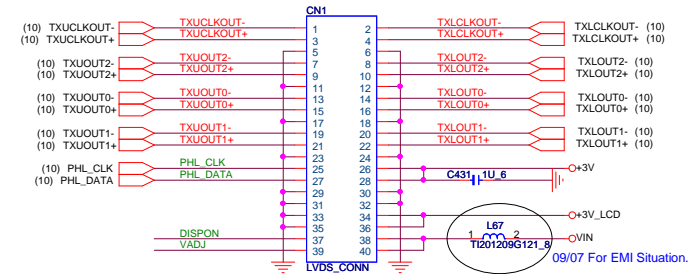
System Auto Detect External CRT Device

	R247	R248	R249
Enable	Not stuffed	Stuffed	Stuffed
Disable (Default)	Stuffed	Not stuffed	Stuffed

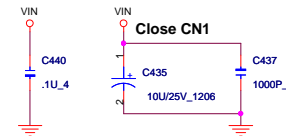
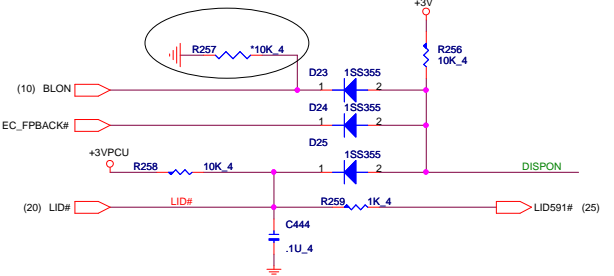


LVDS

LCD Connector



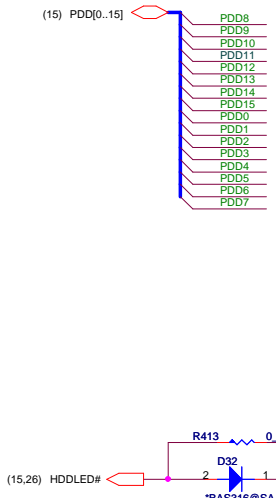
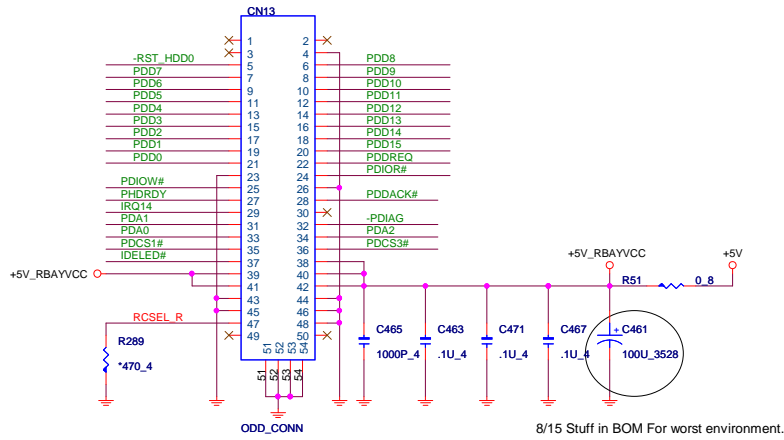
09/11 Del R257 For LCD Power On/Off Sequence



PROJECT : ZR3
Quanta Computer Inc.

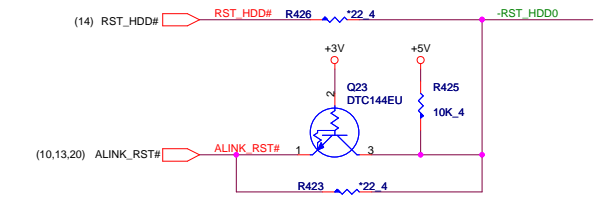
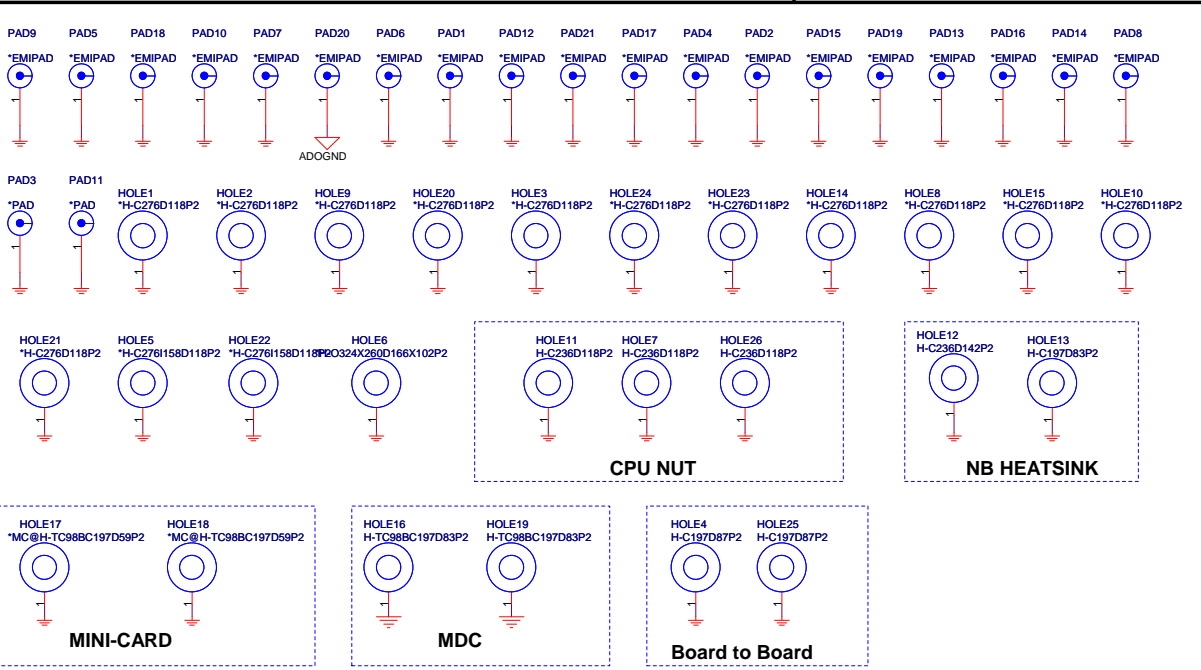
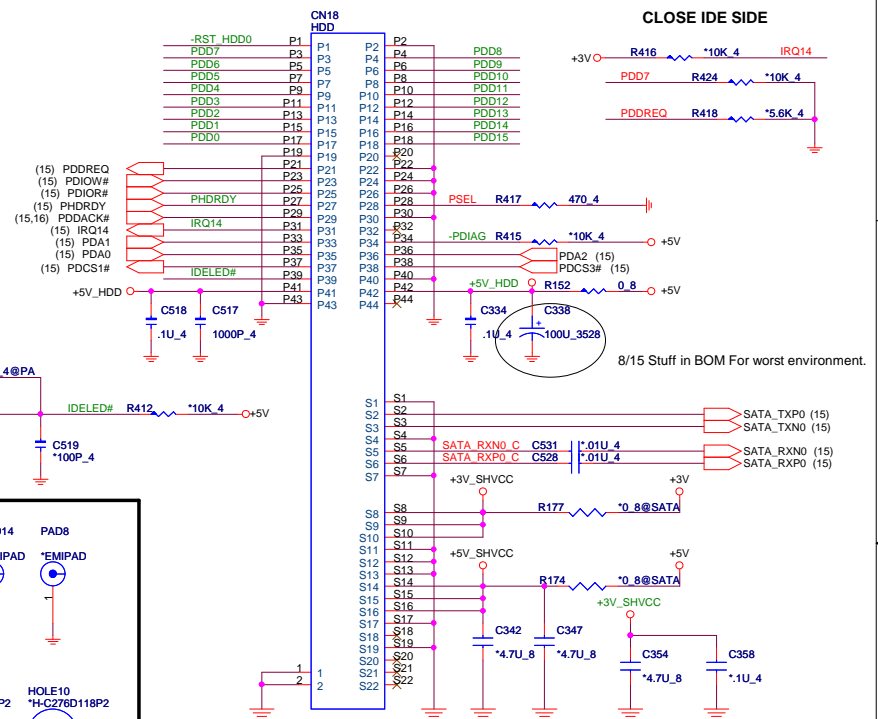
Size	Document Number	Rev
	CRT & LVDS & S-Video	1A
Date:	Wednesday, October 18, 2006	Sheet 21 of 31

ODD CONN



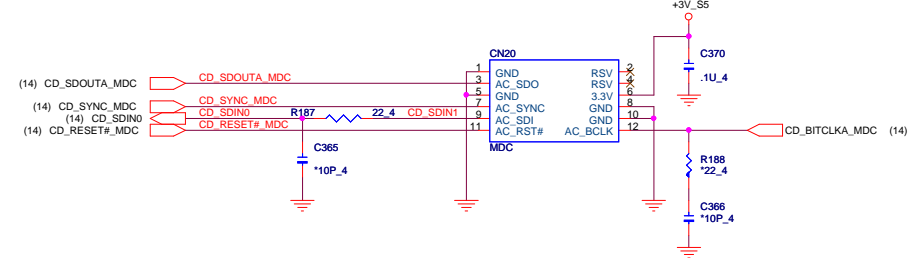
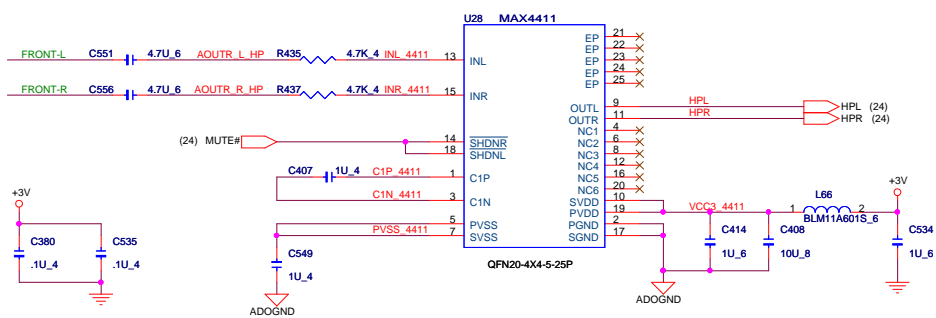
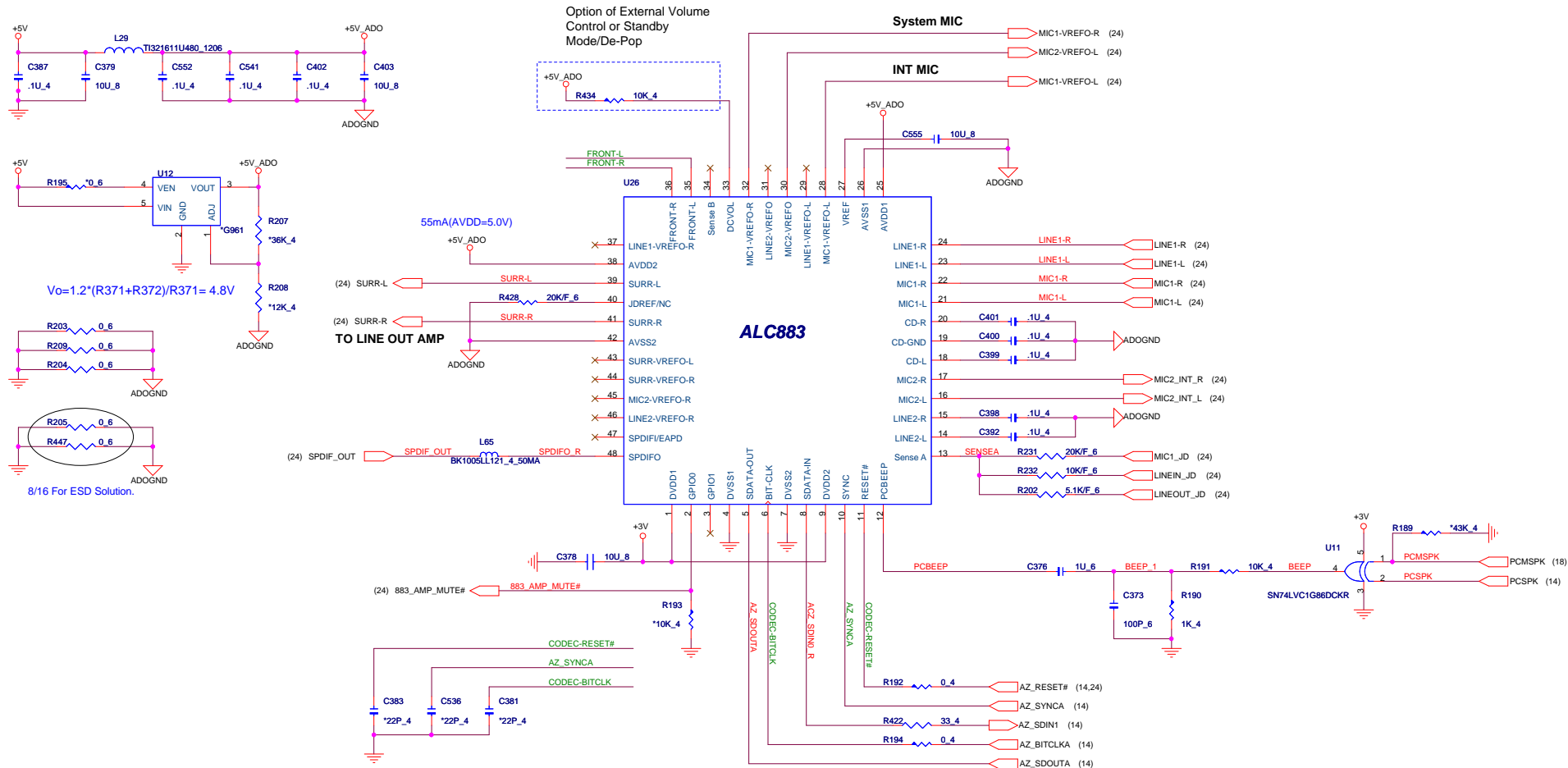
PATA DFHS44FRD28
SATA DFHS22FRA03

HDD CONN

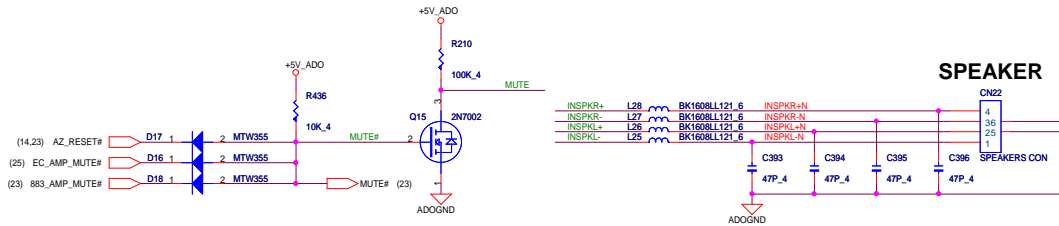
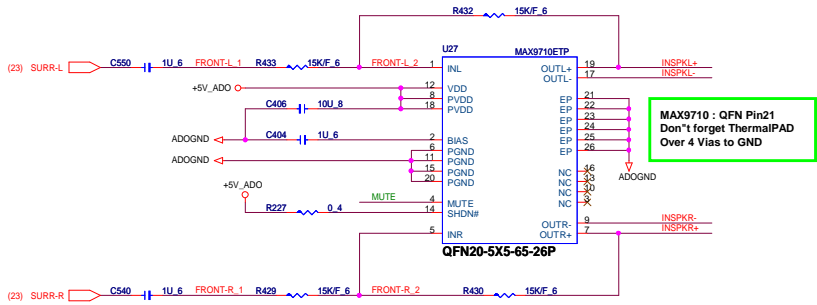


PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM & HOLES	1A
Date:	Wednesday, October 18, 2006	Sheet 22 of 31

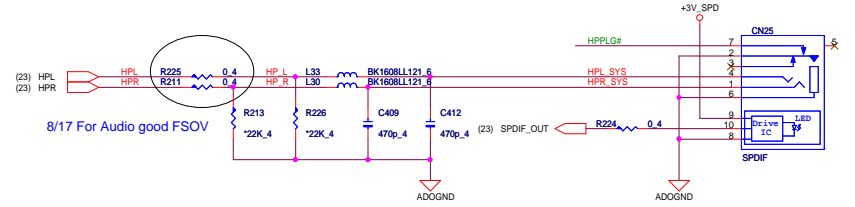


Speaker Amplifier MAX9710

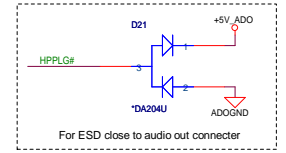
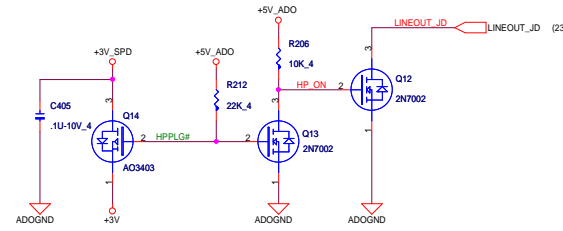


SYSTEM LINE OUT/SPDIF

BLACK

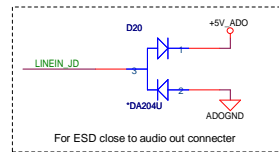
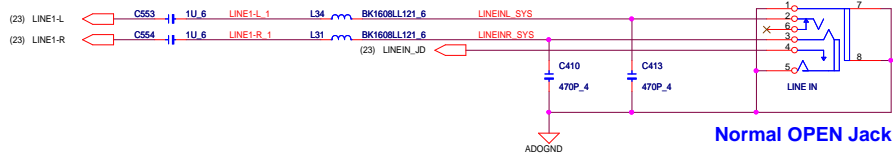


LINEOUT_JD:
HP not insert->H
HP insert->L



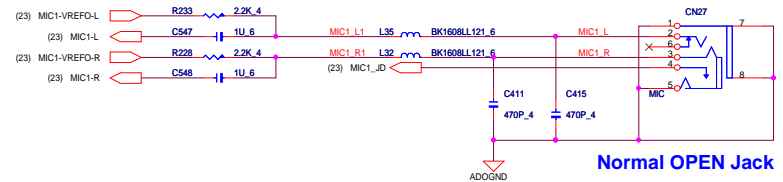
SYSTEM LINE IN

BLUE

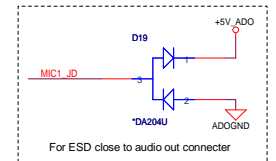
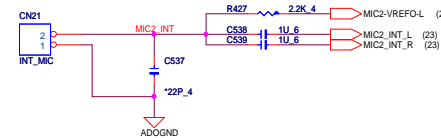


SYSTEM MIC

PINK

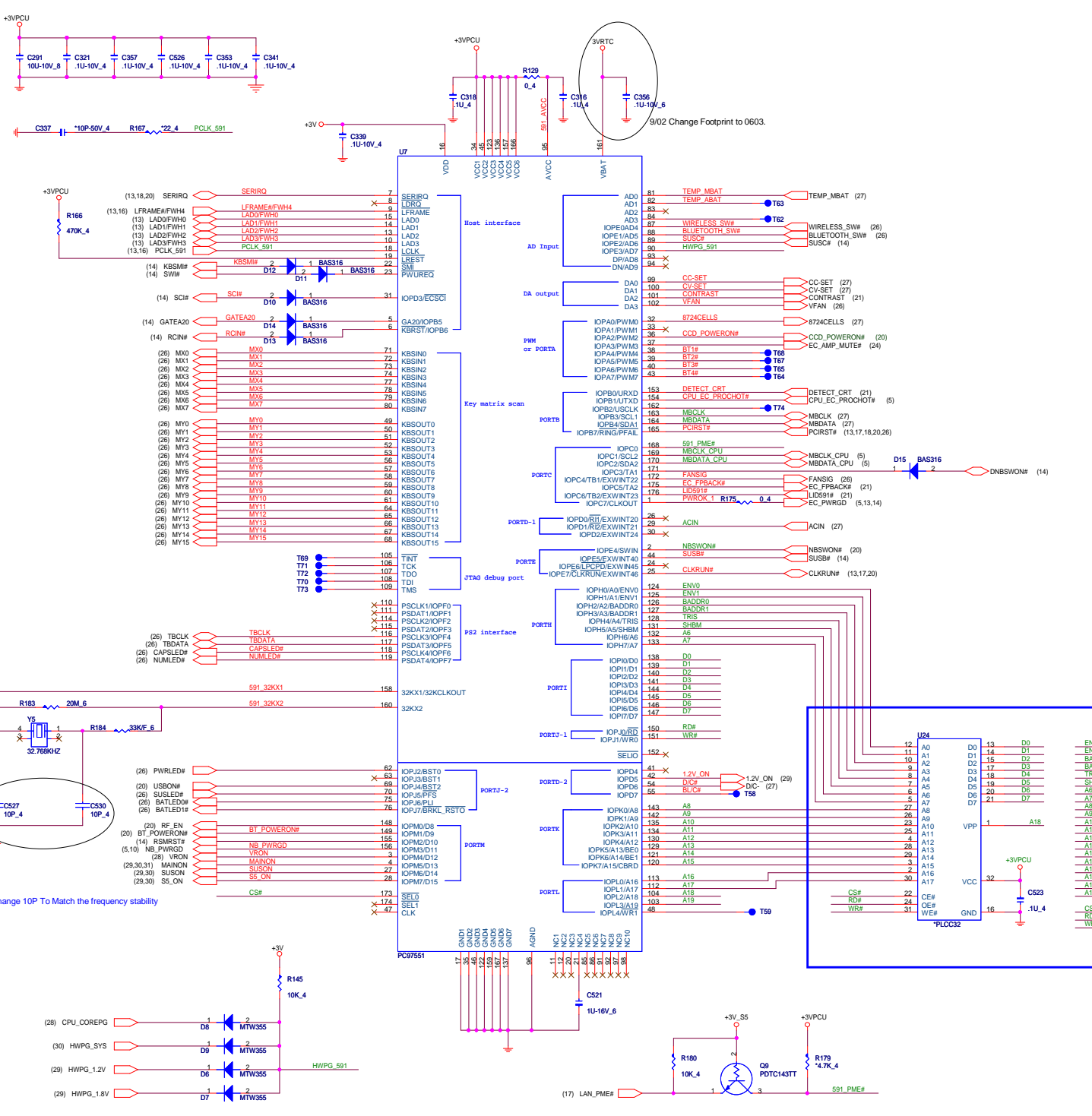


INT MIC

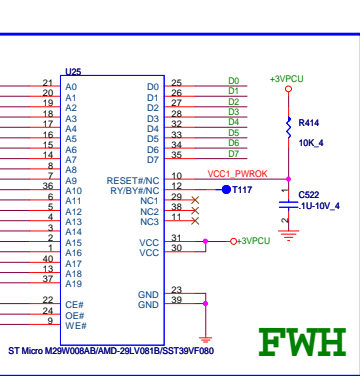
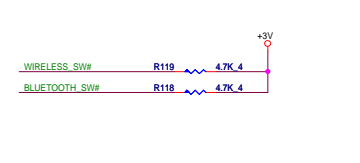
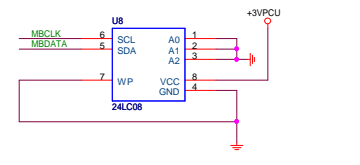
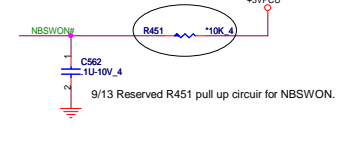
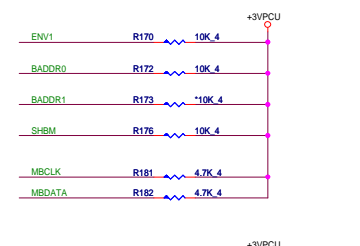


PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SPEAKER AMP / JACK	1A
Date	Wednesday, October 18, 2006	Sheet 24 of 31

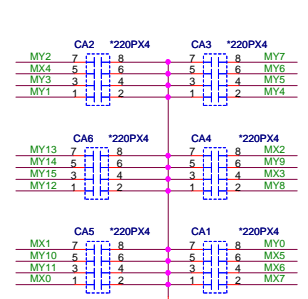
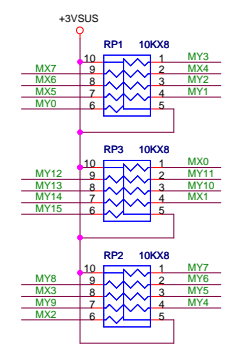
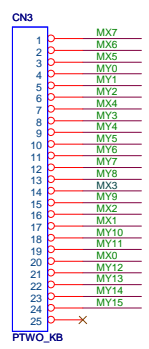
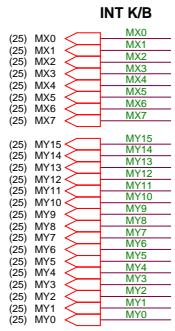


IO Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

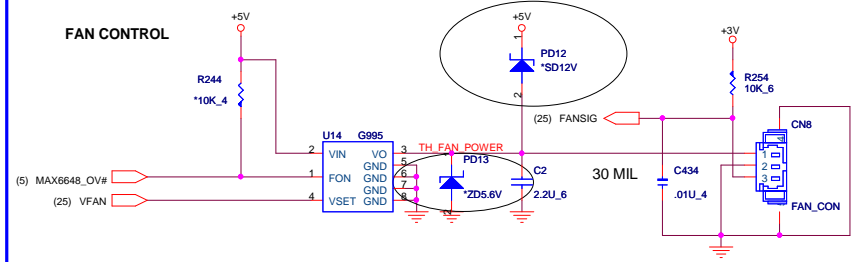


PROJECT : ZR3
Quanta Computer Inc.

Size: _____ Document Number: **97551 & FLASH** Rev: **1A**
Date: **Monday, October 23, 2006** Sheet: **25** of **31**

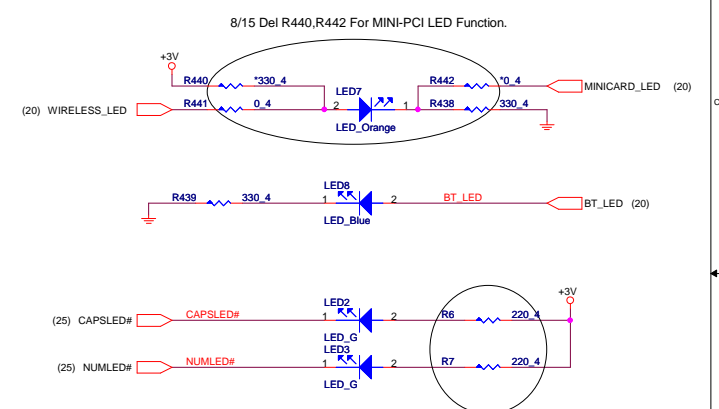
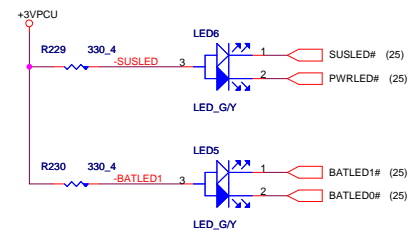
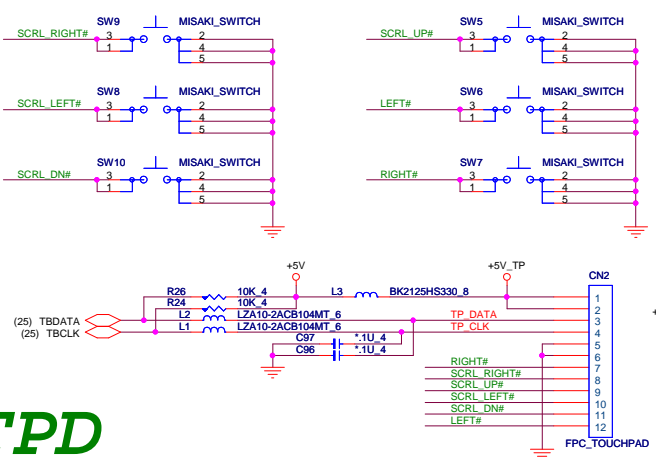


10/19 Preserve Schottky PD12 and Zener PD13 for protecting in U14 (Close to U14 PIN2, PIN3)



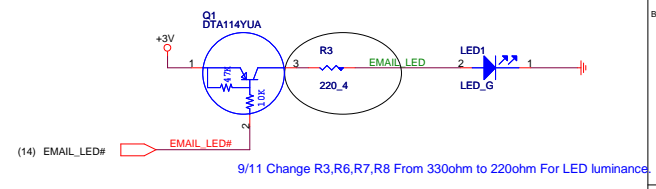
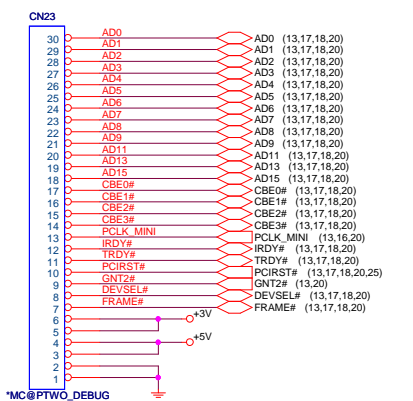
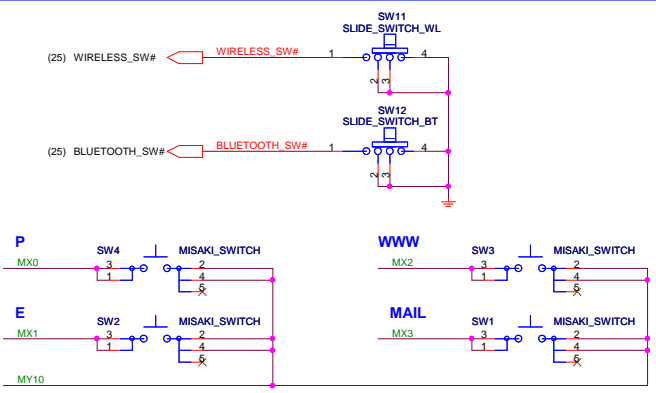
KBC

THM



TPD

9/11 Change R3,R6,R7,R8 From 330ohm to 220ohm For LED



9/11 Change R3,R6,R7,R8 From 330ohm to 220ohm For LED luminance

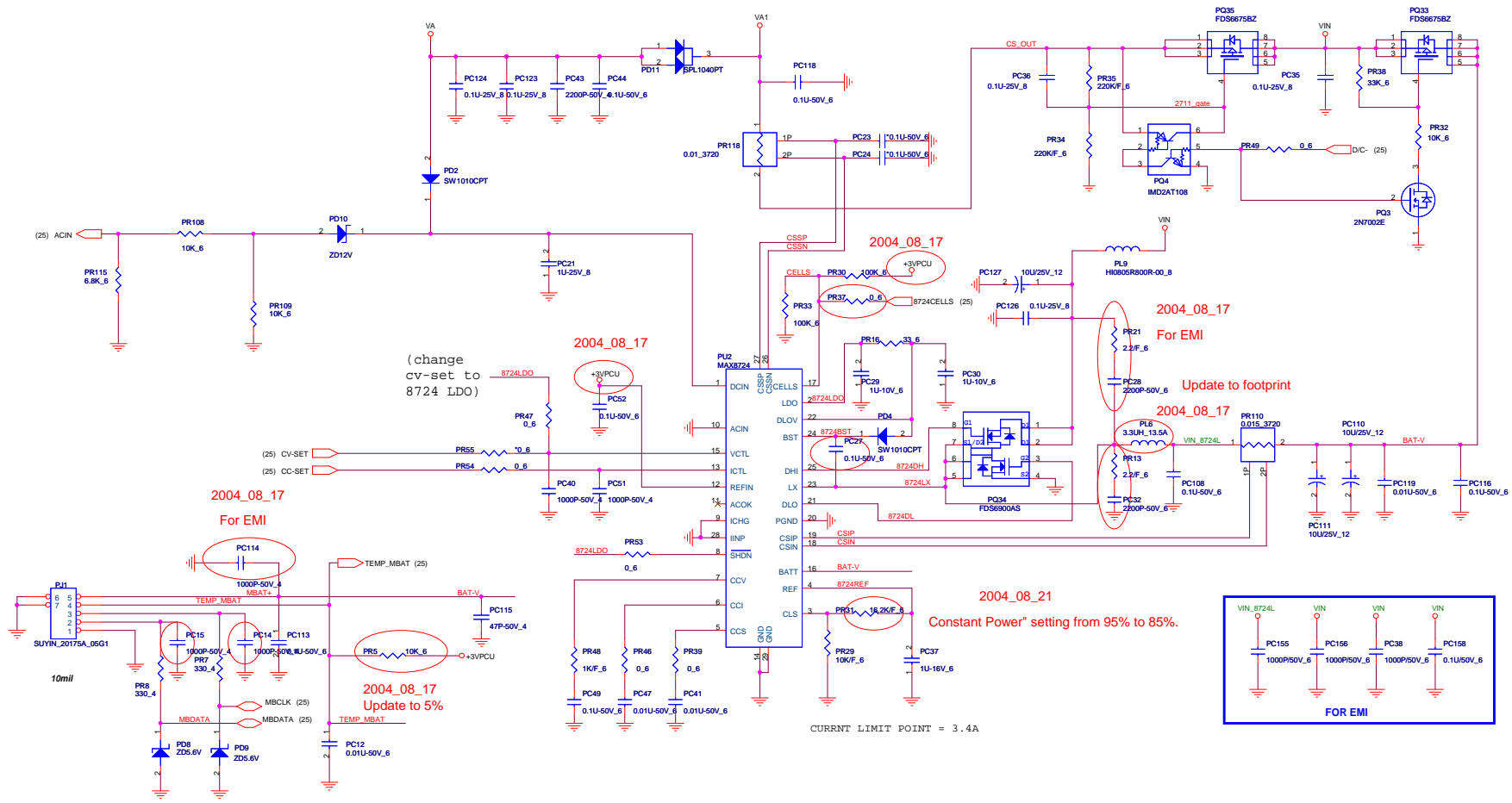
QUICK KEY SWITCH

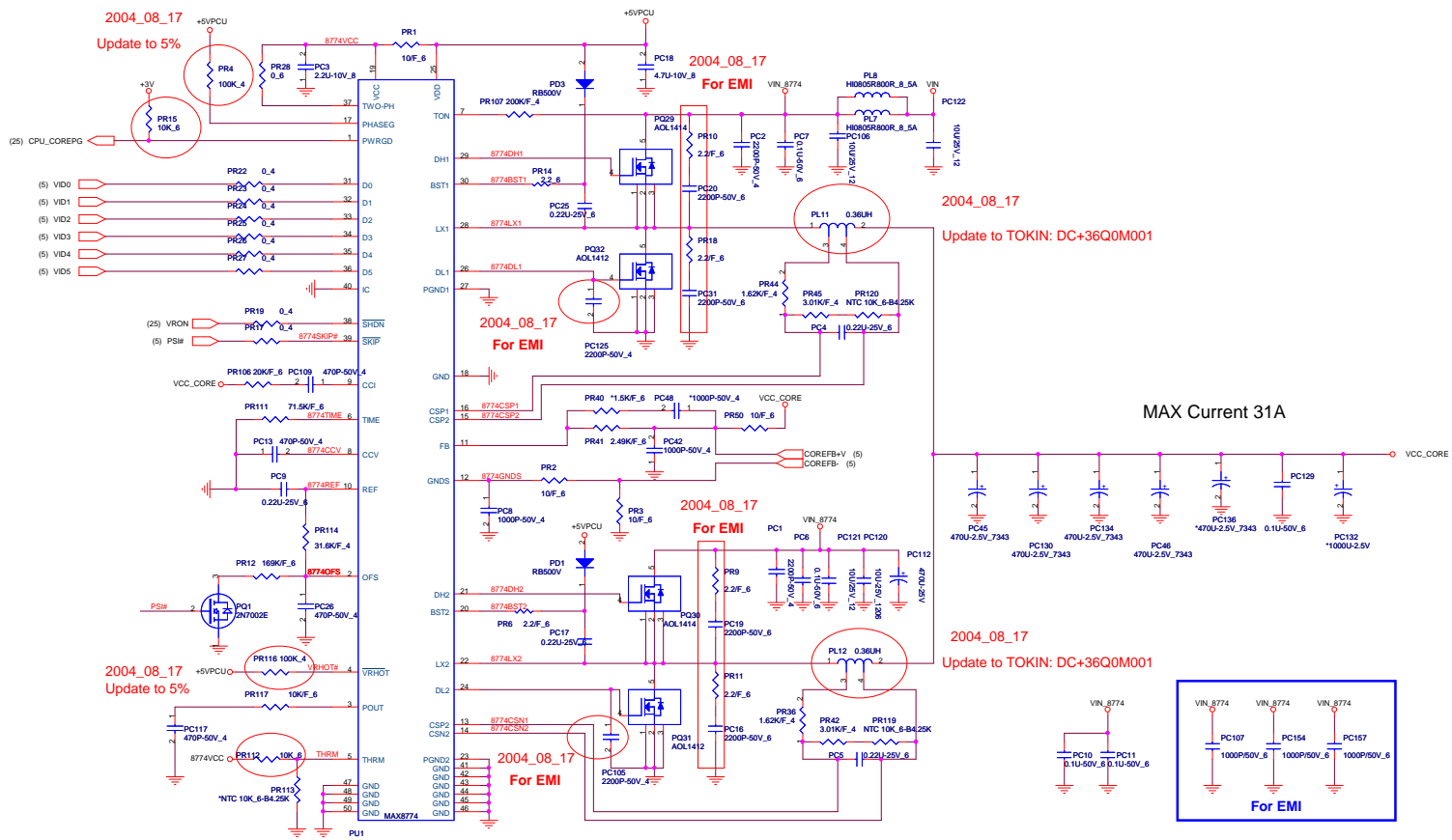
Debug card interface

LED

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	1A
Date:	Monday, October 23, 2006	Sheet 26 of 31





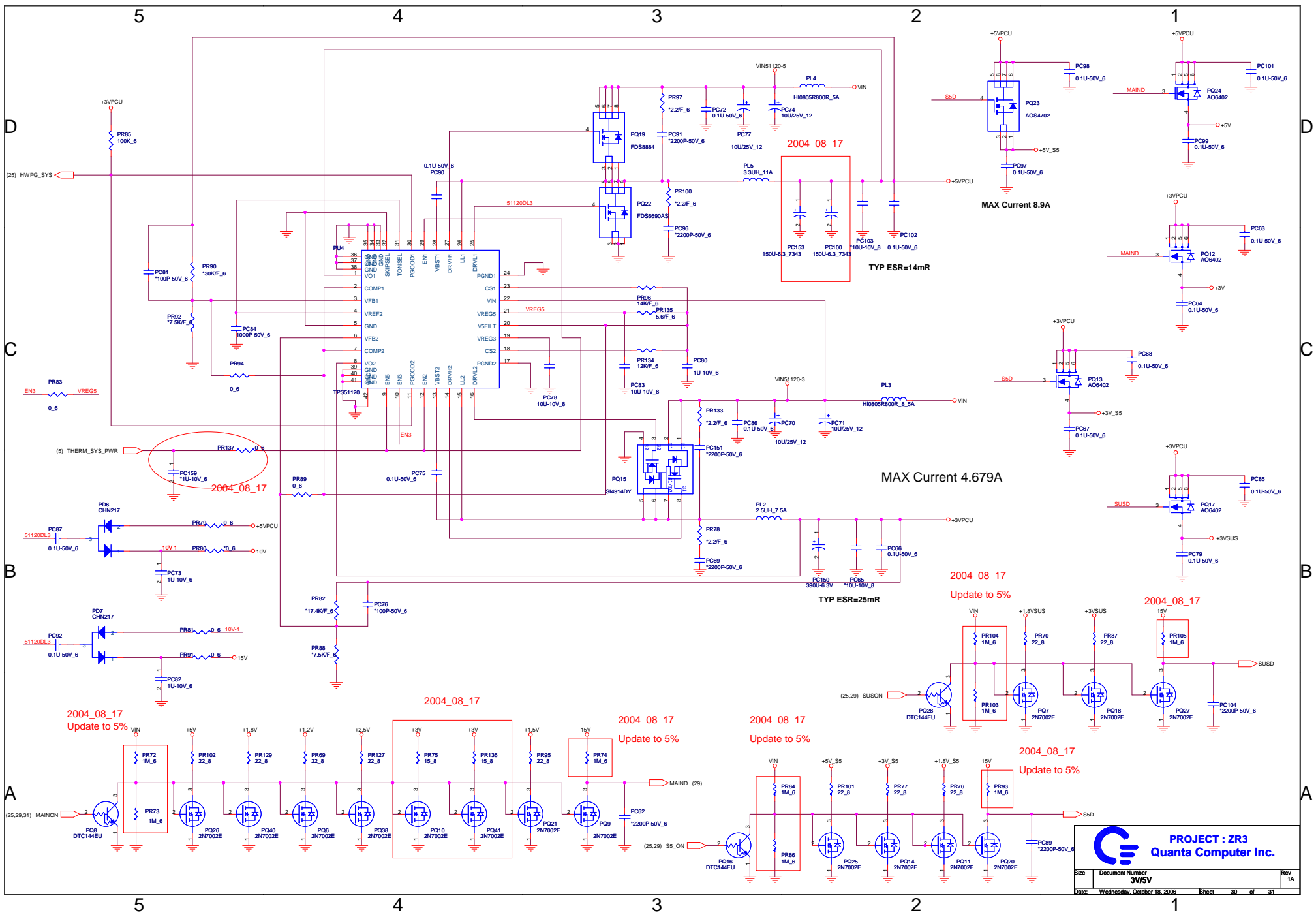
MAX Current 2.25A

MAX Current 5.807A

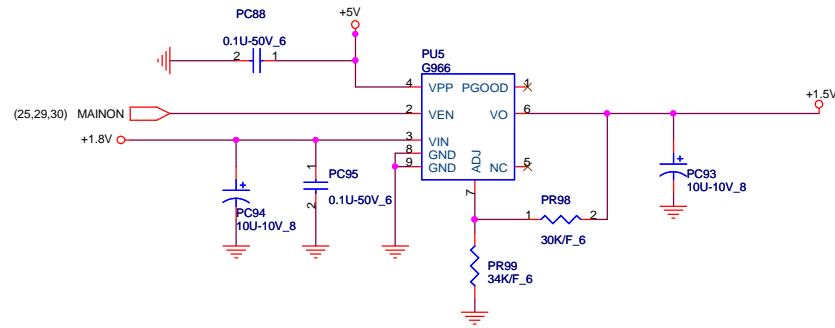
MAX Current 1.323A

MAX Current 8.256A

$$V_{out} = 1.25(1+R1/R2) = 1.25(1+44K/100K) = 1.8V$$



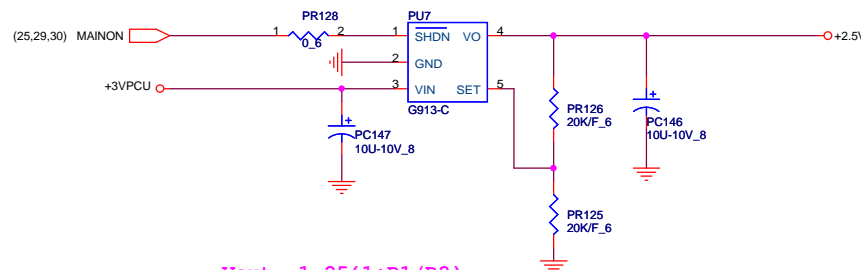
MAX Current 1A



$$V_{out} = 0.8(R1+R2)/R2$$

$$= 0.8(30+34)/34 = 1.5V$$

MAX Current 0.3A



$$V_{out} = 1.25(1+R1/R2)$$

$$= 1.25(1+20K/20K) = 2.5V$$



PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	+1.5V/+2.5V	1A
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