

Discrete/UMA /Muxless Schematics Document

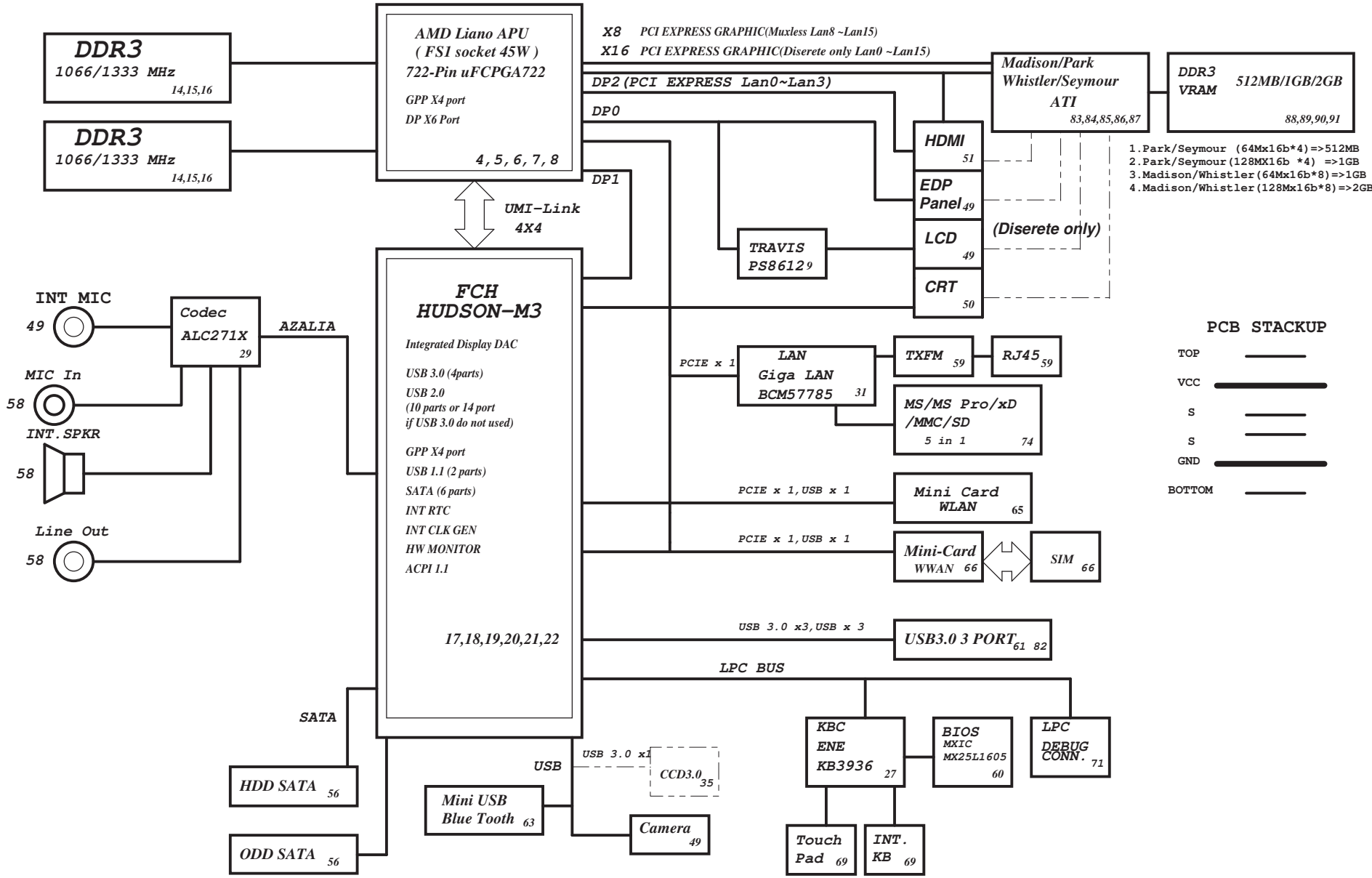
AMD LIANO CPU FS1

AMD GPU Manhattan(Park/Madison M2) and Vancouver(Seymour/Whistler M2)

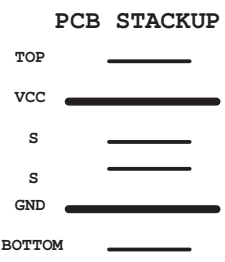
<Variant Name>

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Title			
Cover Page			
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A4	JE50 SB		SB
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JE50-SB Block Diagram



1. Park/Seymour (64Mx16b*4)=>512MB
2. Park/Seymour (128MX16b *4) =>1GB
3. Madison/Whistler (64Mx16b*8)=>1GB
4. Madison/Whistler (128Mx16b*8)=>2GB



SYSTEM DC/DC		RT8239	41
INPUTS	OUTPUTS		
DCBATOUT	5V_S5 (5.5A)	3D3V_S5 (5A)	
SYSTEM DC/DC		RT8207	44
5V_S5	1D5V_S3 (15A)		
SYSTEM DC/DC		RT8207	44
5V_S5	0D75_S0 (1.2A)		
SYSTEM DC/DC		RT8238	46
INPUTS	OUTPUTS		
5V_S5	1D1V_S5 (1.4A)		
SYSTEM DC/DC		RT8238	45
5V_S5	1D2V_S0 (5.2A)		
SYSTEM DC/DC		RT9025	93
3D3V_S5	1D8V_VGA_S0		
1D5V_S3	1V_VGA_S0		
SYSTEM DC/DC		RT9025	48
3D3V_S0	2D5V_S0 (200mA)		
SYSTEM DC/DC		RT8208	92
5V_S5	VGA_CORE		
CHARGER		BQ24745	40
INPUTS	OUTPUTS		
DCBATOUT	CHG_PWR 18V 6.0A	UP+5V 5V 100mA	
SYSTEM DC/DC		ISL6267	42,43
INPUTS	OUTPUTS		
DCBATOUT	VCC_CORE_S0 0~1.55V 18A	VDDNB 0~1.55V 4A	

<Variant Name>

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Title: **Block Diagram**

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Strapping

REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH_GPO199	PCL_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

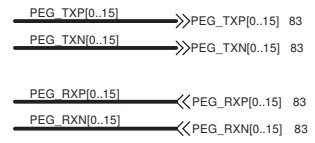
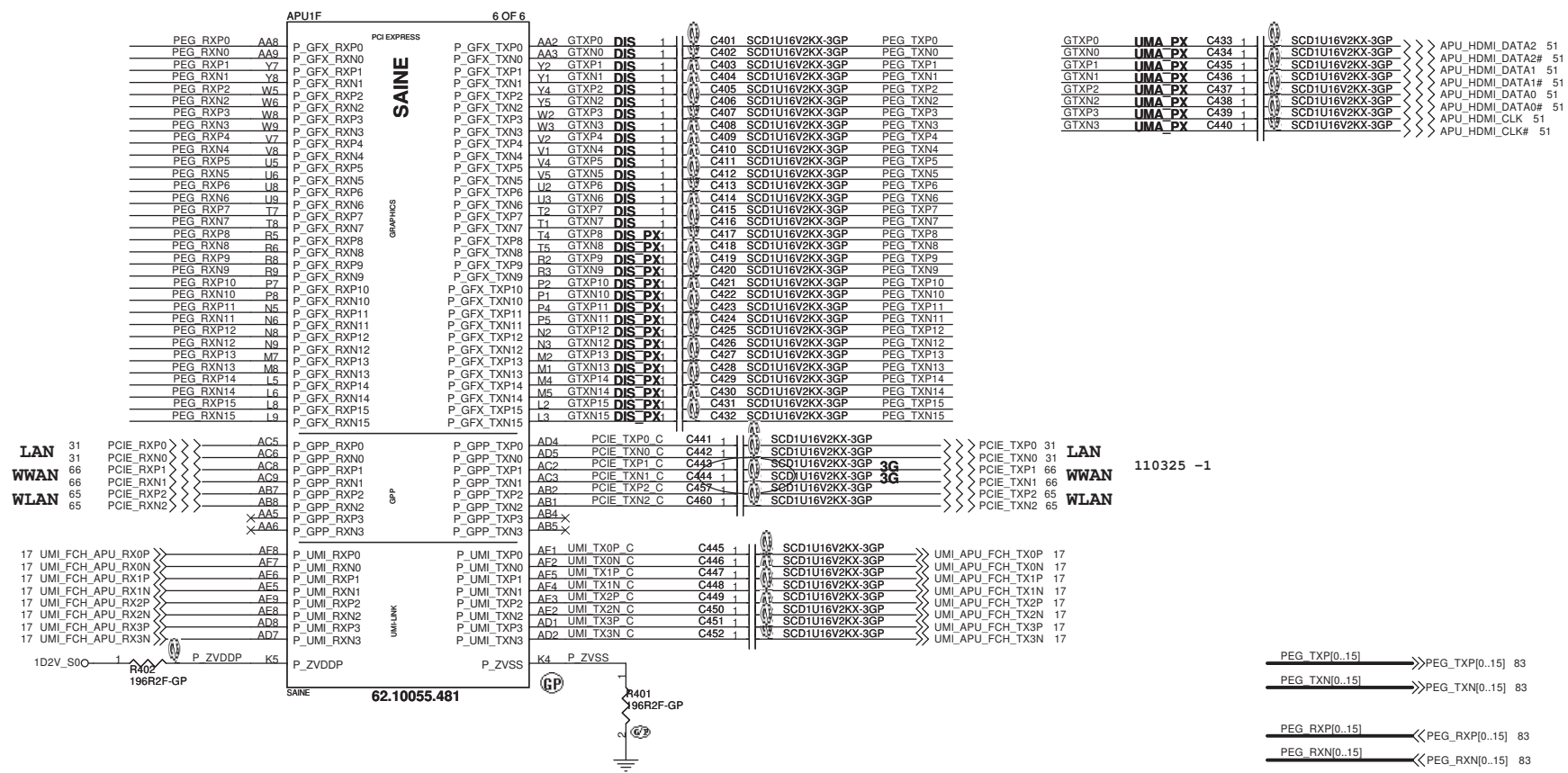
USB Table

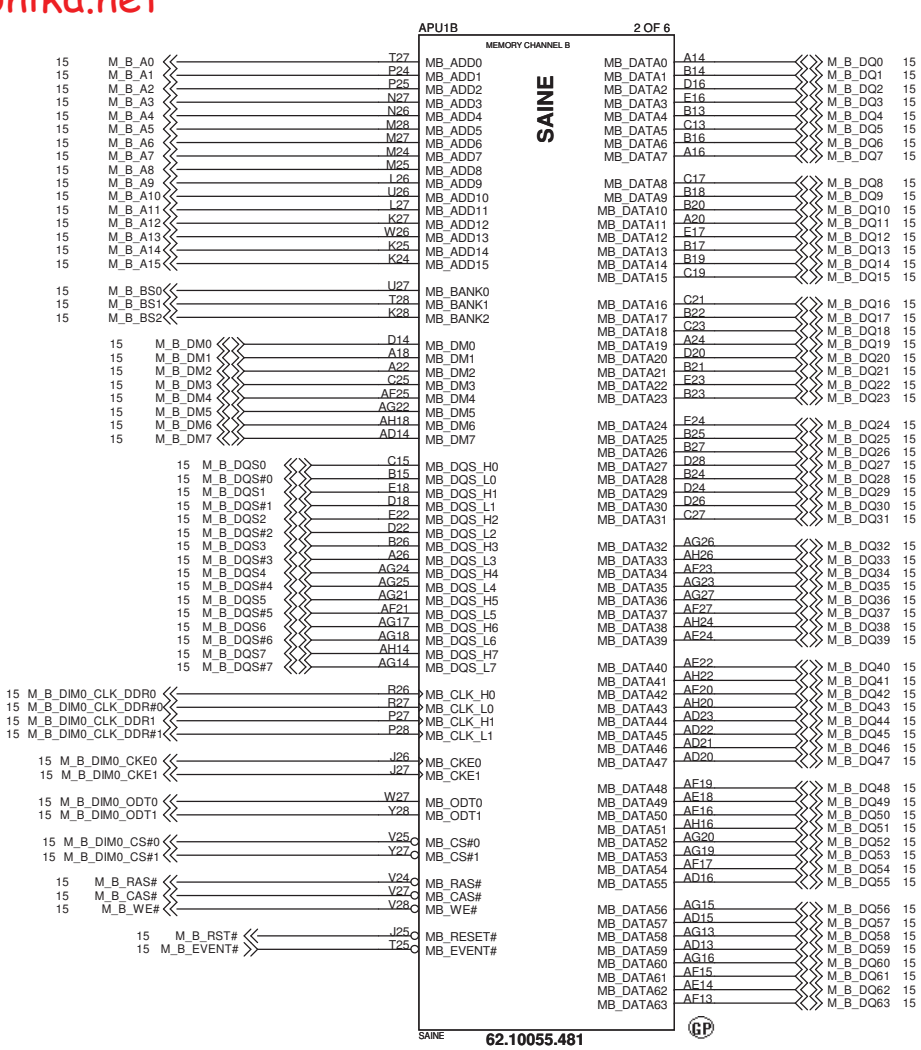
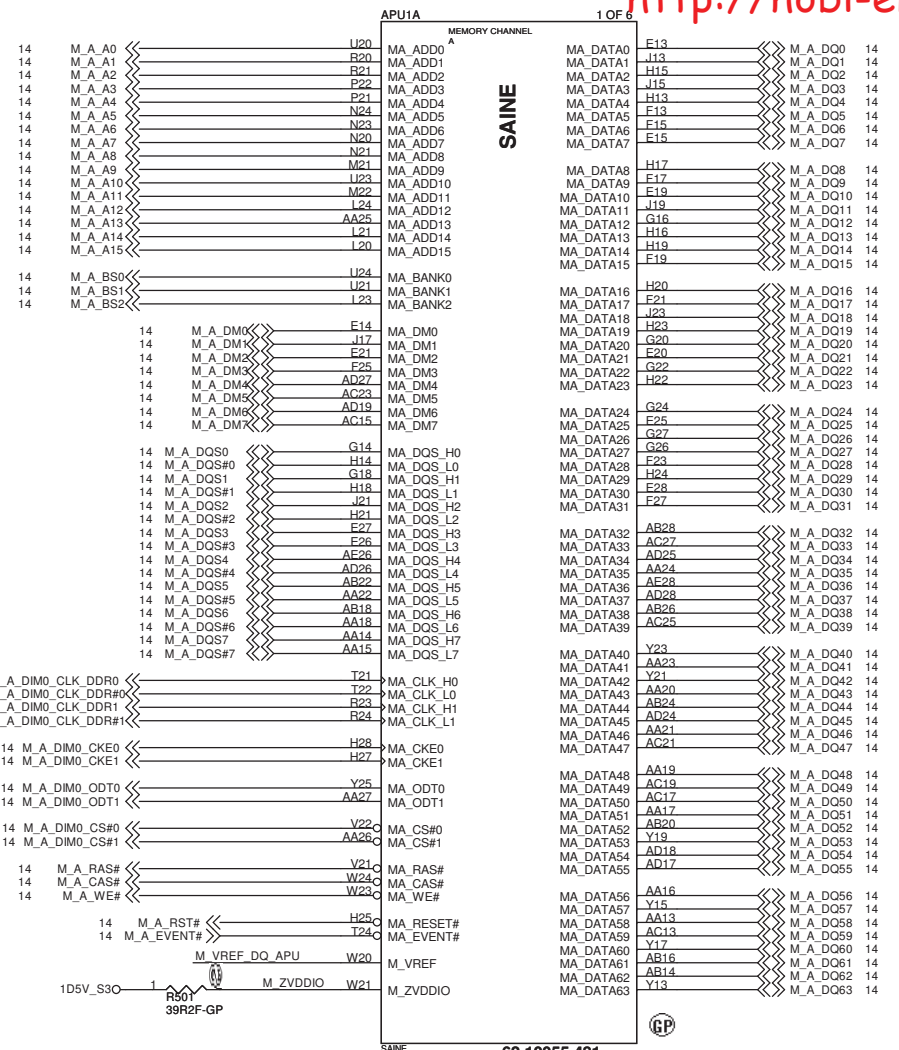
USB	
Pair	Device
0	USB 2.0 EXT2 (For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	NC
7	CCD
8	NC
9	Card Reader
10	USB 3.0 port 1
11	USB 2.0 EXT2
12	USB 2.0 EXT3
13	NC

PCIE Routing

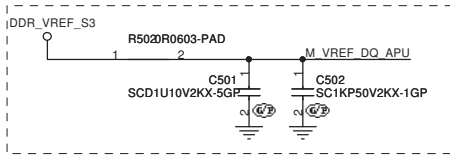
APU	
LANE0	LAN
LANE1	WWAN
LANE2	LAN
LANE3	

FCH	
LANE0	
LANE1	
LANE2	
LANE3	

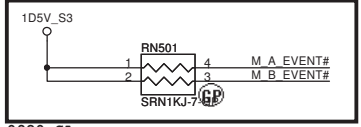




APU_VREF_DQ



LAYOUT: place them close to APU



0920-SA

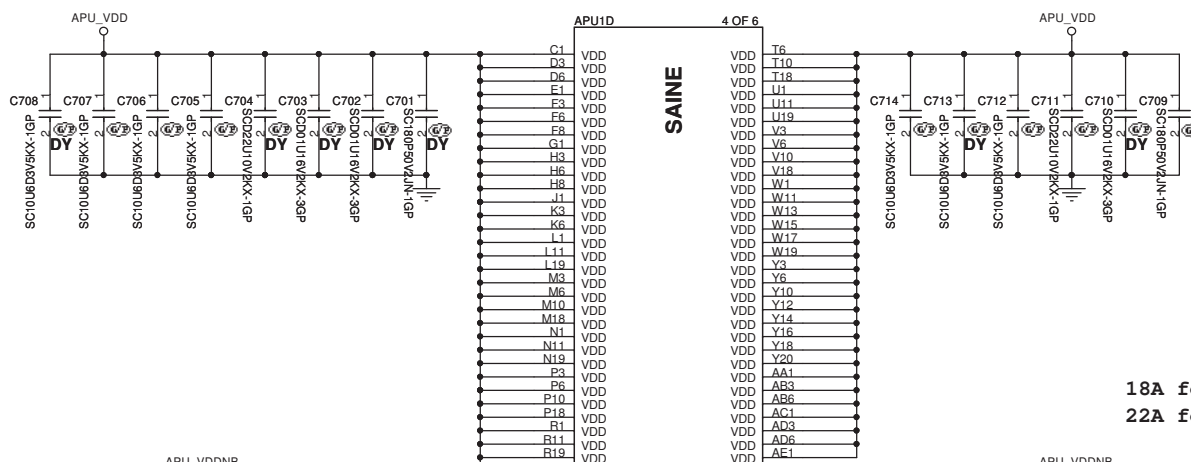
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Title: **APU DDR(2/5)**

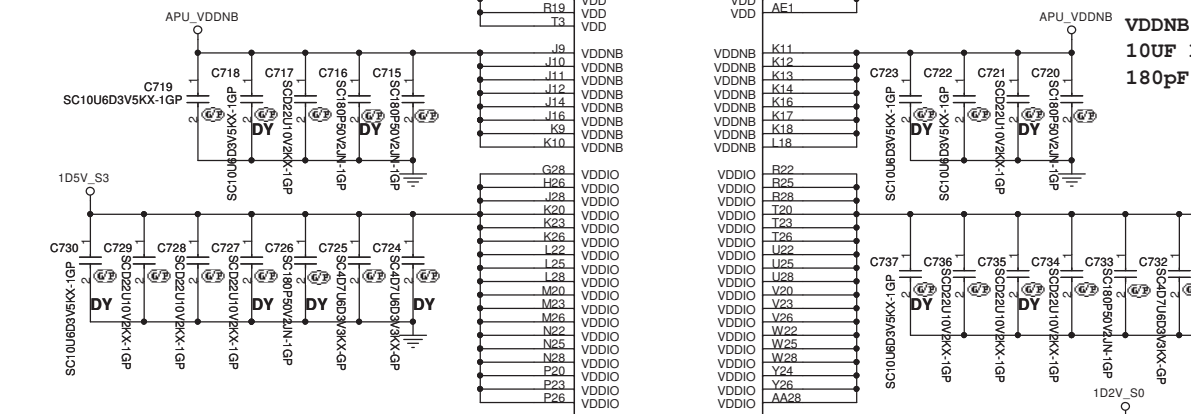
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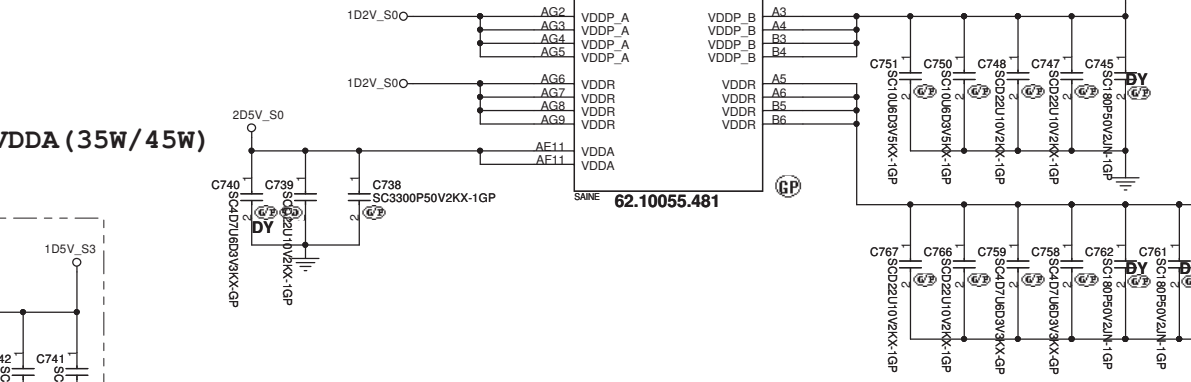
36A for VDD (35W CPU)
45A for VDD (45W CPU)

VDD:
10UF X7 0.22UF X2 10nF X3
180pF Cap for EMI requirement



18A for VDDNB (35W CPU)
22A for VDDNB (45W CPU)

VDDNB:
10UF X4 0.22UF X2
180pF Cap for EMI requirement

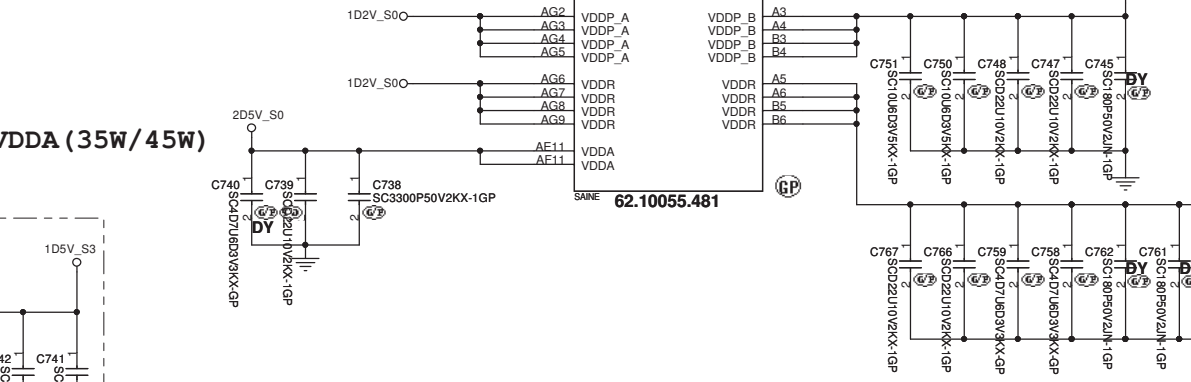


4A for VDDIO (35W CPU)
4.6A for VDDIO (45W CPU)

VDDIO:
10UF X2 0.22UF X6 4.7uFUF X4
180pF Cap for EMI requirement

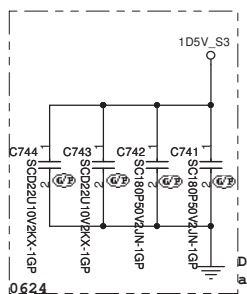
3.5A for VDDP (35W/45W)

0.75A for VDDA (35W/45W)



VDDP:
10UF X2 0.22uF X2
180pF Cap for EMI requirement

3A for VDDR (35W)
3.5A for VDDR (45W)



Decoupling between processor and DIMMs across VDDIO and VSS Split

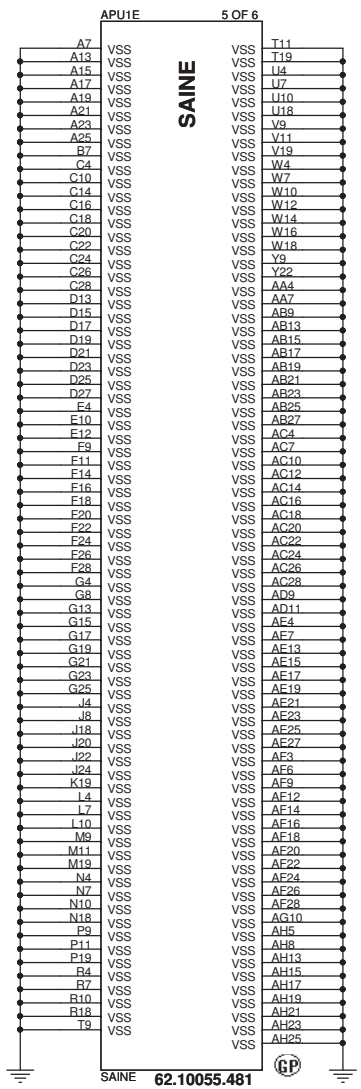
VDDR:
4.7UF X2 0.22uF X2
180pF Cap for EMI requirement

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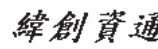
緯創資通 Wistron Corporation
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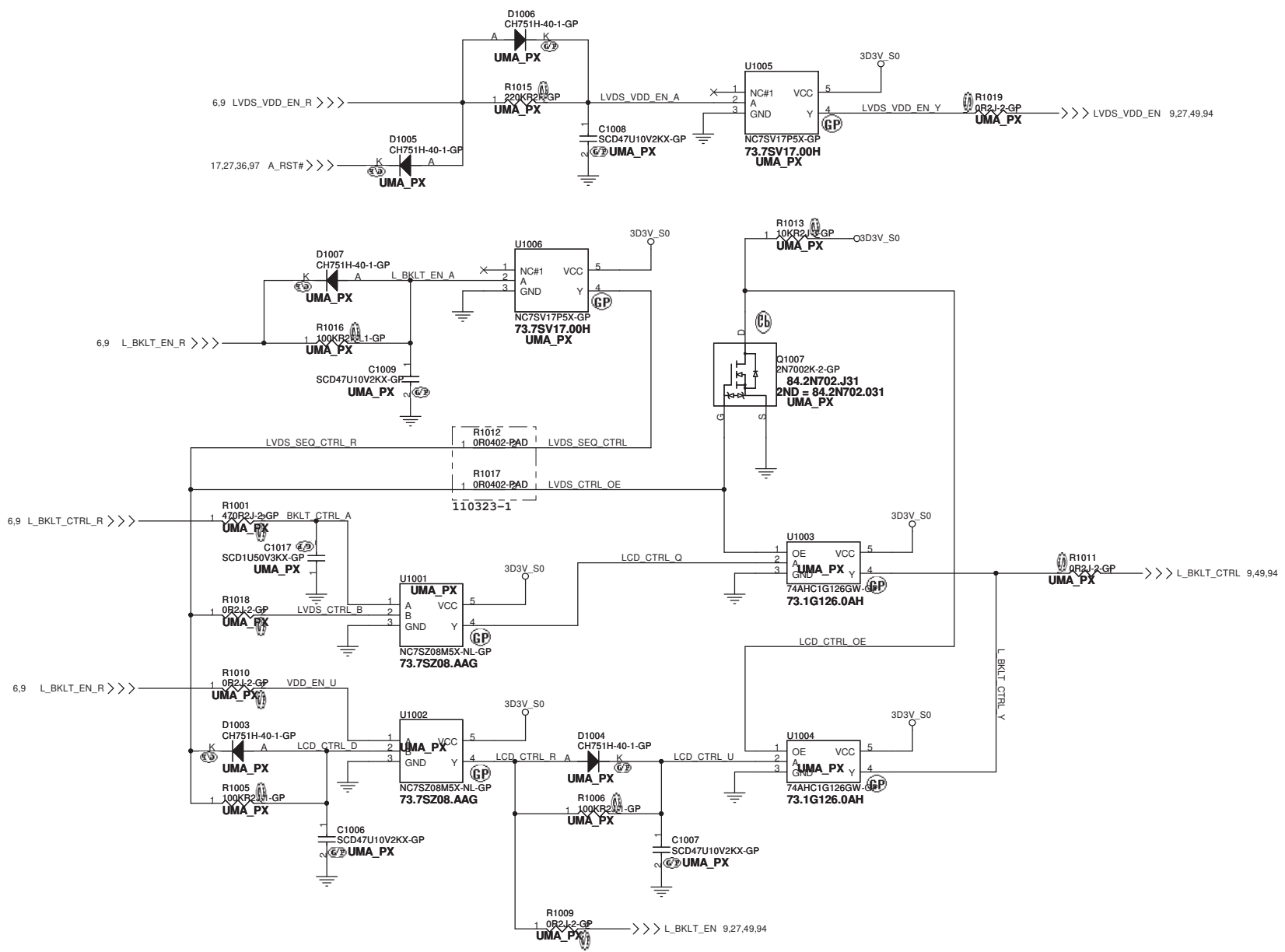
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APU VSS(5/5)		
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Title

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<Variant Name>

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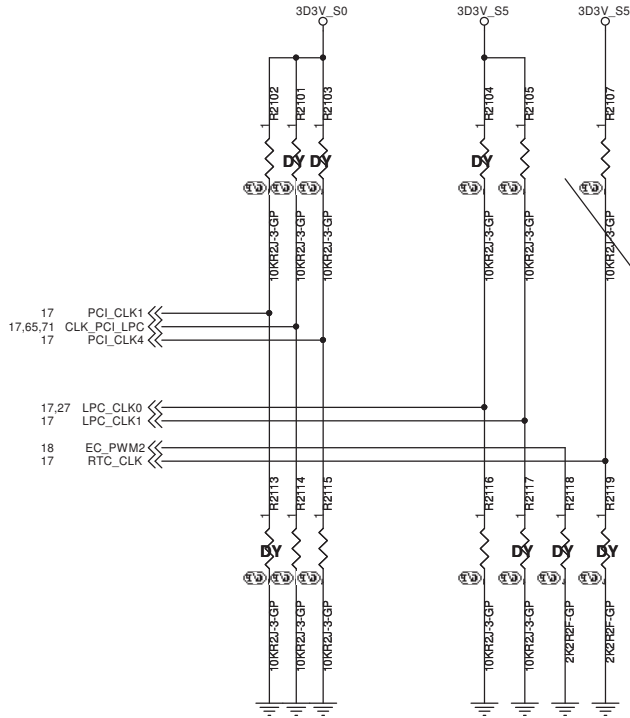
Title		
Reserved		

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REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5
 checklist:PU 3.3V_S5
 no support S5 PLUS function,PU 3.3V_S5



LPC ROM implemented
 checklist suggestion:
 no PU or PD required
 (integrated PU 10K)
 CRB: do not stuff PU Res

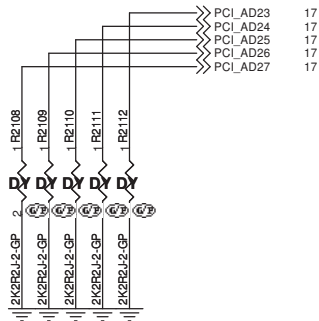
REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

Ball Name	Strap Function	Description
	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

<Variant Name>

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Title: **HUDSON-M2(5/6)**

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<Variant Name>

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Title

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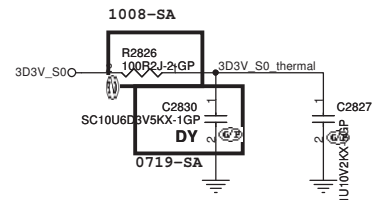
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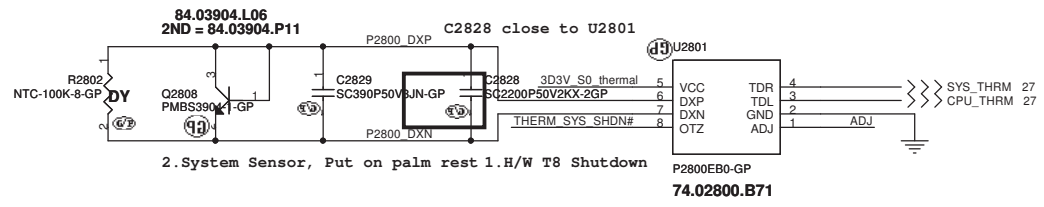
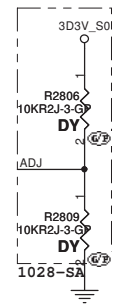
Title	
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ADJ IN
 Over temperature threshold setting by external resistor divider
 Floating= 85oC, GND=90oC, VCC=95oC

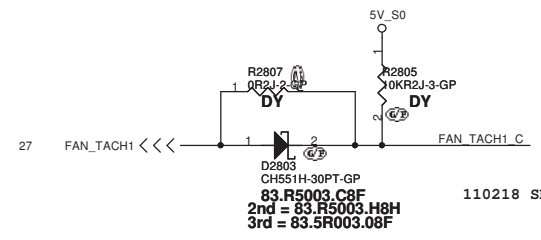


Layout notice :
 Both DXN and DXP routing 10 mil
 trace width and 10 mil spacing.

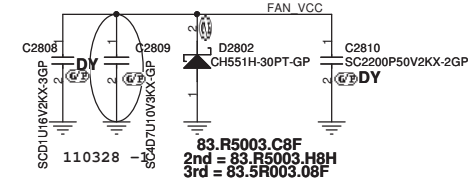


2. System Sensor, Put on palm rest 1.H/W T8 Shutdown

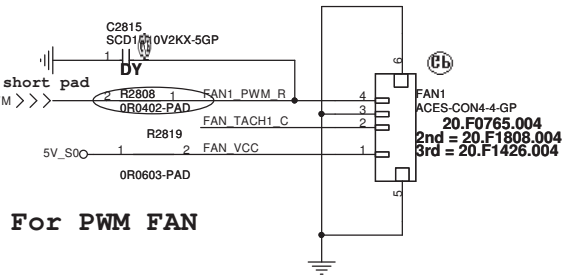
P2800EB0-GP
 74.02800.B71



Layout 15 mil

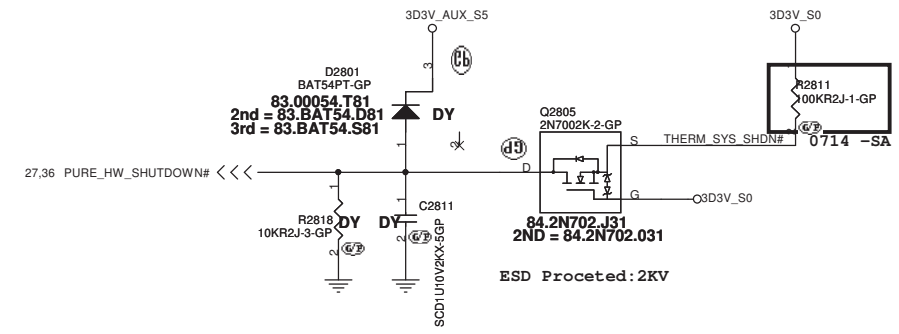


110218 SB change to short pad



For PWM FAN

VGA Thermal sensor P2800



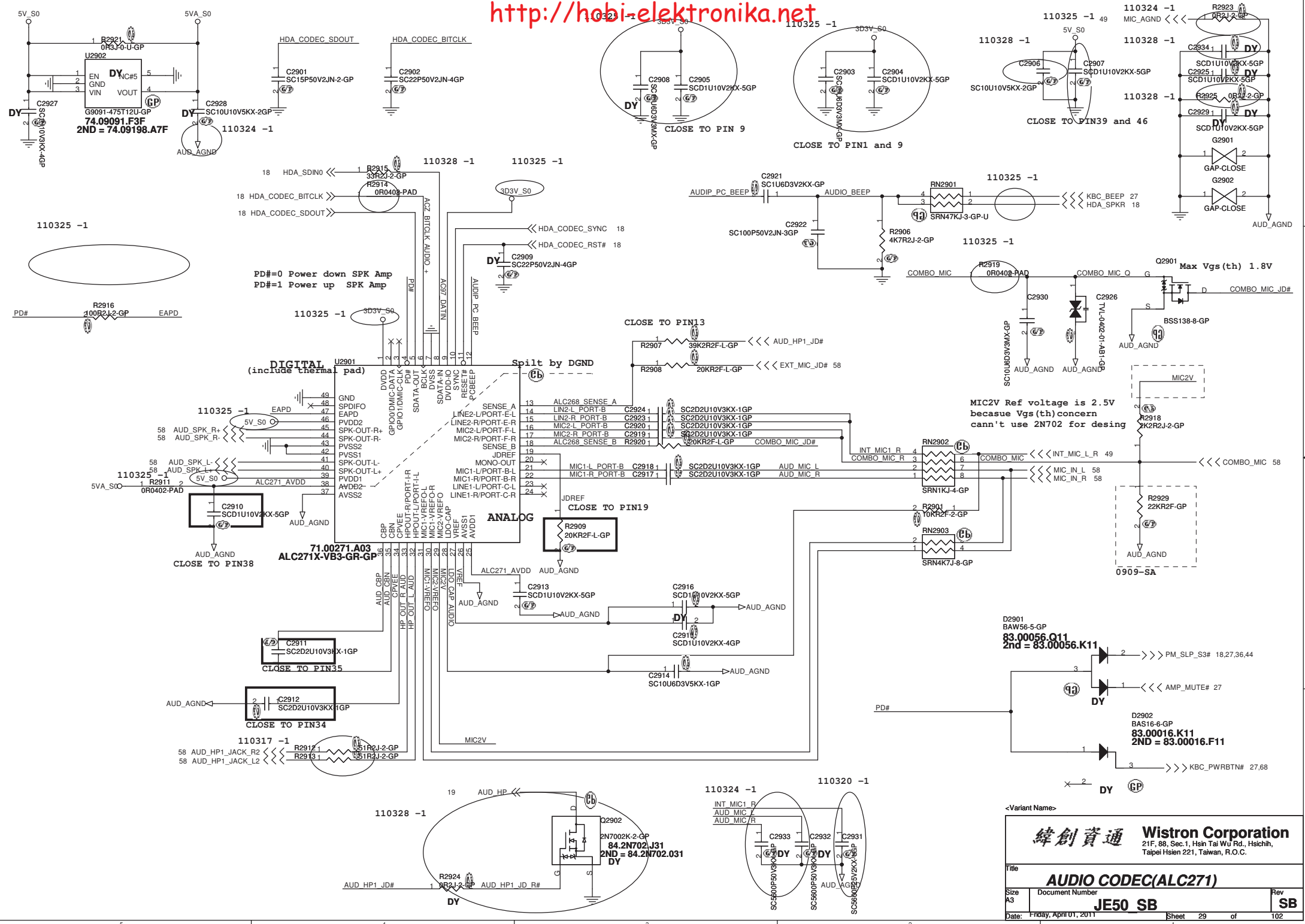
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Title: **Thermal P2800**

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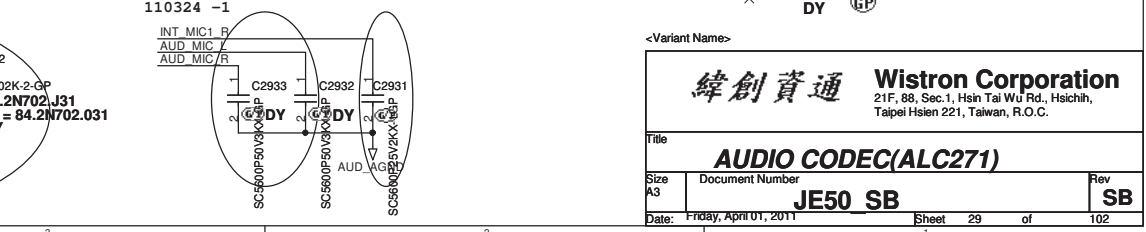
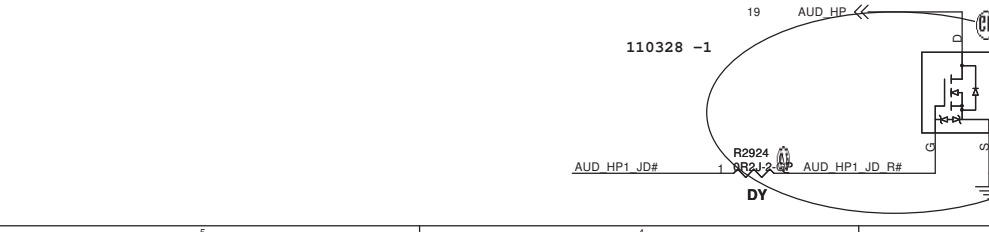
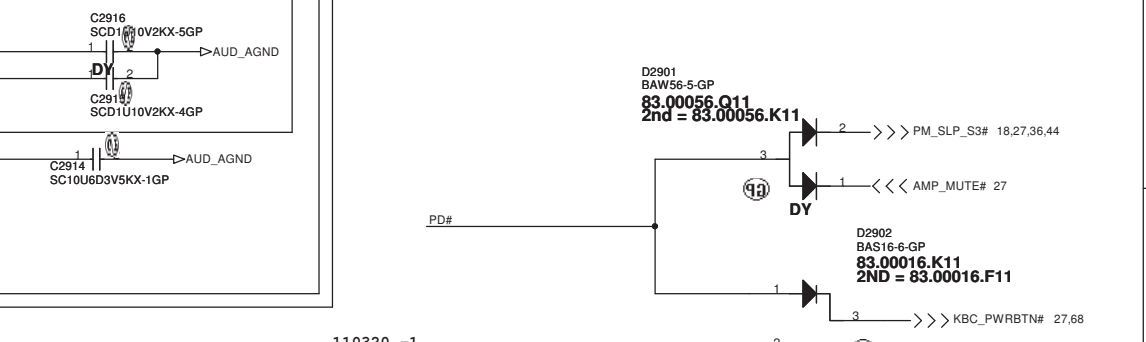
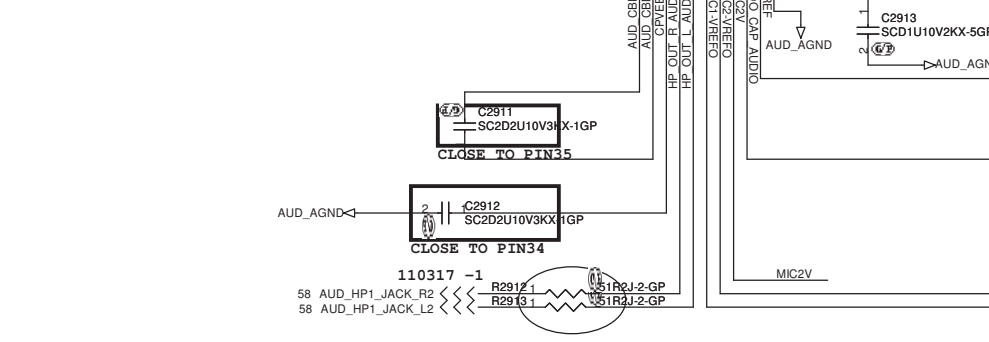
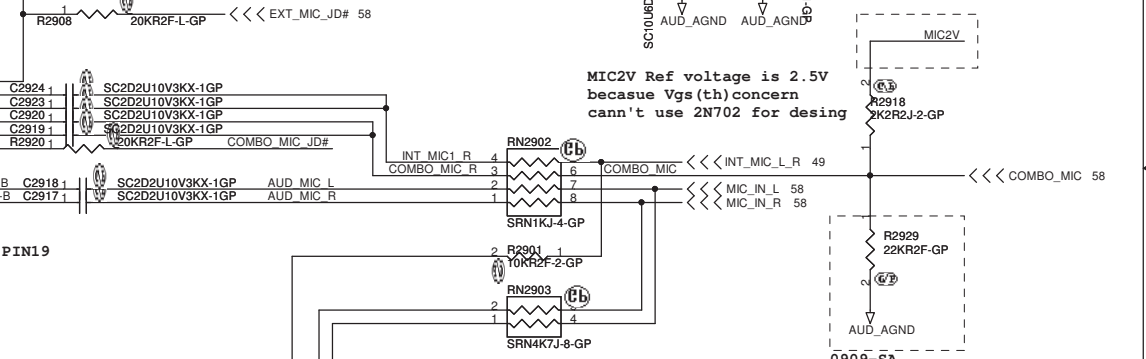
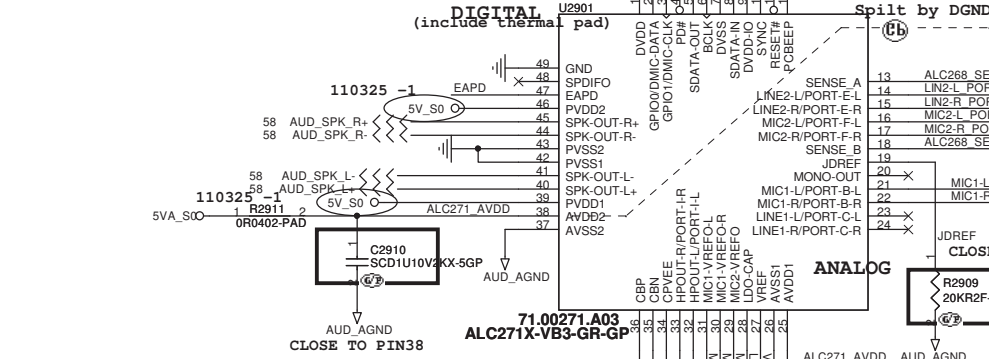
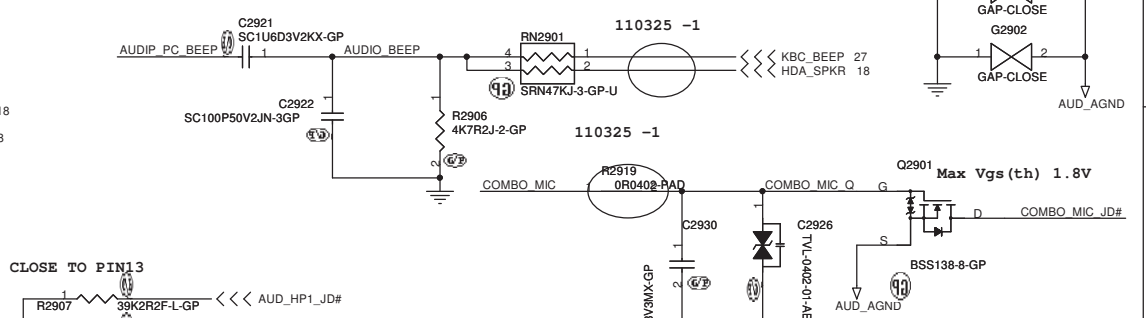
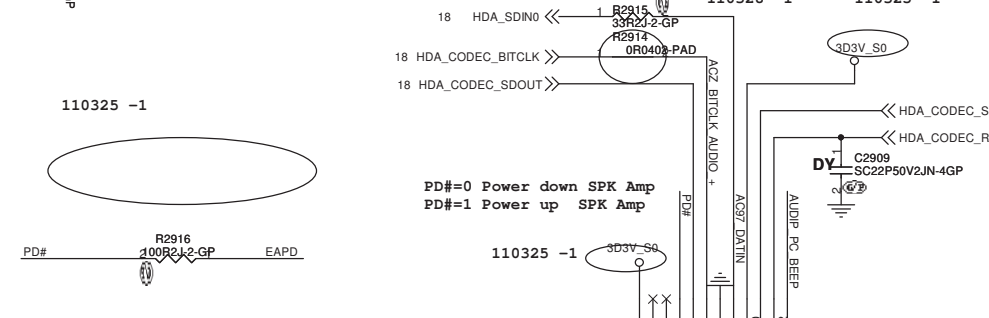
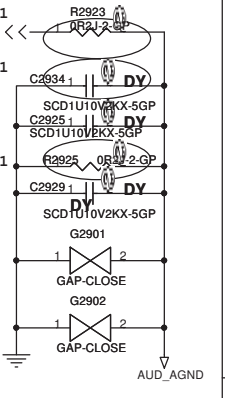
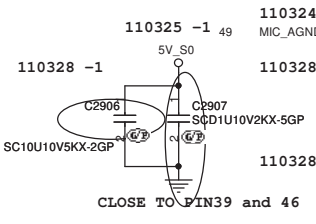
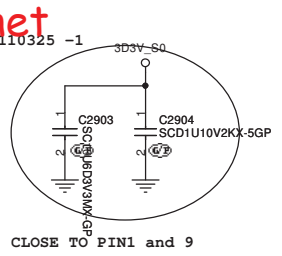
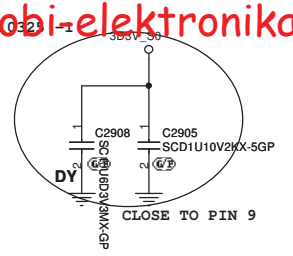
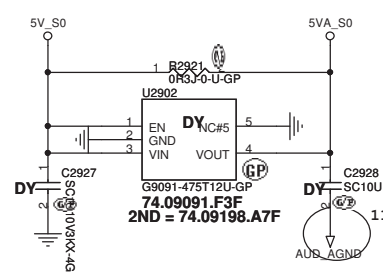
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Title: **AUDIO CODEC(ALC271)**

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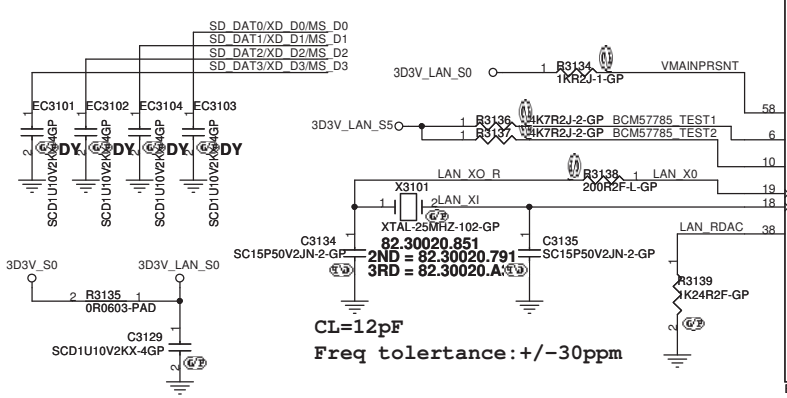
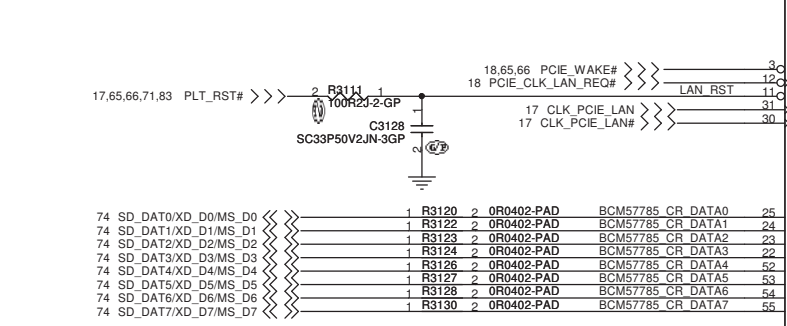
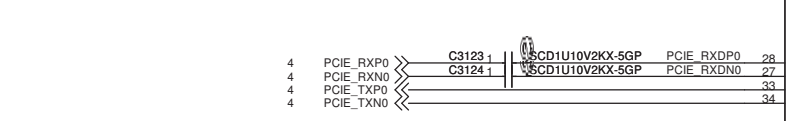
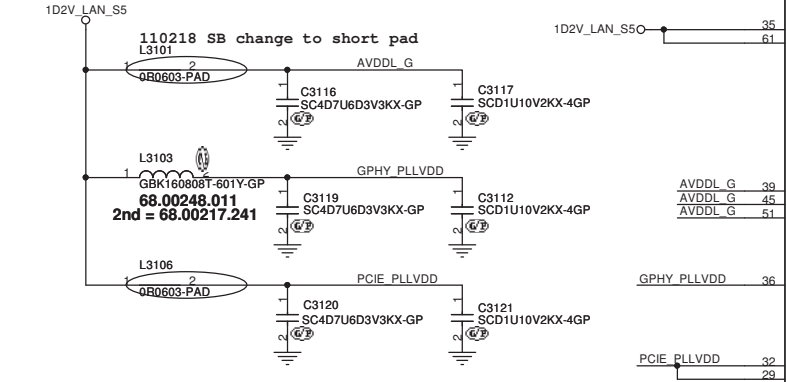
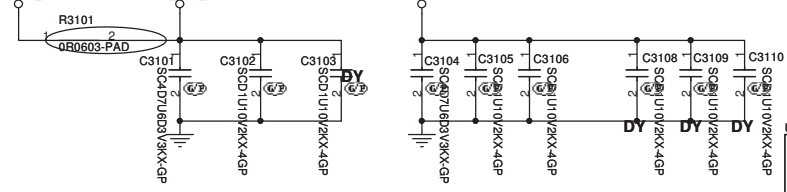


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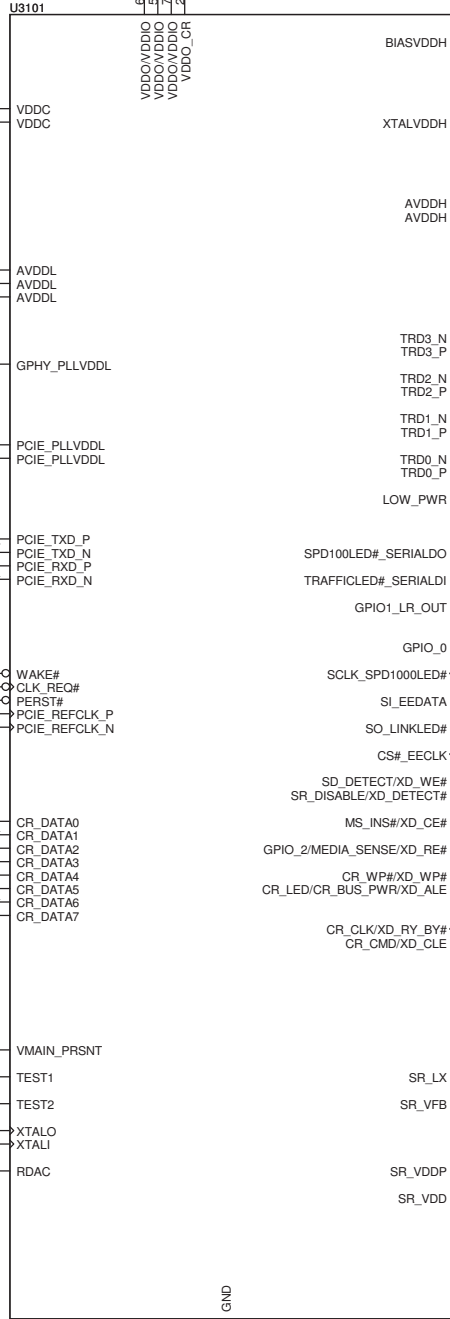
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110218 SB change to short pad

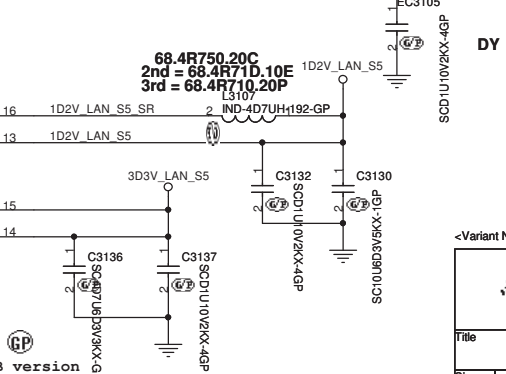
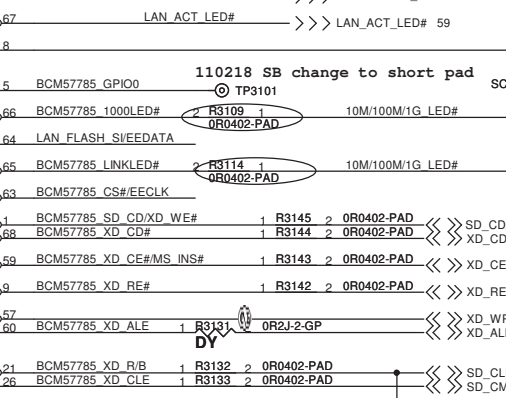
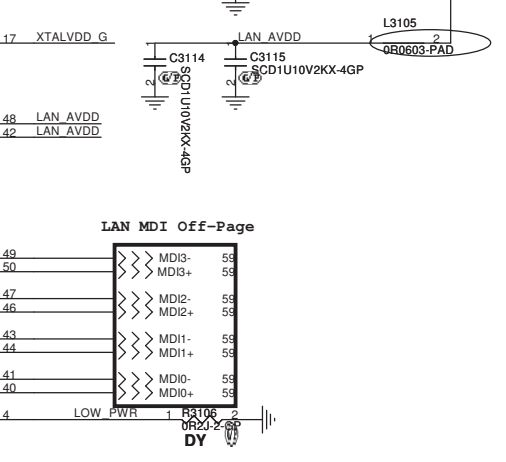
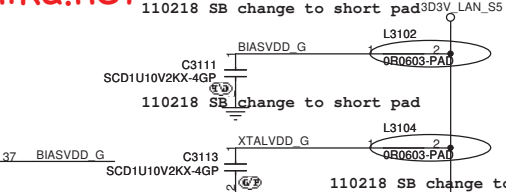


CL=12pF
Freq tolerance: +/-30ppm

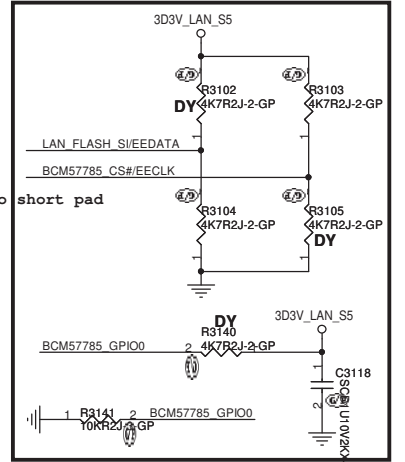


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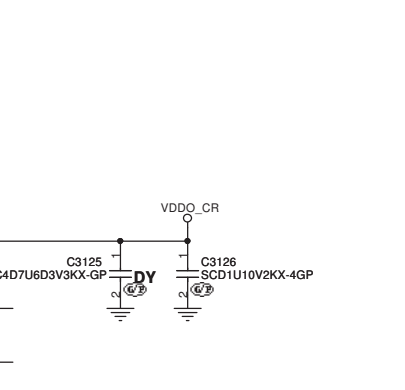
110218 SB change to short pad



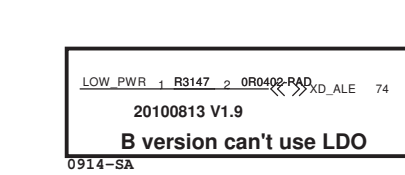
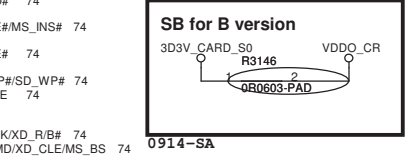
JE40-HR SB change to B version
P/N: 71.57785.M03



1008-SA



110218 SB change to short pad



20100813 V1.9
B version can't use LDO

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **LOM**

Size A3 Document Number: **JE50 SB** Rev: **SB**

Date: Friday, April 01, 2011 Sheet 31 of 102

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RTS5138

Size

A4

Document Number

JE50 SB

Rev

SB

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<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	
Reserved	

Size	Document Number	Rev
A4	JE50 SB	SB

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(Blanking)

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

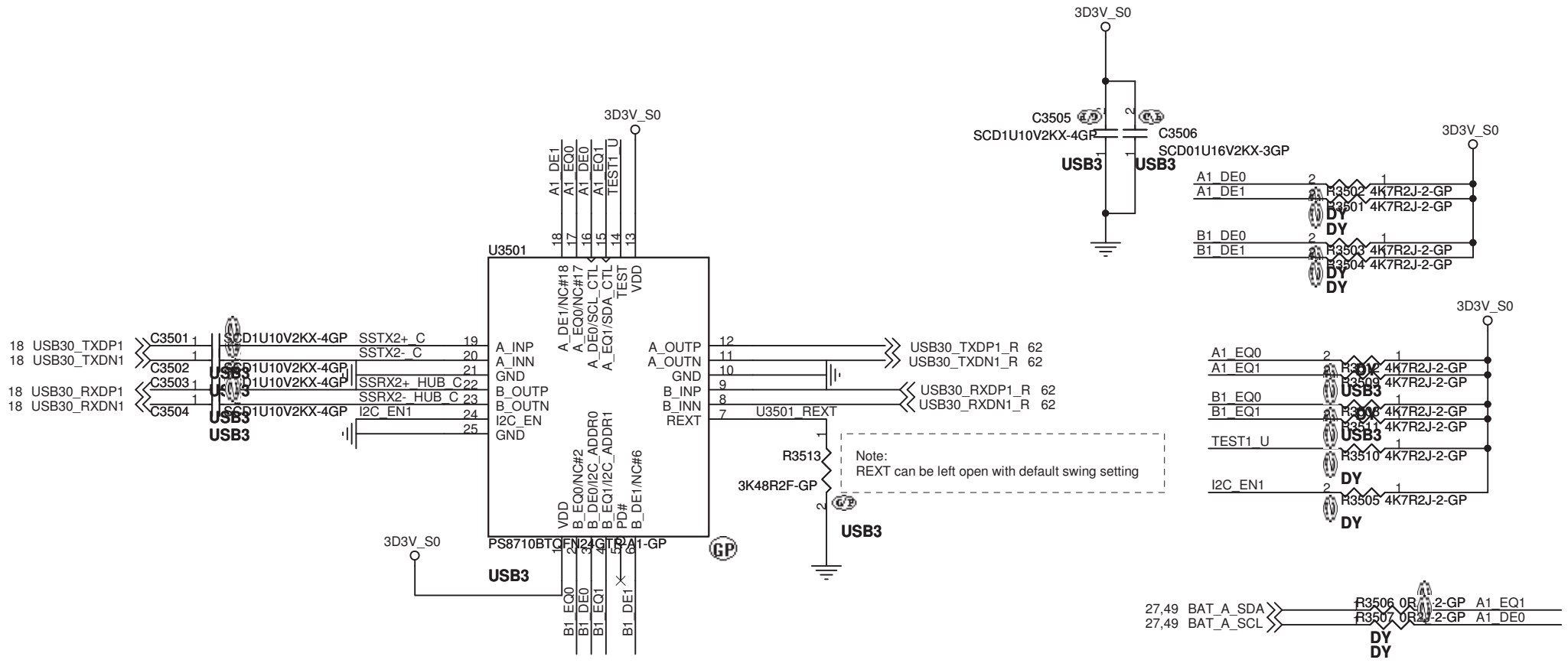
JE50 SB

Rev

SB

Date: Friday, April 01, 2011

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<Variant Name>


 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Title **Reserved**

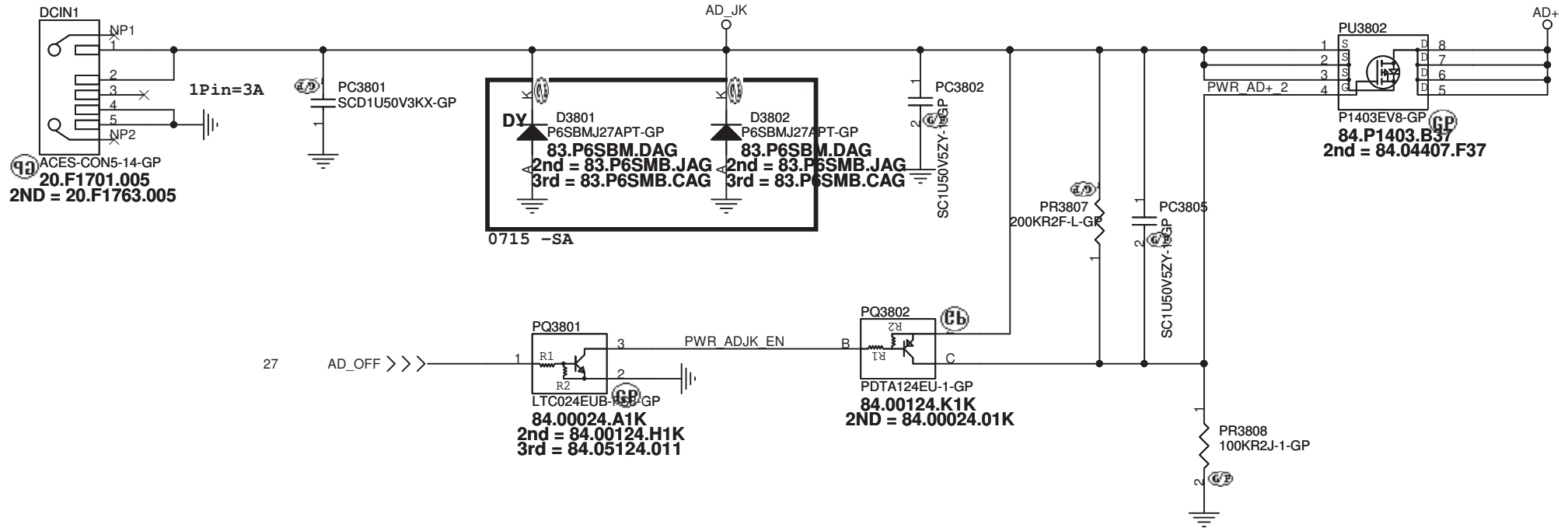
Size A4	Document Number JE50 SB	Rev SB
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Title		
Reserved		
Size	Document Number	Rev
A4	JE50 SB	SB
Date:	Friday, April 01, 2011	Sheet 37 of 102

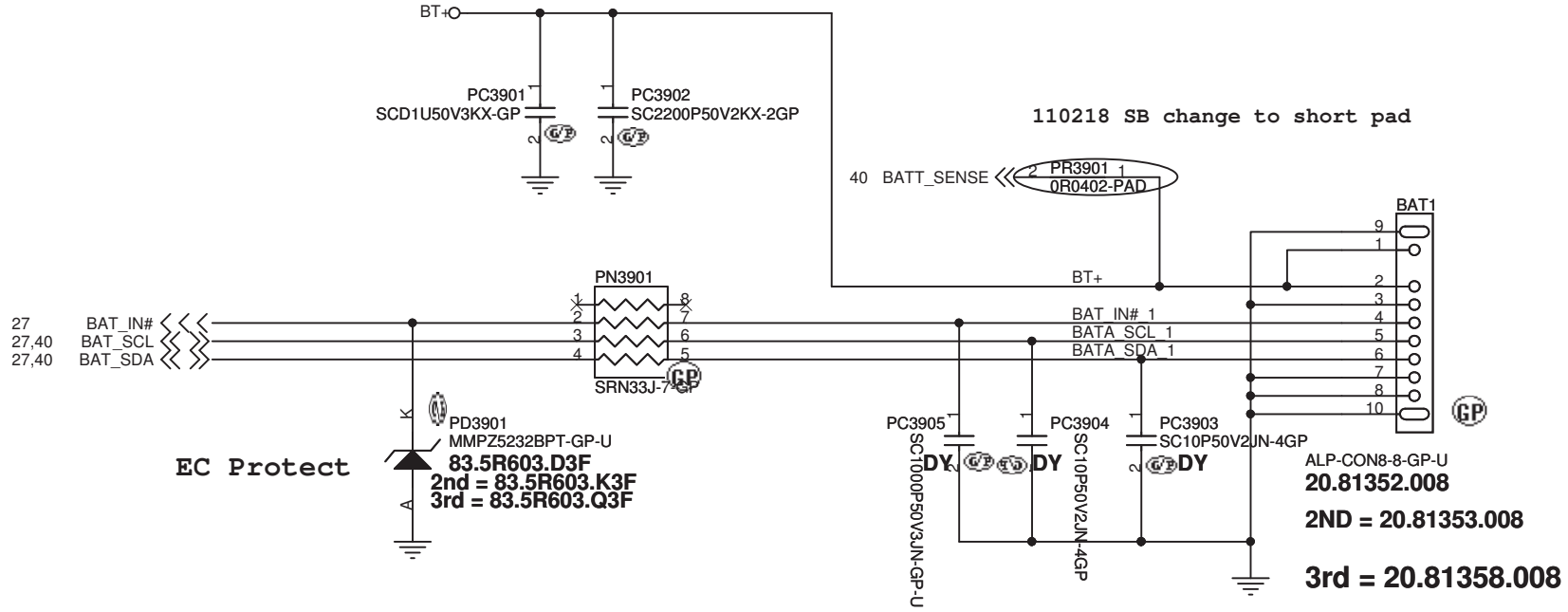
Adaptor in to generate DCBATOUT




<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DCIN JACK	
Size A4	Document Number JE50 SB
Date: Friday, April 01, 2011	Rev SB
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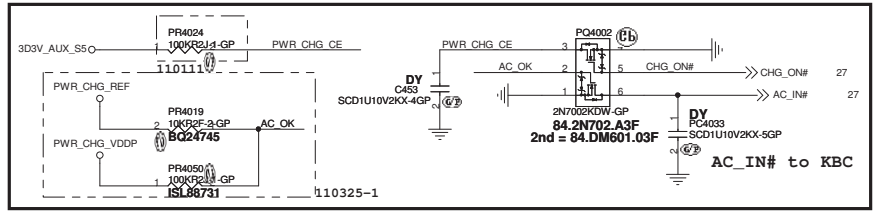
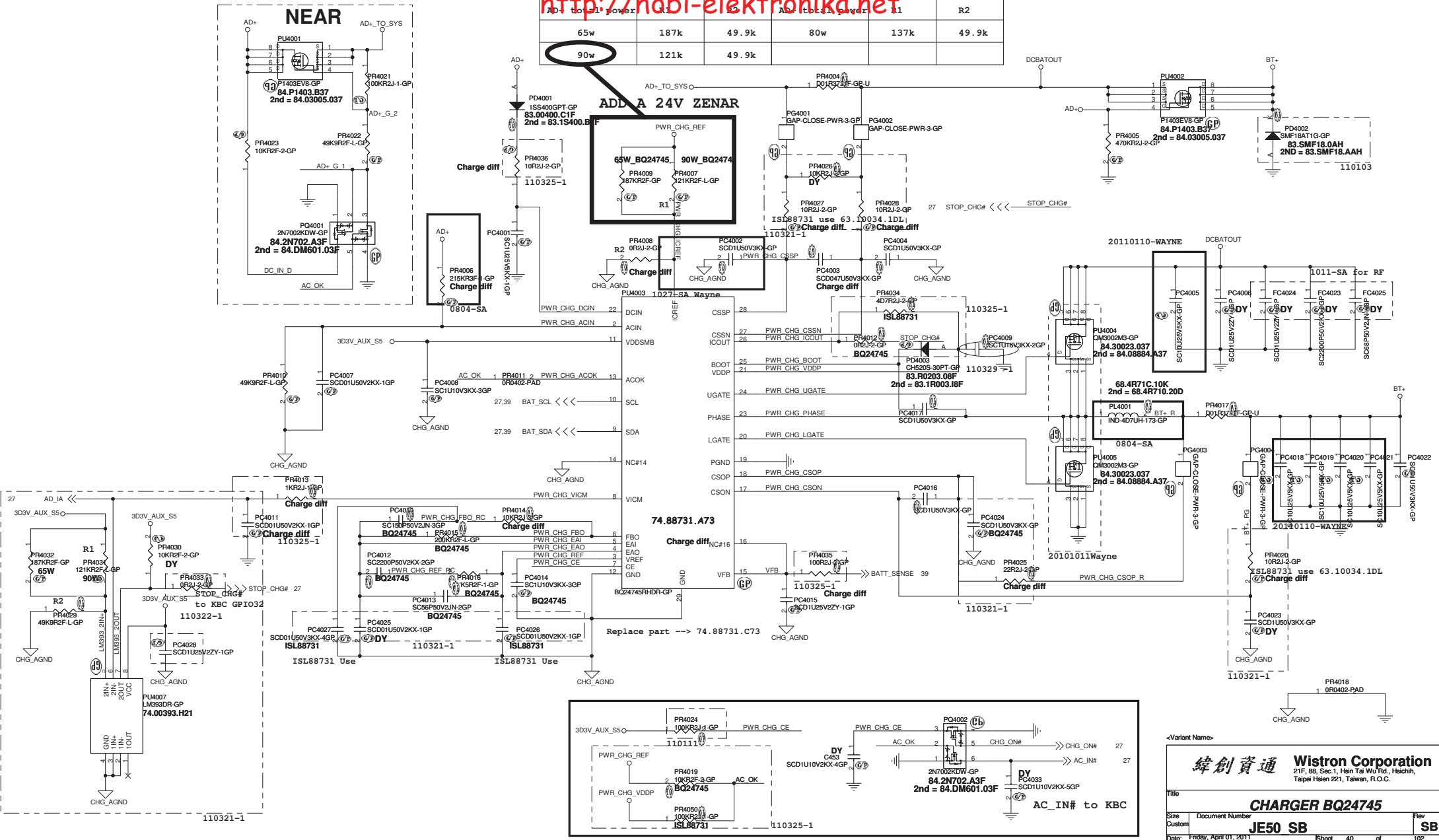
BATTERY CONNECTOR



<Variant Name>

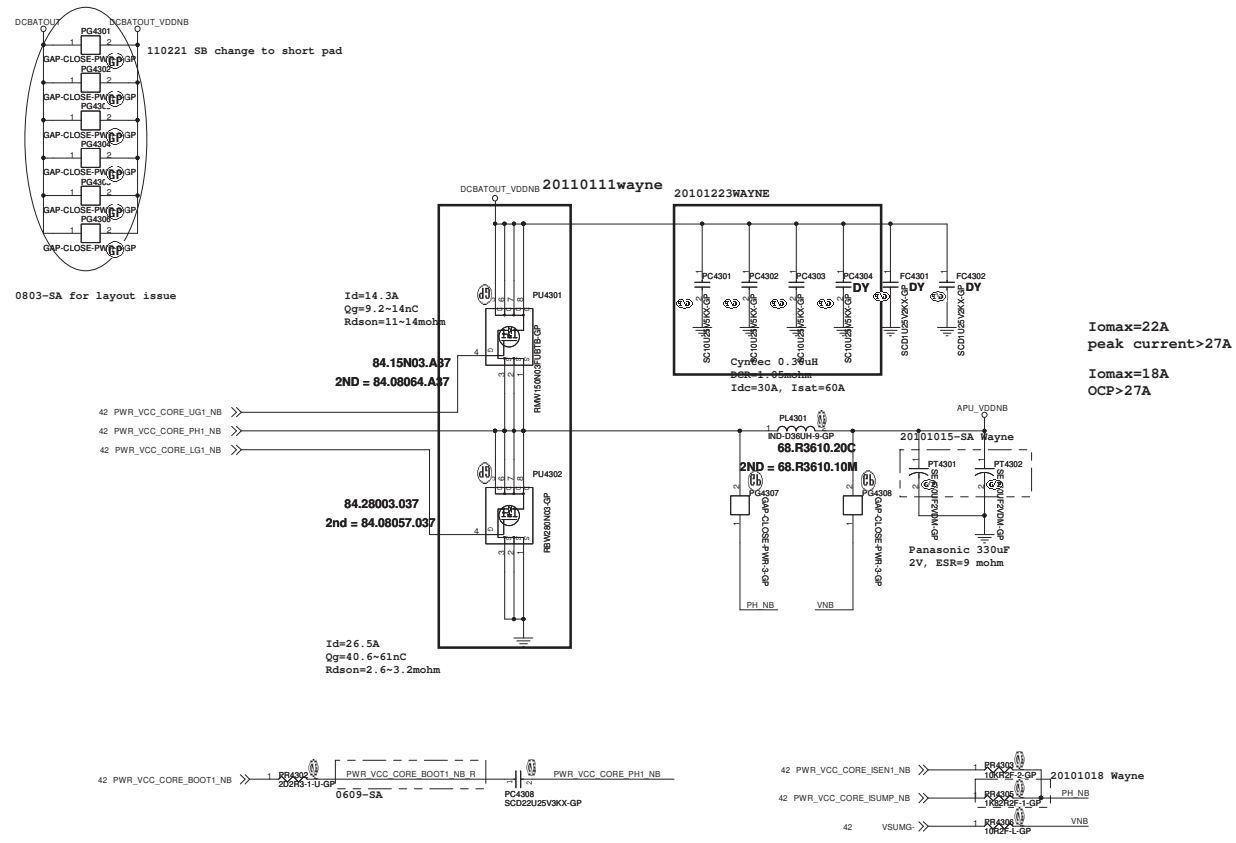
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BATT CONN	
Size A4	Document Number JE50 SB
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AD+ TO SYS	Power	R1	R2
	65w	187k	49.9k
	80w	137k	49.9k
	90w	121k	49.9k

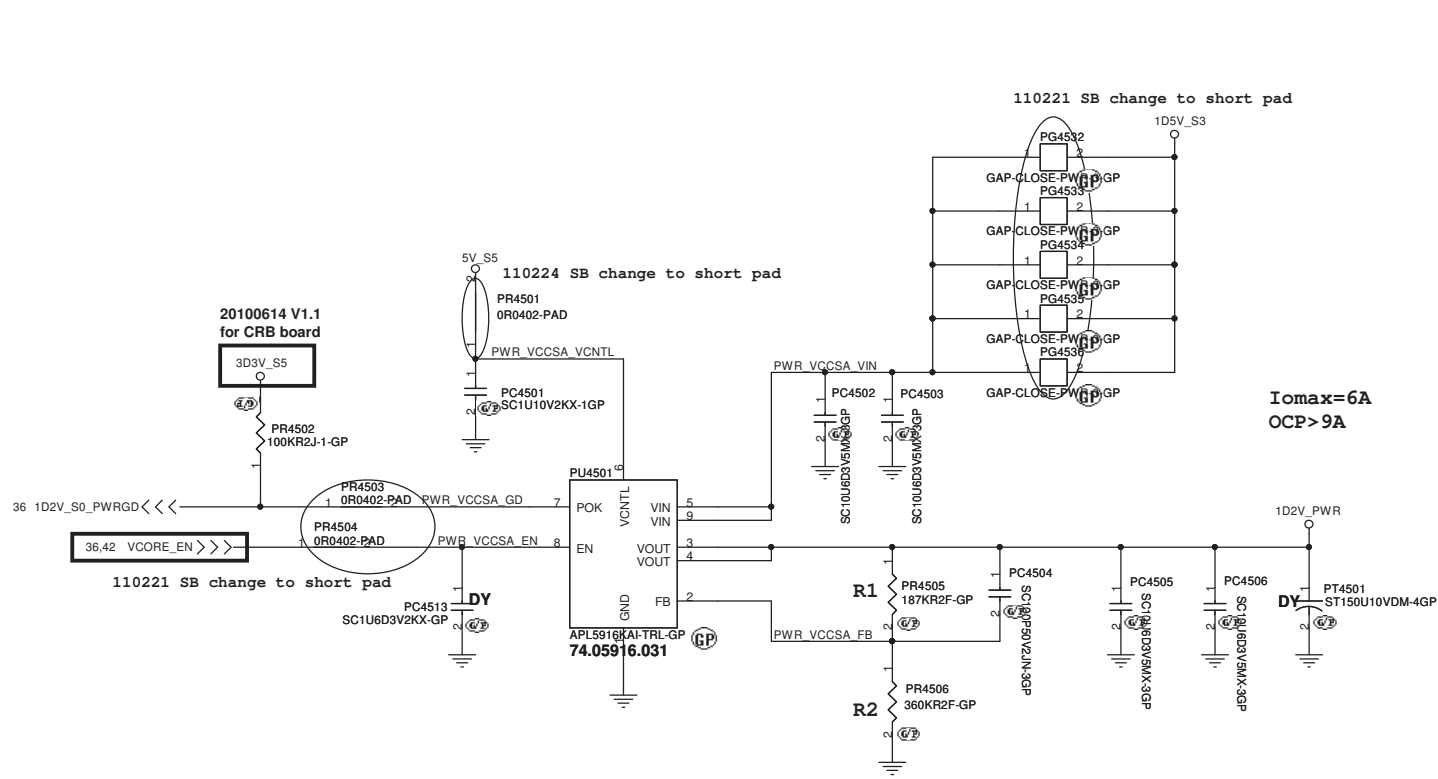


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichü,
 Taipei Hsien 221, Taiwan, R.O.C.

CHARGER BQ24745
 JE50 SB
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APL5916 for VDDR&VDDP(1D2V_S0)



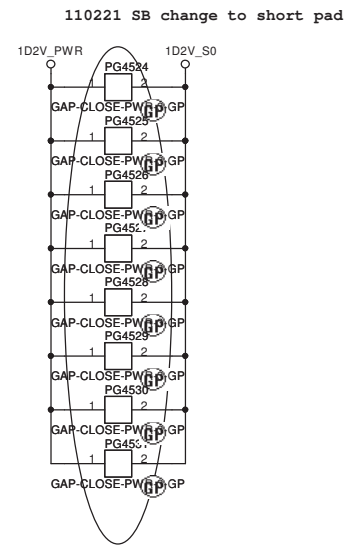
110221 SB change to short pad

110224 SB change to short pad

20100614 V1.1 for CRB board

110221 SB change to short pad

I_{omax} = 6A
OCP > 9A



<Variant Name>		
緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
APL5916(1D2V_S0)		
Size A3	Document Number	Rev
	JE50 SB	SB
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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

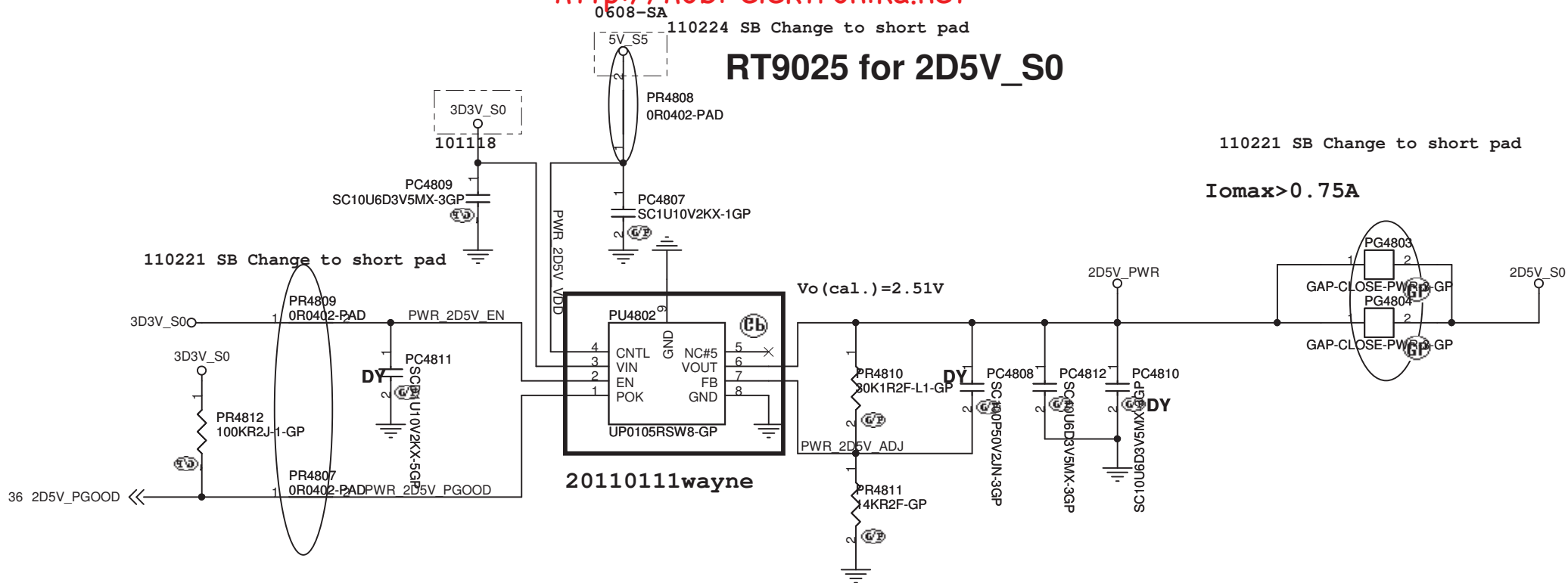
SB

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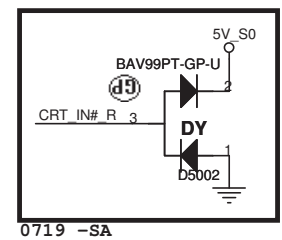
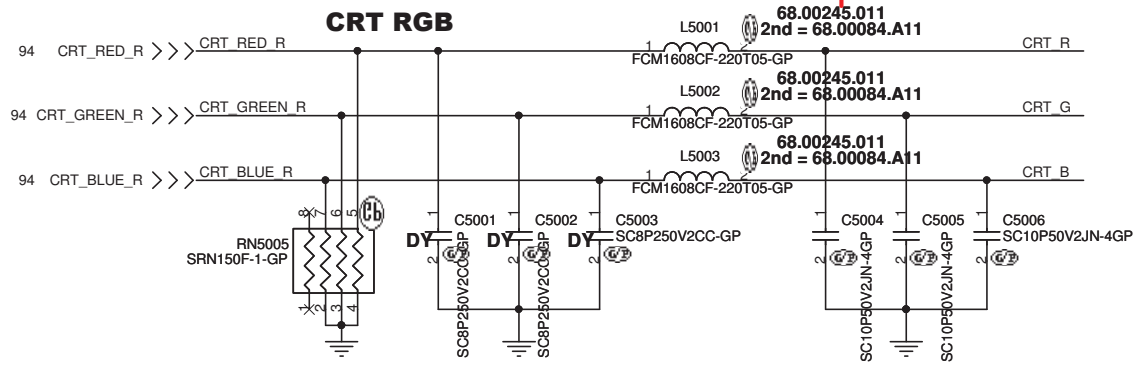
102

RT9025 for 2D5V_S0

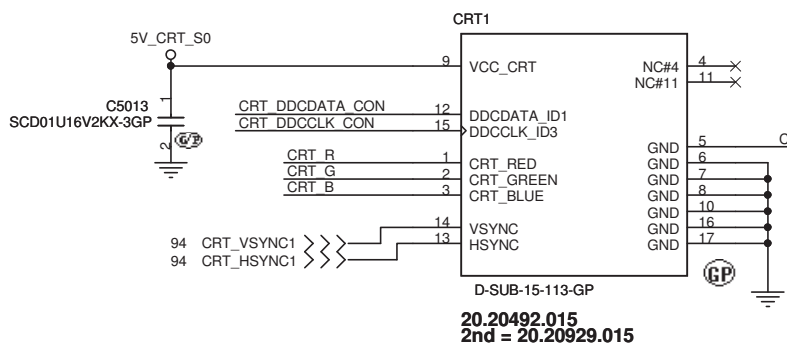


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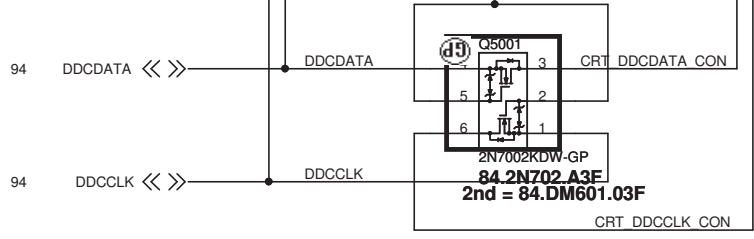
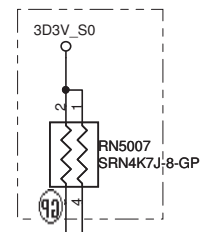
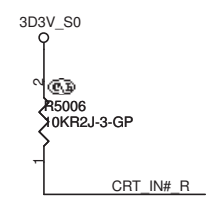
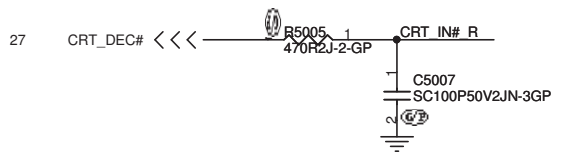
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RT9025(2D5V S0)			
Size A4	Document Number JE50 SB		Rev SB
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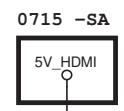
0719 -SA



20.20492.015
2nd = 20.20929.015

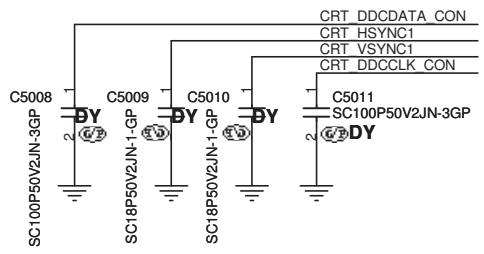


84.2N702.A3E
2nd = 84.DM601.03F



0715 -SA

500mA
D5001 CH551H-30PT-GP
83.R5003.C8F
2nd = 83.R5003.H8H
3rd = 83.5R003.08F



<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Connector			
Size	Document Number	Rev	
Custom	JE50 SB	SB	
Date:	Friday, April 01, 2011	Sheet	50 of 102

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

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SB

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<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	
Reserved	

Size	Document Number	Rev
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<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	
Reserved	

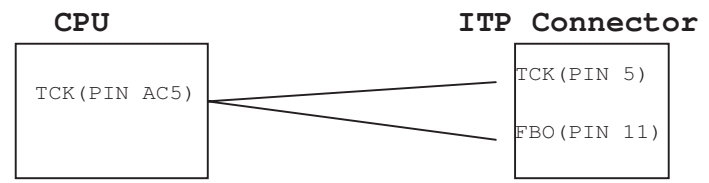
Size	Document Number	Rev
A4	JE50 SB	SB

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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Variant Name>

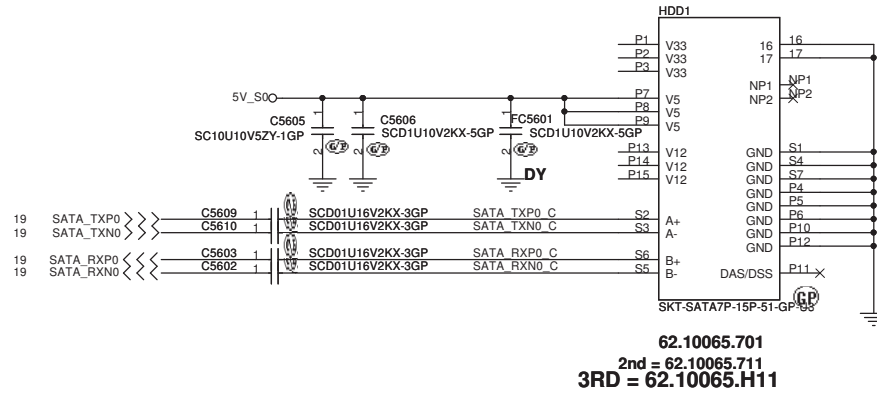
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title ***ITP***

Size A4	Document Number JE50 SB	Rev SB
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SSID = SATA

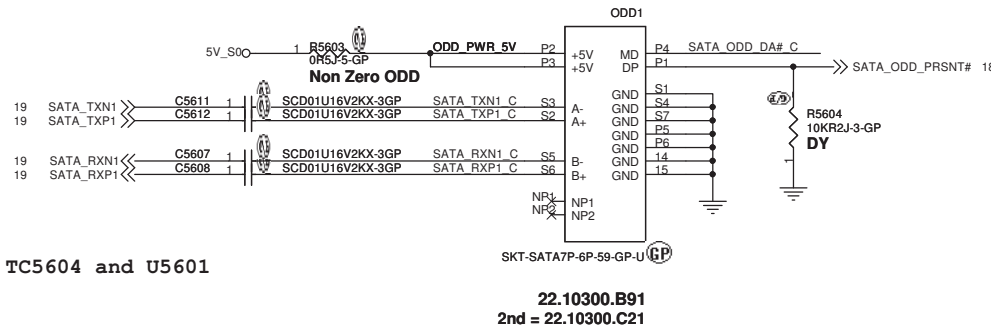
<http://hobi-elektronika.net>
SATA HDD Connector



ODD Connector

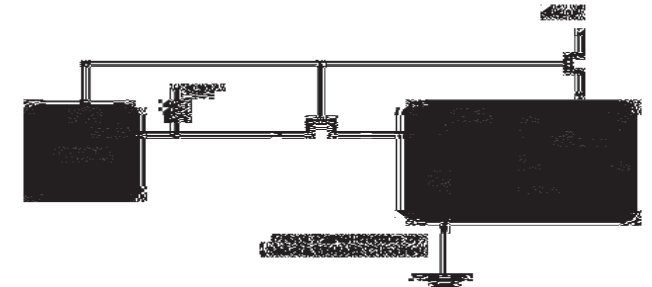
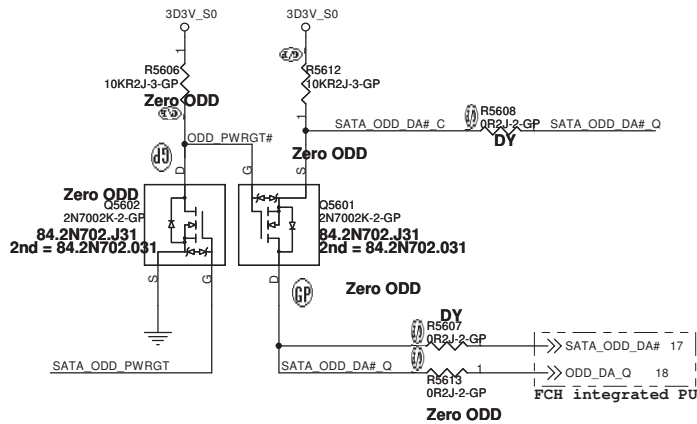
SATA_RX- and SATA_RX+ Trace
 Length match within 10 mil

Following AMD routing table

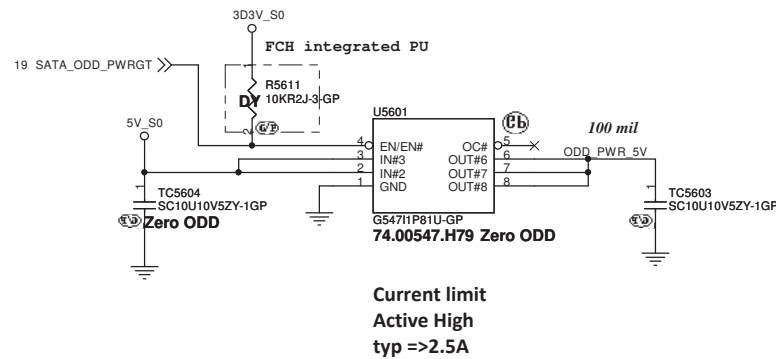


If support Zero Power ODD

Stuff R5604, R5612, Q5601 and R5613 TC5604 and U5601
 DY R5603



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
 When the drive is powered off, the FET to the MD/DA pin is ON



<Variant Name>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDD/ODD	
Size A3	Document Number JE50 SB
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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ESATA/USB Charger

Size

A4

Document Number

JE50 SB

Rev

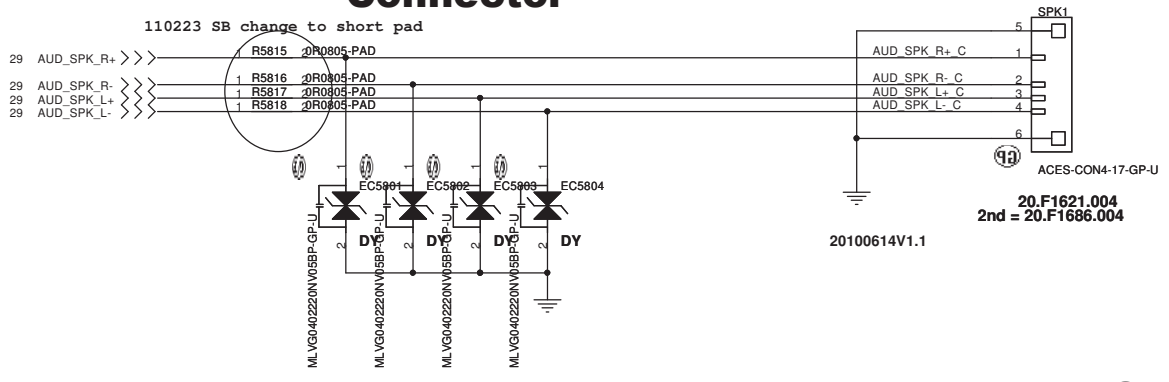
SB

Date: Friday, April 01, 2011

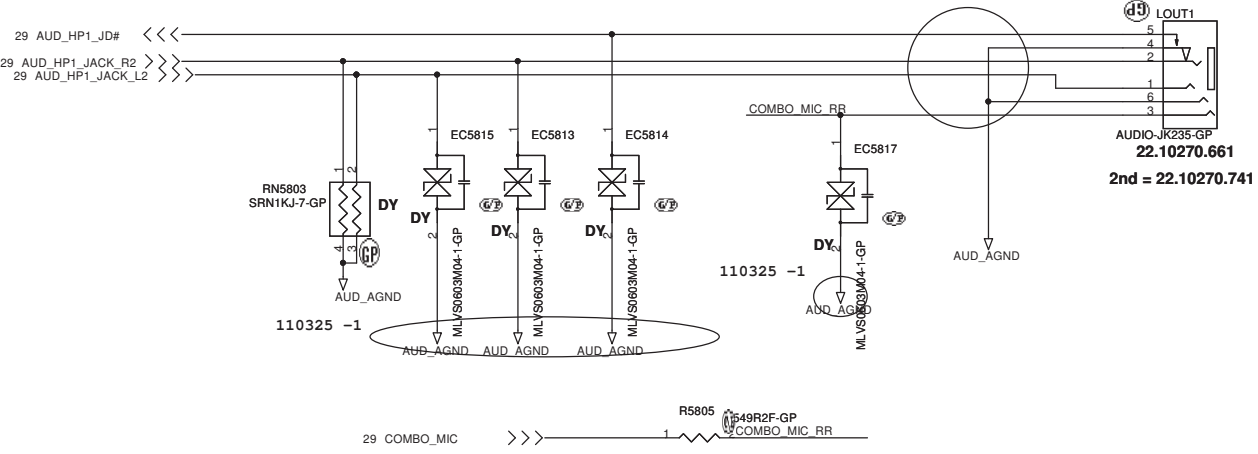
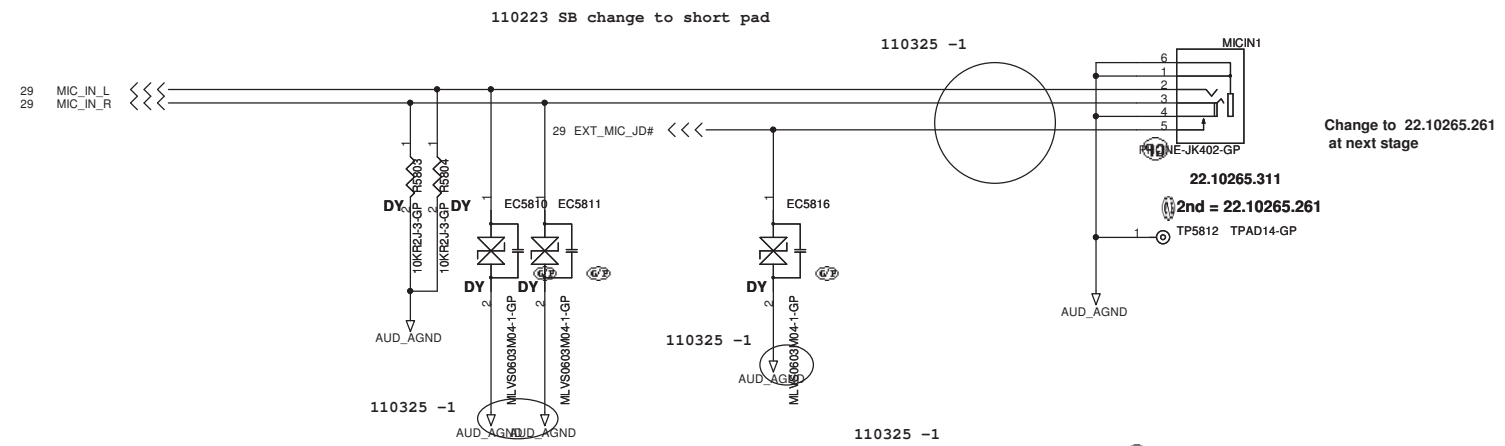
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SSID = AUDIO

Speaker Connector



MIC IN



<Variant Name>

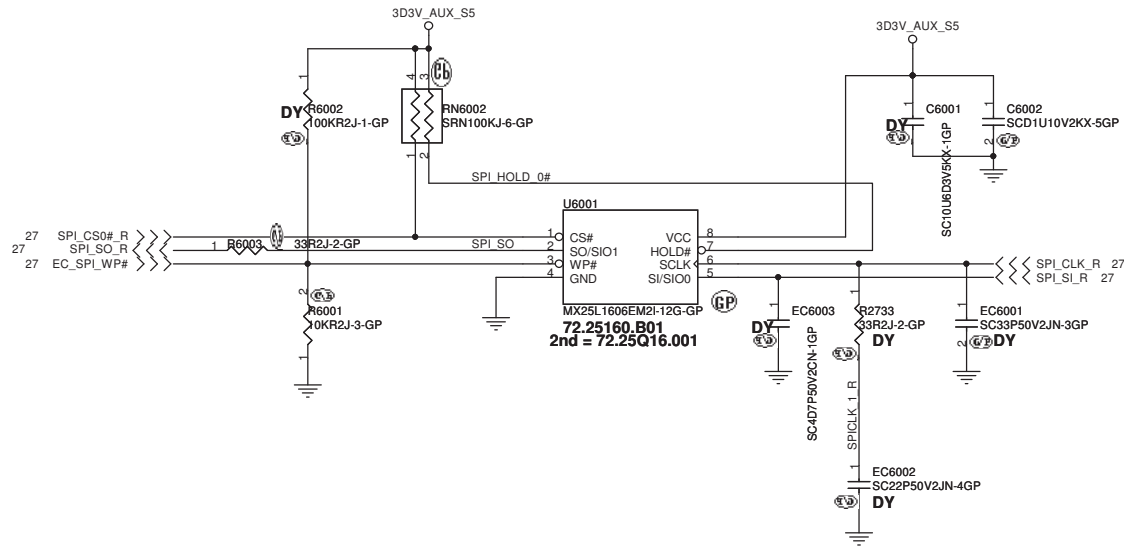
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

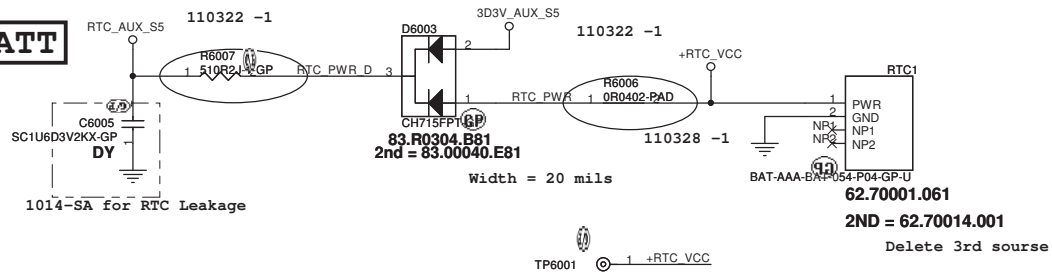
Size A3 Document Number: **JE50 SB** Rev: **SB**


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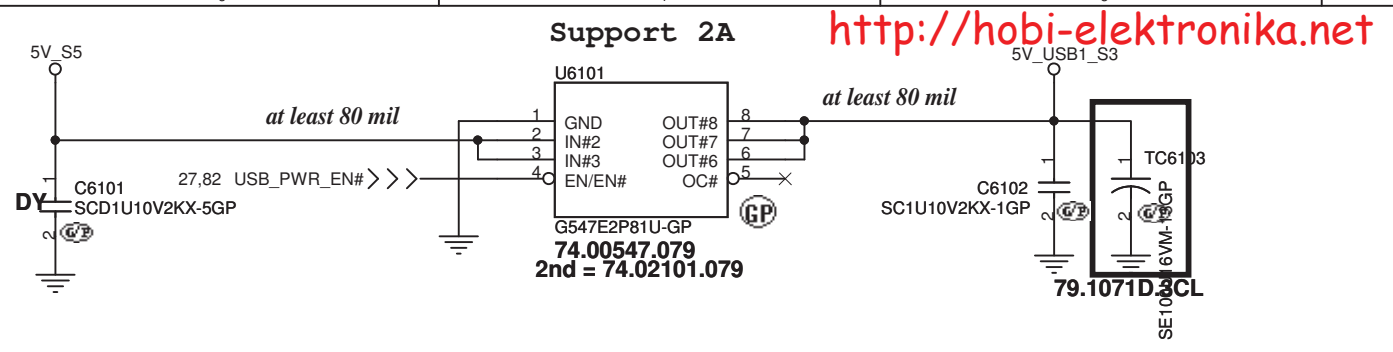
SPI FLASH ROM (2M byte) for KBC <http://hobi-elektronika.net>



SSID = RBATT



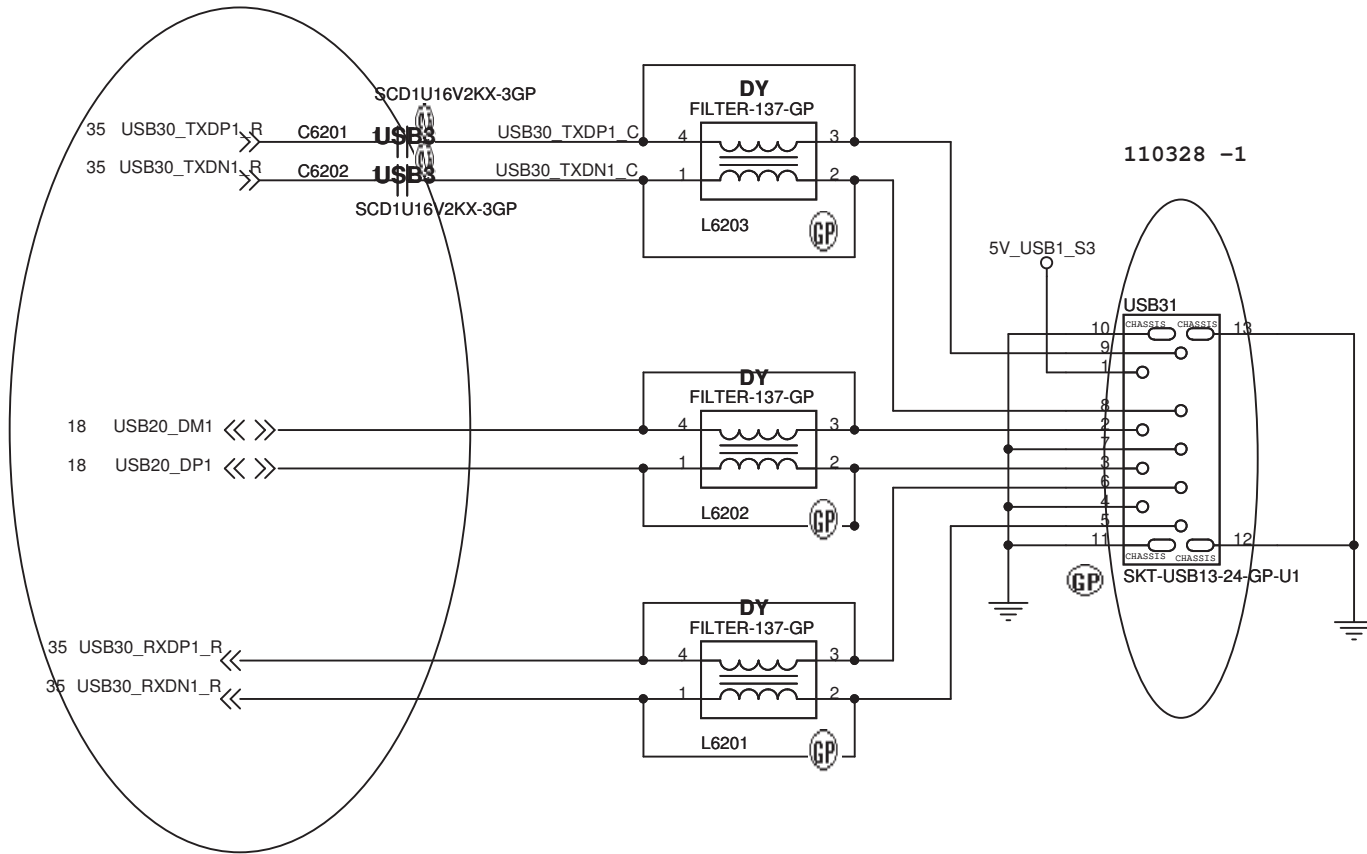
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Flash/RTC		
Size A3	Document Number JE50 SB	Rev SB
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<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
USB Power SW		
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110221 SB Change from port2 to port1



**USB 3.0 Connector
Pin definition**

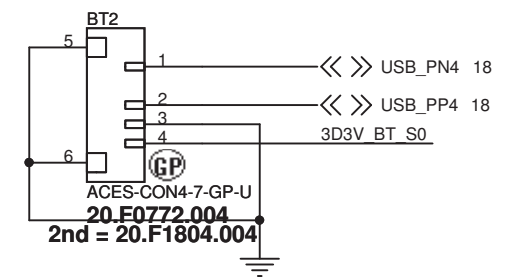
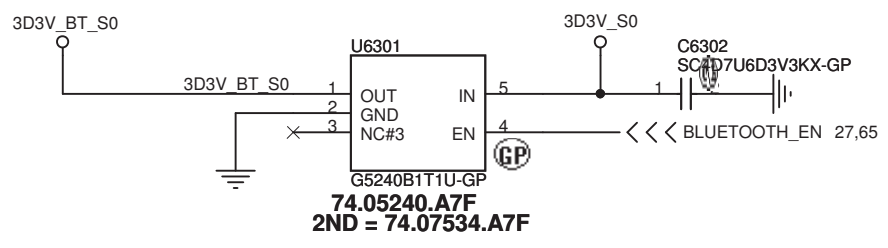
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB 3.0	
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ANNIE Bluetooth Module

1.5A / High Active Voltage 2V



<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
BLUE TOOTH		
Size A4	Document Number JE50 SB	Rev SB
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<Variant Name>

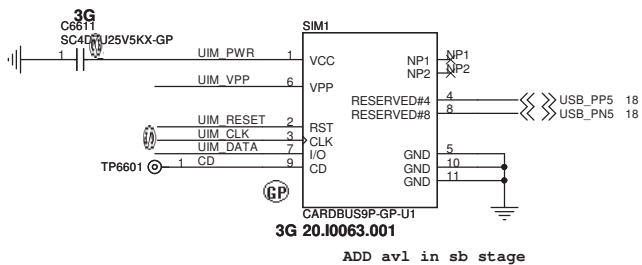
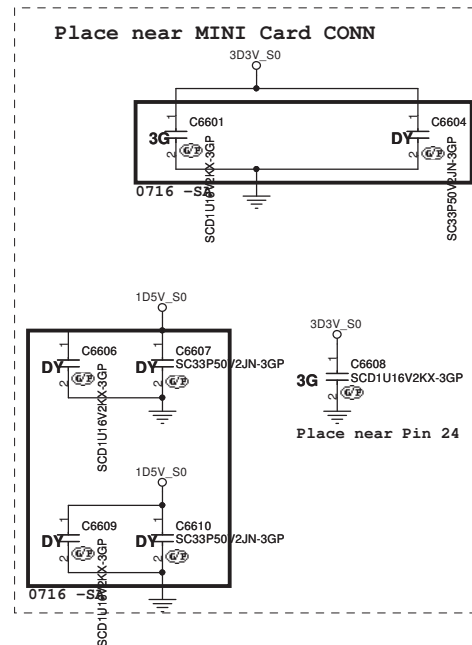
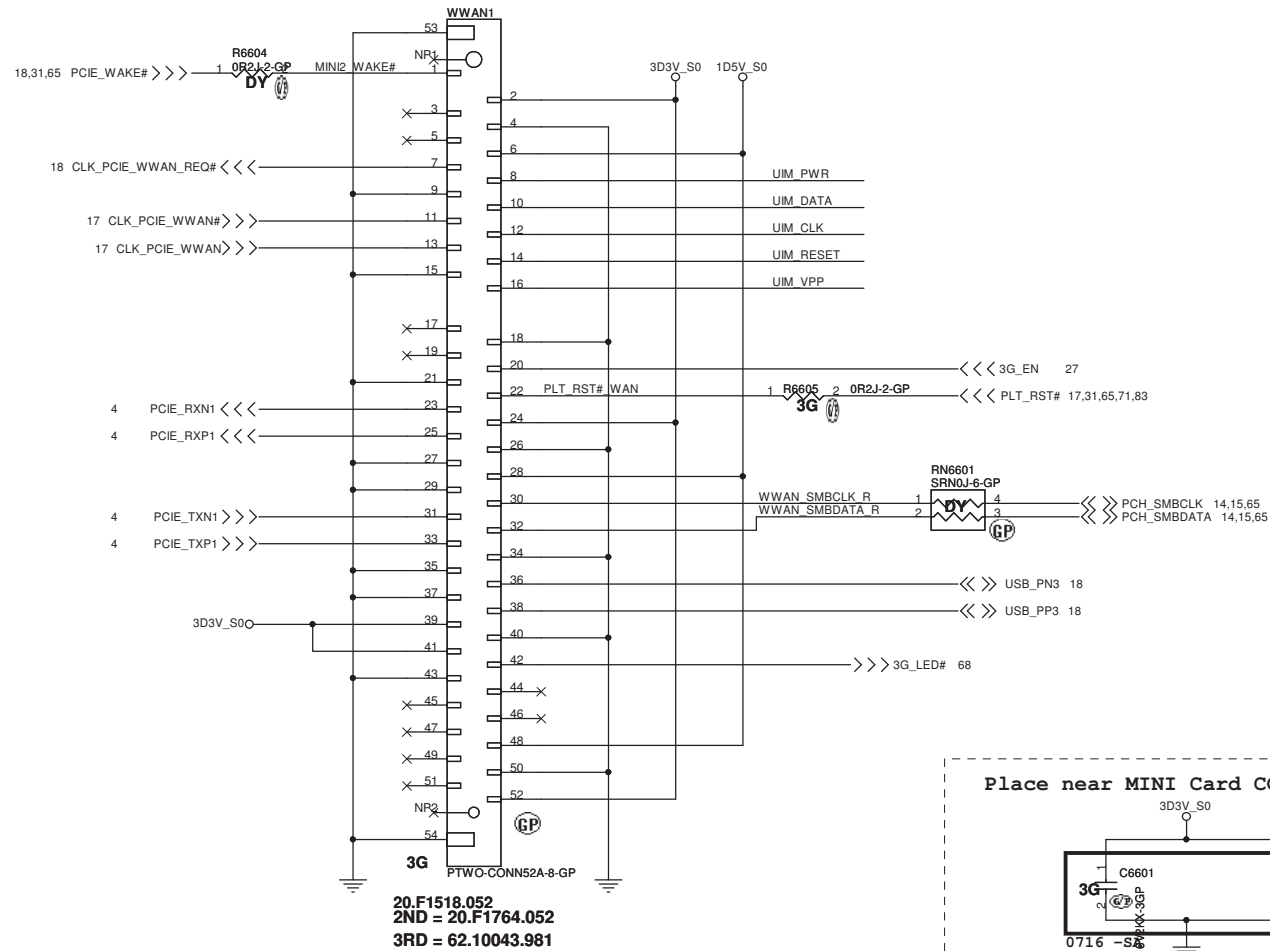
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	
Reserved	

Size	Document Number	Rev
A4	JE50 SB	SB

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Mini Card Connector(WWAN) <http://hobi-elektronika.net>



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
WWAN		
Size	Document Number	Rev
A3	JE50 SB	SB
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<Variant Name>

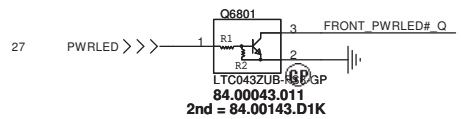
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	
Reserved	

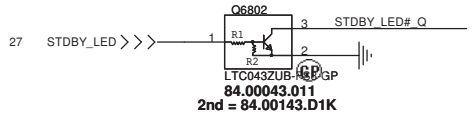
Size	Document Number	Rev
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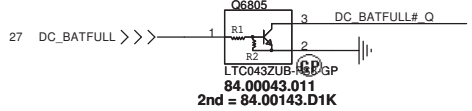
Power button LED



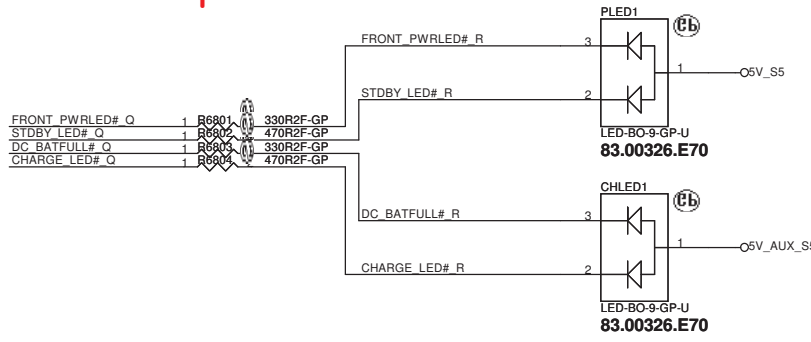
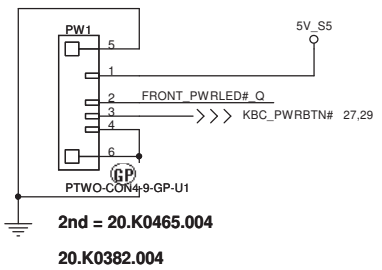
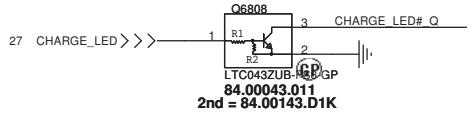
Power STDBY_LED



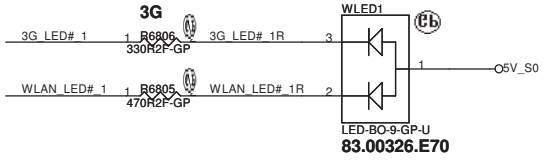
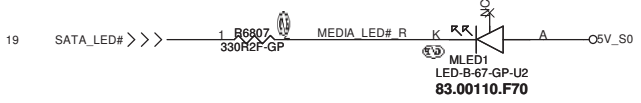
Battery LED2 (DC_BATFULL)



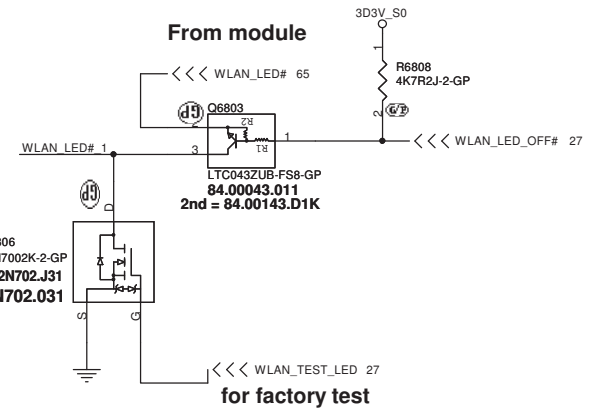
Battery LED1 (CHARGE)



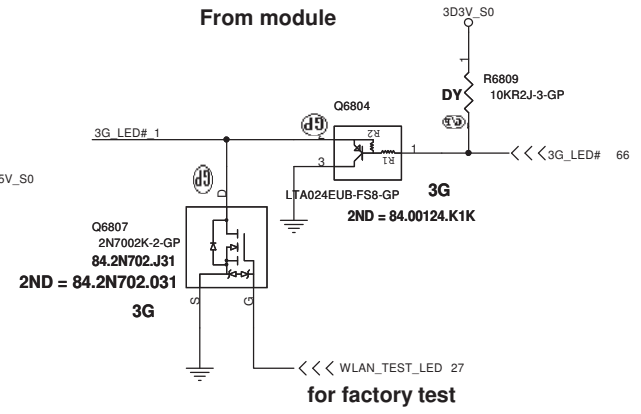
SATA HDD LED

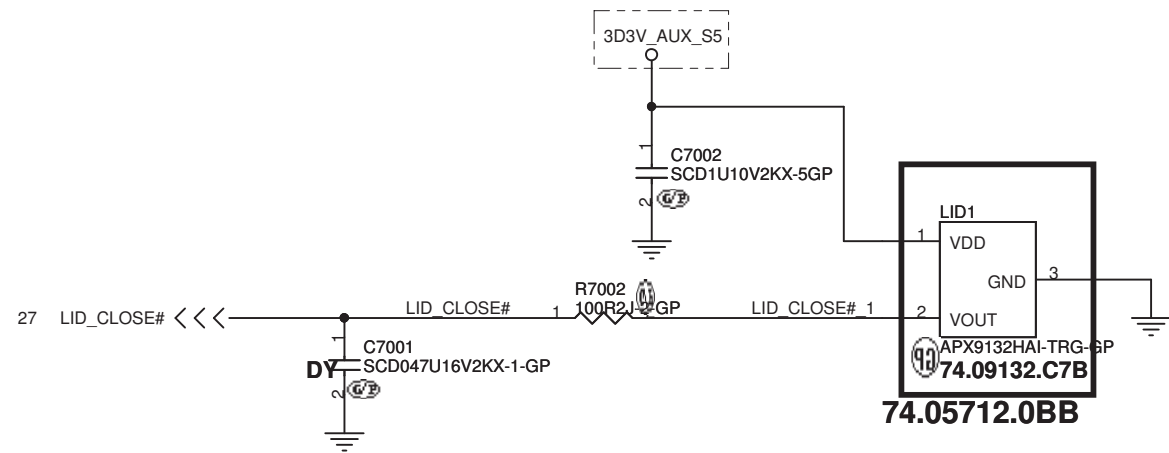


WLAN_LED



3G LED





<Variant Name>

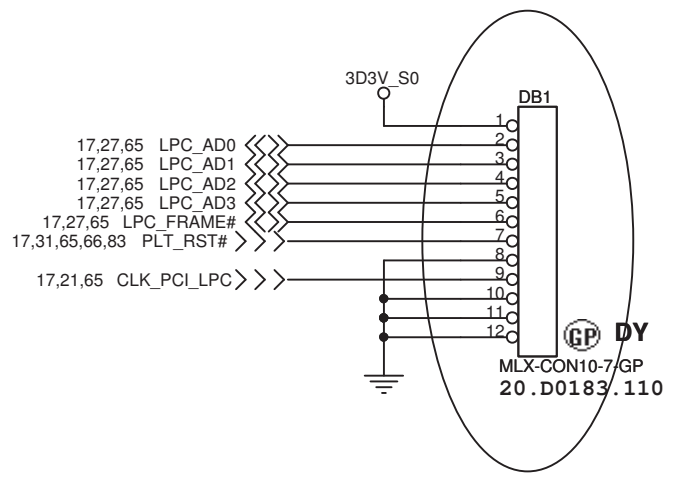
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Hall Sensor**

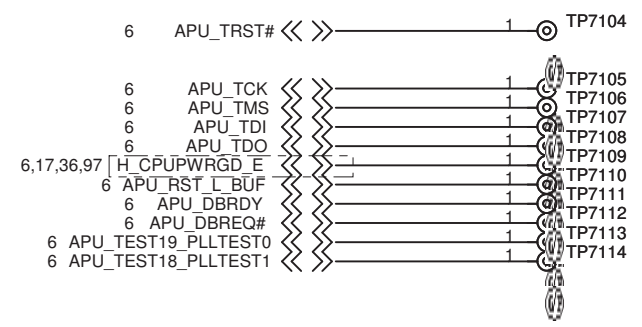
Size A4 Document Number **JE50 SB** Rev **SB**

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110218 SB BOM Change



HDT+ Connectors



CRB:placed 0-ohm
 Checklist: If both SCAN and HDT+ header are implement
 placed 15-ohm

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
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<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
Reserved		

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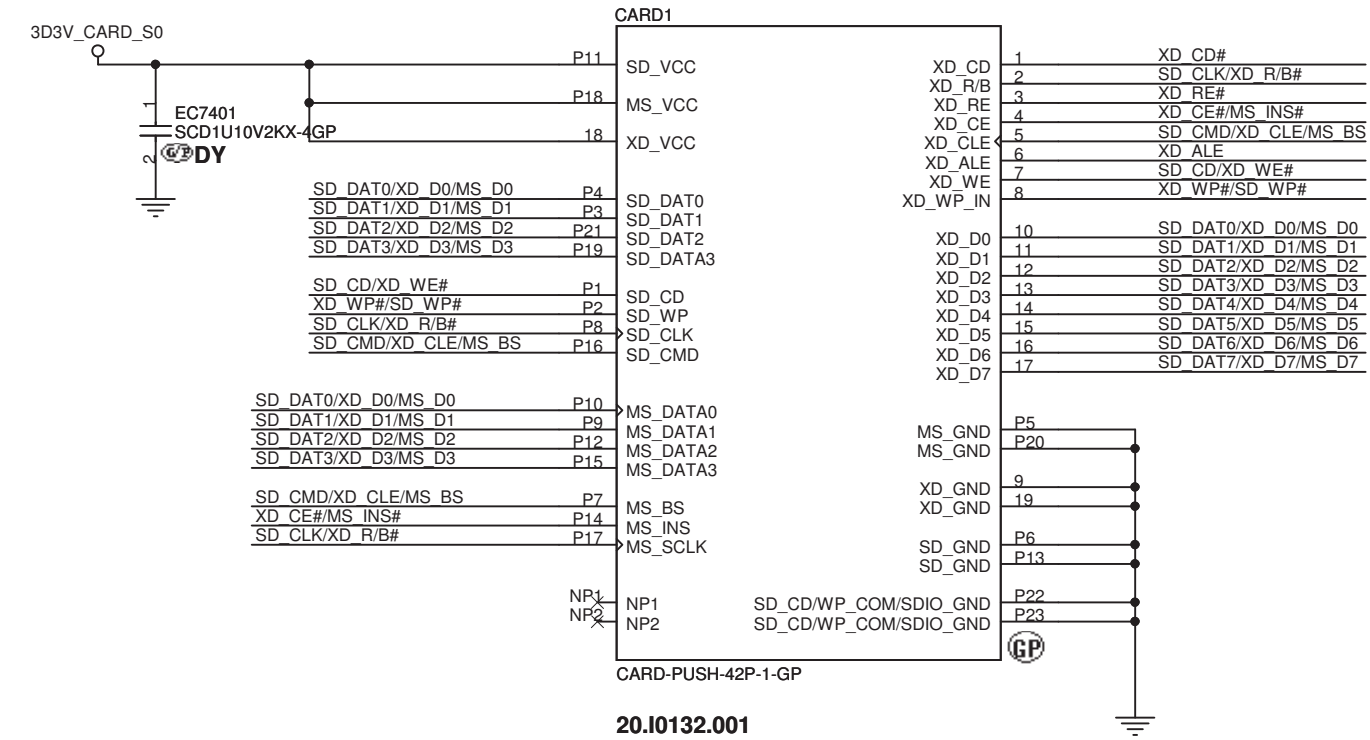
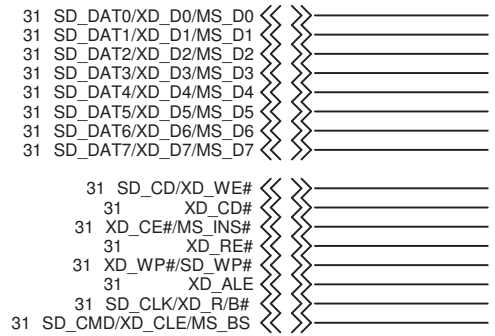
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	JE50 SB		SB
Date:	Friday, April 01, 2011	Sheet 73 of	102

<http://hobi-elektronika.net>
SD/XD/MS Card Reader

SSID = SDIO



Pin	Signal	Function
1	SD_VCC	Power
2	XD_CD	Card Detect
3	XD_R/B	Reset
4	XD_RE	Reset Enable
5	XD_CE#/MS_INS#	Chip Enable
6	XD_CLE	Command Latch Enable
7	XD_ALE	Address Latch Enable
8	XD_WE#	Write Enable
9	XD_WP#/SD_WP#	Write Protect
10	XD_D0	Data 0
11	XD_D1	Data 1
12	XD_D2	Data 2
13	XD_D3	Data 3
14	XD_D4	Data 4
15	XD_D5	Data 5
16	XD_D6	Data 6
17	XD_D7	Data 7
18	MS_VCC	Power
19	SD_DATA3	Data 3
20	MS_GND	Ground
21	SD_DATA2	Data 2
22	MS_DATA2	Data 2
23	SD_DATA1	Data 1
24	MS_DATA1	Data 1
25	SD_DATA0	Data 0
26	MS_DATA0	Data 0
27	SD_CMD	Command
28	MS_SCLK	Serial Clock
29	SD_CD/WP_COM/SDIO_GND	Control/IO Ground
30	SD_CD/WP_COM/SDIO_GND	Control/IO Ground
31	SD_CMD/XD_CLE/MS_BS	Command/Block Strobe
32	SD_CLK/XD_R/B#	Clock/Reset
33	SD_CE#/MS_INS#	Chip Enable
34	SD_CD/XD_WE#	Card Detect/Write Enable

Pin	Signal	Function
1	SD_VCC	Power
2	XD_CD	Card Detect
3	XD_R/B	Reset
4	XD_RE	Reset Enable
5	XD_CE#/MS_INS#	Chip Enable
6	XD_CLE	Command Latch Enable
7	XD_ALE	Address Latch Enable
8	XD_WE#	Write Enable
9	XD_WP#/SD_WP#	Write Protect
10	XD_D0	Data 0
11	XD_D1	Data 1
12	XD_D2	Data 2
13	XD_D3	Data 3
14	XD_D4	Data 4
15	XD_D5	Data 5
16	XD_D6	Data 6
17	XD_D7	Data 7
18	MS_VCC	Power
19	SD_DATA3	Data 3
20	MS_GND	Ground
21	SD_DATA2	Data 2
22	MS_DATA2	Data 2
23	SD_DATA1	Data 1
24	MS_DATA1	Data 1
25	SD_DATA0	Data 0
26	MS_DATA0	Data 0
27	SD_CMD	Command
28	MS_SCLK	Serial Clock
29	SD_CD/WP_COM/SDIO_GND	Control/IO Ground
30	SD_CD/WP_COM/SDIO_GND	Control/IO Ground
31	SD_CMD/XD_CLE/MS_BS	Command/Block Strobe
32	SD_CLK/XD_R/B#	Clock/Reset
33	SD_CE#/MS_INS#	Chip Enable
34	SD_CD/XD_WE#	Card Detect/Write Enable

<Variant Name>
 Card-reader Off-Page

緯創資通 **Wistron Corporation**
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Title: **CARD Reader CONN**

Size: A4 | Document Number: **JE50 SB** | Rev: **SB**

Date: Friday, April 01, 2011 | Sheet 74 of 102

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<Variant Name>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

SB

Date: Friday, April 01, 2011

Sheet 75 of 102

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

SB

Date: Friday, April 01, 2011

Sheet 76 of 102

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

SB

Date: Friday, April 01, 2011

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102

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<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

JE50 SB

Rev
SB

Date: Friday, April 01, 2011

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<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

SB

Date: Friday, April 01, 2011

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

SB

Date: Friday, April 01, 2011

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

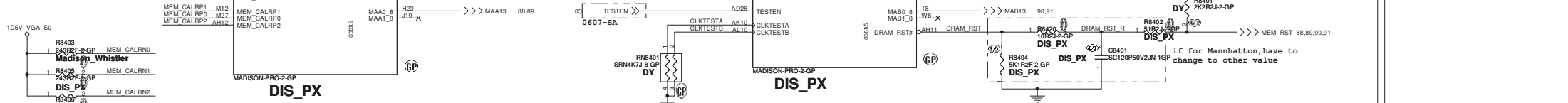
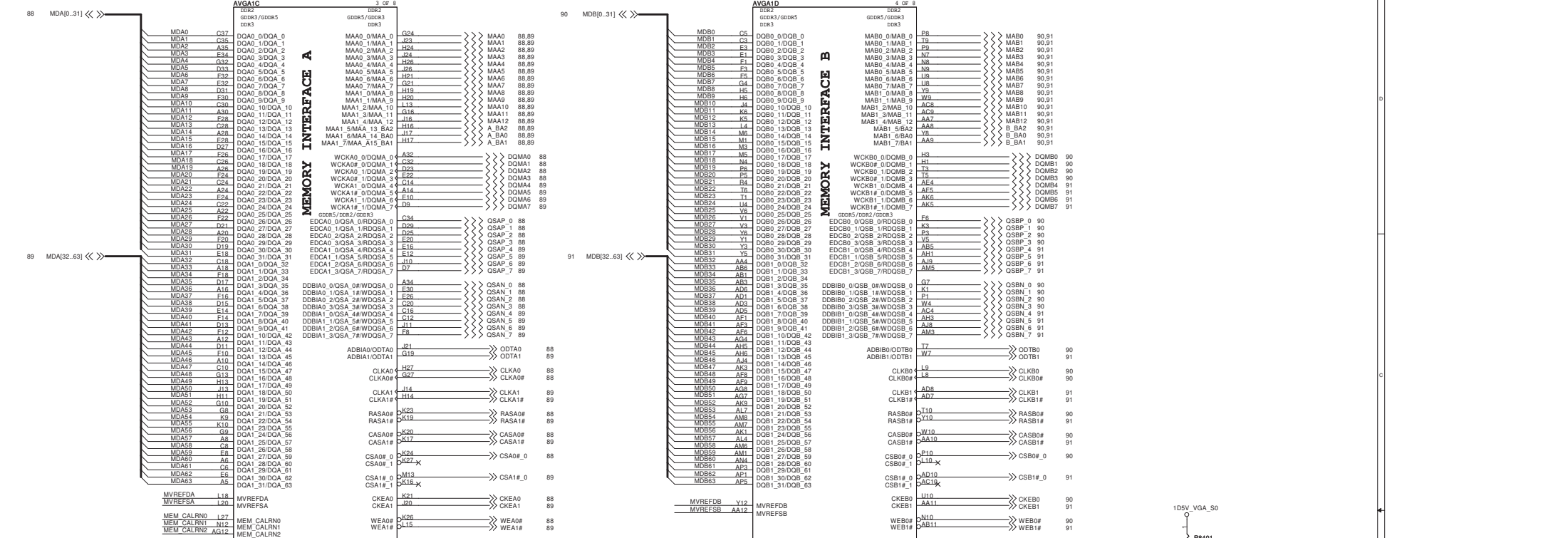
JE50 SB

Rev

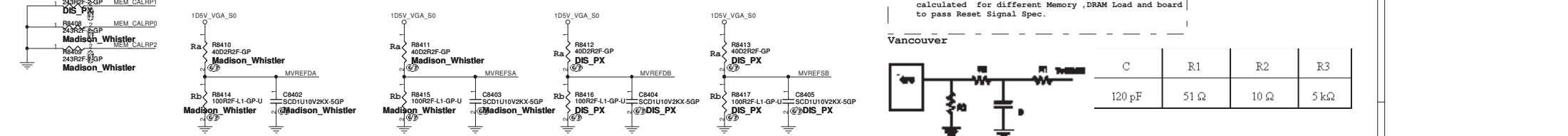
SB

Date: Friday, April 01, 2011

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PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

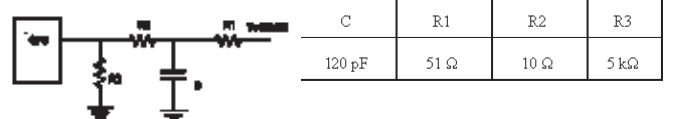


DDR3/GDDR3 Memory Stuff Option(Mad/Park)

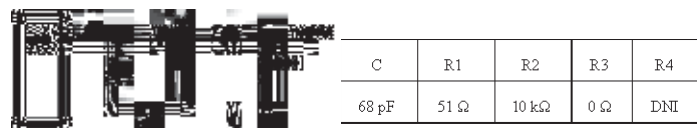
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Vancouver



Mannhattan



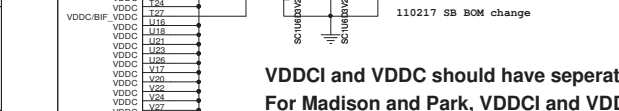
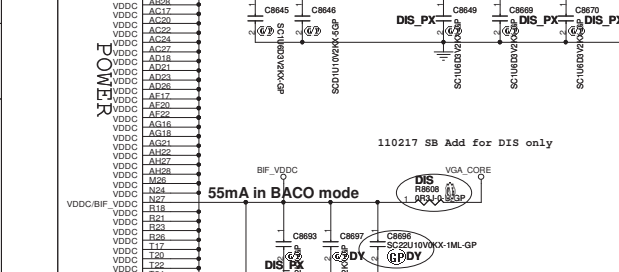
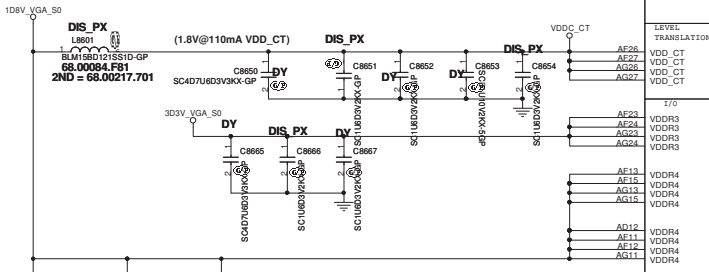
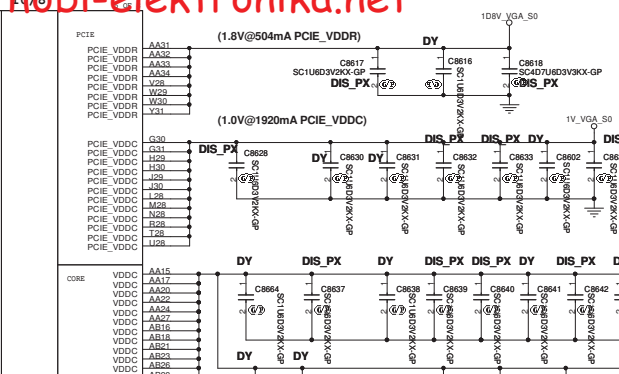
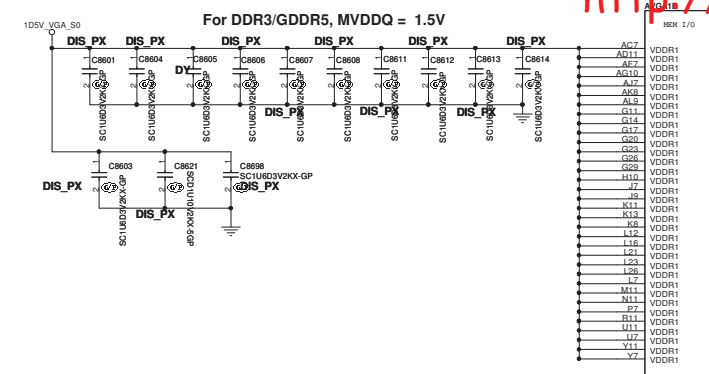
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

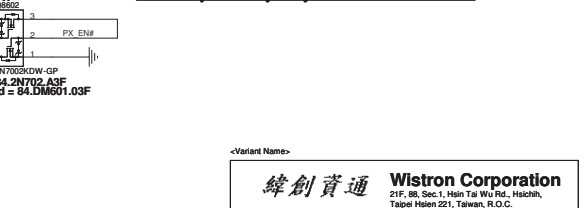
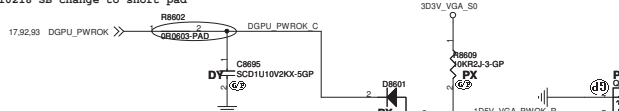
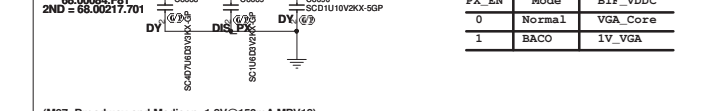
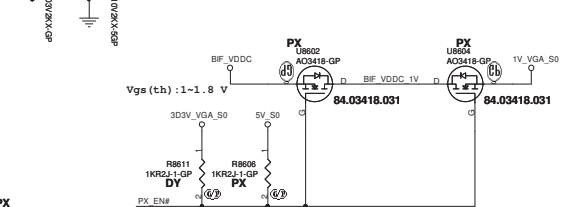
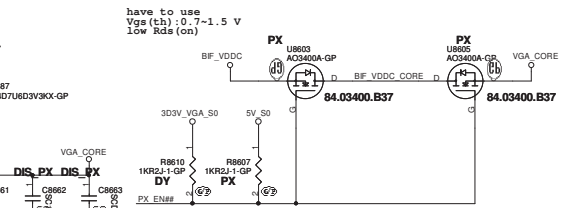
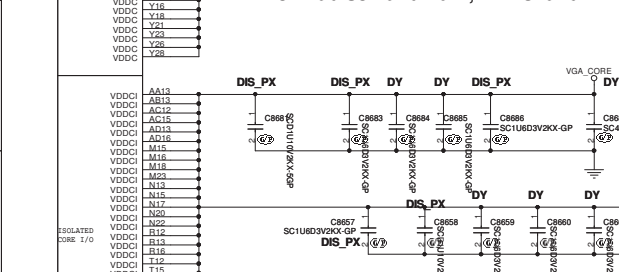
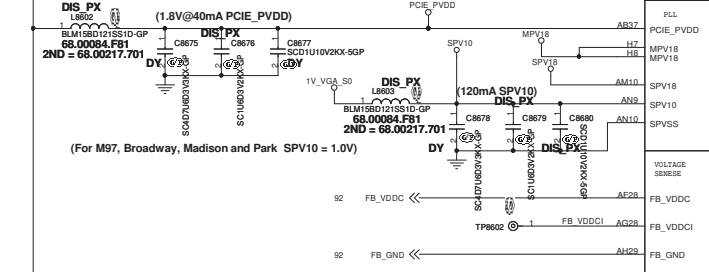
Title: GPU Memory(2/5)

Size: Document Number: JE50 SB Rev: SB

Date: Friday, April 01, 2011 Sheet: 84 of 102



VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator



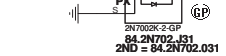
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

110218 SB change to short pad

17.92.93 DGPU_PWROK >> R8602



92 8209A_ENDMEM_VGA <<<



ESD Protected: 2KV



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緯創資通

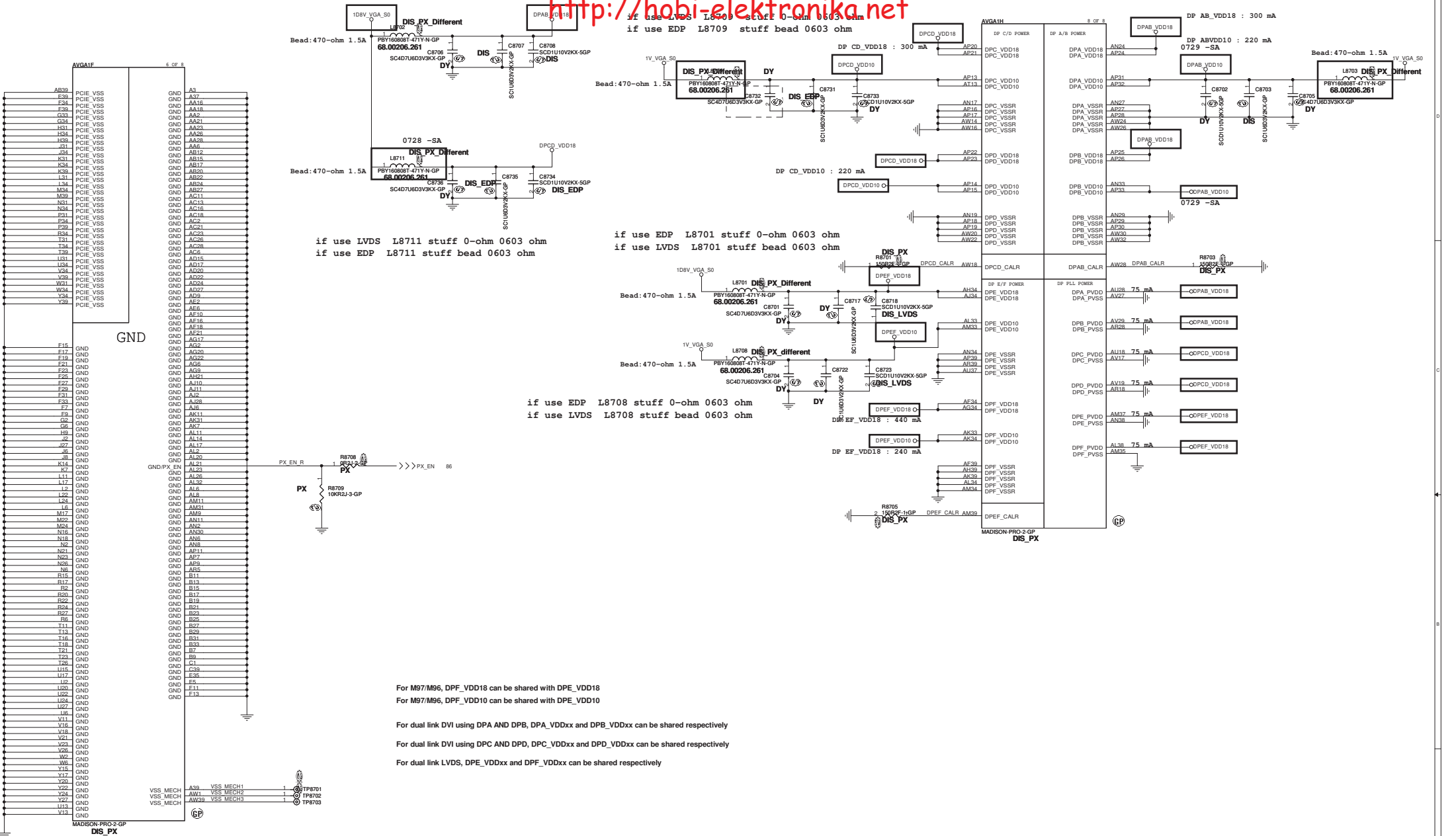
GPU POWER(4/5)

JE50 SB

Rev SB

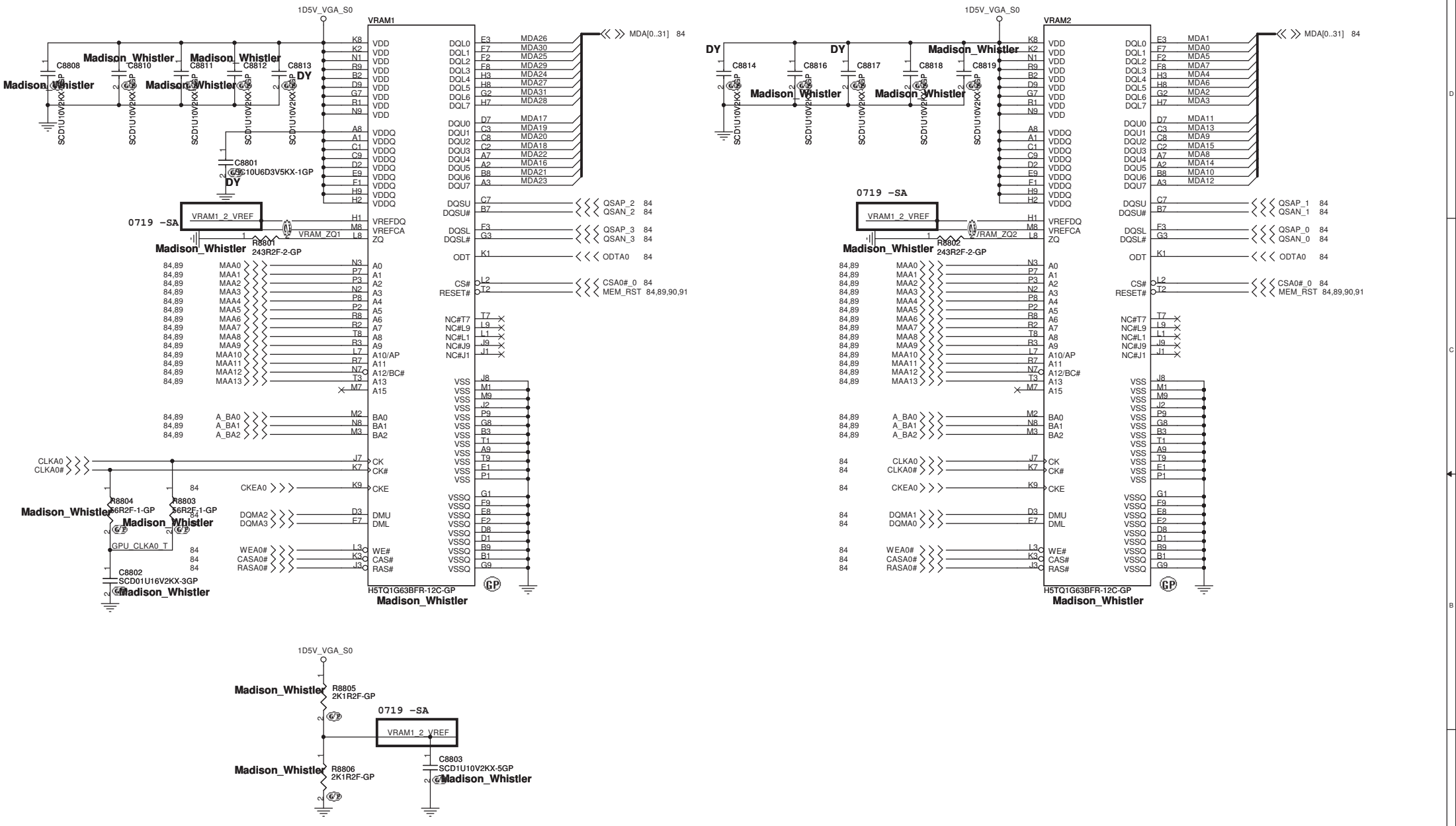
Date: Friday, April 01, 2011

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For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
 For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
 For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
 For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively



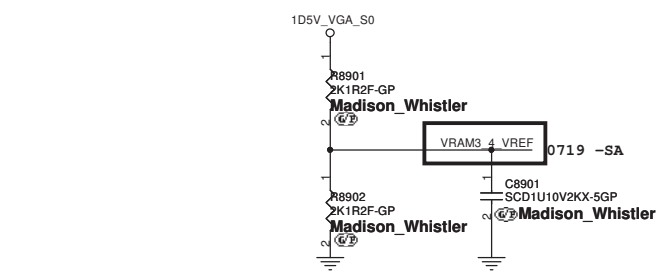
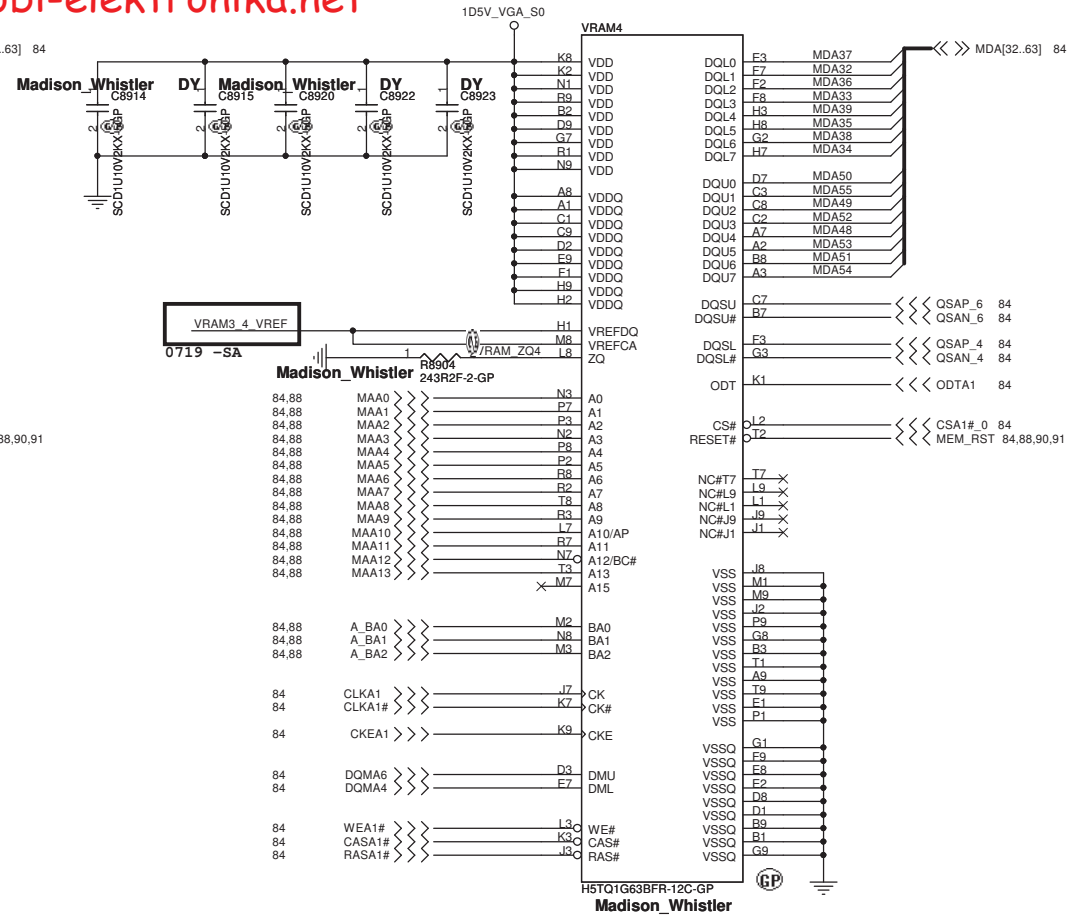
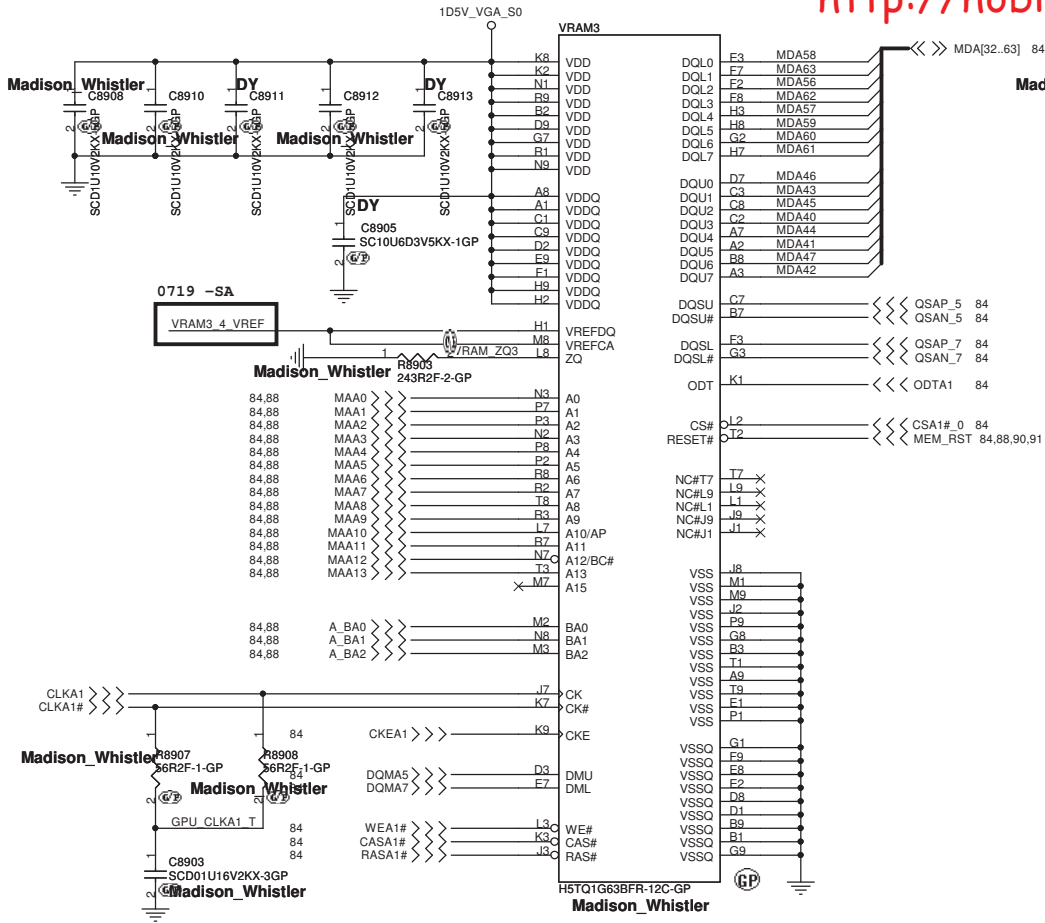
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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

Size A3 Document Number **JE50 SB** Rev **SB**

Date: Friday, April 01, 2011 Sheet 88 of 102

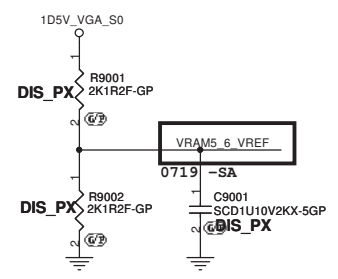
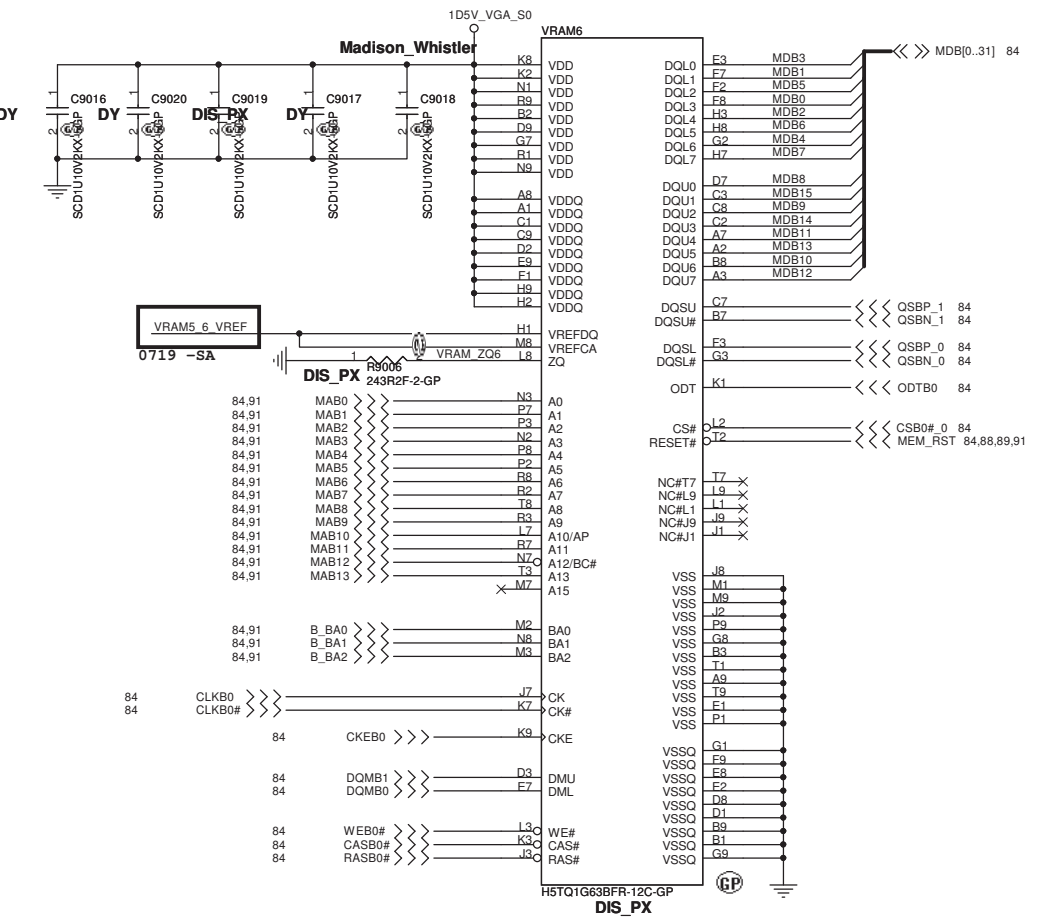
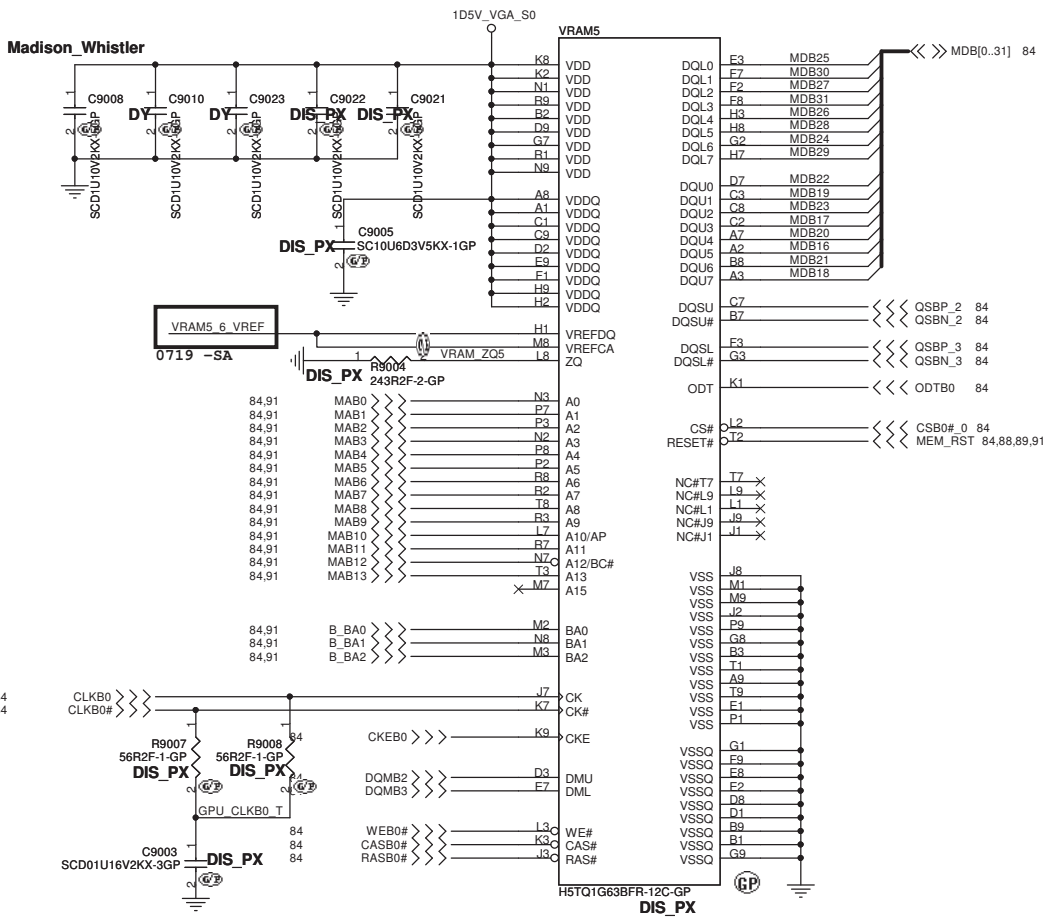


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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM3,4 (2/4)**

Size A3	Document Number	Rev
	JE50 SB	SB
Date: Friday, April 01, 2011	Sheet 89 of 102	

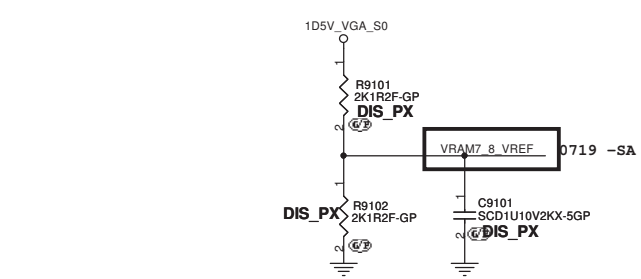
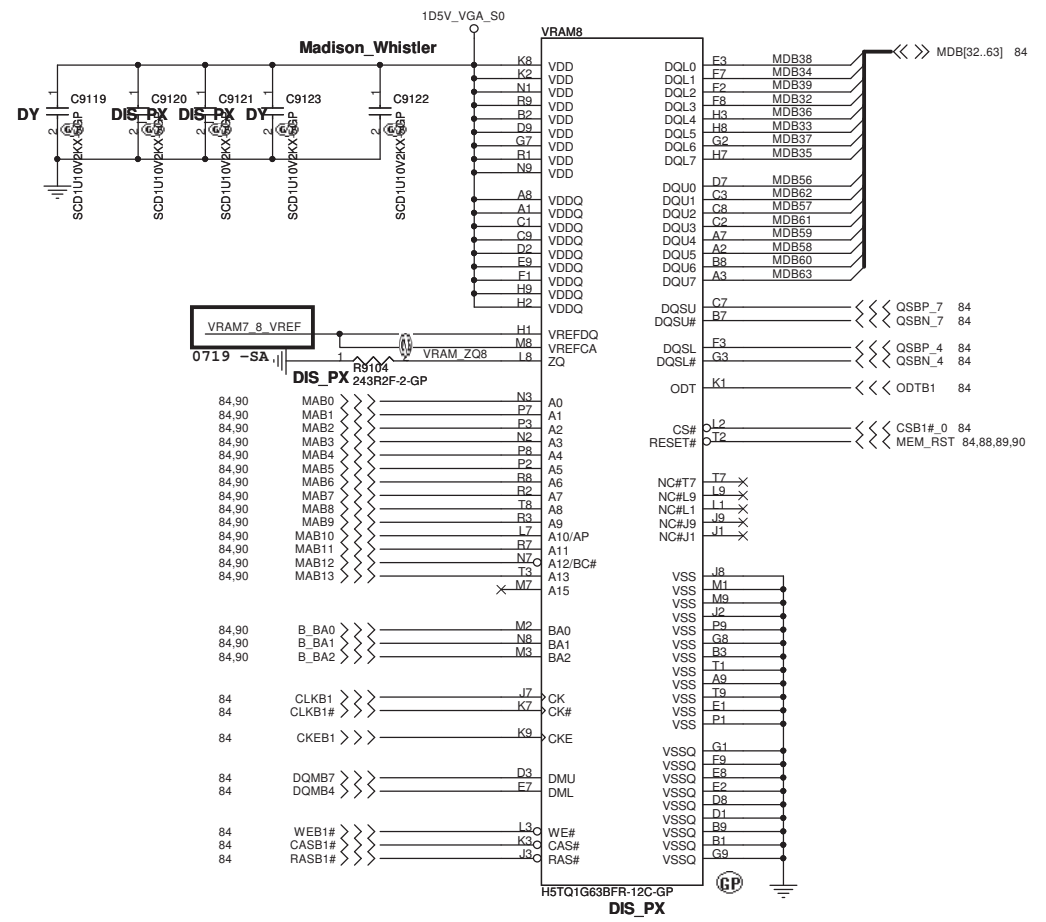
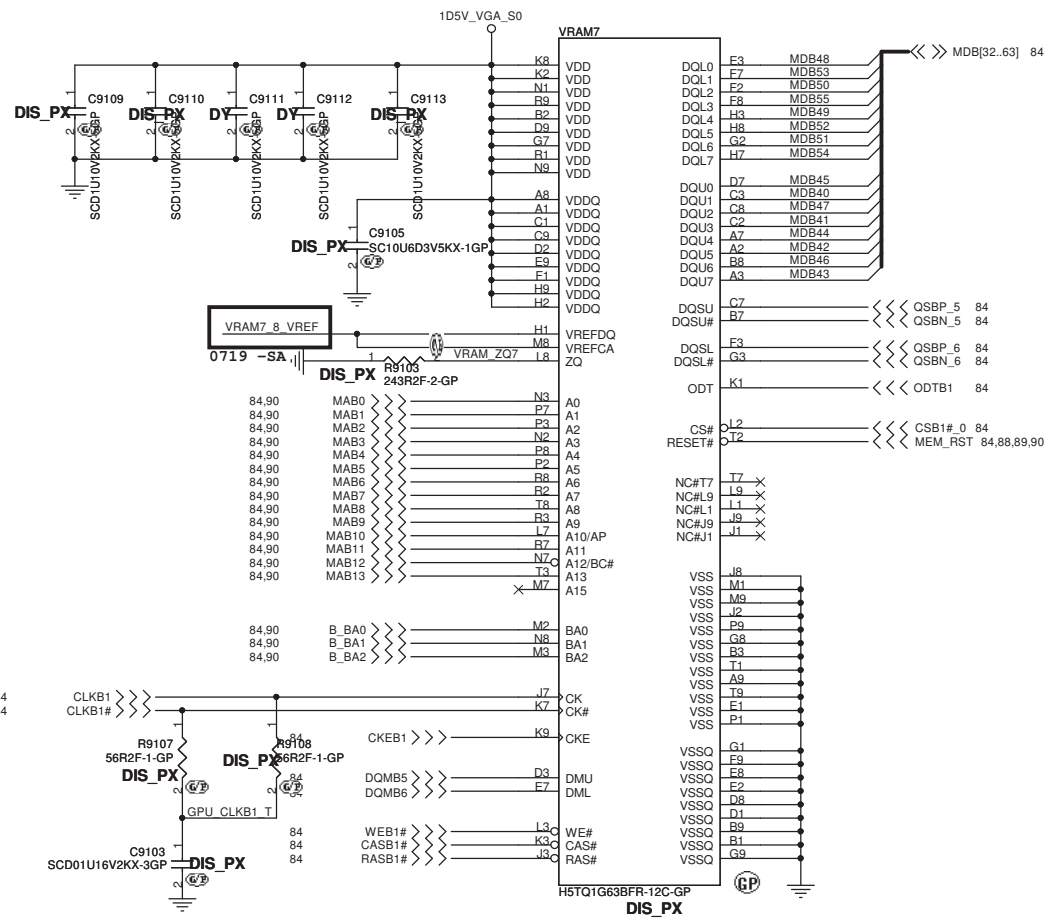


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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM5,6 (3/4)**

Size A3	Document Number	Rev
	JE50 SB	SB
Date: Friday, April 01, 2011	Sheet 90 of 102	



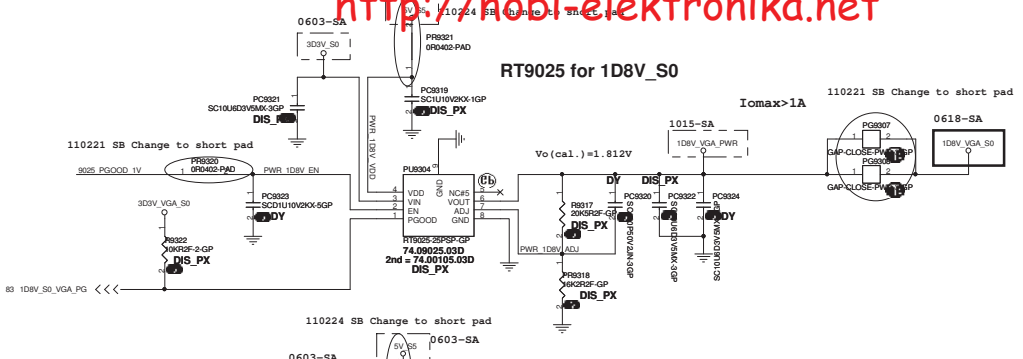
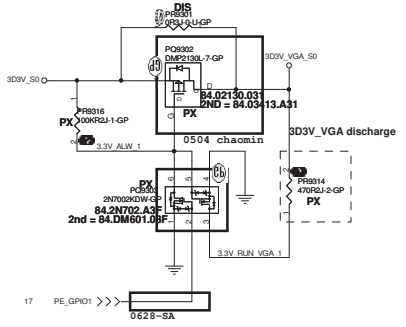
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

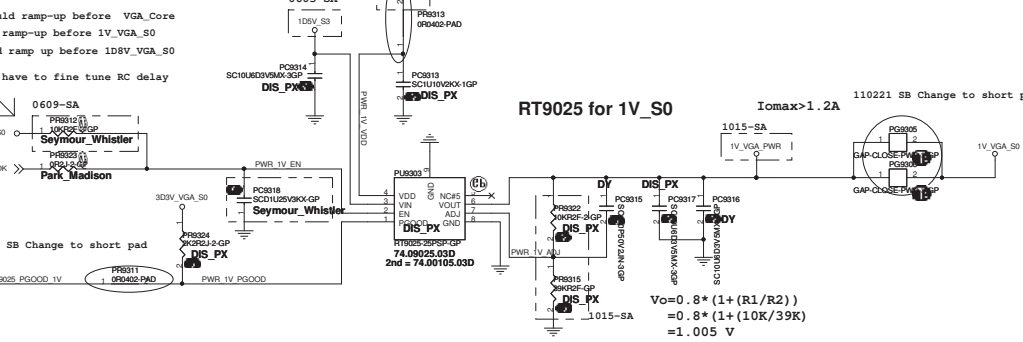
Size A3	Document Number	Rev
	JE50 SB	SB
Date: Friday, April 01, 2011	Sheet 91 of 102	

+3VS to 3.3V_DELAY Transfer

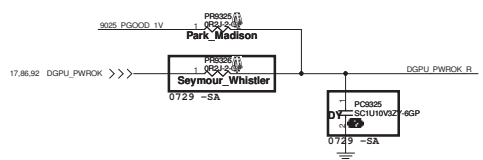
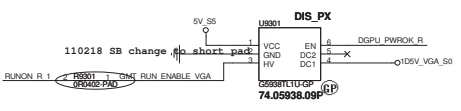
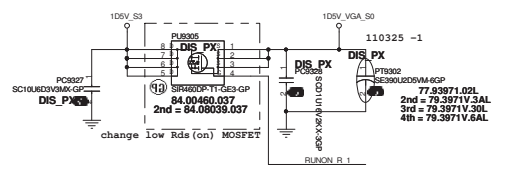


3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
So 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

	PE_GPI00	PE_GPI01
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H



A04468, SO-8
Id=11.6A, Qg=9-12nC
Rds(on)=17.4-22m ohm

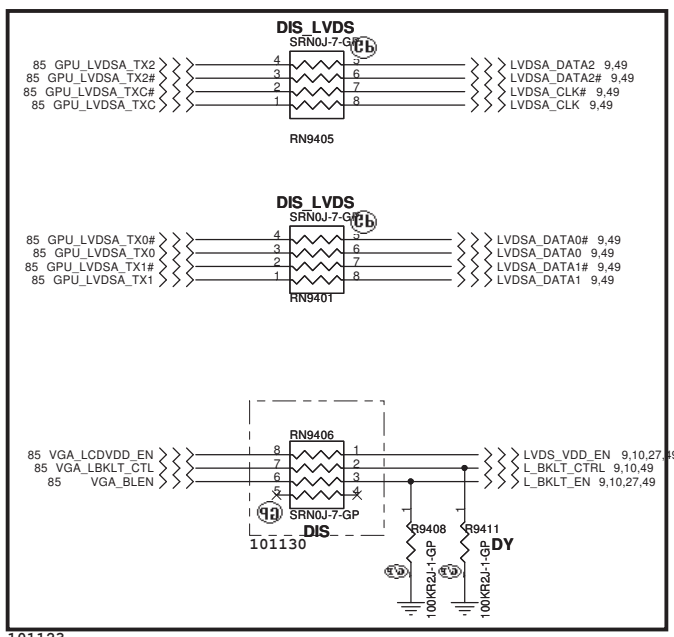


3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
1D5V_VGA_S0 sequence no define specially
So 1D5V_VGA_S0 EN have to fine tune RC delay after 1V_VGA_S0

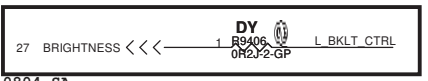
Wistron Corporation
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsinshih,
Taipai Hsien 221, Taiwan, R.O.C.

DISCRETE VGA POWER

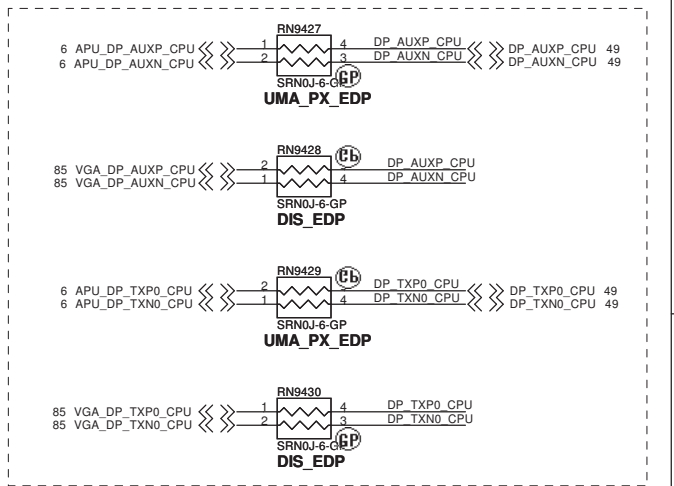
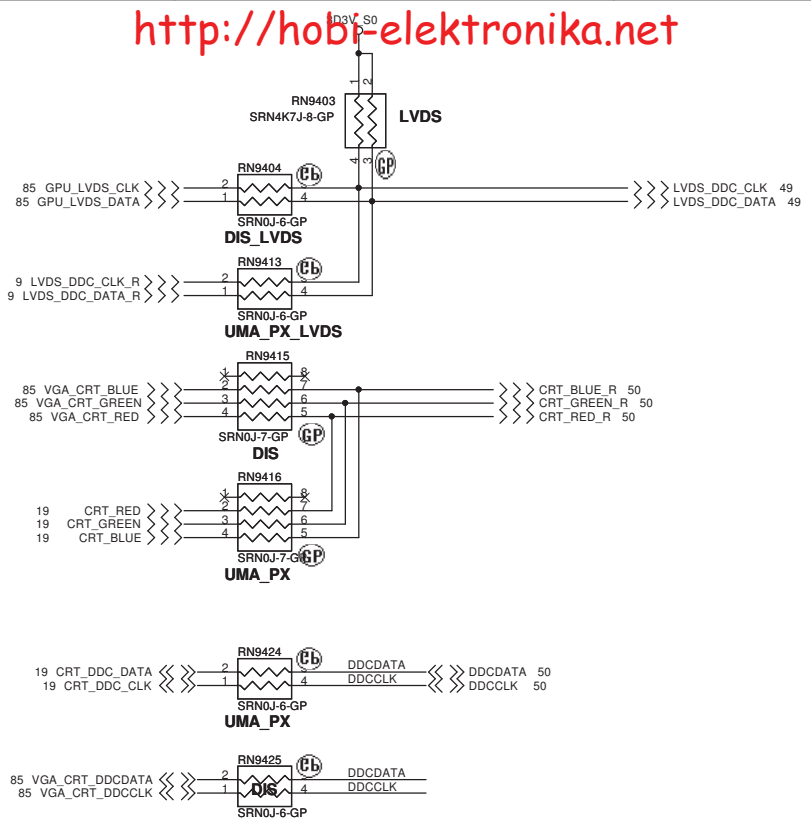
JE50_SB



101123

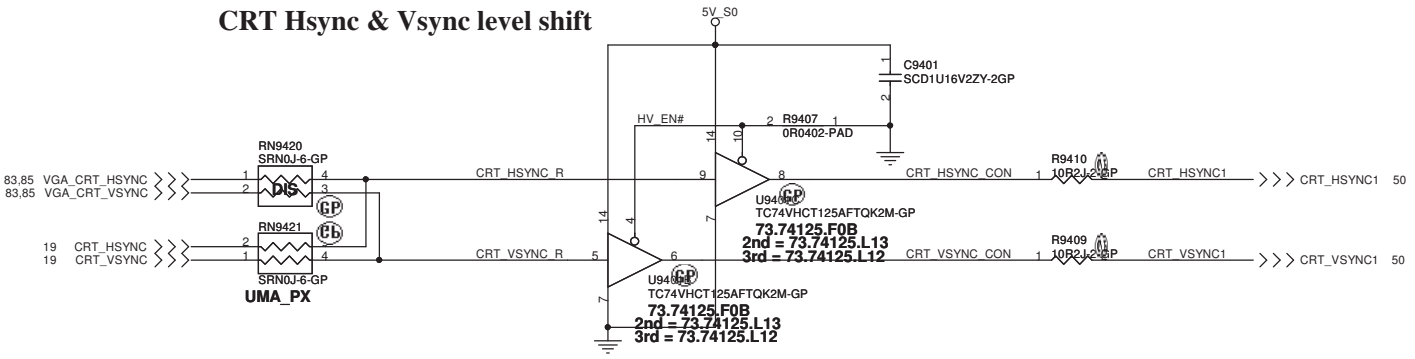


0804-SA



if Co-layout LVDS and EDP panel, have to place Res near LVDS Cap for Reflection Prevent

CRT Hsync & Vsync level shift



<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LVDS Switch			
Size A3	Document Number	JE50 SB	
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<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A	JE50 SB		SB
Date:	Friday, April 01, 2011	Sheet 95 of	102

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

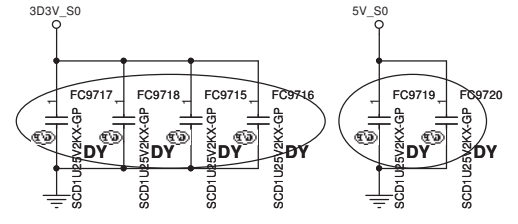
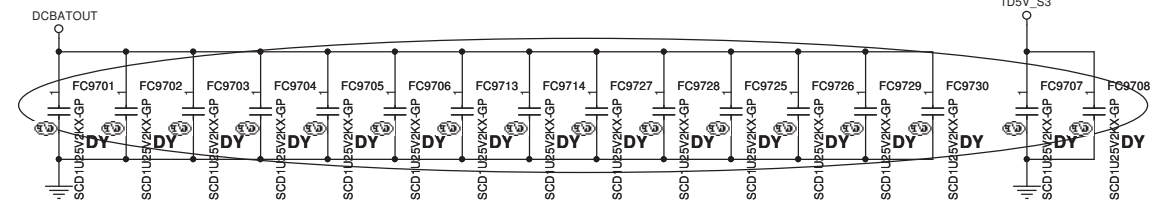
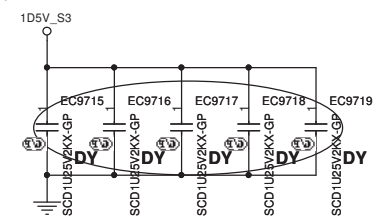
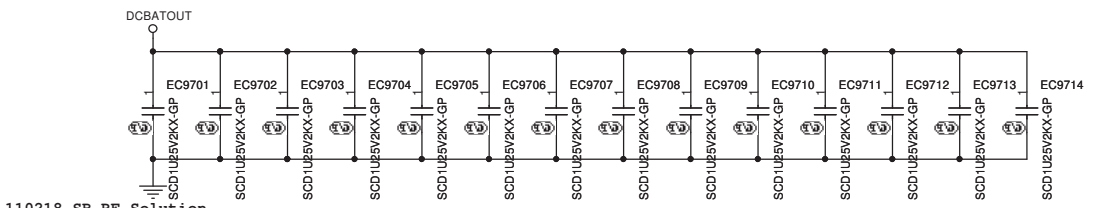
Rev

SB

Date: Friday, April 01, 2011

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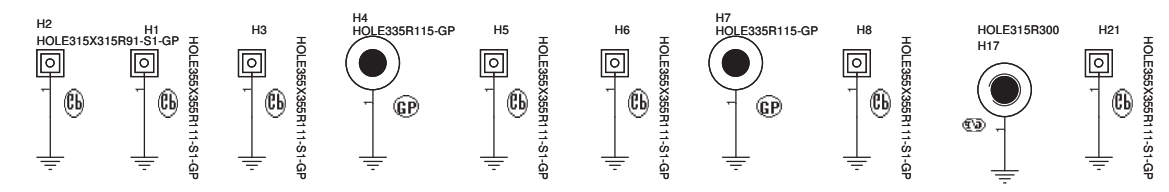
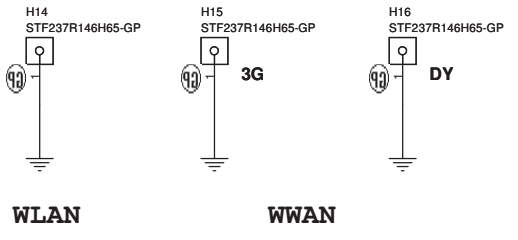
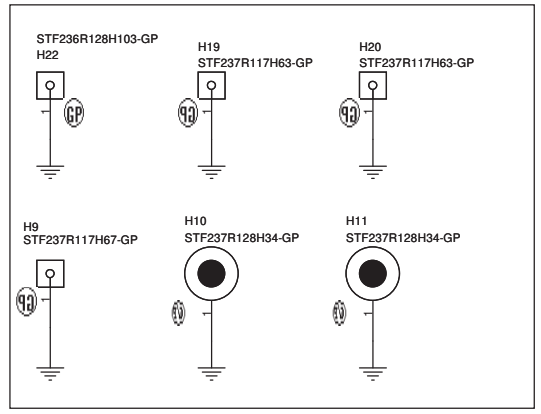
110223 SB RF Solution



Check test point

3D3V_S0C	1	TP9701
3D3V_AUX_S5C	1	TP9702
3D3V_S5C	1	TP9703
5V_S5C	1	TP9704
18,27_PM_PWRBTN#	<<<	TP9705
6,17,36,71_H_CUPUPWRGD_E	>>>	TP9706
27,36_S5_ENABLE	<<<	TP9707
10,17,27,36_A_RST#	>>>	TP9708

Test Point放在Dimm Door打開可量測處



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **UNUSED PARTS/CAP**

Size A3 Document Number: **JE50 SB** Rev: **SB**

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Modify list

65 W: PR4007 -> 187K(64.18735.6DL)
90 W: PR4007 -> 121K (64.12135.6DL)

UMA and PX R5114 ~ R5121 -> 604-ohm (64.60405.6DL)
Diserete -> R5114 ~ R5121-> 499-ohm(64.49905.6DL)

R8332 stuff 1K for Mannhatton VGA
stuff 5.1K(64.51015.6DL) for Vancouver VGA

if use LVDS L8711,L8709 stuff 0-ohm 0603
if use LVDS L8701,L8708 stuff bead 0603
if use EDP L8711,L8709 stuff bead 0603 ohm
if use EDP L8701,L8708 stuff 0-ohm 0603

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