Compal Confidential

NEW71/91 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
NV N11P-GV2H

2009-12-23

REV:0.1

Security Classification	Compal Secret Data		
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Title: Cover Page		
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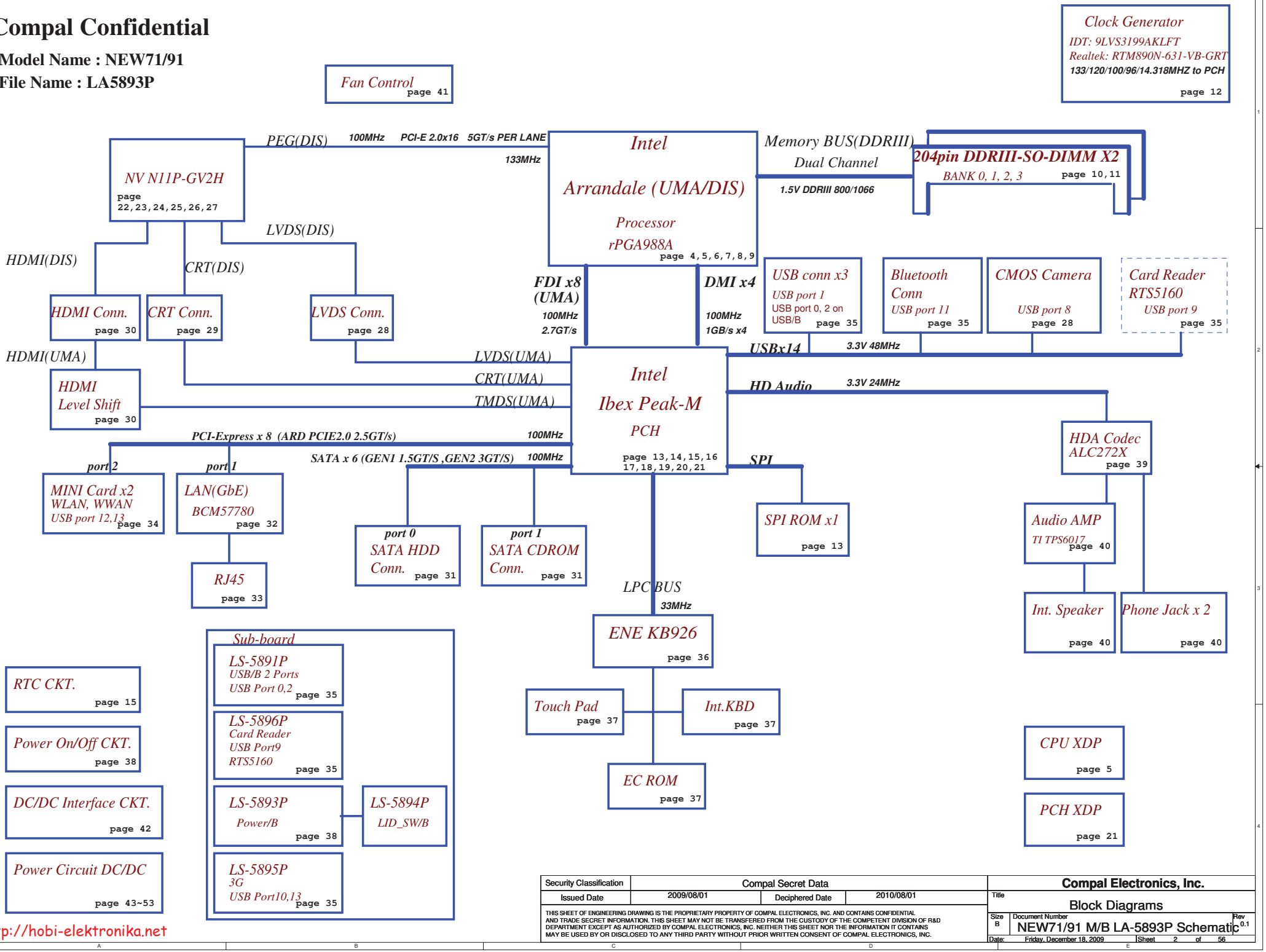
Model Name : NEW71/91
File Name : LA5893P



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Title	Block Diagrams	
Size B	Document Number NEW71/91 M/B LA-5893P Schematic	Rev 0.1
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
NEW71 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,XDP@
NEW91 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,91@,X7621@,XDP@

VRAM BOM Config

X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM

X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
XDP	XDP@
NonSG	NonSG@
NEW71	71@
NEW91	91@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

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Title: Notes List

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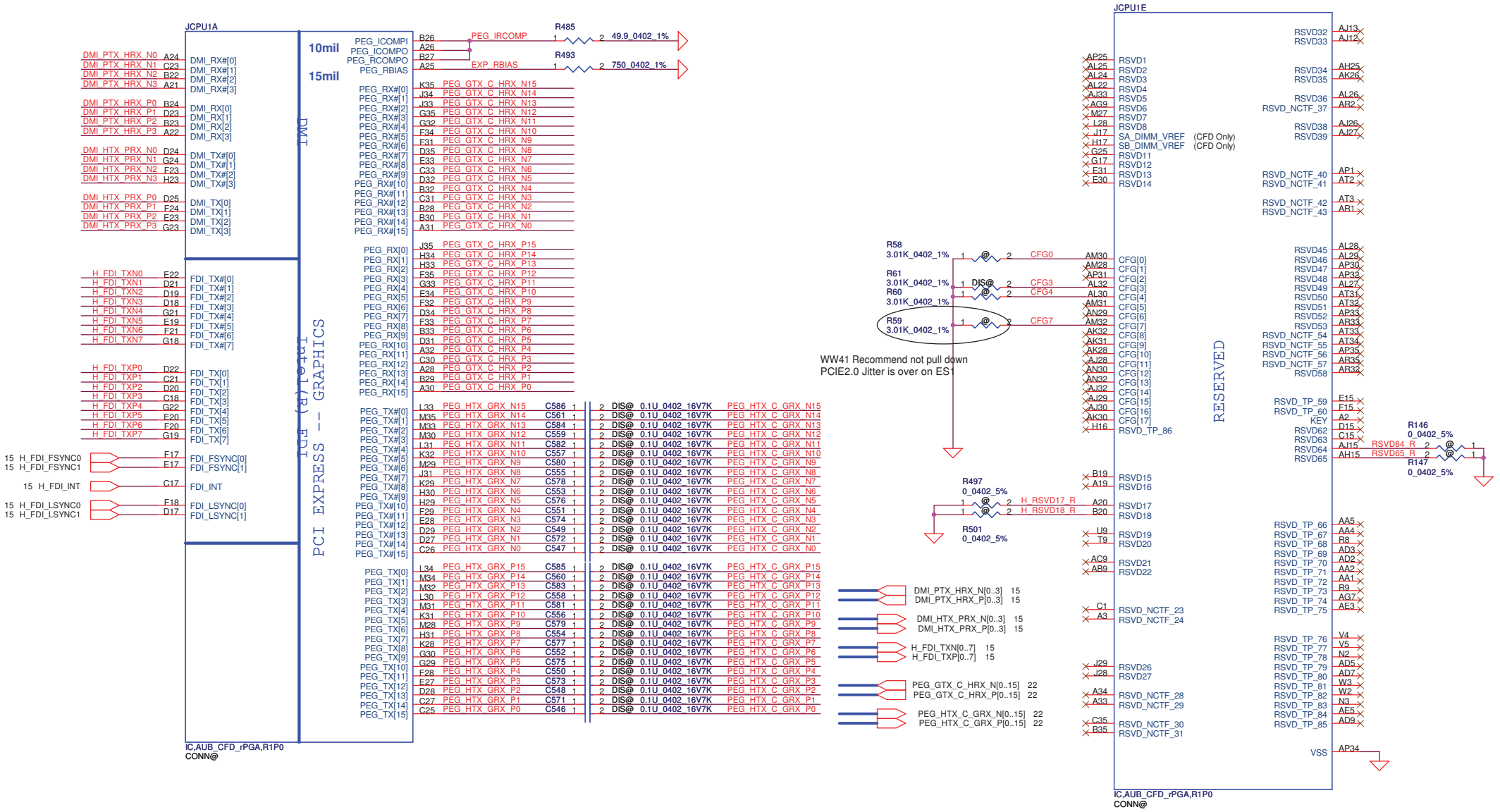

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

H_FDI_FSYNC0 R519 1 DIS ONLY@ 1K_0402_5%
H_FDI_FSYNC1 R517 1 DIS ONLY@ 1K_0402_5%
H_FDI_INT R513 1 DIS ONLY@ 1K_0402_5%
H_FDI_LSYNC0 R520 1 DIS ONLY@ 1K_0402_5%
H_FDI_LSYNC1 R515 1 DIS ONLY@ 1K_0402_5%

CheckList0.8 1.22
Auburndale Graphics Disable

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title: PROCESSOR (1/6) DMI,FDI,PEG

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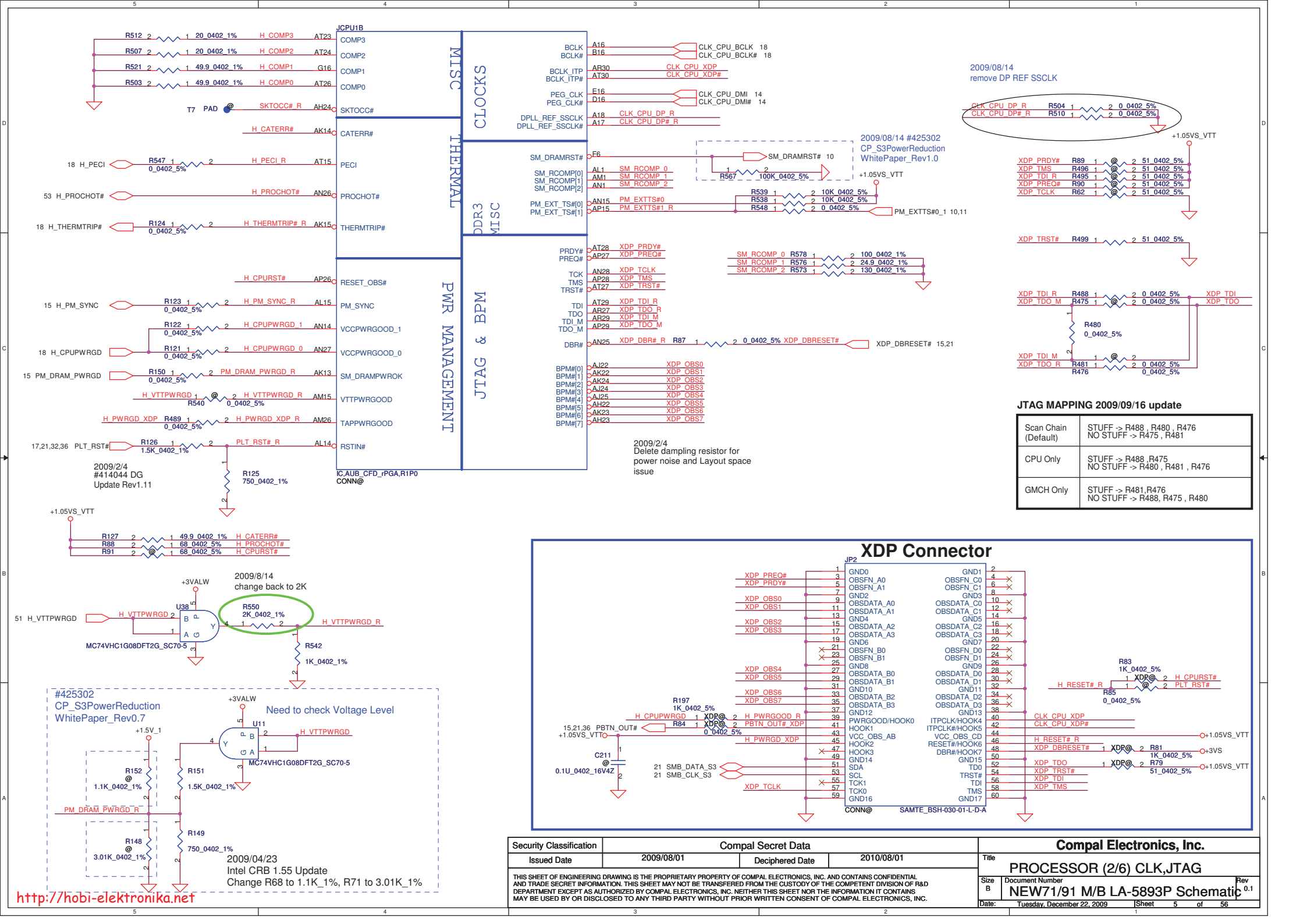

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

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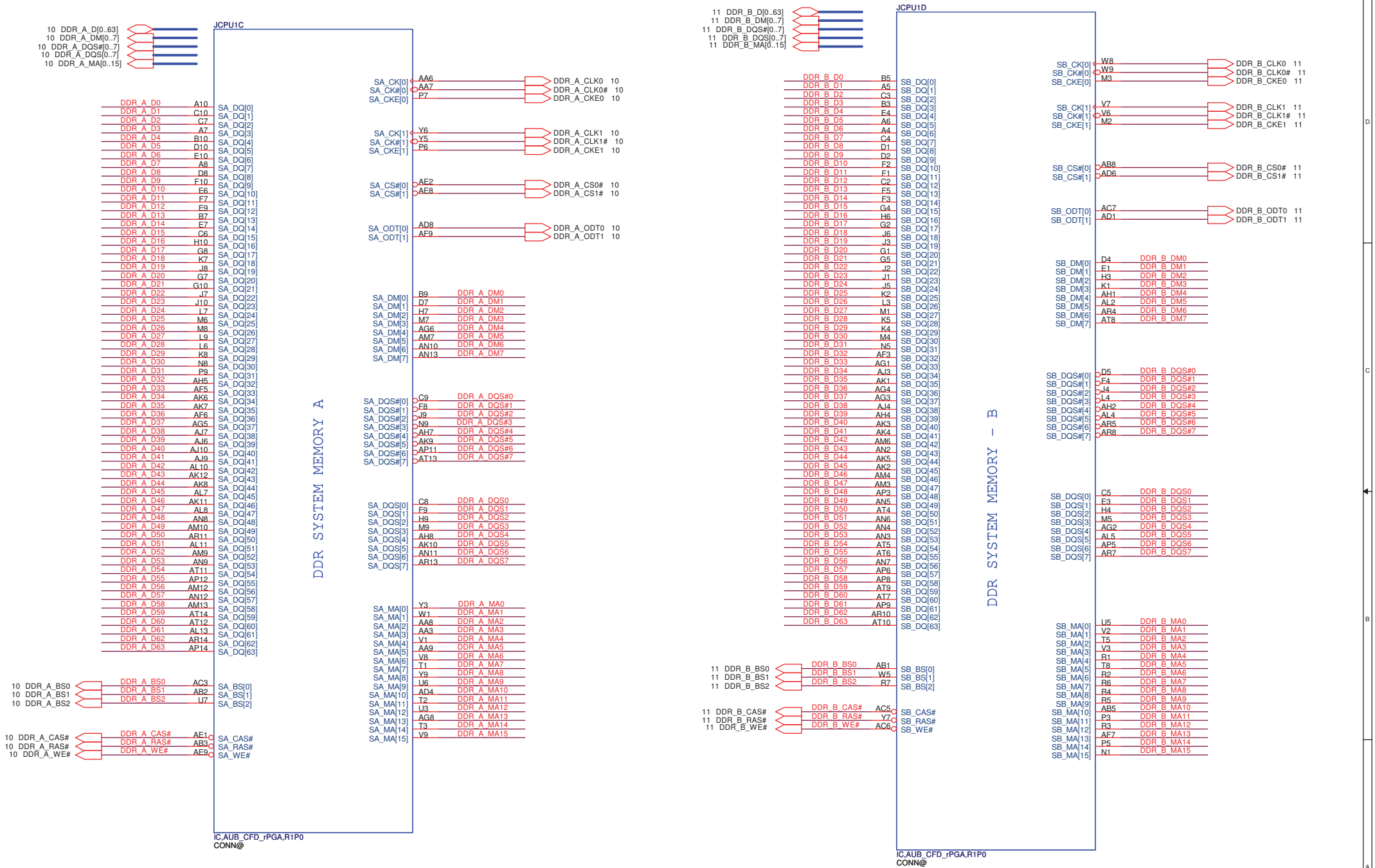

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Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

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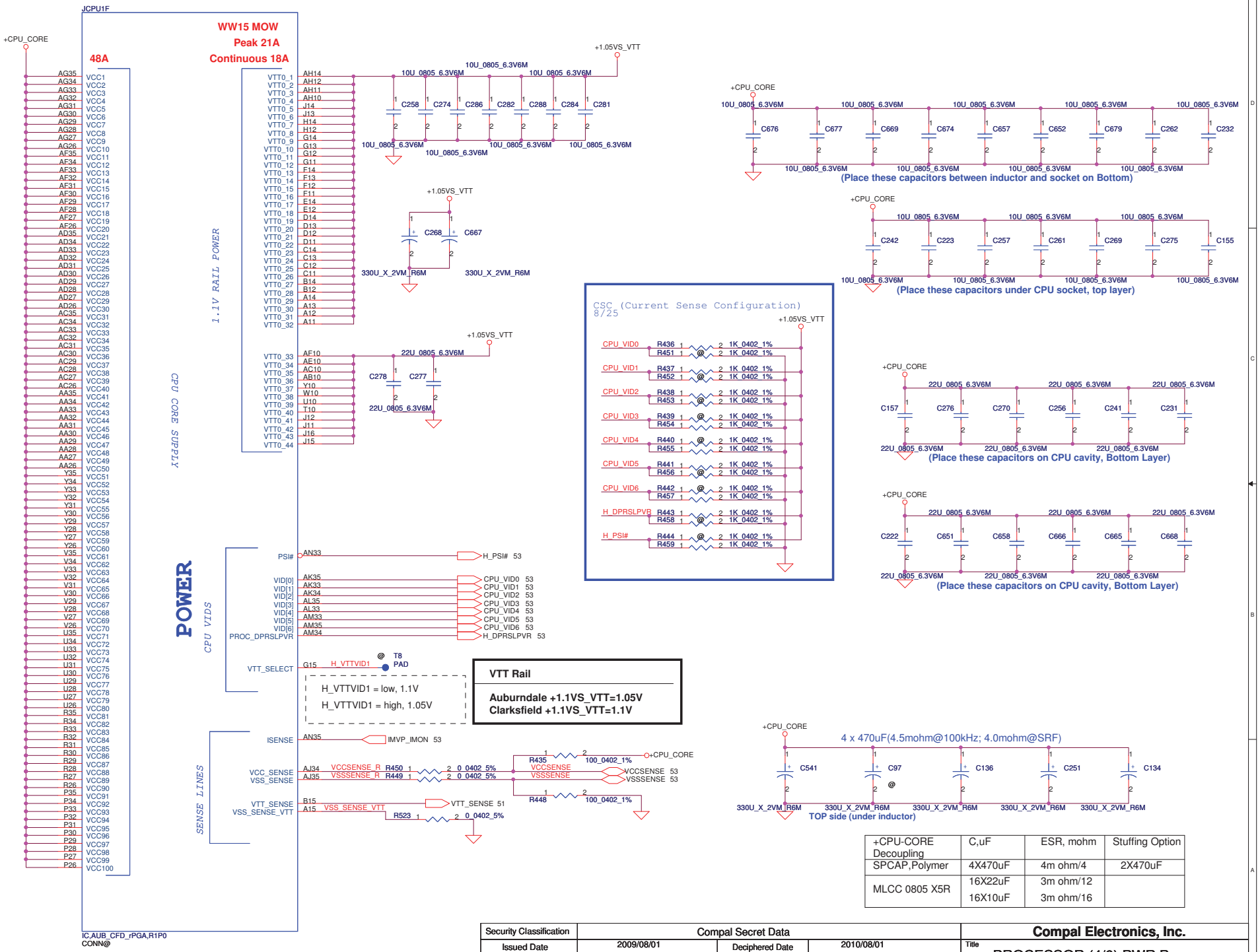

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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Title: PROCESSOR (4/6) PWR,Bypass

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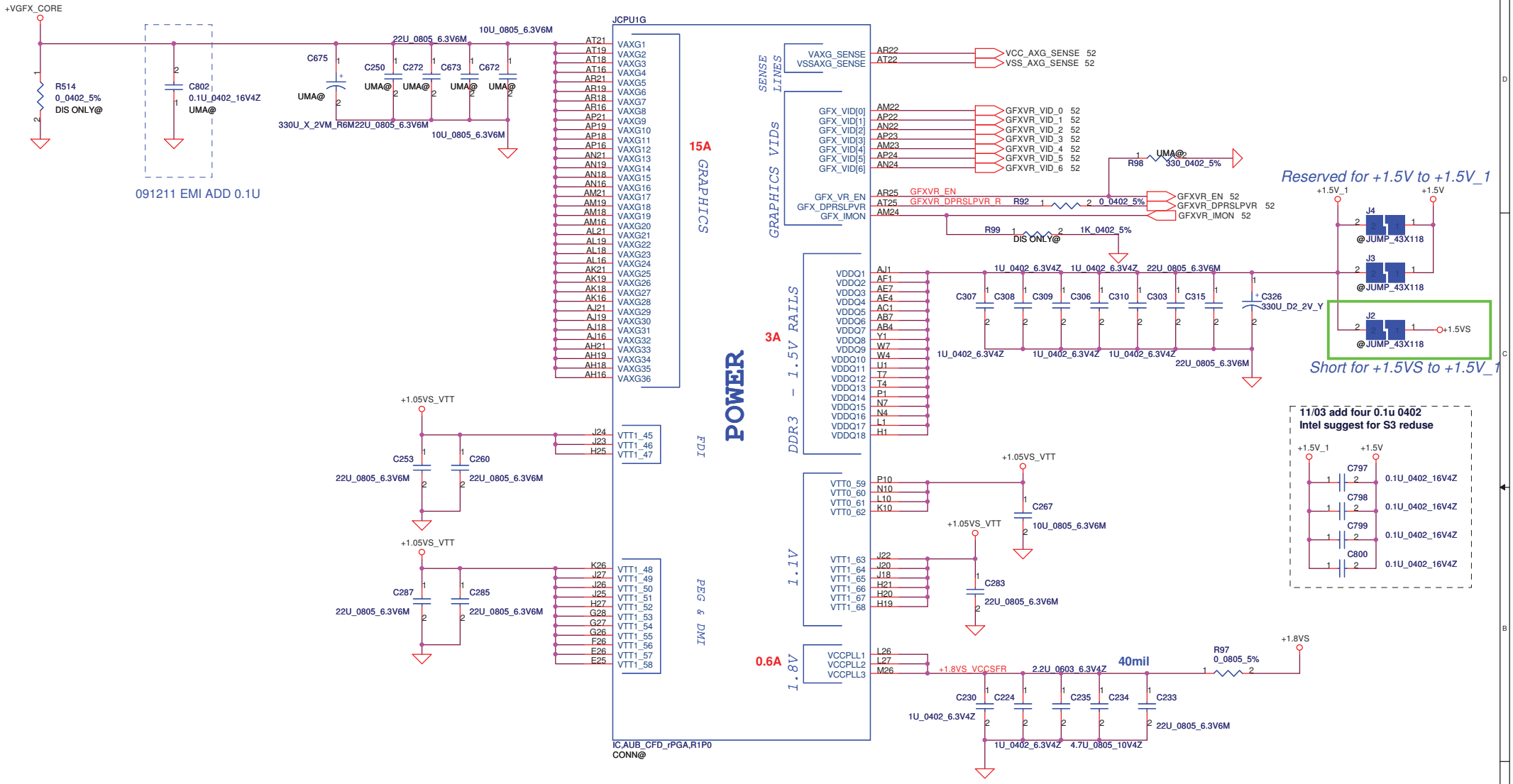

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Title	PROCESSOR (5/6) PWR		
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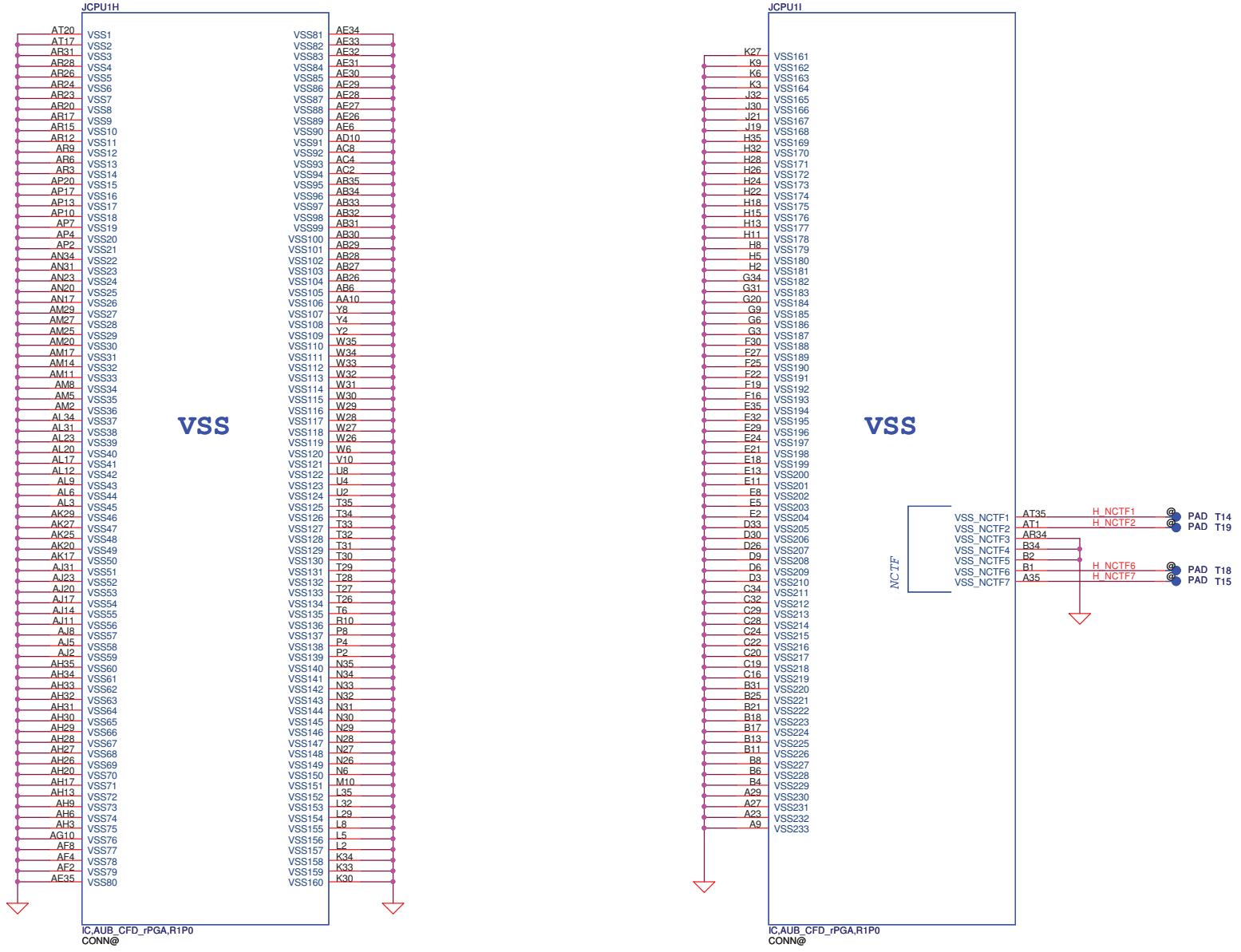

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Title: PROCESSOR (6/6) VSS

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DIMMA VREFDQ M1 Circuit

+1.5V

R222 1K_0402_1%

+DIMM_VREFDQA

20mil

R227 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V

R203 1K_0402_1%

+DIMM_VREFCA

20mil

R201 1K_0402_1%

6 DDR_A_DQS#[0..7]
6 DDR_A_D[0..63]
6 DDR_A_DM[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_MA[0..15]

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

+1.5V

R254 0_0402_5%

R274 1K_0402_1%

5 SM_DRAMRST#

Q17 BSS138LT1G_SOT23-3

DIMM_DRAMRST#

DIMM_DRAMRST# 11

C422 0.047U_0402_16V7K

18 RST_GATE

RST_GATE

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

10U_0805_6.3V6M: C354, C355, C356, C405, C404, C406, C400

0.1U_0402_16V4Z: C362, C363, C399

C425 330U_2.5V_M_R15 @

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

1U_0402_6.3V4Z: C391, C388, C397, C396

C394 10U_0805_6.3V6M

1U_0402_6.3V4Z

+DIMM_VREFDQA

C401 0.1U_0402_16V4Z

C402 2.2U_0603_6.3V4Z

+1.5V

JDIMM1

	VREF_DQ	VSS1	
	VSS2	DQ4	DDR_A_D4
DDR_A_D0	DQ0	DQ5	DDR_A_D5
DDR_A_D1	DQ1	VSS3	
	VSS4	DQS#0	DDR_A_DQS#0
DDR_A_DM0	DM0	DQS0	DDR_A_DQS0
	VSS5	DQ6	DDR_A_D6
DDR_A_D2	DQ2	DQ7	DDR_A_D7
DDR_A_D3	DQ3	VSS8	
	VSS7	DQ12	DDR_A_D12
DDR_A_D8	DQ8	DQ13	DDR_A_D13
DDR_A_D9	DQ9	VSS10	
	VSS9	DM1	DDR_A_DM1
DDR_A_DQS#1	DQS#1	RESET#	DIMM_DRAMRST#
DDR_A_DQS1	DQS1	VSS12	
	VSS11	DQ14	DDR_A_D14
DDR_A_D10	DQ10	DQ15	DDR_A_D15
DDR_A_D11	DQ11	VSS14	
	VSS13	DQ20	DDR_A_D20
DDR_A_D16	DQ16	DQ21	DDR_A_D21
DDR_A_D17	DQ17	VSS16	
	VSS15	DM2	DDR_A_DM2
DDR_A_DQS#2	DQS#2	VSS17	
DDR_A_DQS2	DQS2	DQ22	DDR_A_D22
	VSS18	DQ23	DDR_A_D23
DDR_A_D18	DQ18	VSS19	
DDR_A_D19	DQ19	DQ28	DDR_A_D28
	VSS20	DQ29	DDR_A_D29
DDR_A_D24	DQ24	VSS21	
DDR_A_D25	DQ25	DQS#3	DDR_A_DQS#3
	VSS22	DQS3	DDR_A_DQS3
DDR_A_DM3	DM3	VSS24	
	VSS23	DQ30	DDR_A_D30
DDR_A_D26	DQ26	DQ31	DDR_A_D31
DDR_A_D27	DQ27	VSS26	
	VSS25		
6 DDR_A_CKE0 DDR_A_CKE0	CKE0	CKE1	DDR_A_CKE1 DDR_A_CKE1 6
	VDD1	VDD2	DDR_A_MA15
	NC1	A15	DDR_A_MA14
6 DDR_A_BS2 DDR_A_BS2	BA2	A14	
	VDD3	VDD4	DDR_A_MA11
DDR_A_MA12	A12/BC#	A11	DDR_A_MA7
DDR_A_MA9	A9	A7	
	VDD5	VDD6	DDR_A_MA6
DDR_A_MA8	A8	A6	DDR_A_MA4
DDR_A_MA5	A5	A4	
	VDD7	VDD8	DDR_A_MA2
DDR_A_MA3	A3	A2	DDR_A_MA0
DDR_A_MA1	A1	A0	
	VDD9	VDD10	DDR_A_CLK1
6 DDR_A_CLK0 DDR_A_CLK0	CK0	CK1	DDR_A_CLK1# DDR_A_CLK1 6 DDR_A_CLK1# 6
6 DDR_A_CLK0# DDR_A_CLK0#	CK0#	CK1#	
	VDD11	VDD12	DDR_A_BS1
DDR_A_MA10	A10/AP	BA1	DDR_A_BS1 6 DDR_A_RAS#
DDR_A_BS0 6 DDR_A_BS0	BA0	RAS#	DDR_A_RAS# 6
	VDD13	VDD14	DDR_A_CS0#
6 DDR_A_WE# DDR_A_WE#	WE#	S0#	DDR_A_CS0# 6 DDR_A_ODT0
6 DDR_A_CAS# DDR_A_CAS#	CAS#	ODT0	DDR_A_ODT0 6
	VDD15	VDD16	DDR_A_ODT1
DDR_A_MA13	A13	ODT1	DDR_A_ODT1 6
6 DDR_A_CS1# DDR_A_CS1#	S1#	NC2	
	VDD17	VDD18	20mil
	NCTEST	VREF_CA	DDR_VREF_CA_DIMMA R202 1 2 0_0402_5%
	VSS27	VSS28	
DDR_A_D32	DQ32	DQ36	DDR_A_D36
DDR_A_D33	DQ33	DQ37	DDR_A_D37
	VSS29	VSS30	
DDR_A_DQS#4	DQS#4	DM4	DDR_A_DM4
DDR_A_DQS4	DQS4	VSS31	
	VSS32	DQ38	DDR_A_D38
DDR_A_D34	DQ34	DQ39	DDR_A_D39
DDR_A_D35	DQ35	VSS33	
	VSS34	DQ44	DDR_A_D44
DDR_A_D40	DQ40	DQ45	DDR_A_D45
DDR_A_D41	DQ41	VSS35	
	VSS36	DQS#5	DDR_A_DQS#5
DDR_A_DM5	DM5	DQS5	DDR_A_DQS5
	VSS37	VSS38	
DDR_A_D42	DQ42	DQ46	DDR_A_D46
DDR_A_D43	DQ43	DQ47	DDR_A_D47
	VSS39	VSS40	
DDR_A_D48	DQ48	DQ52	DDR_A_D52
DDR_A_D49	DQ49	DQ53	DDR_A_D53
	VSS41	VSS42	
DDR_A_DQS#6	DQS#6	DM6	DDR_A_DM6
DDR_A_DQS6	DQS6	VSS43	
	VSS44	DQ54	DDR_A_D54
DDR_A_D50	DQ50	DQ55	DDR_A_D55
DDR_A_D51	DQ51	VSS45	
	VSS46	DQ60	DDR_A_D60
DDR_A_D56	DQ56	DQ61	DDR_A_D61
DDR_A_D57	DQ57	VSS47	
	VSS48	DQS#7	DDR_A_DQS#7
DDR_A_DM7	DM7	DQS7	DDR_A_DQS7
	VSS49	VSS50	
DDR_A_D58	DQ58	DQ62	DDR_A_D62
DDR_A_D59	DQ59	DQ63	DDR_A_D63
	VSS51	VSS52	
R218 1 2 10K_0402_5%	SA0	EVENT#	PM_EXTTS#0_1 PM_EXTTS#0_1 5,11
	VDDSPD	SDA	D_CK_SDATA D_CK_SDATA 11,12
	SA1	SCL	D_CK_SCLK D_CK_SCLK 11,12
	VTT1	VTT2	+0.75VS
	G1	G2	

FOX_AS0A626-U8RN-7F

+3VS

C403 2.2U_0603_6.3V4Z

C398 0.1U_0402_16V4Z

R217 10K_0402_5%

+DIMM_VREFCA

C358 2.2U_0603_6.3V4Z

C361 0.1U_0402_16V4Z

DDR3 SO-DIMM A
H=8mm

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Title: DDRIII-SODIMM SLOT1

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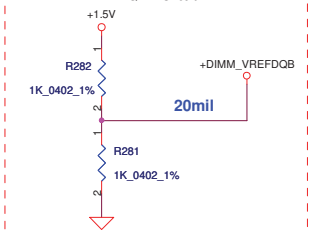
6 DDR_B_DQS#[0..7]
6 DDR_B_D[0..63]
6 DDR_B_DM[0..7]
6 DDR_B_DQS[0..7]
6 DDR_B_MA[0..15]

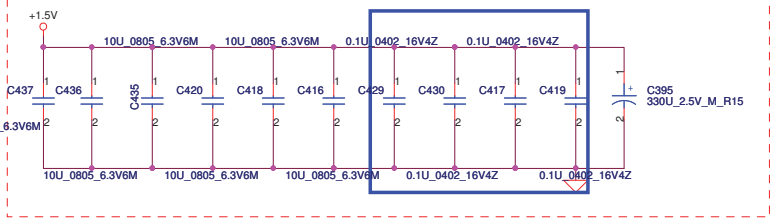
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

DIMMB VREFDQ M1 Circuit

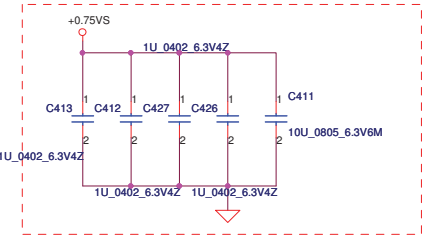


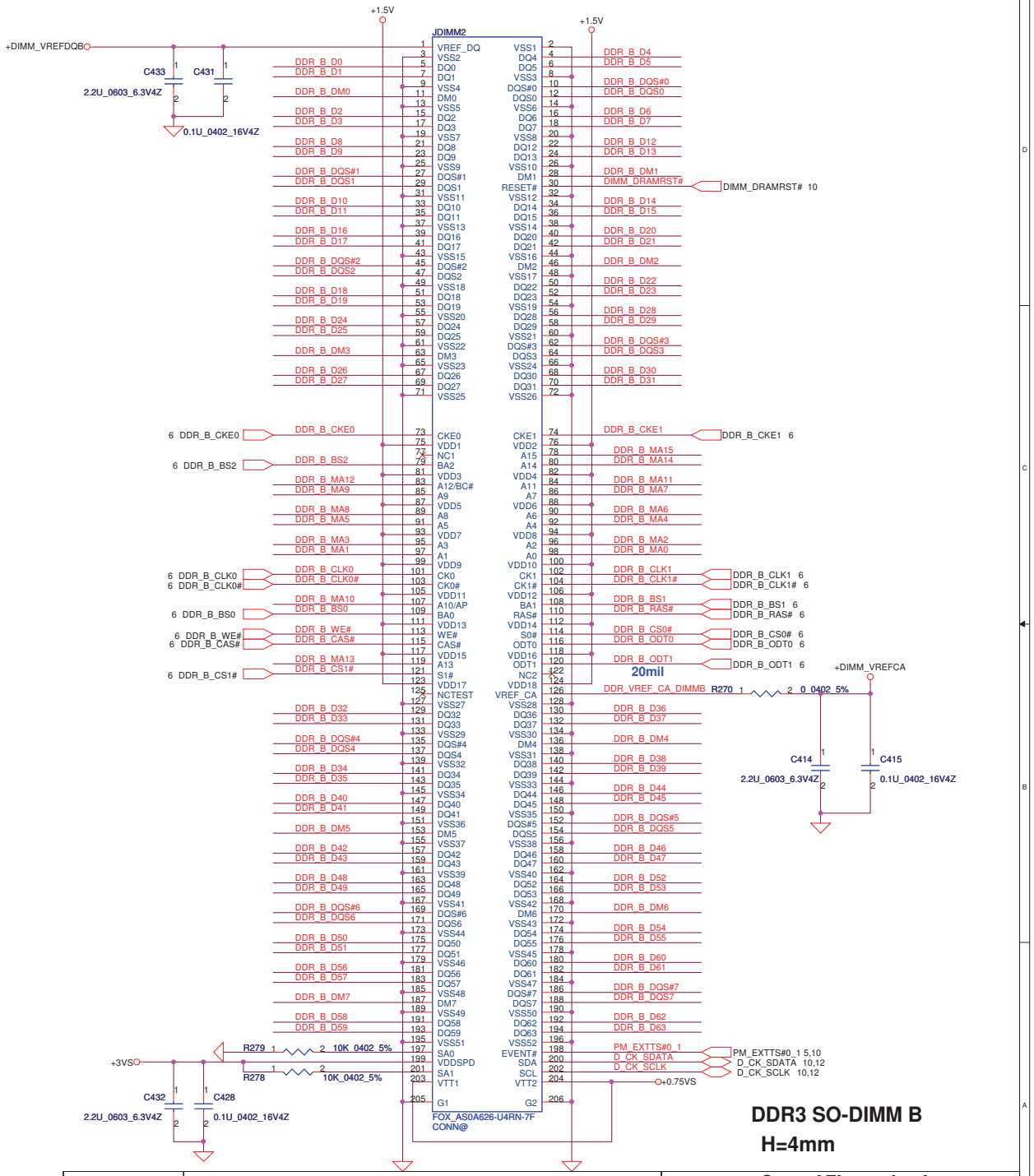
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDIMM2.203 & JDIMM2.204





DDR3 SO-DIMM B
H=4mm

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 11 of 56

SM010014520 3000ma 220ohm@100mhz DCR 0.04

+1.05VS_VTT — L76 FBMA-L11-201209-221LMA30T_0805 — +CLK_1.05VS 40mil

C782 10U_0805_10V4Z

C774 10U_0805_10V4Z

C757 0.1U_0402_16V4Z

C770 0.1U_0402_16V4Z

SM010014520 3000ma 220ohm@100mhz DCR 0.04

+3VS — L69 FBMA-L11-201209-221LMA30T_0805 — +CLK_3VS 40mil

C737 10U_0805_10V4Z

C740 10U_0805_10V4Z

C750 0.1U_0402_16V4Z

C741 0.1U_0402_16V4Z

SM010014520 3000ma 220ohm@100mhz DCR 0.04

+1.5VS — L74 FBMA-L11-201209-221LMA30T_0805 @ — L75 FBMA-L11-201209-221LMA30T_0805 — +CLK_1.5VS 40mil

C781 10U_0805_10V4Z

C768 10U_0805_10V4Z

C742 0.1U_0402_16V4Z

C771 0.1U_0402_16V4Z

C769 0.1U_0402_16V4Z

Clock Generator

U47 IDT SA00003HR00 SLG8SP587VTR_QFN32_5X5

+CLK_3VS, +CLK_1.5VS

1	VDD_USB_48	SCL	32
2	VSS_48M	SDA	31
3	DOT_96	REF_0/CPU_SEL	30
4	DOT_96#	VDD_REF	29
5	VDD_27	XTAL_IN	28
6	27MHZ	XTAL_OUT	27
7	27MHZ_SS	VSS_REF	26
8	USB_48	CKPWRGD/PD#	25
9	VSS_27M	VDD_CPU	24
10	SATA	CPU_0	23
11	SATA#	CPU_0#	22
12	VSS_SRC	VSS_CPU	21
13	SRC_1	CPU_1	20
14	SRC_1#	CPU_1#	19
15	VDD_SRC_IO	VDD_CPU_IO	18
16	CPU_STOP#	VDD_SRC	17
33	TGND		

14 CLK_BUF_DREF_96M — CLK_BUF_DREF_96M — R717 0_0402_5% @

14 CLK_BUF_DREF_96M# — CLK_BUF_DREF_96M#

22 27M_CLK — 27M_CLK — R716 0_0402_5% @

22 27M_SSC — 27M_SSC

14 CLK_BUF_PCIE_SATA — CLK_BUF_PCIE_SATA

14 CLK_BUF_PCIE_SATA# — CLK_BUF_PCIE_SATA#

14 CLK_BUF_CPU_DMI — CLK_BUF_CPU_DMI

14 CLK_BUF_CPU_DMI# — CLK_BUF_CPU_DMI#

+CLK_1.05VS — H_STP_CPU#

D_CK_SCLK — D_CK_SCLK 10,11

D_CK_SDATA — D_CK_SDATA 10,11

REF_0/CPU_SEL — R682 33_0402_5% — CLK_BUF_ICH_14M 14

CLK_XTAL_IN

CLK_XTAL_OUT

CK505_PWRGD

CLK_BUF_CPU_BCLK — CLK_BUF_CPU_BCLK 14

CLK_BUF_CPU_BCLK# — CLK_BUF_CPU_BCLK# 14

+CLK_1.05VS

+CLK_1.5VS

IDT: 9LRS3199AKLFT, SA000030P00

SILEGO: SLG8SP587V(WF), SA00002XY10

Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00

Realtek: RTM890N-631-VB-GRT, SA00003HQ10

IDT 9LVS3199AKLFT NC

+3VS

Silego Have Internal Pull-Up

R690 10K_0402_5% H_STP_CPU#

IDT Have Internal Pull-Down

FOR Realtek

R683 10K_0402_5% REF_0/CPU_SEL

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

+3VS — R678 4.7K_0402_5% — +3VS

14,21,34 PCH_SMBDATA — D_CK_SDATA — Q46 2N7002E-T1-GE3_SOT23-3

+3VS — R677 4.7K_0402_5% — +3VS

14,21,34 PCH_SMBCLK — D_CK_SCLK — Q45 2N7002E-T1-GE3_SOT23-3

+3VS — R693 10K_0402_5%

CK505_PWRGD — R691 0_0402_5% @ — VGATE 15,53

CLK_ENABLE# 53 — Q48 2N7002E-T1-GE3_SOT23-3

CLK_XTAL_IN — C755 27P_0402_50V8J

Y4 14.31818MHZ 20PF 7A14300003

CLK_XTAL_OUT — C762 27P_0402_50V8J

Change to 5x3.2

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Clock Generator (CK505)

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RC Delay 18~25mS

close to RAM door

HDA for AUDIO

(HDA_SYNC Have internal Pull-Down)

HDA_SYNC
On Die PLL VR is supplied by
1.5V when sampled High,
1.8V when sampled Low.

Have internal PD

If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.

GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manfacturing/ debug.

2009/08/23
Debug Port DG1.7 P27.28
TDO,TDI,TMS
Pull Up for Production Units
unpop TDO,TDI,TMS resister

2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R724, R722 on ES2 Sample

MP mount R646, R644, R645, R643 and remove others

S3 CRB 1.1 Change to 4.7K

enable iTPM: SPI_MOSI High

MOSI This signal has a weak internal pull-down resistor. This signal must be sampled low.

modify to 330K

INTVRMEN - Integrated SUS 1.05V VRM Enable High - Enable Internal VRs

HDA_SDO ,This signal has a weak internal pull-down resistor. Should not be Pull High

GPIO33 can not pull down (manufacturing environments)

2/10 SATA2, SATA3 not support on HM55

SATA for HDD1

SATA for ODD

GPIO21 Project ID2

SPI ROM Footprint 200mil

	GPIO19 (PCH_GPIO19)	GPIO37 (VGA_PRSNT_L#)
dGPU	0	0
iGPU	0	1
* SG	1	X

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 13 of 56

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

U41B REV1.0

For PCIE LAN
For Wireless LAN
For Mini2
For PCIE LAN
For Wireless LAN

2009/08/25: remove PCIE5

2/10 PCIE7, PCIE8 not support on HM55

2009/08/25: Change back to +3V remove mini2

2009/08/25: remove mini2 clk

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

Change to 5x3.2

Project Structure ID

Pull high +3VS at KB926 side

9/1: Change to +3VS

2009/08/13: Change back to +3V

Schematic_Checklist_Rev1.6

GPIO18	Main (core) power well (+V3.3S)	Muxed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)
GPIO25	Resume (Sus) well (+V3.3A)	Muxed with PCIECLKRQ3# If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

Project Structure			
GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
* 1	0	0	NEW71/91

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 14 of 56

4 DMI_HTX_PRX_N[0..3] → DMI_HTX_PRX_N[0..3]
4 DMI_HTX_PRX_P[0..3] → DMI_HTX_PRX_P[0..3]
4 DMI_PTX_HRX_N[0..3] → DMI_PTX_HRX_N[0..3]
4 DMI_PTX_HRX_P[0..3] → DMI_PTX_HRX_P[0..3]

4 H_FDI_TXN[0..7] → H_FDI_TXN[0..7]
4 H_FDI_TXP[0..7] → H_FDI_TXP[0..7]

+3VS
R657 1 2 PM_CLKRUN# 8.2K_0402_5%

+3V
R648 1 2 SUS_PWR_DN_ACK 10K_0402_5%
R628 1 2 PCH_GPIO72 8.2K_0402_5%
R198 1 2 EC_SWI# 10K_0402_5%
R641 1 2 PCH_PCIE_WAKE# 10K_0402_5%
R248 1 @ 2 PM_SLP_LAN# 10K_0402_5%

09/09/14 WW37 PCH WAKE# PU 10K

+1.05VS_PCH
R600 49.9_0402_1% 1 2 DMI_COMP

U41C
REV1.0
IBEXPEAK-M_FCBGA107

DMI
DMI_HTX_PRX_N0 BC24 DMI0RXN
DMI_HTX_PRX_N1 BJ22 DMI1RXN
DMI_HTX_PRX_N2 AW20 DMI2RXN
DMI_HTX_PRX_N3 BJ20 DMI3RXN
DMI_HTX_PRX_P0 BD24 DMI0RXP
DMI_HTX_PRX_P1 BG22 DMI1RXP
DMI_HTX_PRX_P2 BA20 DMI2RXP
DMI_HTX_PRX_P3 BG20 DMI3RXP
DMI_PTX_HRX_N0 BE22 DMI0TXN
DMI_PTX_HRX_N1 BF21 DMI1TXN
DMI_PTX_HRX_N2 BD20 DMI2TXN
DMI_PTX_HRX_N3 BE18 DMI3TXN
DMI_PTX_HRX_P0 BD22 DMI0TXP
DMI_PTX_HRX_P1 BH21 DMI1TXP
DMI_PTX_HRX_P2 BC20 DMI2TXP
DMI_PTX_HRX_P3 BD18 DMI3TXP
BH25 DMI_ZCOMP
BF25 DMI_IRCOMP

FDI
FDI_RXN0 BA18 H_FDI_TXN0
FDI_RXN1 BH17 H_FDI_TXN1
FDI_RXN2 BD16 H_FDI_TXN2
FDI_RXN3 BJ16 H_FDI_TXN3
FDI_RXN4 BA16 H_FDI_TXN4
FDI_RXN5 BE14 H_FDI_TXN5
FDI_RXN6 BA14 H_FDI_TXN6
FDI_RXN7 BC12 H_FDI_TXN7
FDI_RXP0 BB18 H_FDI_TXP0
FDI_RXP1 BF17 H_FDI_TXP1
FDI_RXP2 BC16 H_FDI_TXP2
FDI_RXP3 BG16 H_FDI_TXP3
FDI_RXP4 AW16 H_FDI_TXP4
FDI_RXP5 BD14 H_FDI_TXP5
FDI_RXP6 BB14 H_FDI_TXP6
FDI_RXP7 BD12 H_FDI_TXP7
FDI_INT BJ14 H_FDI_INT 4
FDI_FSYNC0 BF13 H_FDI_FSYNC0 4
FDI_FSYNC1 BH13 H_FDI_FSYNC1 4
FDI_LSYNC0 BJ12 H_FDI_LSYNC0 4
FDI_LSYNC1 BG14 H_FDI_LSYNC1 4

System Power Management
5,21 XDP_DBRESET# → XDP_DBRESET# T6 SYS_RESET#
SYS_PWROK R620 0_0402_5% SYS_PWROK_R M6 SYS_PWROK
VGATE R631 @ 0_0402_5%
SYS_PWROK B17 PWROK
K5 MEPWROK
LAN_RST# A10 LAN_RST#
5 PM_DRAM_PWRGD D9 DRAMPWROK
PCH_RSMRST# C16 RSMRST#
36 SUS_PWR_DN_ACK SUS_PWR_DN_ACK M1 SUS_PWR_DN_ACK / GPIO30
5,21,36 PBTN_OUT# PBTN_OUT# P5 PWRBTN#
+3V R240 10K_0402_5%
36 EC_ACIN D6 CH751H-40PT_SOD323-2 PCH_ACIN P7 ACPRESENT / GPIO31
PCH_GPIO72 A6 BATLOW# / GPIO72
36 EC_SWI# EC_SWI# F14 RI#

WAKE# J12 PCH_PCIE_WAKE# → PCH_PCIE_WAKE# 32,34
CLKRUN# / GPIO32 Y1 PM_CLKRUN# → PM_CLKRUN# 36
SUS_STAT# / GPIO61 P8 PCH_GPIO61 @ PAD T10
SUSCLK / GPIO62 F3 SUSCLK → SUSCLK 36
SLP_S5# / GPIO63 F4 → PM_SLP_S5# 36
SLP_S4# H7 → PM_SLP_S4# 36
SLP_S3# P12 → PM_SLP_S3# 36
SLP_M# K8 PM_SLP_M# @ PAD T11
TP23 N2 PM_SLP_DSW# @ PAD T22
PMSYNCH BJ10 → H_PM_SYNC 5
SLP_LAN# / GPIO29 F6 PM_SLP_LAN#

+3VS
U44 MC74VHC1G08DFT2G_SC70-5
21 SYS_PWROK → SYS_PWROK
EC_PWROK → EC_PWROK 36,38
VGATE → VGATE 12,53

SYS_PWROK R606 10K_0402_5%
EC_PWROK R632 10K_0402_5%
LAN_RST# R617 10K_0402_5%

No used Integrated LAN,
connecting LAN_RST# to GND

R605 @ 0_0402_5%
Q41 MMBT3906_SOT23-3
PCH_RSMRST# → EC_RSMRST# 36
R604 10K_0402_5%
R598 4.7K_0402_5% +3V
D20A BAV99DW-7_SOT363
D20B BAV99DW-7_SOT363
R591 2.2K_0402_5%

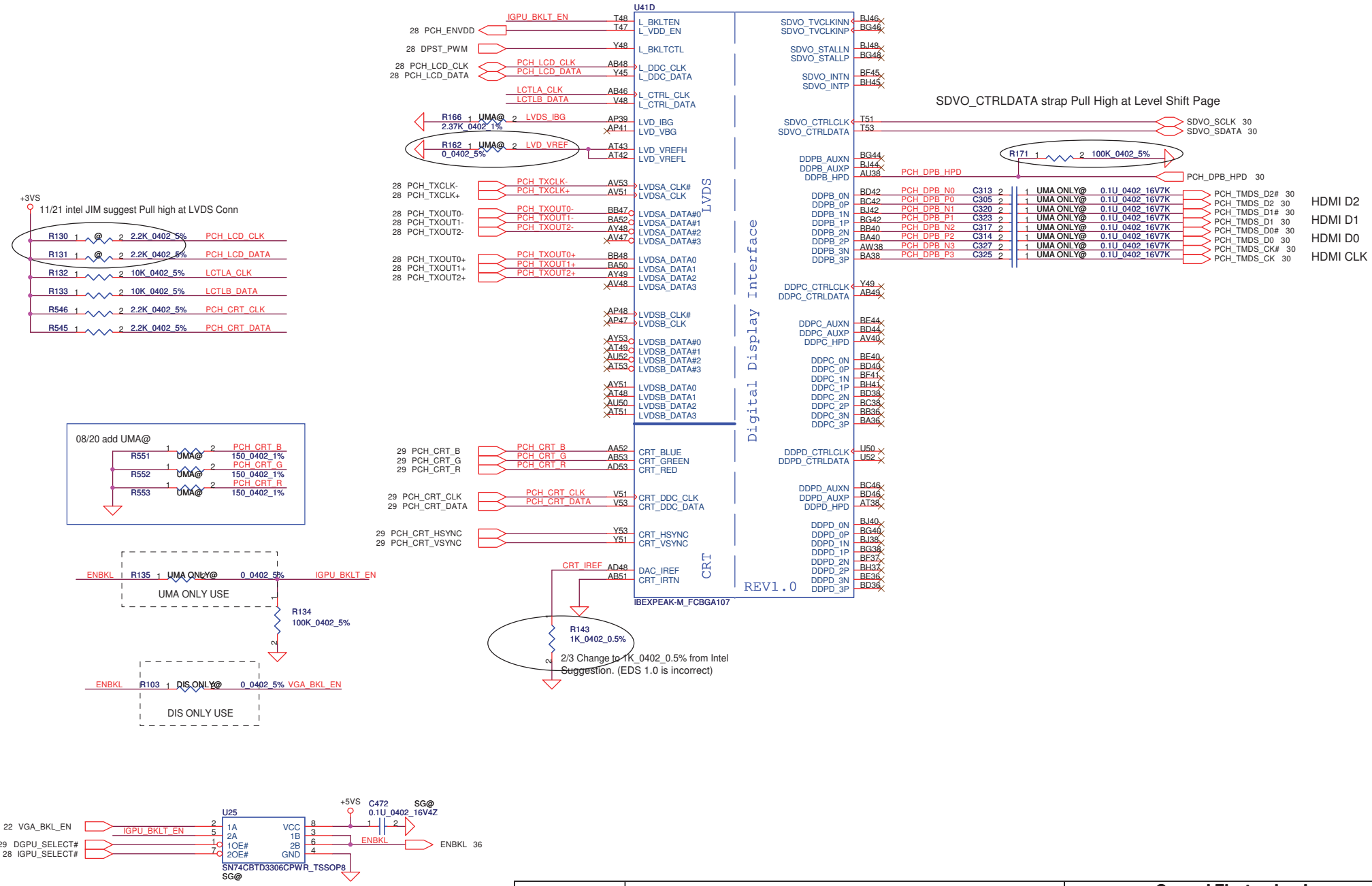
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 15 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

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U41E REV1.0

PCI_GNT0#,PCI_GNT1#,PCI_GNT2#,PCI_GNT3#
has a weak internal pull-up

PCI_GNT2# ESI Strap (Server Only)
this signal should not be pulled low

2008/1/6 2009MOW01 change to 22 ohm

NV_ALE,NV_CLE
has a weak internal pull-down

Design Guide 1.5 Ver:
3.26.13 Terminating Unused Braidwood Interface

If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.

USB/B (Right Side)
USB Port (Left Side)
USB/B (Right Side)
EHCI 1

2/10 USB6, USB7 not support on HM55

CMOS Camera (LVDS)
Card Reader
Mini Card(SIM Card)
Bluetooth
Mini Card(WLAN)
Mini Card(WWAN)
EHCI 2

(For USB Port0, 2)
(For USB Port1)

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating) ★

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +3VS

Disable Intel Anti-Theft Technology : floating(internal PD)

NV_CLE

DMI termination voltage.
weak internal PU, don't PD

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

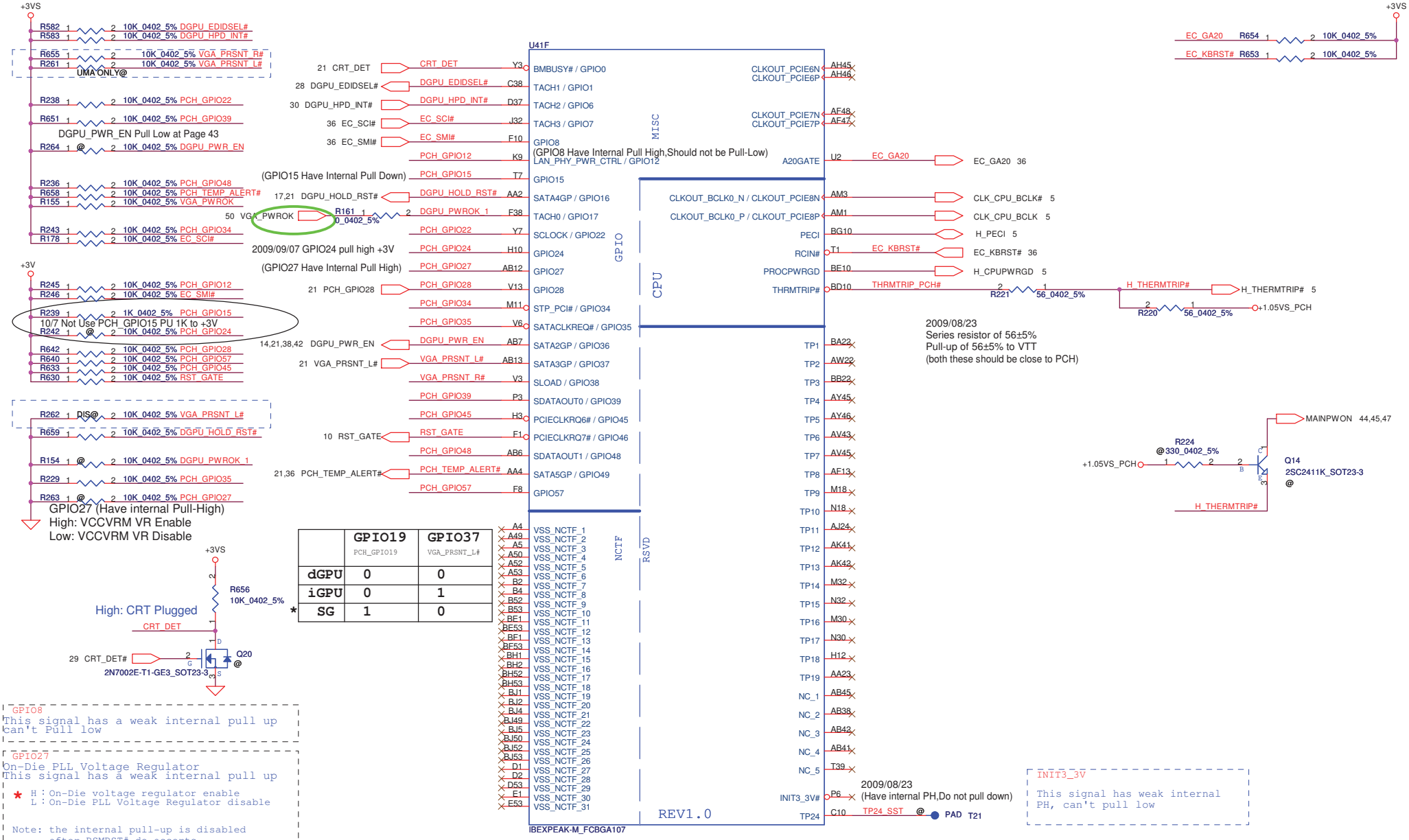
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 17 of 56



	GPIO19 (PCH_GPIO19)	GPIO37 (VGA_PRSNT_L#)
dGPU	0	0
iGPU	0	1
SG	1	0

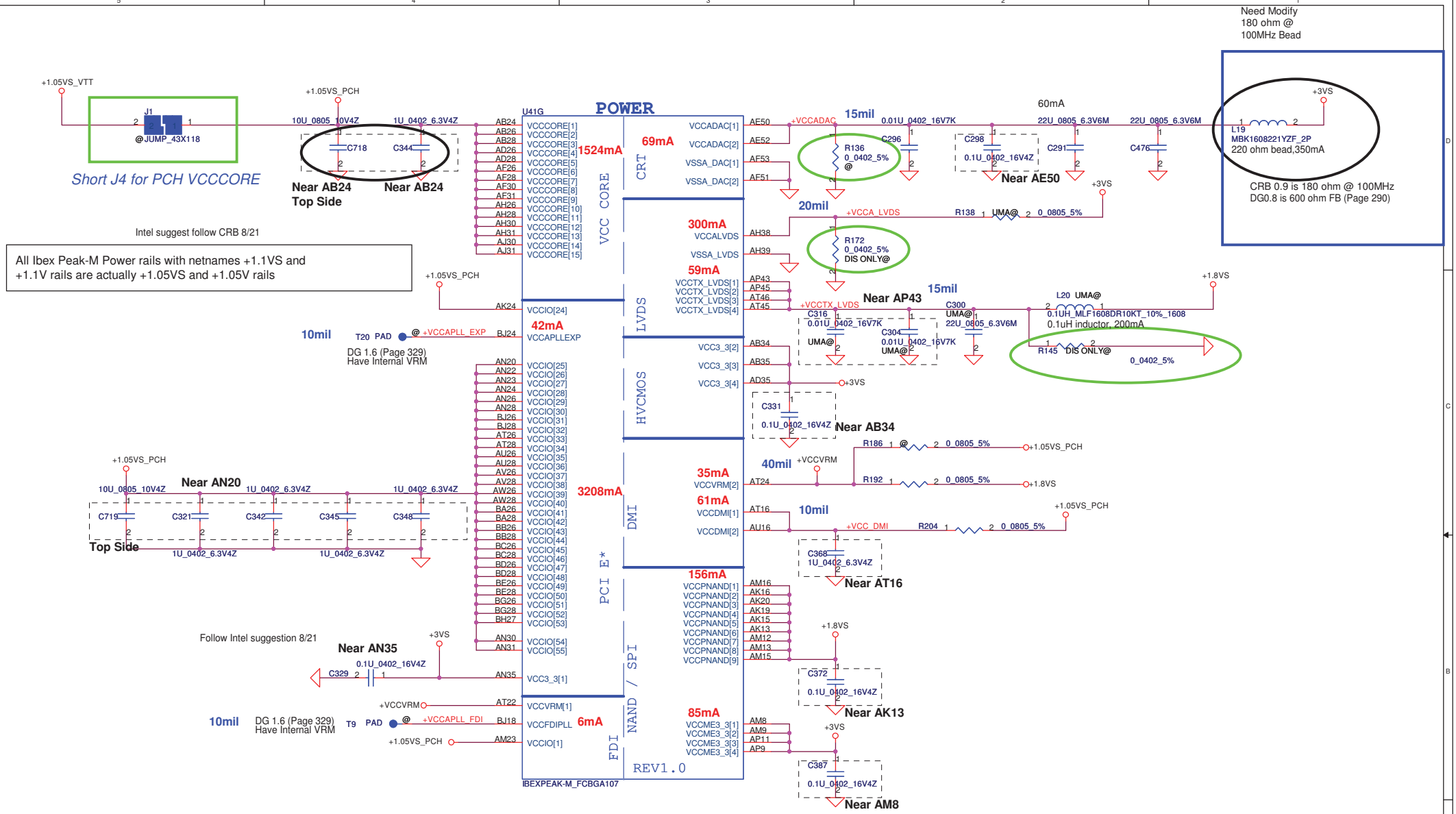
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

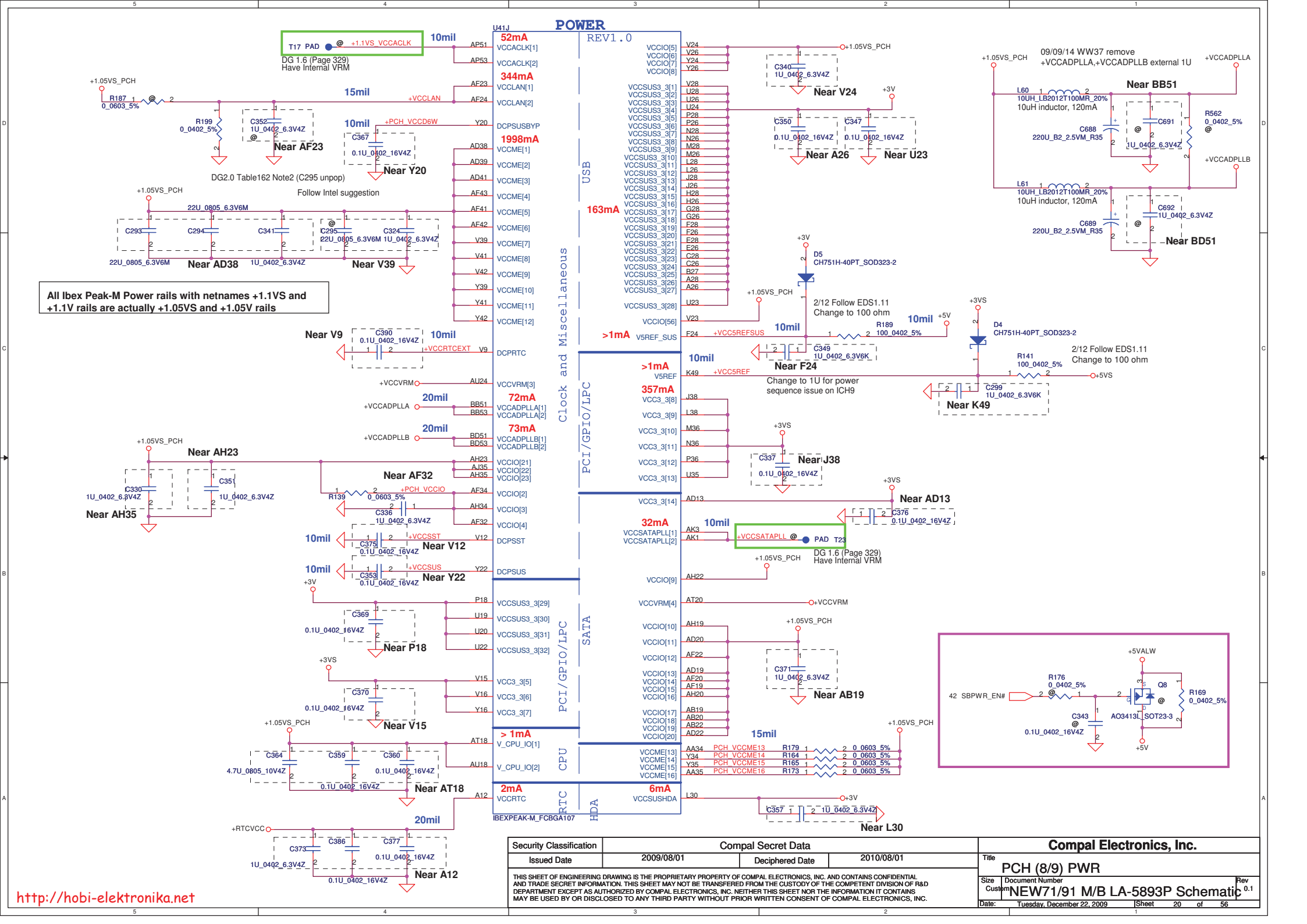
Date: Tuesday, December 22, 2009 | Sheet 18 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title	PCH (7/9) PWR	
Size: Custom	Document Number: NEW71/91 M/B LA-5893P Schematic	Rev: 0.1
Date: Friday, December 18, 2009	Sheet 19 of 56	


POWER
REV1.0
U41J
IBEXPEAK-M_FCBGA107
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails
T17 PAD +1.1VS_VCCACLK
DG 1.6 (Page 329) Have Internal VRM
DG2.0 Table162 Note2 (C295 unpop)
Follow Intel suggestion
09/09/14 WW37 remove +VCCADPLLA,+VCCADPLLB external 1U
10uH inductor, 120mA
2/12 Follow EDS1.11 Change to 100 ohm
Change to 1U for power sequence issue on ICH9
DG 1.6 (Page 329) Have Internal VRM
Near AF23
Near Y20
Near AD38
Near V39
Near V9
Near V24
Near A26
Near U23
Near BB51
Near BD51
Near F24
Near K49
Near J38
Near AD13
Near AH23
Near AF32
Near AH35
Near V12
Near Y22
Near P18
Near V15
Near AT18
Near A12
Near AB19
Near L30
http://hobi-elektronika.net
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Issued Date: 2009/08/01
Deciphered Date: 2010/08/01
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Compal Electronics, Inc.
Title: PCH (8/9) PWR
Size: Custom
Document Number: NEW71/91 M/B LA-5893P Schematic
Rev: 0.1
Date: Tuesday, December 22, 2009
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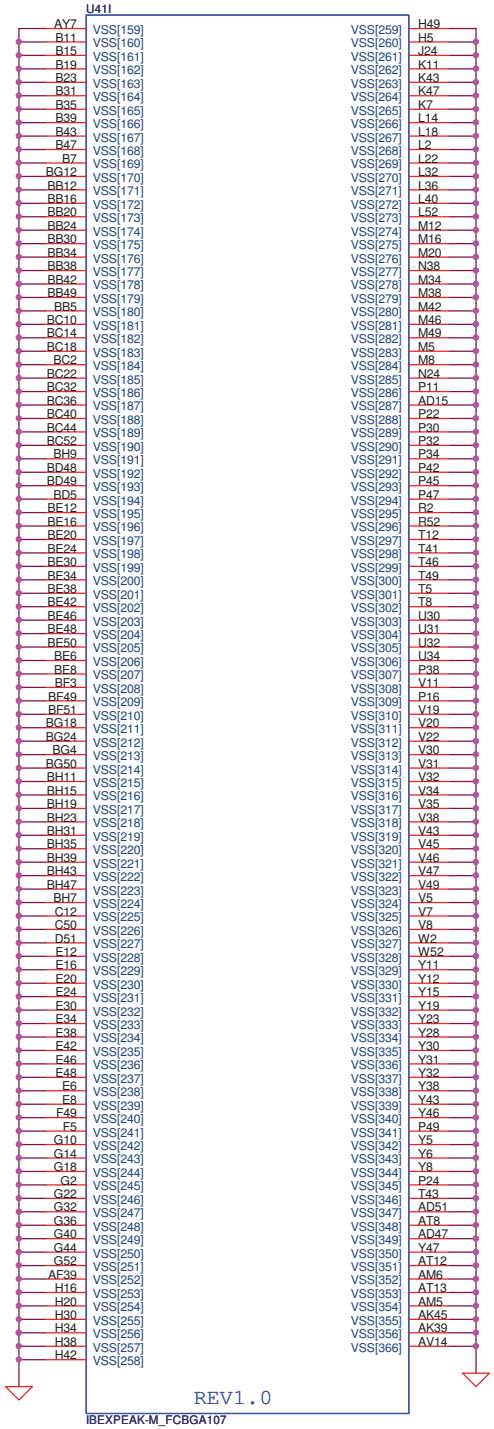
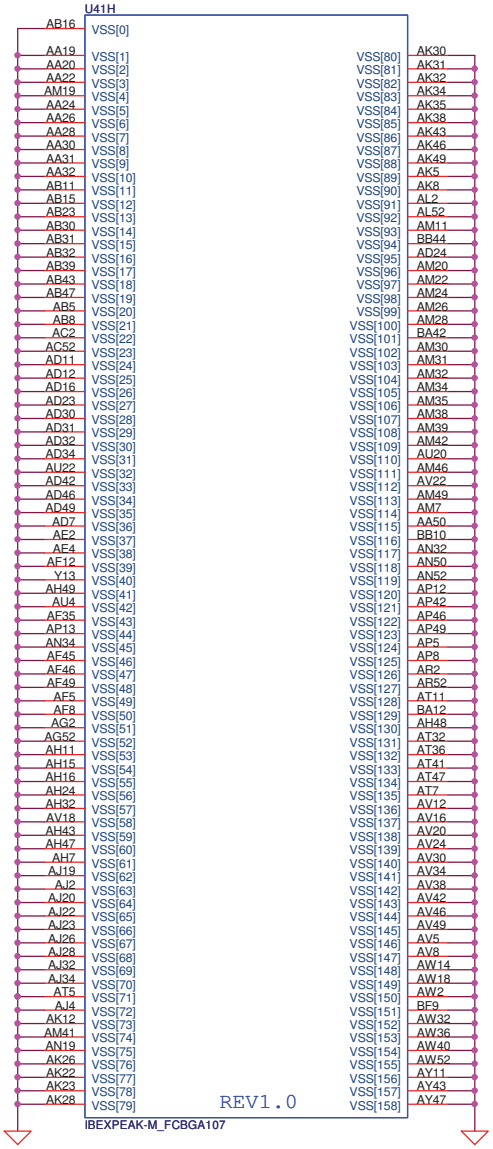
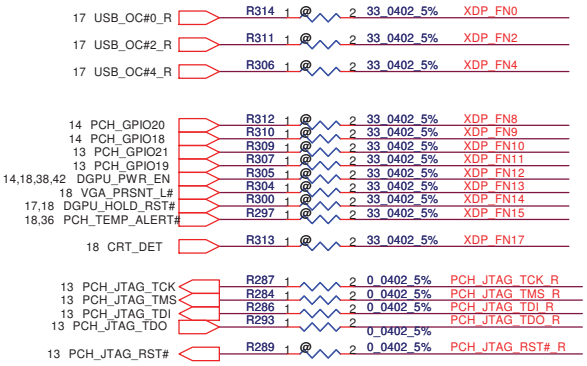
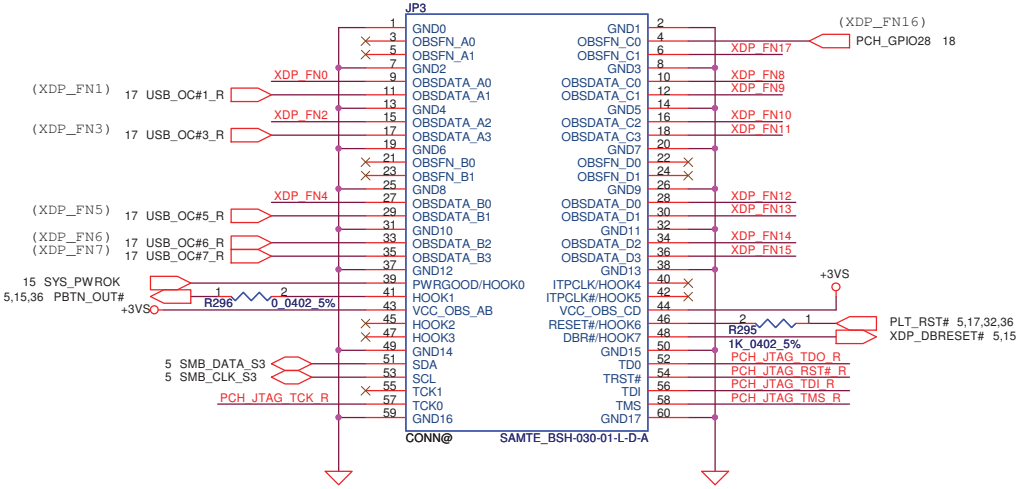
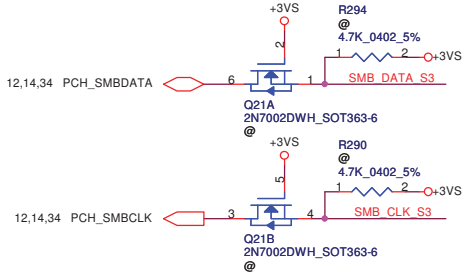
PCH XDP Port











Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 21 of 56

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

Unused MIO interface

When the MIOx interface is unused,
the interface must still be powered by 3.3V,
a decoupling capacitor of 0.1uF
should still be placed on thx MIOx_VDDQ power rail
and 10k pull down should be used on MIOx_CLKIN

External Spread Spectrum

If External Spread Spectrum not stuff then stuff resistor

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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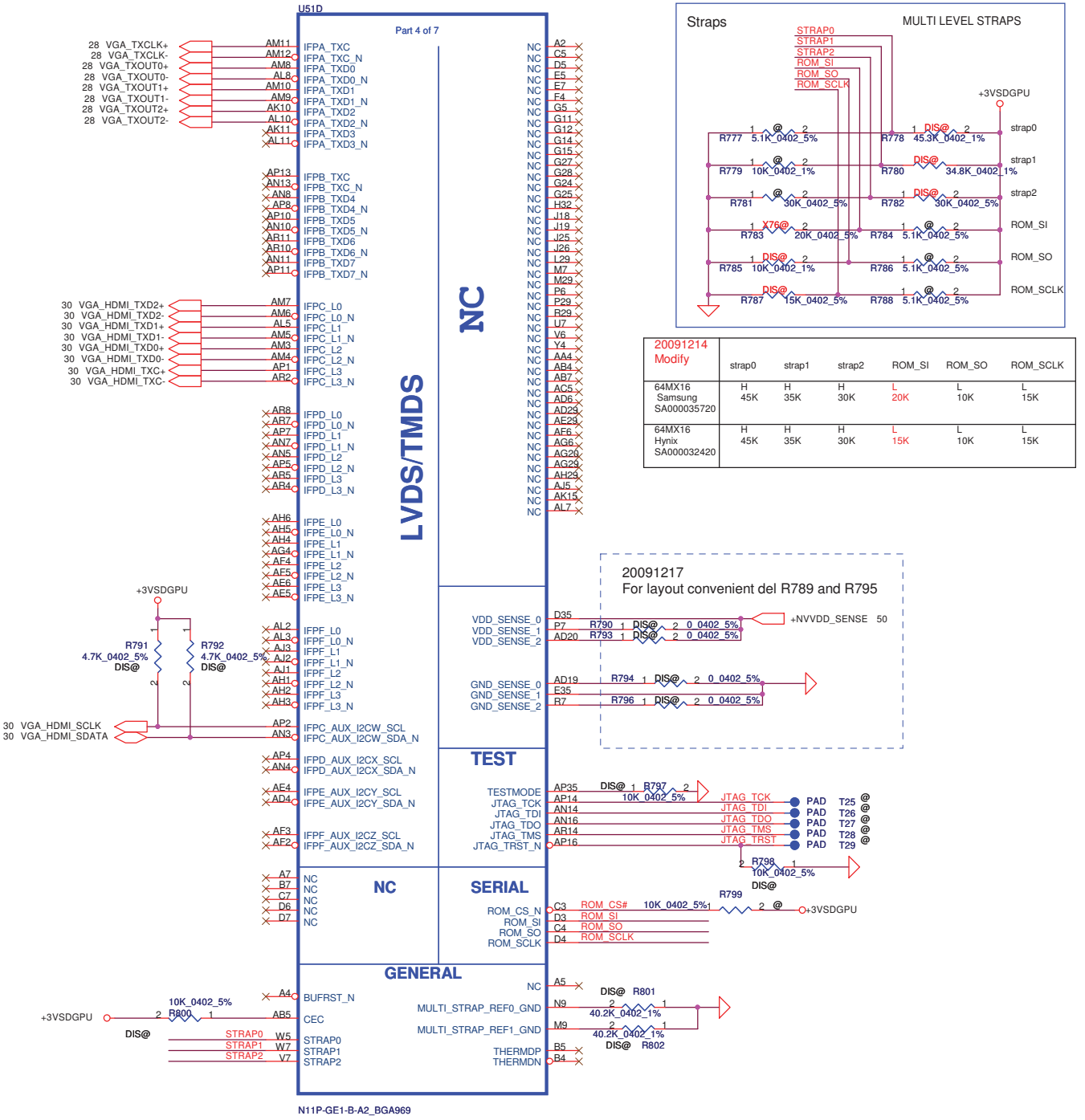
Compal Electronics, Inc.

Title: N11P-GV2H PEG I2C

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Wednesday, December 23, 2009 | Sheet 22 of 56

Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0		CKE_L	
FBx_CMD8	FBx_CMD1		A8	A8
FBx_CMD2	FBx_CMD2		CS0_L*	
FBx_CMD21	FBx_CMD3		A7	A6
FBx_CMD24	FBx_CMD4		A2	A1
FBx_CMD23	FBx_CMD5		A11	A9
FBx_CMD26	FBx_CMD6		A5	A4
FBx_CMD7	FBx_CMD7		A0	A12
FBx_CMD15	FBx_CMD8		CAS*	CAS*
FBx_CMD13	FBx_CMD9		BA1	A3
FBx_CMD4	FBx_CMD10		A9	A11
FBx_CMD18	FBx_CMD11			CS0_H
FBx_CMD29	FBx_CMD12		BA0	BA0
FBx_CMD27	FBx_CMD13		BA2	A15
FBx_CMD6	FBx_CMD14		A3	BA1
FBx_CMD17	FBx_CMD15			CS1_H
FBx_CMD19	FBx_CMD16			ODT_H
FBx_CMD22	FBx_CMD17		A4	A5
FBx_CMD12	FBx_CMD18		A13	A14
FBx_CMD28	FBx_CMD19		WE*	A10
FBx_CMD10	FBx_CMD20		A1	A2
FBx_CMD25	FBx_CMD21		A10	WE*
FBx_CMD9	FBx_CMD22		A12	A0
FBx_CMD1	FBx_CMD23		CS1_L*	
FBx_CMD11	FBx_CMD24		RAS*	RAS*
FBx_CMD0	FBx_CMD25		ODT_L	
FBx_CMD5	FBx_CMD26		A6	A7
FBx_CMD16	FBx_CMD27			CKE_H
FBx_CMD20	FBx_CMD28		RST	RST
FBx_CMD14	FBx_CMD29		A14	A13
FBx_CMD30	FBx_CMD30		A15	BA2
FBx_CMD31				
			LOW	HIGH



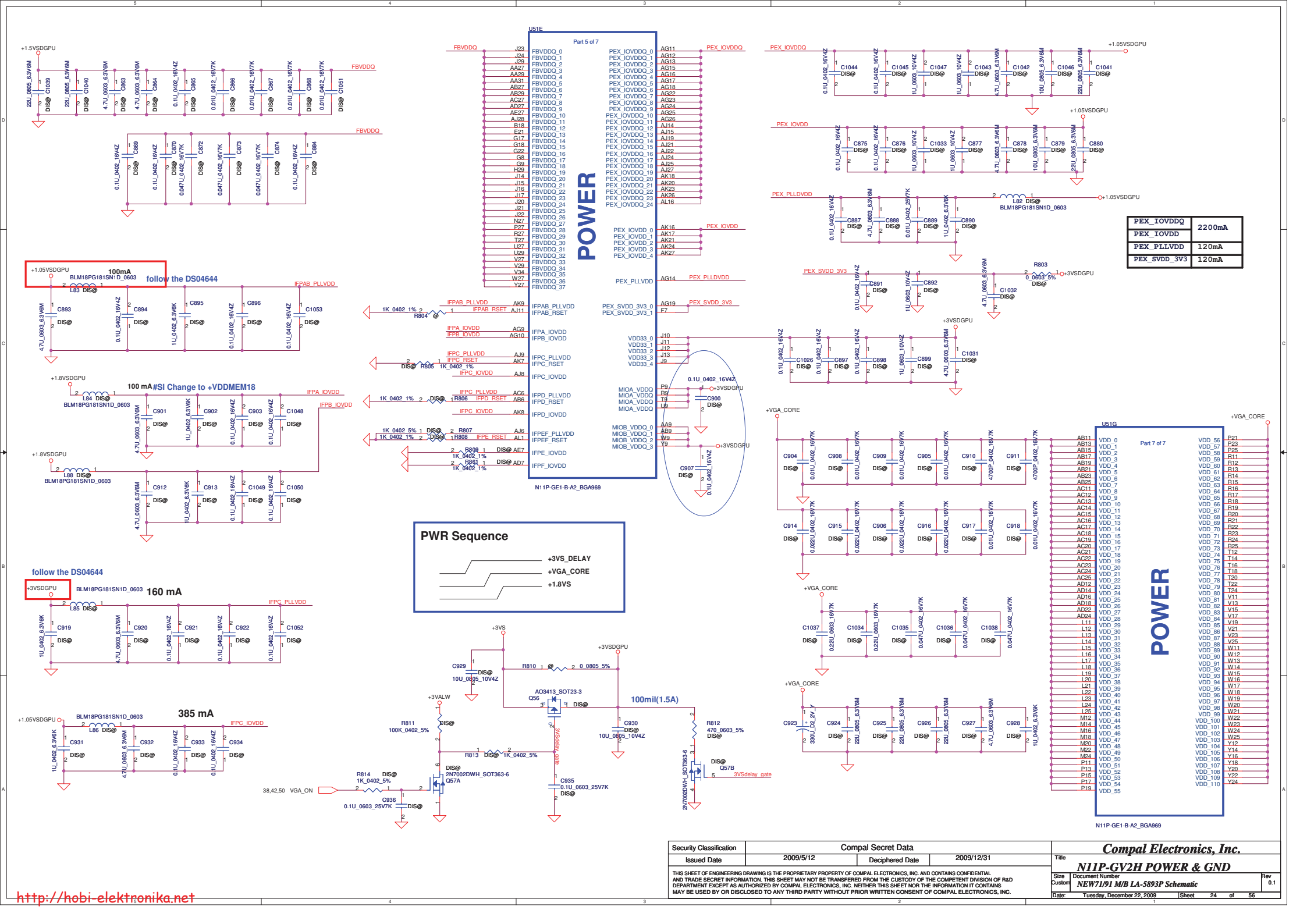
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: N11P-GV2H LVDS

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev:

Date: Tuesday, December 22, 2009 | Sheet 23 of 56



PEX_IOVDDQ	2200mA
PEX_IOVDD	120mA
PEX_PLLVDD	120mA
PEX_SVDD_3V3	120mA

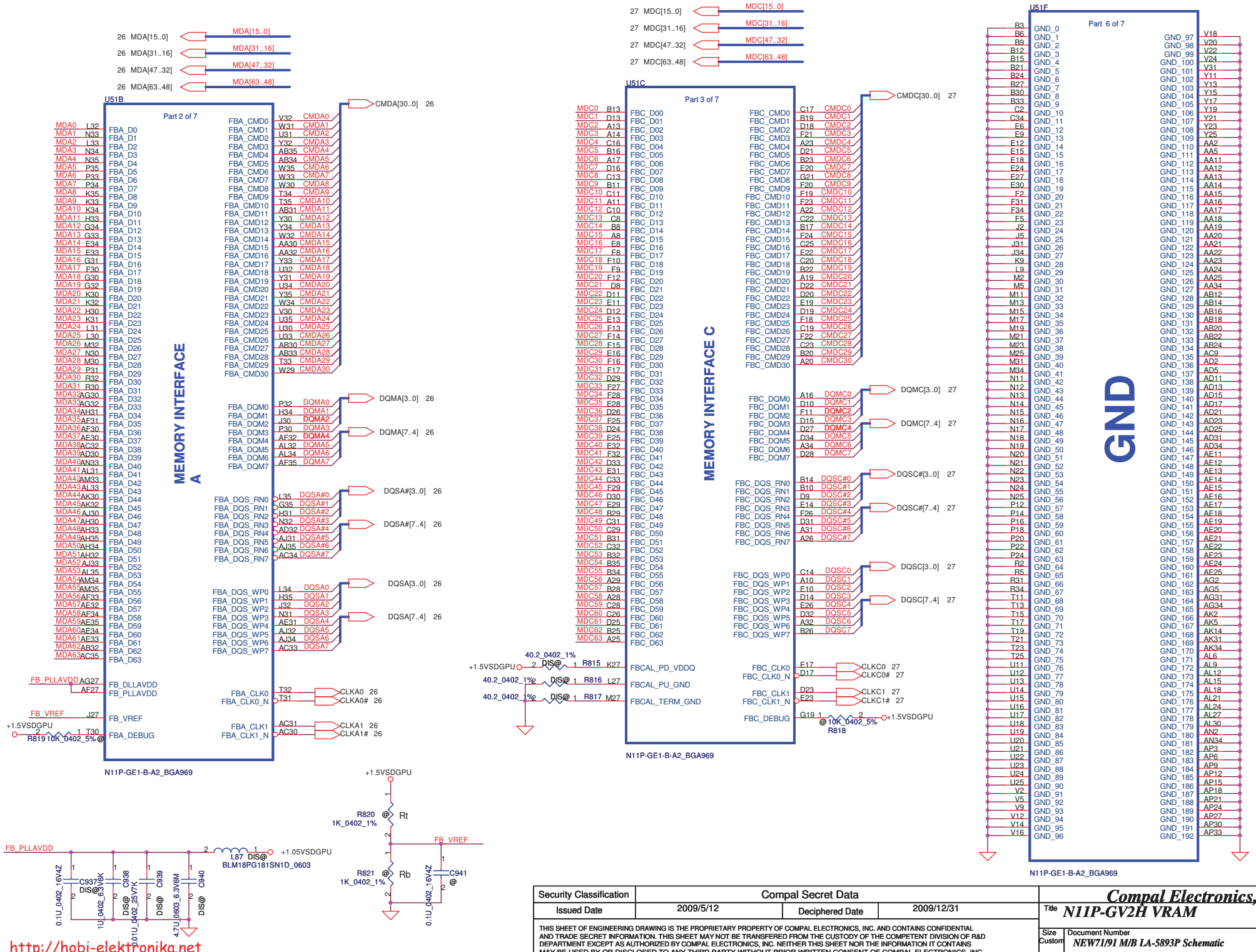
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: N11P-GV2H POWER & GND

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 24 of 56



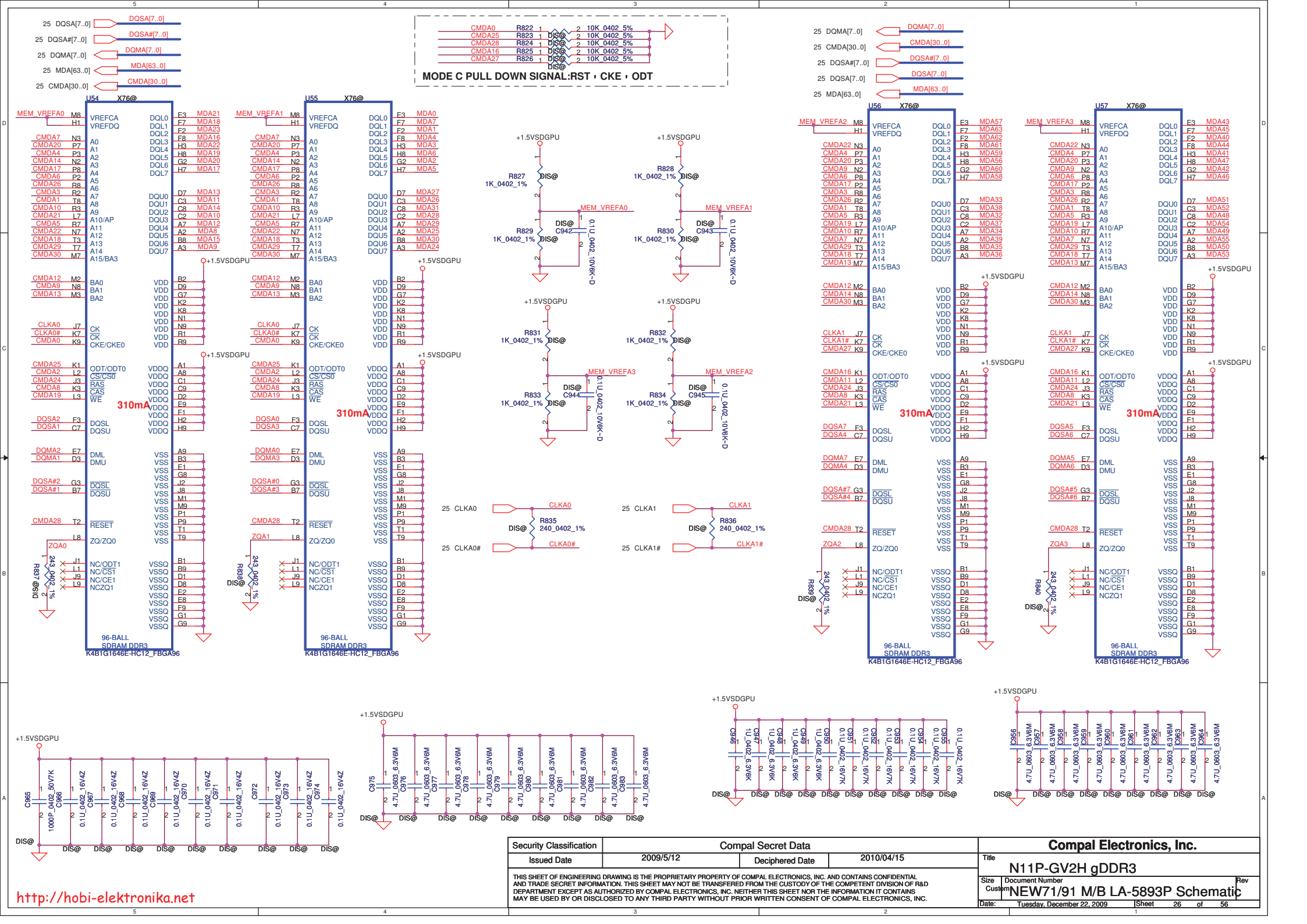
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: N11P-GV2H VRAM

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 25 of 56



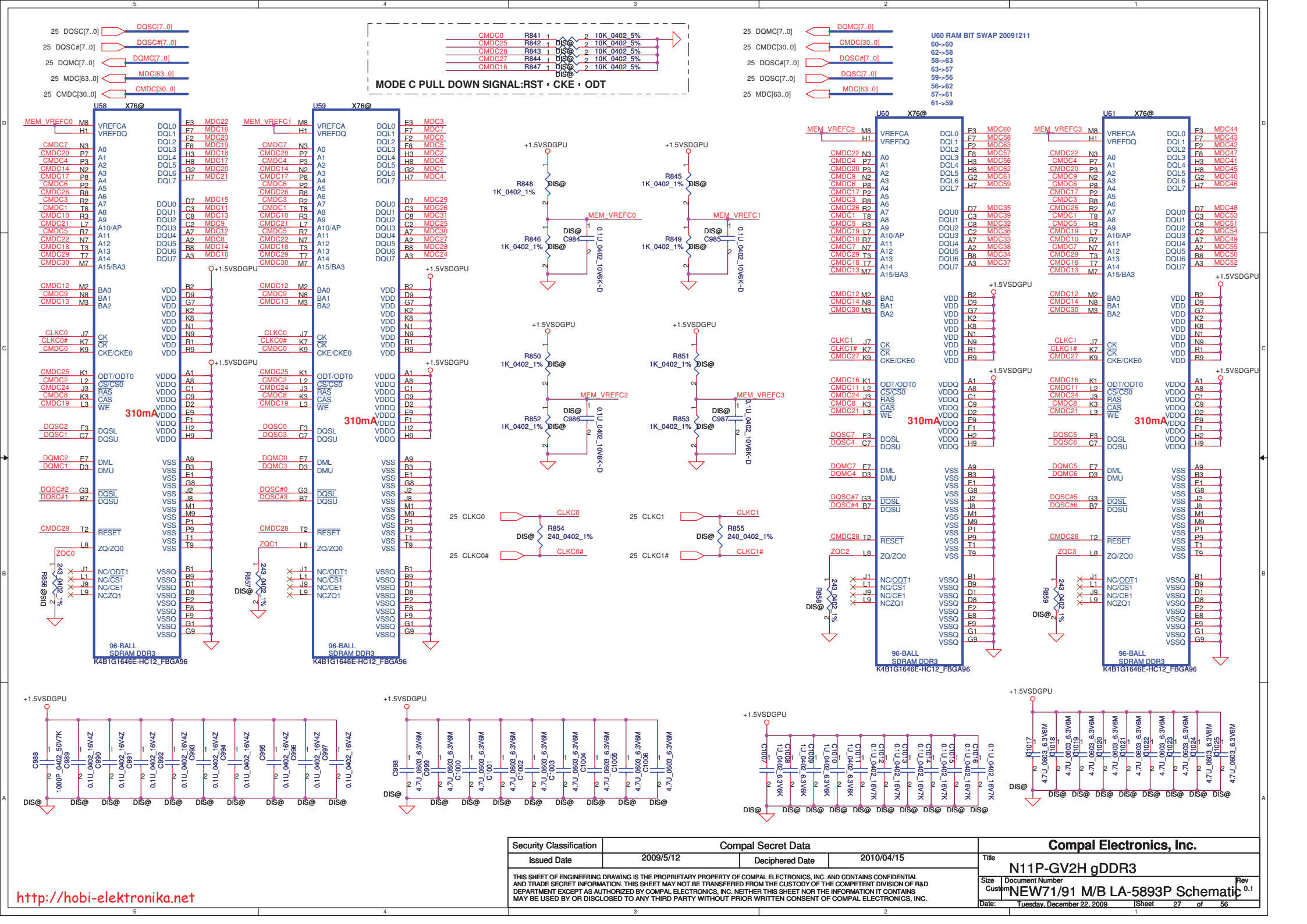
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: N11P-GV2H gDDR3

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev:

Date: Tuesday, December 22, 2009 | Sheet 26 of 56



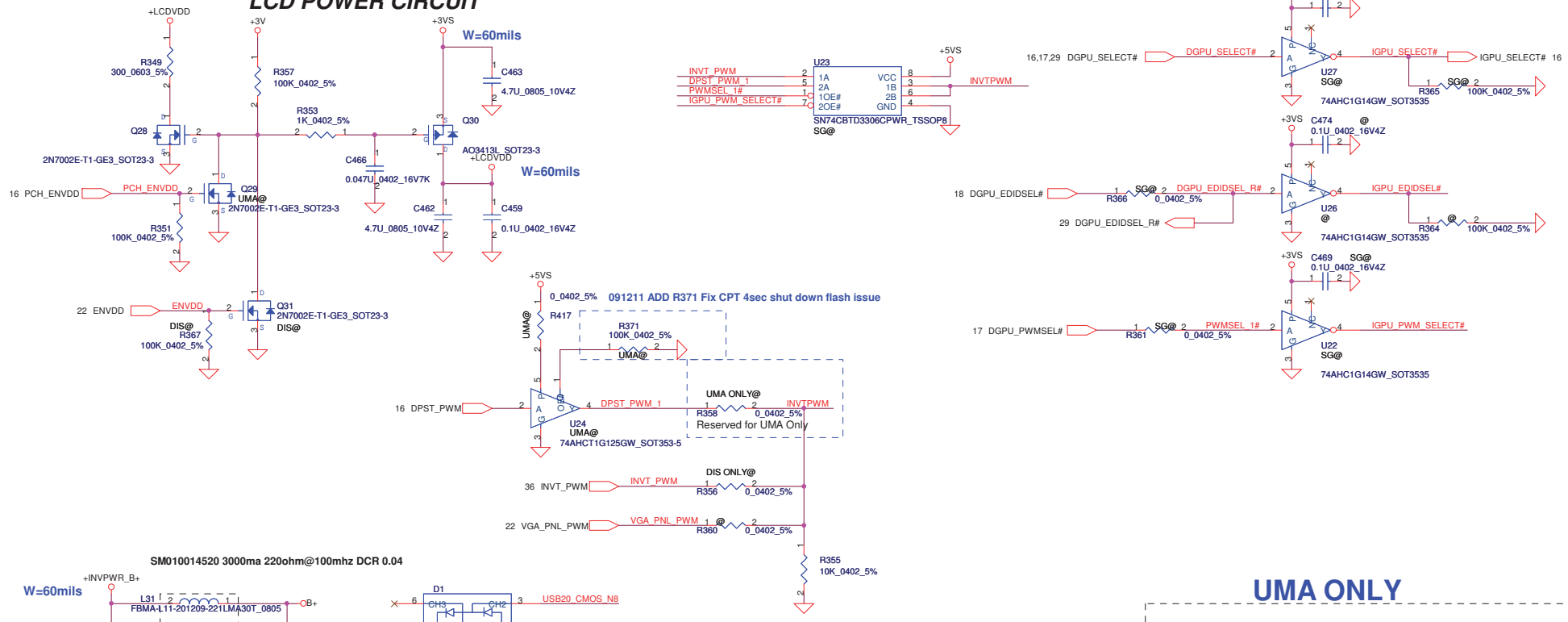
Compal Electronics, Inc.

Title: N11P-GV2H gDDR3

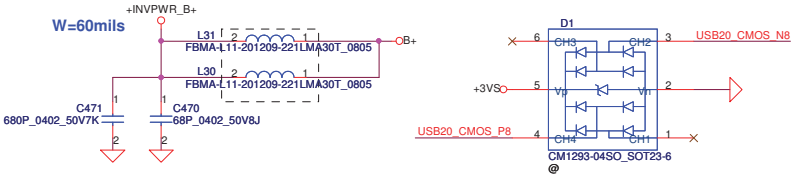
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 27 of 56

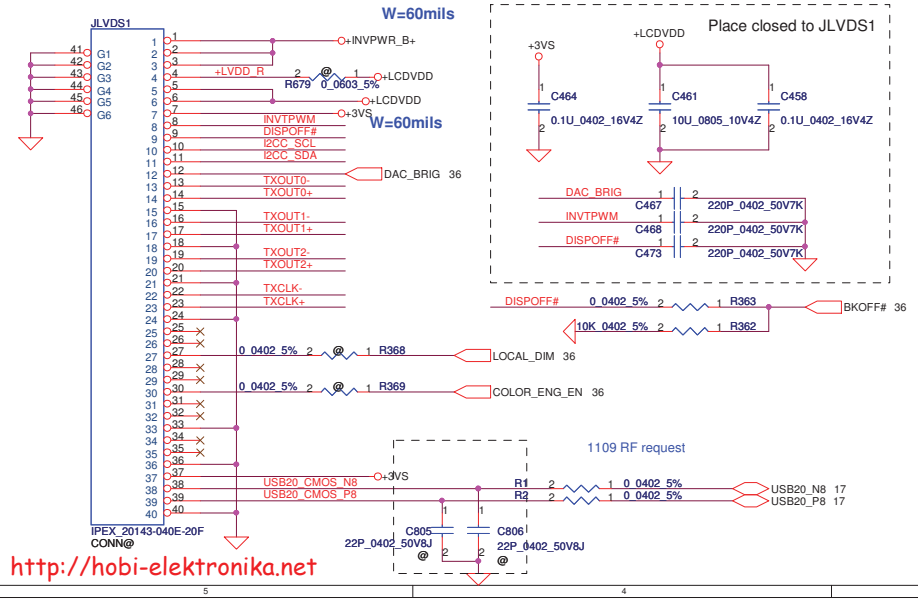
LCD POWER CIRCUIT



SM010014520 3000ma 220ohm@100mhz DCR 0.04



LCD/LED PANEL Conn.

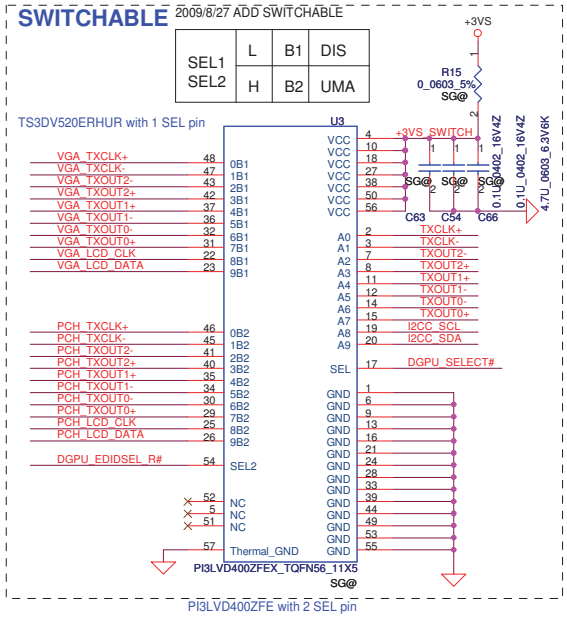


http://hobi-elektronika.net

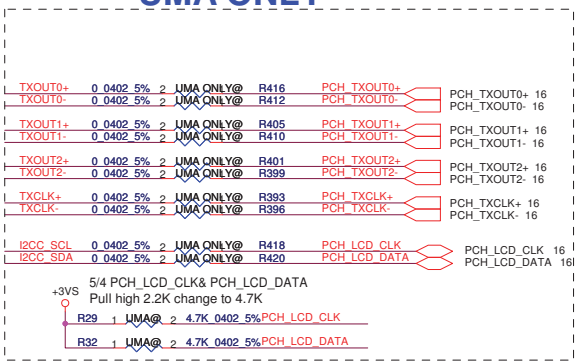
SWITCHABLE

2009/8/27 ADD SWITCHABLE

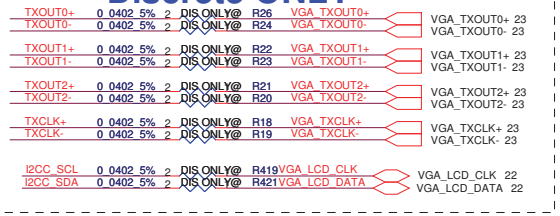
SEL1	L	B1	DIS
SEL2	H	B2	UMA



UMA ONLY



Discrete ONLY



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

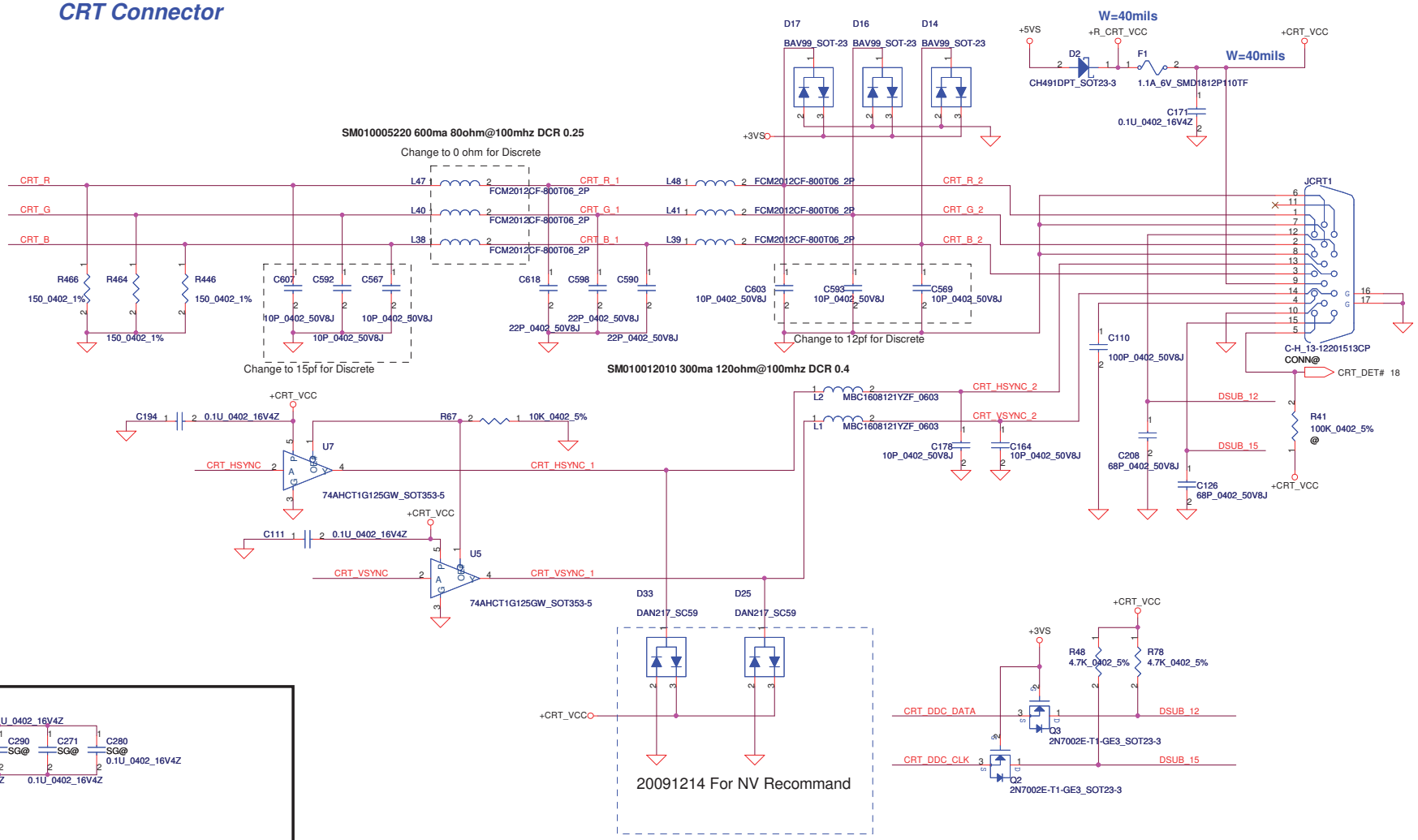
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

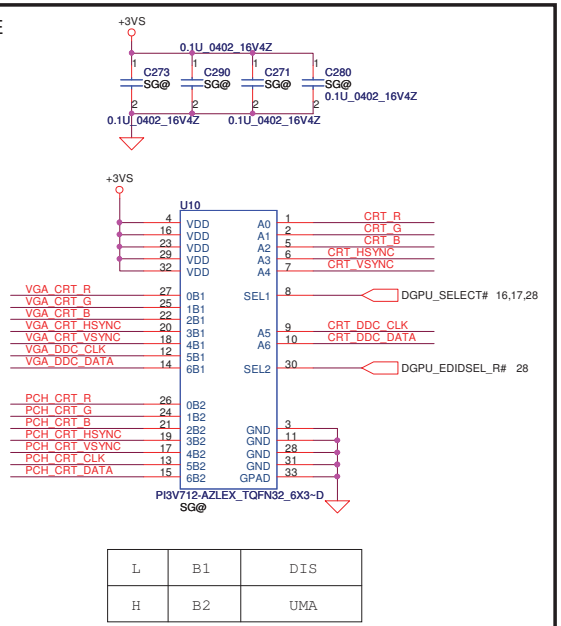
Date: Tuesday, December 22, 2009 | Sheet 28 of 56

CRT Connector



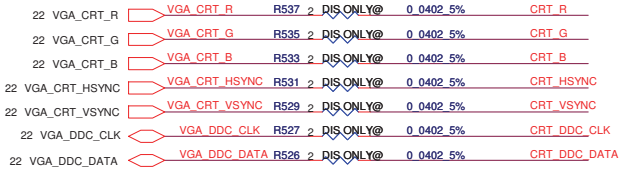
SWITCHABLE

2009/08/27

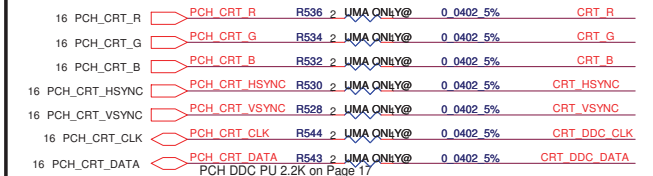


L	B1	DIS
H	B2	UMA

Discrete only



UMA only



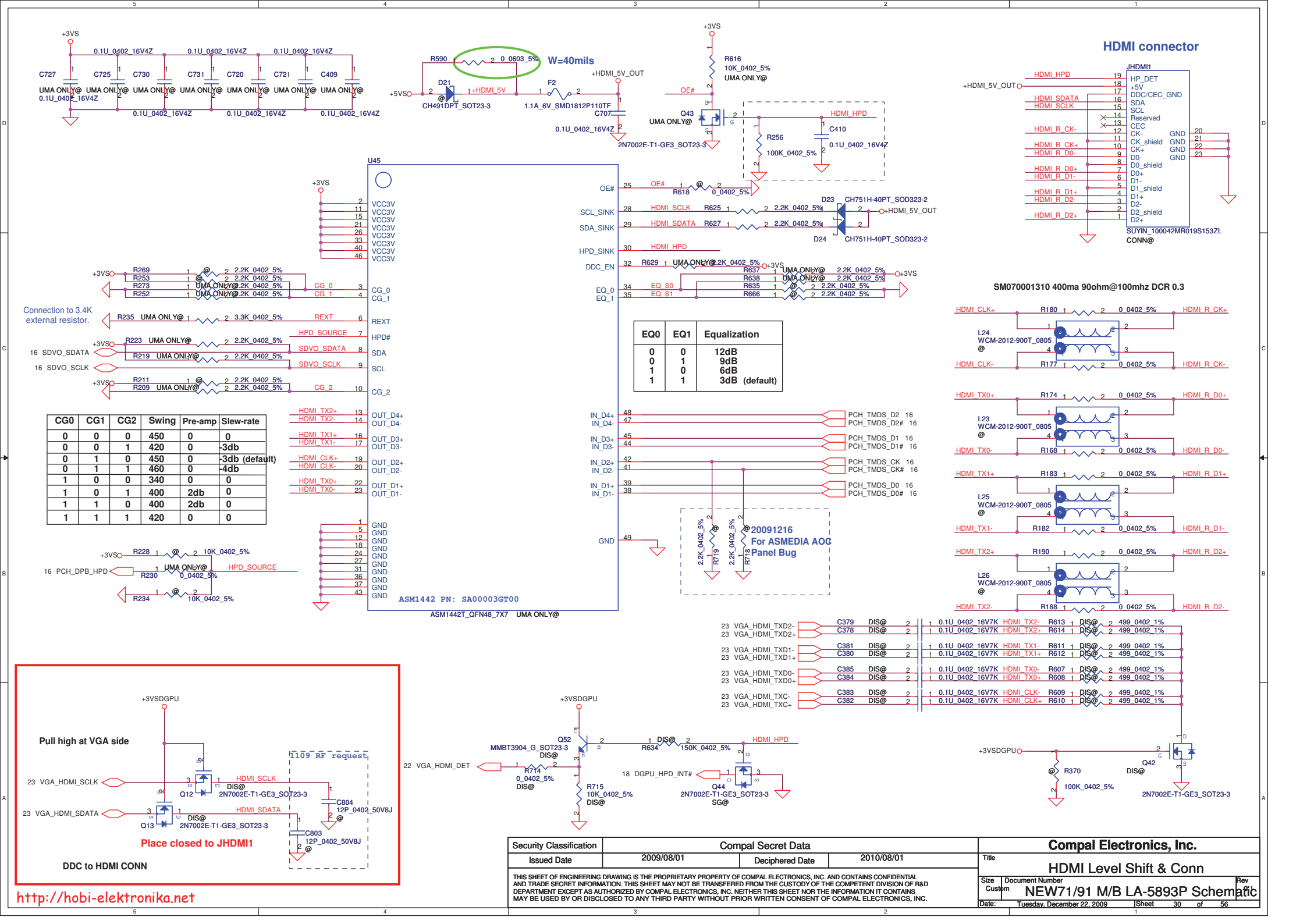
Security Classification	Compal Secret Data	
Issued Date	2009/08/01	Deciphered Date 2010/08/01

Compal Electronics, Inc.

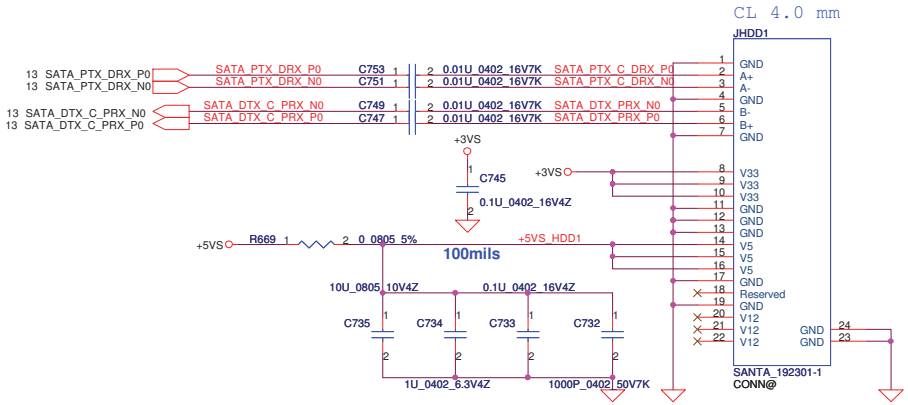
Title: CRT Connector

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

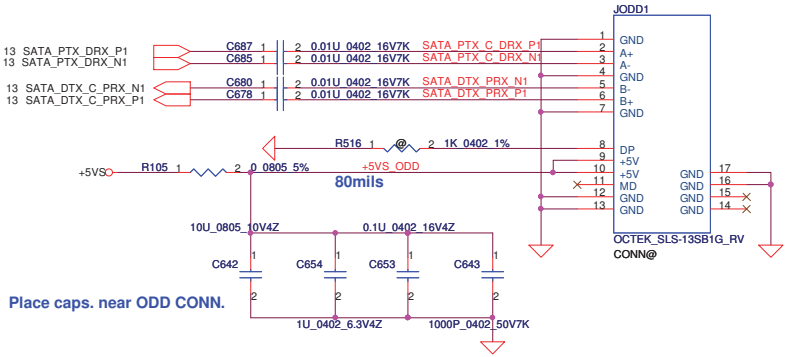
Date: Tuesday, December 22, 2009 | Sheet 29 of 56


HDMI connector
JHDMI1
SUYIN_100042MR019S153ZL
CONN@
SM070001310 400ma 90ohm@100mhz DCR 0.3
U45
ASM1442 PN: SA00003GT00
ASM1442T_QFN48_7X7 UMA ONLY@
Connection to 3.4K external resistor.
EQ0 EQ1 Equalization
0 0 12dB
0 1 9dB
1 0 6dB
1 1 3dB (default)
CG0 CG1 CG2 Swing Pre-amp Slew-rate
0 0 0 450 0 0
0 0 1 420 0 -3db
0 1 0 450 0 -3db (default)
0 1 1 460 0 -4db
1 0 0 340 0 0
1 0 1 400 2db 0
1 1 0 400 2db 0
1 1 1 420 0 0
20091216
For ASMEDIA AOC
Panel Bug
W=40mils
Pull high at VGA side
Place closed to JHDMI1
DDC to HDMI CONN
1109 RF request
http://hobi-elektronika.net
Compal Electronics, Inc.
HDMI Level Shift & Conn
NEW71/91 M/B LA-5893P Schematic
Compal Secret Data
2009/08/01
2010/08/01
Tuesday, December 22, 2009
Sheet 30 of 56

SATA HDD1 Conn.



SATA ODD Conn.



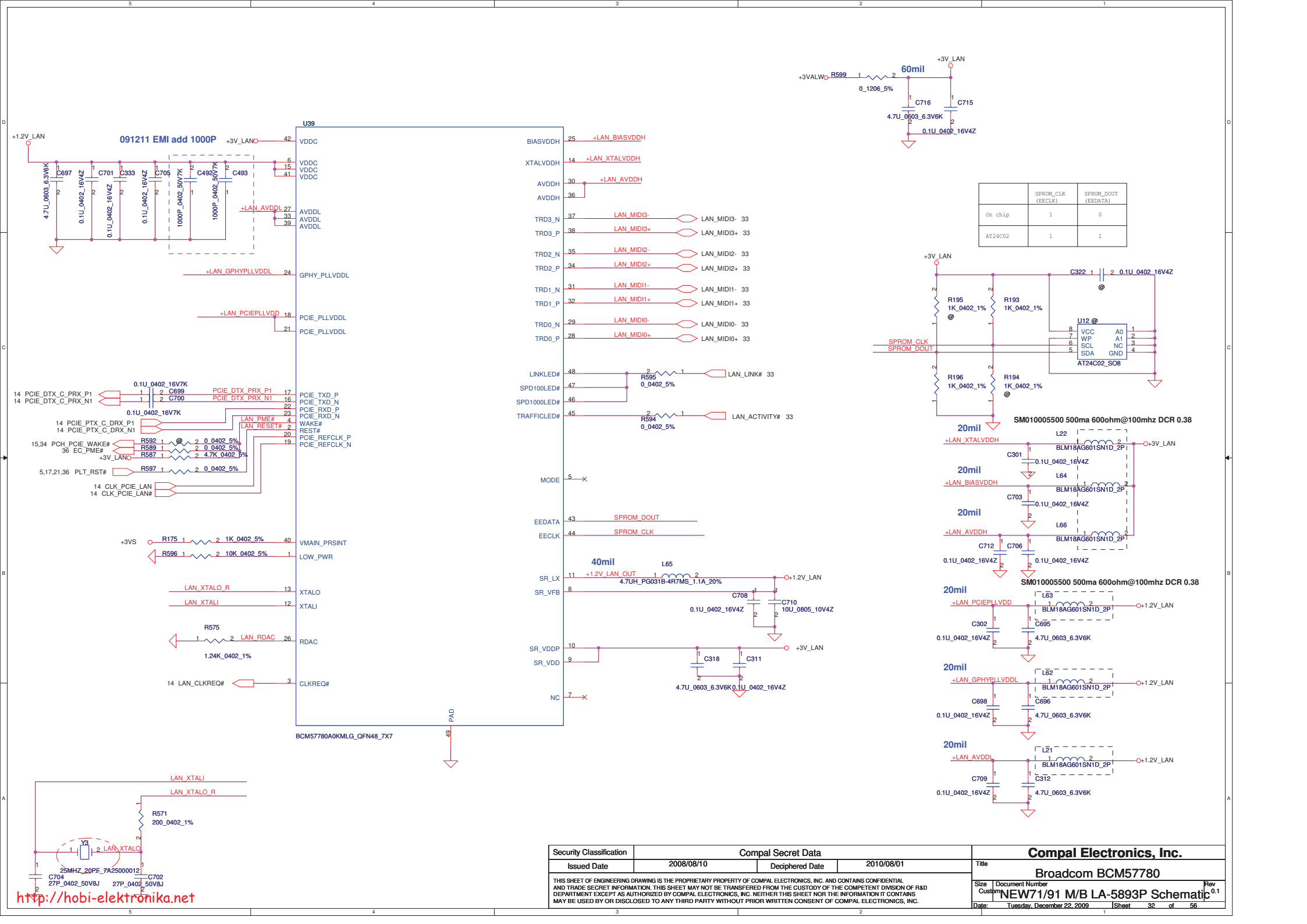
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 31 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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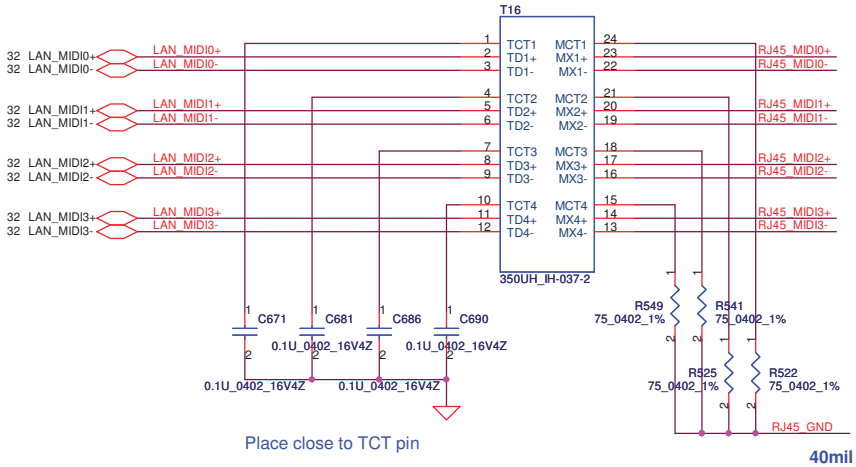
Compal Electronics, Inc.

Title: Broadcom BCM57780

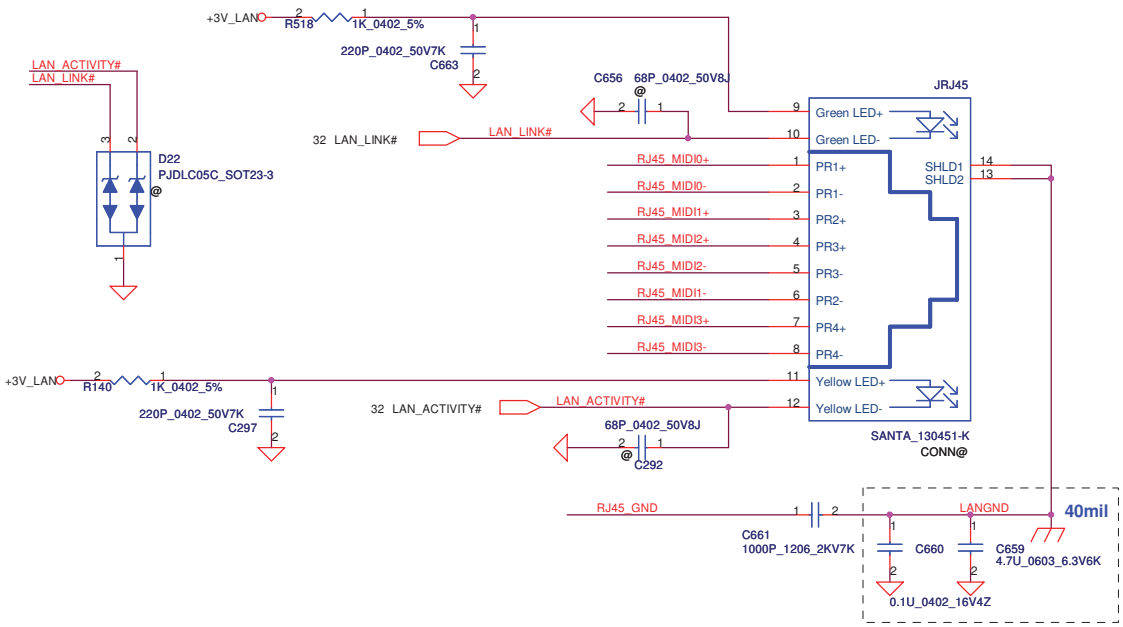
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 32 of 56

LAN Connector



BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



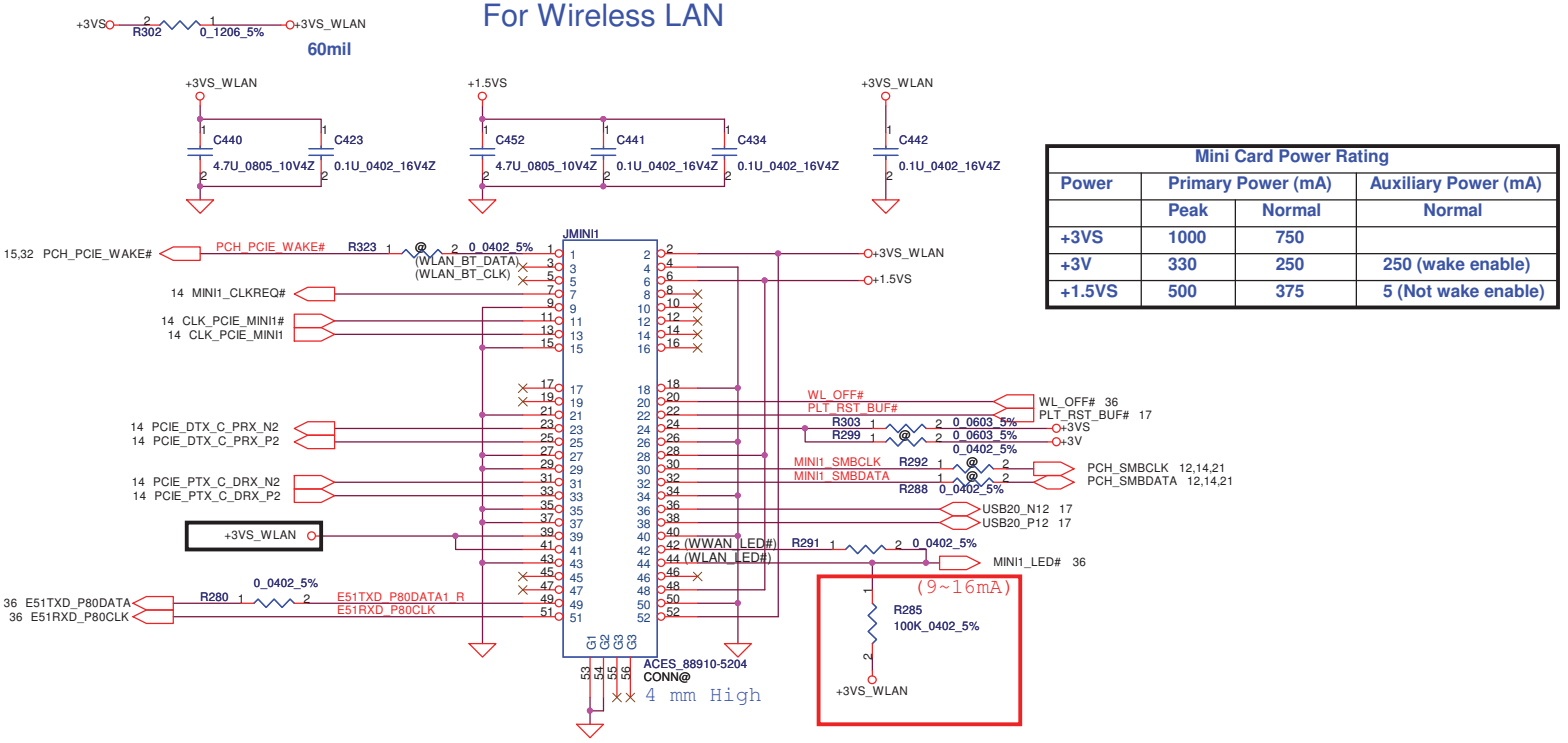
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

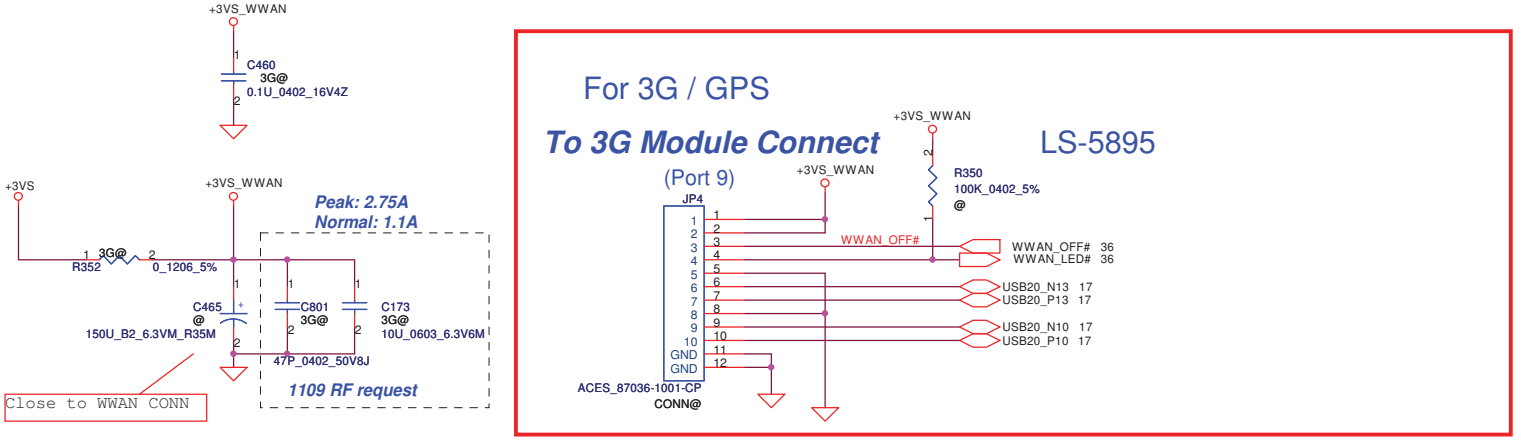
Title: LAN Magnetic & RJ45

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 33 of 56



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



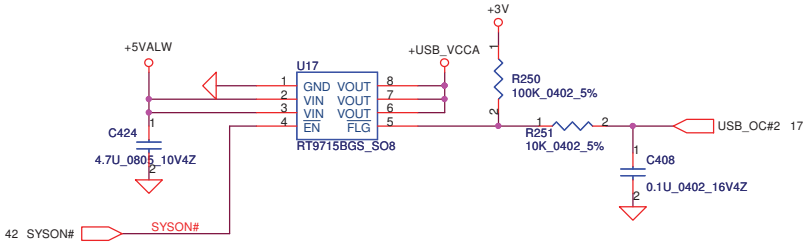
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

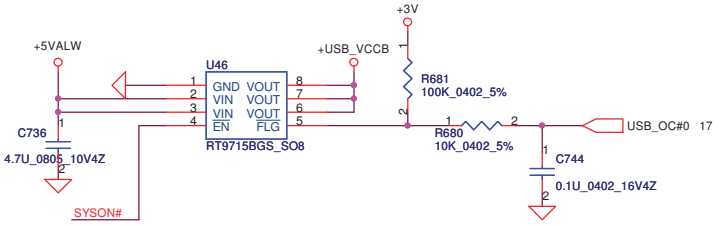
Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

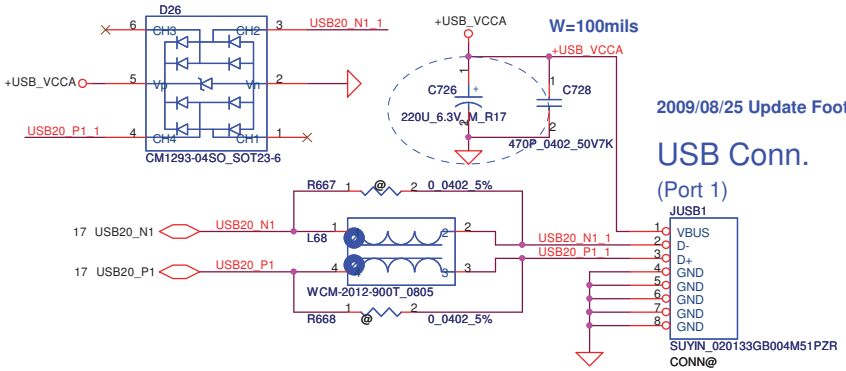
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 34 of 56





2009/08/14 CHANGE cap



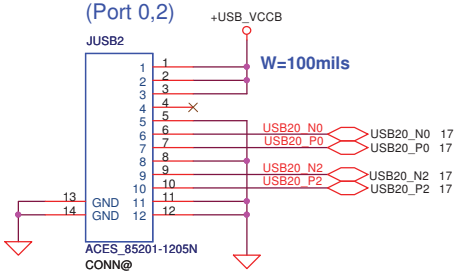
2009/08/25 Update Footprint(follow NAL00)

USB Conn.

(Port 1)

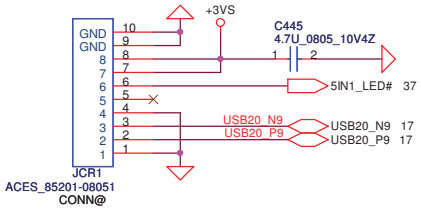
USB/B Conn. LS-5891

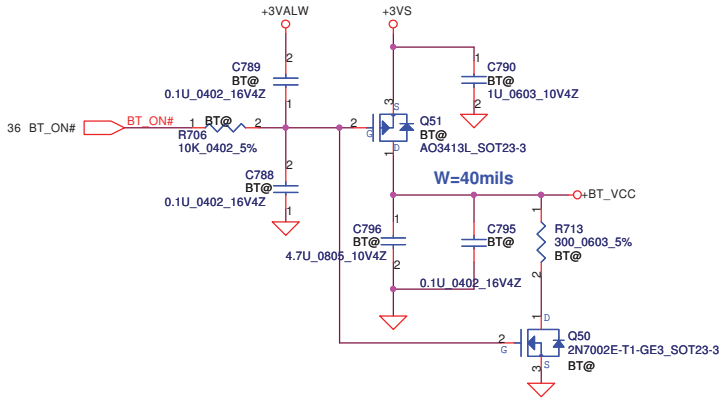
(Port 0,2)



2009/08/24 CHANGE Conn to FFC Type

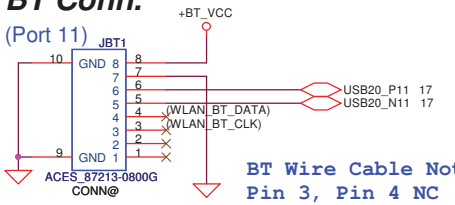
Card Reader Conn. LS-5896





BT Conn.

(Port 11)



BT Wire Cable Note:
Pin 3, Pin 4 NC

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Thursday, December 24, 2009 | Sheet 35 of 56

SM010015410 300ma 80ohm@100mhz DCR 0.3

For EC Tools

Place on RAM door

JP6 — ACES_85205-0400 @

E51RXD_P80CLK → E51RXD_P80CLK 34
E51TXD_P80DATA → E51TXD_P80DATA 34

Place on MiniCard

JP5 — ACES_85205-0400 @

E51RXD_P80CLK
E51TXD_P80DATA

Board ID definition, Please see page 3.

+3VALW
Ra R389 100K_0402_5% @
AD_BID0
Rb R382 0_0402_5%
C496 0.1U_0402_16V4Z

Project ID definition, Please see page 3.

+3VALW
Ra R394 100K_0402_5% @
EC_PROJECTID
Rb R397 0_0402_5%
C511 0.1U_0402_16V4Z @

PCH_TEMP_ALERT# Pull high at Page 18 (PCH side)

+5VS
TP_CLK R404 4.7K_0402_5%
TP_DATA R408 4.7K_0402_5%

+3VALW
3S/4S# R423 100K_0402_5%
65W/90W# R424 100K_0402_5%
VGA_idle R428 DIS@ 100K_0402_5%

1109 RF request

C516 22P_0402_50V8J
R403 47_0402_5%
17 CLK_PCI_LPC
+3VALW R375 47K_0402_5%
C487 0.1U_0402_16V4Z
5,17,21,32 PLT_RST#

For Low PWR Pannel use

+3VS
R508 E51TXD_P80DATA 100K_0402_5%
R509 LOCAL_DIM 100K_0402_5%
R511 COLOR_ENG_EN 100K_0402_5%

15 SUSCLK — R740 @ 0_0402_5% — EC_CRY1 / EC_CRY2

+3VS
R398 EC_SMB_CK2 2.2K_0402_5%
R400 EC_SMB_DA2 2.2K_0402_5%
R402 GFX_CORE_PWRGD 10K_0402_5%

+3VALW
R392 EC_SMB_CK1 2.2K_0402_5%
R395 EC_SMB_DA1 2.2K_0402_5%
R422 LID_SW# 100K_0402_5%
R374 KSO1 47K_0402_5%
R373 KSO2 47K_0402_5%
R426 @ EC_PME# 10K_0402_5%

+3VALW — R385 0_0805_5% — 0.1U_0402_16V4Z / 0.1U_0402_16V4Z / 40mil / +3VALW_EC
C512 C519 C533 C538 C524 C488 1000P_0402_50V7K
0.1U_0402_16V4Z 0.1U_0402_16V4Z 1000P_0402_50V7K

L32 FBMA-L11-160808-800LMT_0603 — 20mil — +EC_VCCA
C505 0.1U_0402_16V4Z
ECAGND

KSI[0..7] → KSI[0..7] 37
KSO[0..17] → KSO[0..17] 37

U32 — KB926QFD3_LQFP128_14X14 — <BOM Structure>

VCC 9, 22, 33, 96, 111, 125 — AVCC 67 — GND 11, 24, 35, 94, 113 — AGND 69

LPC & MISC
- 18 EC_GA20 → EC_GA20 → GA20/GPIO00
- 18 EC_KBRST# → EC_KBRST# → KBRST#/GPIO01
- 13 SERIRQ → SERIRQ → SERIRQ#
- 13 LPC_FRAME# → LPC_FRAME# → LFRAME#
- 13 LPC_AD3 → LPC_AD3 → LAD3
- 13 LPC_AD2 → LPC_AD2 → LAD2
- 13 LPC_AD1 → LPC_AD1 → LAD1
- 13 LPC_AD0 → LPC_AD0 → LAD0
- PCICLK
- 5,17,21,32 PLT_RST# → EC_RST# → PCIRST#/GPIO05
- ECRST#
- 18 EC_SCI# → EC_SCI# → SCI#/GPIO0E
- 15 PM_CLKRUN# → CLKRUN#/GPIO1D

PWM Output
- INVT_PWM/PWM1/GPIO0F
- BEEP#/PWM2/GPIO10 → BEEP# 39
- FANPWM1/GPIO12 → ME_OVERRIDE 13
- ACOFF/FANPWM2/GPIO13 → ACOFF 27 → ACOFF 46,47

AD Input
- BATT_TEMP/AD0/GPIO38 → BATT_TEMP 63 → BATT_TEMP 44
- BATT_OVP/AD1/GPIO39 → BATT_OVP 64 → BATT_OVP 46
- ADP_I/AD2/GPIO3A → ADP_I 65 → ADP_I 46
- AD3/GPIO3B → AD_BID0 66
- AD4/GPIO42 → EC_PROJECTID 75
- SELIO2#/AD5/GPIO43 76

DA Output
- DAC_BRIG/DA0/GPIO3C → DAC_BRIG 68 → DAC_BRIG 28
- EN_DFAN1/DA1/GPIO3D → EN_DFAN1 70 → EN_DFAN1 41
- IREF/DA2/GPIO3E → IREF 71 → IREF 46
- CALIBRATE#/DA3/GPIO3F → CALIBRATE# 72 → CALIBRATE# 46

PS2 Interface
- PSCLK1/GPIO4A → EC_MUTE# 83 → EC_MUTE# 40
- PSDAT1/GPIO4B → GFX_CORE_PWRGD 84 → GFX_CORE_PWRGD 52
- PSCLK2/GPIO4C → WWAN_LED# 85 → WWAN_LED# 34
- PSDAT2/GPIO4D → VGA_idle 86 → VGA_idle 22
- TP_CLK/PSCLK3/GPIO4E → TP_CLK 87 → TP_CLK 37
- TP_DATA/PSDAT3/GPIO4F → TP_DATA 88 → TP_DATA 37

SPI Device Interface
- SDICS#/GPXOA00 → 3S/4S# 97 → 3S/4S# 46
- SDICLK/GPXOA01 → 65W/90W# 98 → 65W/90W# 46
- SDIDO/GPXOA02 → SBPWR_EN 99 → SBPWR_EN 42
- SDIDI/GPXID0 → LID_SW# 109 → LID_SW# 37

SPI Flash ROM
- SPIDI/RD# → EC_SI_SPI_SO 119 → EC_SI_SPI_SO 37
- SPIDO/WR# → EC_SO_SPI_SI 120 → EC_SO_SPI_SI 37
- SPICLK/GPIO58 → EC_SPICLK 126 → EC_SPICLK 37
- SPICS# → EC_SPICS#/FSEL# 128 → EC_SPICS#/FSEL# 37

Int. K/B Matrix
- KSI0/GPIO30 … KSI7/GPIO37 (55–62)
- KSO0/GPIO20 … KSO17/GPIO49 (39–54, 81, 82)

GPIO
- CIR_RX/GPIO40 → WWAN_OFF# 73 → WWAN_OFF# 34
- CIR_RLC_TX/GPIO41 → PCH_TEMP_ALERT# 74 → PCH_TEMP_ALERT# 18,21
- FSTCHG/SELIO#/GPIO50 → FSTCHG 89 → FSTCHG 46
- BATT_CHGI_LED#/GPIO52 → BATT_GRN_LED# 90 → BATT_GRN_LED# 37
- CAPS_LED#/GPIO53 → 3G_LED# 91 → 3G_LED# 37
- BATT_LOW_LED#/GPIO54 → BATT_AMB_LED# 92 → BATT_AMB_LED# 37
- SUSP_LED#/GPIO55 → PWR_LED 93 → PWR_LED 37
- SYSON/GPIO56 → SYSON 95 → SYSON 42,49
- VR_ON/XCLK32K/GPIO57 → VR_ON 121 → VR_ON 38,53
- AC_IN/GPIO59 → ACIN 127 → ACIN 37,42,43

(CAPS_LED#)

SM Bus
- 44 EC_SMB_CK1 → EC_SMB_CK1 77 → SCL1/GPIO44
- 44 EC_SMB_DA1 → EC_SMB_DA1 78 → SDA1/GPIO45
- 14,22 EC_SMB_CK2 → EC_SMB_CK2 79 → SCL2/GPIO46
- 14,22 EC_SMB_DA2 → EC_SMB_DA2 80 → SDA2/GPIO47

GPIO
- 15 PM_SLP_S3# → PM_SLP_S3# 6 → PM_SLP_S3#/GPIO04
- 15 PM_SLP_S5# → PM_SLP_S5# 14 → PM_SLP_S5#/GPIO07
- 18 EC_SMI# → EC_SMI# 15 → EC_SMI#/GPIO08
- 15 EC_ACIN → EC_ACIN 16 → LID_SW#/GPIO0A
- 34 MINI1_LED# → MINI1_LED# 17 → SUSP#/GPIO0B
- 28 LOCAL_DIM → LOCAL_DIM 18 → PBTN_OUT#/GPIO0C
- 28 COLOR_ENG_EN → COLOR_ENG_EN 19 → EC_PME#/GPIO0D
- 28 INVT_PWM → INVT_PWM 25 → EC_THERM#/GPIO11
- 41 FAN_SPEED1 → FAN_SPEED1 28 → FAN_SPEED1/FANFB1/GPIO14
- 35 BT_ON# → BT_ON# 29 → FANFB2/GPIO15
- E51TXD_P80DATA 30 → EC_TX/GPIO16
- E51RXD_P80CLK 31 → EC_RX/GPIO17
- 38 ON/OFF → ON/OFF 32 → ON_OFF/GPIO18
- 37 PWR_SUSP_LED → PWR_SUSP_LED 34 → PWR_LED#/GPIO19
- 37 WLAN_LED# → WLAN_LED# 36 → NUMLED#/GPIO1A

GPO
- EC_RSMRST#/GPXO03 → EC_RSMRST# 100 → EC_RSMRST# 15
- EC_LID_OUT#/GPXO04 → EC_LID_OUT# 101 → EC_LID_OUT# 14
- EC_ON/GPXO05 → EC_ON 102 → EC_ON 38
- EC_SWI#/GPXO06 → EC_SWI# 103 → EC_SW# 15
- ICH_PWROK/GPXO07 → EC_PWROK 104 → EC_PWROK 15,38
- BKOFF#/GPXO08 → BKOFF# 105 → BKOFF# 28
- WL_OFF#/GPXO09 → WL_OFF# 106 → WL_OFF# 34
- GPXO10 107
- GPXO11 108

GPI
- PM_SLP_S4#/GPXID1 → PM_SLP_S4# 110 → PM_SLP_S4# 15
- ENBKL/GPXID2 → ENBKL 112 → ENBKL 16
- GPXID3 → EAPD 114 → EAPD 39
- GPXID4 → SUS_PWR_DN_ACK 115 → SUS_PWR_DN_ACK 15
- GPXID5 → SUSP# 116 → SUSP# 38,42,46,48
- GPXID6 → PBTN_OUT# 117 → PBTN_OUT# 5,15,21
- GPXID7 → EC_PME# 118 → EC_PME# 32

XCLK1 / XCLK0 — EC_CRY1 122 / EC_CRY2 123

V18R 124 — C539 4.7U_0805_10V4Z

L33 FBMA-L11-160808-800LMT_0603 — 20mil — ECAGND

C491 0.01U_0402_16V7K

ENBKL — R425 100K_0402_5%

32.768KHZ_12.5PF_Q13MC14610002

EC_CRY1 — C536 15P_0402_50V8J — X1 (OSC, OSC, NC, NC) — C537 15P_0402_50V8J — EC_CRY2

C490 100P_0402_50V8J
BATT_TEMP — C489 100P_0402_50V8J
BATT_OVP — C534 100P_0402_50V8J
ACIN 100P_0402_50V8J

SM010015410 300ma 80ohm@100mhz DCR 0.3

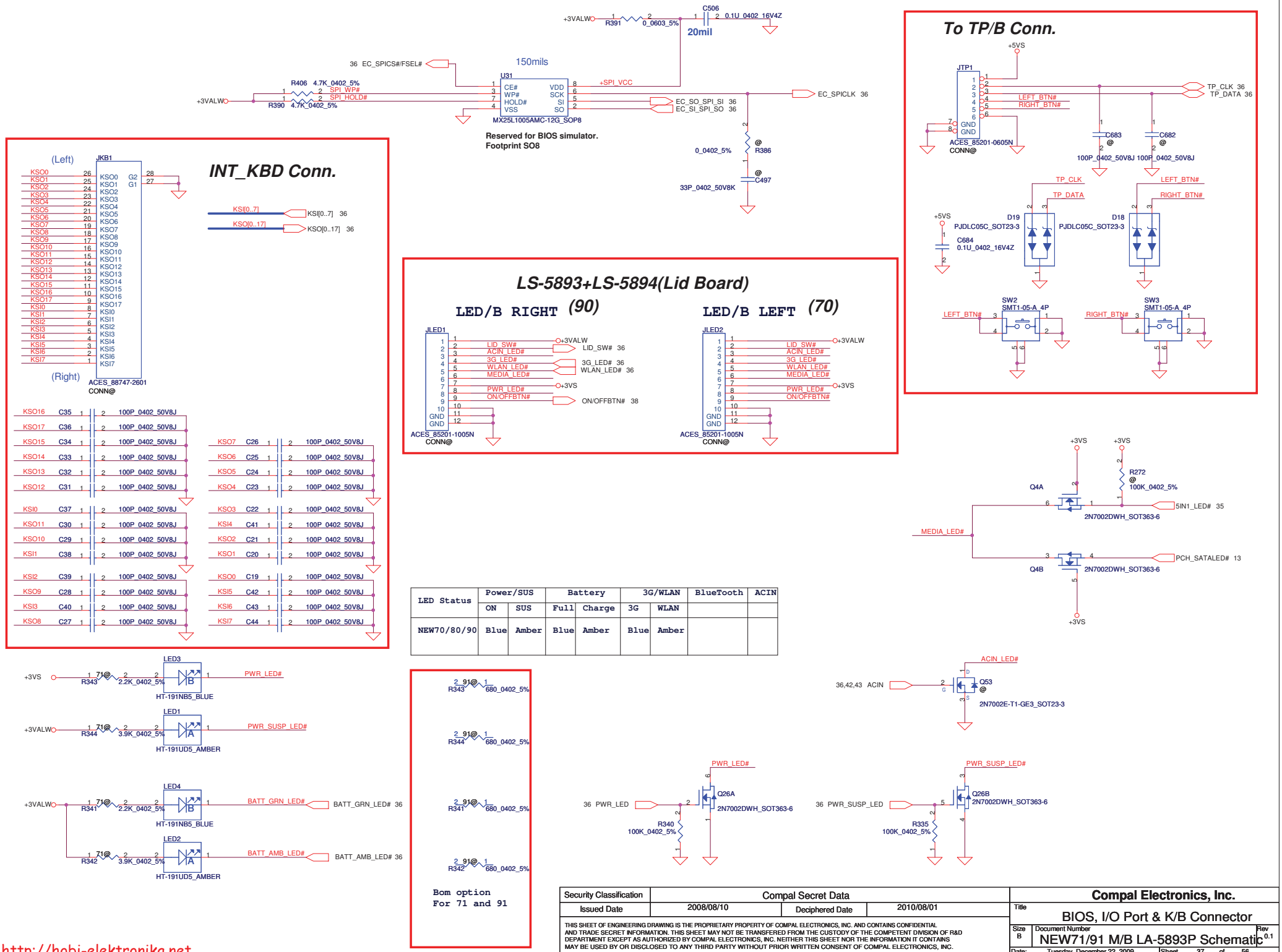
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 36 of 56



LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

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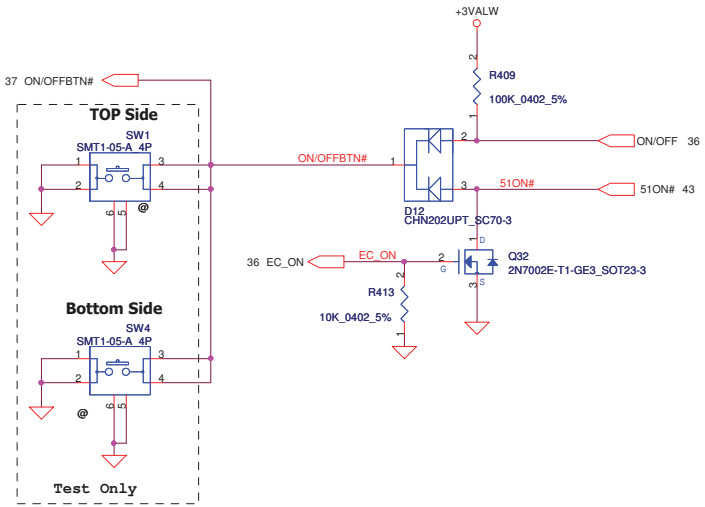
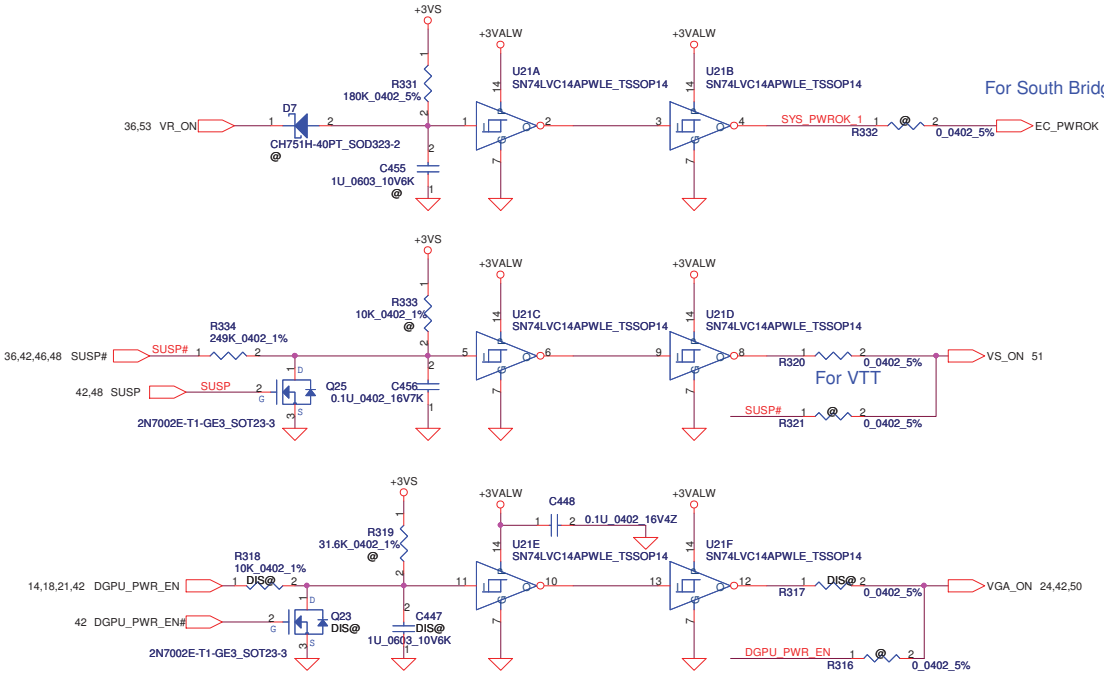
Power Button

ON/OFF switch



Power ON Circuit



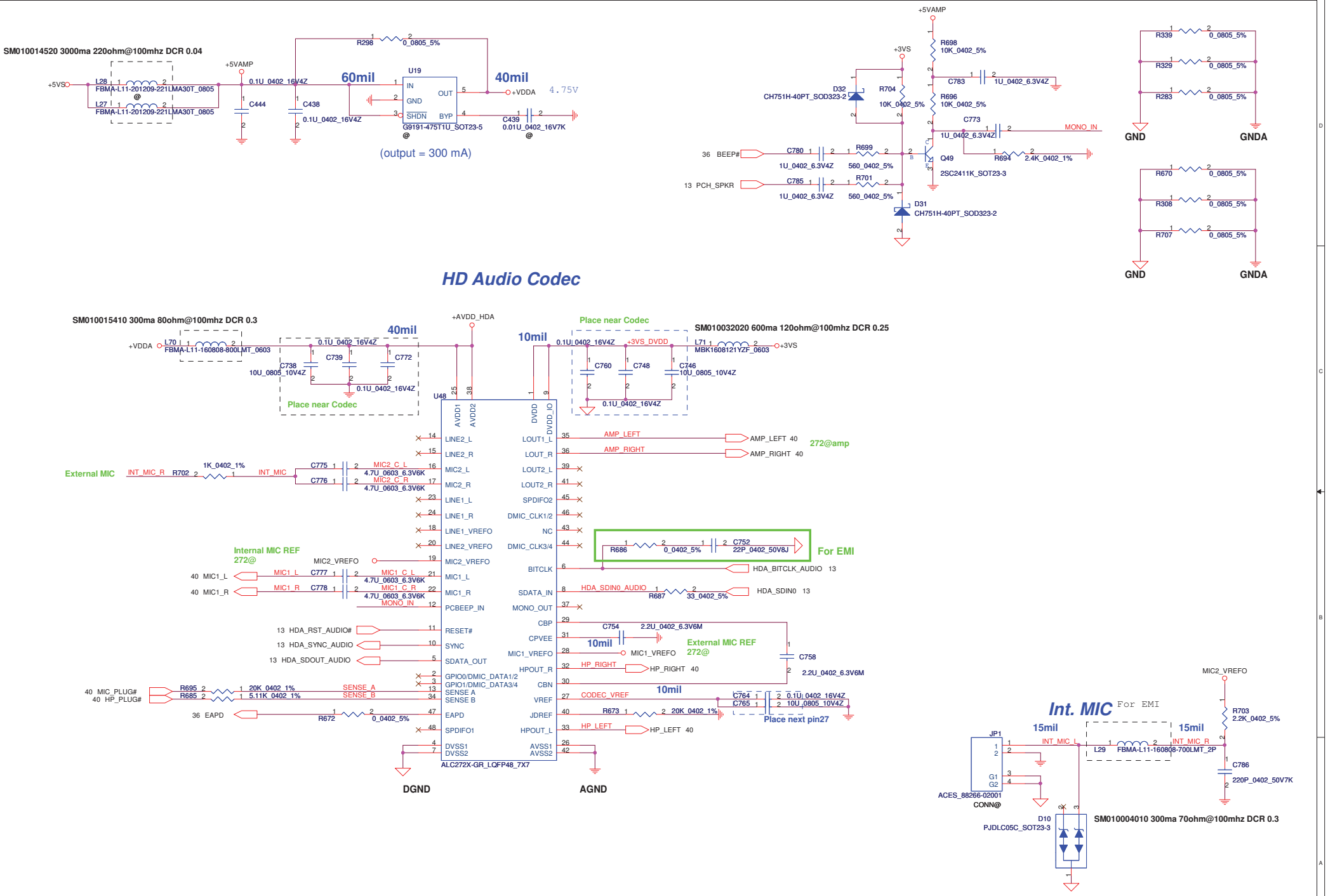
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Power OK

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 38 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

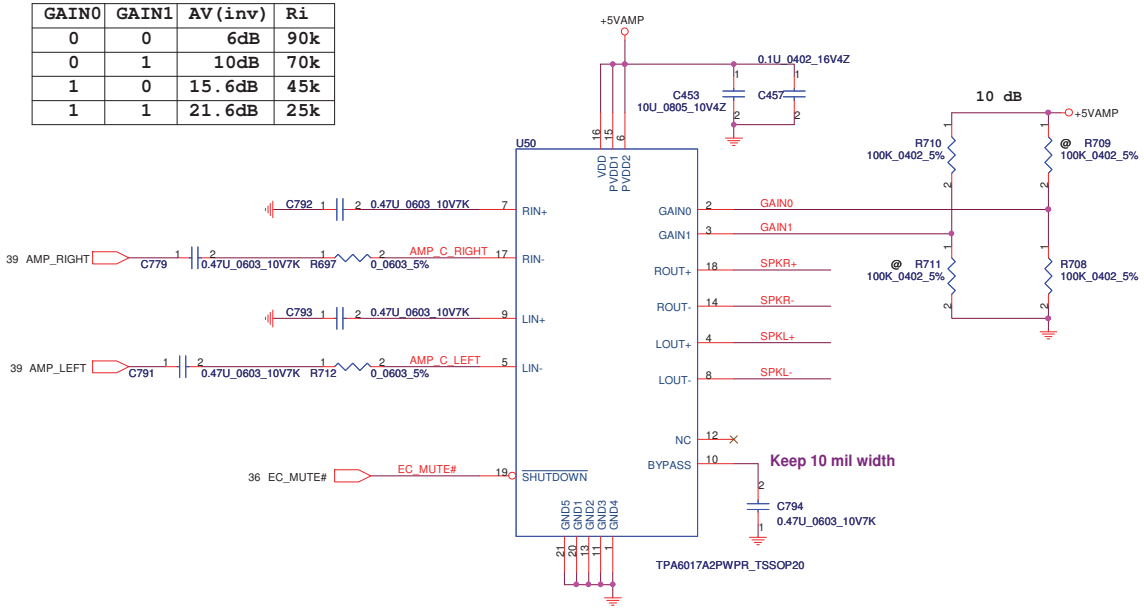
Compal Electronics, Inc.

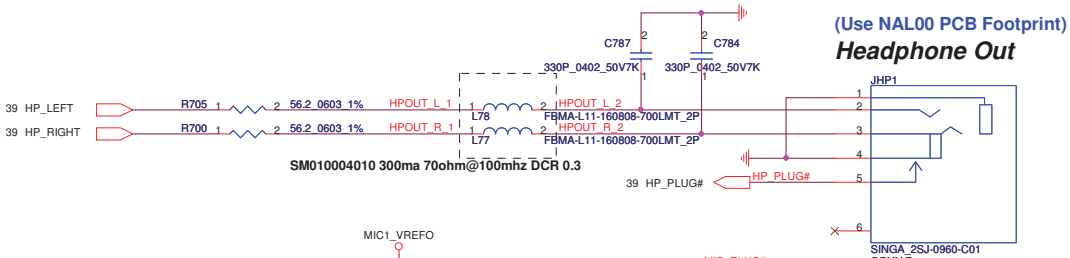
Title: HD Audio Codec ALC272X

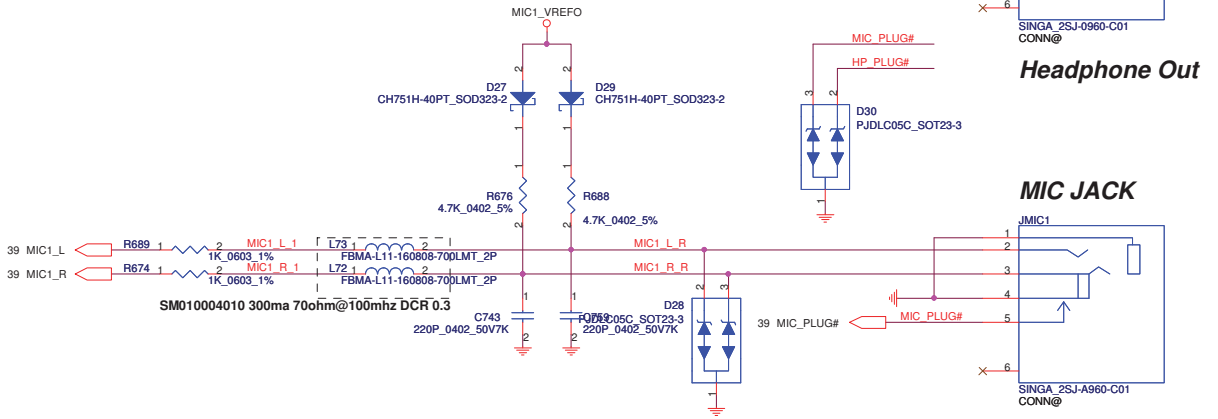
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

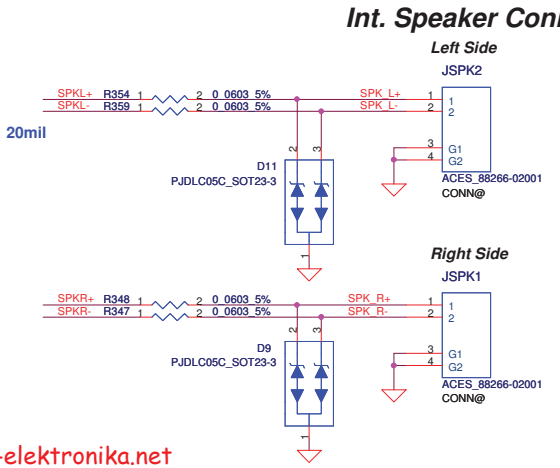
Date: Tuesday, December 22, 2009 | Sheet 39 of 56

GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k









Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

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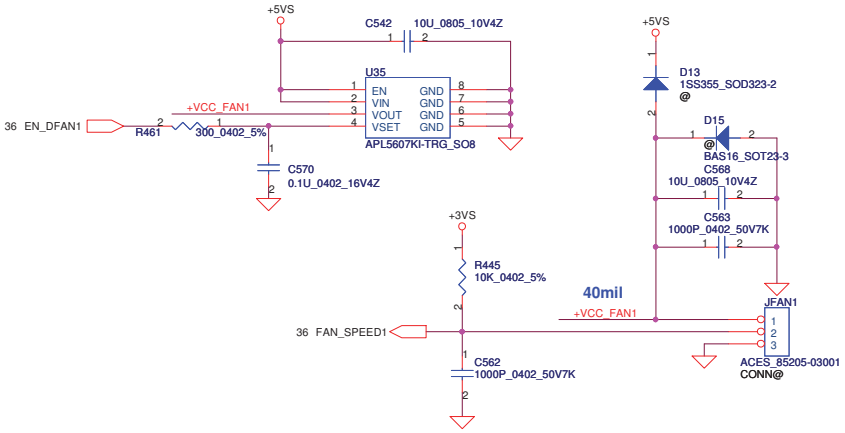
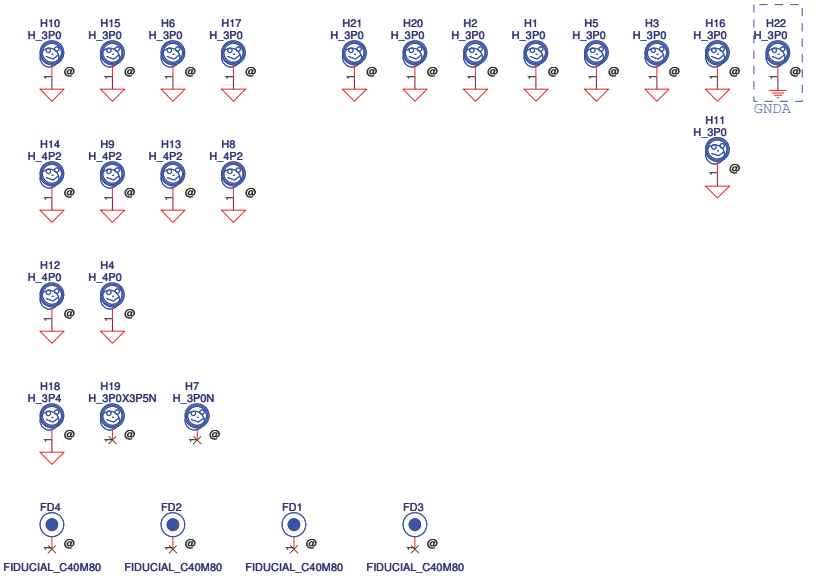
FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

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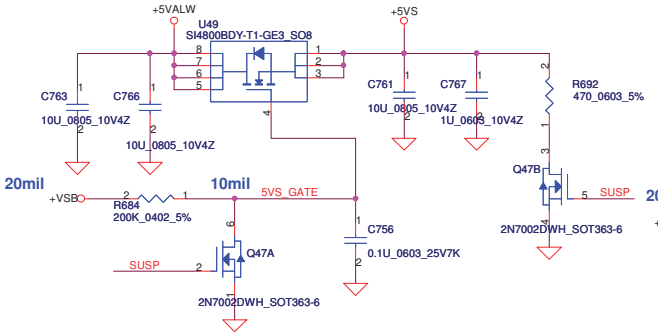
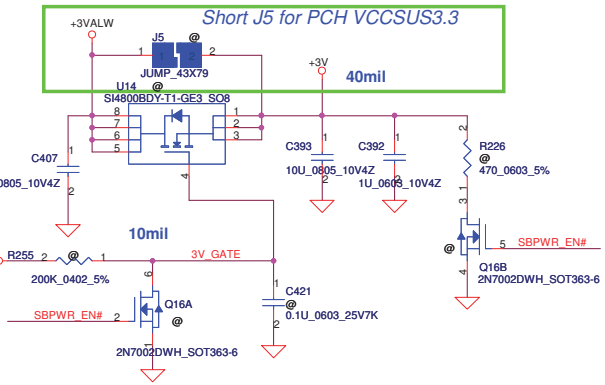
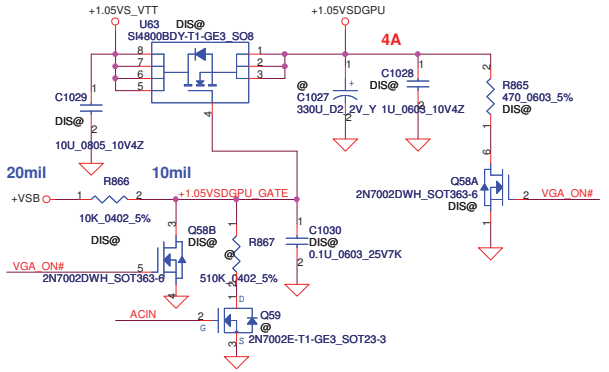
+5VALW TO +5VS



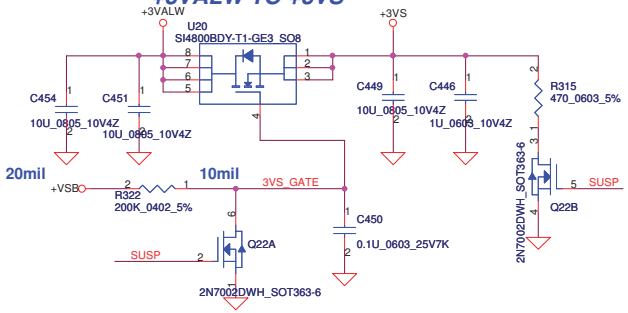
+3VALW TO +3V(PCH AUX Power)



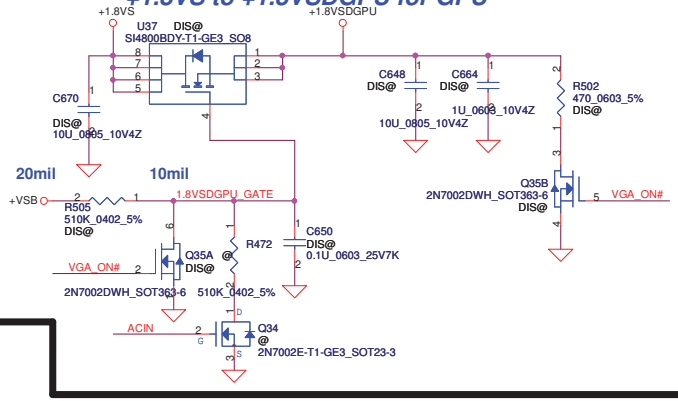
+1.05VS_VTT to +1.05VSDGPU for GPU

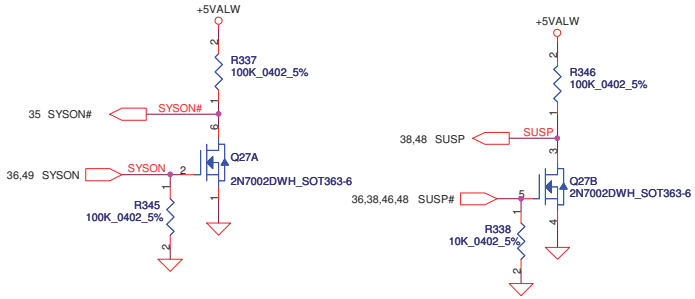


+3VALW TO +3VS

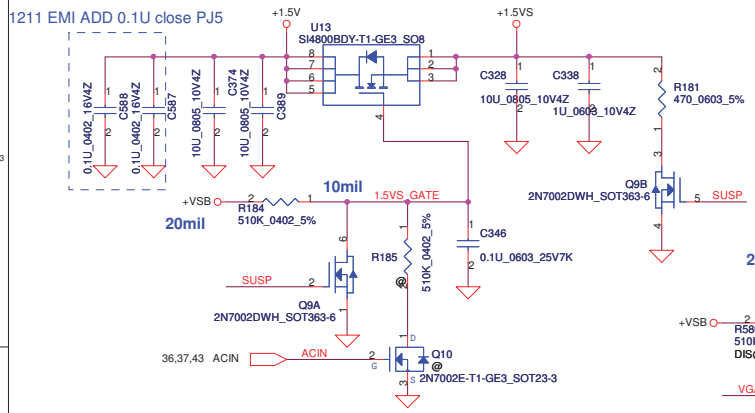


+1.8VS to +1.8VSDGPU for GPU

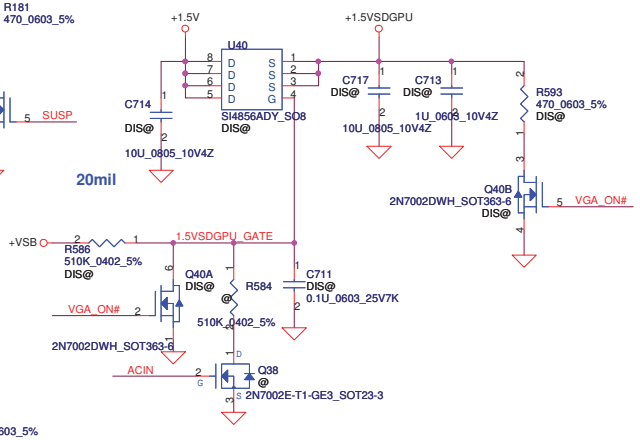


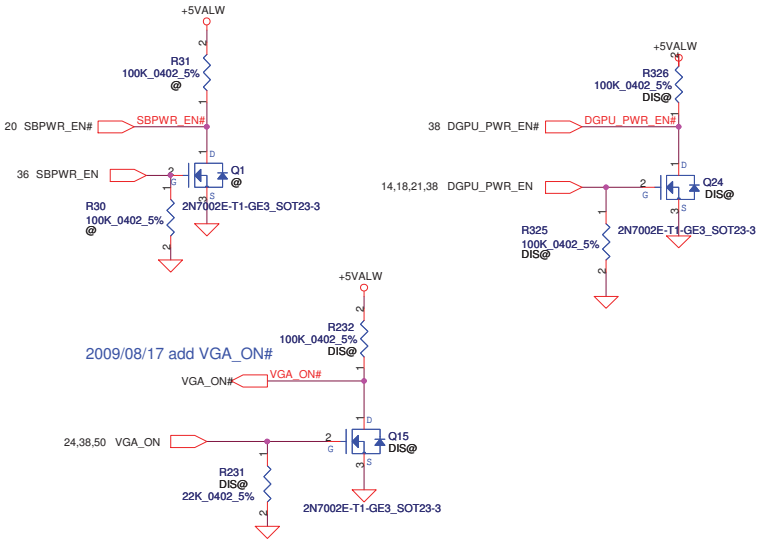


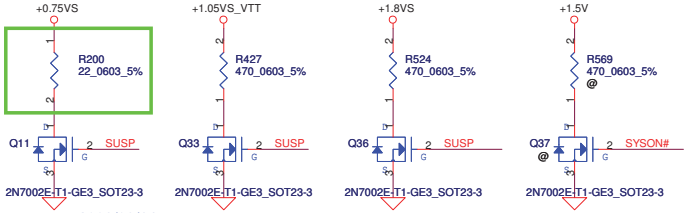
+1.5V to +1.5VS



+1.5V to +1.5VSDGPU for GPU







2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
1.5VS power change

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

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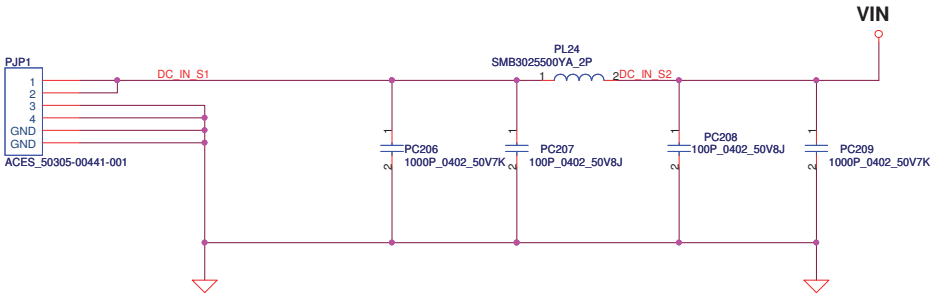
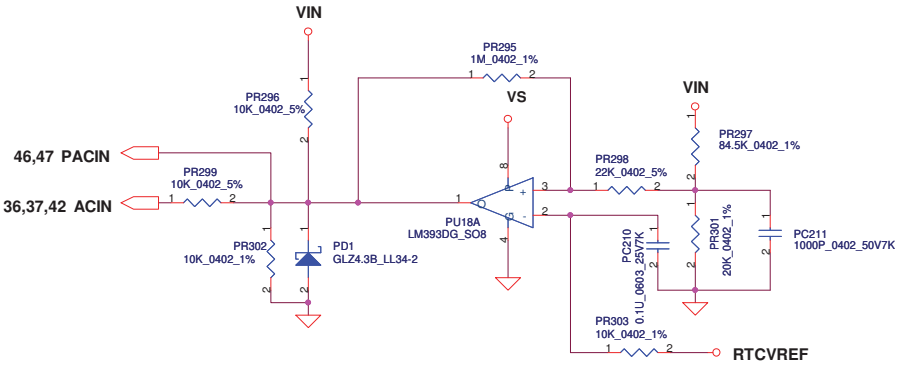
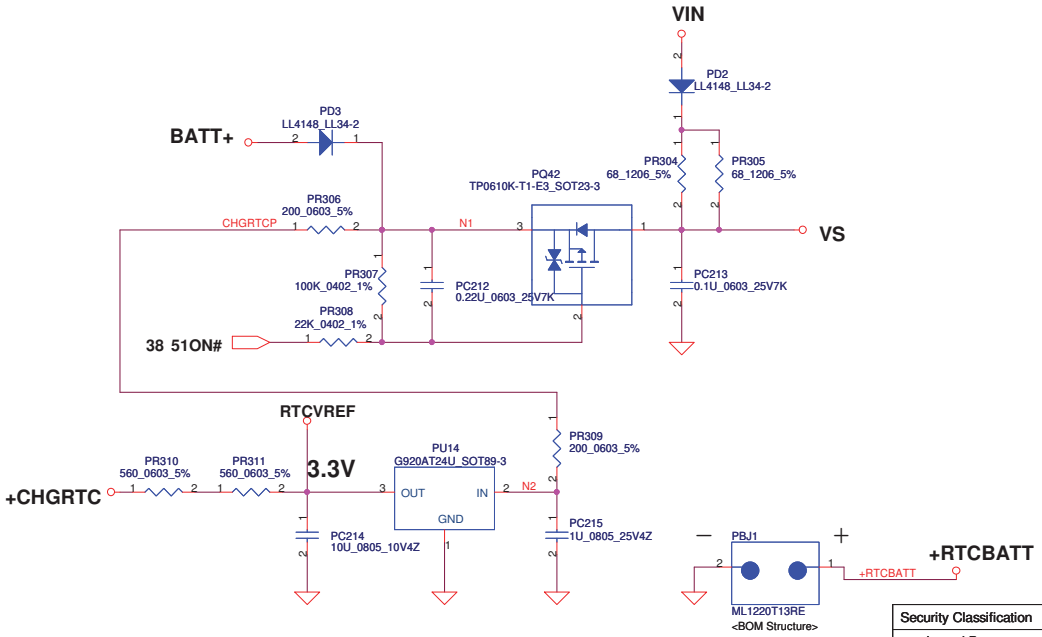
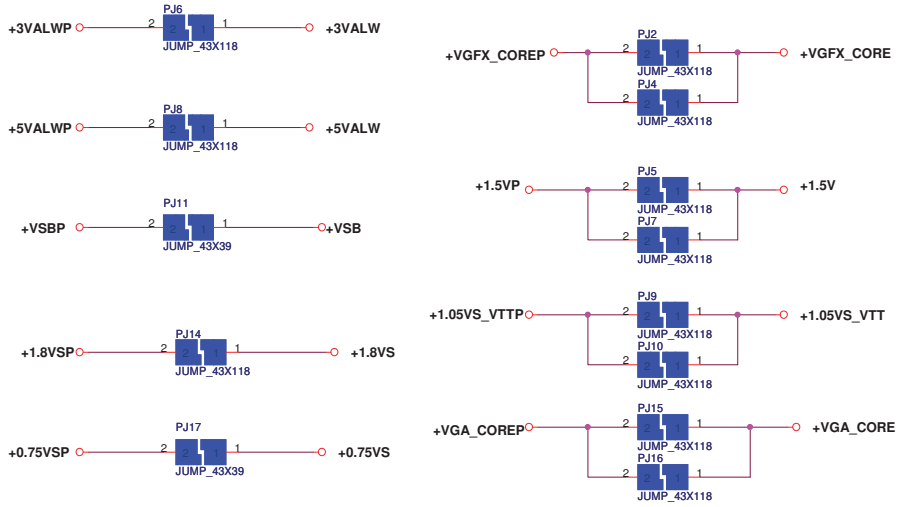




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





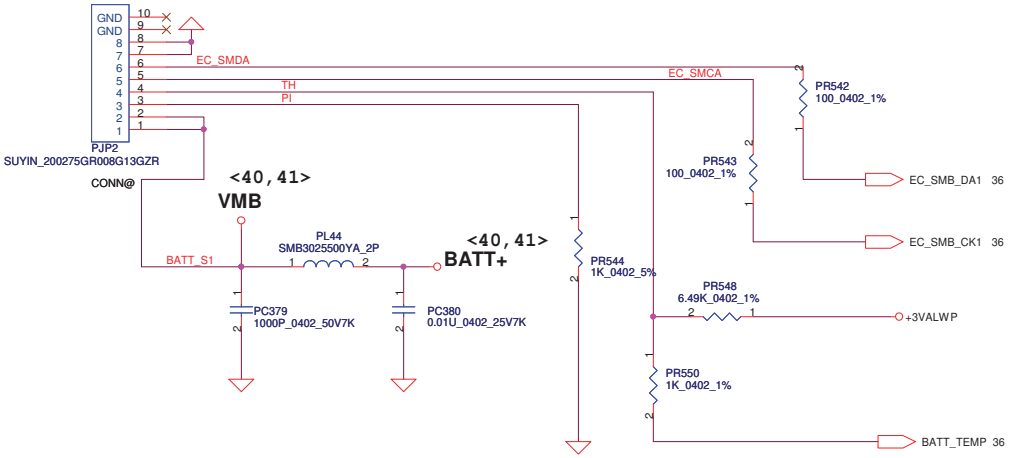
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

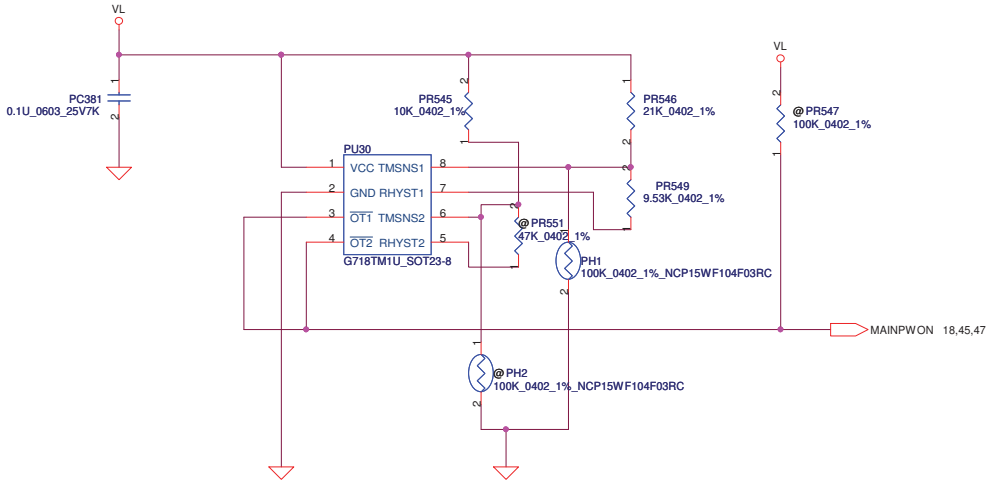
Size	Document Number	Rev
Custom	NEW71	0.1

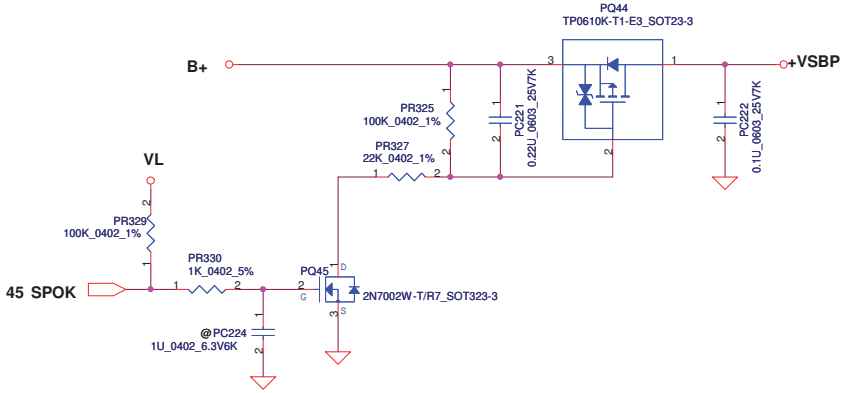
Date: Tuesday, December 22, 2009 | Sheet 43 of 56



PH1 under CPU botten side :

CPU thermal protection at 92 degree C





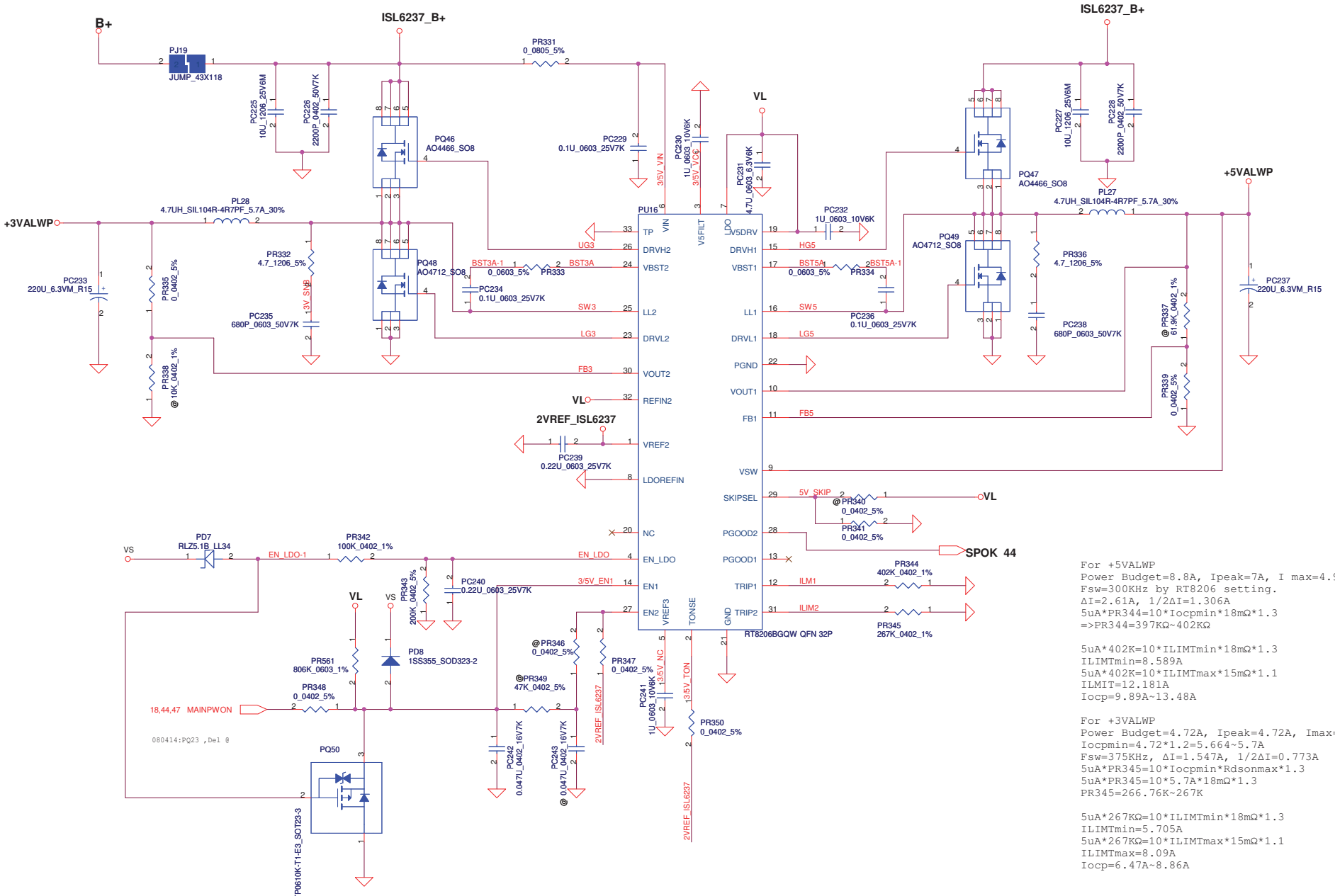
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 44 of 56



For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=300KHz by RT8206 setting.
ΔI=2.61A, 1/2ΔI=1.306A
5uA*PR344=10*Iocpmin*18mΩ*1.3
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.3
ILIMTmin=8.589A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=9.89A~13.48A

For +3VALWP
Power Budget=4.72A, Ipeak=4.72A, Imax=4A
Iocpmin=4.72*1.2=5.664~5.7A
Fsw=375KHz, ΔI=1.547A, 1/2ΔI=0.773A
5uA*PR345=10*Iocpmin*Rdsonmax*1.3
5uA*PR345=10*5.7A*18mΩ*1.3
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ*1.3
ILIMTmin=5.705A
5uA*267KΩ=10*ILIMTmax*15mΩ*1.1
ILIMTmax=8.09A
Iocp=6.47A~8.86A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: 3VALW/5VALW

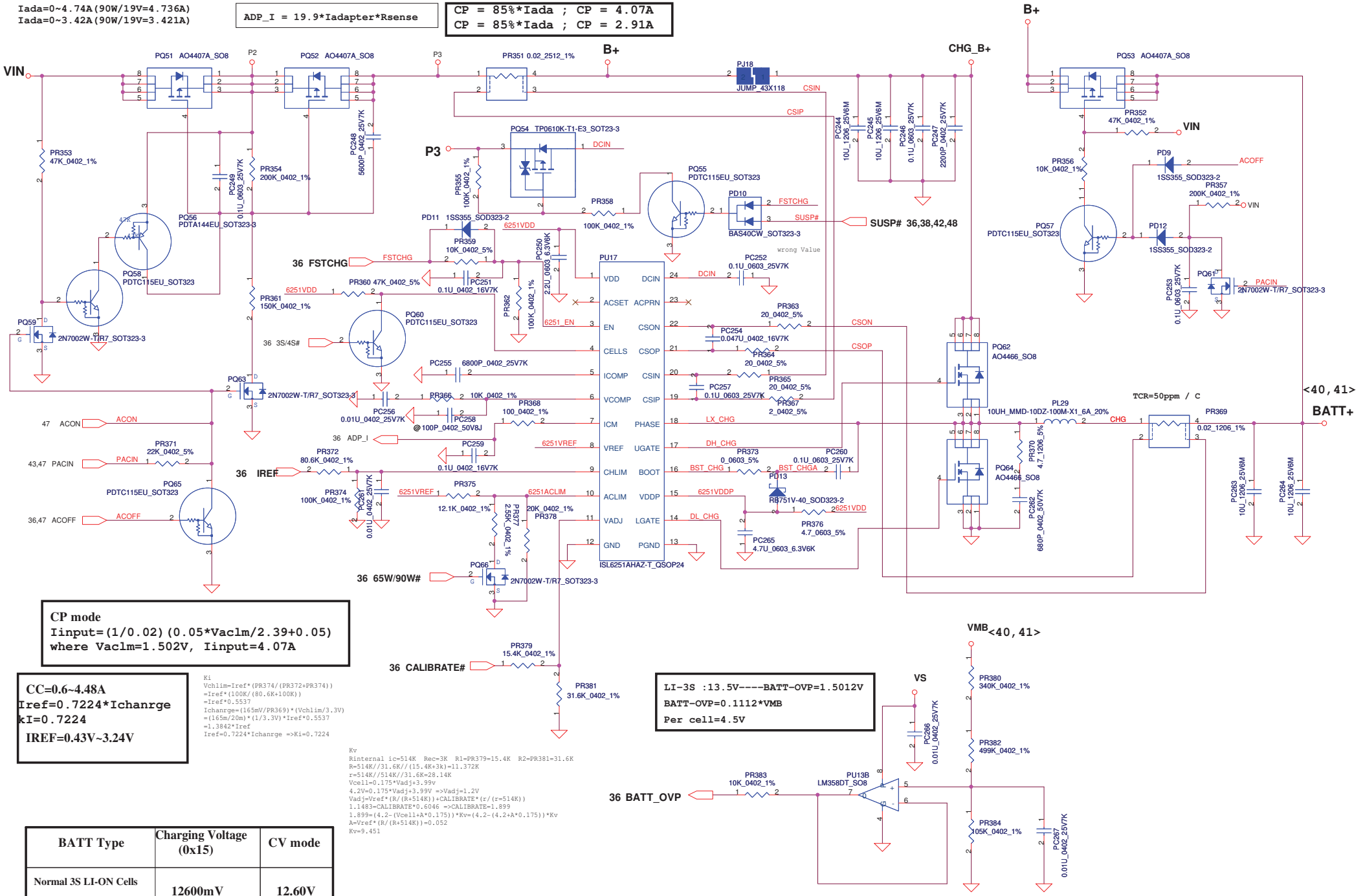
Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 45 of 56

Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.183=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NEW71 | Rev: 0.1

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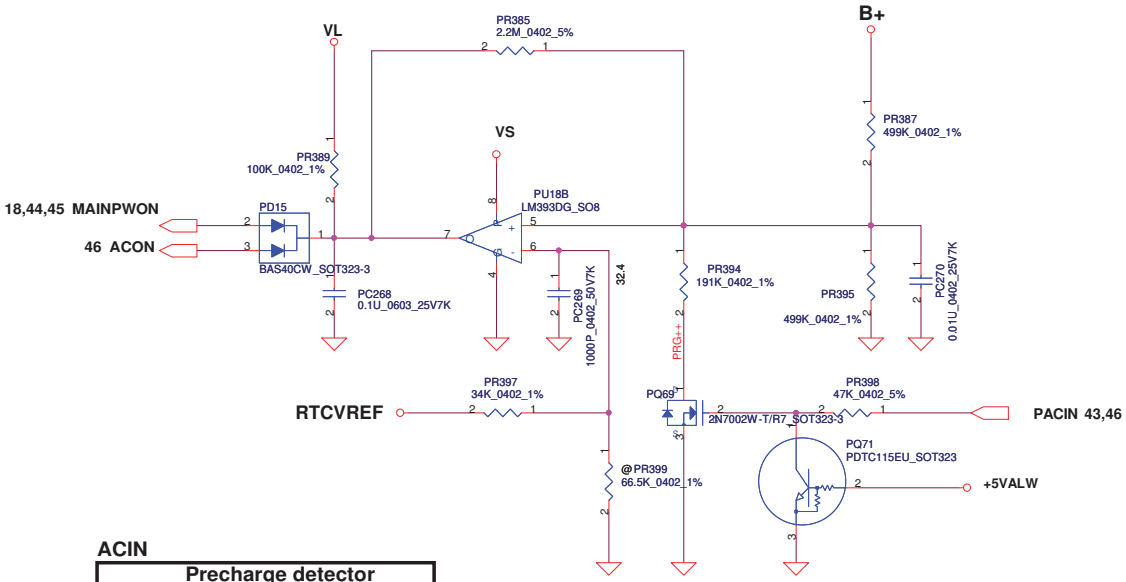

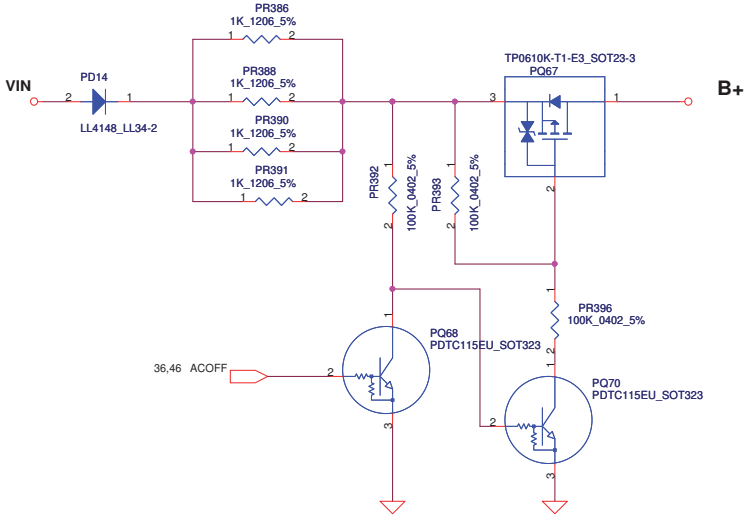

ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **PRECHARGE**

Size	Document Number	Rev
Custom	NEW71	0.1

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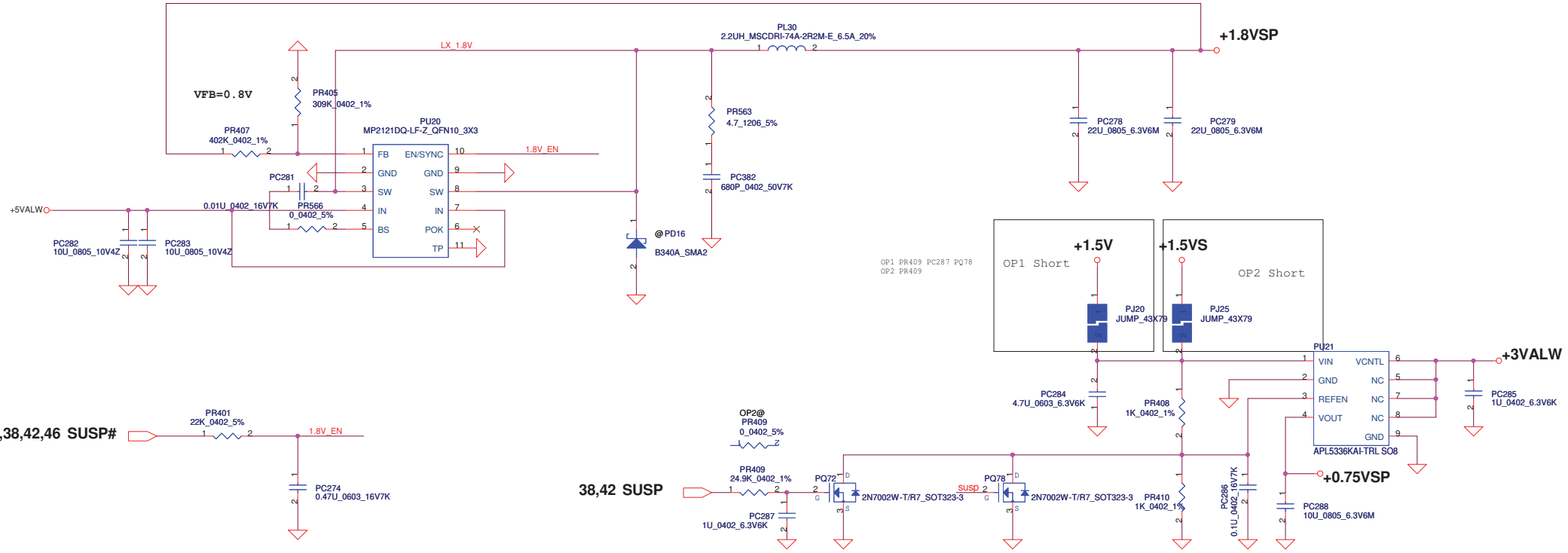


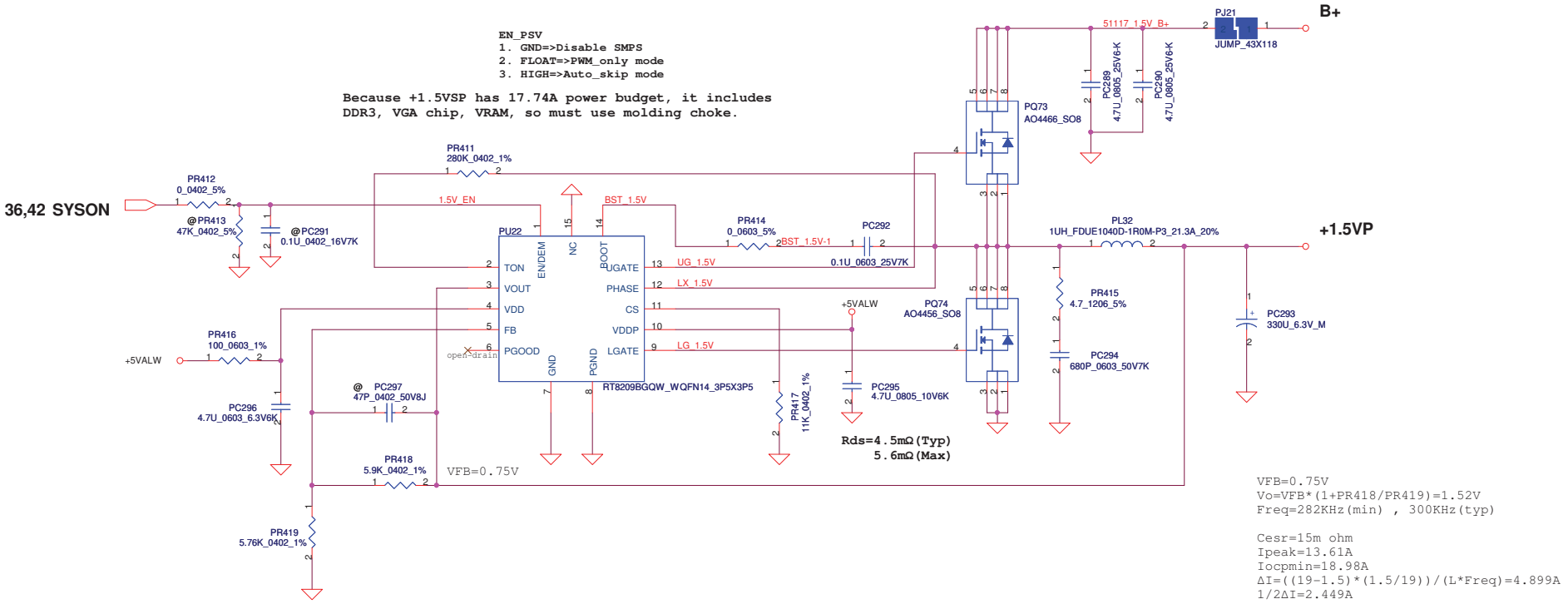
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 48 of 56



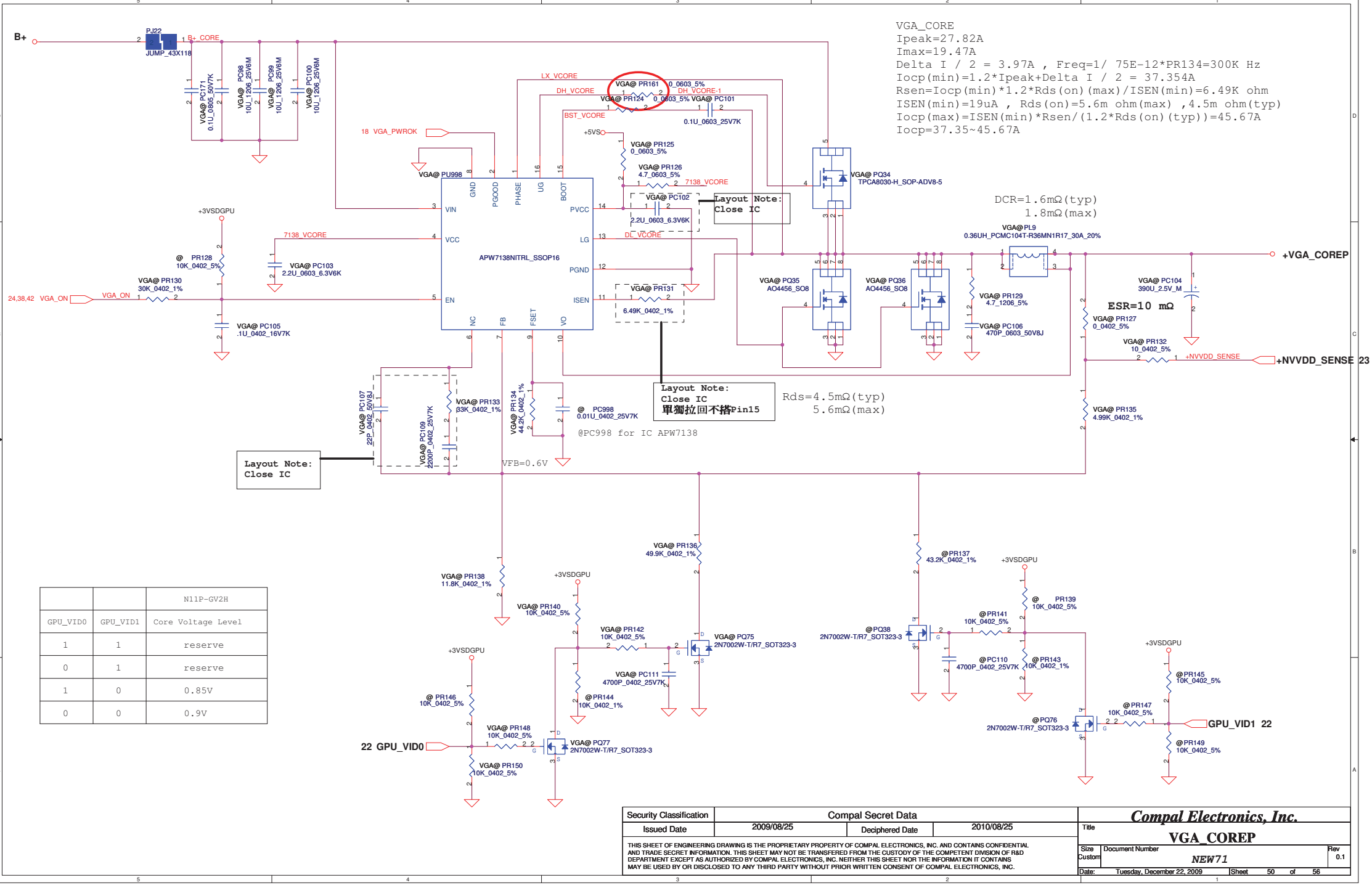
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **1.5VP**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 49 of 56



		N11P-GV2H
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	reserve
0	1	reserve
1	0	0.85V
0	0	0.9V

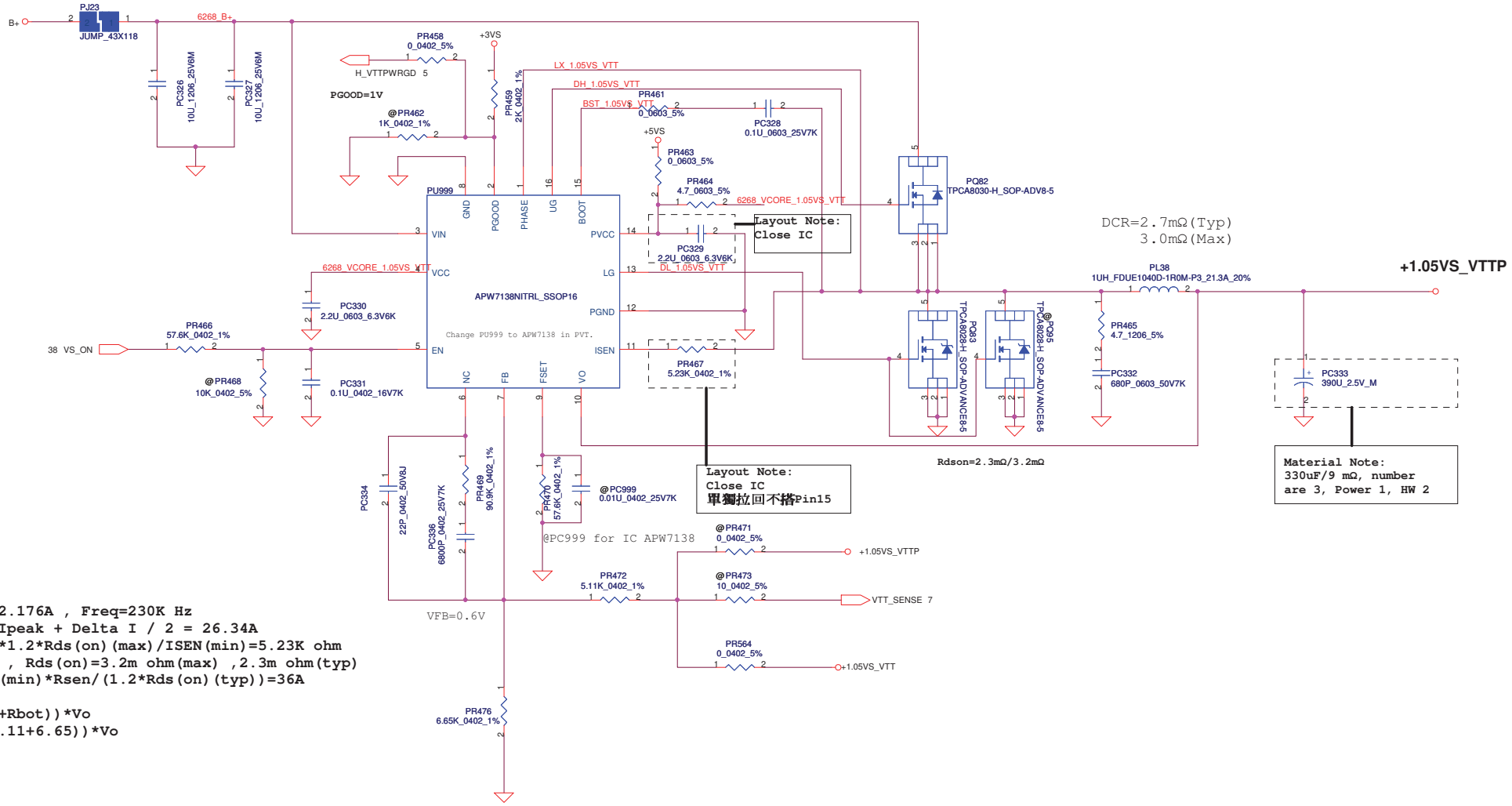
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: VGA_COREP

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 50 of 56



+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: +1.05VS_VTTP

Size: Custom | Document Number: NEW71 | Rev: 0.1

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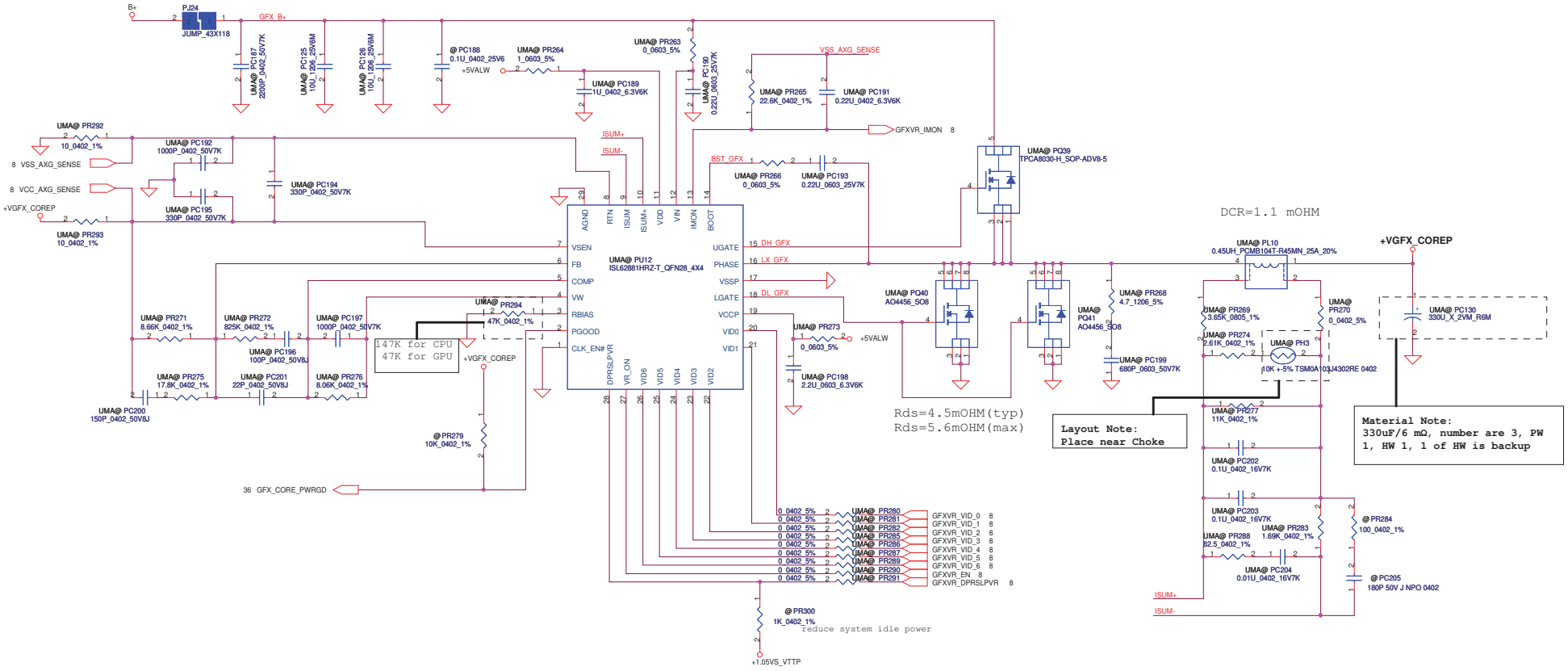
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: GFX_COREP

Size	Document Number	Rev
C	NEW71	0.1

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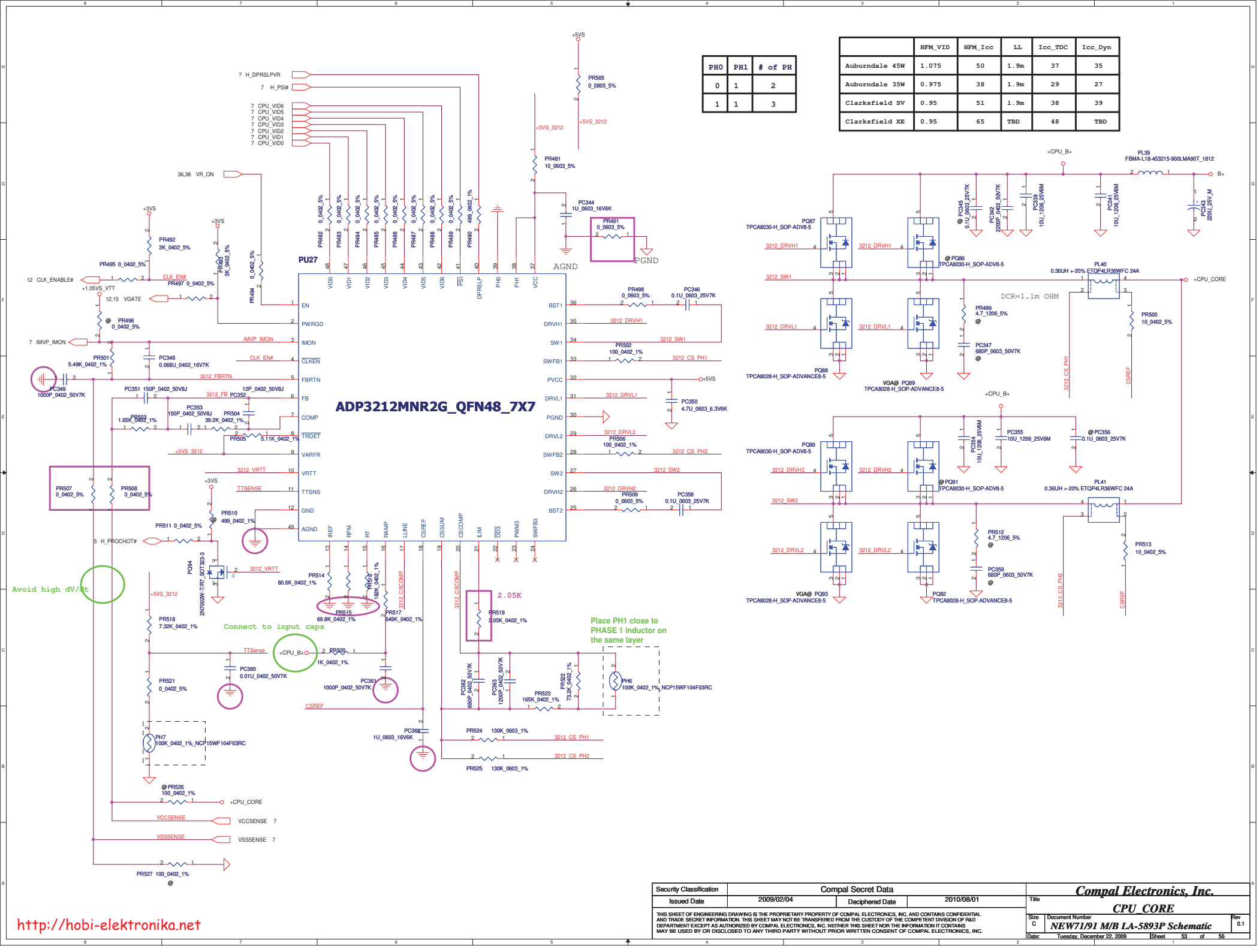

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

Compal Electronics, Inc.	
Title	CPU_CORE
Size: C	Document Number: NEW71/91 M/B LA-5893P Schematic
Rev: 0.1	
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12 13	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004O80(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280. Delete PC273 SE075103K80 PC275 SE000000I10	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC272 SE107475K80, PC271 SE107105M80 Delete PR401 and PR403 SD028220280, PC274 SE026474K80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Change PR196 from SD034442280 to SD034365280. Change PL14 from SL200000V00 to SH000005680	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK SO8)	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

Compal Electronics, Inc.
Title: PIR (PWR)
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A -->Modify item

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PIR (HW)

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5891P Schematic	0.1

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PCB

ZZZ

LA-5893P REV0 M/B

ZZZ1

X76198BOL21

ALT. GROUP PARTS 1G SAM

ZZZ2

X76198BOL22

ALT. GROUP PARTS 1G HYN

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Option Component

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 0.1

Date: Monday, December 21, 2009 | Sheet 56 of 56