

# Compal Confidential

## KBLG0 Schematics Document

**AMD Puma : Griffin Processor with RS780MN/SB700/M92-M2 XT**

**Tigris : Caspian Processor with RS880M/SB710/M92-M2 XT**

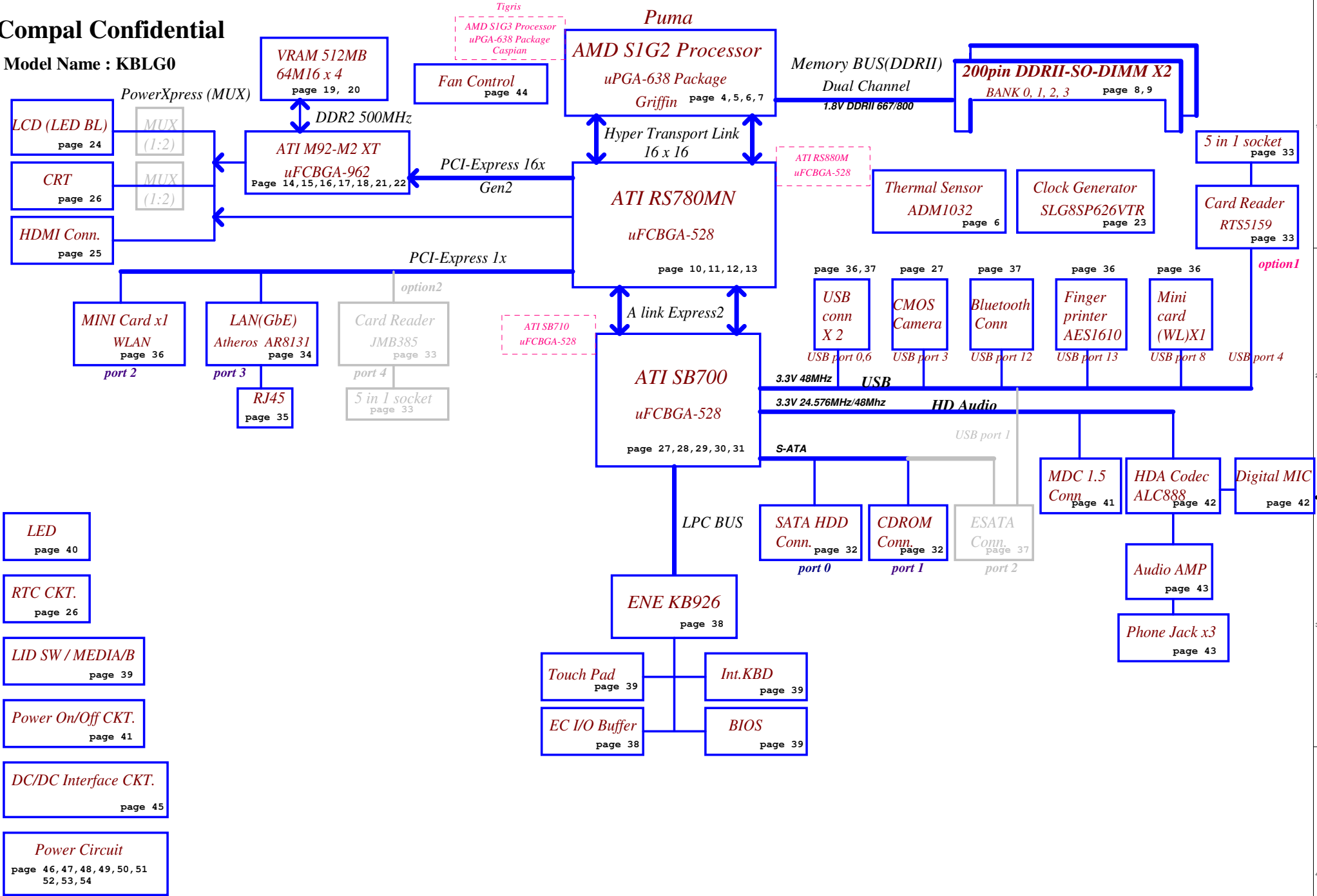
**2009-03-11**

**REV: 1.0**

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# Compal Confidential

Model Name : KBLG0



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Smart Battery	0001 011X b	16H	98H
ADI ADM1032 (CPU)	1001 100X b		9AH
GMT G781-1 (GPU)	1001 101X b		9CH
SB-Temp Sensor			

## EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

## SB700

### SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8P626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

## SB700

### SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

## BTO Option Table

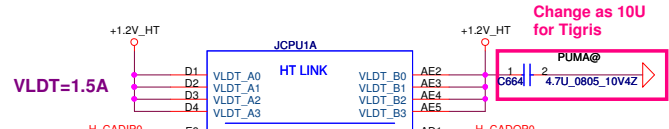
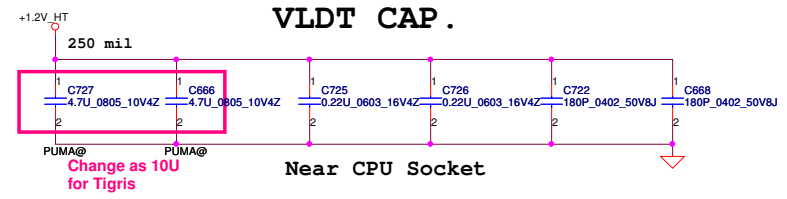
BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

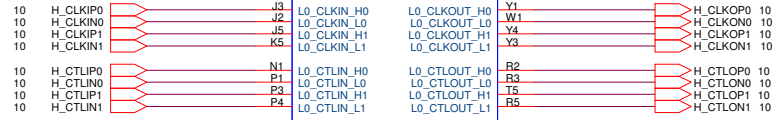
	KB926					
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

	KB926	
	PX_GPIO1_SB	
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)	
IGP only mode	X	
PowerXpress mode	H : Enable	

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H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	L1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	E5	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

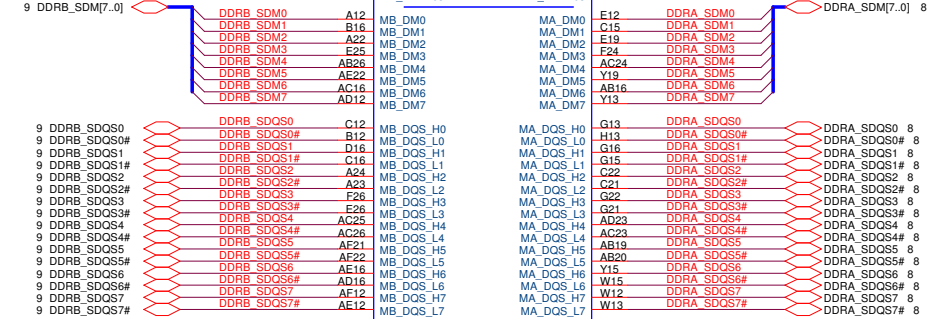
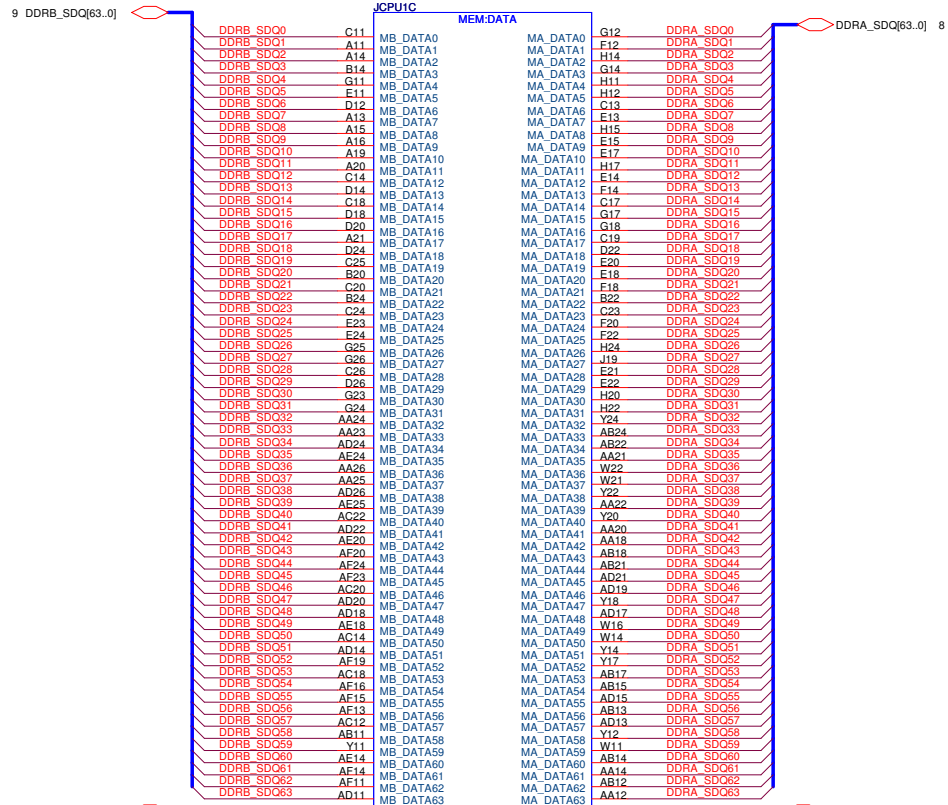
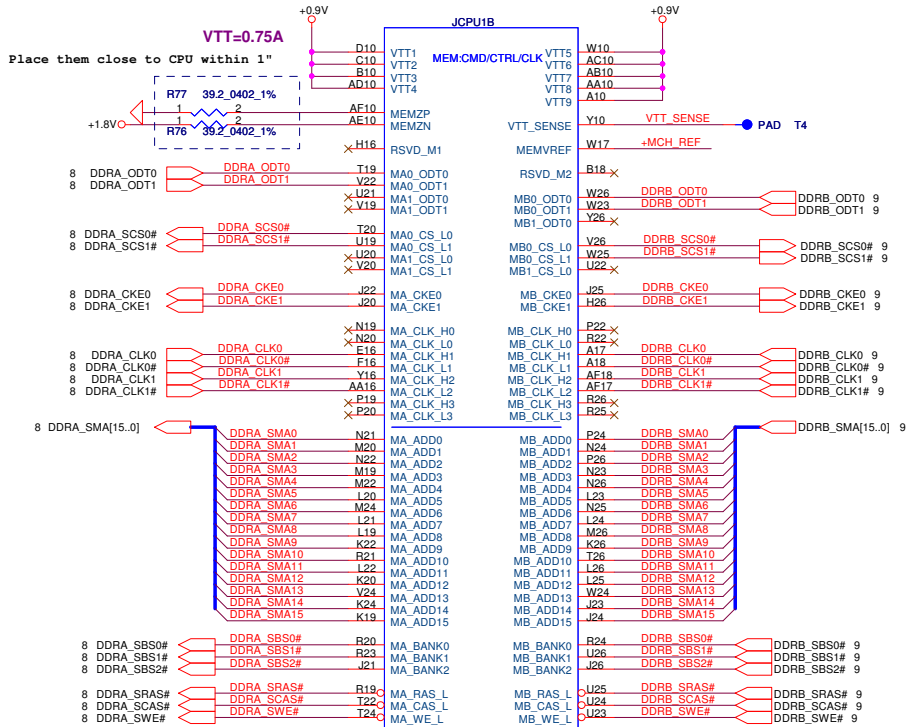
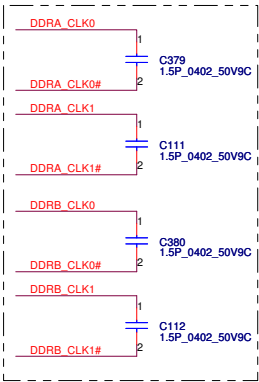
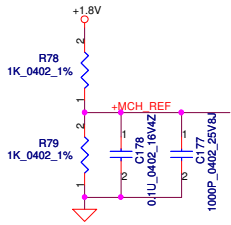


6090022100G\_B conn@

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# Processor DDR2 Memory Interface

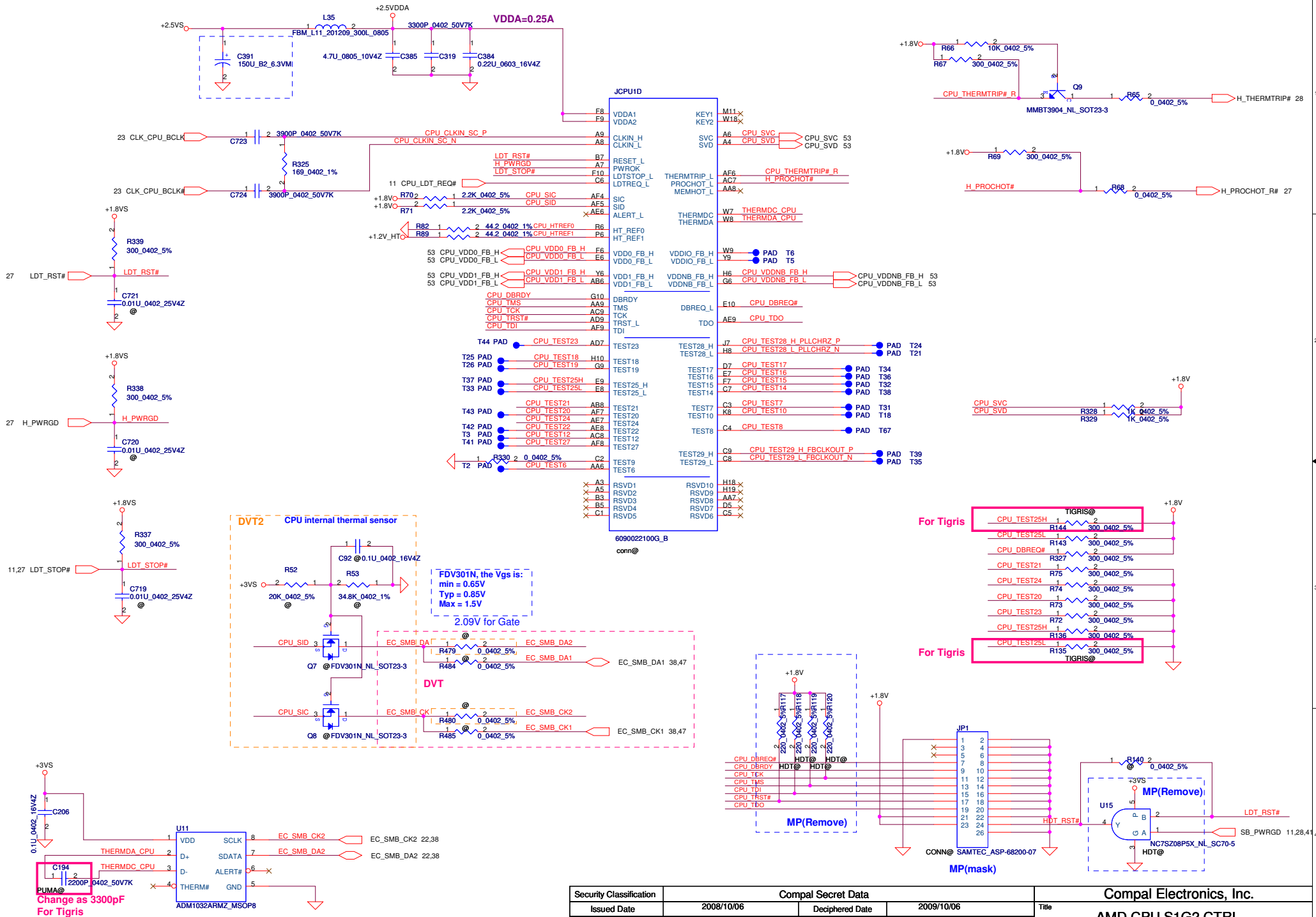
**PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH**



6090022100G\_B  
conn@

6090022100G\_B  
conn@

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Customer		<b>KBLG0 LA-4921P</b>		Rev 0.1
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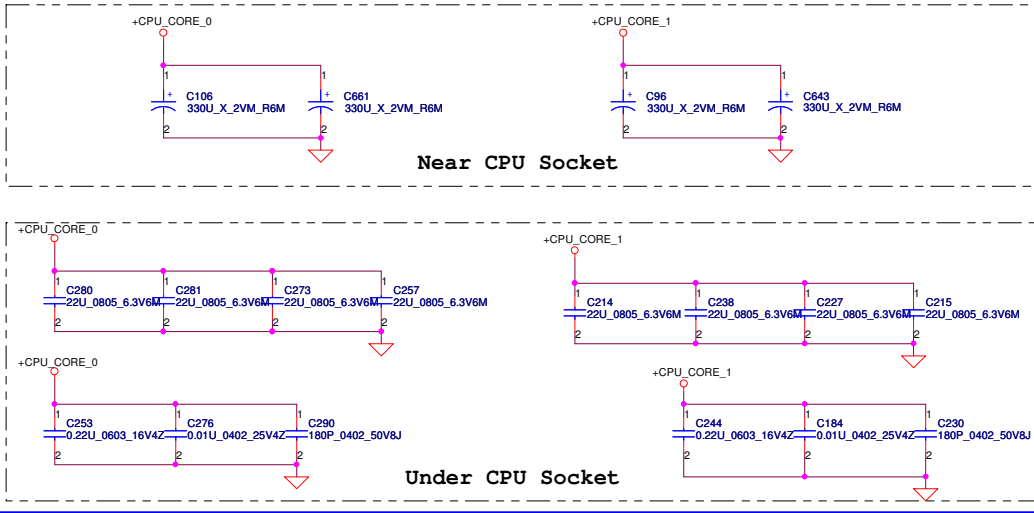


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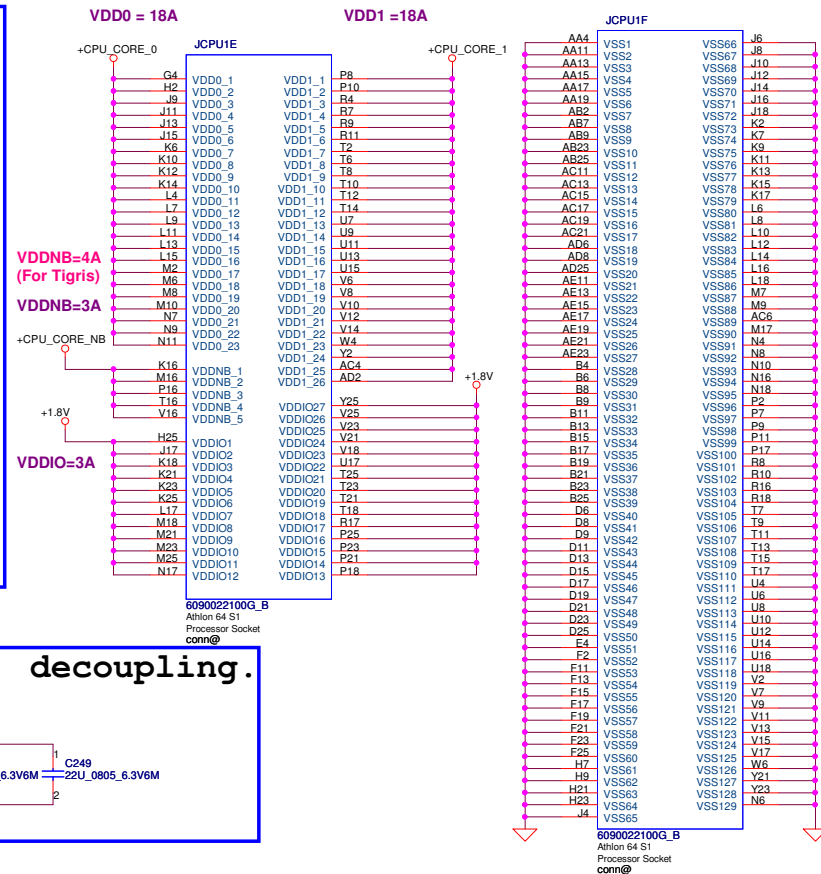
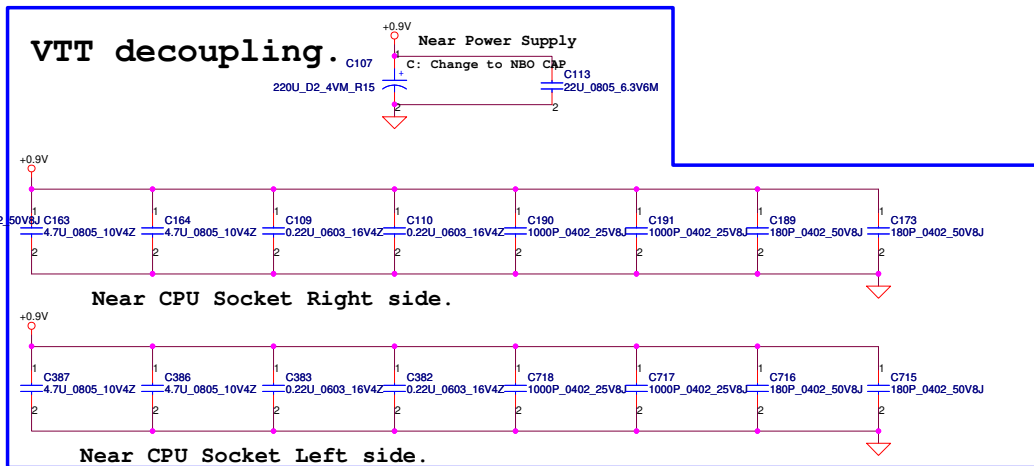
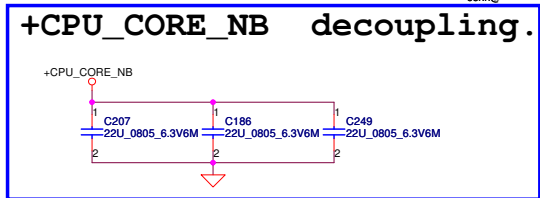
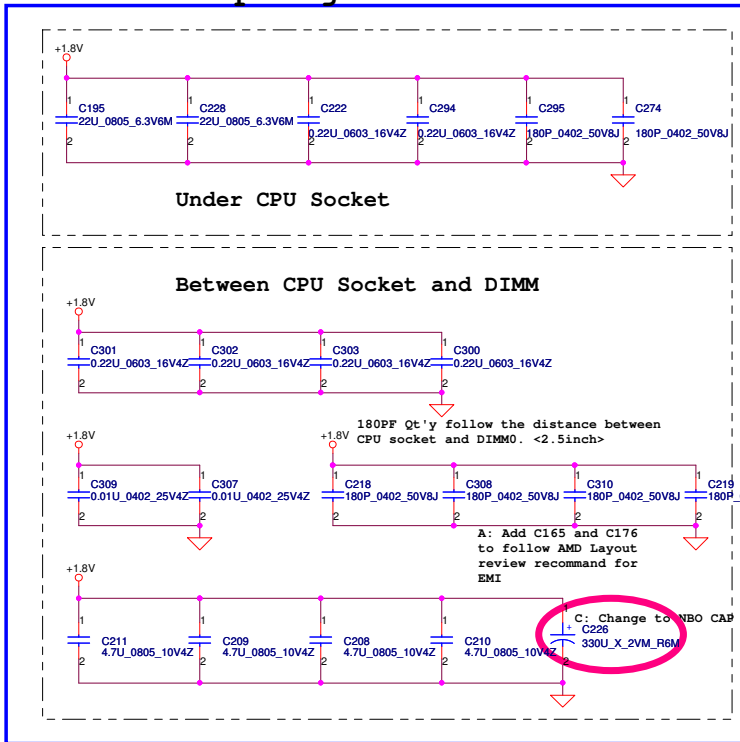
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AMD CPU S1G2 CTRL		
Title	Size	Document Number
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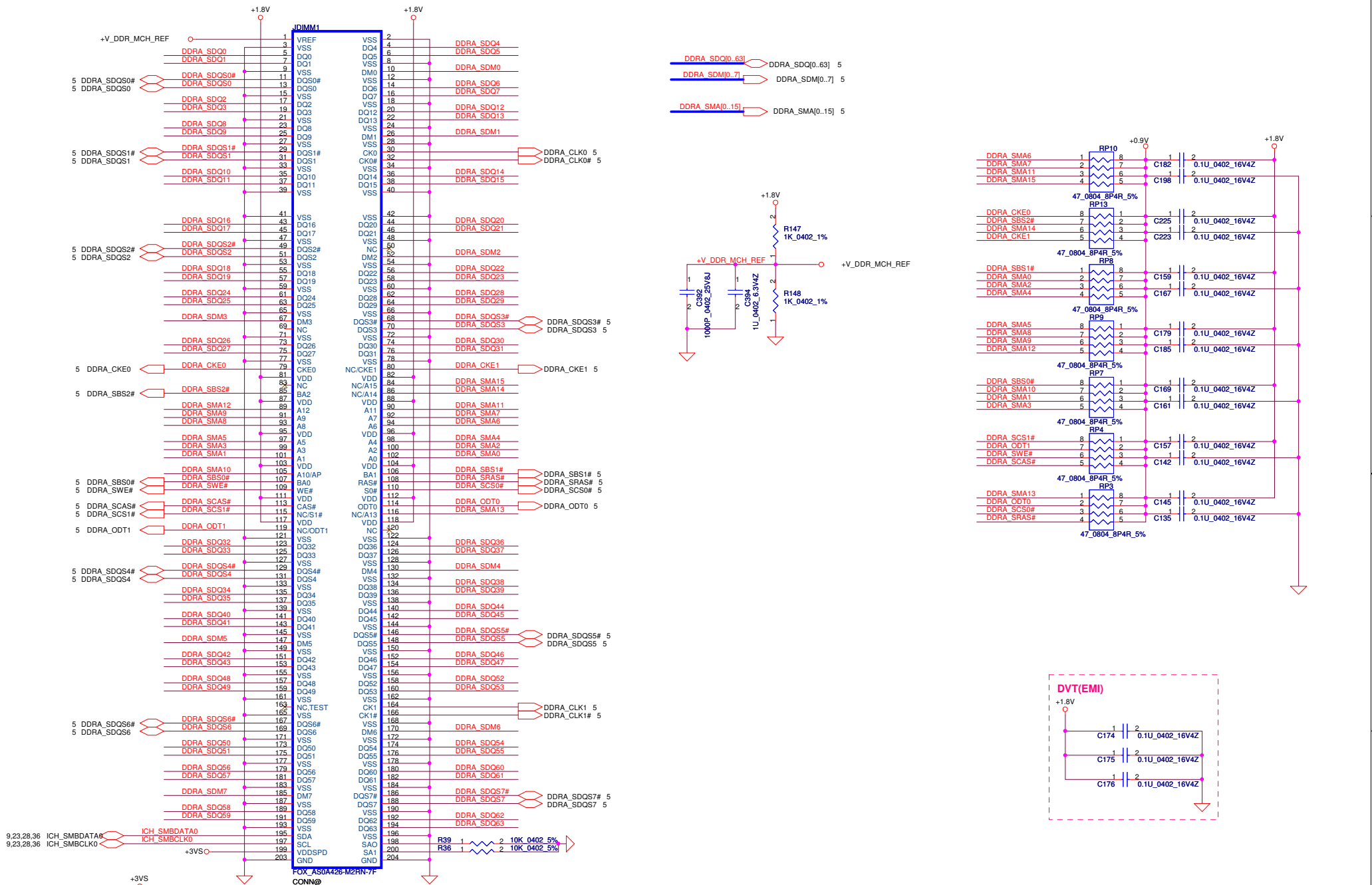
# VDD (+CPU\_CORE) decoupling.



# VDDIO decoupling.



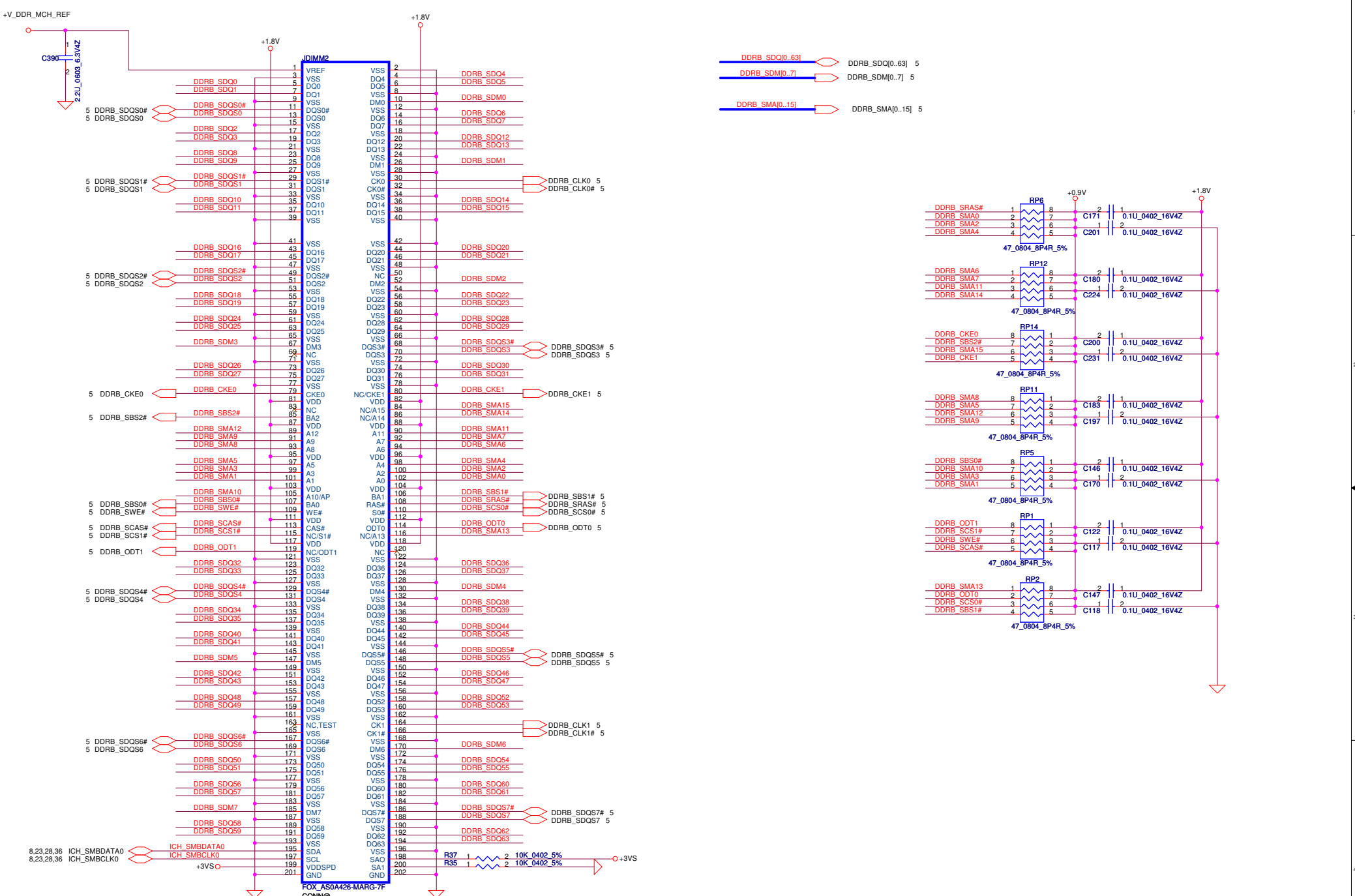
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DIMM1 REV H:5.2mm (BOT)

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**DIMM2 REV H:9.2mm (BOT)**

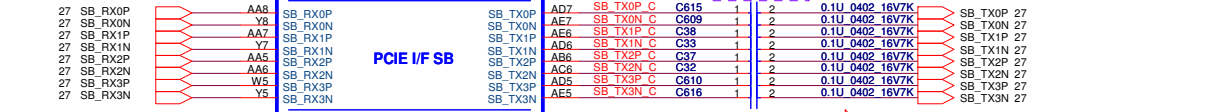
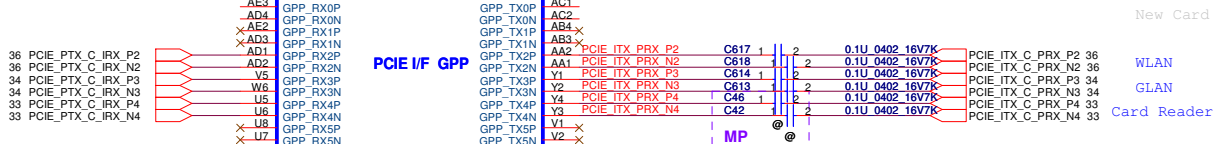
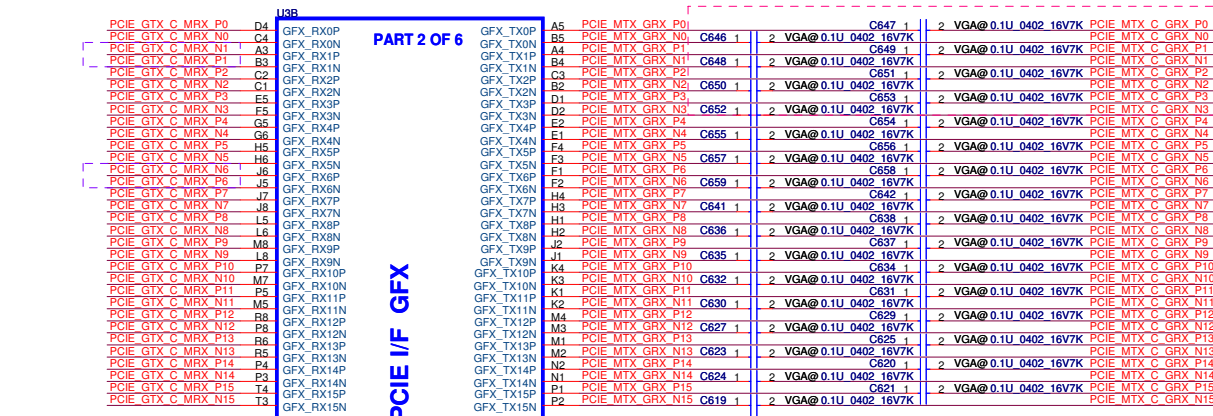
Security Classification		Compal Secret Data		Title	
Issued Date		2008/10/06	Deciphered Date	2009/10/06	DDRIR SO-DIMM 2
8,23,28,36 ICH_SMBDATA0		8,23,28,36 ICH_SMBCLK0		KBLG0 LA-4921P	
+3VS		R37 1 2 10K 0402 5%		Date: Thursday, February 19, 2009	
R35 1 2 10K 0402 5%		FOX_AS0A426-MARG-7F		Sheet 9 of 57	
CONN		Compal Electronics, Inc.		Rev 0.1	

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14 PCIE GTX\_C\_MRX\_P0..15] PCIE GTX\_C\_MRX\_P0..15] PCIE GTX\_C\_MRX\_N0..15] PCIE GTX\_C\_MRX\_N0..15]

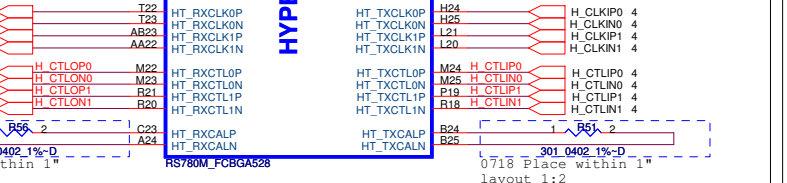
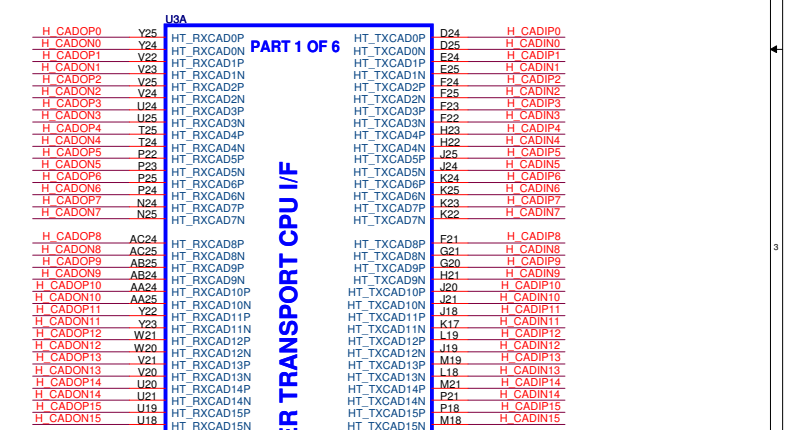
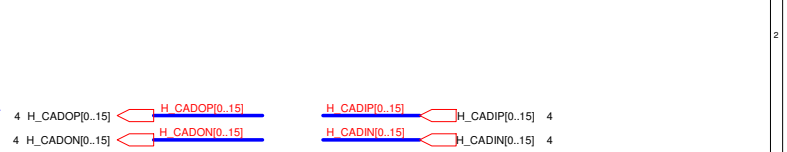
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PCIE\_MTX\_GRX\_N0..3] PCIE\_MTX\_GRX\_N0..3] 25 PCIE\_MTX\_GRX\_P0..3] PCIE\_MTX\_GRX\_P0..3] 25



**RS780M Display Port Support (muxed on GFX)**

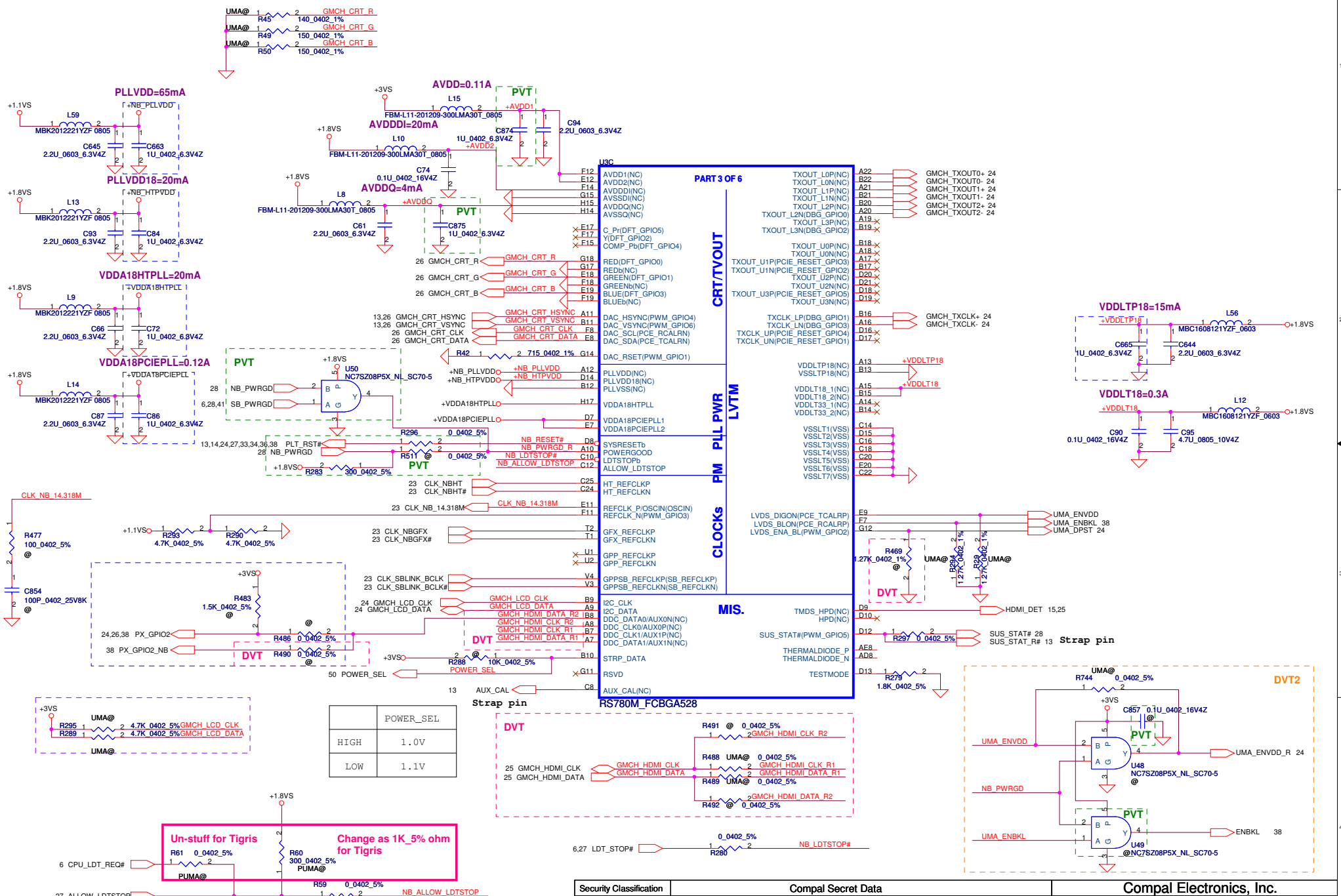
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



SA00002DR30 S IC 216-0674026 A13 RS780MN FCBGA 0FA

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				<b>RS780-HT/PCIE</b>
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For RS780M A13  
 RED: Connected to GND through two separate 140ohm 1% resistor

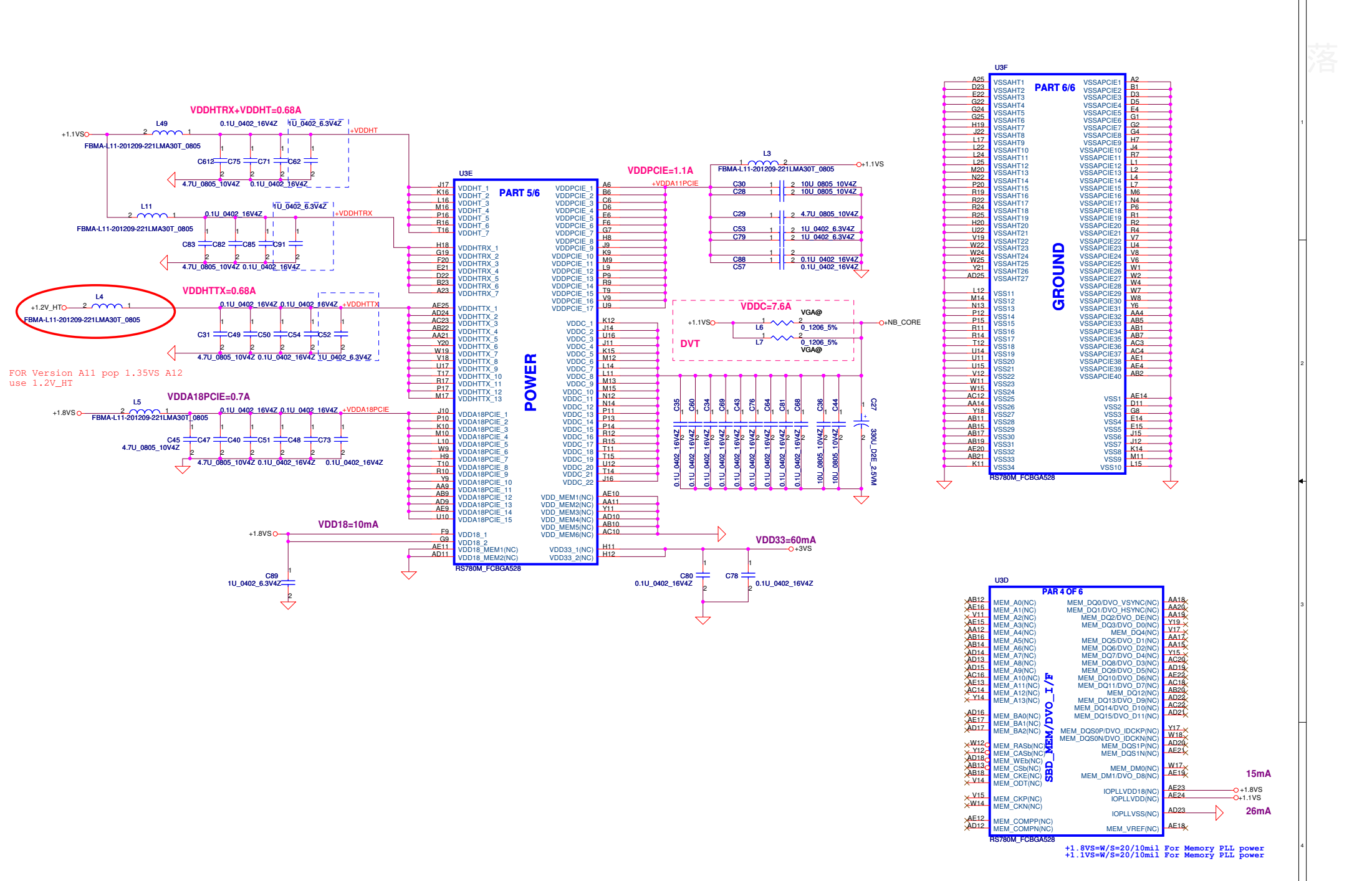


POWER_SEL	POWER_SEL
HIGH	1.0V
LOW	1.1V

Un-stuff for Tigris  
 R61 0.0402 5%  
 R60 300.0402 5%  
 PUMA@

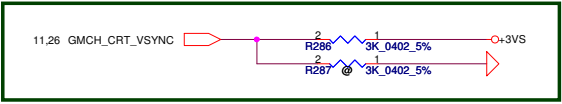
Change as 1K\_5% ohm for Tigris  
 R59 0.0402 5%  
 NB\_ALLOW\_LDTSTOP

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Issued Date	2008/10/06	Deciphered Date	2009/10/06	RS780 VEDIO/CLK GEN	
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Custom	KBLG0 LA-4921P	Date		Thursday, March 19, 2009	Sheet 11 of 57
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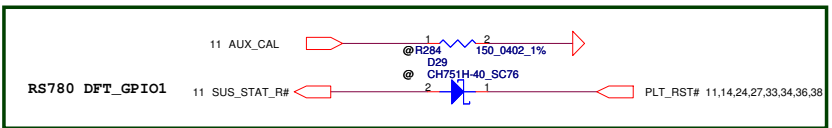
FOR Version All pop 1.35VS A12 use 1.2V\_HT

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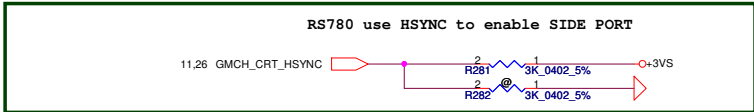
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO. (VSYNC)  
 1 : Disable (RS780)  
 0 : Enable (Rs780)



**DFT\_GPIO1:LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**RS780 use HSYNC to enable SIDE PORT**

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 0 : Enable (RS780)  
 1 : Disable(RS780)

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				Custom	KBLG0 LA-4921P
				Date:	Thursday, February 19, 2009
				Sheet	13 of 57
				Rev	0.1

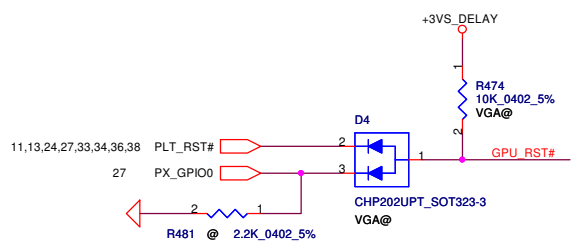
- 10 PCIE\_GTX\_C\_MRX\_P[0..15] <-- PCIE GTX C MRX P[0..15]
- 10 PCIE\_GTX\_C\_MRX\_N[0..15] <-- PCIE GTX C MRX N[0..15]
- 10 PCIE\_MTX\_C\_GRX\_P[0..15] <-- PCIE MTX C GRX P[0..15]
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**PCIE LANE REVERSAL**

**PCIE LANE REVERSAL**

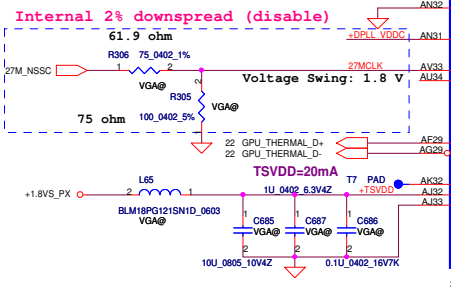
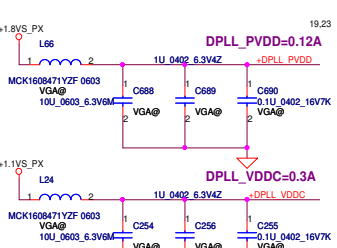
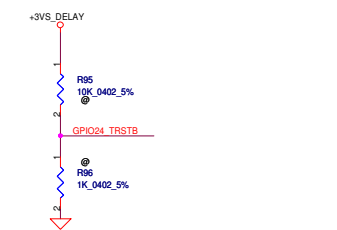
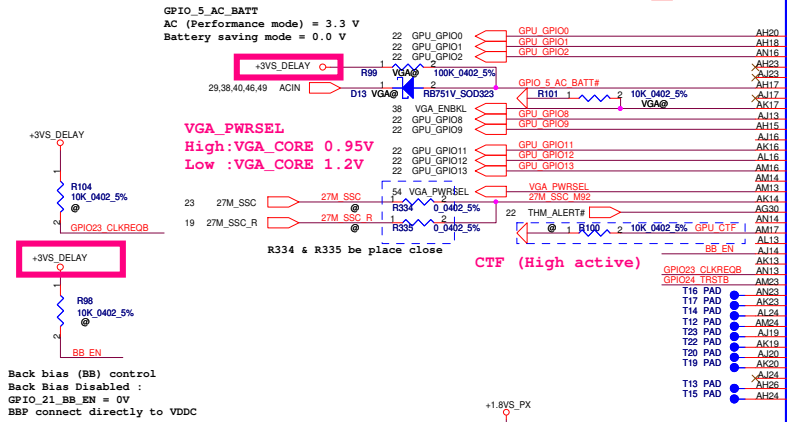
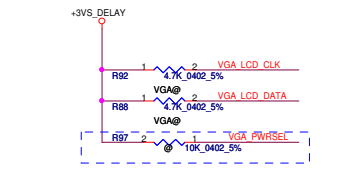
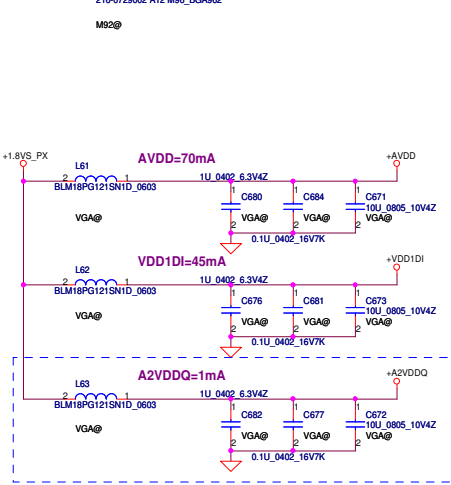
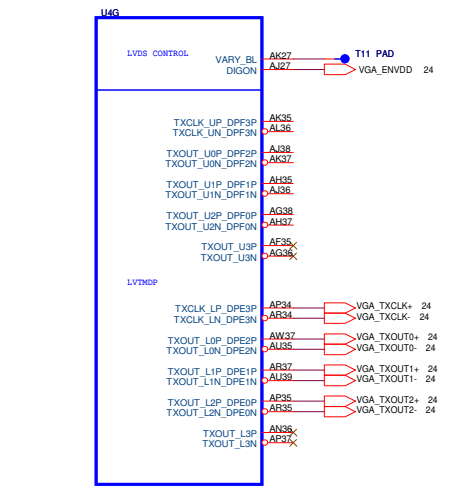
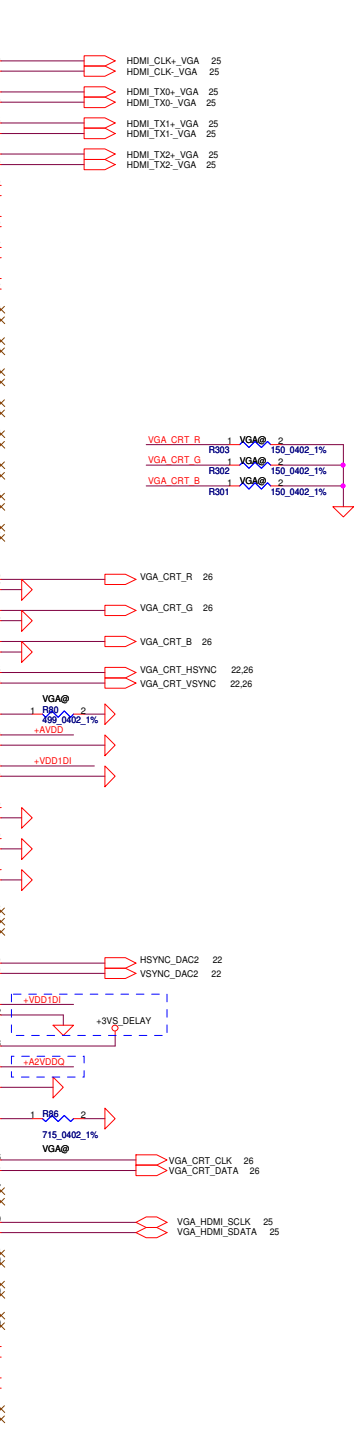


- 23 CLK\_PCIE\_VGA <-- CLK\_PCIE\_VGA# AB35
- 23 CLK\_PCIE\_VGA# <-- CLK\_PCIE\_VGA# AA36



PCI EXPRESS INTERFACE

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Size	Document Number	Rev		0.1	
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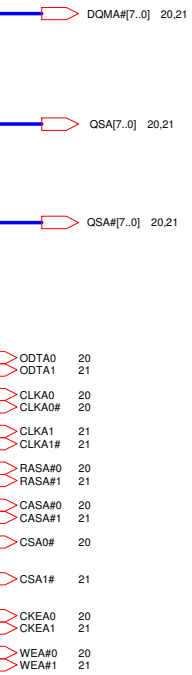


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				C	KBLG0 LA-4921P
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**MEMORY INTERFACE B**

- MDA0 C5 DOB\_0
- MDA1 C3 DOB\_1
- MDA2 E3 DOB\_2
- MDA3 E1 DOB\_3
- MDA4 F1 DOB\_4
- MDA5 F3 DOB\_5
- MDA6 F5 DOB\_6
- MDA7 G4 DOB\_7
- MDA8 H5 DOB\_8
- MDA9 H6 DOB\_9
- MDA10 U4 DOB\_10
- MDA11 K6 DOB\_11
- MDA12 K5 DOB\_12
- MDA13 L4 DOB\_13
- MDA14 M6 DOB\_14
- MDA15 M1 DOB\_15
- MDA16 M3 DOB\_16
- MDA17 M5 DOB\_17
- MDA18 N4 DOB\_18
- MDA19 P6 DOB\_19
- MDA20 P5 DOB\_20
- MDA21 R4 DOB\_21
- MDA22 T6 DOB\_22
- MDA23 T1 DOB\_23
- MDA24 U4 DOB\_24
- MDA25 V6 DOB\_25
- MDA26 V1 DOB\_26
- MDA27 V3 DOB\_27
- MDA28 Y6 DOB\_28
- MDA29 Y1 DOB\_29
- MDA30 Y3 DOB\_30
- MDA31 Y5 DOB\_31
- MDA32 A44 DOB\_32
- MDA33 AB6 DOB\_33
- MDA34 AB1 DOB\_34
- MDA35 AB3 DOB\_35
- MDA36 AD6 DOB\_36
- MDA37 AD1 DOB\_37
- MDA38 AD3 DOB\_38
- MDA39 AD5 DOB\_39
- MDA40 AF1 DOB\_40
- MDA41 AF3 DOB\_41
- MDA42 AF6 DOB\_42
- MDA43 AG4 DOB\_43
- MDA44 AH5 DOB\_44
- MDA45 AH6 DOB\_45
- MDA46 AU4 DOB\_46
- MDA47 AK3 DOB\_47
- MDA48 AF8 DOB\_48
- MDA49 AF9 DOB\_49
- MDA50 AG8 DOB\_50
- MDA51 AG7 DOB\_51
- MDA52 AK9 DOB\_52
- MDA53 AL7 DOB\_53
- MDA54 AM8 DOB\_54
- MDA55 AM7 DOB\_55
- MDA56 AK1 DOB\_56
- MDA57 AL4 DOB\_57
- MDA58 AM1 DOB\_58
- MDA59 AM6 DOB\_59
- MDA60 AN4 DOB\_60
- MDA61 AP3 DOB\_61
- MDA62 AP1 DOB\_62
- MDA63 AP5 DOB\_63

- P8 MAA0
- T9 MAA1
- P9 MAA2
- N7 MAA3
- N8 MAA4
- N9 MAA5
- U9 MAA6
- U8 MAA7
- Y9 MAA8
- W9 MAA9
- AC8 MAA10
- AC9 MAA11
- AA7 MAA12
- AA8 MAA13
- Y8 BA0
- AA9 BA1
- H3 DMA#0
- H1 DMA#1
- T3 DMA#2
- T5 DMA#3
- AE4 DMA#4
- AF5 DMA#5
- AK6 DMA#6
- AK5 DMA#7
- F6 OSA0
- K3 OSA1
- P3 OSA2
- V5 OSA3
- AB5 OSA4
- AH1 OSA5
- AJ9 OSA6
- AM5 OSA7
- G7 OSA#0
- K1 OSA#1
- P1 OSA#2
- W4 OSA#3
- AC4 OSA#4
- AH3 OSA#5
- AJ8 OSA#6
- AM3 OSA#7
- T7 ODTA0
- W7 ODTA1
- L9 CLKA0
- LB CLKA0#
- AD8 CLKA1
- AD7 CLKA1#
- T10 RASA#0
- Y10 RASA#1
- W10 CASA#0
- AA10 CASA#1
- P10 CSA0#
- L10 CSA0#
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- AA11 CKEA1
- N10 WEA#0
- AB11 WEA#1



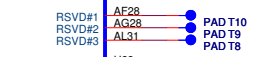
DRAM\_RST

216-0729002 A12 M96\_BGA962  
M92@

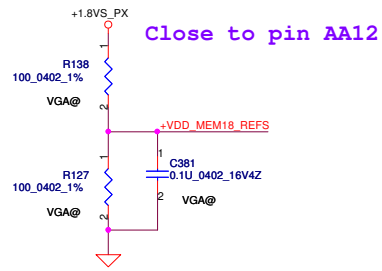
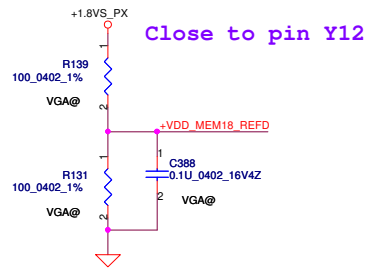
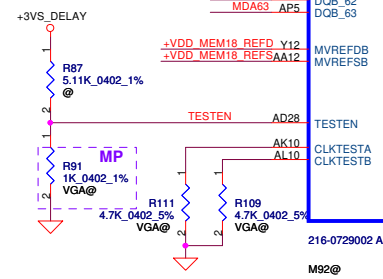
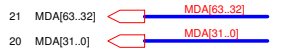
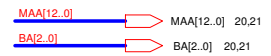
**MEMORY INTERFACE A**

- C37 DOA\_0
- C35 DOA\_1
- A35 DOA\_2
- E34 DOA\_3
- G32 DOA\_4
- D33 DOA\_5
- F32 DOA\_6
- E32 DOA\_7
- D31 DOA\_8
- F30 DOA\_9
- A30 DOA\_10
- D30 DOA\_11
- F28 DOA\_12
- C28 DOA\_13
- A28 DOA\_14
- E28 DOA\_15
- D27 DOA\_16
- F26 DOA\_17
- C26 DOA\_18
- A26 DOA\_19
- F24 DOA\_20
- C24 DOA\_21
- A24 DOA\_22
- E24 DOA\_23
- C22 DOA\_24
- A22 DOA\_25
- F22 DOA\_26
- K3 OSA\_0
- A50 DOA\_27
- D28 DOA\_28
- D29 DOA\_29
- D19 DOA\_30
- E18 DOA\_31
- C18 DOA\_32
- A18 DOA\_33
- F18 DOA\_34
- D17 DOA\_35
- A16 DOA\_36
- F16 DOA\_37
- D15 DOA\_38
- E14 DOA\_39
- F14 DOA\_40
- D13 DOA\_41
- F12 DOA\_42
- A12 DOA\_43
- D11 DOA\_44
- F10 DOA\_45
- A10 DOA\_46
- C10 DOA\_47
- G13 DOA\_48
- H13 DOA\_49
- J13 DOA\_50
- H11 DOA\_51
- G10 DOA\_52
- G8 DOA\_53
- K9 DOA\_54
- K10 DOA\_55
- G9 DOA\_56
- C8 DOA\_57
- C8 DOA\_58
- E8 DOA\_59
- A6 DOA\_60
- C6 DOA\_61
- E6 DOA\_62
- A5 DOA\_63
- L18 MVREFDA
- L20 MVREFSA
- L27 NC\_MEM\_CALRN0
- N12 NC\_MEM\_CALRN1
- AG12 NC\_MEM\_CALRN2
- M12 MEM\_CALRP1
- M27 NC\_MEM\_CALRP0
- AH12 NC\_MEM\_CALRP2

- MAA\_0 G24
- MAA\_1 J23
- MAA\_2 H24
- MAA\_3 J24
- MAA\_4 H26
- MAA\_5 J26
- MAA\_6 G21
- MAA\_7 H19
- MAA\_8 H20
- MAA\_9 G16
- MAA\_10 G16
- MAA\_11 H16
- MAA\_12 J16
- MAA\_13/B2A H18
- MAA\_14/BA0 H17
- MAA\_15/BA1 H17
- DOA\_0 A32
- DOA\_1 C32
- DOA\_2 D33
- DOA\_3 E22
- DOA\_4 C14
- DOA\_5 A14
- DOA\_6 K10
- DOA\_7 D9
- OSA\_0/RDQSA\_0 C34
- OSA\_1/RDQSA\_1 D25
- OSA\_2/RDQSA\_2 E20
- OSA\_3/RDQSA\_3 E16
- OSA\_4/RDQSA\_4 E12
- OSA\_5/RDQSA\_5 H10
- OSA\_6/RDQSA\_6 D7
- OSA\_7/RDQSA\_7 D7
- OSA\_0B/WDQSA\_0 A34
- OSA\_1B/WDQSA\_1 E26
- OSA\_2B/WDQSA\_2 C20
- OSA\_3B/WDQSA\_3 C16
- OSA\_4B/WDQSA\_4 C12
- OSA\_5B/WDQSA\_5 H11
- OSA\_6B/WDQSA\_6 F8
- OSA\_7B/WDQSA\_7 F8
- ODTA0 J21
- ODTA1 G19
- CLKA0 H27
- CLKA0B G27
- CLKA1 J14
- CLKA1B H14
- RASA0B K23
- RASA1B K19
- CASA0B K20
- CASA1B K17
- CSA0B\_0 K24
- CSA0B\_1 K27
- CSA1B\_0 M13
- CSA1B\_1 K16
- CKEA0 K21
- CKEA1 J20
- WEA0B K26
- WEA1B L15
- RSVD#1 AF28
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- RSVD#3 AL31
- RSVD#5 H23
- RSVD#6 J19
- RSVD#9 T8
- RSVD#11 W8



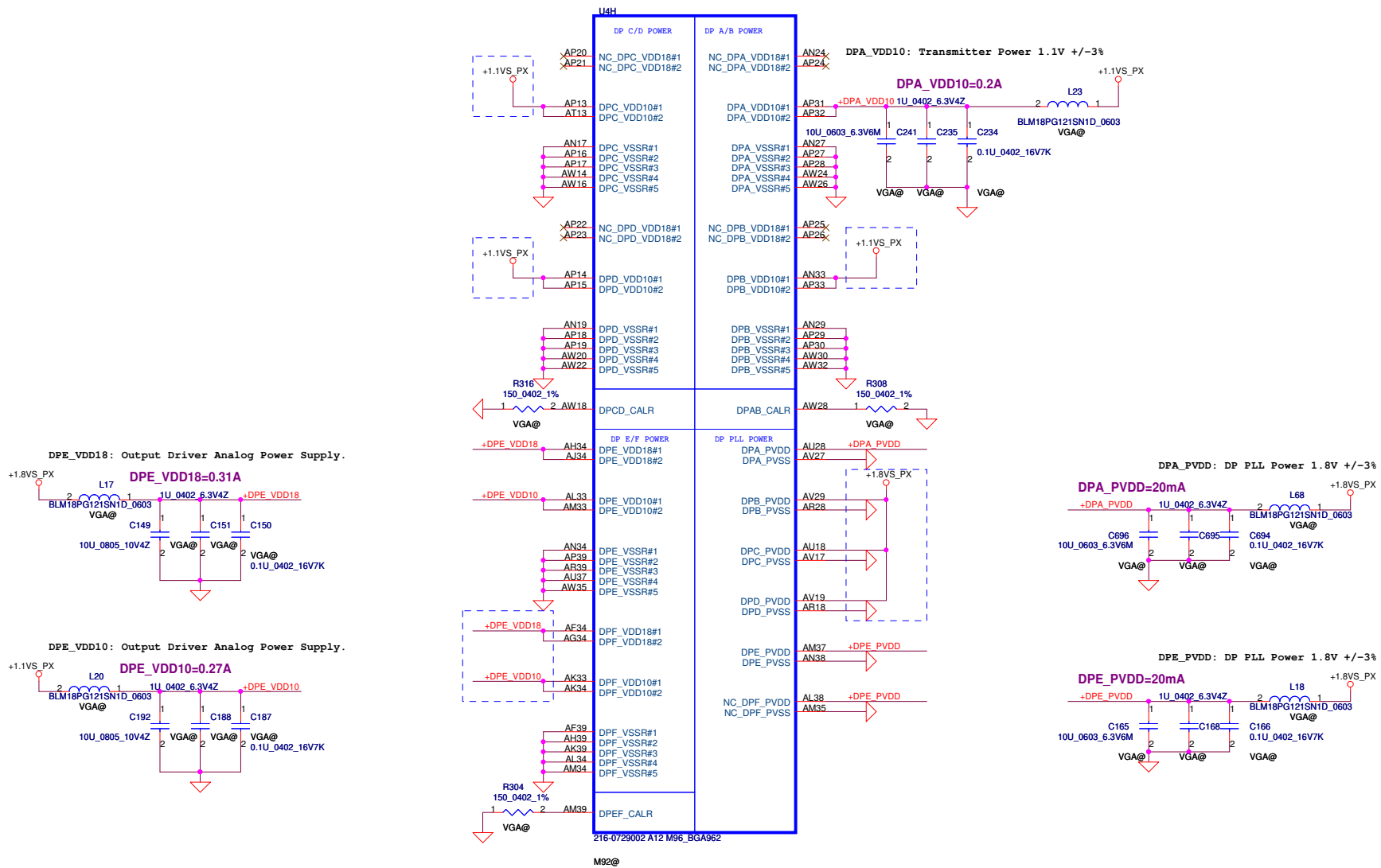
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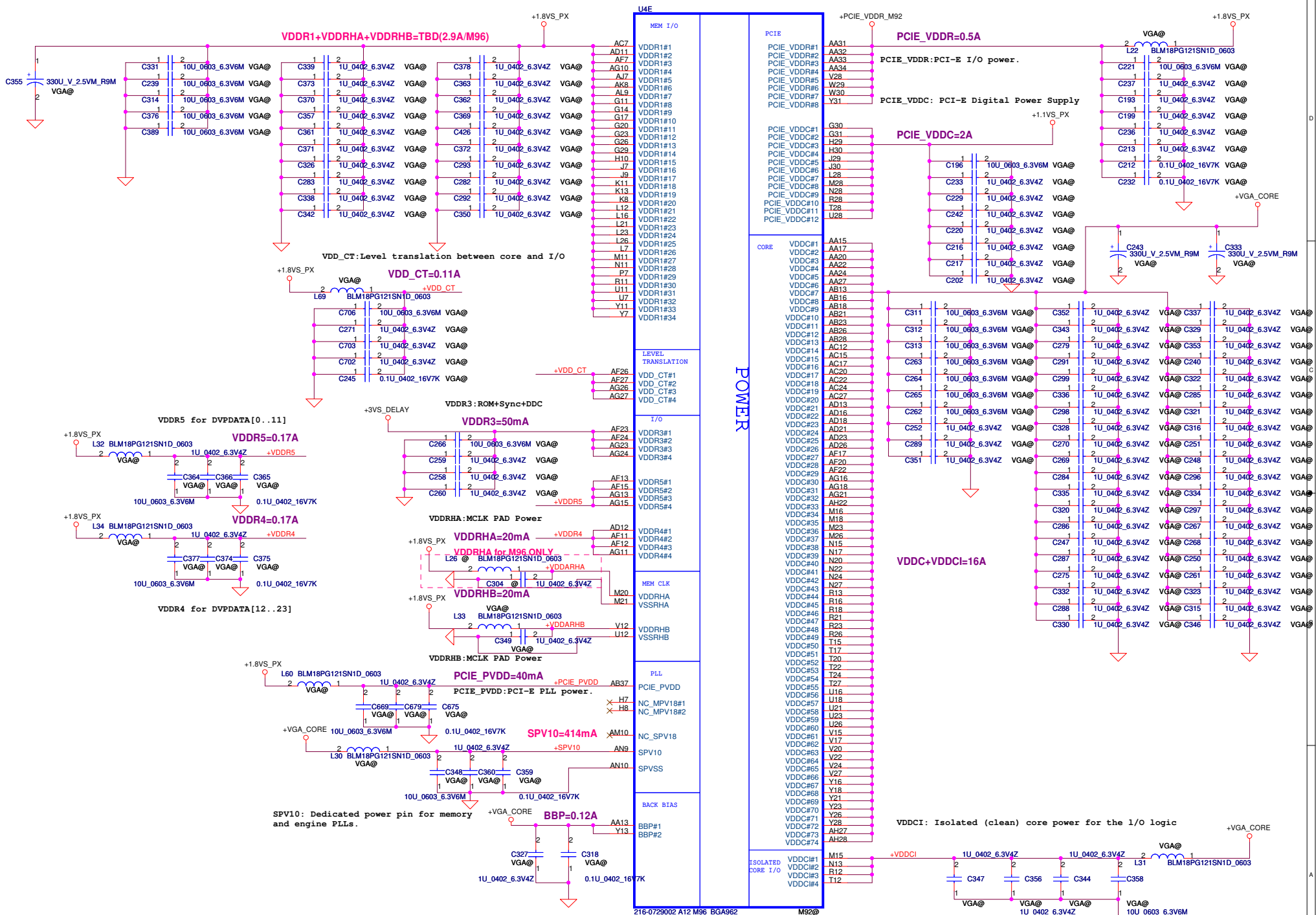
M92-S2 and M92-M use memory group A only while M92-M2 uses memory group B only.

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Size	Document Number	Rev		0.1	
Custom	KBLG0 LA-4921P				
Date:	Thursday, January 15, 2009	Sheet	18	of 57	

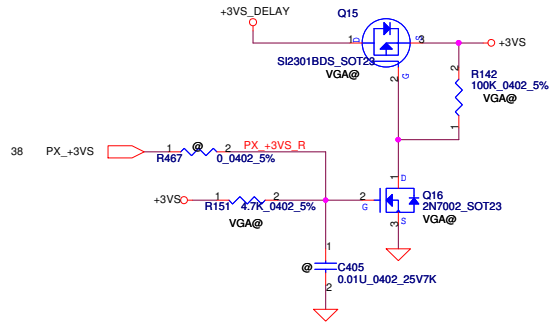
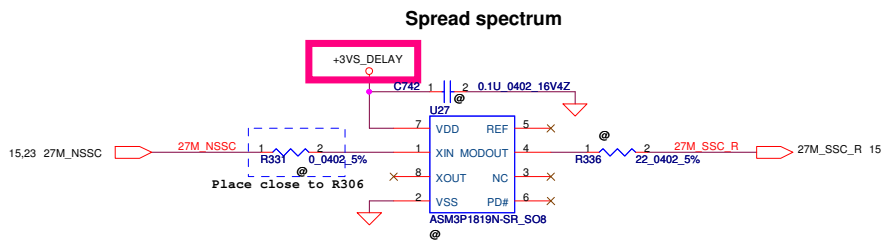
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E39	PCIE_VSS#2	A37
F34	PCIE_VSS#3	GND#3
F39	PCIE_VSS#4	AA16
G33	PCIE_VSS#5	GND#4
G34	PCIE_VSS#6	AA18
H31	PCIE_VSS#7	GND#5
H34	PCIE_VSS#8	AA2
H39	PCIE_VSS#9	GND#6
J1	PCIE_VSS#10	GND#7
J4	PCIE_VSS#11	GND#8
K31	PCIE_VSS#12	GND#9
K34	PCIE_VSS#13	GND#10
K39	PCIE_VSS#14	GND#11
L31	PCIE_VSS#15	GND#12
L34	PCIE_VSS#16	GND#13
M34	PCIE_VSS#17	GND#14
M39	PCIE_VSS#18	GND#15
N31	PCIE_VSS#19	GND#16
N34	PCIE_VSS#20	GND#17
P31	PCIE_VSS#21	GND#18
P34	PCIE_VSS#22	GND#19
P39	PCIE_VSS#23	GND#20
R34	PCIE_VSS#24	GND#21
T31	PCIE_VSS#25	GND#22
T34	PCIE_VSS#26	GND#23
T39	PCIE_VSS#27	GND#24
U31	PCIE_VSS#28	GND#25
U34	PCIE_VSS#29	GND#26
V34	PCIE_VSS#30	GND#27
V39	PCIE_VSS#31	GND#28
W31	PCIE_VSS#32	GND#29
W34	PCIE_VSS#33	GND#30
Y34	PCIE_VSS#34	GND#31
Y39	PCIE_VSS#35	GND#32
GND		
F15	GND#101	A39
F17	GND#102	AW1
F19	GND#103	AW39
F21	GND#104	
F24	GND#105	
F25	GND#106	
F27	GND#107	
F29	GND#108	
F31	GND#109	
F33	GND#110	
F7	GND#111	
F9	GND#112	
G2	GND#113	
G6	GND#114	
H9	GND#115	
J2	GND#116	
J27	GND#117	
J6	GND#118	
J6	GND#119	
K14	GND#120	
K7	GND#121	
L11	GND#122	
L17	GND#123	
L2	GND#124	
L22	GND#125	
L24	GND#126	
L6	GND#127	
M17	GND#128	
M22	GND#129	
M24	GND#130	
N16	GND#131	
N18	GND#132	
N2	GND#133	
N21	GND#134	
N23	GND#135	
N26	GND#136	
N6	GND#137	
R15	GND#138	
R17	GND#139	
R2	GND#140	
R20	GND#141	
R22	GND#142	
R24	GND#143	
R27	GND#144	
R6	GND#145	
T11	GND#146	
T12	GND#147	
T16	GND#148	
T18	GND#149	
T21	GND#150	
T24	GND#151	
T26	GND#152	
U15	GND#153	
U17	GND#154	
U2	GND#155	
U20	GND#156	
U22	GND#157	
U24	GND#158	
U27	GND#159	
U6	GND#160	
V11	GND#161	
V16	GND#162	
V18	GND#163	
V21	GND#164	
V23	GND#165	
V26	GND#166	
W2	GND#167	
W6	GND#168	
Y15	GND#169	
Y17	GND#170	
Y20	GND#171	
Y22	GND#172	
Y24	GND#173	
Y27	GND#174	
U13	GND#175	
Y13	GND#176	

216-0729002 A12 M96\_BGA962

M92@

VSS\_MECH#1  
VSS\_MECH#2  
VSS\_MECH#3

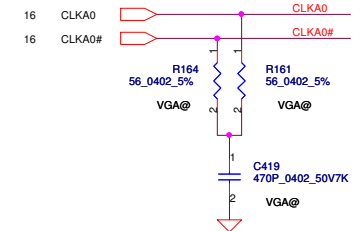
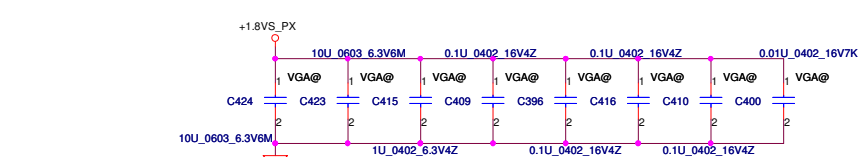
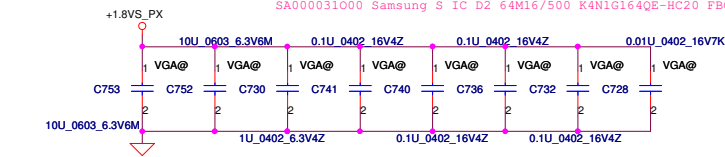
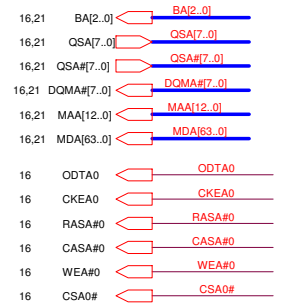
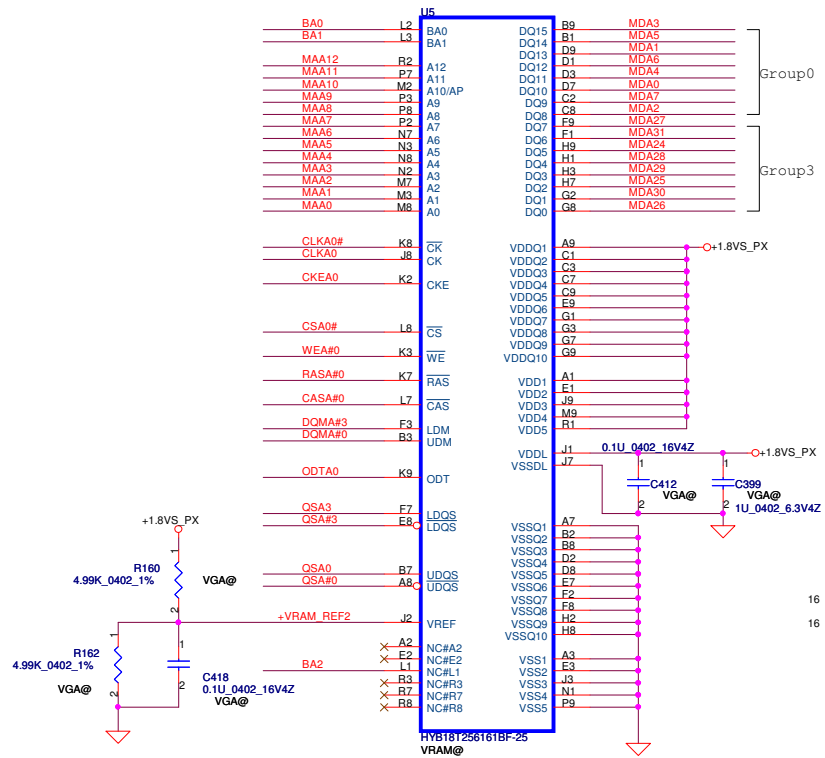
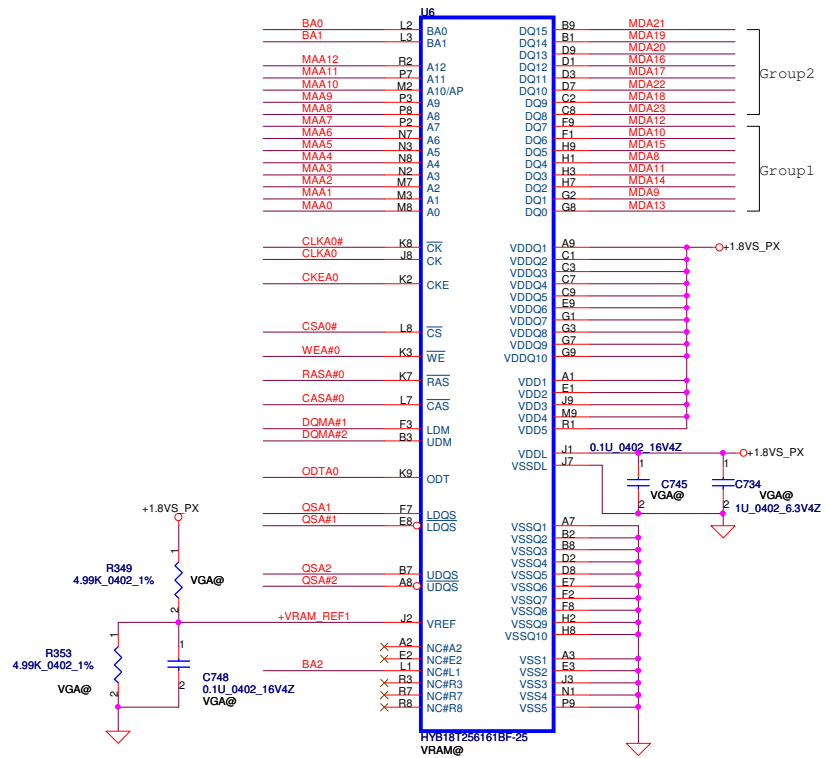
A39  
AW1  
AW39



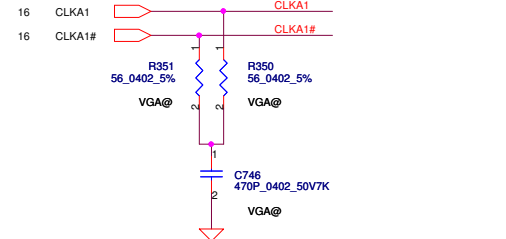
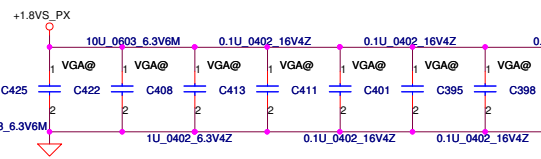
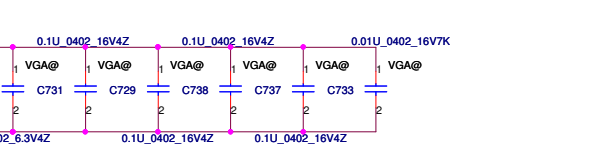
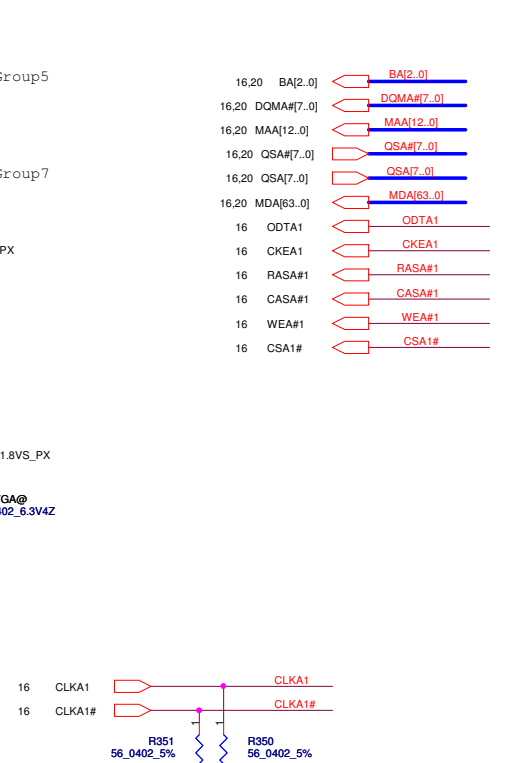
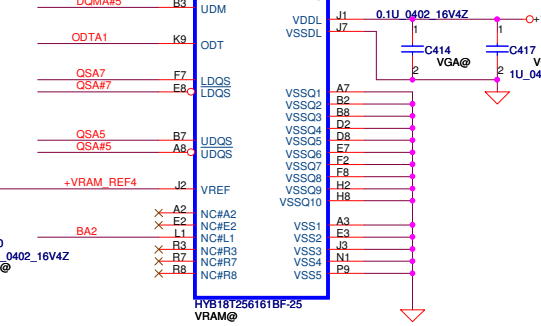
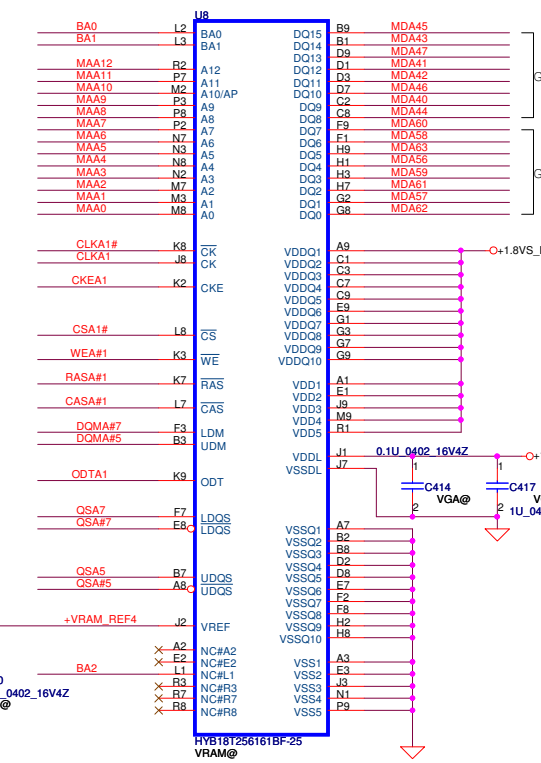
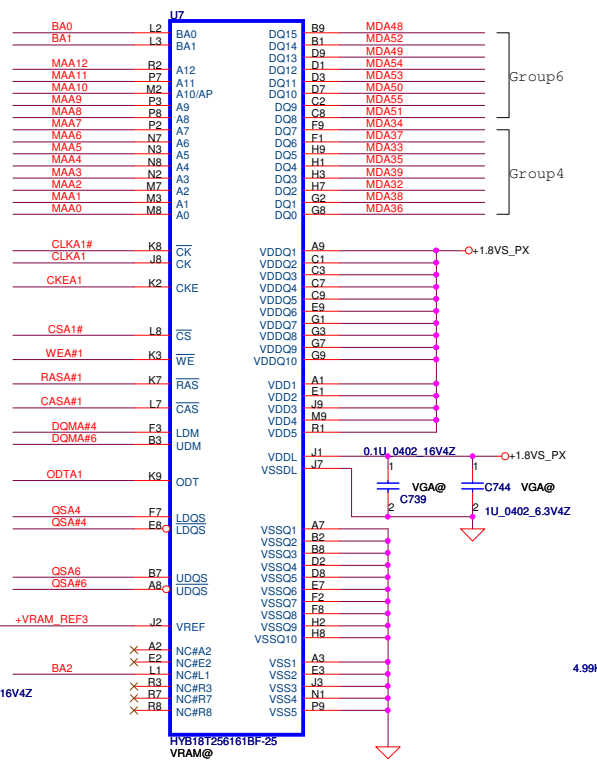
Use Delay 3.3V BUS (VDDR3) for GPIO/DDC Pull up to reduce Leakage to VDDR3 Bus.

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M92 GND			
Size	Document Number	Rev	
Custom	KBLG0 LA-4921P	0.1	
Date:	Thursday, February 19, 2009	Sheet	19 of 57

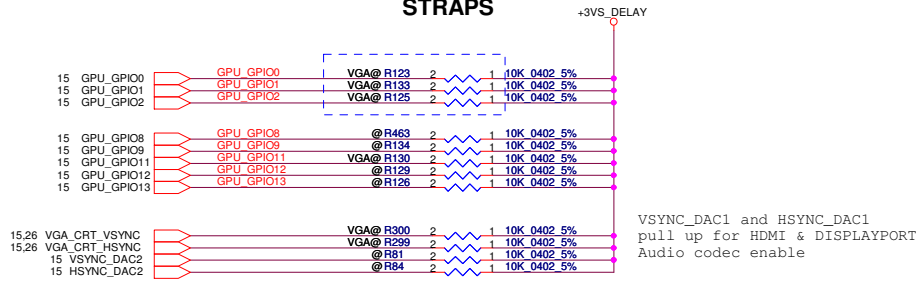


Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	M92 VRAM
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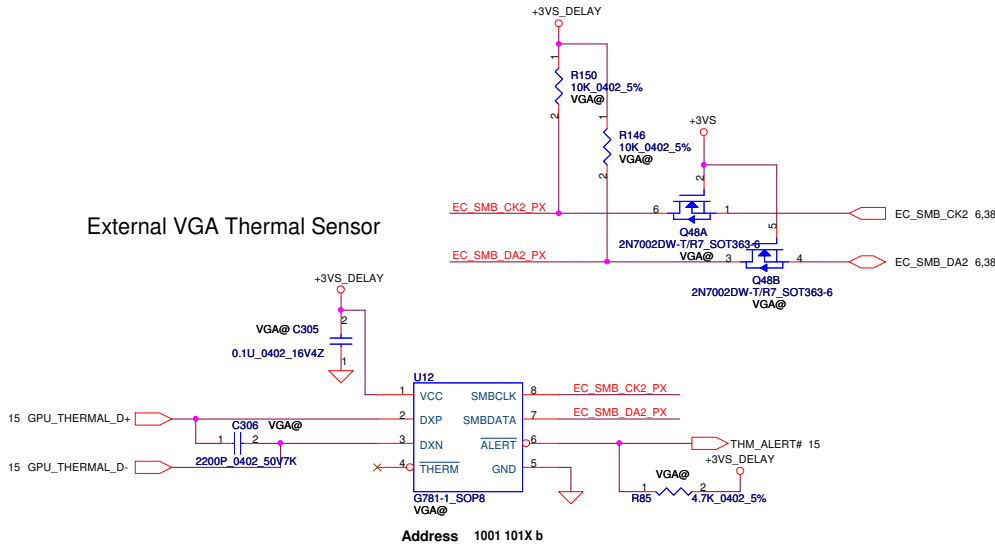


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				M92 VRAM	
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				Rev	0.1

### STRAPS



### External VGA Thermal Sensor



### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable	1 : PCIe bus Full Tx output swing 0 : PCIe bus 50% Tx output swing
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable	1 : Tx de-emphasis enabled 0 : Tx de-emphasis disabled
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 (5.0 GT/s capability will be controlled by software)
VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller	0 : VGA Controller capacity enabled 1 : The device will not be recognized as the system's VGA controller
CONFIG(20)	GPIO[13:11]	Size of the primary memory apertures	0 0 1
VIP_DEVICE_STRAP_EN	V2SYNC		0
RESERVED	H2SYNC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYSN	1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	
RESERVED	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0

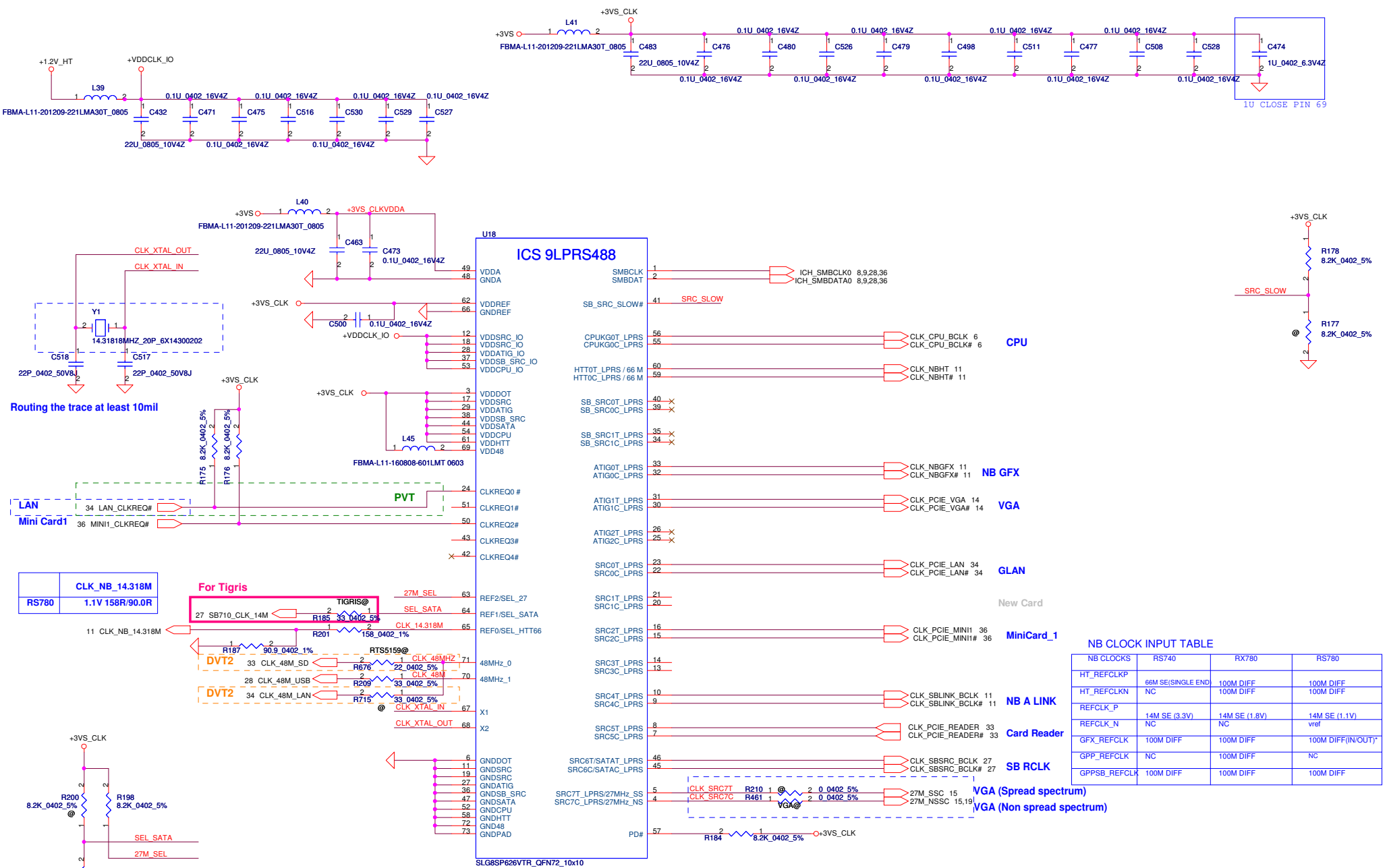
### AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO	GPIO21_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M92-M2 XT	JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (Q-die)	SA00002MD00	0 0 0 0
			JV40-PU_KBLG0	512M(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
			JV40-PU_KBLG0	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00 PVT	0 0 1 0
			JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

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1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN  
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

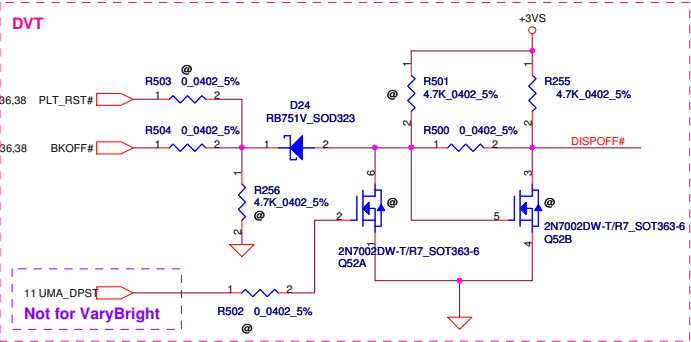
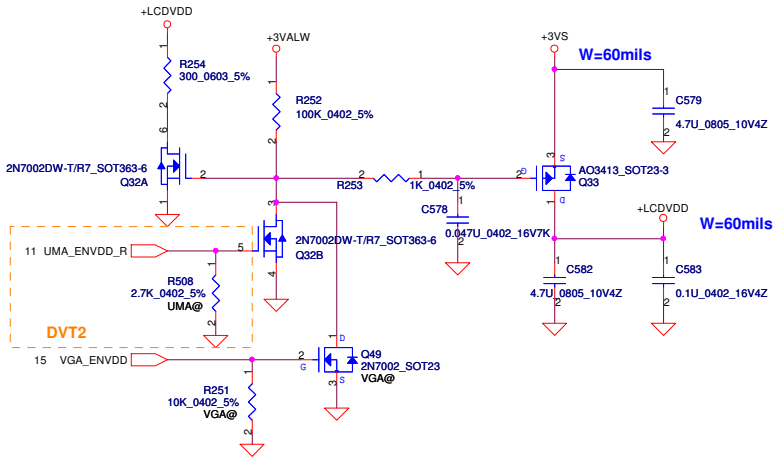
27M_SEL	1*	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

Security Classification	Compal Secret Data	
Issued Date	2008/10/06	Deciphered Date
		2009/10/06

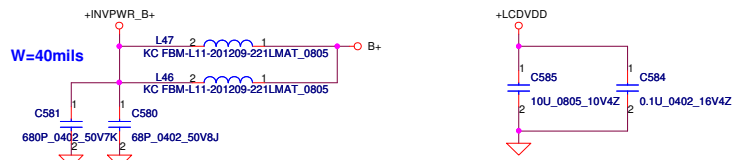
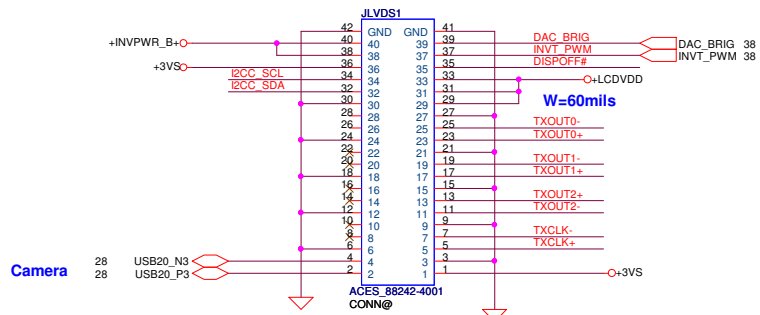
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Compal Electronics, Inc.			
Clock generator			
Title	Size	Document Number	Rev
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Date:	Wednesday, March 11, 2009		Sheet 23 of 57

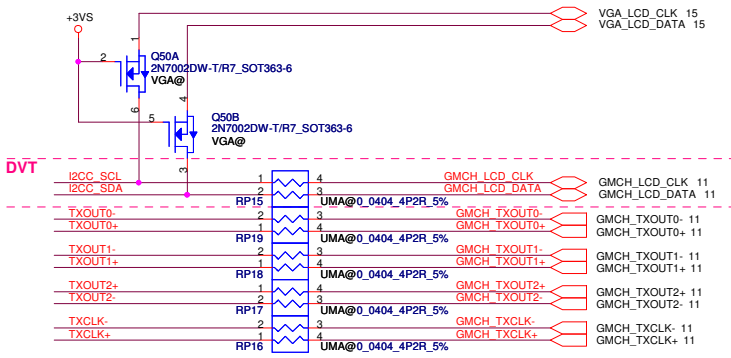
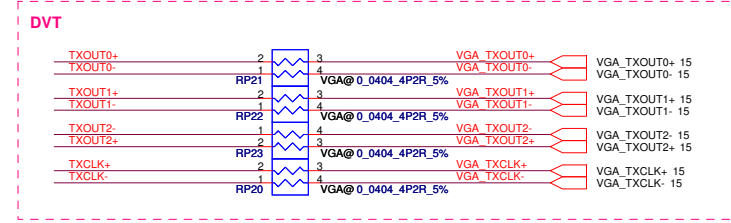
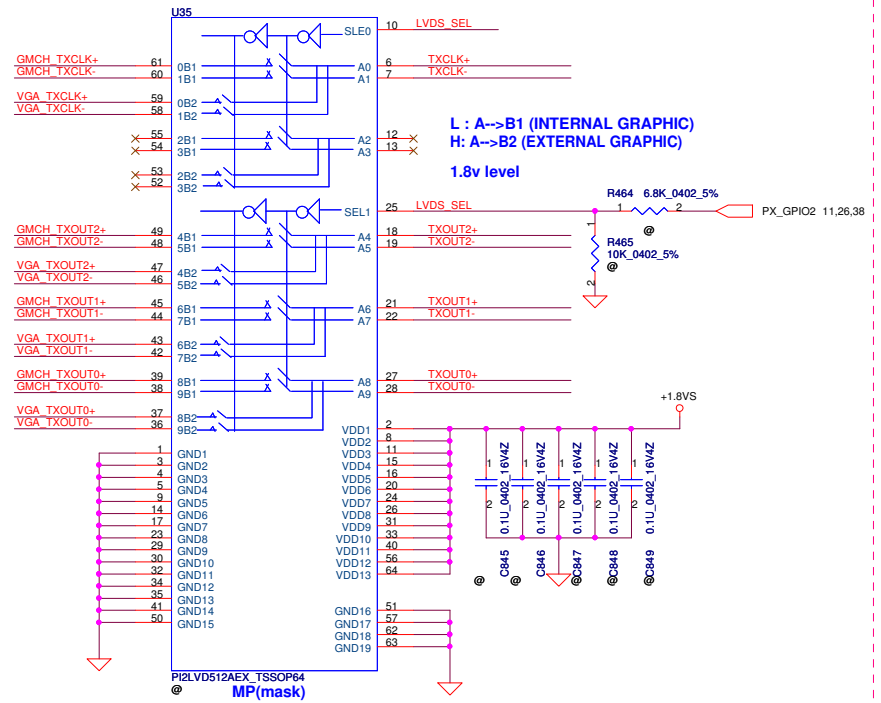
### LCD POWER CIRCUIT



### LCD/PANEL BD. Conn.



### DVT

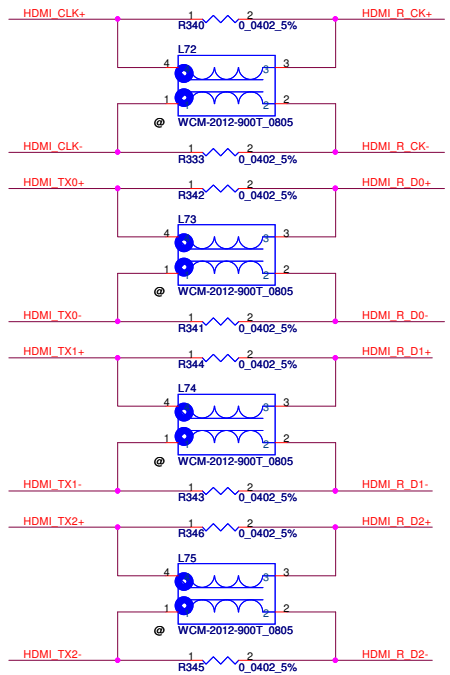
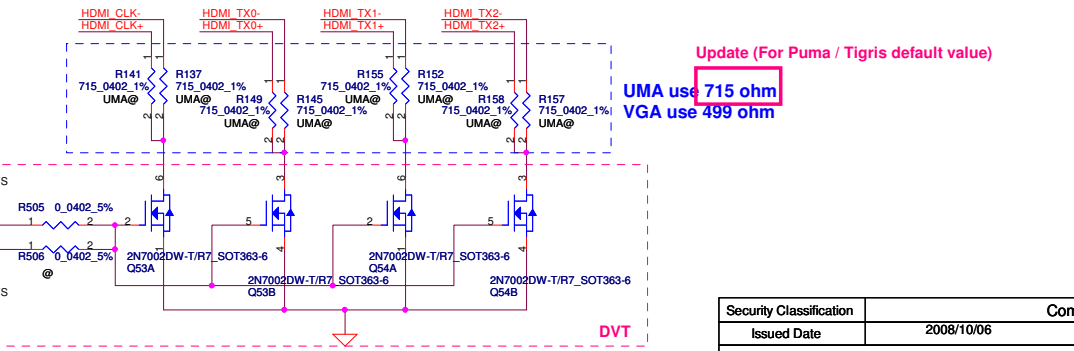
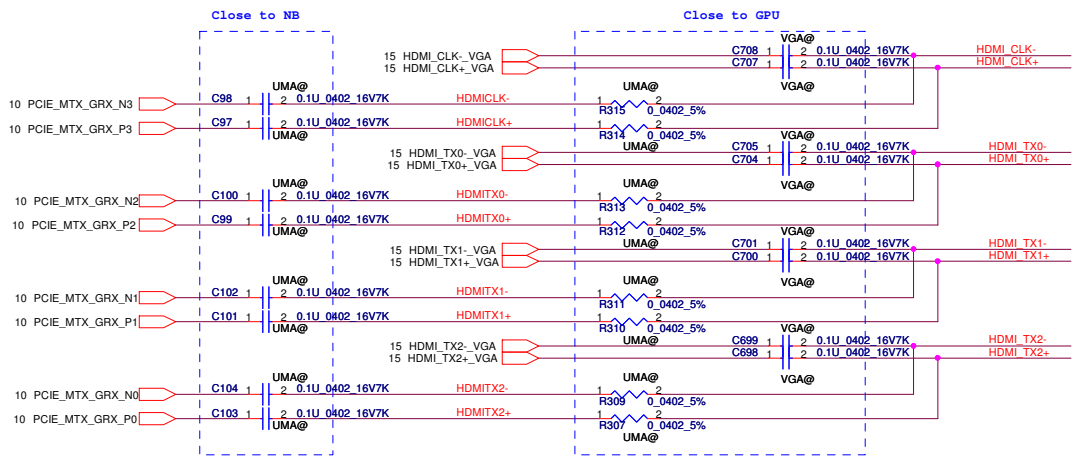
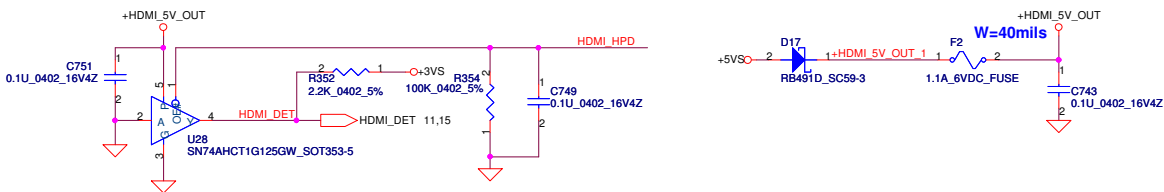
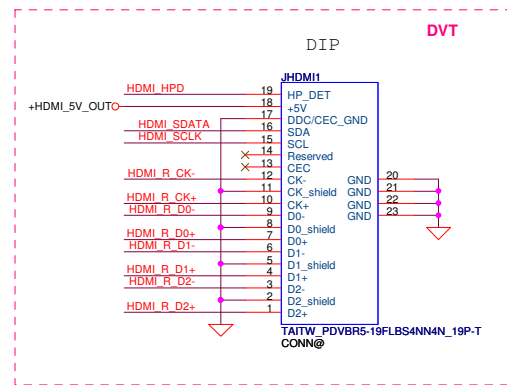
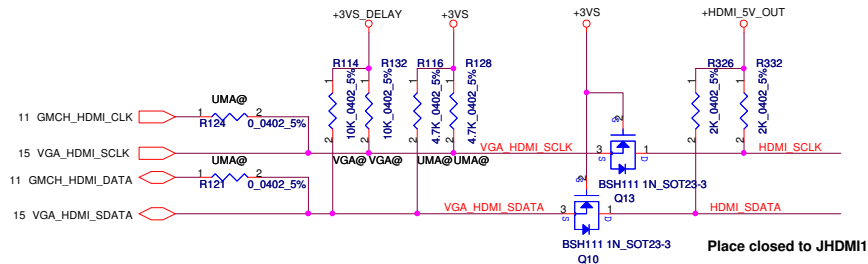


Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Compal Electronics, Inc.	
				LVDS Connector	
Size	Document Number	Date		Rev	
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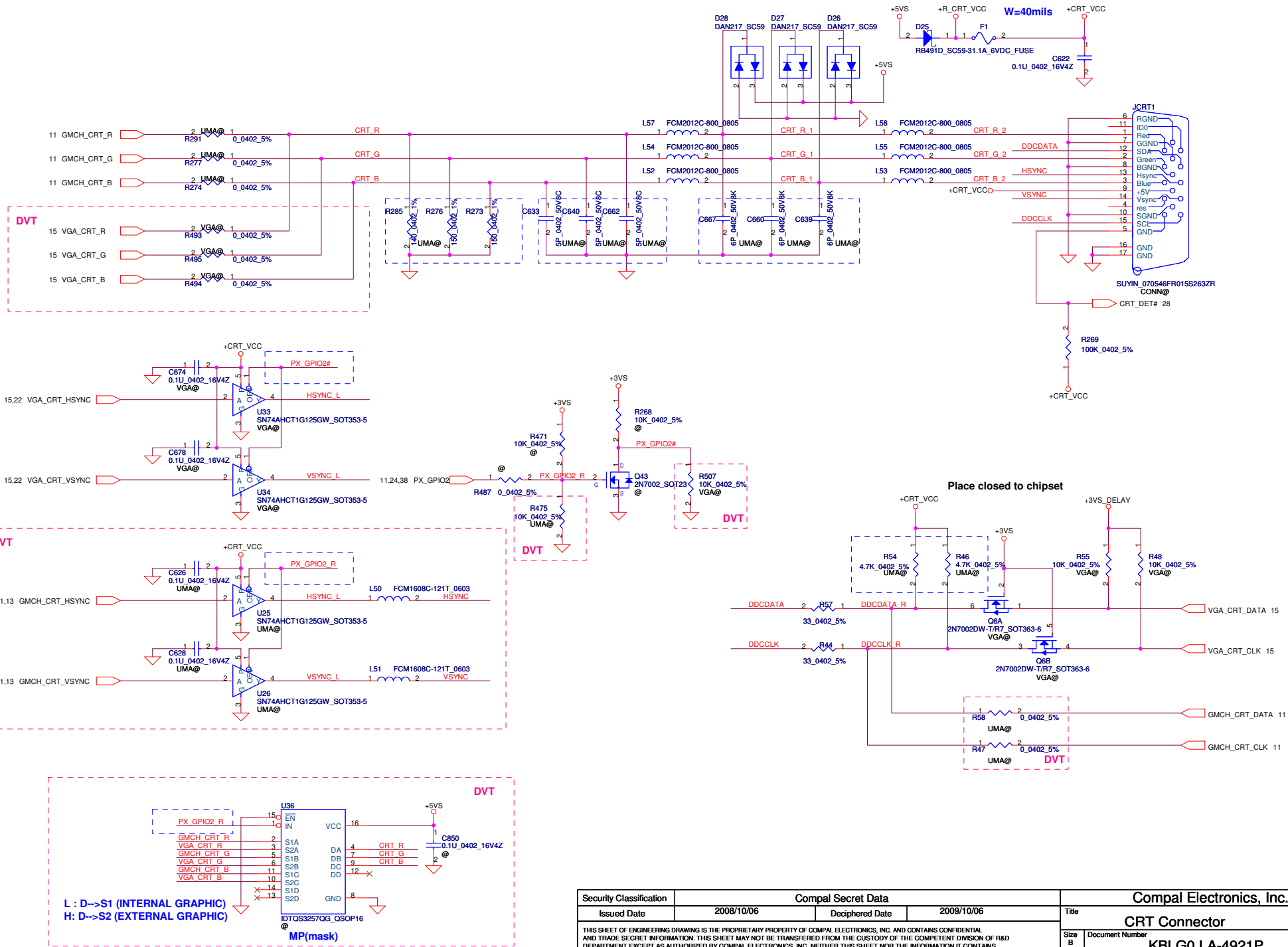


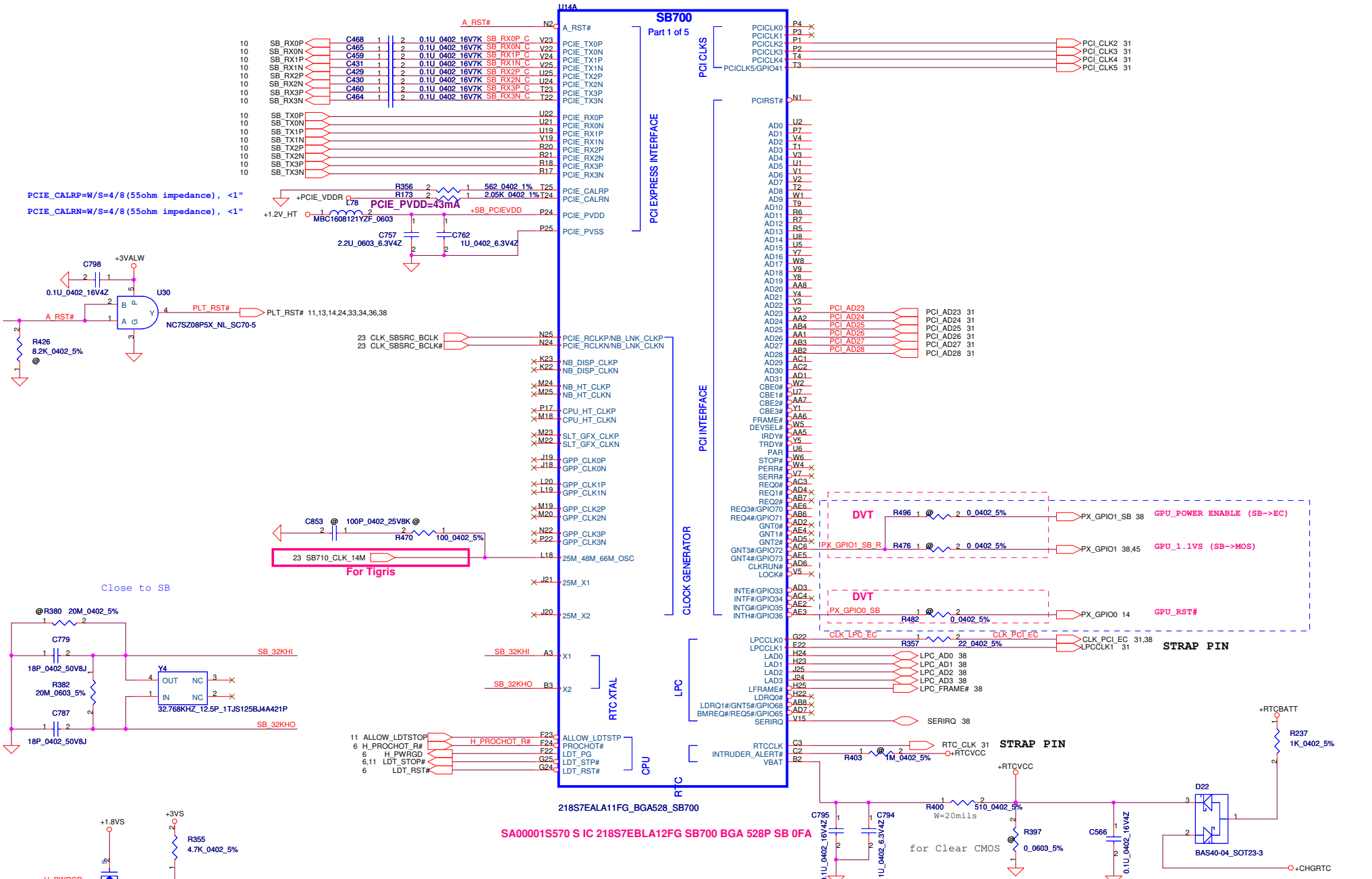
**DDC to HDMI CONN**



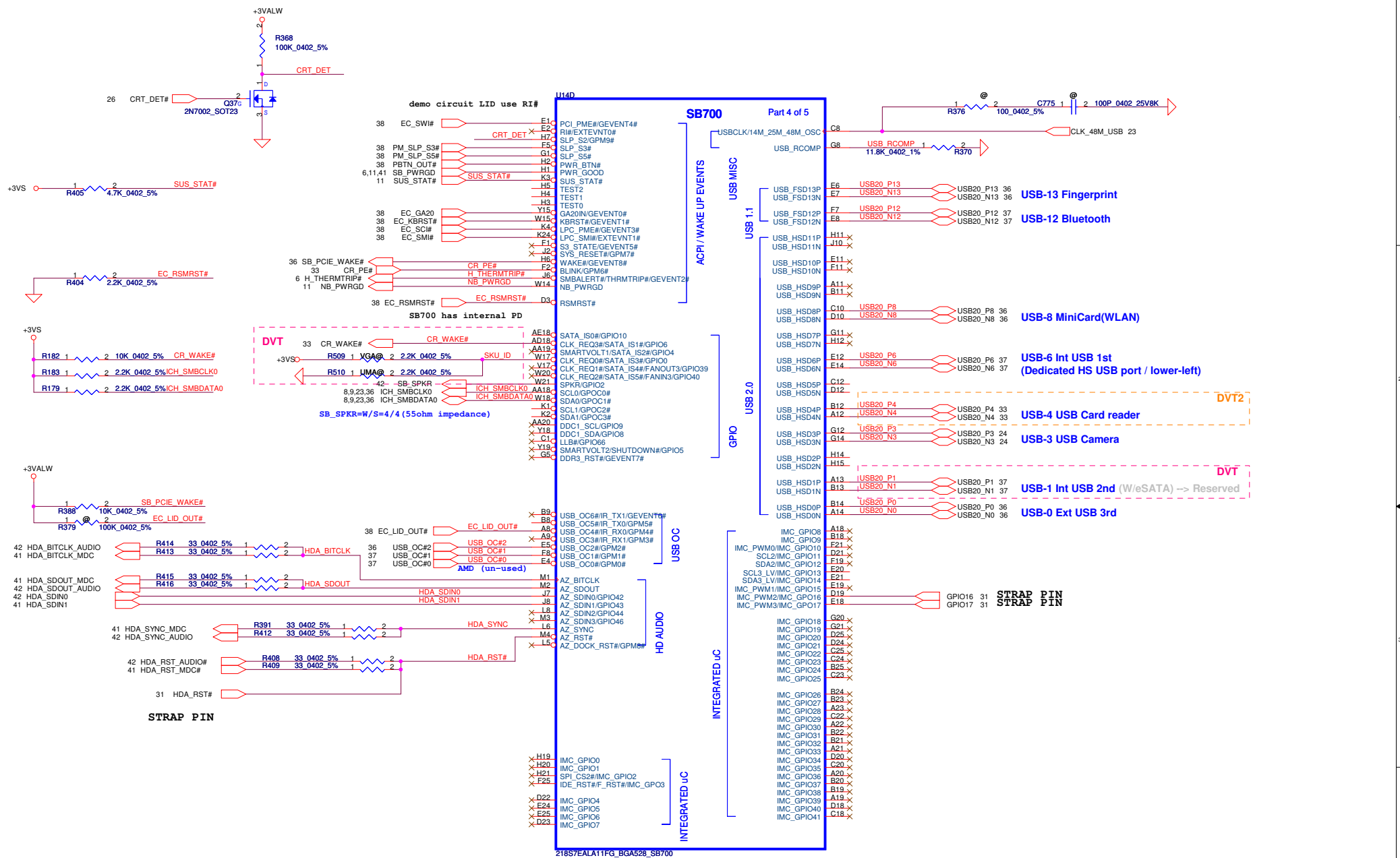
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
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Size	Document Number	KBLG0 LA-4921P		Rev	0.1
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# CRT CONNECTOR



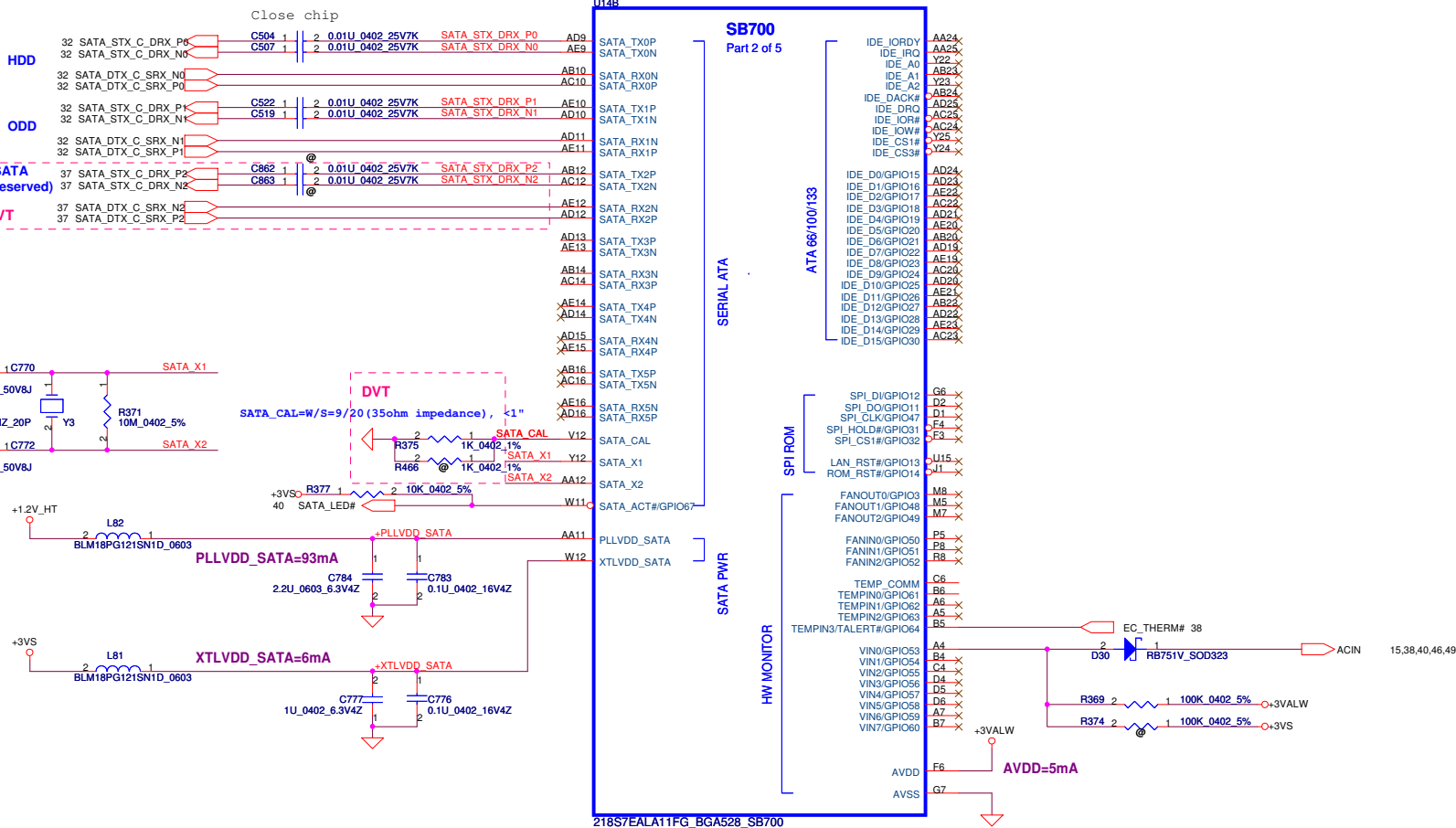


Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	SB700-PCIE/PCI/ACPI/LPC/RTC
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Size	Document Number	KBLG0 LA-4921P		Rev
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Date:	Thursday, February 19, 2009	Sheet	27	of 57

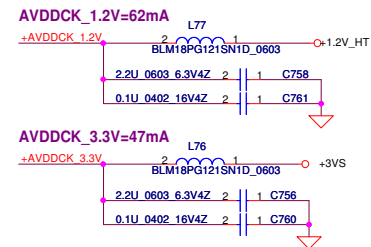
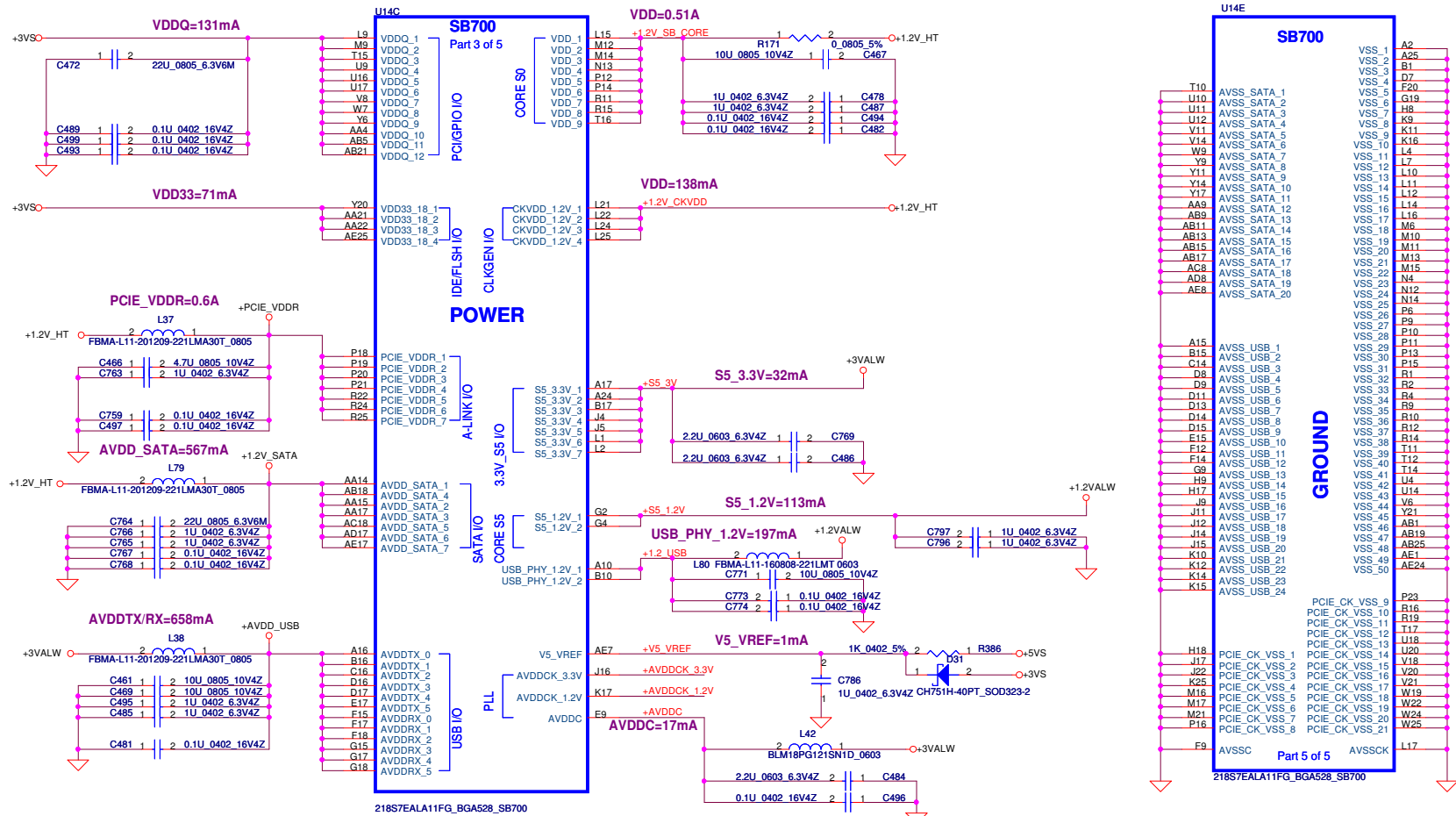


21857/EAL11FG\_BGA528\_SB700

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	Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	SB700 USB/HD audio
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Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller



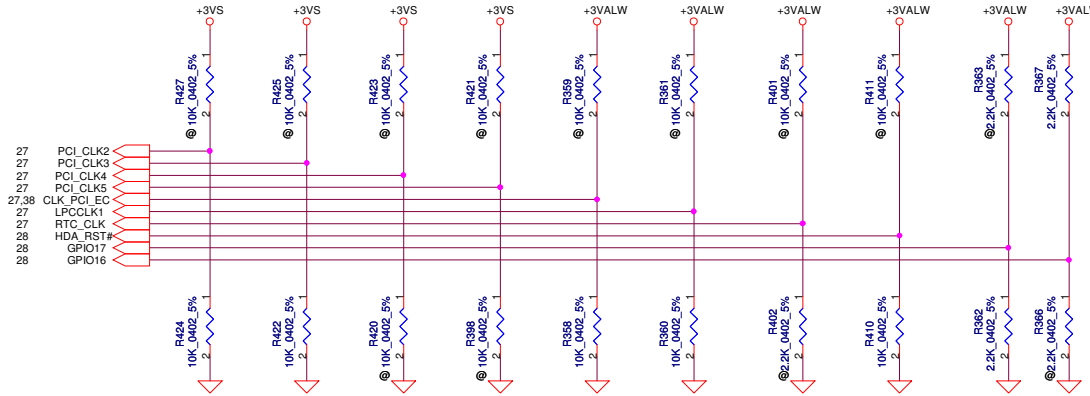
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Issued Date	2008/10/06	Deciphered Date
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Compal Electronics, Inc.		
Title		
SB700 power/GND		
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# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

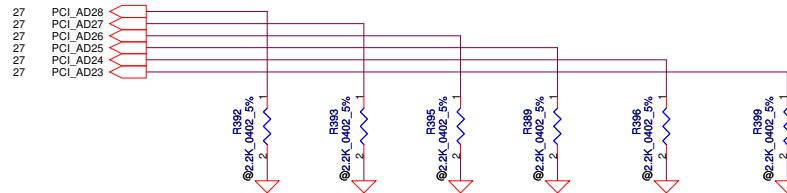
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	<b>INTERNAL RTC</b>  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) LL = FWH ROM



# DEBUG STRAPS

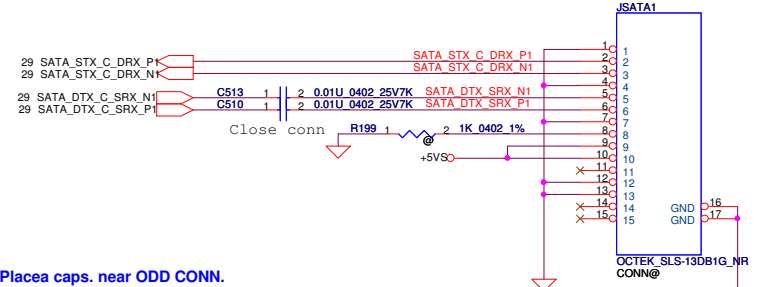
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

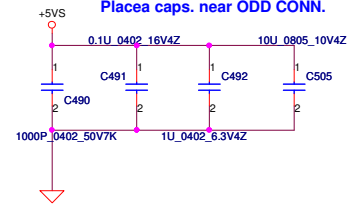


Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	
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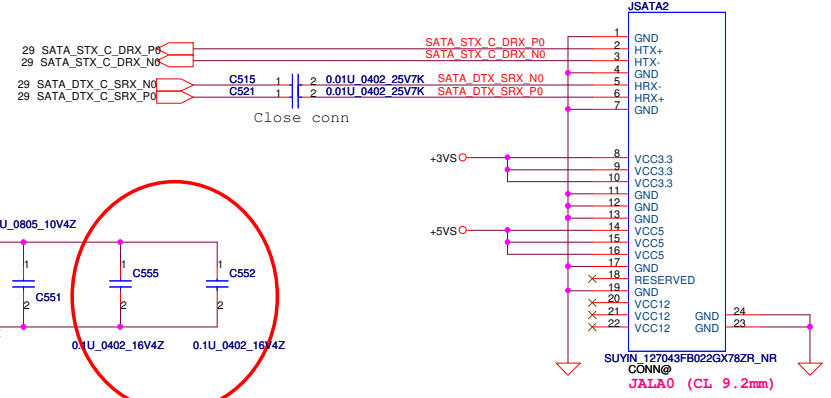
### SATA ODD Conn.



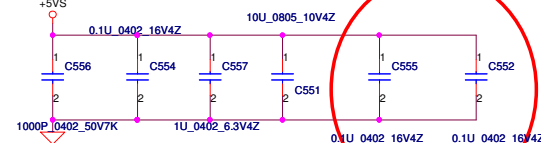
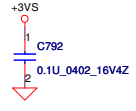
Place caps. near ODD CONN.



### SATA HDD Conn.

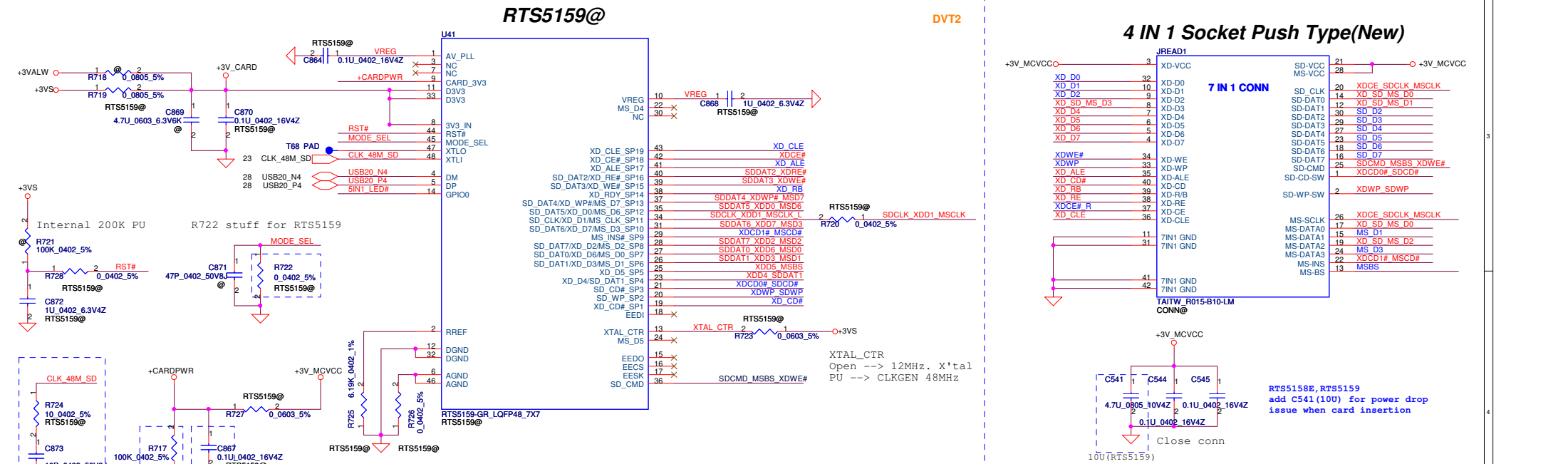
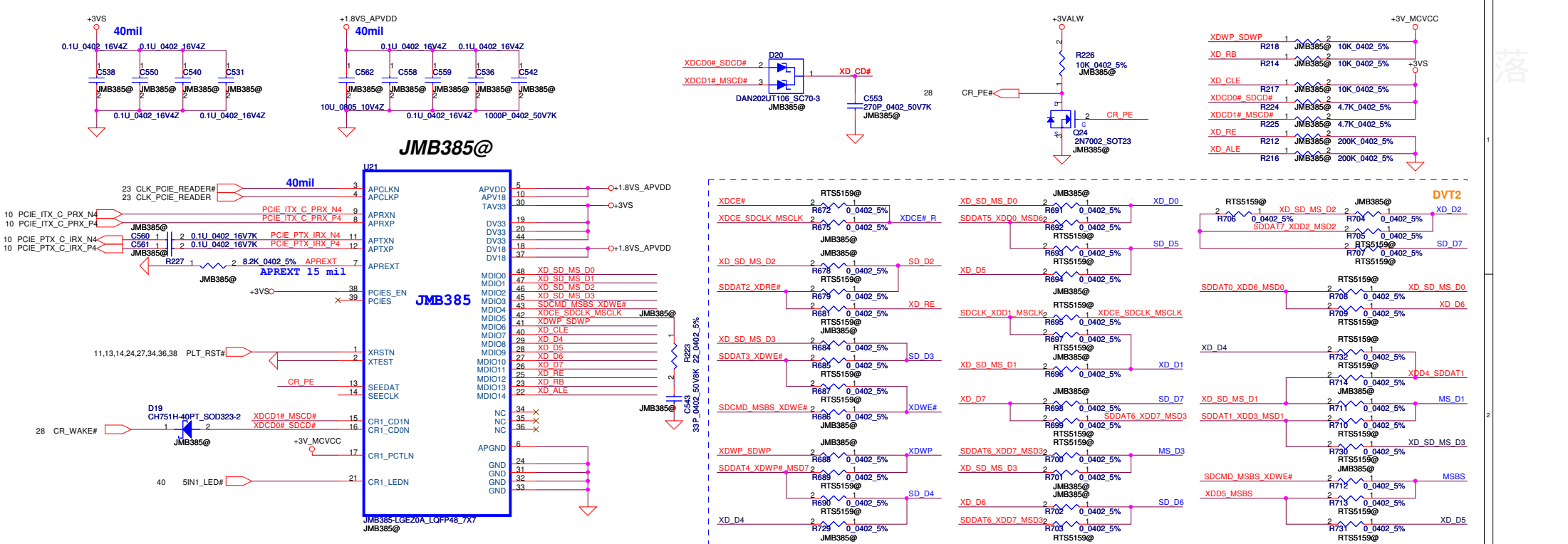


for ESD issue

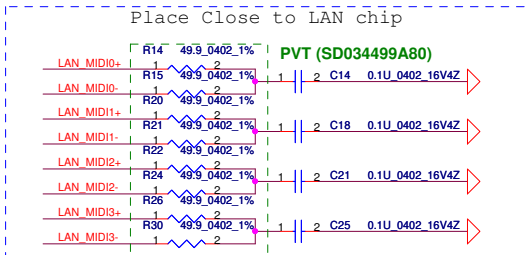
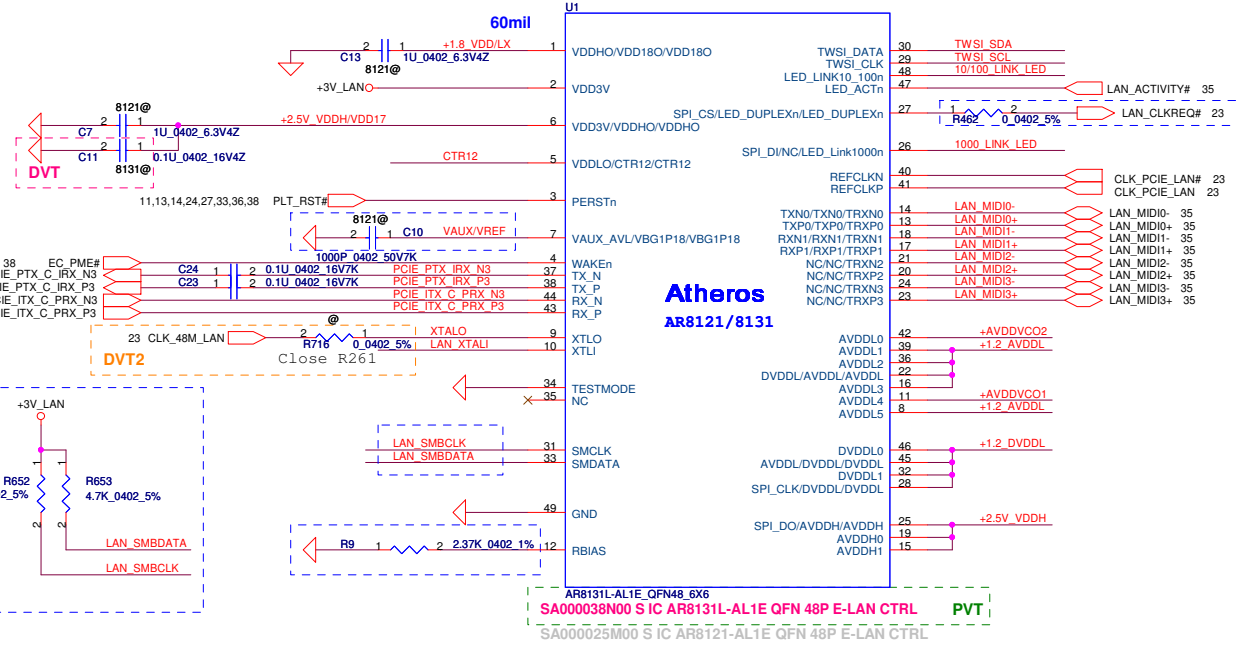
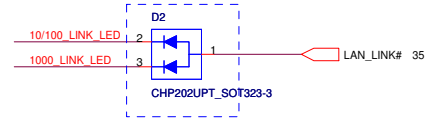
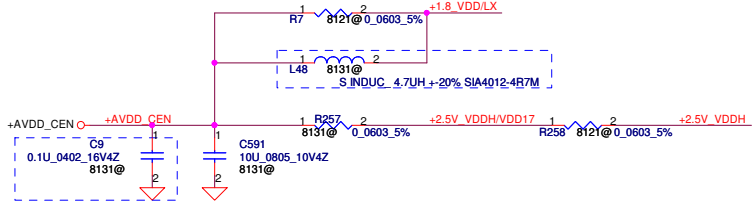
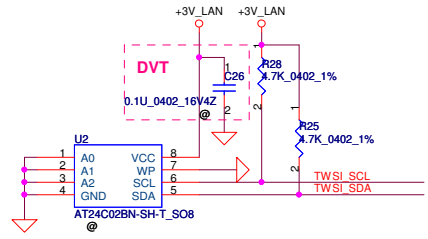
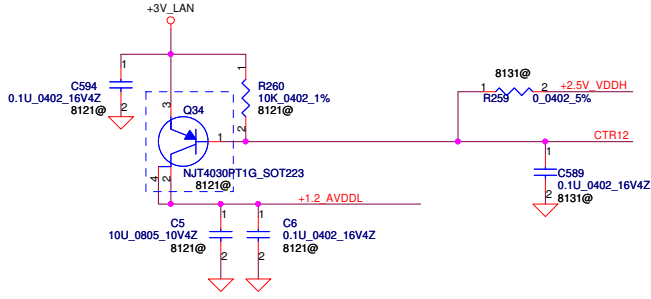
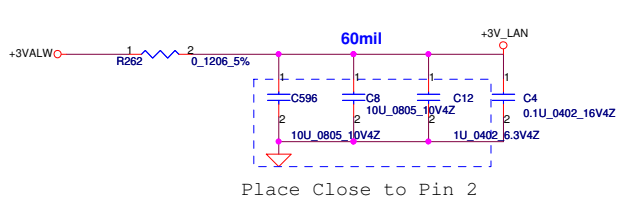


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Size B	Document Number	KBLG0 LA-4921P		Rev	0.1
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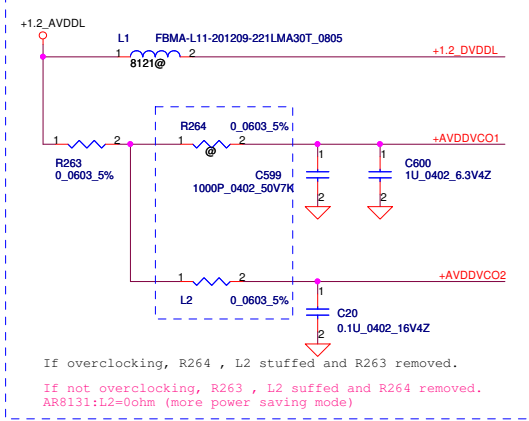
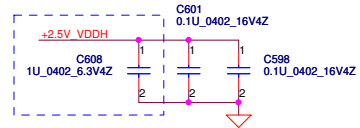




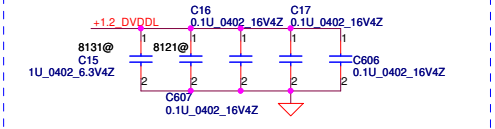
Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	RTS5159 / (JMB385) card reader	
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				Custom	0.1
				KBLG0 LA-4921P	
				Date:	Thursday, February 19, 2009
				Sheet	33 of 57



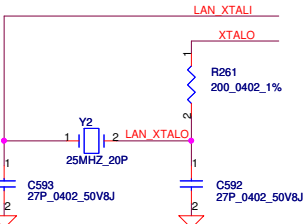
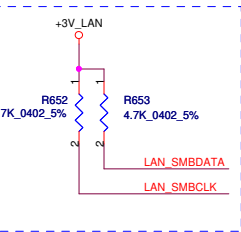
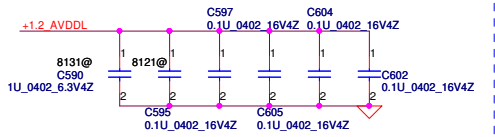
Place Close to Pin15、19、25  
C608 close to Pin15



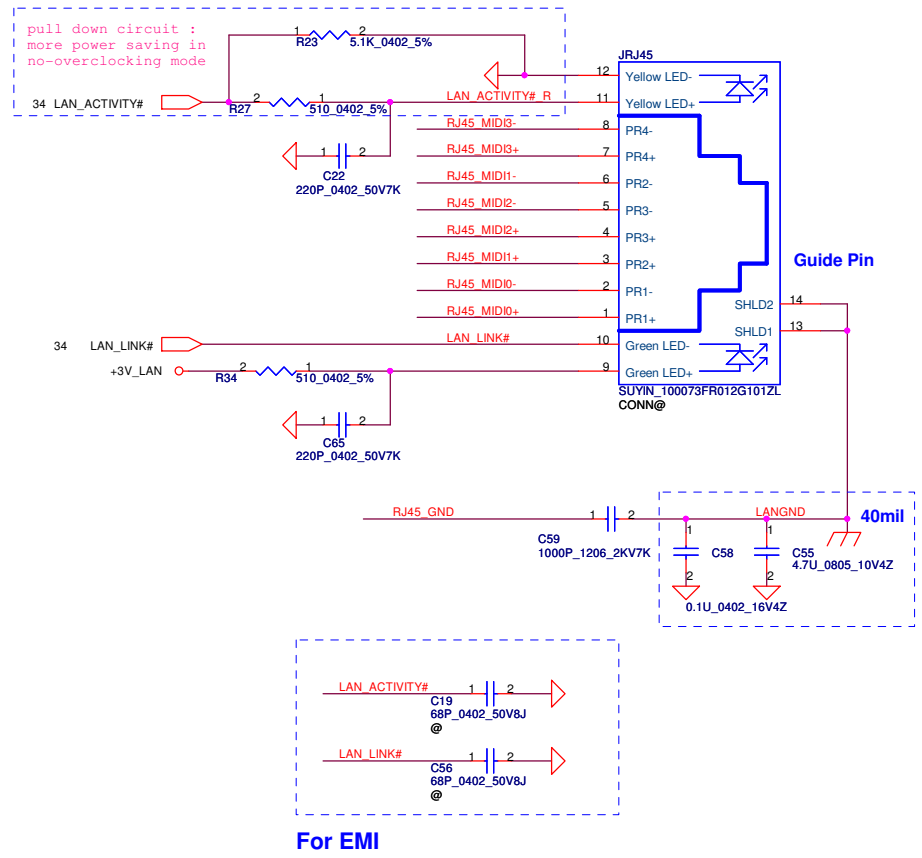
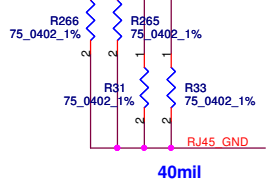
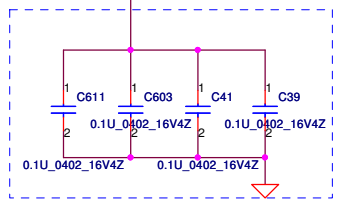
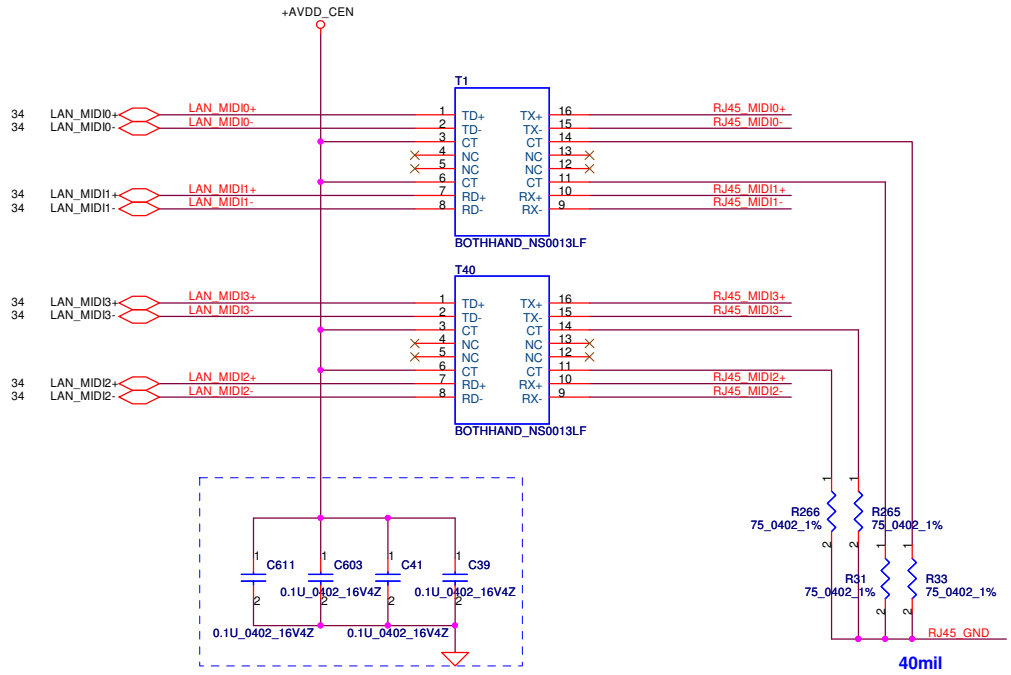
Place Close to Pin 28、32、45、46  
C15 and C607 close to Pin46  
C16 close to Pin45



Place Close to Pin8、16、22、36、39  
C590 and C595 close to Pin8

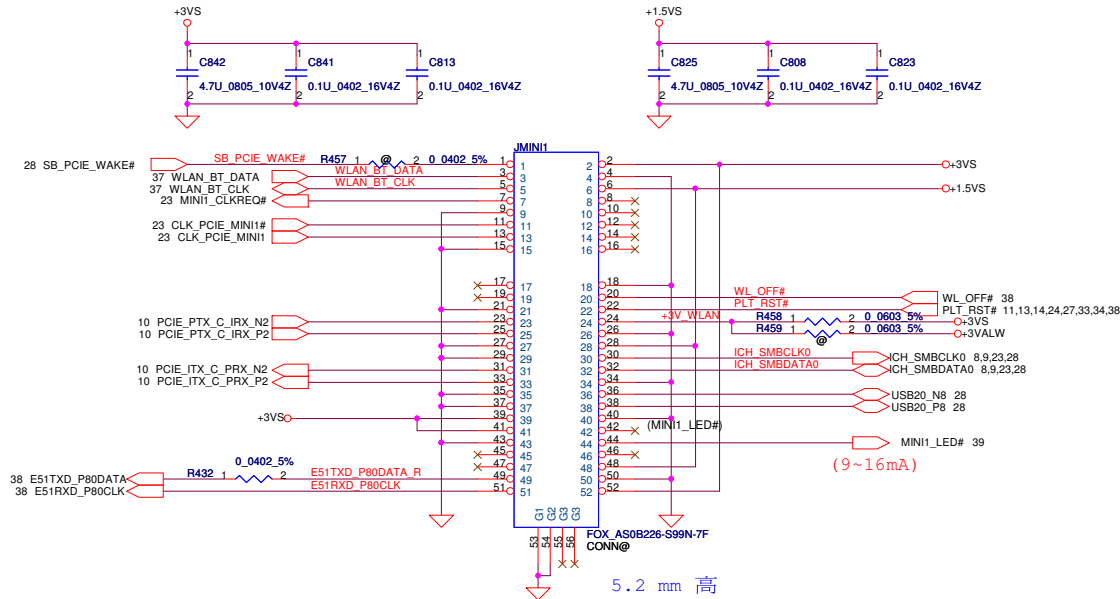


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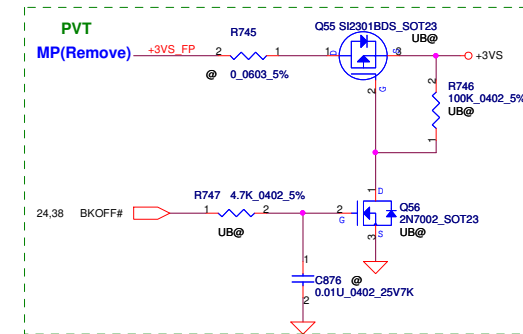
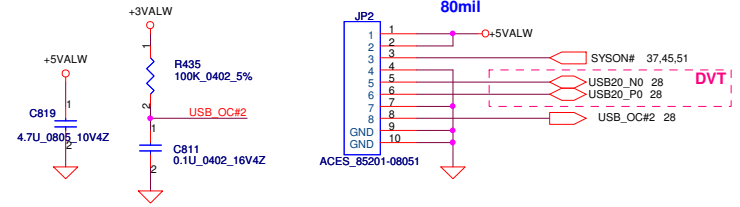
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
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Size B	Document Number	KBLG0 LA-4921P		Rev	0.1
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### For Wireless LAN

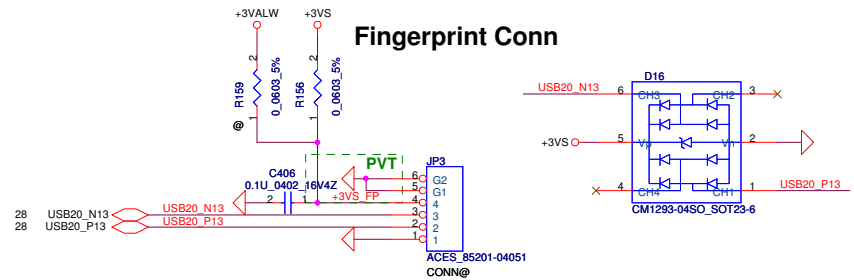


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

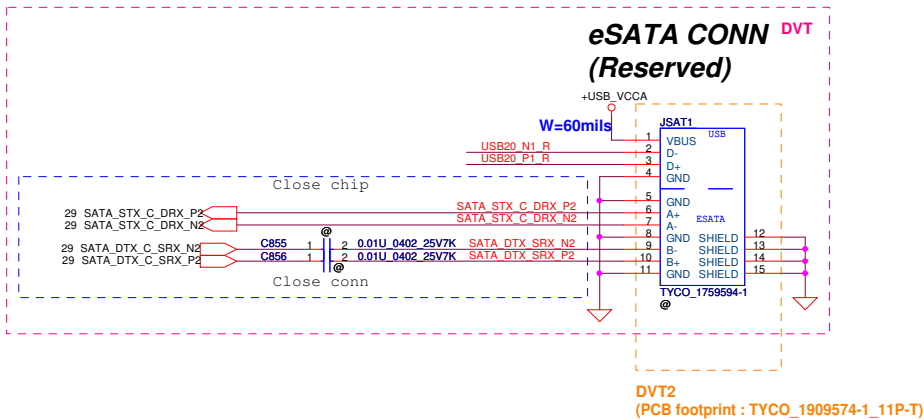
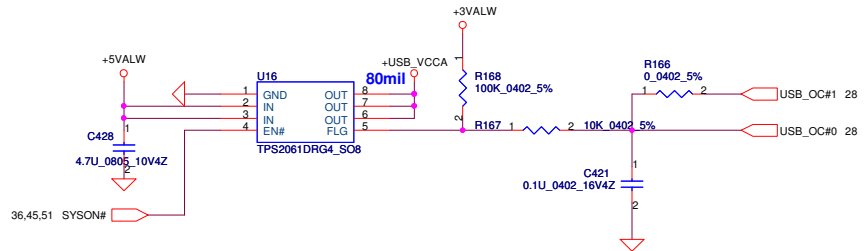
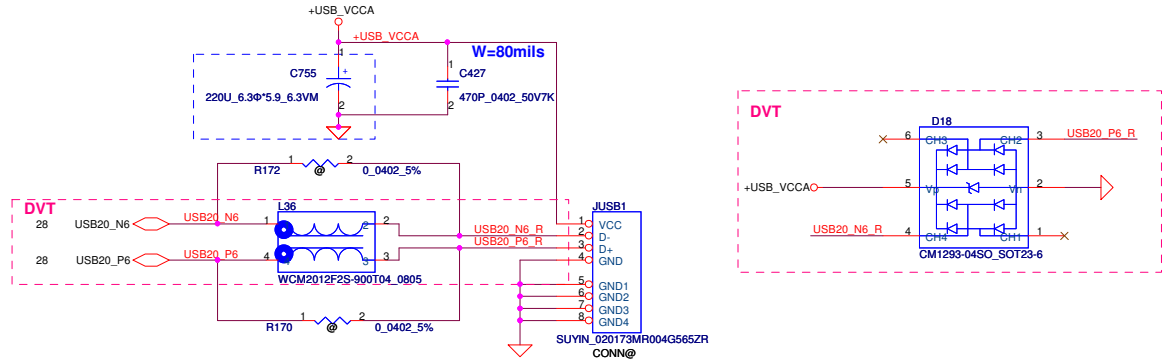
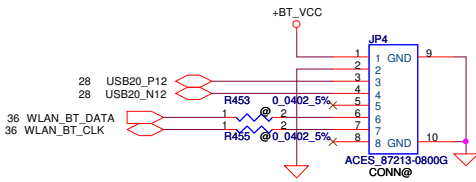
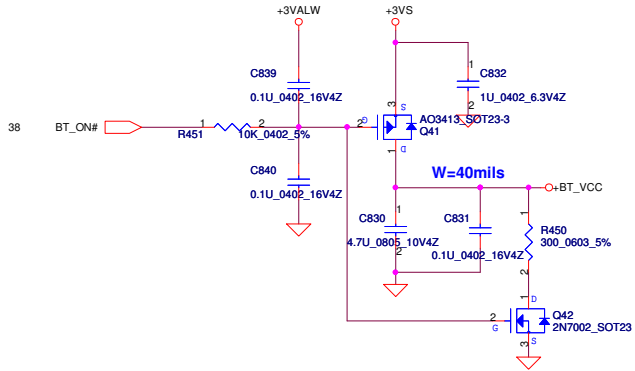
### To USB/B Connector



### Fingerprint Conn

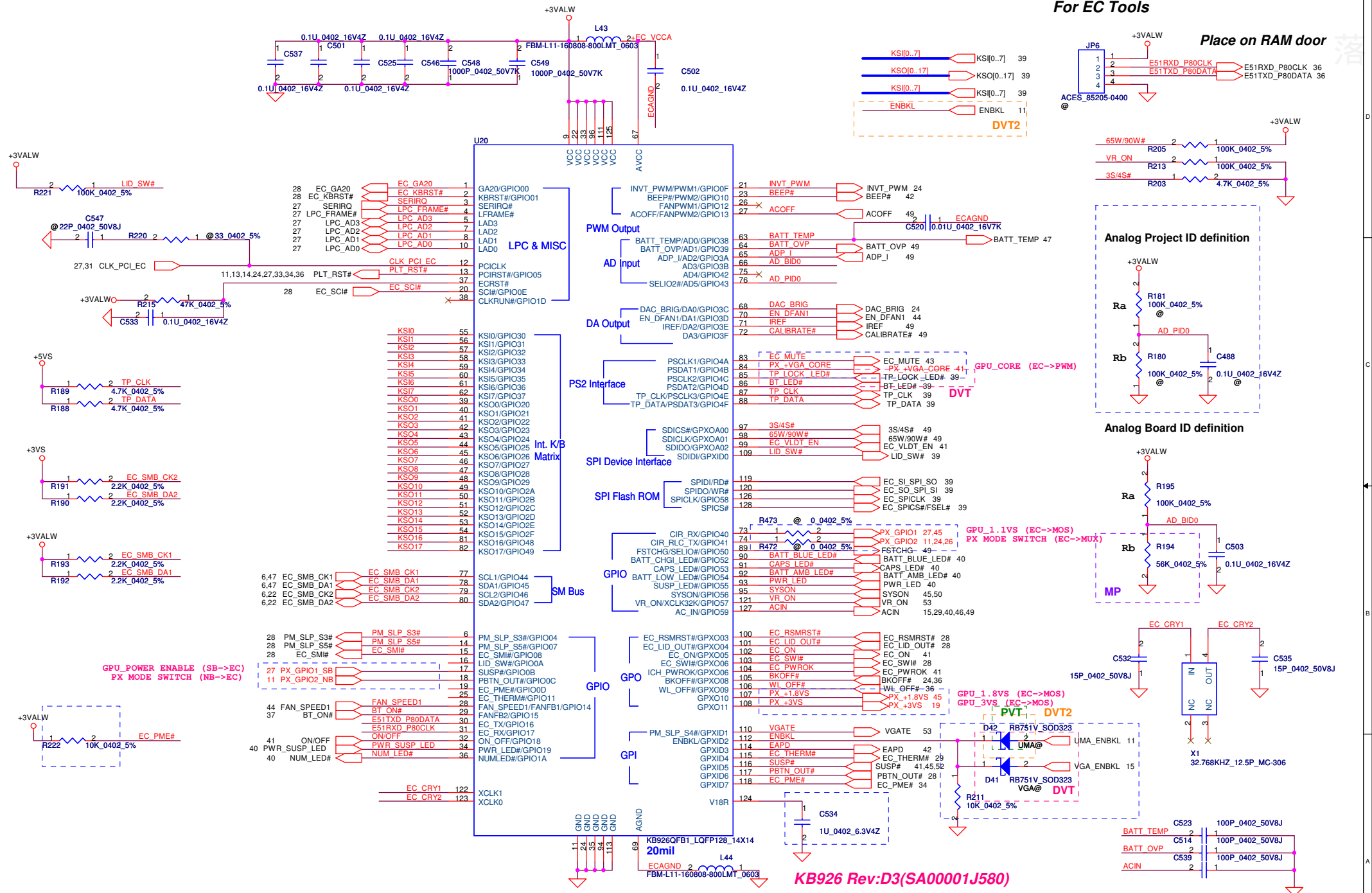


# Bluetooth Conn.



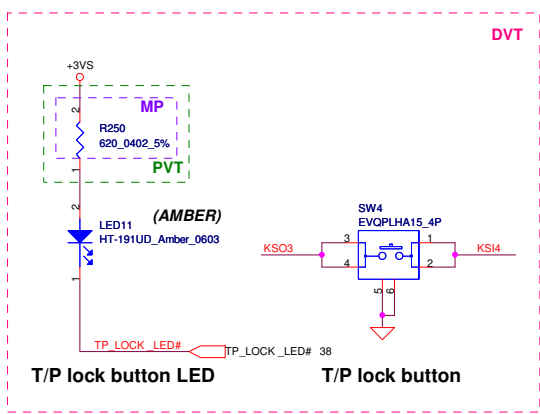
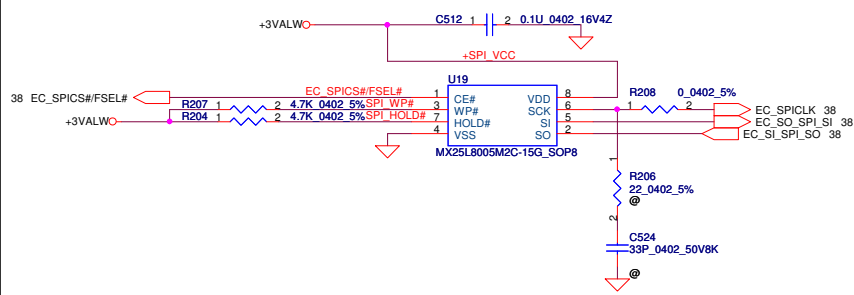
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title		
				Bluetooth / Int USB x2 /eSATA		
				Size	Document Number	Rev
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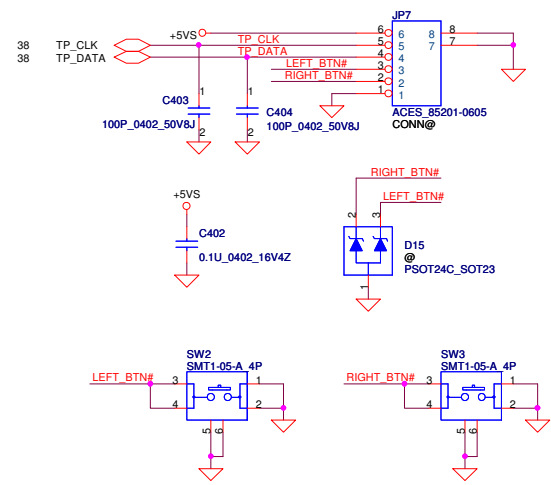


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		B	KBLG0 LA-4921P	0.1	
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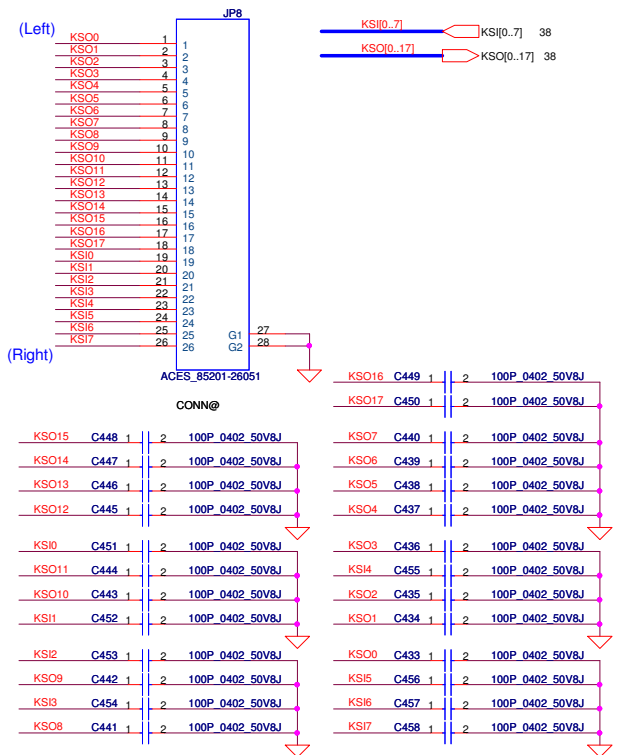
### BIOS(SYS / EC / VGA)



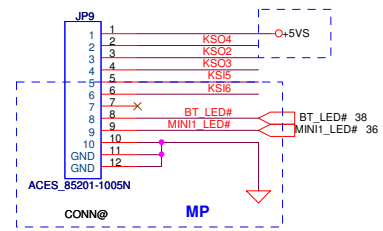
### To TP/B Conn.



### INT\_KBD Conn.

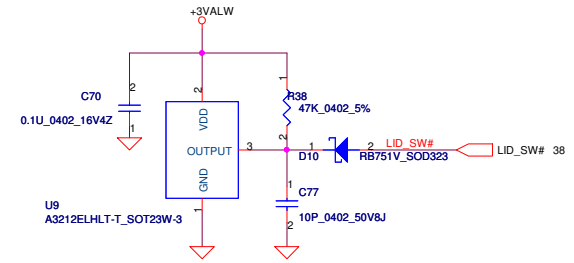


### To FUN/B Conn (10PIN)

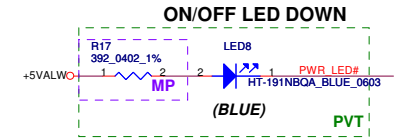
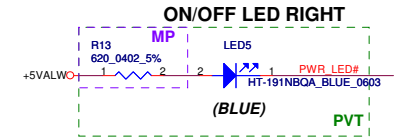
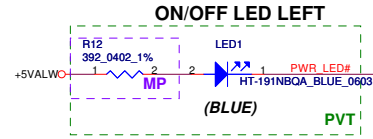
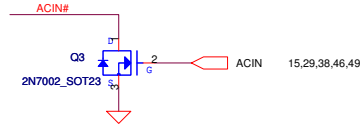
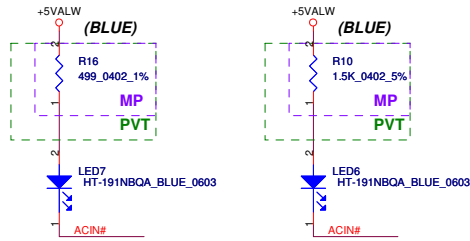


	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

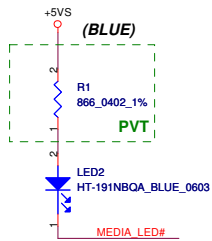
### Lid Switch (Hall Effect Switch)



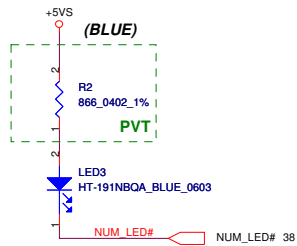
### Enlightener LED



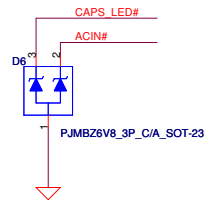
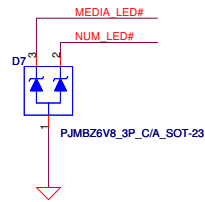
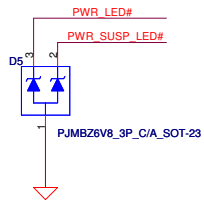
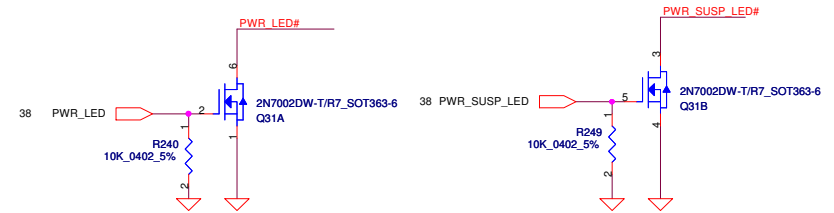
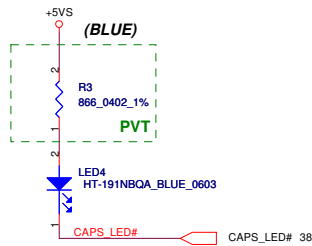
### MEDIA\_LED



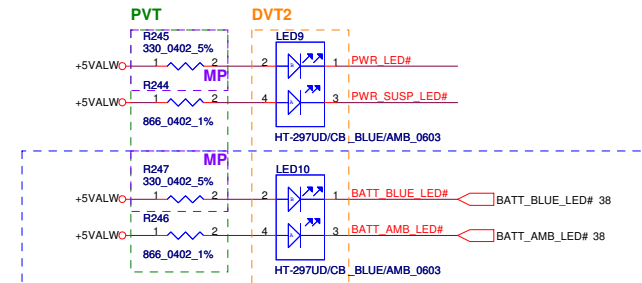
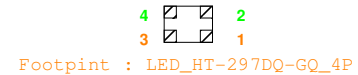
### NUM\_LED



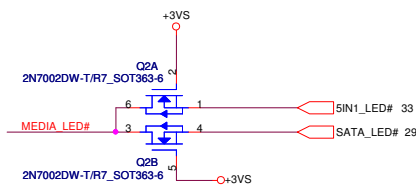
### CAPS\_LED



### Compal Footprint



### BLUE/AMBER

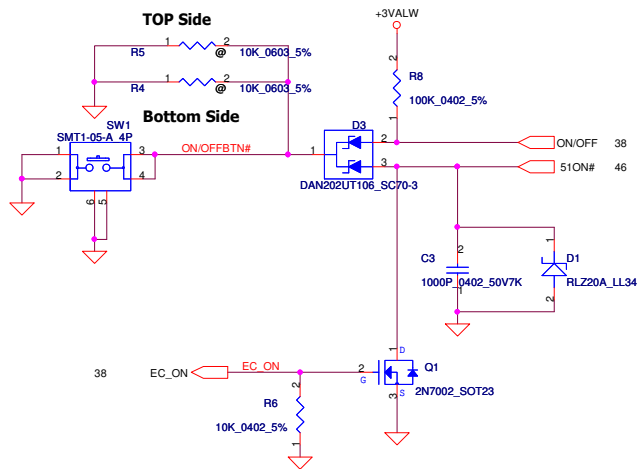


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				Document Number <b>KBLG0 LA-4921P</b>
				Rev 0.1
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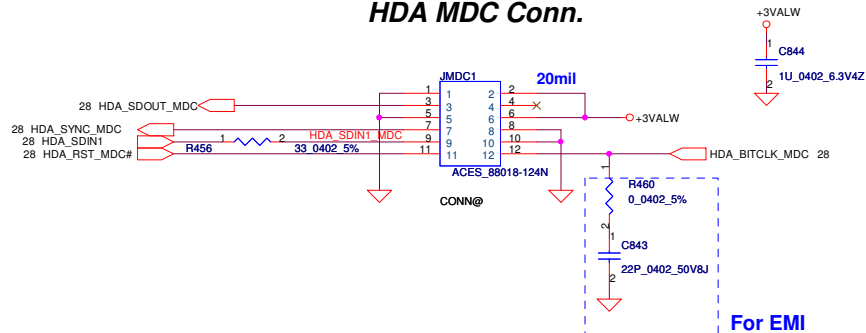


# Power Button

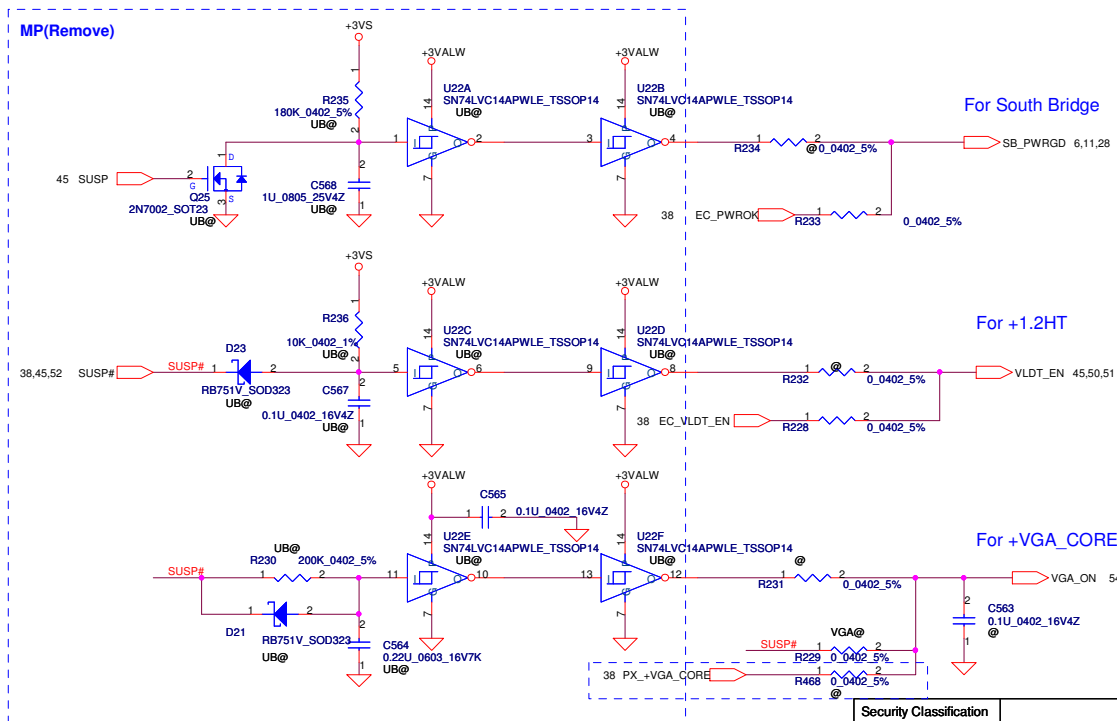
ON/OFF switch



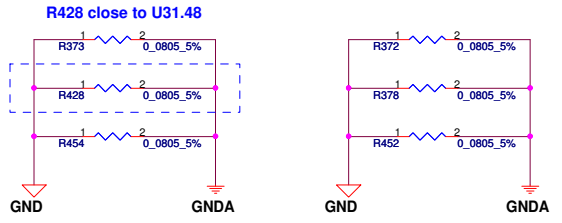
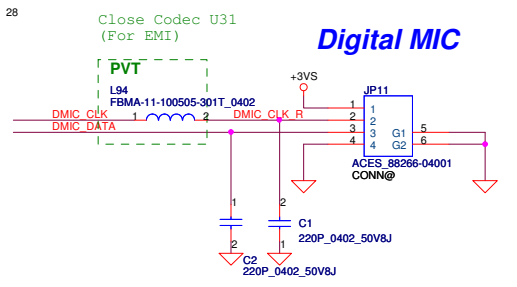
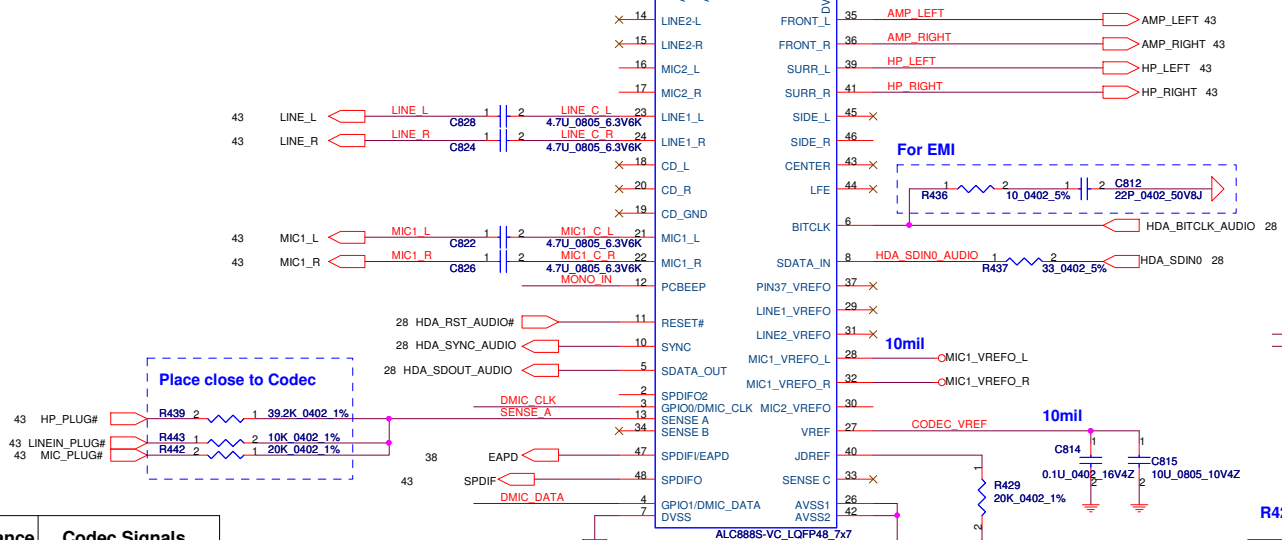
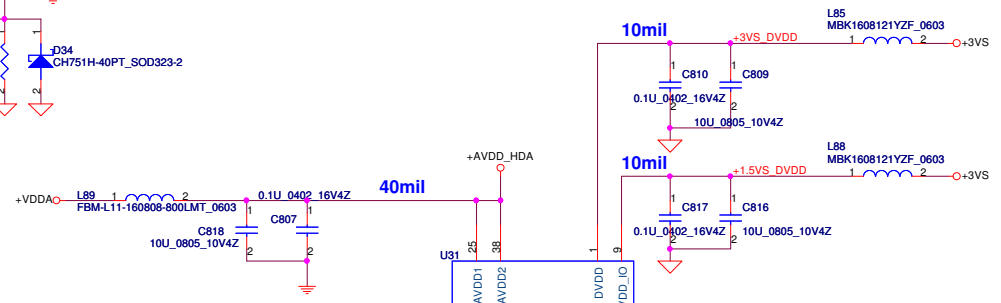
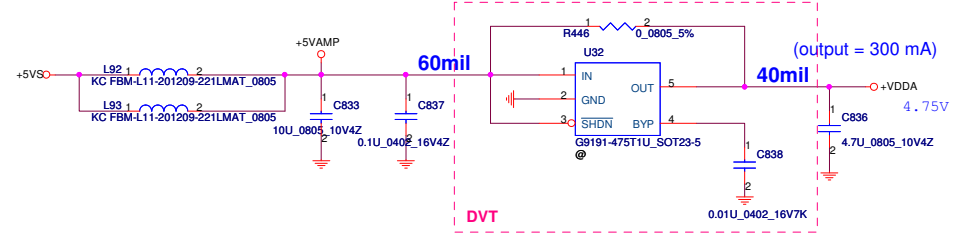
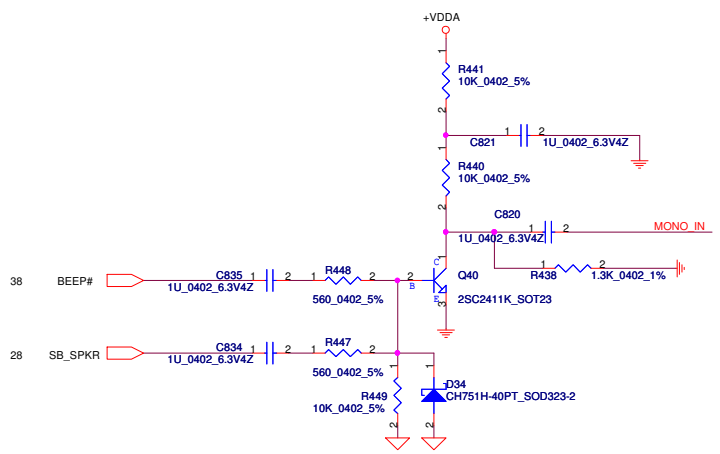
# HDA MDC Conn.



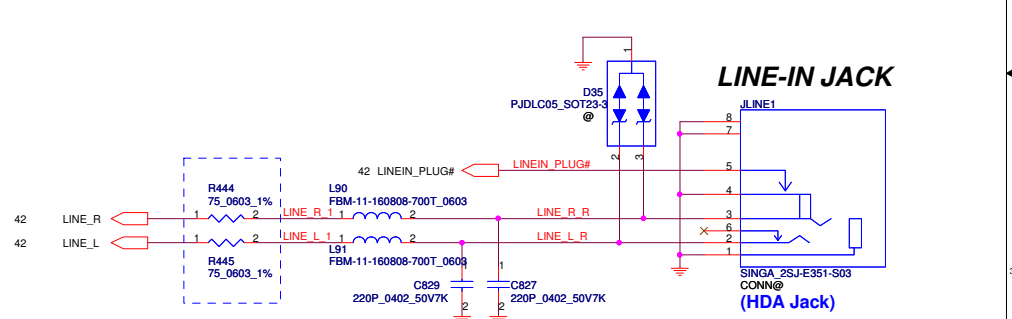
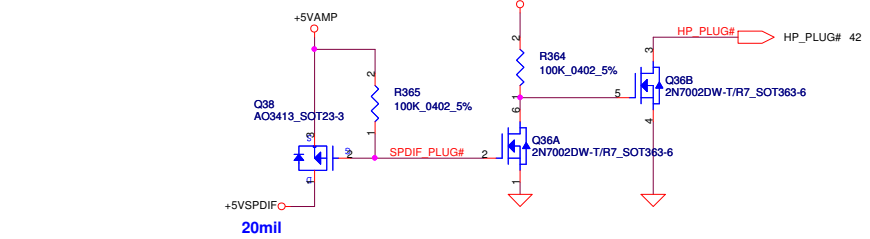
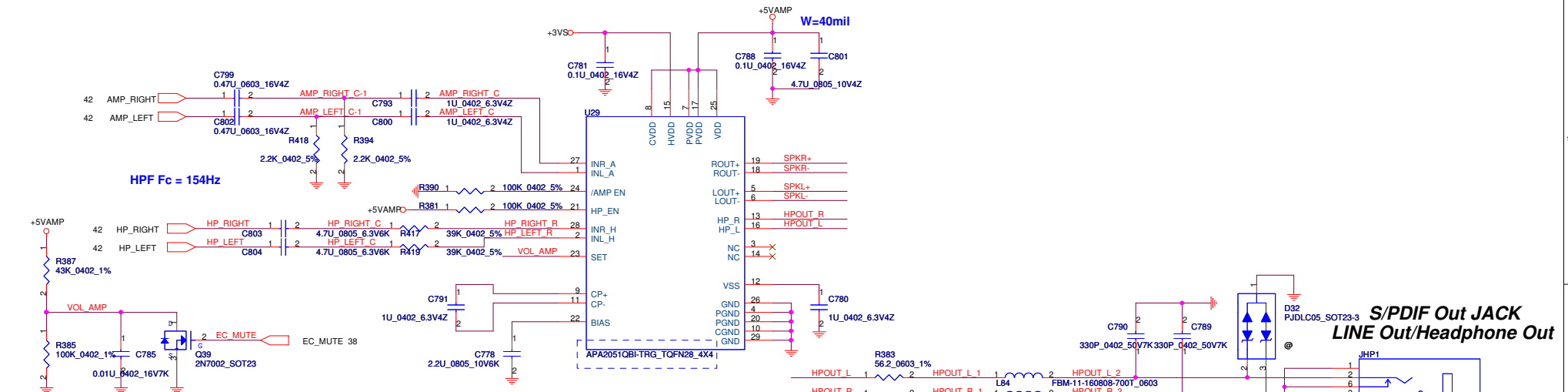
# Power ON Circuit



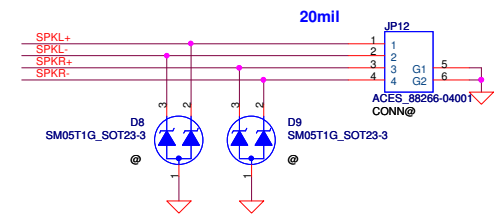
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Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



**Int. Speaker Conn.**

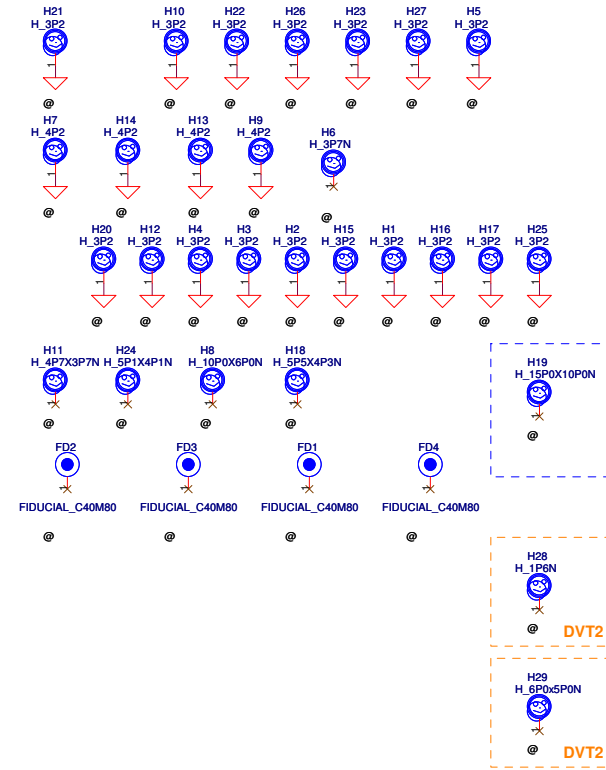
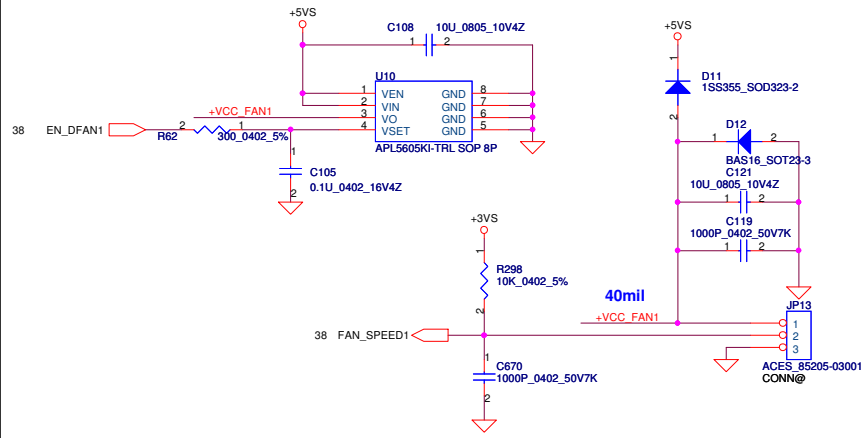


For ESD I/O status:  
 a. input/output mount 75 ohm  
 b. input only mount 1K ohm

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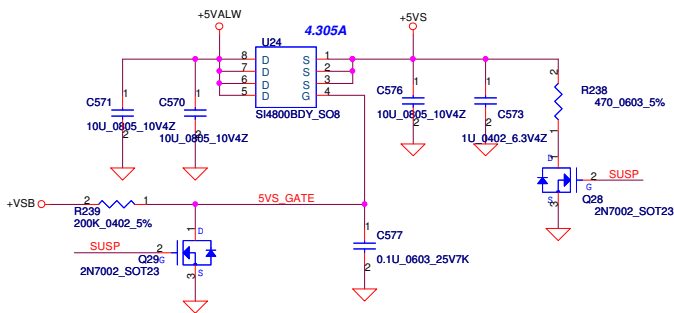
**KBLG0 LA-4921P**

### FAN1 Conn

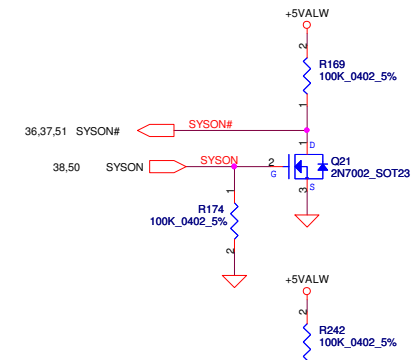
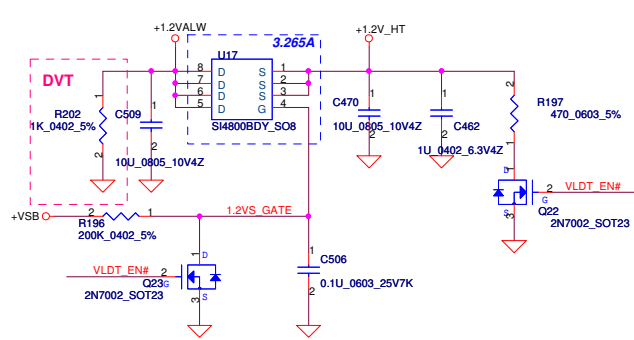


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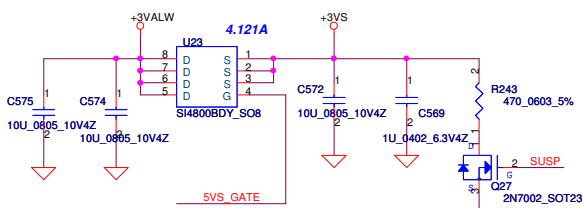
**+5VALW TO +5VS**



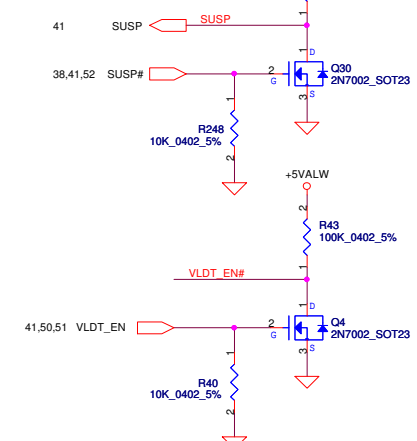
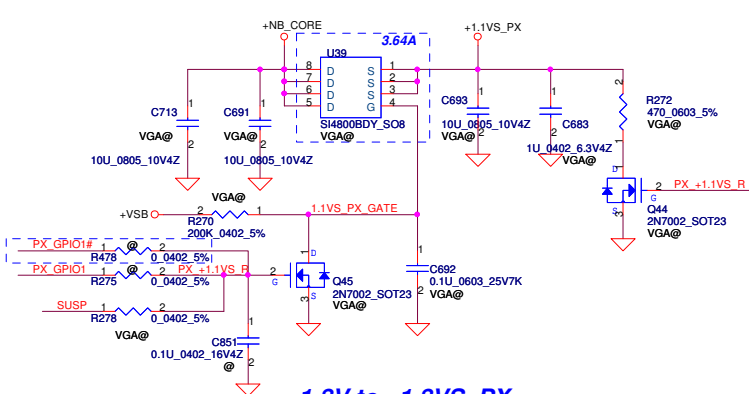
**+1.2VALW TO +1.2V\_HT**



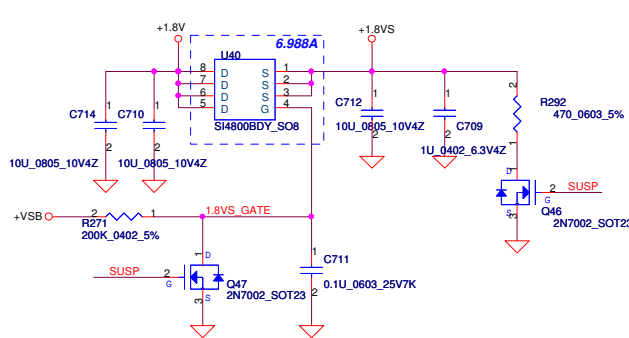
**+3VALW TO +3VS**



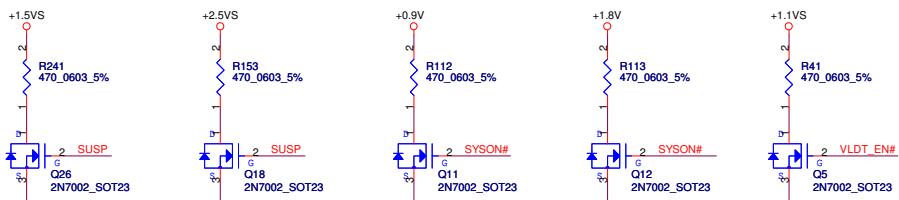
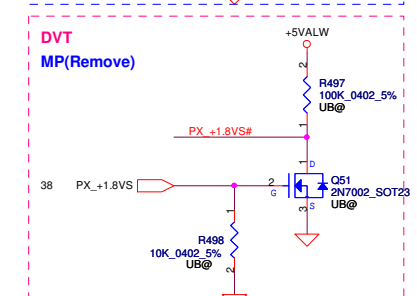
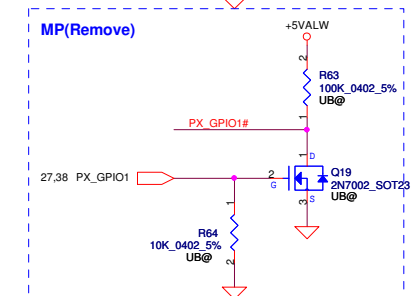
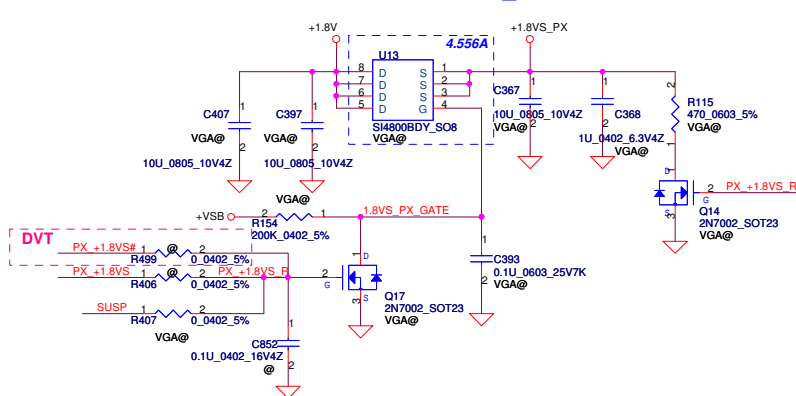
**+NB\_CORE TO +1.1VS\_PX**



**+1.8V to +1.8VS**



**+1.8V to +1.8VS\_PX**

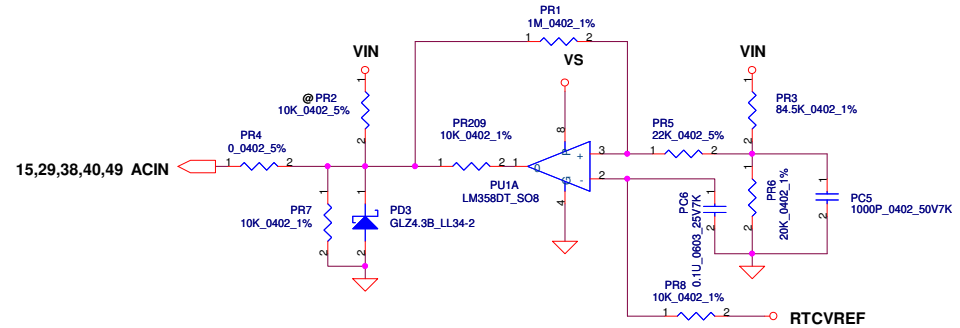
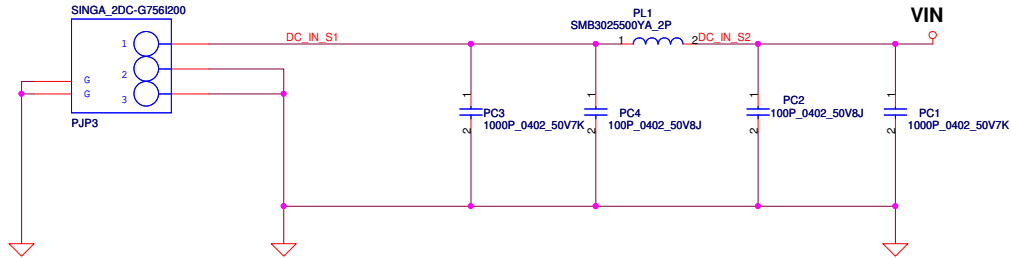


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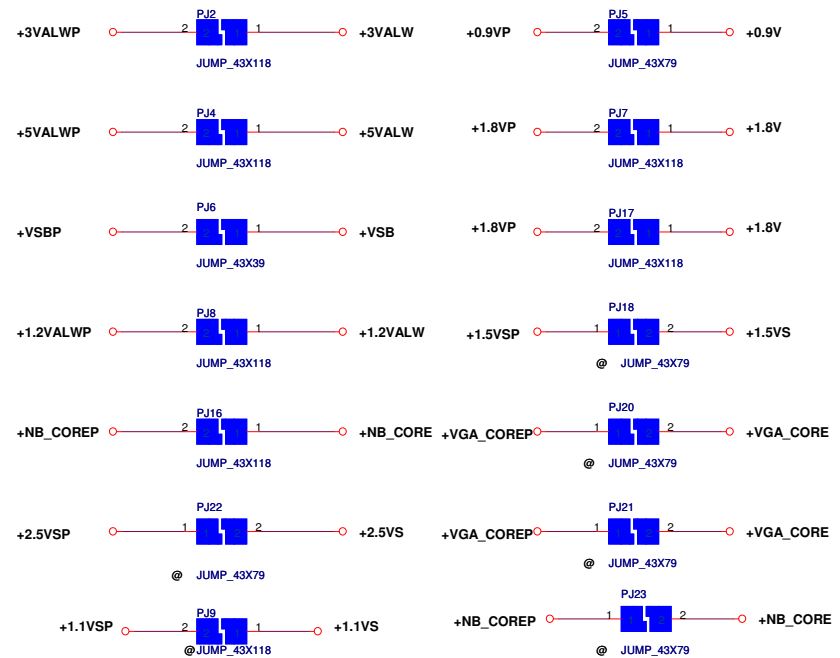
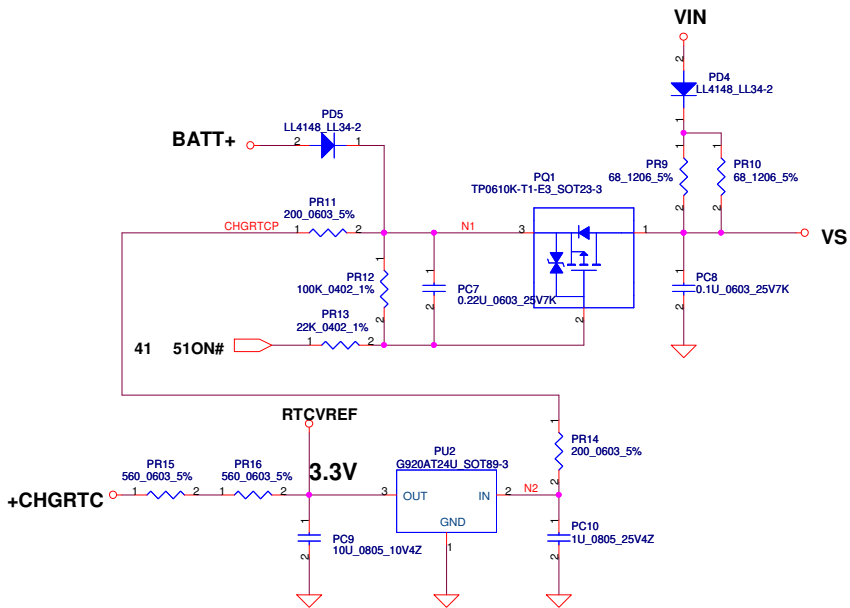
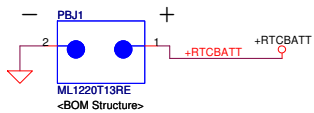
Compal Electronics, Inc.			
DC Interface			
Title	Document Number	Rev	
	KBLG0 LA-4921P	0.1	
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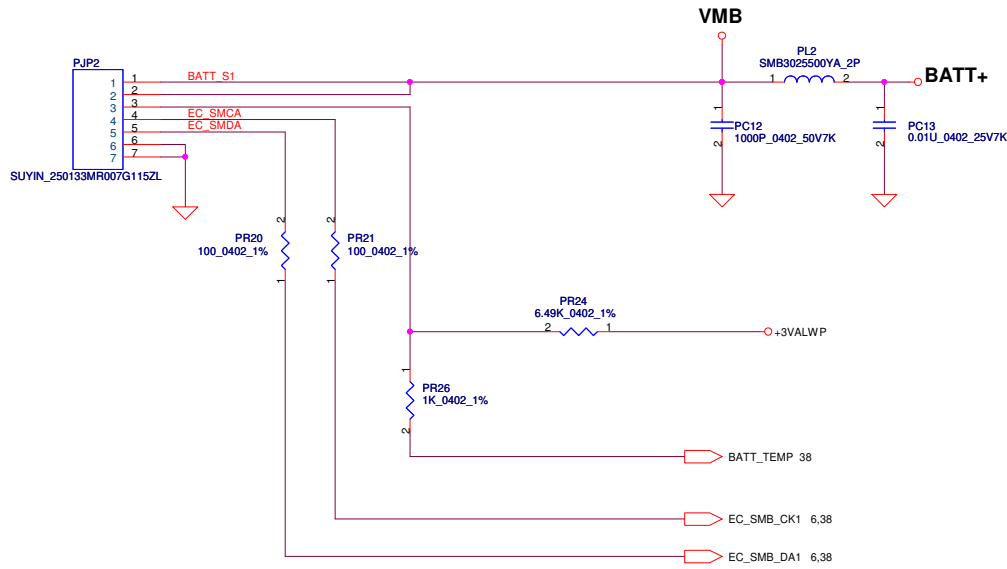
**DC231000500**

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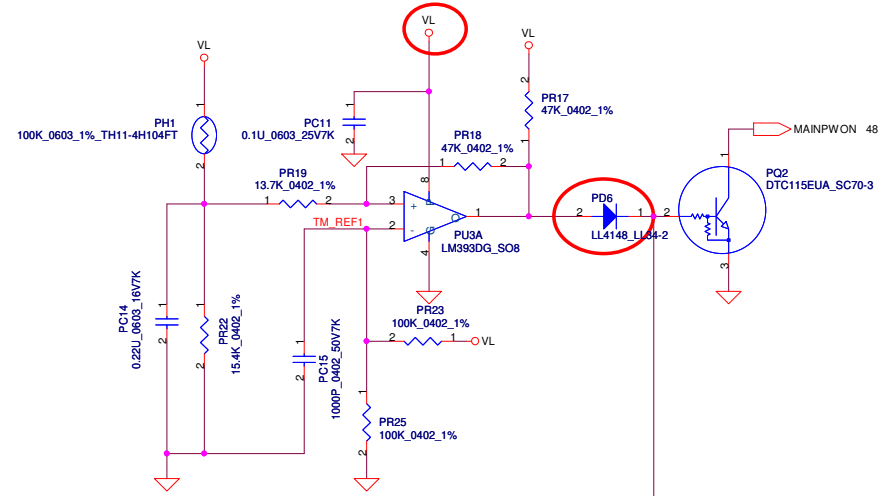


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

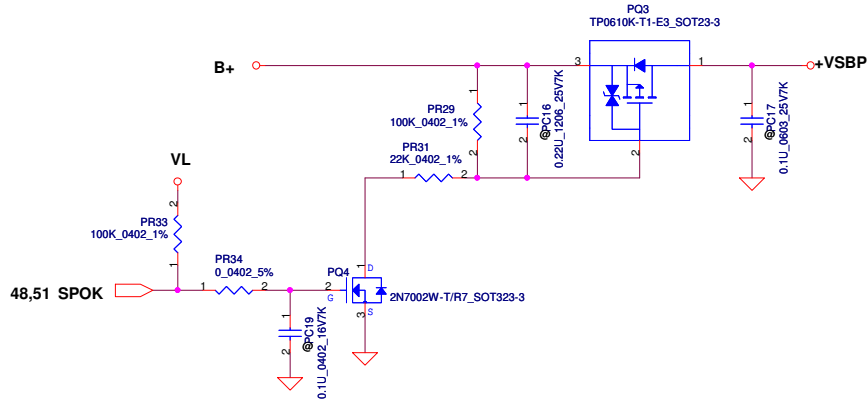
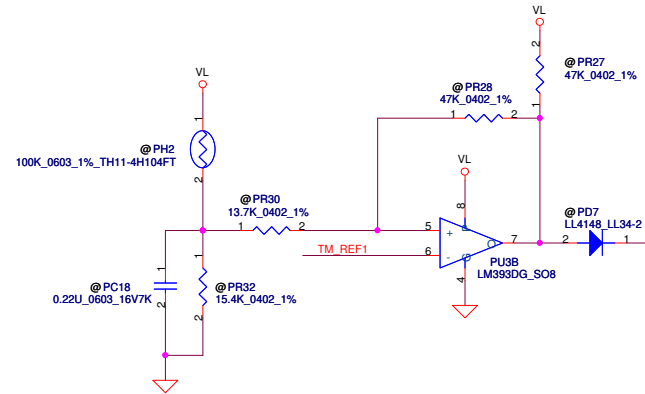




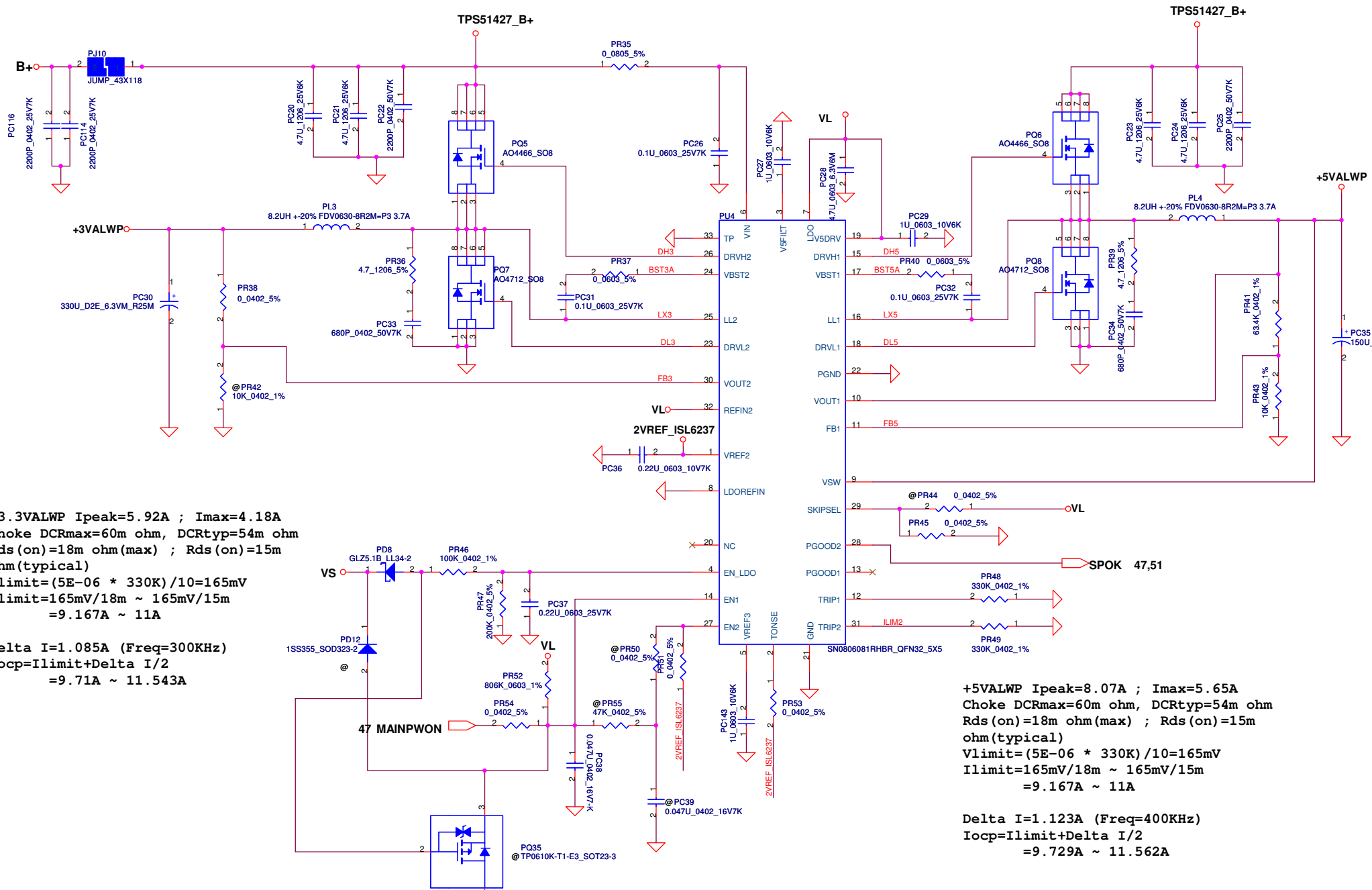
**PH1 under CPU botten side :**  
 CPU thermal protection at 93 degree C  
 Recovery at 57 degree C



**PH2 near Battery CONN :**  
 BAT. thermal protection at 79 degree C  
 Recovery at 47 degree C



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Size	Document Number	Rev		0.1	
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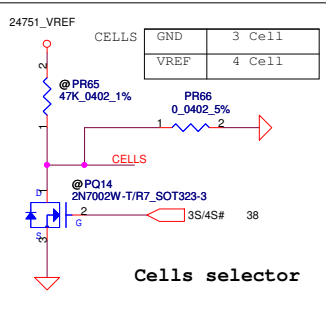
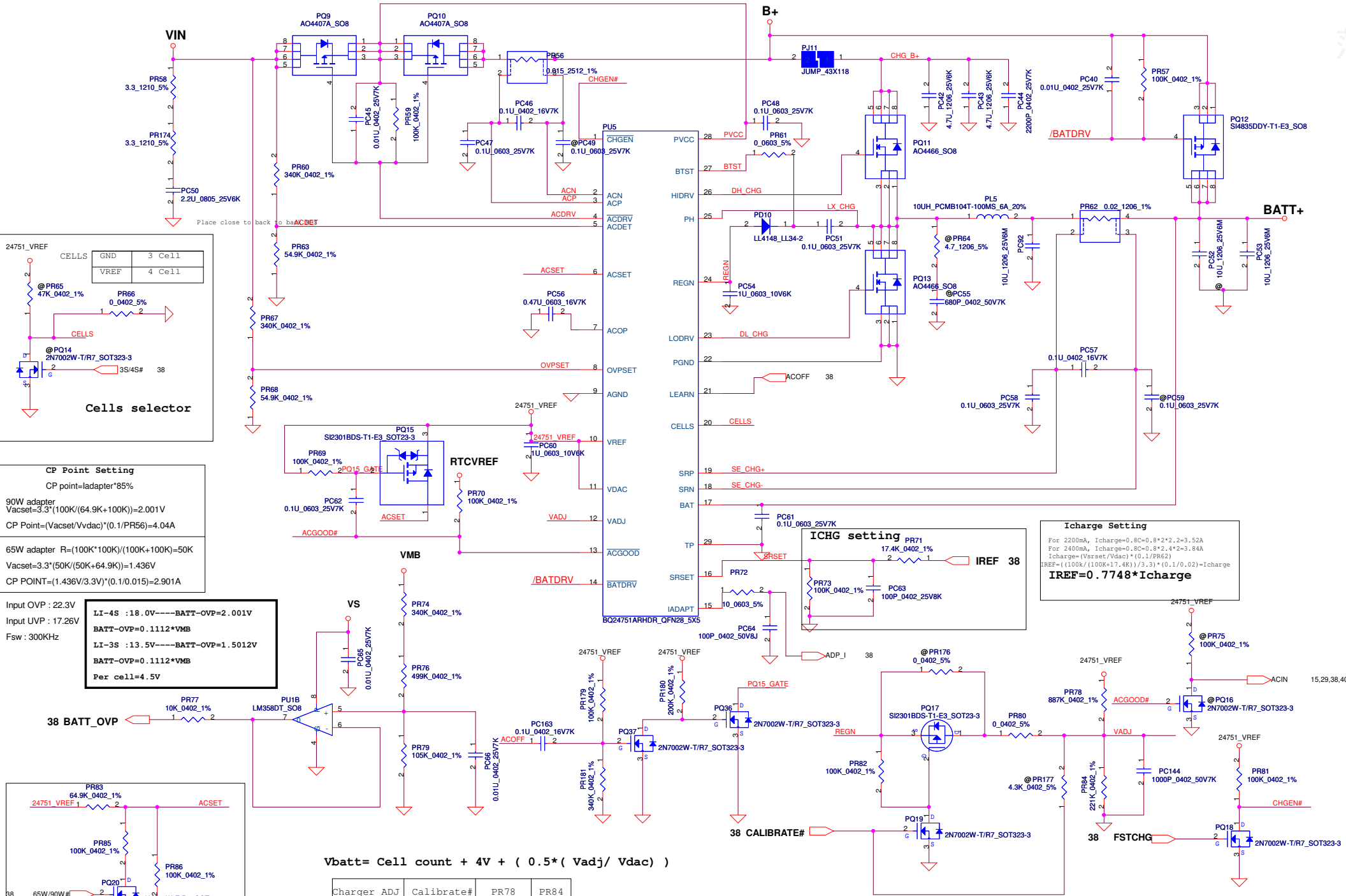


**+3.3VALWP** Ipeak=5.92A ; I<sub>max</sub>=4.18A  
 Choke DCR<sub>max</sub>=60m ohm, DCR<sub>typ</sub>=54m ohm  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>limit</sub>=(5E-06 \* 330K)/10=165mV  
 I<sub>limit</sub>=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
  
 Delta I=1.085A (Freq=300KHz)  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =9.71A ~ 11.543A

**+5VALWP** Ipeak=8.07A ; I<sub>max</sub>=5.65A  
 Choke DCR<sub>max</sub>=60m ohm, DCR<sub>typ</sub>=54m ohm  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>limit</sub>=(5E-06 \* 330K)/10=165mV  
 I<sub>limit</sub>=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
  
 Delta I=1.123A (Freq=400KHz)  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =9.729A ~ 11.562A

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**CP Point Setting**

CP point=ladapler\*85%

90W adapter  
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$   
 $CP\ Point = (V_{acset} / V_{dacc}) \cdot (0.1 / PR56) = 4.04A$

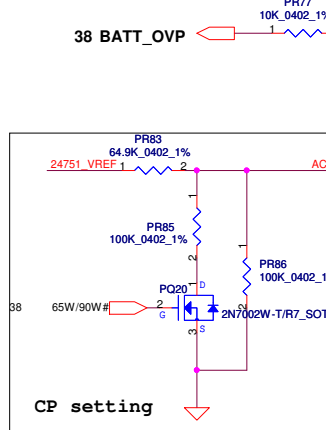
65W adapter  $R = (100K \cdot 100K) / (100K + 100K) = 50K$   
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$   
 $CP\ POINT = (1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V  
 BATT-OVP=0.1112\*VMB

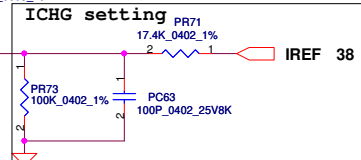
LI-3S : 13.5V----BATT-OVP=1.5012V  
 BATT-OVP=0.1112\*VMB

Per cell=4.5V



$$V_{batt} = \text{Cell count} + 4V + (0.5 \cdot (V_{adj} / V_{dacc}))$$

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V(1.32)	H	@	@



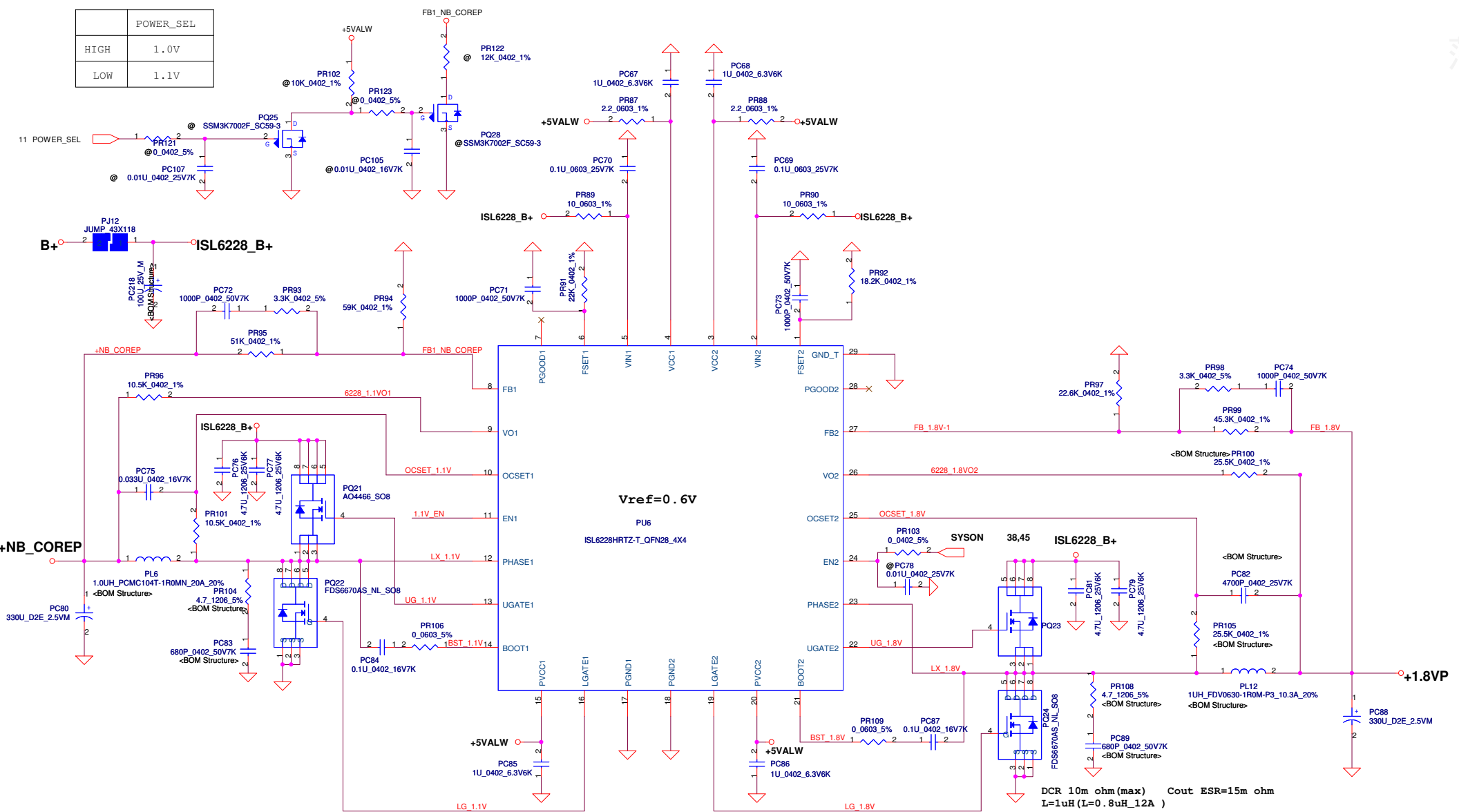
**Icharge Setting**

For 2200mA, Icharge=0.8C=0.8\*2\*2.2=3.52A  
 For 2400mA, Icharge=0.8C=0.8\*2.4\*2=3.84A  
 $I_{charge} = (V_{acset} / V_{dacc}) \cdot (0.1 / PR62)$   
 $I_{REF} = (100K / (100K + 17.4K)) / 3.3 \cdot (0.1 / 0.02) = I_{charge}$   
**IREF=0.7748\*Icharge**

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Compal Electronics, Inc.			
<b>CHARGER</b>			
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	POWER_SEL
HIGH	1.0V
LOW	1.1V

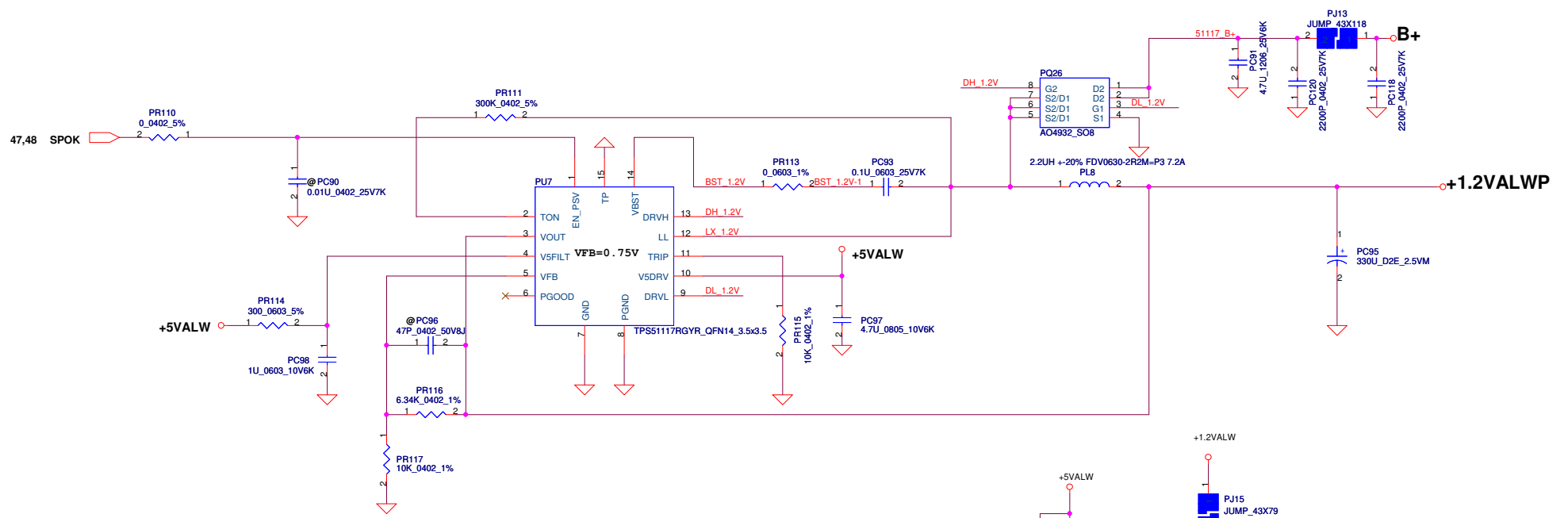


DCR3.5m ohm(max) Cout ESR=15m ohm  
 NB\_CORE (1.1VSP) OCP Setting  
 $Fsw=1/1.5E-10*22k=303K$   
 $Vo=Vref*((PR95+PR94)/PR94)$   
 $Ipeak=17.53A, Imax=12.27A$   
 $Iocp=17.53*1.2=21.04A$   
 $\Delta I=3.838A$   
 $Iocp*DCR=(Rocset*9.5uA)=(21.04+1.92)*3.5m; Roset=8.44k$   
 now chose Roset=8.66k  
 $Csen=L/(DCR*Roset)=0.9uH/(3.5m*8.44k); Csen=0.031uF$   
 now chose Csen=0.033uF  
 $Iocp\_min=(8.66K*9.5uA)/(3.5m\ ohm*1.3)=18.08A$   
 $Iocp\_max=(8.66*10.5uA)/(3m\ ohm*1.3)=23.32A$



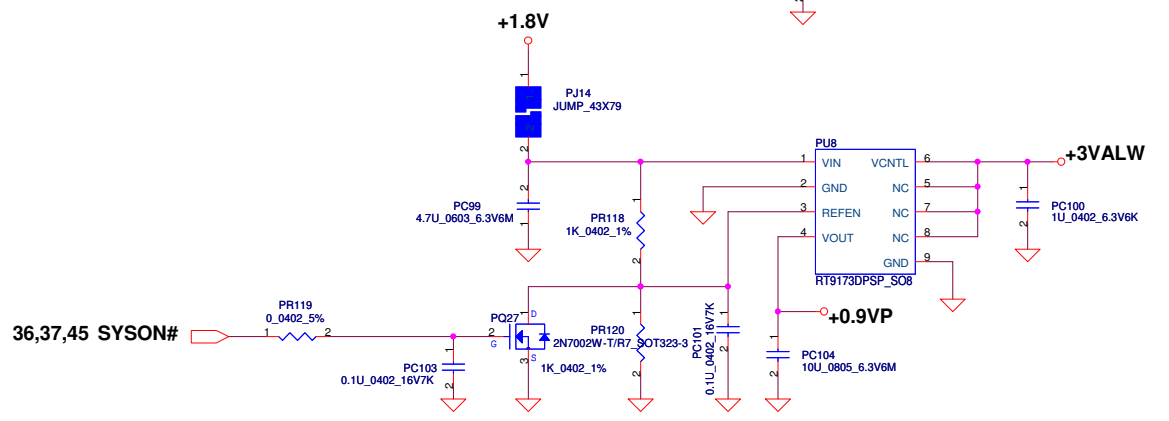
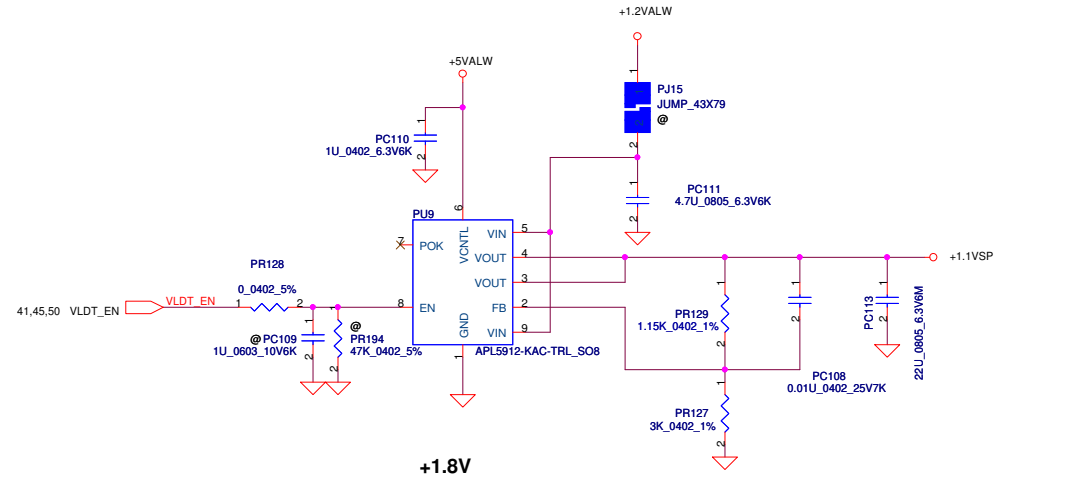
DCR 10m ohm(max) Cout ESR=15m ohm  
 $L=1uH(L=0.8uH_{12A})$   
 $1.8VP\ Ipeak=15.51A, Imax=10.86A$   
 $Fsw=1/1.5E-10*18.2k=366K$   
 $Vo=Vref*((PR97+PR99)/PR97)$   
 $Ipeak=15.51A, Imax=10.86A$   
 $Iocp=15.51*1.2=18.61A$   
 $\Delta I=5.565A$   
 $Iocp*DCR=(Rocset*9.5uA)=(18.61+2.7825)*10m; Roset=22.5k$   
 now chose Roset=22.6k  
 $Csen=L/(DCR*Roset)=0.8uH/(10m*22.5k); Csen=3.56nF$   
 now chose Csen=3300pF  
 $Iocp\_min=(22.6K*9.5uA)/(10m\ ohm*1.3)=16.52A$   
 $Iocp\_max=(22.6*10.5uA)/(10m\ ohm)=23.73A$

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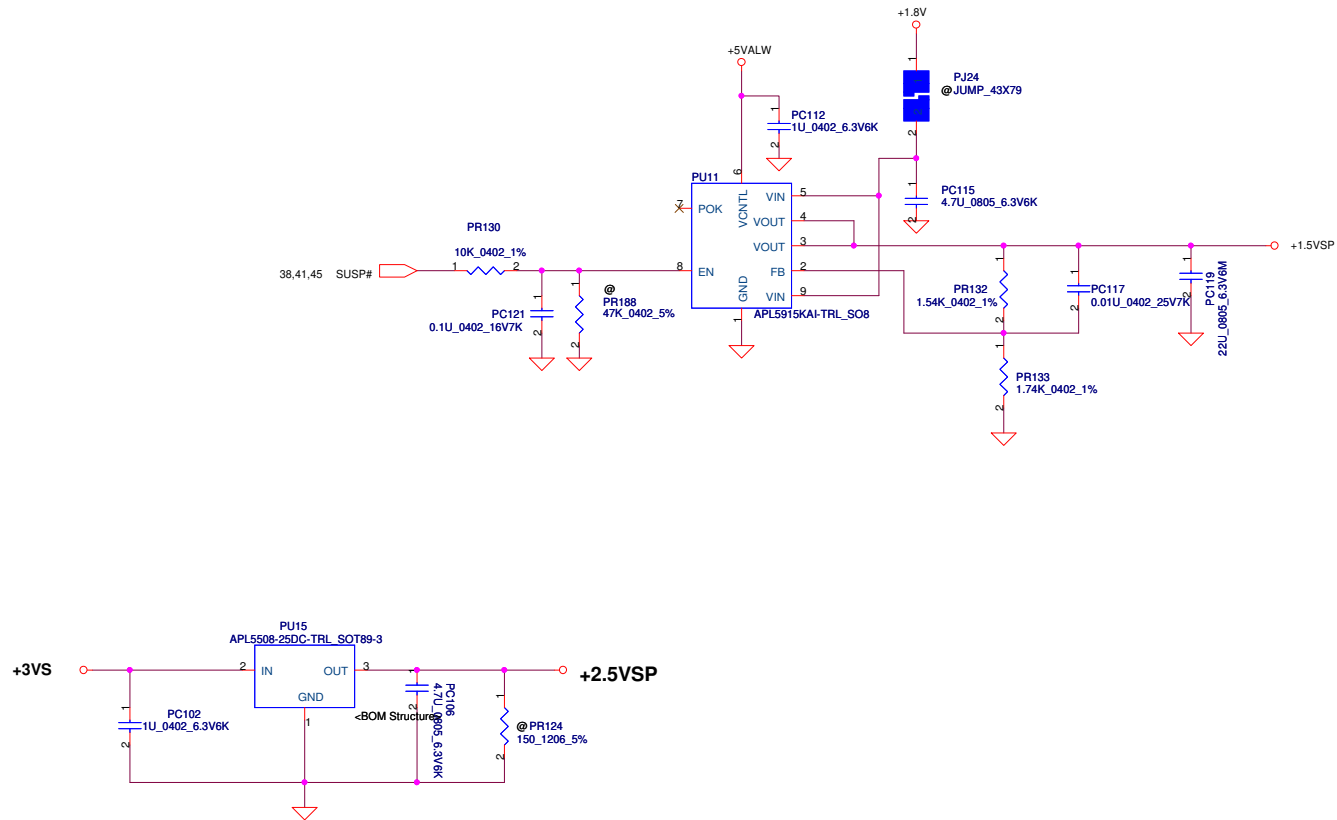


VFB=0.75V  
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / v_{in} + 50ns = 3.2E-7$   
 $F_{sw} = 200KHz$

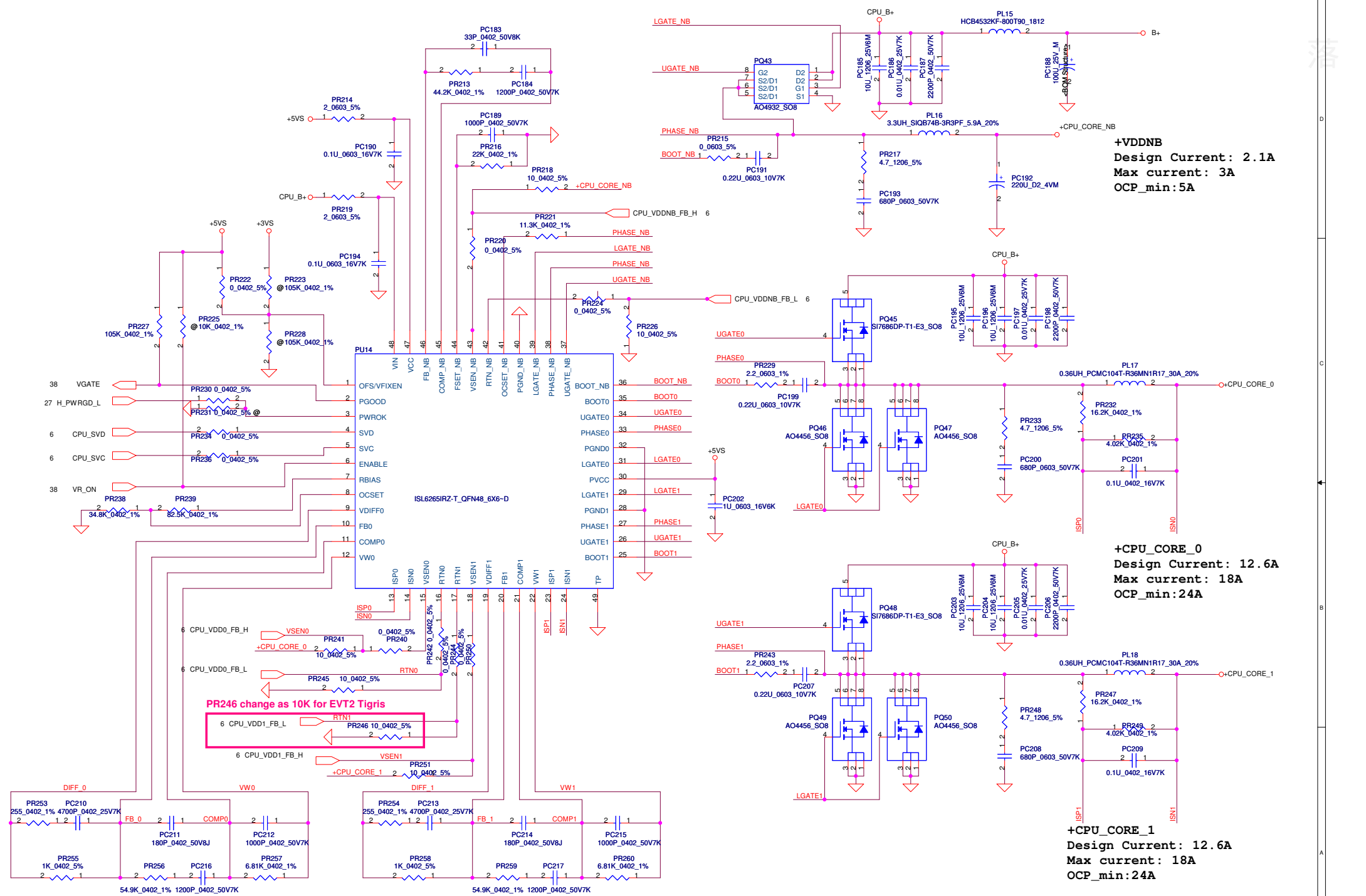
$C_{out} ESR = 15m\ \Omega$   
 $I_{peak} = 3.58A, I_{max} = 2.51A$   
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw}) = 2.59A$   
 $\Rightarrow 1/2 \Delta I = 1.295A$   
 $V_{trip} = R_{trip} * I_{0uA} = 10K * 10uA = 0.1V$   
 $I_{ocp\_min} = V_{trip} / R_{dsonmax} * 1.4 + 1.295A$   
 $= 0.1 / (0.0196 * 1.4) + 1.295 = 3.644A + 1.295A = 4.939A$   
 $I_{ocp\_max} = (0.1 / (0.016 * 1.2)) + 1.1.295A = 5.208A + 1.295A = 6.503A$   
 $I_{ocp} = 6.503A \sim 4.939A$



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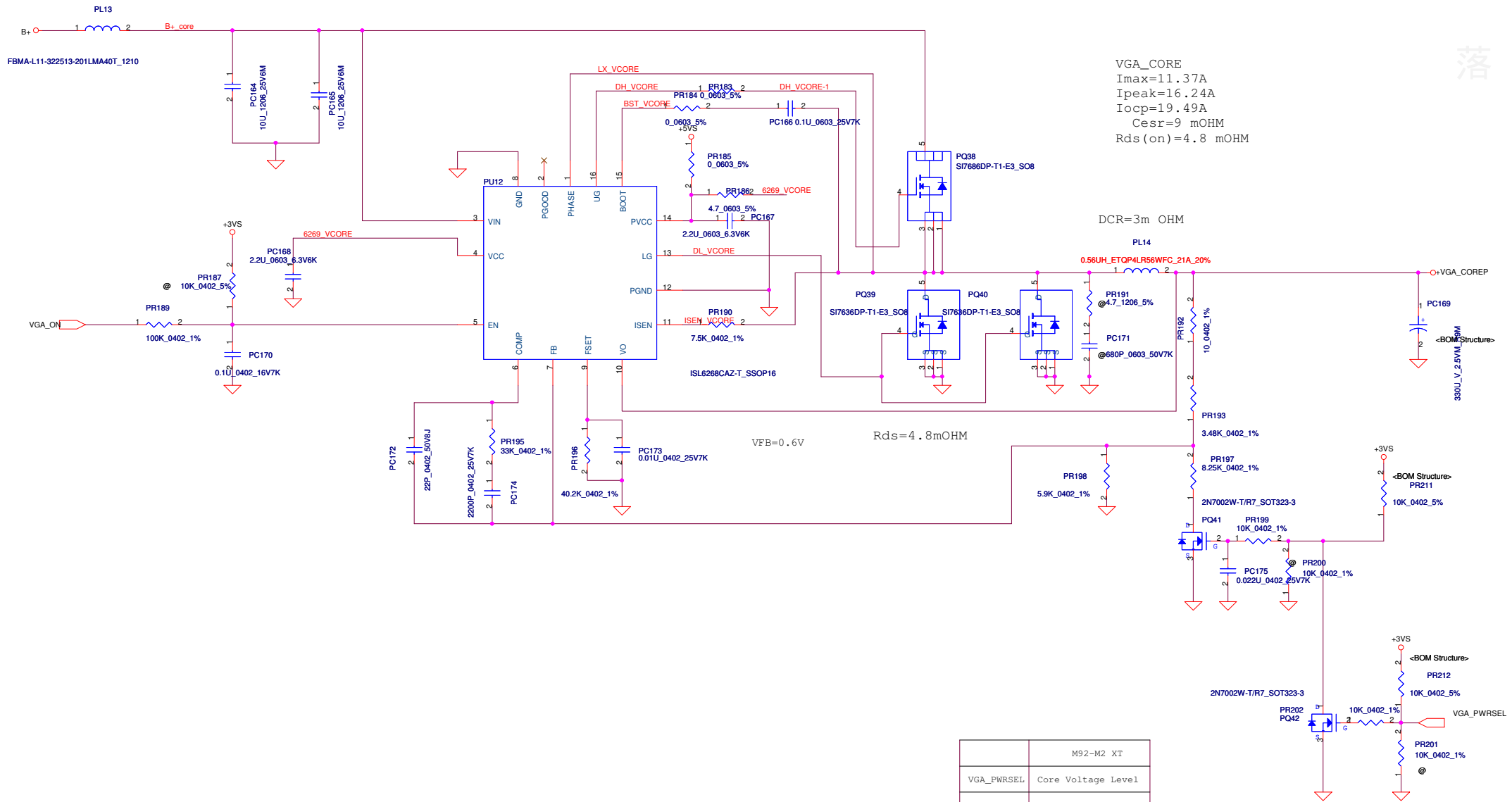


**+VDDNB**  
 Design Current: 2.1A  
 Max current: 3A  
 OCP\_min: 5A

**+CPU\_CORE\_0**  
 Design Current: 12.6A  
 Max current: 18A  
 OCP\_min: 24A

**+CPU\_CORE\_1**  
 Design Current: 12.6A  
 Max current: 18A  
 OCP\_min: 24A

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Issued Date	2008/04/16	Deciphered Date	2009/04/16	+CPU_CORE
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT

12  
13  
14  
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Rev Code

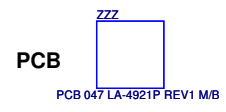
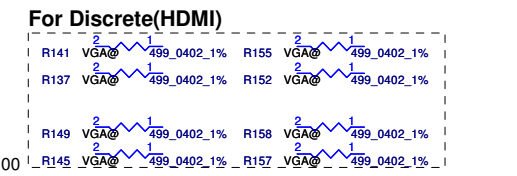
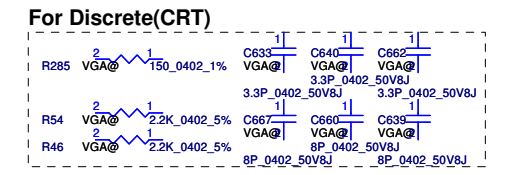
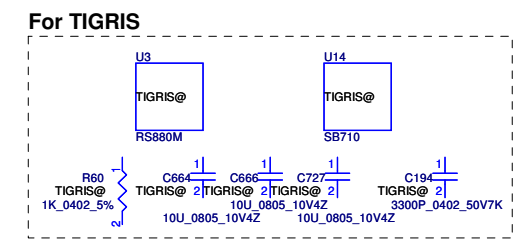
PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor	Reserved EC SMBUS1 due to +3VS leakage when S3 entry with SMBUS2
	P.8	Add C174/C175/C176 (0.1u_0402)	EMI request
	P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@	BOM error
	P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)	UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0
	P.11	Reserve R490(0ohm_0402)	NA
	P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@	For DIS +1.1VS power source from fixed +NB_CORE
	P.22	Remove VRAM Samsung(Q-die) & Qimonda type	Customer request
	P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@	Separately as DIS sku only & UMA sku only
	P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@	For DIS sku only
	P.24	Reserve Q52/R501/R502/R503	Reserve for UMA sku white screen flash when boot issue check
	P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)	DFX request
	P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506	NA (Just no need to modify)
	P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@	Separately as DIS sku only & UMA sku only
	P.27	Add R496 with @ & R476/R482 with @	NA
	P.28	Add R509 with VGA@ & R510 with UMA@	Reserve SKU ID for SW even SW check device ID instead currently
	P.29	Reserve C862/C863/C855/C856	Reserve eSATA function for future request
	P.37	Change JUSB1 as SB700 USB port6	Dedicated HS port on lower-left position
	P.38	Change U20 as KB926 D3 version (SA00001J580)	NA
	P.38	D41 with VGA@ & D42 with UMA@	Separately as DIS sku only & UMA sku only
	P.38	U20.85 defined as TP_LOCK_LED# feature	LED control simultaneously with Tutch-Pad locked function
	P.38	Change R194 as 8.2kohm_0402	Change board ID as 1 (PCB revision : 0.2)

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PHASE	PAGE	MODIFICATION LIST	PURPOSE
	P.39	Add R250/LED11/SW4	Add T/P lock button & T/P lock button LED
	P.45	Reserve R499 , R497/R498/Q51	NA
	P.45	Stuff R202	+1.2VALW leakage 640mv pulse when AC insertion & then might cause OVP
	P.34	C26 with @ & C11 as SE070104Z80	NA
	P.42	Stuff R446(0ohm_0805) & un-stuff U32(Audio LDO)	NA
DVT2	P.6	Remove CPU side-band(internal) temp sensor function	NA
	P.11/38	Add U49/C857/R744 (Reserve U48) & D42 with @, remove D42	NA
	P.23/34	Add R676 for CLK_48M_SD , reserve R715 / R716 for CLK_48M_LAN	NA
	P.24	Add R508(2.7K_0402) for ENVDD of UMA sku	NA
	P.28	SB700 USB port 4 for Realtek RTS5159 card reader	NA
	P.33	Add(co-layout) Realtek RTS5159 card reader	NA
	P.37	Change JSAT1 PCB footprint as TYCO_1909574-1_11P-T	NA
	P.38	R194 change as 18K_0402	Change board ID as 2 (PCB revision : 0.3)
	P.40	LED1 / 5 / 8 / 9 /10 PCB footprint change as LED_HT-297DQ-GQ_4P	For DFX
	P.44	Add H28 & H29	For thermal
PVT	P.11	Add R511 with @ & U50	For LCD white screen flash when coldboot issue
	P.11	Add C874 / C875 (1u_0402)	For CRT(acer lab) flicker
	P.11/38	C857 / U49 with @ , R744 / D42 with UMA@	NA
	P.42	Add L94(SM010027780) close to audio codec	For EMI
	P.40	Modify LED 1 / 5 / 8 from dual Blue/Amber LED as single Blue LED	Follow acer spec
	P.39/40	Modify R12/R13/R17/R16 (300->220ohm) , modify R1/R2/R3 (1.2K->866ohm) , modify R10 (300->715ohm) , modify R245/R247 (4.99K->750ohm) , modify R244/R246 (4.99K->866ohm) , modify R250 (1.2K->5.1K)	For LED brightness test
	P.23	Change LAN_CLKREQ# from U18.51 to U18.24 output	NA
	NA	Change test pad (except T8/T13/T15/T17/T18/T24/T28 /T29/T33/T45/T46/T48/T50/T56/T57/T12) from TPC12 to TPC24	
	P.36	Reserve Q55 / Q56 / R745 / R746 / R747 / C876 to turn off power of finger printer	
	P.38	R194 change as 18K_0402 for change board ID as 3 (PCB revision : 0.4)	



LA4921MB Rev0: DA80000DP00  
 LA4921MB Rev1: DA80000DP10  
 LA4921MB with Sub/B Rev1: DAZ07R00100

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