

# ZQ5 SYSTEM BLOCK DIAGRAM

**BOM MARK**  
 IV@: INT VGA  
 EV@: STUFF FOR EXT VGA  
 SP@: STUFF FOR UMA or VGA

**REV:B**

<b>DDR3 PWR</b> TPS51116 P40	<b>CHARGER</b> ISL88731A P36
<b>THERMAL PROTECTION</b> P44	<b>3/5V SYS PWR</b> RT8206 P37
<b>DISCHARGER</b> P42	<b>CPU CORE PWR</b> ISL6266A P39
<b>VGA CORE MAX8792</b> P41	<b>+1.05V</b> UP6111A P38

**CLOCK GENERATOR**  
 ICS:  
 SELGO: SLG8SP513VTR  
 P2

XTAL  
 14.318MHz

**Penryn 478**  
 uFCPGA  
 P3, P4

**Thermal Sensor**  
 (G780P81U)  
 P3

**Fan Driver**  
 (G991)  
 P25

**DDRIII**  
 SO-DIMM 0  
 SO-DIMM 1  
 P16,P17

**NB Cantiga**  
 (GM45/ PM45/ GL40)  
 P5, P6, P7, P8, P9, P10, P11

**ATI-Park**  
 VRAM DDRIII  
 512MB  
 P18-P23

**SWITCH CIRCUIT**  
 P25

**HDMI switch (PS8101T)**  
 P25

**CRT**  
 P24

**LVDS**  
 P24

**HDMI**  
 P25

**HDD (SATA) \***  
 P26

**ODD (SATA)**  
 P26

**Ext USB Port x 2**  
 USB 0,2  
 P27

**Int USB Port x 1**  
 USB 6  
 P27

**Bluetooth**  
 USB3  
 P27

**CCD**  
 USB11  
 P24

**SB ICH9M**  
 P12,P13,P14,P15

**Media Cardreader (AU6437)**  
 USB2  
 P30

**Giga-LAN BCM57780**  
 P30

**Audio CODEC (272)**  
 P28

**EC (WPC781)**  
 P33

**Card Reader Connector**  
 P32

**Transformer**  
 P31

**Audio Amplifier G1453L**  
 P28

**MIC Jack**  
 P29

**Int. MIC**  
 P29

**Int. Speaker**  
 P29

**SPI ROM**  
 P33

**Touch Pad**  
 P26

**K/B COON.**  
 P33

**Mini Card WLAN**  
 P27

**RJ45**  
 P31

FSB  
 667/800/1067 Mhz

Dual Channel DDR3  
 667/800 MHz

X4 DMI interface

PCI-Express

PCI-E-4

USB1

PCI-E-6

LPC

SATA0

SATA1


USB 2.0

Azalia

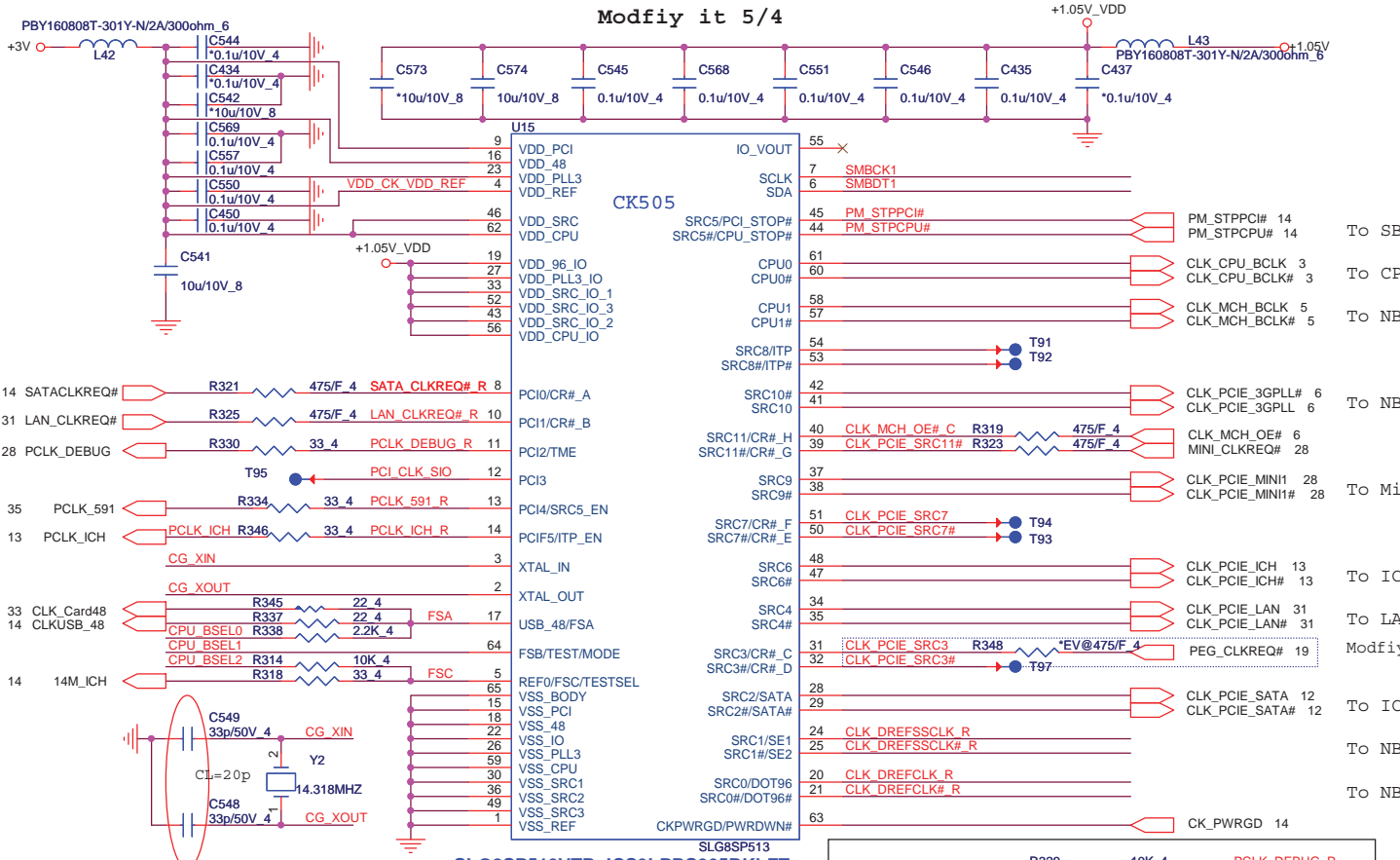
XTAL  
 32.768KHz

XTAL  
 32.768KHz

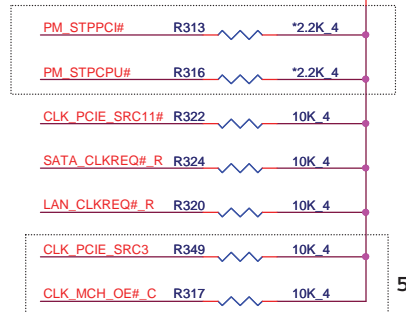
XTAL  
 25MHz

	<b>PROJECT : ZQ5</b>	
	Quanta Computer Inc.	
	Size	Document Number
Date:	Monday, July 12, 2010	Sheet 1 of 43
	<b>Block Diagram</b>	1A

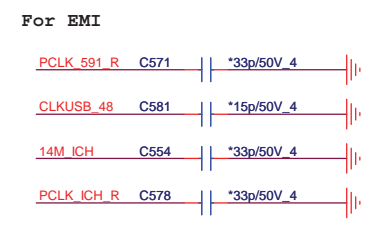
# Clock Generator(CLK)



5/7 Modiy



5/5 Add



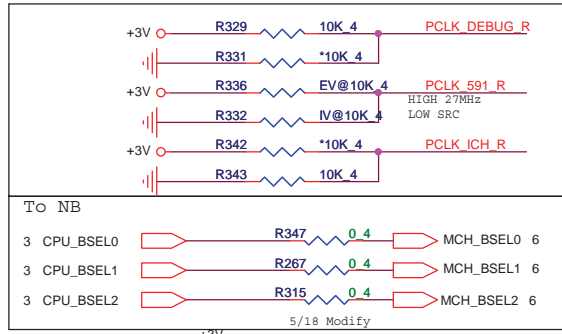
SEL2 SEL1 SEL0 Frequency select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	Reserved		

Default

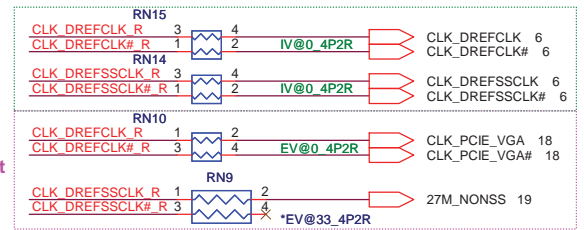
5/5 modify

Pin	IC(S9LRS3165BKLF) (ALPRS365000)	RTM875T-606 (AL000875000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 12	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 13	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 14	PCIP-5/ITP_EN	PCIP-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)



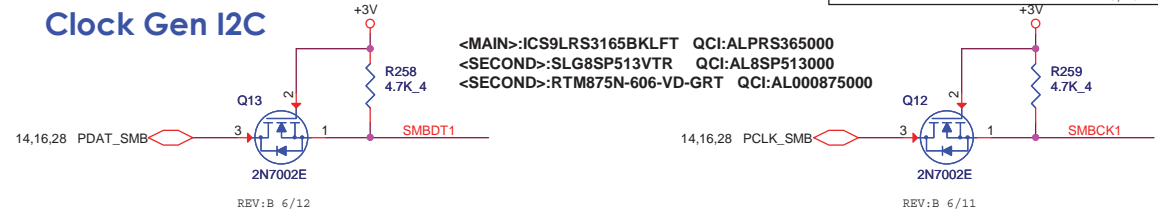
From GMCH

From Deisceret



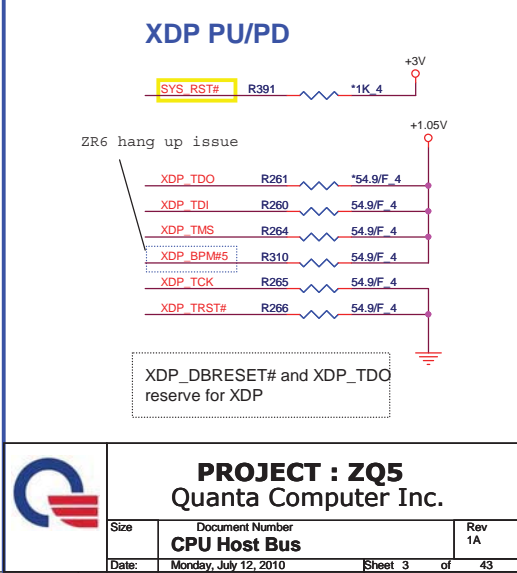
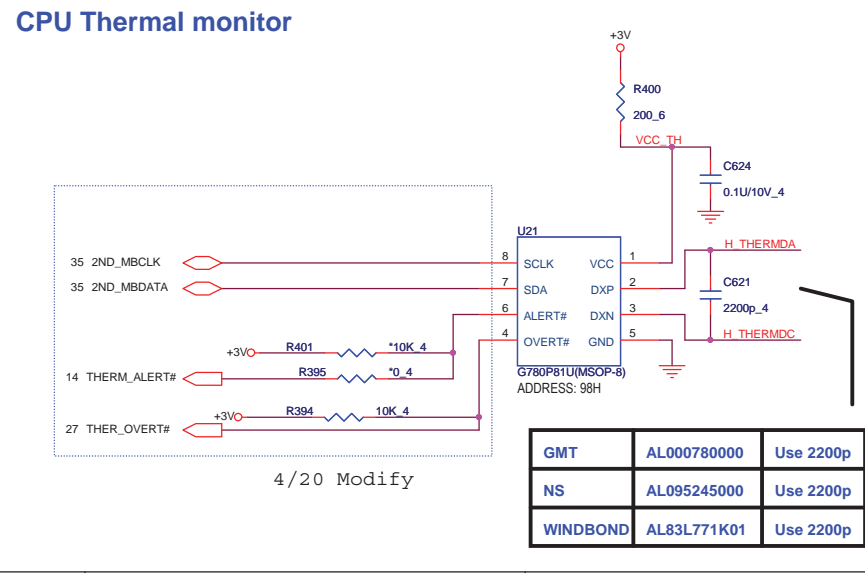
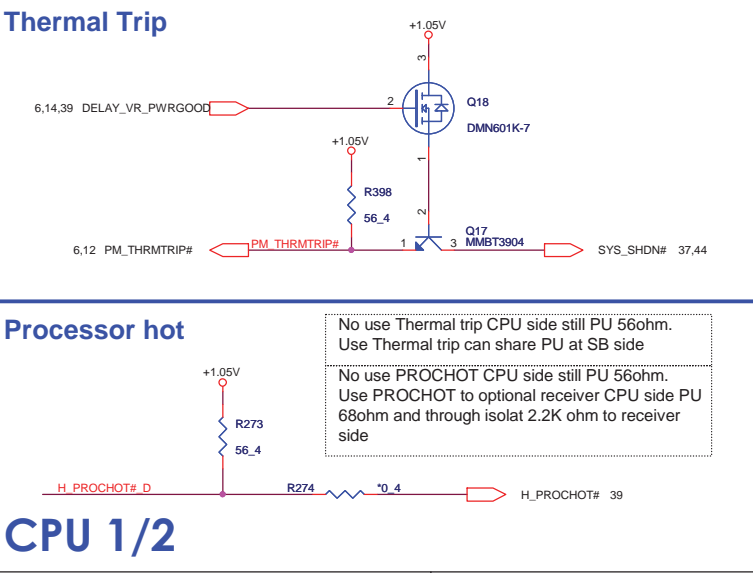
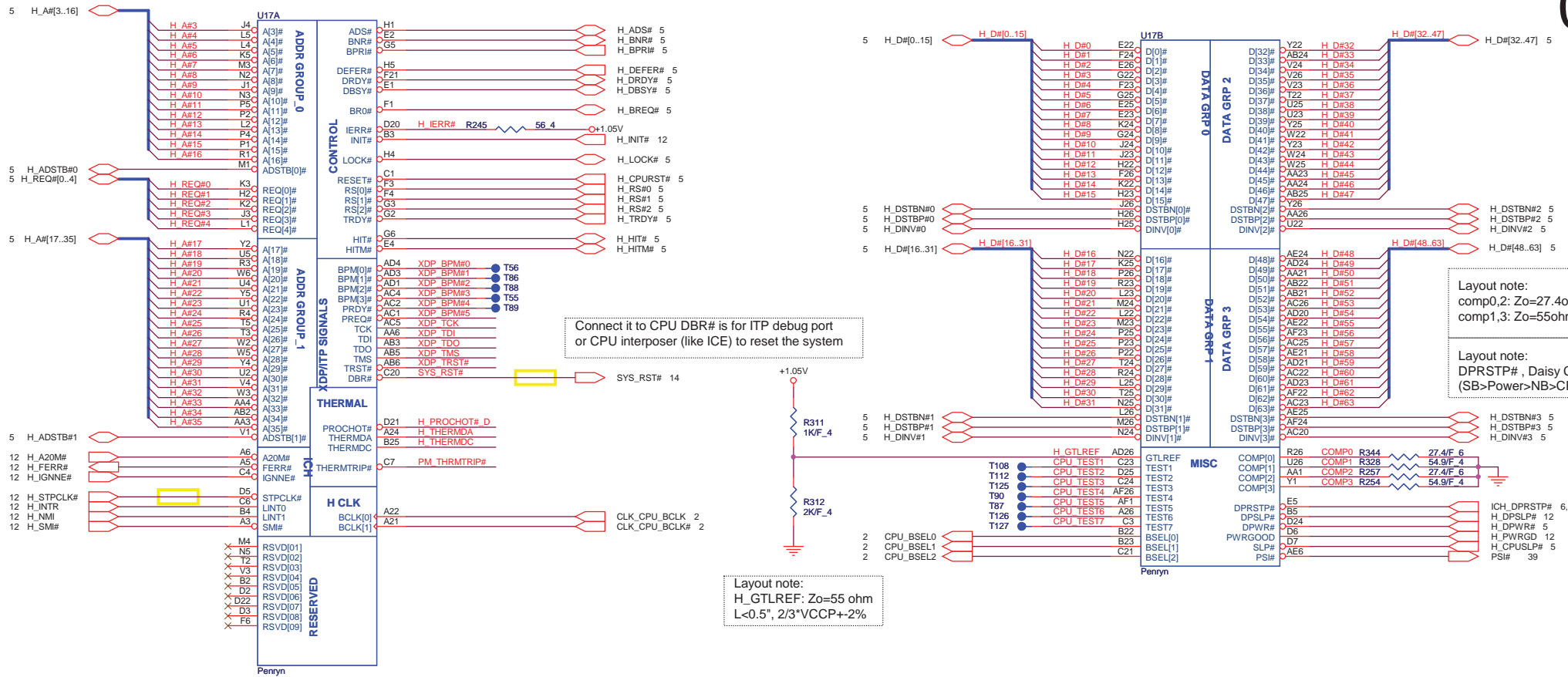
5/22 modify

## Clock Gen I2C



**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>CLOCK GENERATOR</b>	1A
Date:	Monday, July 12, 2010	Sheet 2 of 43



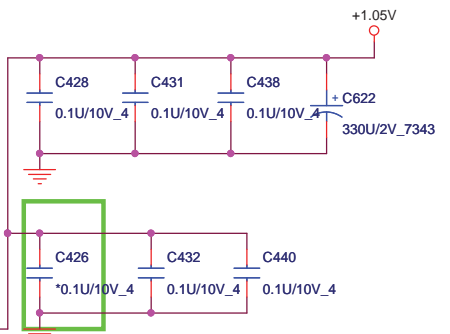
**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CPU Host Bus</b>	1A
Date:	Monday, July 12, 2010	Sheet 3 of 43

VCC:38A (Low power type)  
VCC:47A (Standard type)

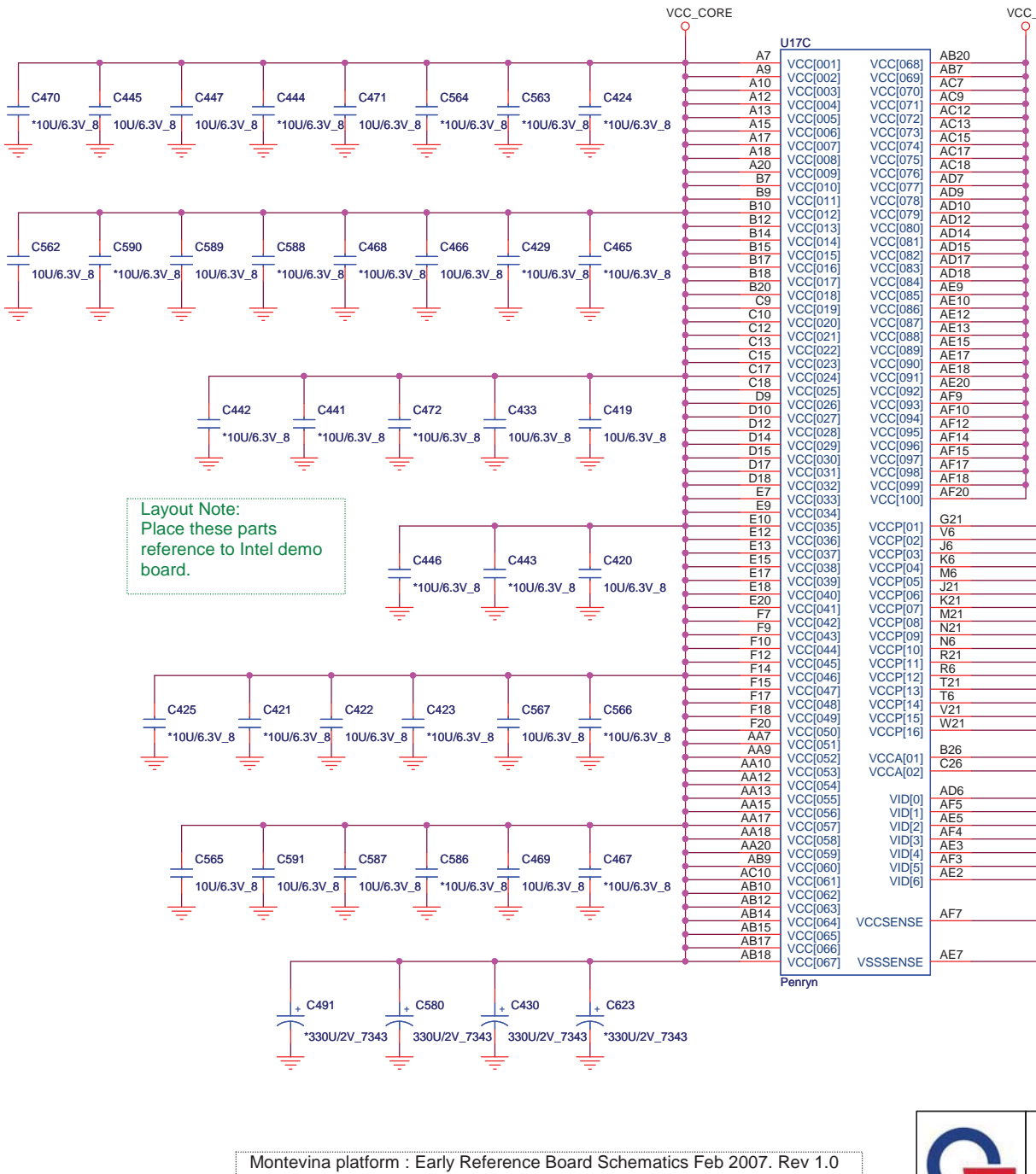
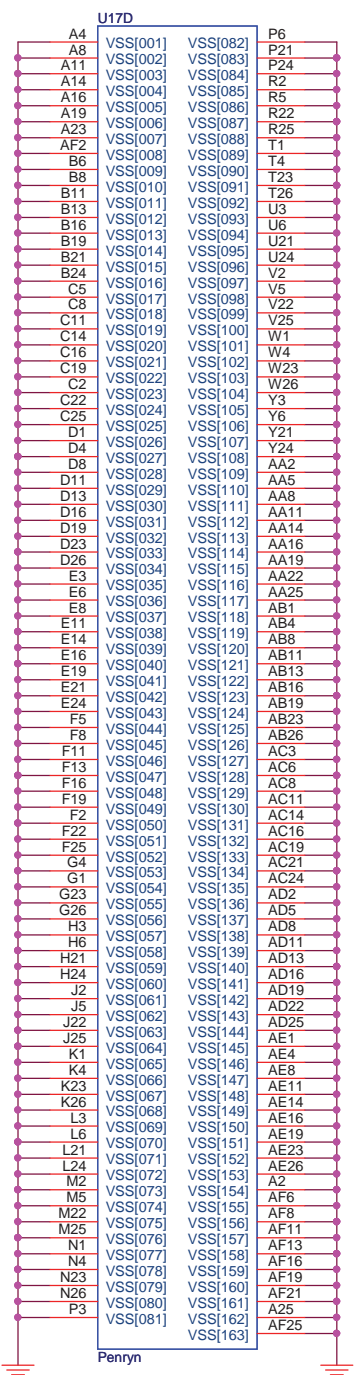
Layout Note:  
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)  
4.5A(Supply before VCC Stable)



VCCA:130mA +1.5V

Layout Note:  
Z0=27.4,PU/PD L<1"



Layout Note:  
Place these parts  
reference to Intel demo  
board.

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0  
stuff 22U\*34, NC 22U\*2  
stuff 330U\*2, NC330U\*2

CPU 2/2

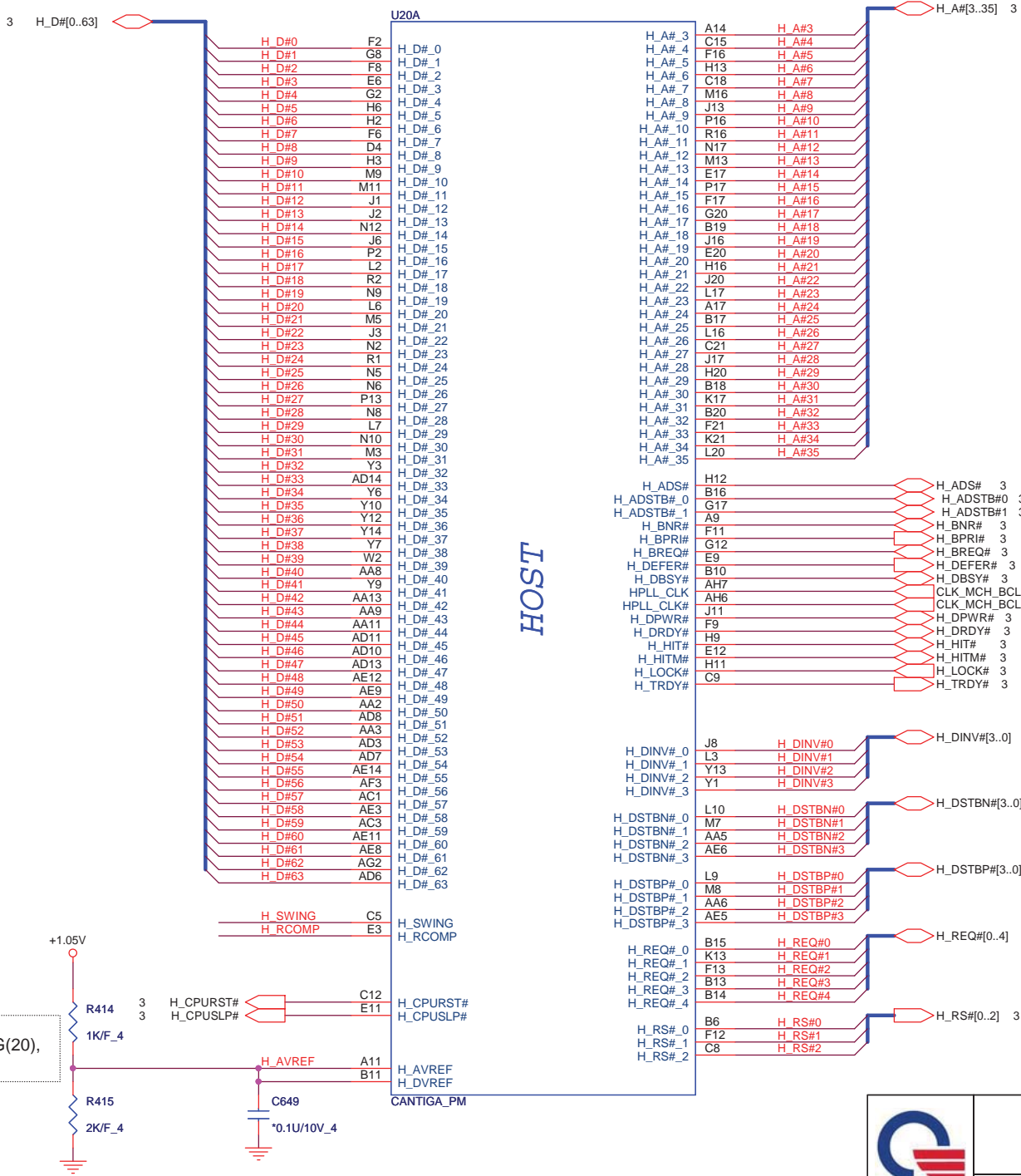


PROJECT : ZQ5  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>CPU Power</b>	1A
Date:	Monday, July 12, 2010	Sheet 4 of 43

# GMCH (CANTIGA)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



HOST

0.3125\*VCCP  
WIDE(10):SPACING(20),  
L<0.5"

Layout Note:  
WIDE(10):SPACING(20),  
L<0.5"

2/3\*VCCP  
WIDE(10):SPACING(20),  
L<0.5"



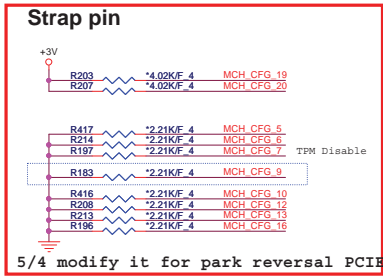
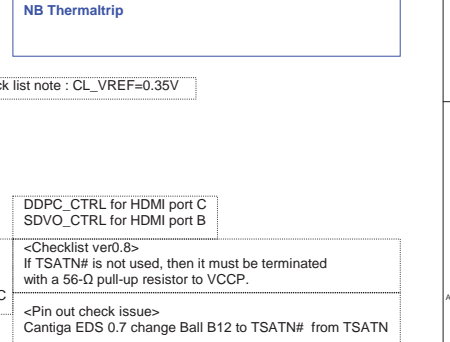
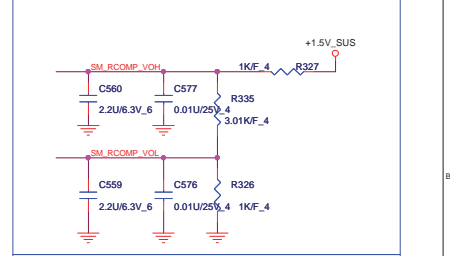
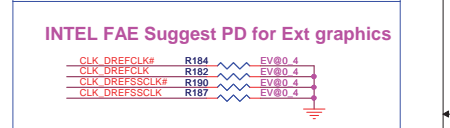
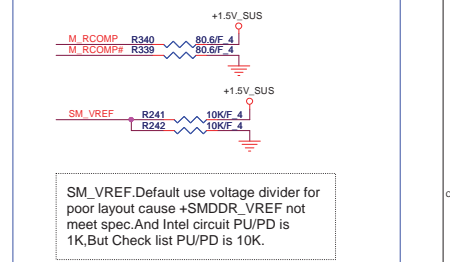
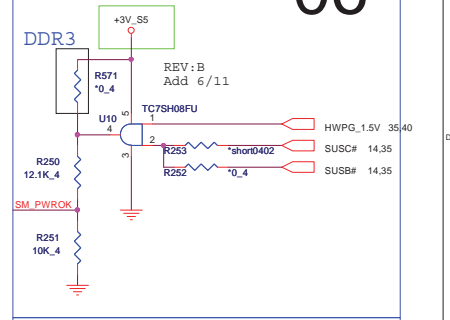
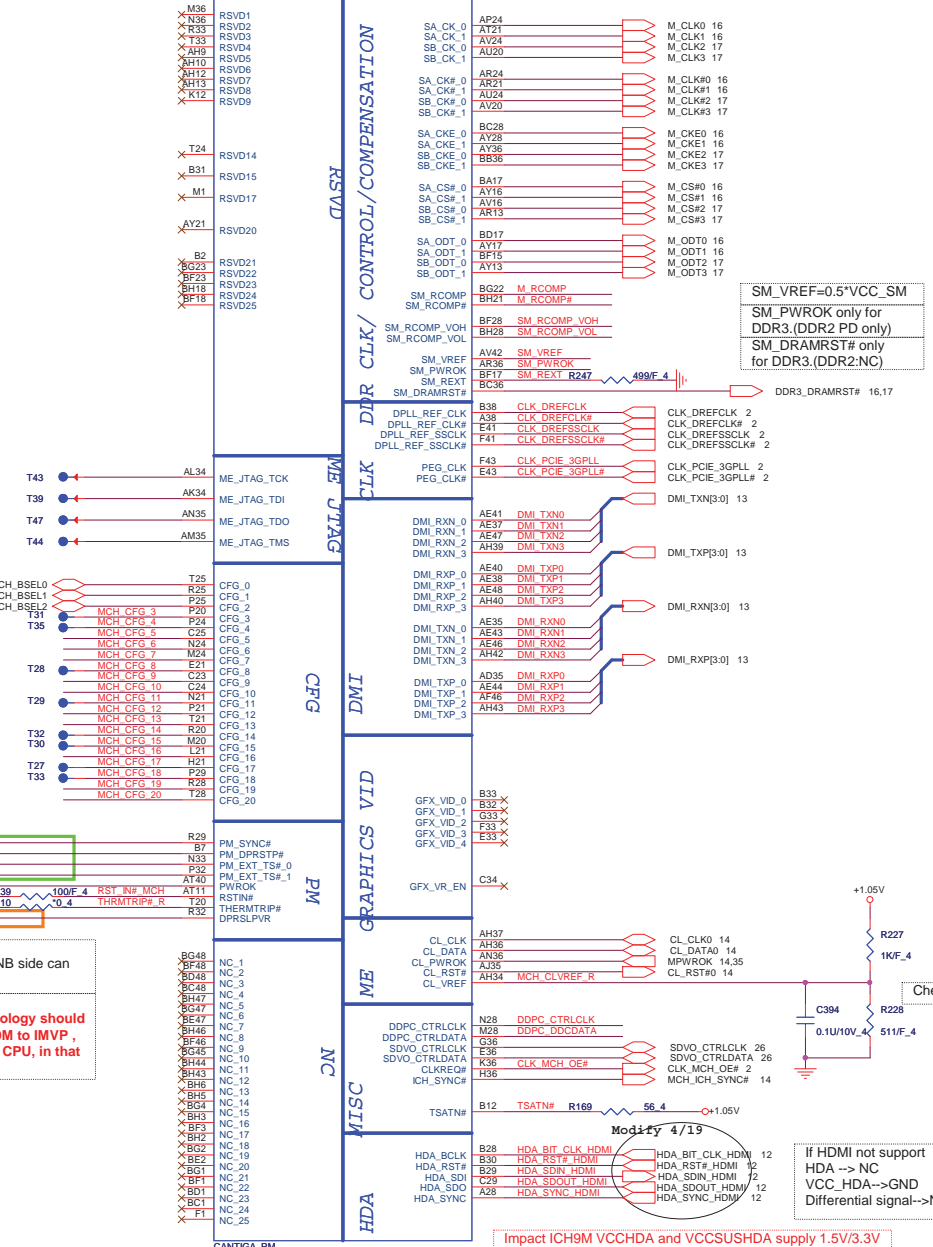
**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>GMCH HOST</b>	1A
Date:	Monday, July 12, 2010	Sheet 5 of 43

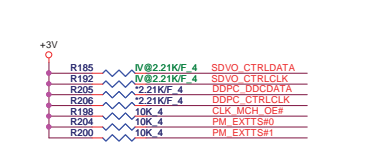
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 106MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent (Default) 1 = Digital display(HDMI/DP) device present

U20B



NB Thermal trip pin  
No use Thermal trip NB side can NC, (NB has ODT)  
PM\_DPRSTP#  
The Daisy chain topology should be routed from ICH9M to IMVP, then to (G)MCH and CPU, in that order.



Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V  
NOTE:  
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size: Document Number: **GMCH DMI** Rev: 1A  
Date: Monday, July 12, 2010 Sheet 6 of 43

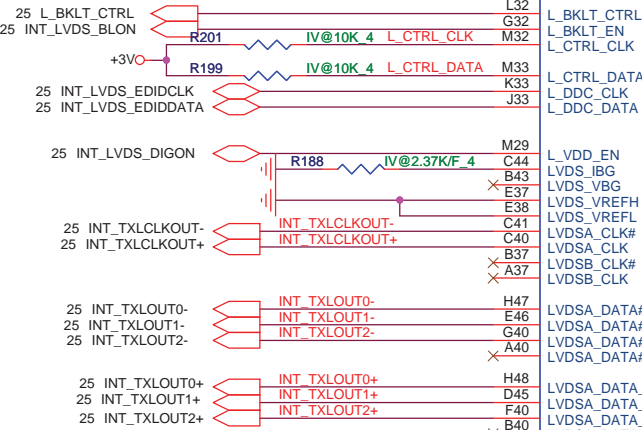
IV@

EV@ IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

SP@

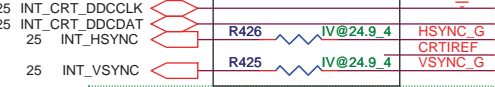
07



**SP@**  
TV\_A/B/C  
For IV: 75ohm  
For EV:0ohm

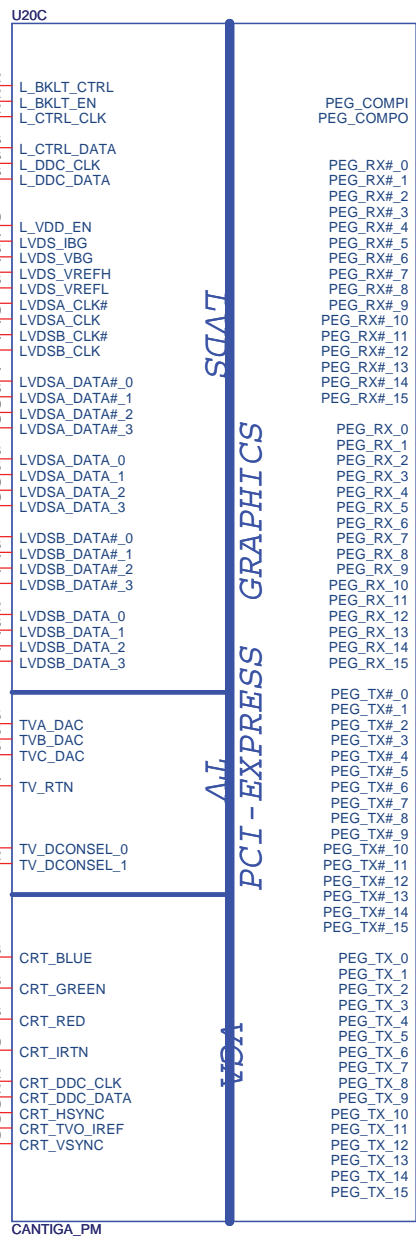
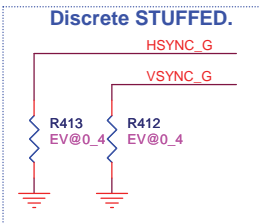


**6/14 Modify**  
REV: B

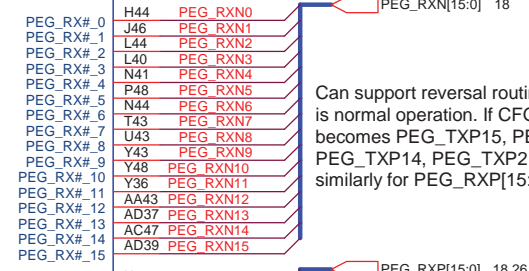


HSYNC/VSYNC serial R place close to NB

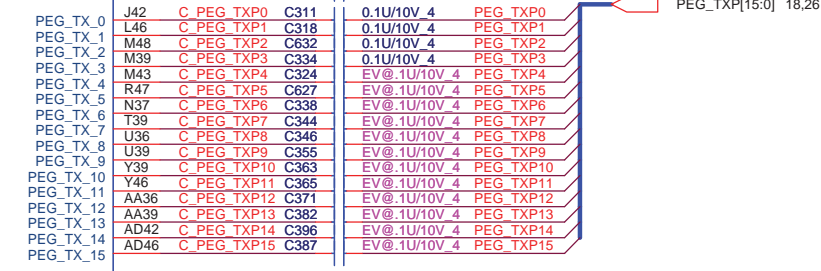
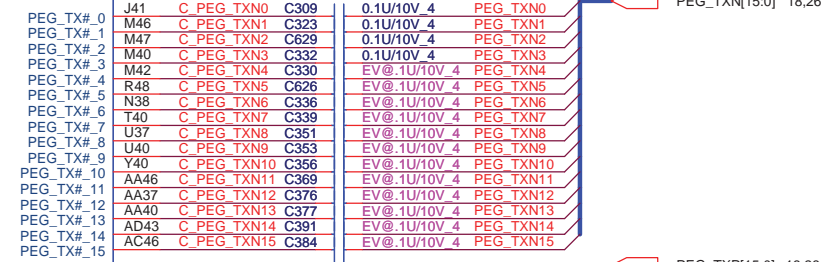
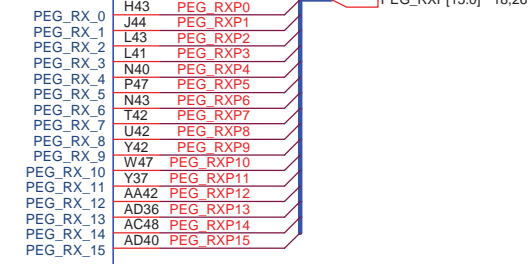
CRTIREF pull down  
for IV cantiga 1k ohm/F



L<0.5" , If PCIE not support  
still connect to +VCC\_PEG



Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG\_TXP0 becomes PEG\_TXP15, PEG\_TXP1 becomes PEG\_TXP14, PEG\_TXP2 becomes PEG\_TXP13, etc. similarly for PEG\_RXP[15:0] and PEG\_RXN[15:0]



IV&EV Dis/Enable setting

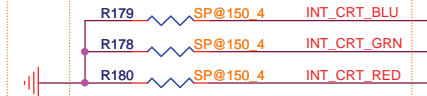
<5/31>Montevina\_Schematics\_Checklist\_Rev0\_8  
a)For TVOUT Disabled, TV\_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.  
b)For CRT DAC Disable, CRT\_DDC\_CLK, CRT\_DDC\_DATA, CRT\_HSNC, CRT\_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list> For EV@ CRT R/G/B 0ohm to GND CRT TIREF 0ohm to GND  
<check list> For IV@ CRT R/G/B 150ohm to GND CRT TIREF 1Kohm to GND

**CRTIREF**  
For IV: 1Kohm  
For EV:0ohm



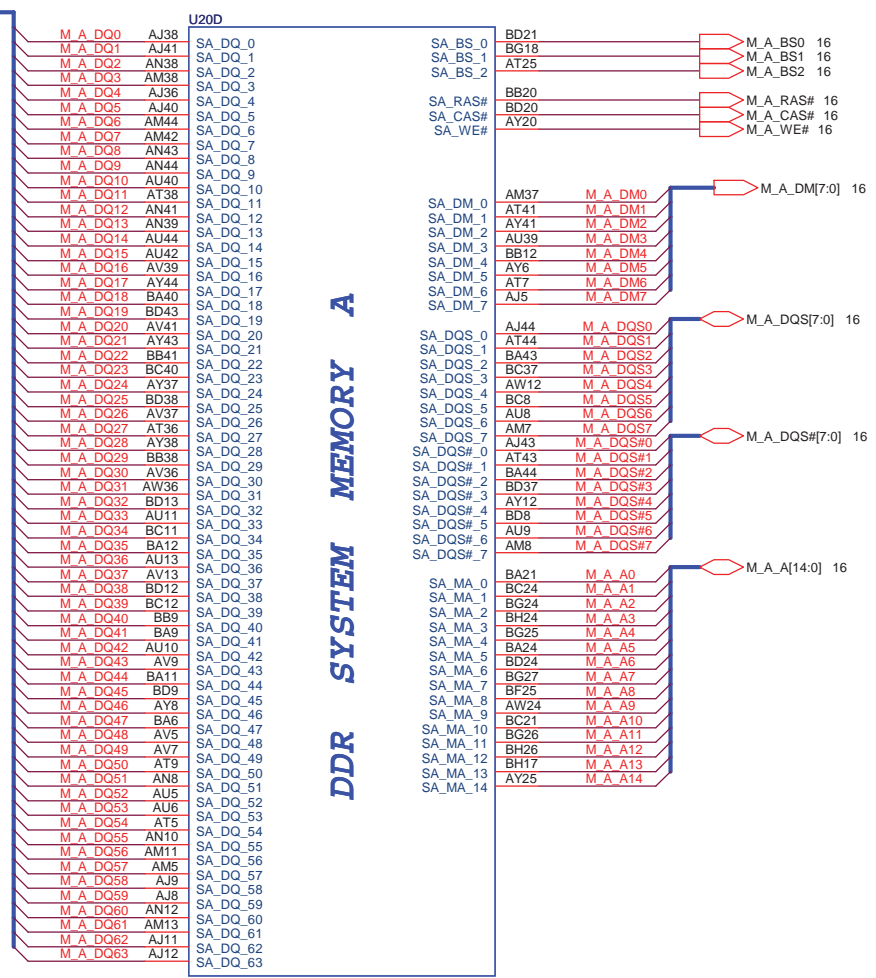
**CRT\_R/G/B**  
For IV: 150ohm  
For EV:0ohm



**PROJECT : ZQ5**  
Quanta Computer Inc.

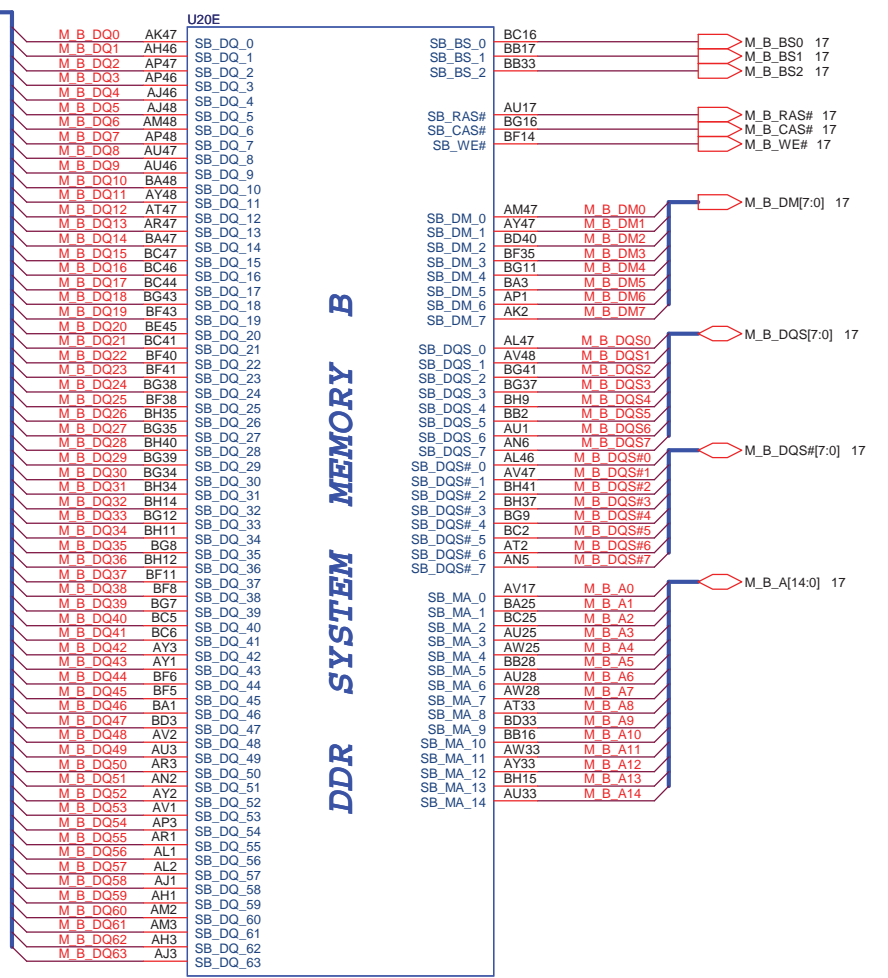
Size	Document Number	Rev
	<b>GMCH VGA</b>	1A
Date:	Monday, July 12, 2010	Sheet 7 of 43

16 M\_A\_DQ[63:0]



CANTIGA\_PM

17 M\_B\_DQ[63:0]



CANTIGA\_PM

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

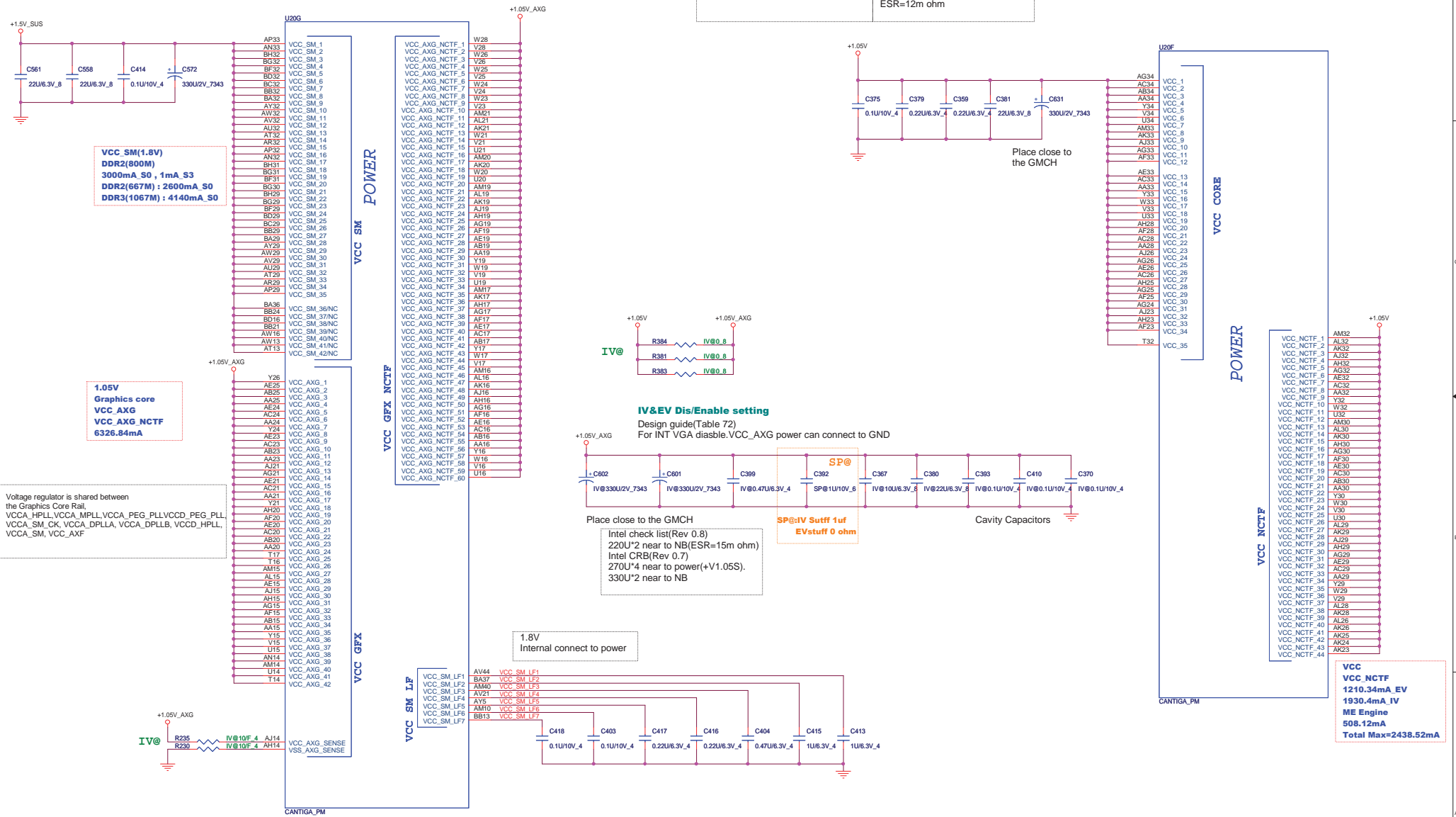


Power consumption reference to Intel  
644135 Cantiga chipset EDS Volume1.  
Section 10

GM TDP 10.5-12W  
GS TDP 7-8W  
PM TDP 7W

Intel check list(Rev 0.8)  
No description for VCC\_SM bulk CAP  
Intel CRB(Rev 0.7)  
330U\*1 Reserve near to power  
330U\*1 near to NB

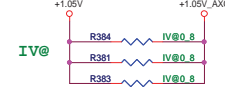
Intel check list(Rev 0.8)  
270U\*1 near to power(+V1.05M).  
270U\*2 near to NB  
Intel CRB(Rev 0.7)  
270U\*3 near to power(+V1.05M).  
270U\*1 near to NB  
ESR=12m ohm



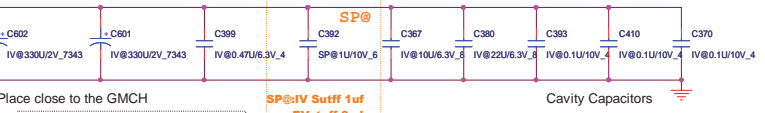
VCC\_SM(1.8V)  
DDR2(800M)  
3000mA S0, 1mA S3  
DDR3(667M) : 2600mA S0  
DDR3(1067M) : 4140mA S0

1.05V  
Graphics core  
VCC\_AGX  
VCC\_AGX\_NCTF  
6326.84mA

Voltage regulator is shared between  
the Graphics Core Rail,  
VCCA\_HPLL,VCCA\_MPLL,VCCA\_PEG\_PLL,VCCD\_PEG\_PLL,  
VCCA\_SM\_CK,VCCA\_DPLLA,VCCA\_DPLLB,VCCD\_HPLL,  
VCCA\_SM,VCC\_AXF



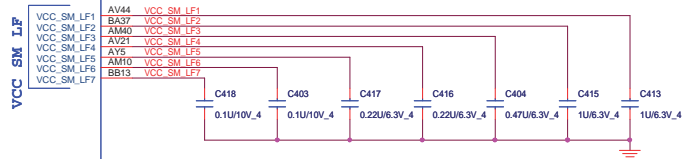
IV&EV Dis/Enable setting  
Design guide(Table 72)  
For INT VGA diasble.VCC\_AGX power can connect to GND



Place close to the GMCH  
Intel check list(Rev 0.8)  
220U\*2 near to NB(ESR=15m ohm)  
Intel CRB(Rev 0.7)  
270U\*4 near to power(+V1.05S).  
330U\*2 near to NB

SP@  
SP@:IV Sufft 1uf  
EVstuff 0 ohm

1.8V  
Internal connect to power



VCC\_NCTF  
VCC\_NCTF  
1930.4mA IV  
ME Engine  
508.12mA  
Total Max=2438.52mA

1. Route VCC\_AGX\_SENSE and VSS\_AGX\_SENSE differentially  
2. VCC\_AGX\_SENSE PU to +V\_GFX\_CORE\_INT with 10ohm  
and VSS\_AGX\_SENSE PD with 100hm for Intel suggest

PROJECT : ZQ5  
Quanta Computer Inc.  
GMCH VCC,NCTF  
Date: Monday, July 12, 2010 Sheet 9 of 43

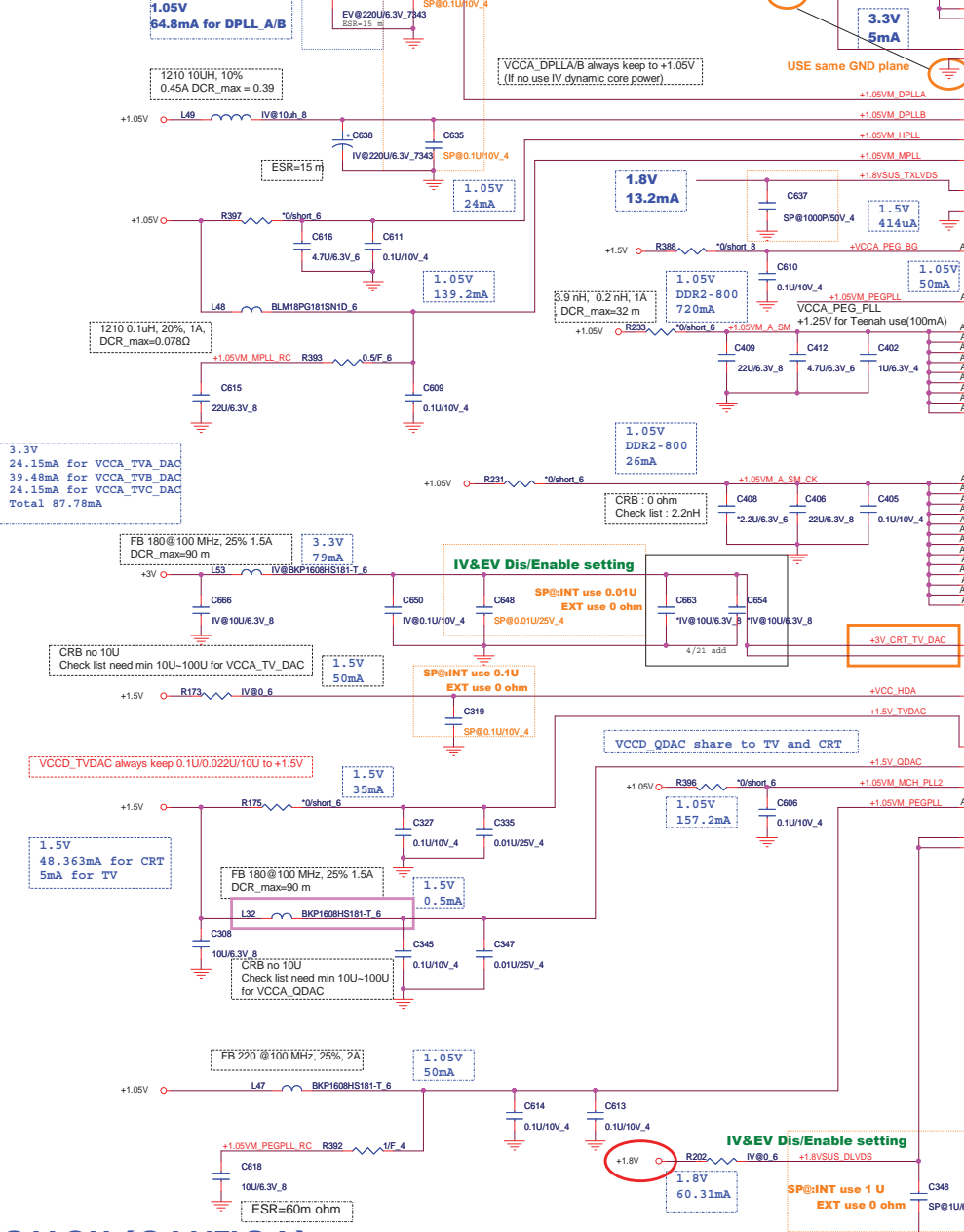
Power consumption reference to Intel Cantiga chipset EDS Volum1, Section 10

External Graphics (GMCH Integrated Graphics Disable)

VCCSYNCR_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

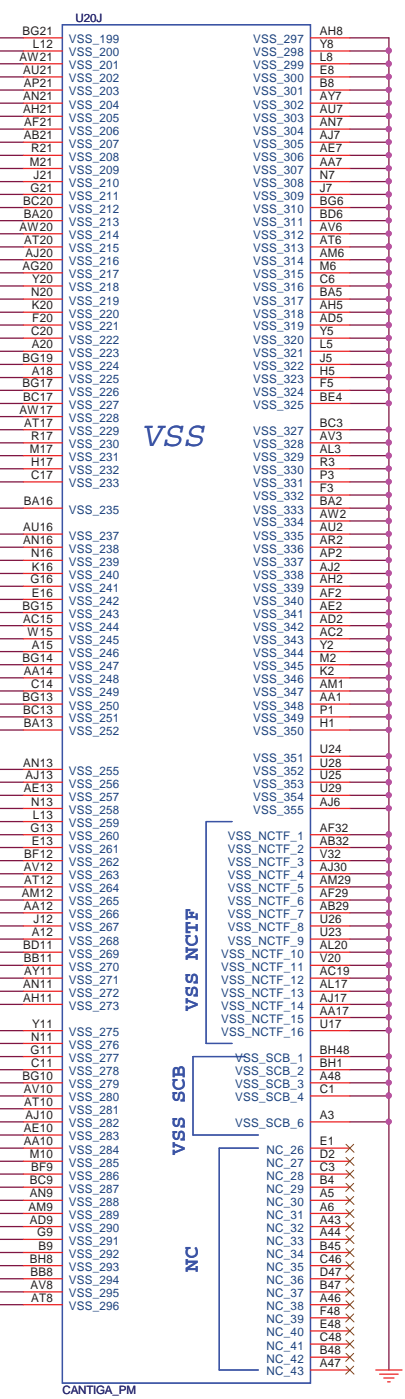
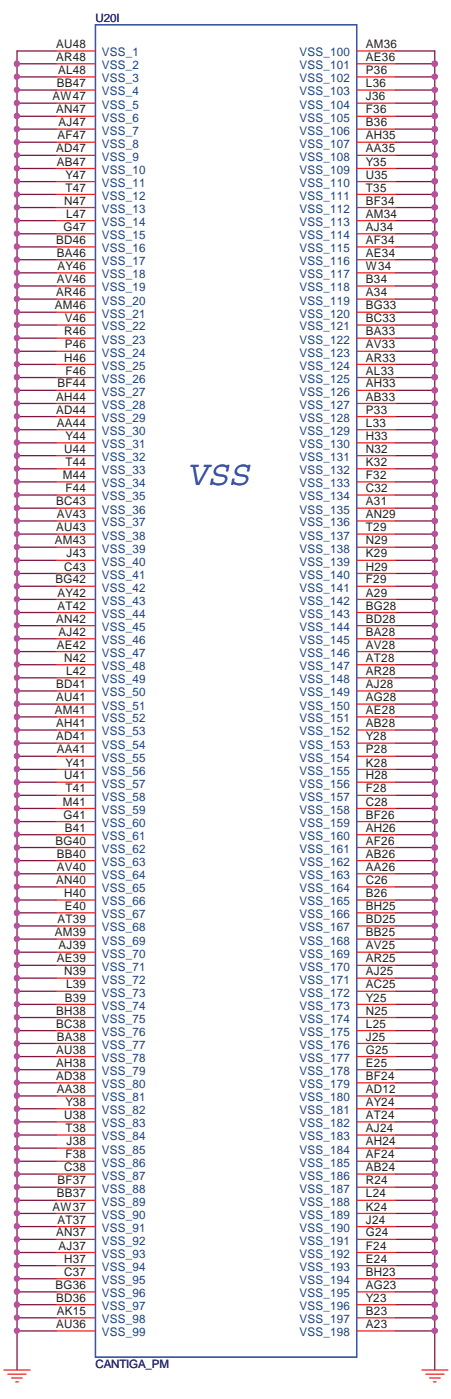
IV@  
EV@  
SP@

5/12 UMA no stuff



Power Net Name	Cantiga (V)
VCC_AXG_#	1.05V
VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_LVDS	1.05V
VCCD_HVLS	1.05V

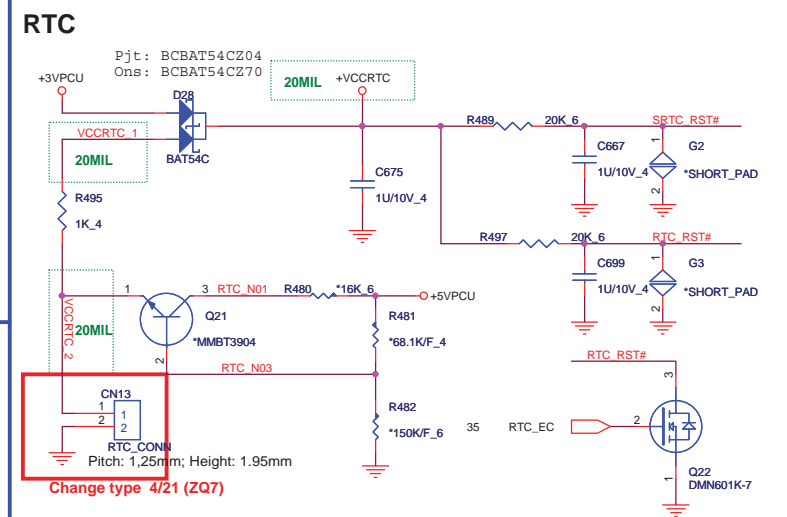
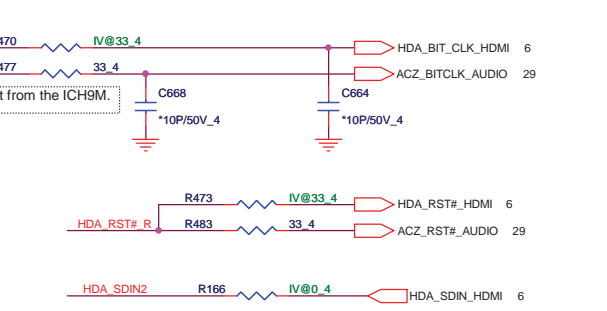
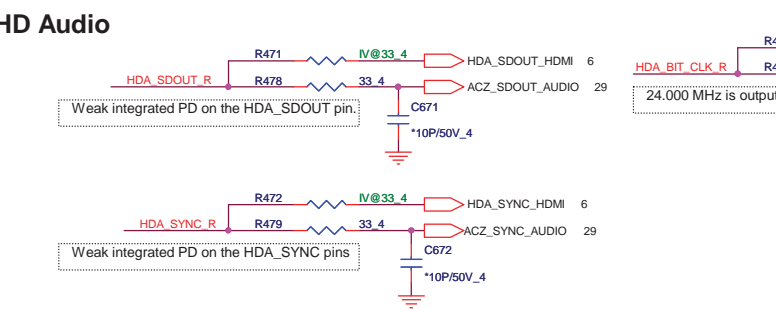
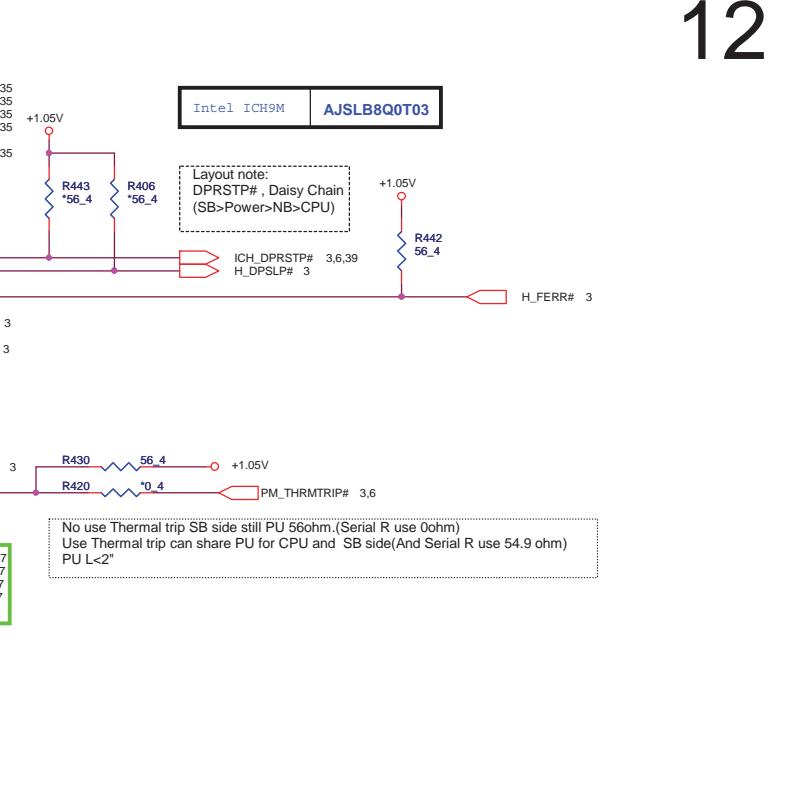
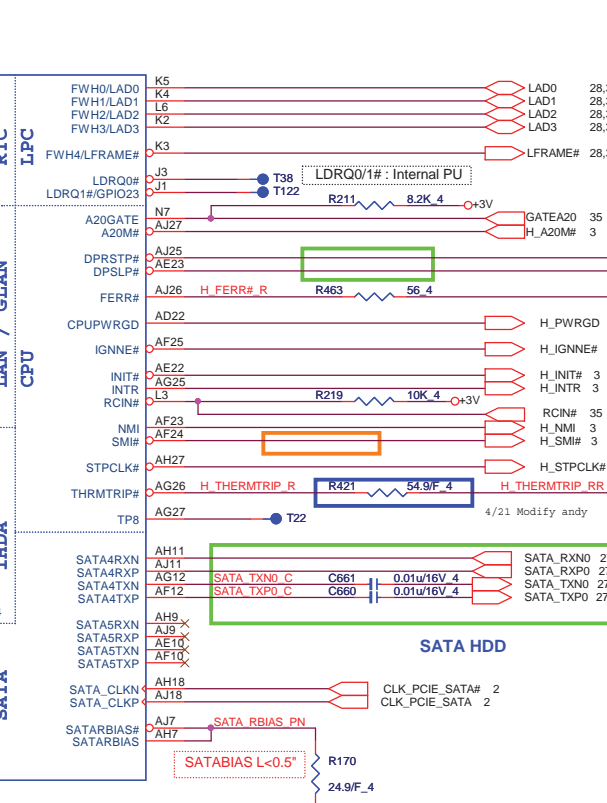
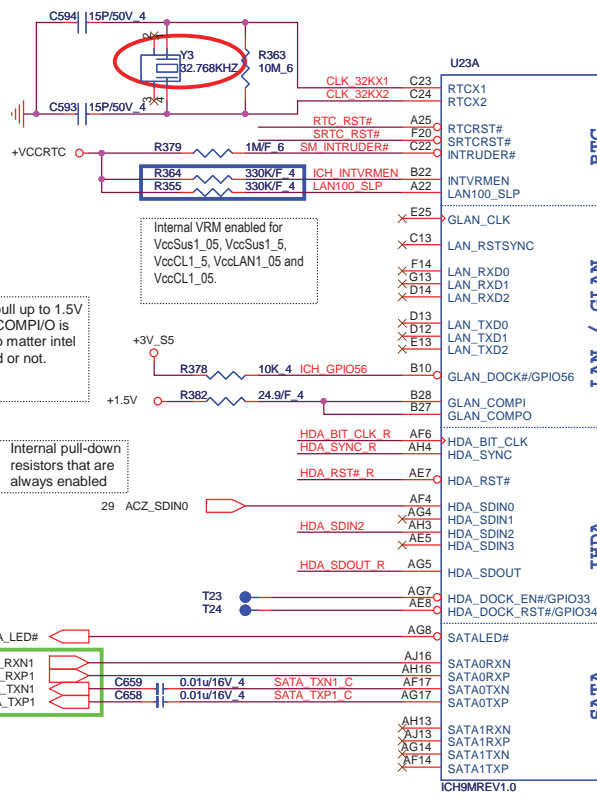




**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>GMCH VSS</b>	1A
Date:	Monday, July 12, 2010	Sheet 11 of 43

ICH9M  
IV@  
EV@

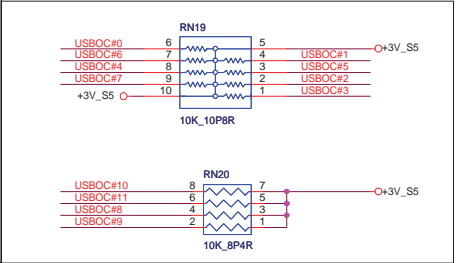
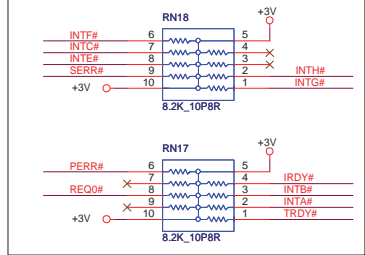
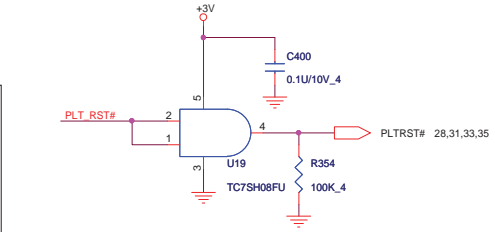
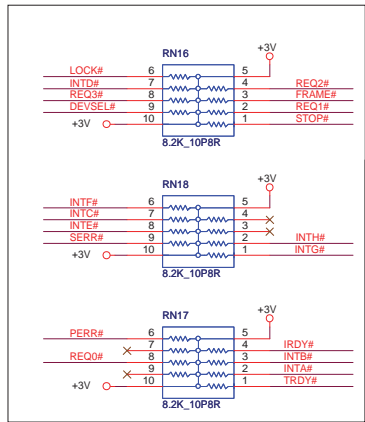
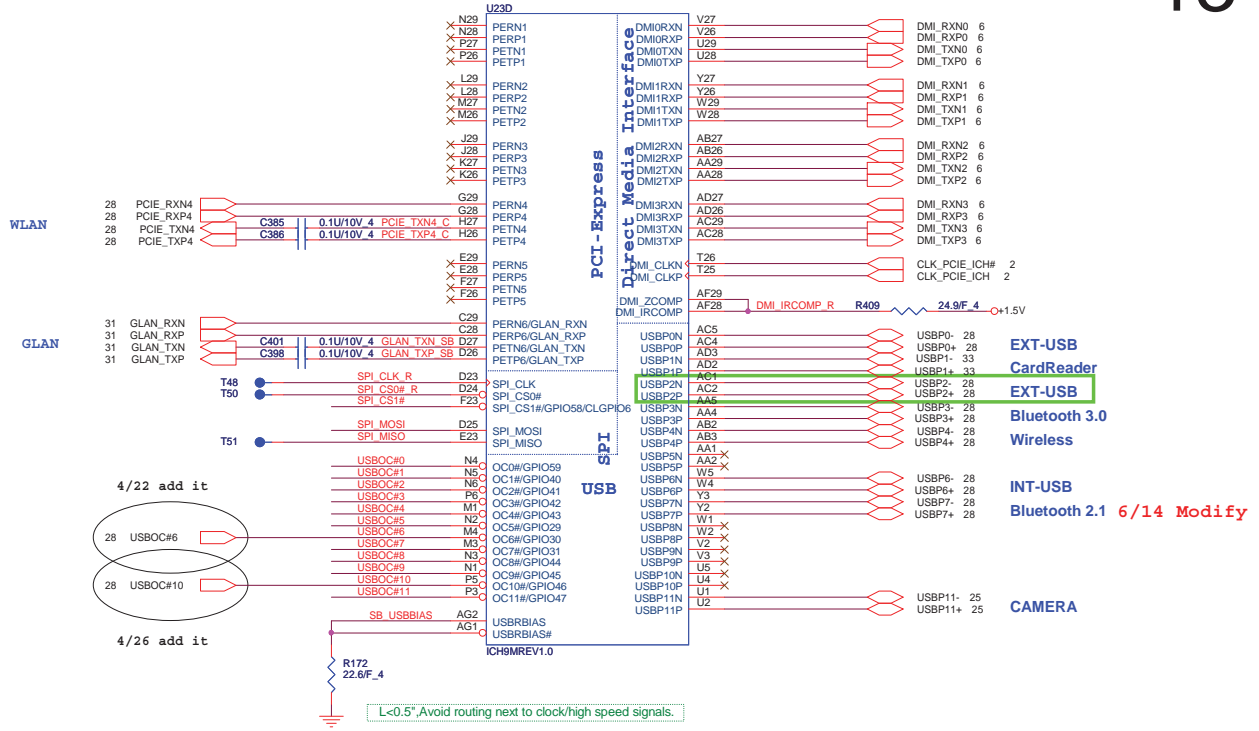
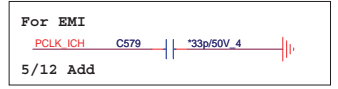
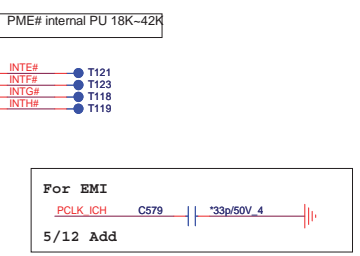
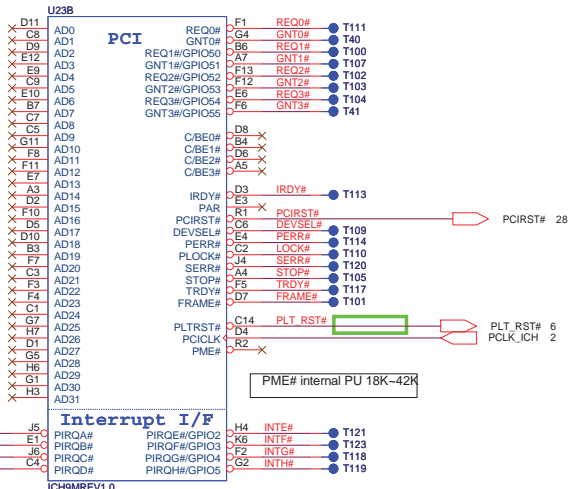


Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3   HDA_SDOUT   Description	14 ICH_TP3 ICH_TP3 R370 *1K 4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1 (Port 1-4)	PWROK	0   0   RSVD	HDA_SDOUD_R R440 *1K 4 +3V
			0   1   Enter XOR Chain	
			1   0   Normal operation(Default)	
			1   1   Set PCIe port config bit 1	

**PROJECT : ZQ5**  
Quanta Computer Inc.

Size: Document Number: ICH9M HOST, Rev 1A  
Date: Monday, July 12, 2010, Sheet 12 of 43

Change type 4/21 (ZQ7)



South Bridge Strap Pin (2/3)

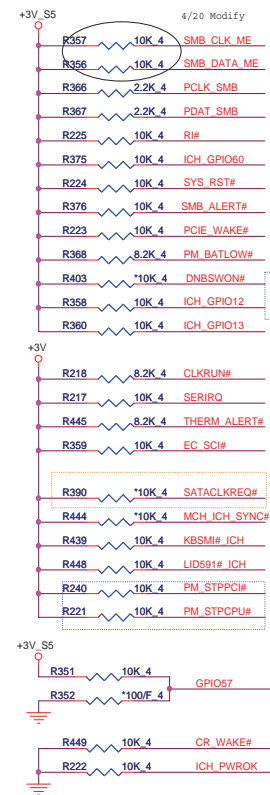
Pin Name	Strap description	Sampled	Configuration	PU/PD									
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0										
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default										
GNT1# / GPIO51	ESI Strap (Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R237 *1K_4									
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R380 *10K_4 >+3V_S5									
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>0</td> <td>1</td> <td>SPI</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI	GNT0# R236 *1K_4			
PCI_GNT#0	SPI_CS#1	Boot Location											
0	1	SPI											
SPI_CS#1 / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table border="1"> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>1</td> <td>1</td> <td>LPC(Default)</td> </tr> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	1	0	PCI	1	1	LPC(Default)	SPI_CS#1 R234 *1K_4
PCI_GNT#0	SPI_CS#1	Boot Location											
1	0	PCI											
1	1	LPC(Default)											

5/11 Swap

5/11 Swap

**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>ICH9M PCIE / PCI / USB</b>	<b>1A</b>
Date:	Monday, July 12, 2010	Sheet 13 of 43

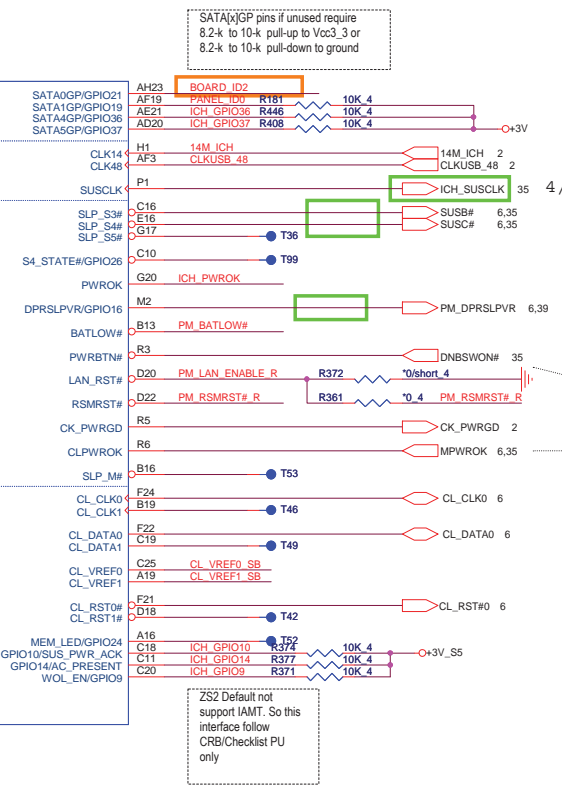
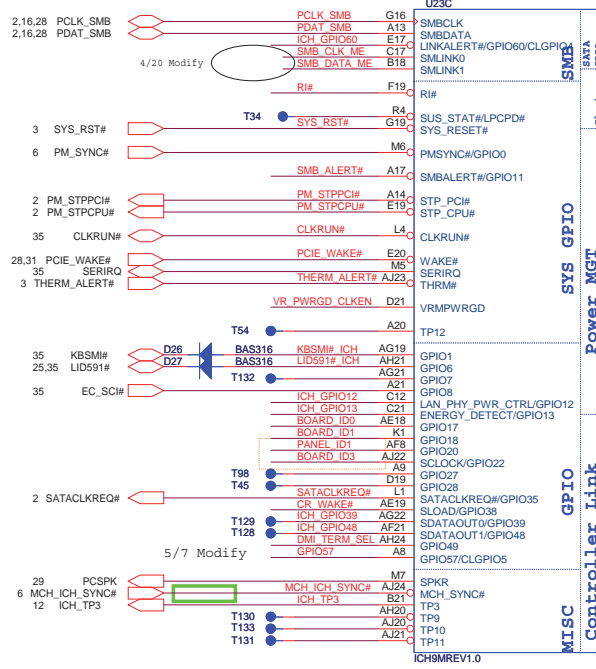


D3A(1131) ASF issue: when iAMT is not implemented, ICH9M SMBus and SMLink should be connected together to support slave mode. Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

PWRBTN : 16 ms of internal debounce logic on this pin and internal PU 24K

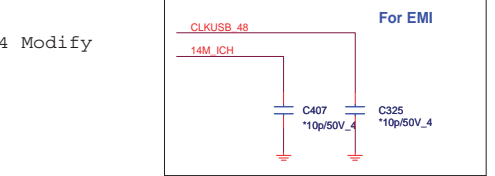
Stuff at GEN

TPM Physical Presence for iTPM.



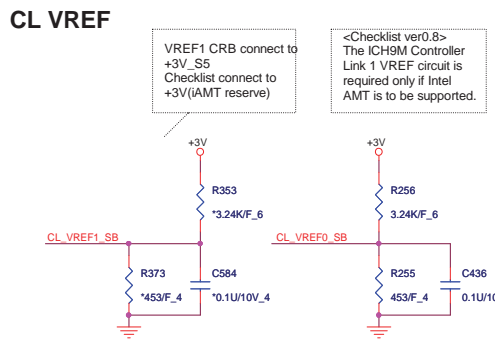
SATA/CP pins if unused require 8.2k to 10k pull-up to Voc3.3 or 8.2k to 10k pull-down to ground

ZS2 Default not support iAMT. So this interface follow CRB/Checklist PU only

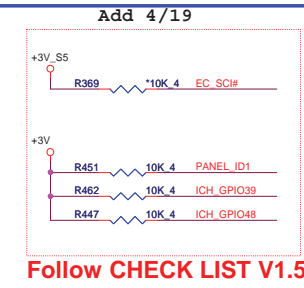


<Checklist ver0.8> If integrated LAN is not used LAN\_RST# tie it to GND. NC serial R from RSMRST#. If Intel LAN is used with Wake On LAN, tie LAN\_RST# to RSMRST# and NC 0ohm.

CL\_PWROK must not assert after PWROK asserts for iAMT. CL\_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no iAMT

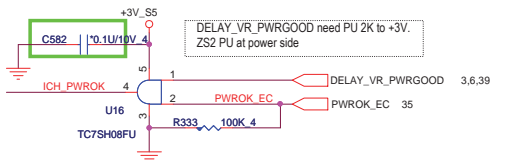


VREF1 CRB connect to +3V\_S5 Checklist connect to +3V(iAMT reserve) <Checklist ver0.8> The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

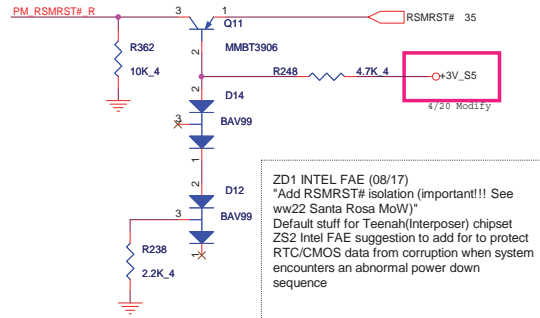


Follow CHECK LIST V1.5

ICH PWROK

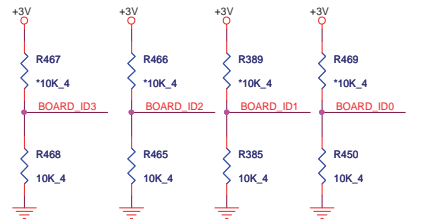


Resume RST



ZD1 INTEL FAE (08/17) "Add RSMRST# isolation (important!! See ww22 Santa Rosa MoW)" Default stuff for Teenah(Interposer) chipset ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

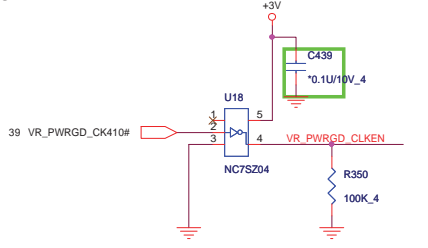


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R216 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R464 *1K_4

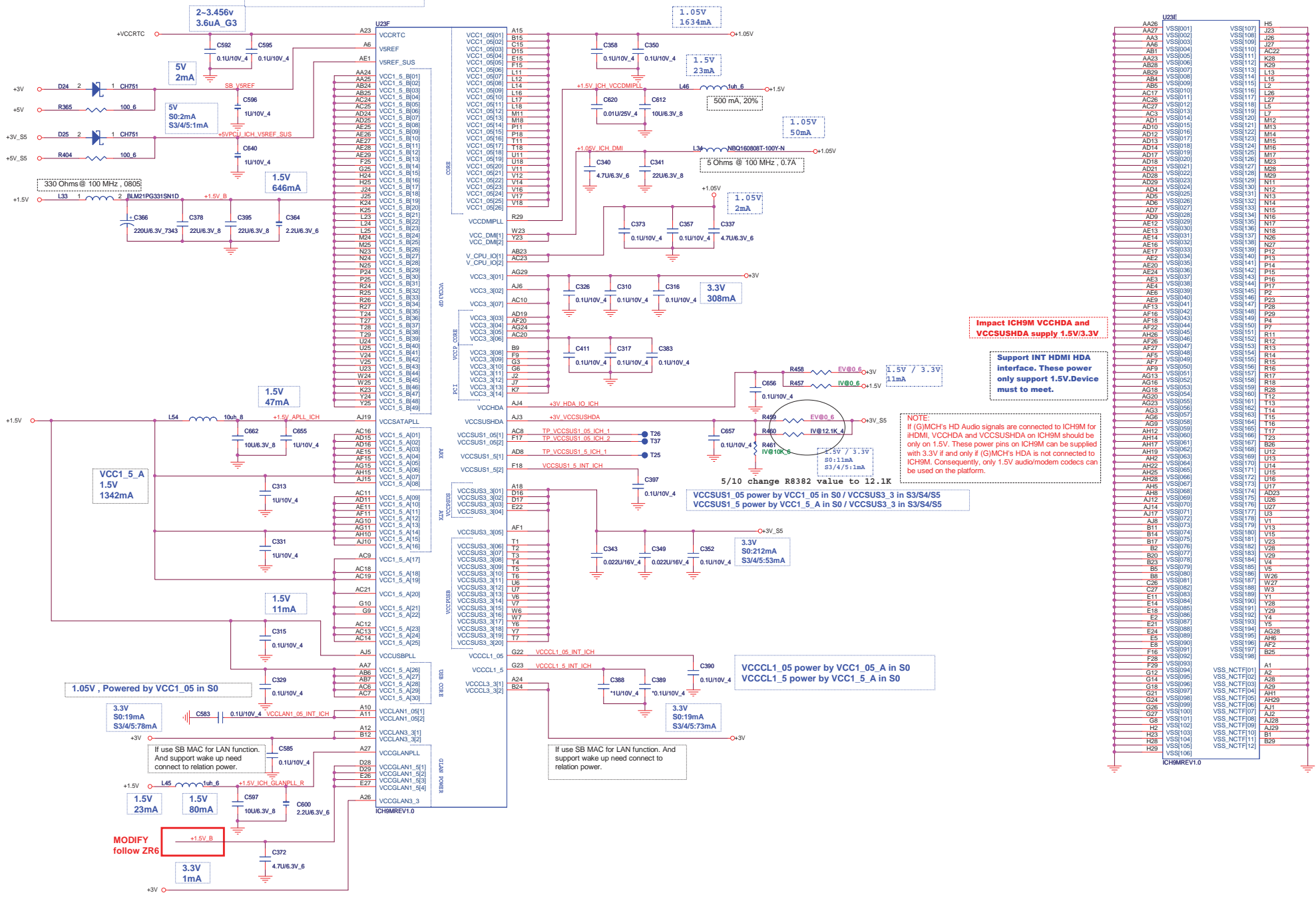
CLK Enable



IV@ EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF



Impact ICH9M VCCHDA and VCCSUSHA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V device must to meet.

NOTE: If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

5/10 change R8382 value to 12.1K

VCCCL1\_05 power by VCC1\_05\_A in S0 / VCCSUS3\_3 in S3/S4/S5

1.05V, Powered by VCC1\_05 in S0

MODIFY follow ZR6

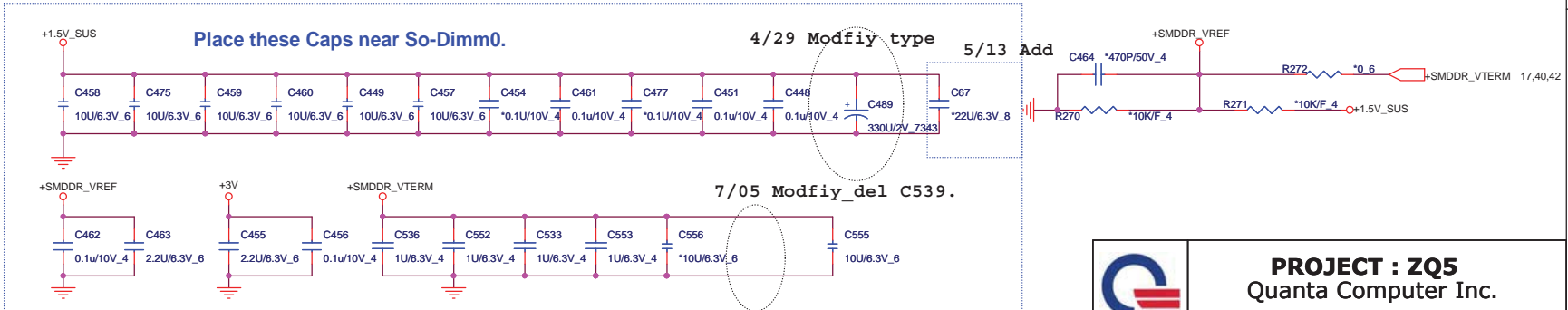
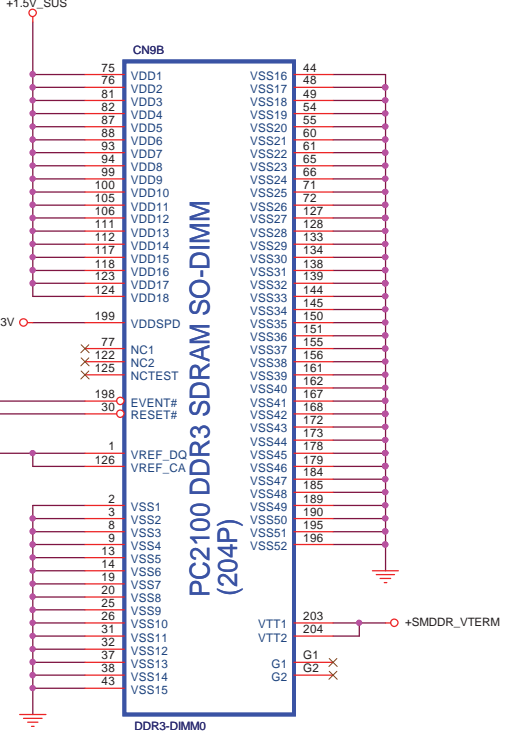
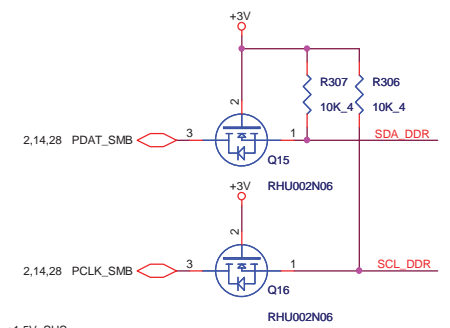
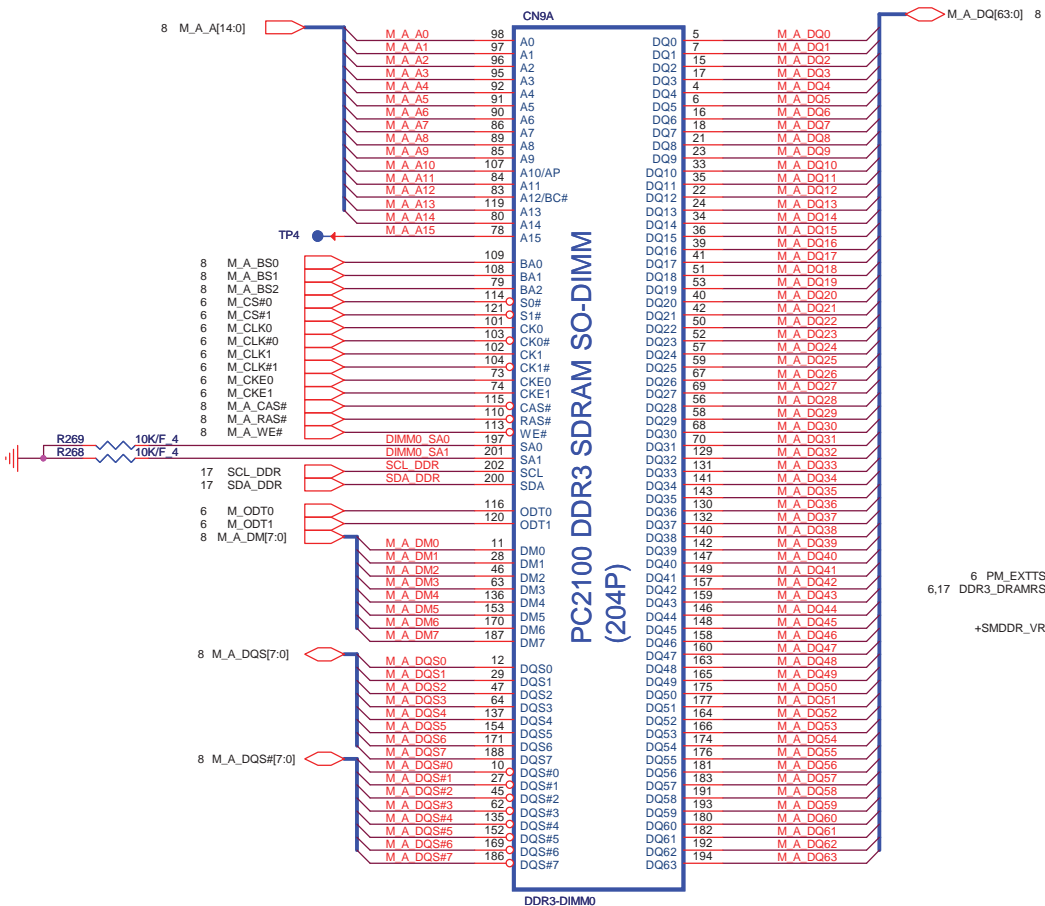
U23E	U23E	U23E
AA26	VSS001	VSS1071
AA27	VSS002	VSS1072
AA3	VSS108	VSS1073
AA6	VSS109	VSS1074
AB1	VSS110	VSS1075
AA23	VSS004	VSS111
AA24	VSS005	VSS112
AB28	VSS006	VSS113
AB4	VSS007	VSS114
AB5	VSS008	VSS115
AC17	VSS009	VSS116
AC26	VSS010	VSS117
AC27	VSS011	VSS118
AC3	VSS012	VSS119
AD1	VSS013	VSS120
AD10	VSS014	VSS121
AD12	VSS015	VSS122
AD13	VSS016	VSS123
AD14	VSS017	VSS124
AD17	VSS018	VSS125
AD18	VSS019	VSS126
AD21	VSS020	VSS127
AD28	VSS021	VSS128
AD29	VSS022	VSS129
AD3	VSS023	VSS130
AD34	VSS024	VSS131
AD5	VSS025	VSS132
AD6	VSS026	VSS133
AD7	VSS027	VSS134
AD9	VSS028	VSS135
AE12	VSS029	VSS136
AE14	VSS030	VSS137
AE2	VSS031	VSS138
AE22	VSS032	VSS139
AE23	VSS033	VSS140
AE3	VSS034	VSS141
AE4	VSS035	VSS142
AE6	VSS036	VSS143
AE7	VSS037	VSS144
AE9	VSS038	VSS145
AF13	VSS039	VSS146
AF16	VSS040	VSS147
AF18	VSS041	VSS148
AF22	VSS042	VSS149
AF24	VSS043	VSS150
AF26	VSS044	VSS151
AF27	VSS045	VSS152
AF3	VSS046	VSS153
AF5	VSS047	VSS154
AF7	VSS048	VSS155
AG13	VSS049	VSS156
AG16	VSS050	VSS157
AG18	VSS051	VSS158
AG20	VSS052	VSS159
AG22	VSS053	VSS160
AG23	VSS054	VSS161
AG24	VSS055	VSS162
AG25	VSS056	VSS163
AG26	VSS057	VSS164
AG27	VSS058	VSS165
AH2	VSS059	VSS166
AH4	VSS060	VSS167
AH7	VSS061	VSS168
AH9	VSS062	VSS169
AH2	VSS063	VSS170
AH22	VSS064	VSS171
AH25	VSS065	VSS172
AH28	VSS066	VSS173
AH29	VSS067	VSS174
AH5	VSS068	VSS175
AH8	VSS069	VSS176
AH12	VSS070	VSS177
AH14	VSS071	VSS178
AH17	VSS072	VSS179
AH19	VSS073	VSS180
AH21	VSS074	VSS181
AH22	VSS075	VSS182
AH23	VSS076	VSS183
AH24	VSS077	VSS184
AH25	VSS078	VSS185
AH26	VSS079	VSS186
AH27	VSS080	VSS187
AH28	VSS081	VSS188
AH29	VSS082	VSS189
AH30	VSS083	VSS190
AH31	VSS084	VSS191
AH32	VSS085	VSS192
AH33	VSS086	VSS193
AH34	VSS087	VSS194
AH35	VSS088	VSS195
AH36	VSS089	VSS196
AH37	VSS090	VSS197
AH38	VSS091	VSS198
AH39	VSS092	VSS199
AH40	VSS093	VSS200
AH41	VSS094	VSS_NCTF01
AH42	VSS095	VSS_NCTF02
AH43	VSS096	VSS_NCTF03
AH44	VSS097	VSS_NCTF04
AH45	VSS098	VSS_NCTF05
AH46	VSS099	VSS_NCTF06
AH47	VSS100	VSS_NCTF07
AH48	VSS101	VSS_NCTF08
AH49	VSS102	VSS_NCTF09
AH50	VSS103	VSS_NCTF10
AH51	VSS104	VSS_NCTF11
AH52	VSS105	VSS_NCTF12
AH53	VSS106	VSS106

**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size: Document Number: ICH9 POWER  
 Date: Monday, July 12, 2010 Sheet 15 of 43

# DDR3 (DDR)

STD H=4.0 MM	QCI P/N
LTK	DGMK4000004
FOX	DGMK4000117



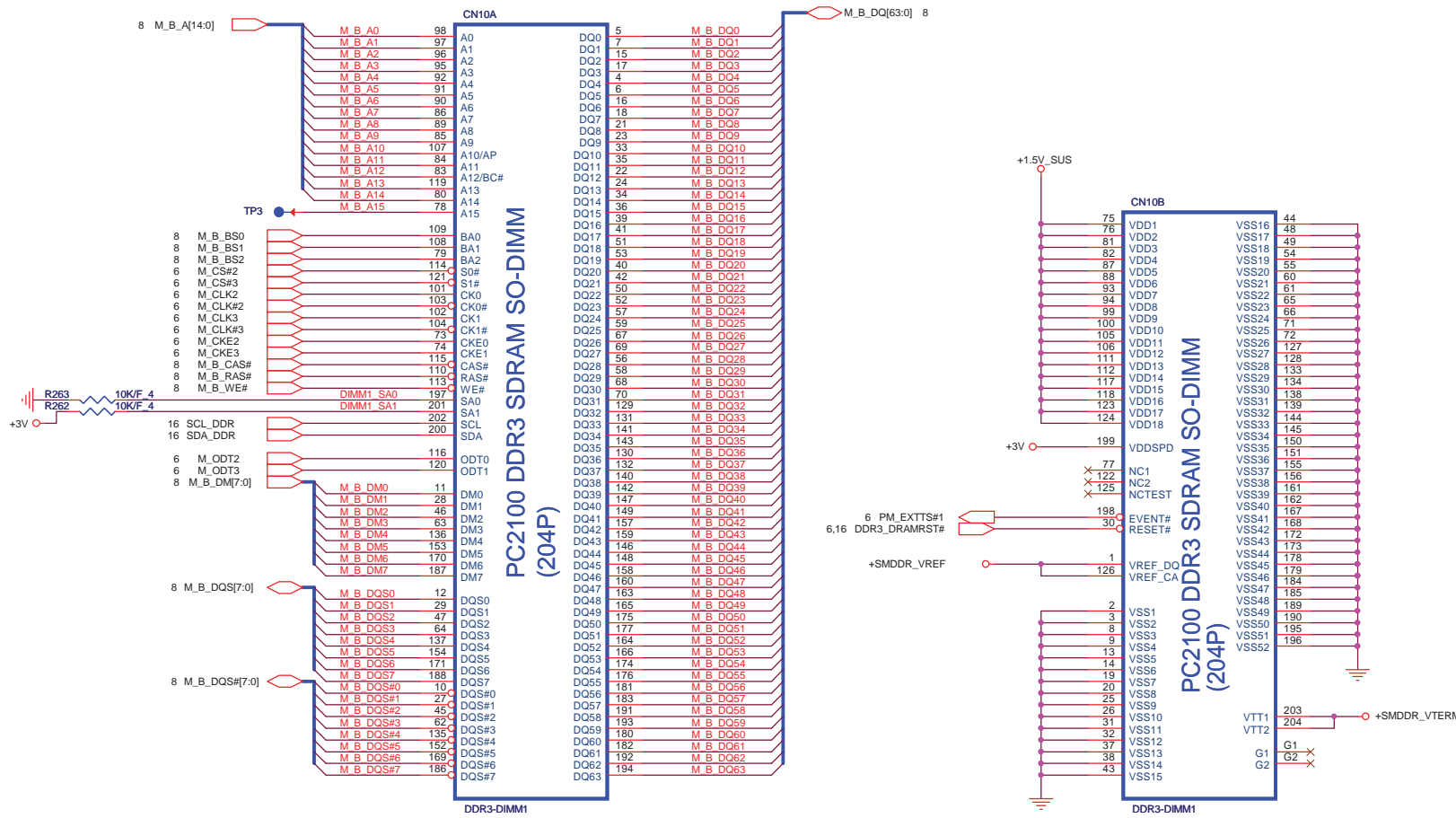
**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>DDR3 DIMM-0(H=5.2)</b>	<b>1A</b>
Date	Monday, July 12, 2010	



# DDR3 (DDR)

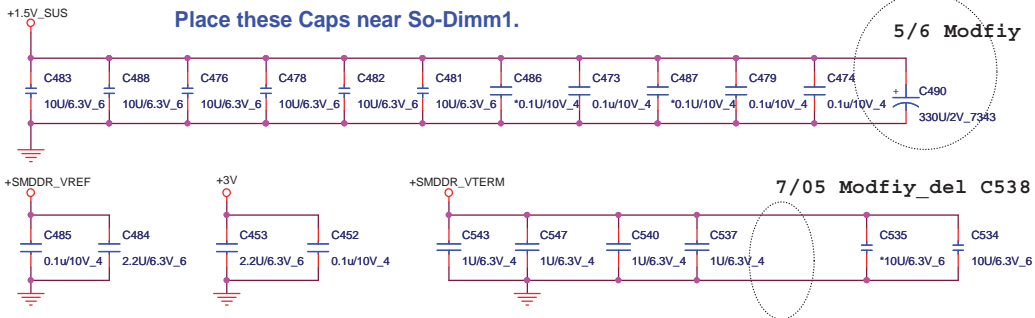
STD H=8.0 MM	QCI P/N
LTK	DGMK4000097
FOX	DGMK4000130



Place these Caps near So-Dimm1.

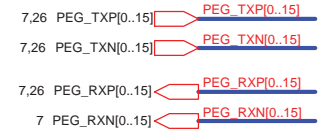
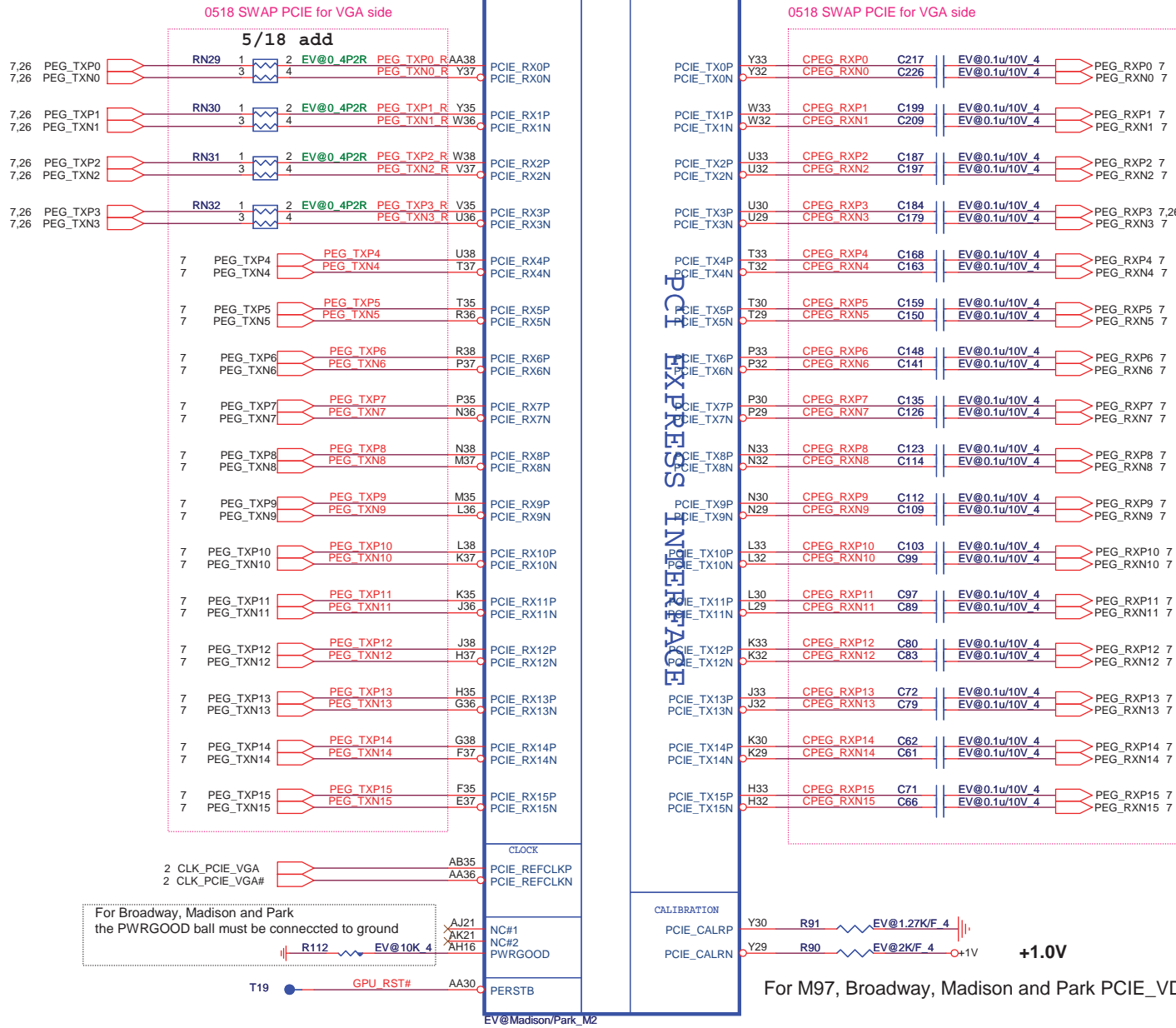
5/6 Modfiy

7/05 Modfiy\_del C538.



**PROJECT : ZQ5**  
**Quanta Computer Inc.**


Size	Document Number	Rev
	<b>DDR3 DIMM-1(H=9.2)</b>	1A
Date	Monday, July 12, 2010	Sheet 17 of 43



Item	Quanta P/N
Park	AJ077400T08
Robson	AJ007740T02

For Broadway, Madison and Park the PWRGOOD ball must be connected to ground

For M97, Broadway, Madison and Park PCIE\_VDDC is 1.0V



**Quanta Computer Inc.**  
PROJECT : ZQ5

Size	Document Number	Rev
	<b>Madison/Park M2-PCIE I/F</b>	1A
Date:	Monday, July 12, 2010	Sheet 18 of 45

GPU\_2(VGA)

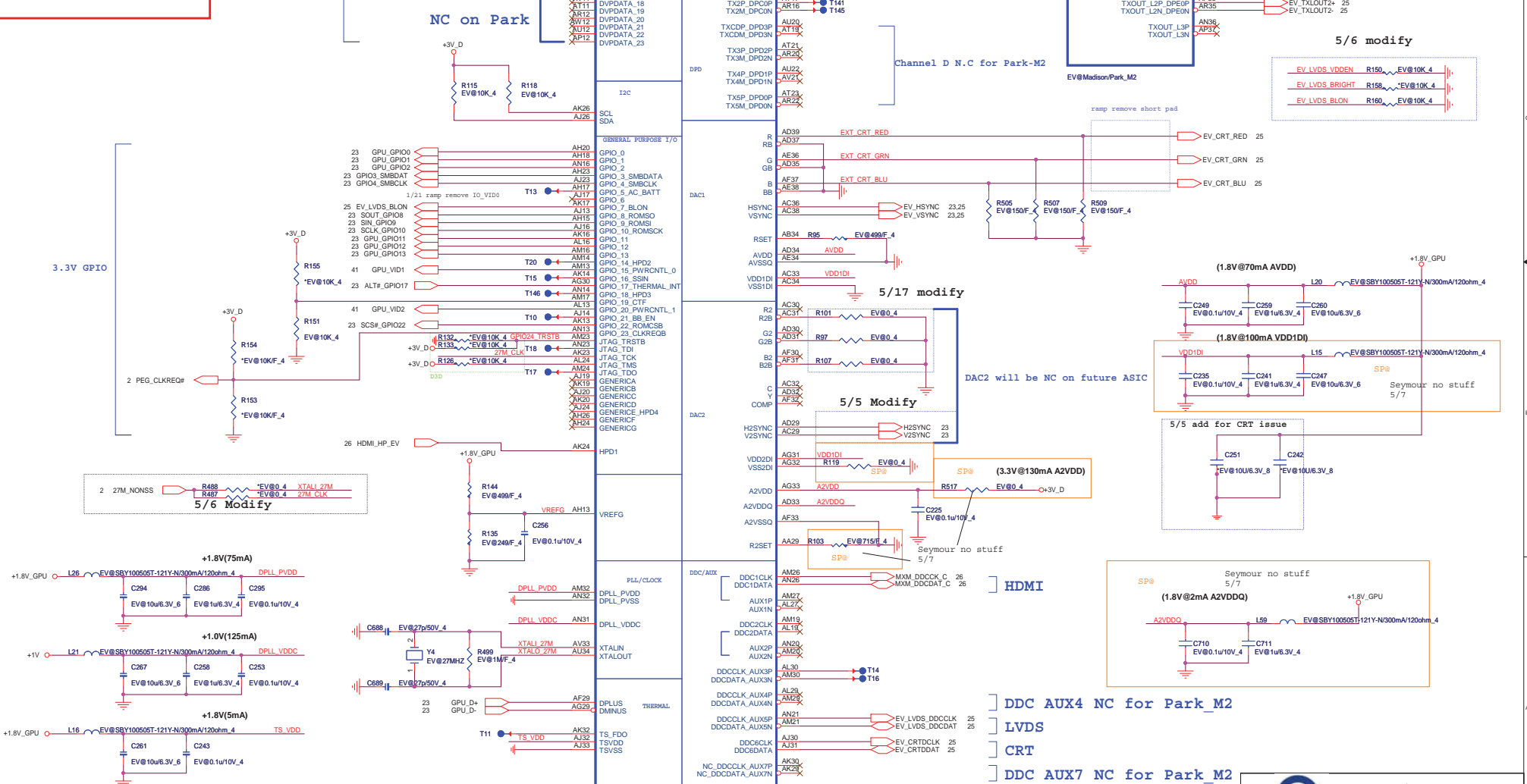
GPU Power-on sequence

- 1 => +3V\_D
- 2 => +VGPU\_CORE
- 3 => +1V
- 4 => +1.5V\_GPU
- 5 => +1.8V\_GPU
- 6 => dGPU\_PWROK


1.8V GPIO

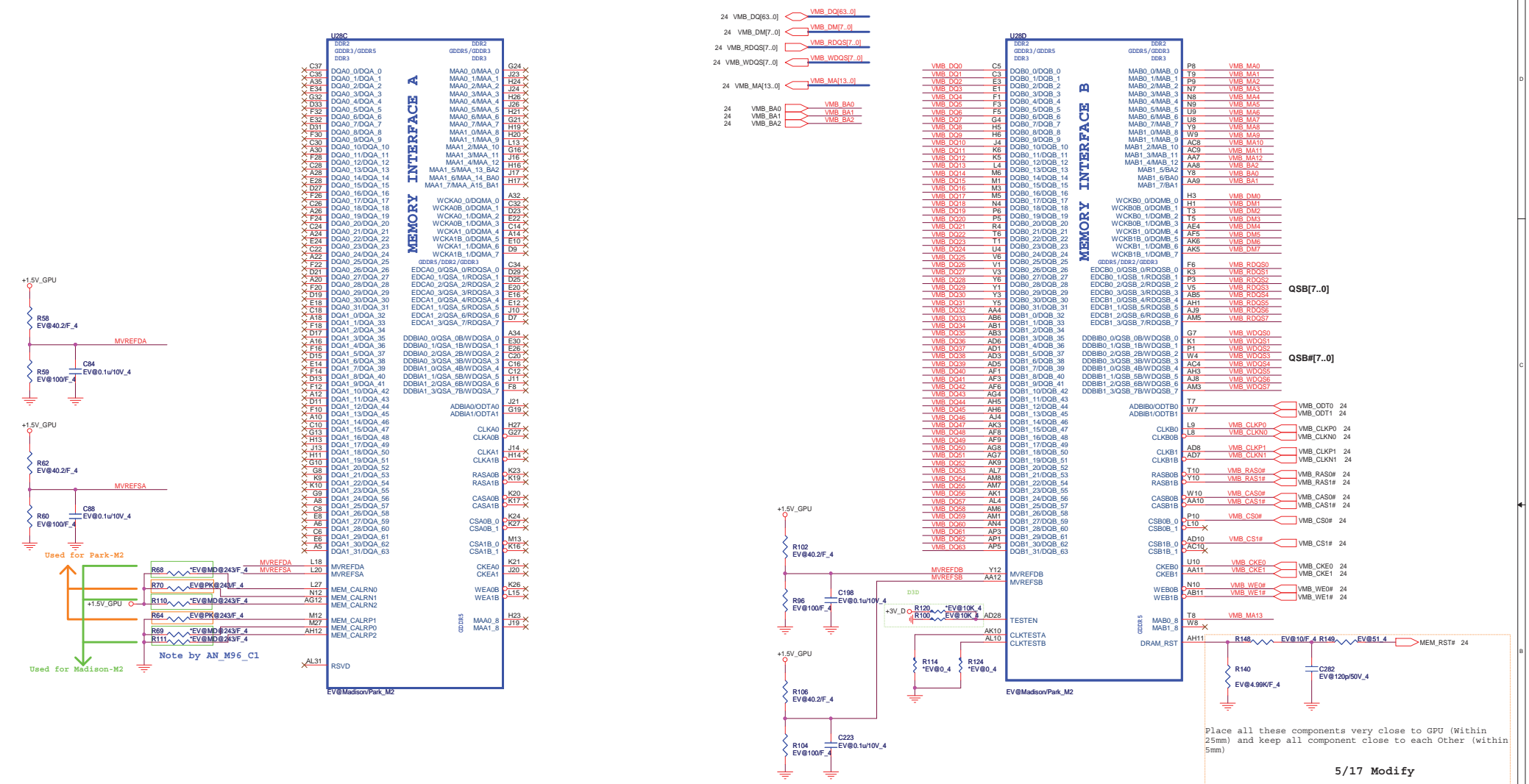
3.3V GPIO

5/6 Modify



<http://laptop-motherboard-schematic.blogspot.com/>

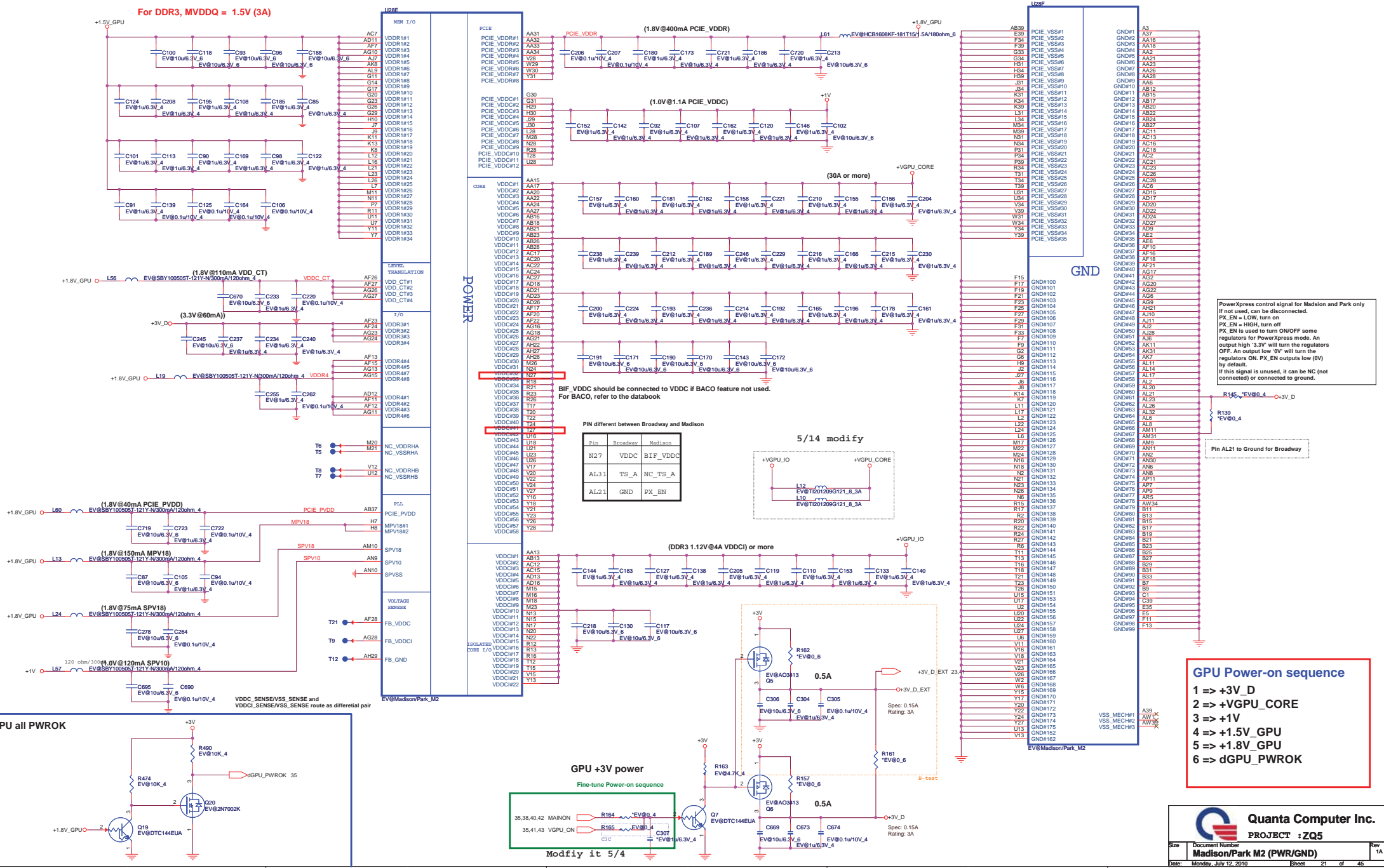

**Quanta Computer Inc.**  
 PROJECT : ZQ5  
 Size Document Number  
**Madison/Park M2-HOST I/F**  
 Date: Monday, July 12, 2010 Sheet 19 of 45



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm)

5/17 Modify

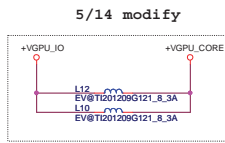
For DDR3, MVDDQ = 1.5V (3A)



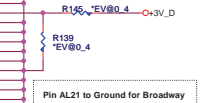
BIF\_VDDC should be connected to VDDC if BACO feature not used. For BACO, refer to the databook

Pin different between Broadway and Madison

Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	FX_EN



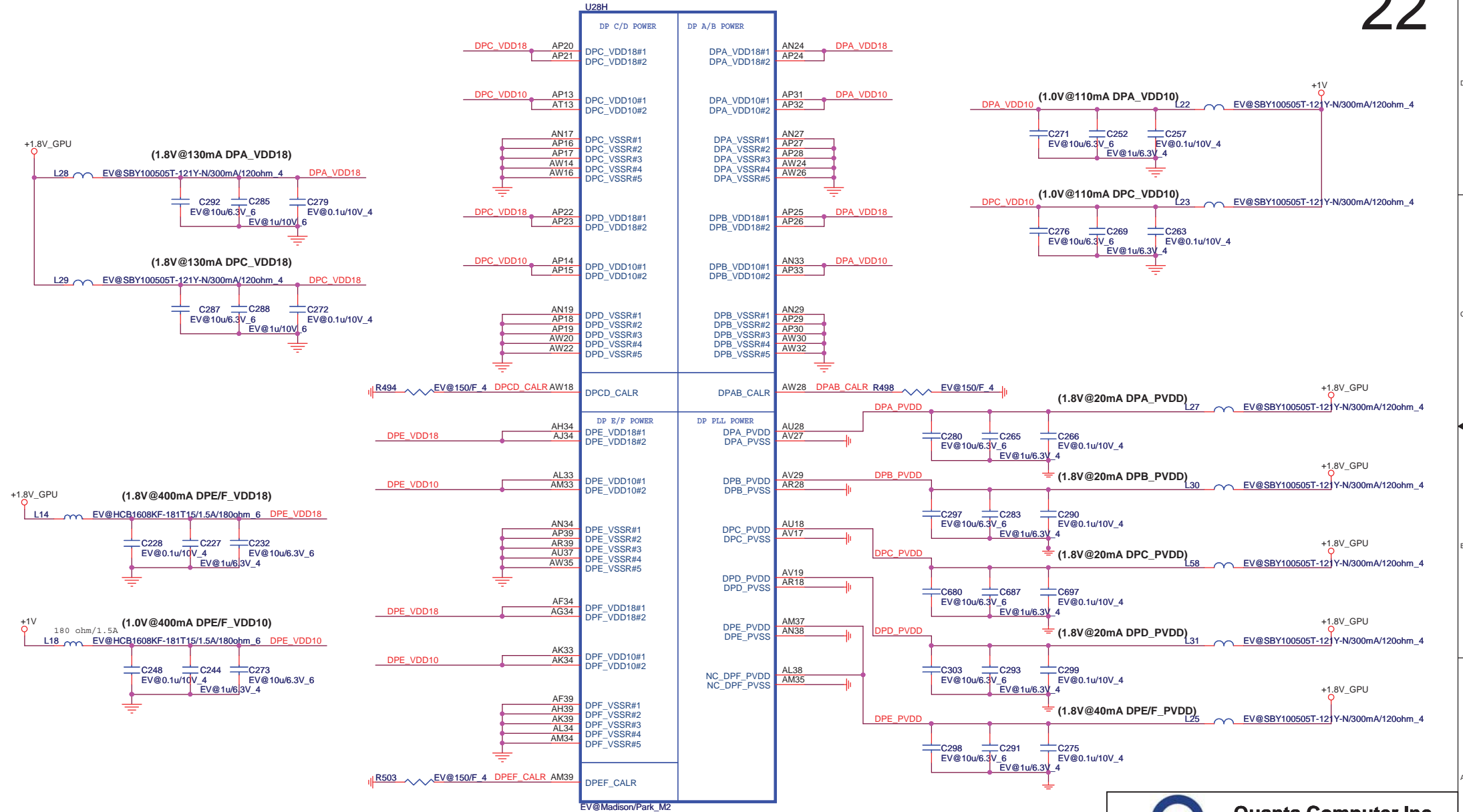
PowerXpress control signal for Madison and Park only  
 If not used, can be disconnected.  
 FX\_EN = LOW, turn on  
 FX\_EN = HIGH, turn off  
 An output high 3.3V will turn the regulators OFF. An output low 0V will turn the regulators ON. FX\_EN outputs low (0V) by default.  
 If this signal is unconnected, it can be NC (not connected) or connected to ground.



- GPU Power-on sequence**
- 1 => +3V\_D
  - 2 => +VGPU\_CORE
  - 3 => +1V
  - 4 => +1.5V\_GPU
  - 5 => +1.8V\_GPU
  - 6 => dGPU\_PWROK

**Quanta Computer Inc.**  
 PROJECT : ZQ5  
 Document Number : Madison/Park M2 (PWR/GND)  
 Date: Monday, July 12, 2010 Sheet 21 of 45 Rev 1A

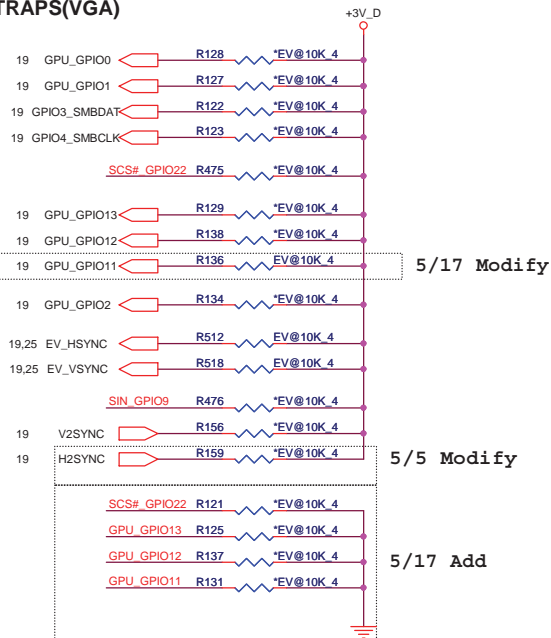
GPU\_5(VGA)



**Quanta Computer Inc.**  
**PROJECT : ZQ5**

Size	Document Number	Rev
	<b>Madison/Park M2 (DP_PWR/GND)</b>	1A
Date:	Monday, July 12, 2010	Sheet 22 of 45

**PIN STRAPS(VGA)**

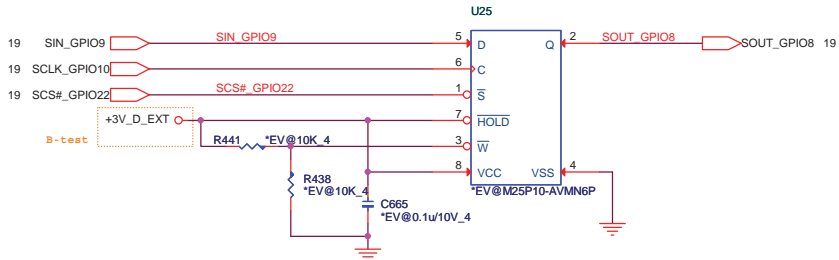


ROM Table	
Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
32 MB	011

ROM Table		
EXT_HS_SYNC	EXT_VS_SYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	1	
ROMIDCFG(2:0)	GPIO[13:11]	Primary Memory Aperture size requested at PCI Configuration	001	table 3-35
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

**EEPROM(VGA)**

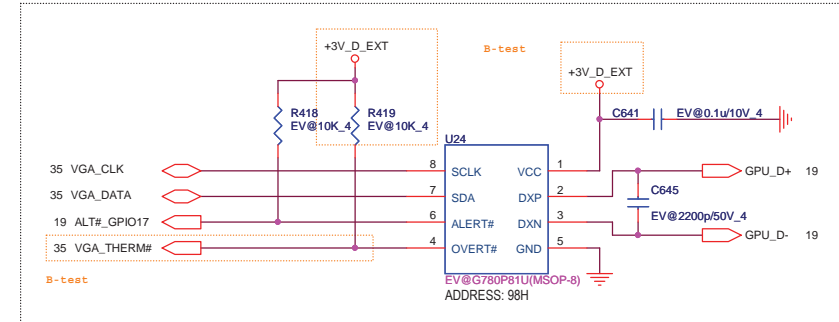


**Thermal Sensor(VGA)**

5/6 modify

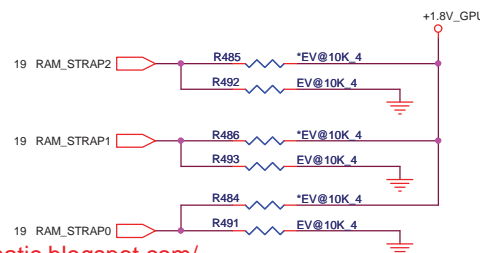
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



**DDR3 Memory Aperture size(GPU)**

DDR3 Memory Aperture size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
			1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128M*16)	0	0	1



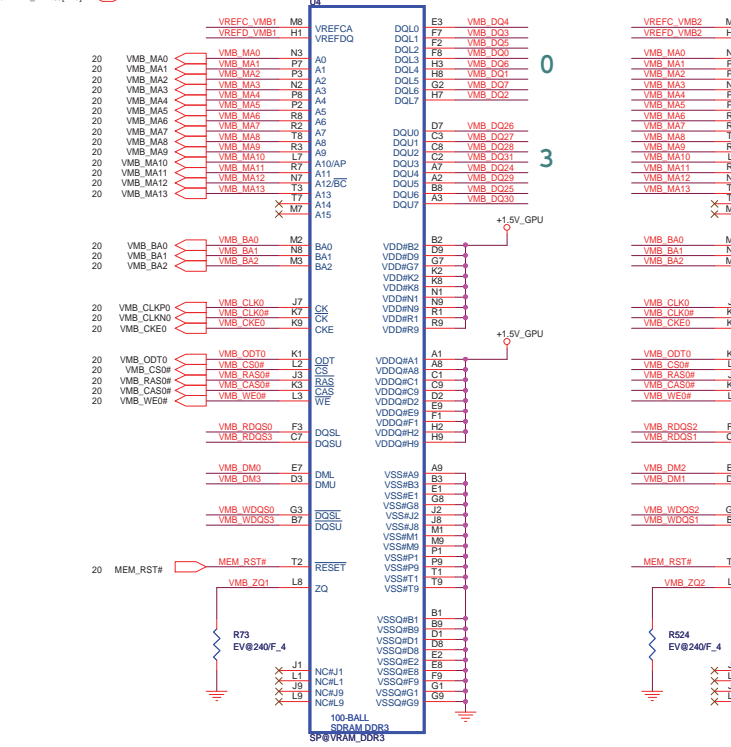
RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

**Quanta Computer Inc.**  
PROJECT : ZQ5

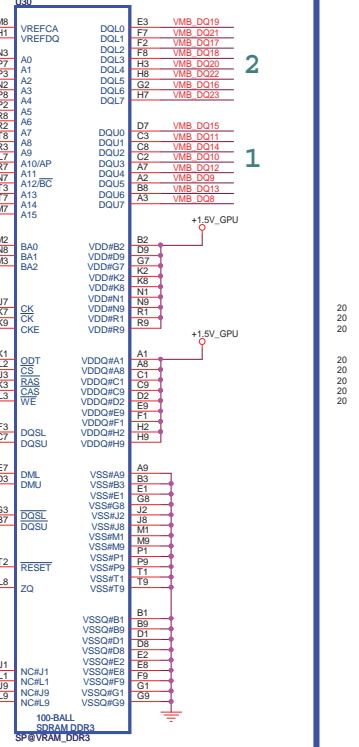
Size	Document Number	Rev
	Strip/Thermal	1A
Date:	Monday, July 12, 2010	Sheet 23 of 45

20 VMB\_DQ[63..0]  
20 VMB\_DM[7..0]  
20 VMB\_RDSQ[7..0]  
20 VMB\_WDQS[7..0]

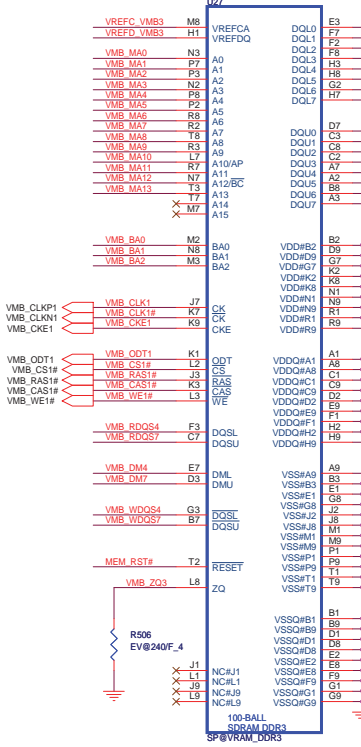
QSA7[..0]  
QSA#7[..0]



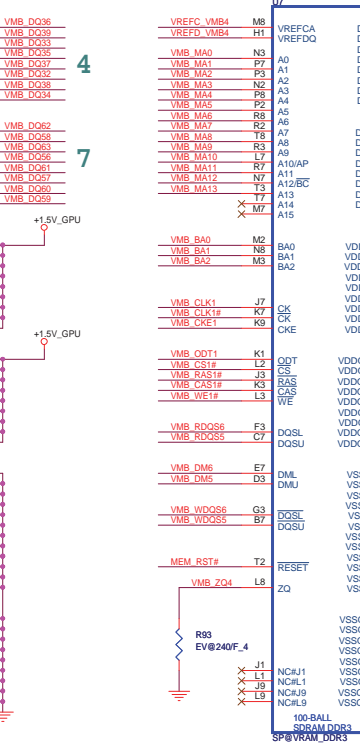
BOT Down



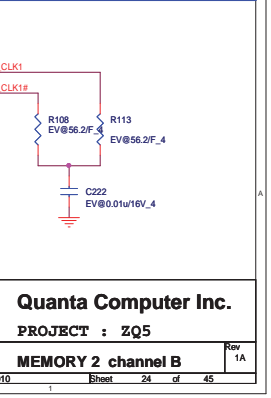
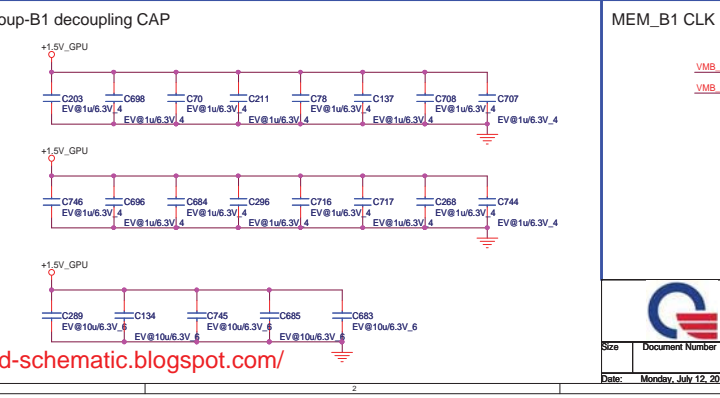
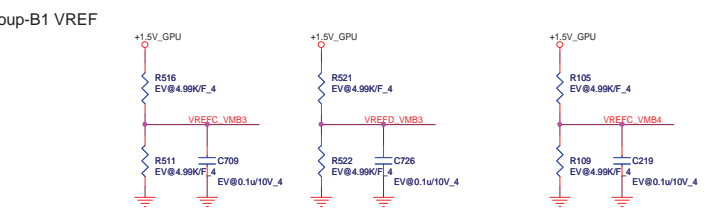
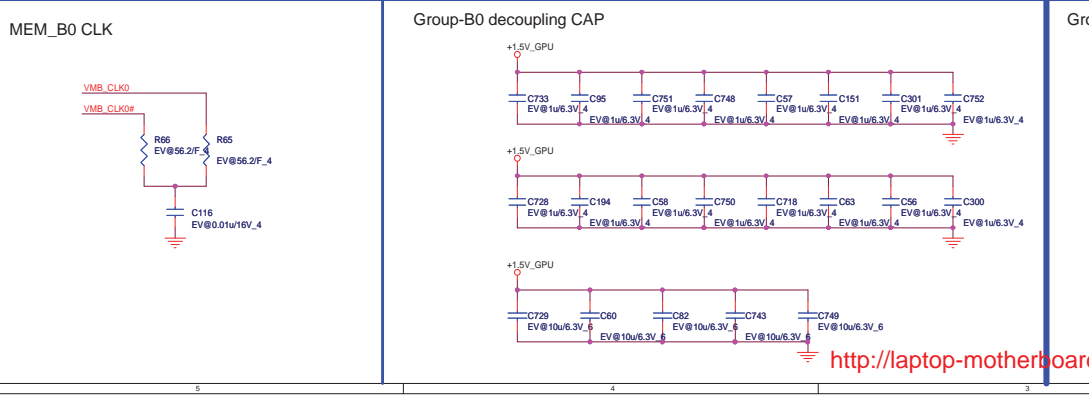
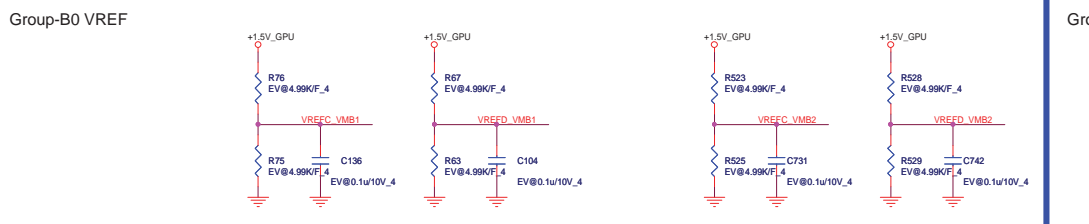
TOP Down



TOP Up



BOT Up



<http://laptop-motherboard-schematic.blogspot.com/>

**Quanta Computer Inc.**  
PROJECT : ZQ5  
Sheet 24 of 45  
Date: Monday, July 12, 2010

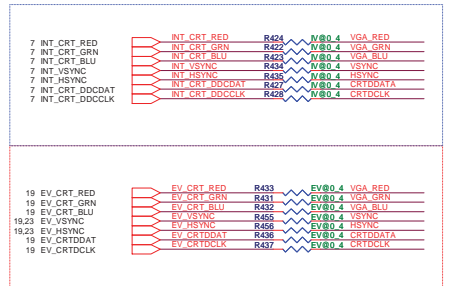


### CRT Switch

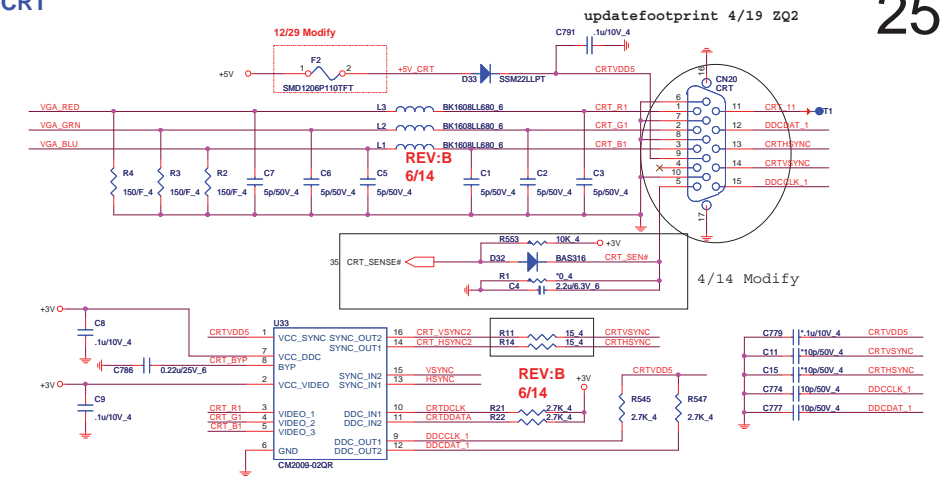
IV@ -> iGPU only  
EV@ -> dGPU only

iGPU only

4/16  
dGPU only

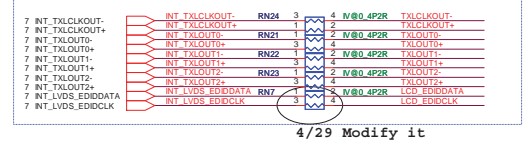


### CRT

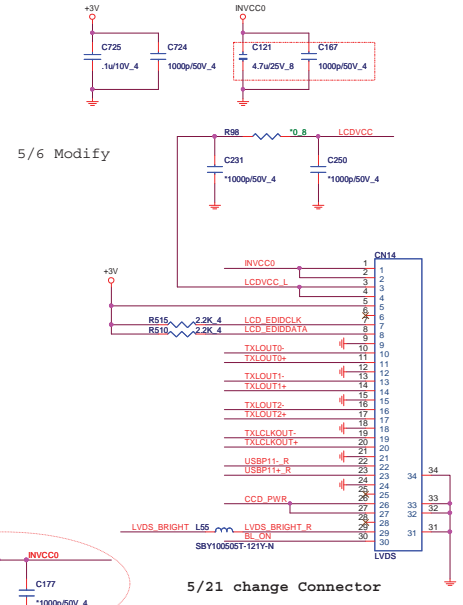
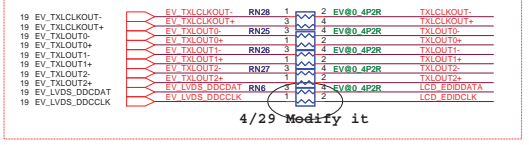


### LVDS

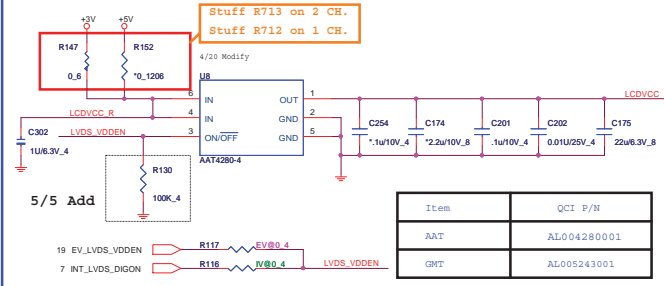
iGPU only 5/11 Swap net



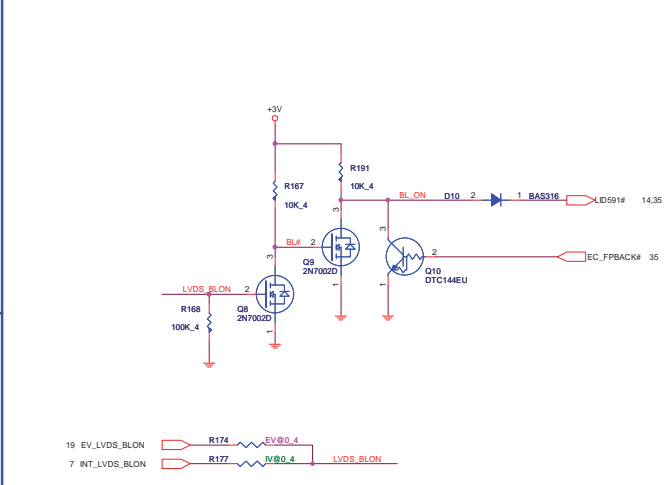
dGPU only 5/11 Swap net



### LCD\_ON (LCD Power)



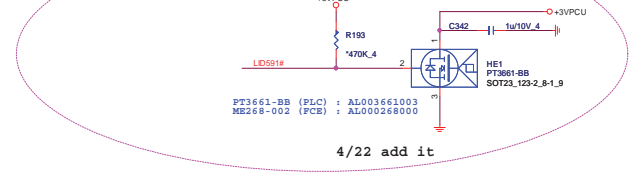
### Backlight Control



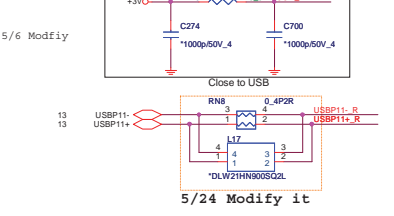
### Brightness



### Lid Switch (HSR)

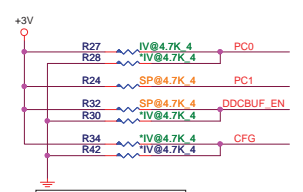
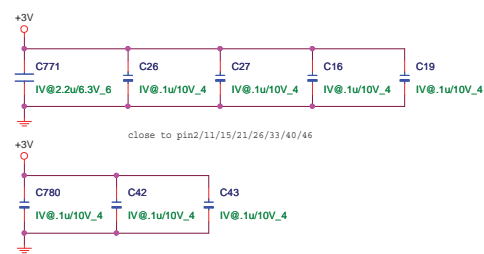


### CCD



### IGPU HDMI LEVEL SHIFTER

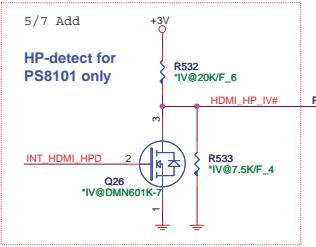
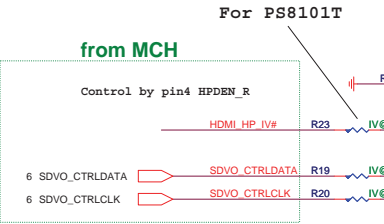
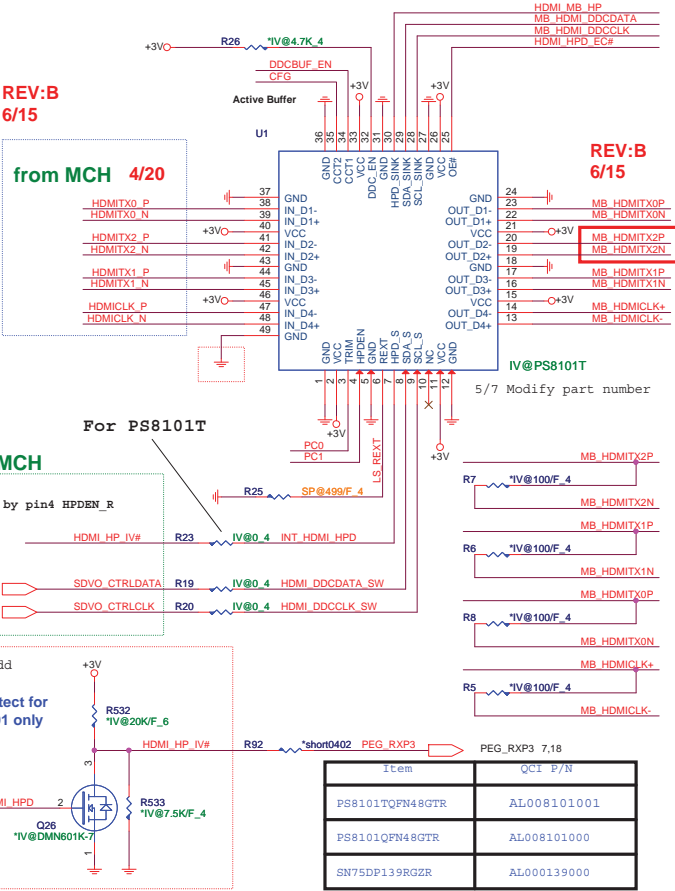
IV@ --> iGPU only  
EV@ --> dGPU only



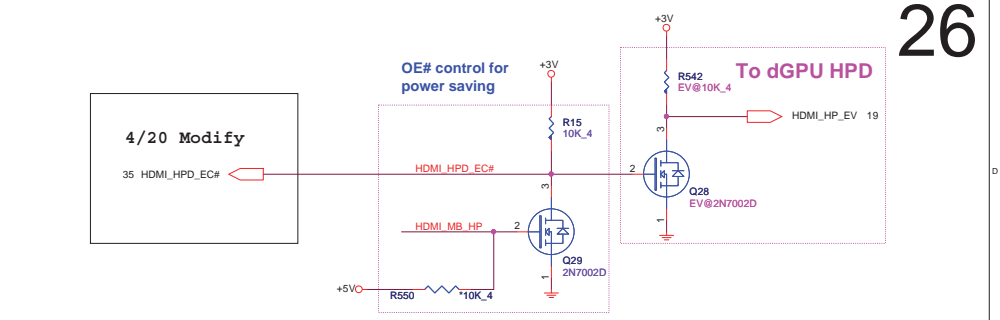
Equalization Control		
PC1	PCd	EQ Control
L	L	8dB
L	L	4dB
H	L	12dB
H	H	0dB

PC0 internal PD  
PC1 internal PD  
DDCBUF\_EN internal PD  
CFG internal PD  
DDC\_EN internal PU

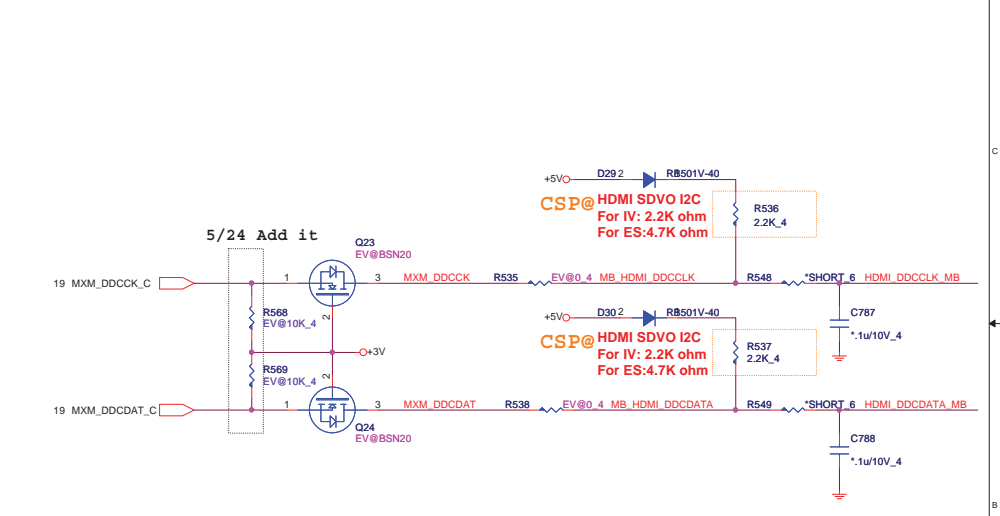
- SP@SN75DP139  
1. Pin34 HPDINV for 8101T Stuff R32  
2. Stuff R24  
3. R25 change 3.9K (CS23902FB14)



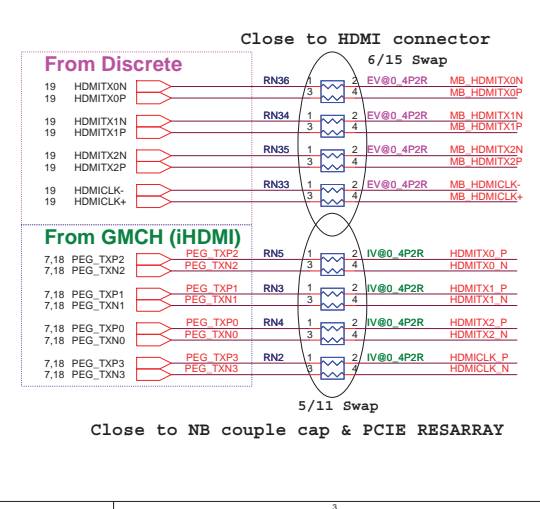
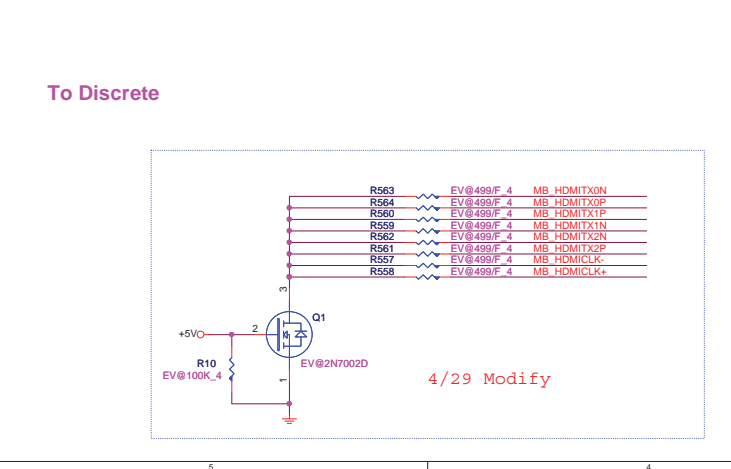
Item	QCI P/N
PS8101TQFN48GTR	AL008101001
PS8101QFN48GTR	AL008101000
SN75DP139RGZR	AL000139000



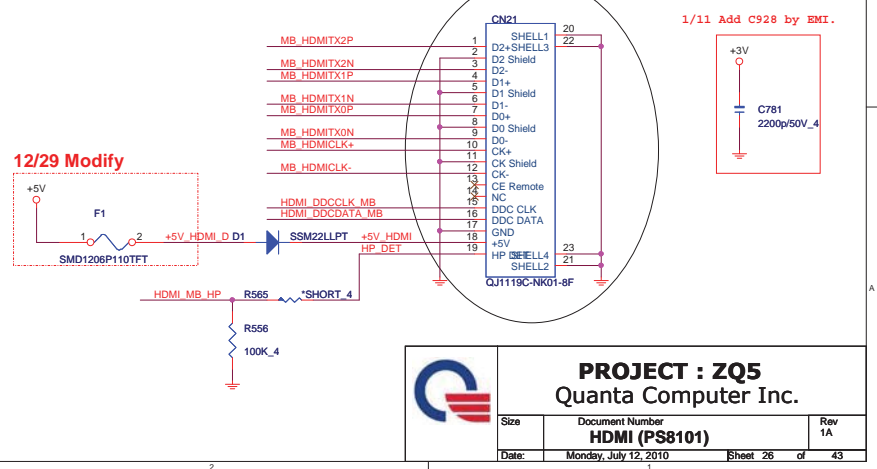
### SDVO I2C Control



### GPU Switchable Graphic HDMI source



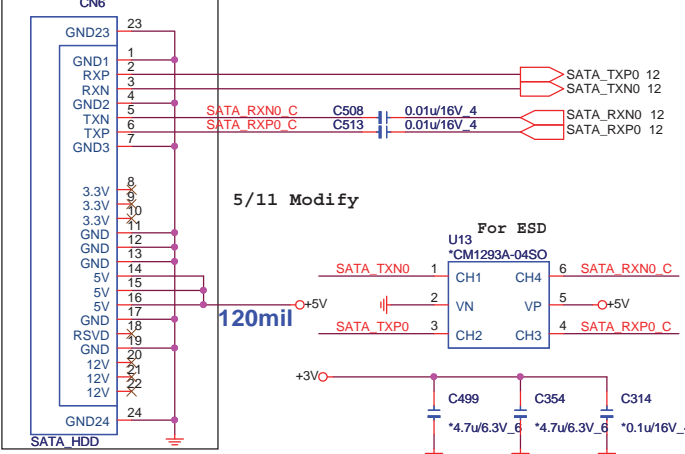
### HDMI connector



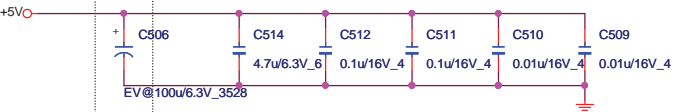
**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>HDMI (PS8101)</b>	1A
Date:	Monday, July 12, 2010	Sheet 26 of 43

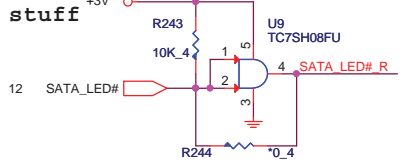
## SATA HDD(HDD)



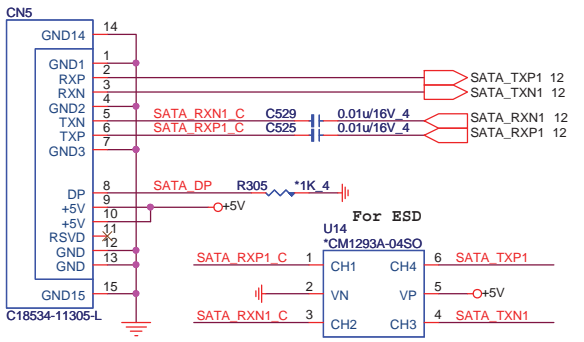
### 5/4 change footprint (ZQ2)



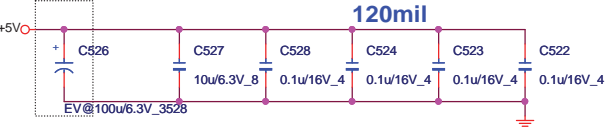
### 5/12 UMA no stuff



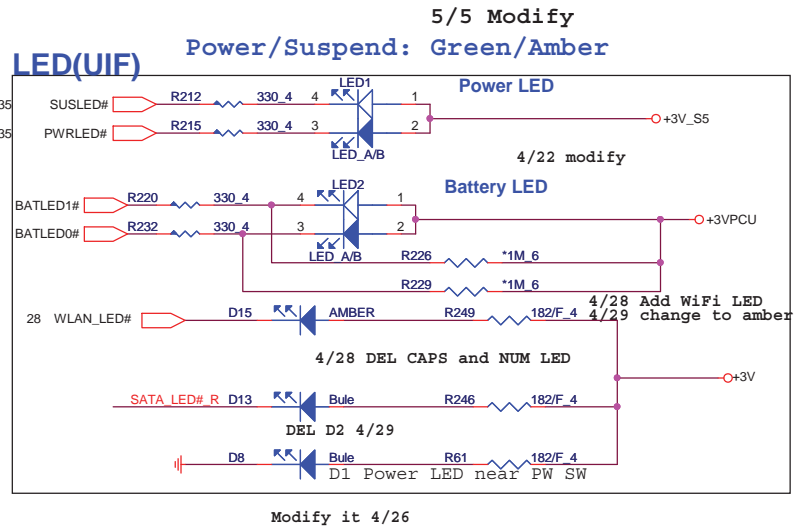
## SATA ODD(ODD)



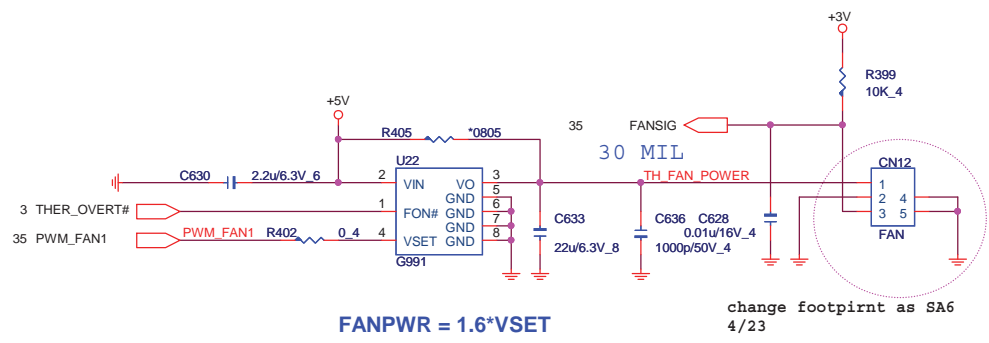
### 5/12 UMA no stuff



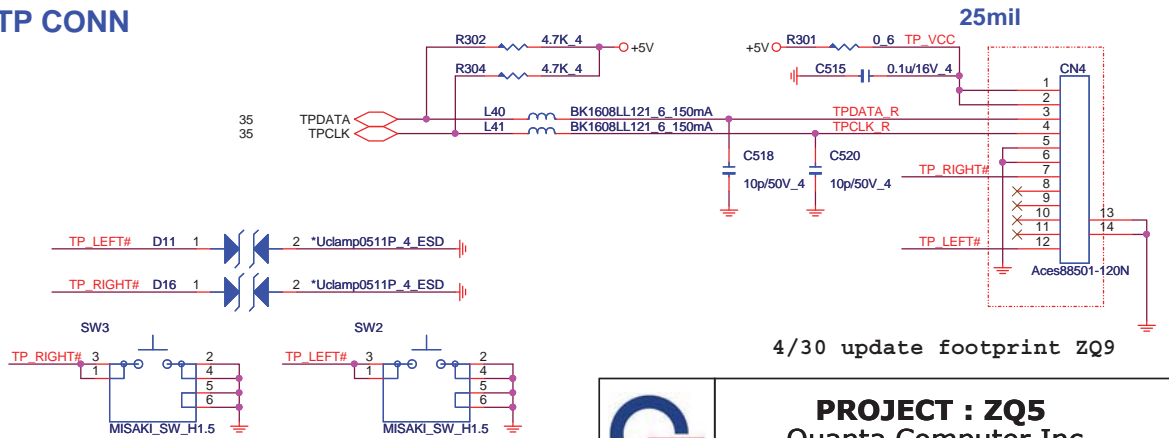
## LED(UIF)



## FAN(THM)



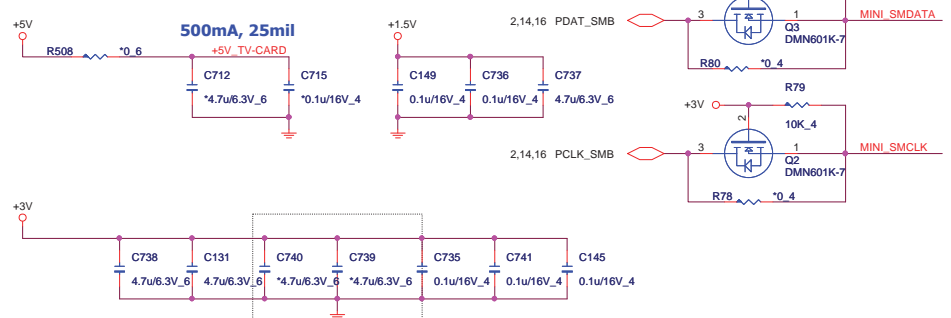
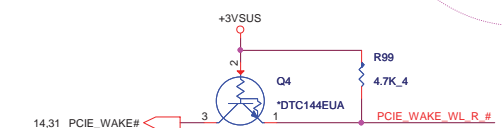
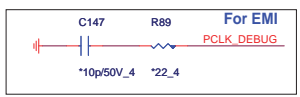
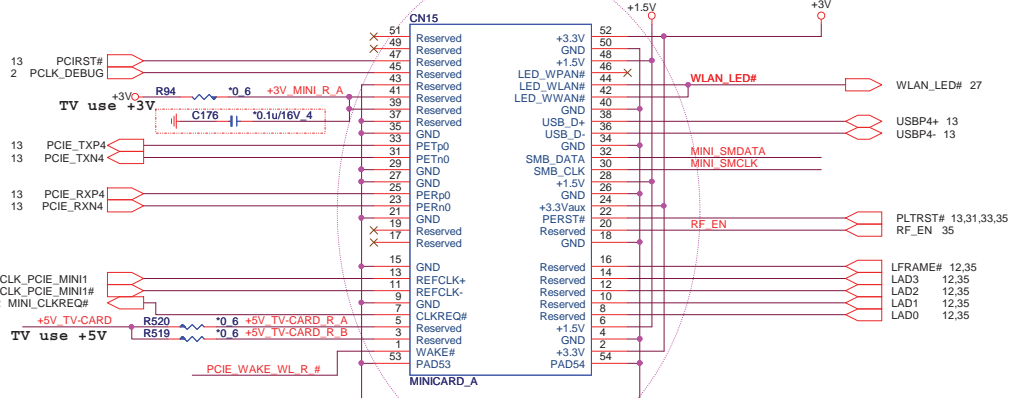
## TP CONN



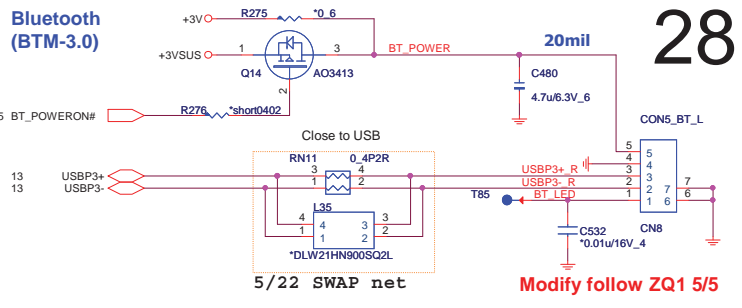
	<b>PROJECT : ZQ5</b>		Rev 1A
	Quanta Computer Inc.		
Size	Document Number		Sheet 27 of 43
Date:	Monday, July 12, 2010		

# MINI-CARD(MPC)

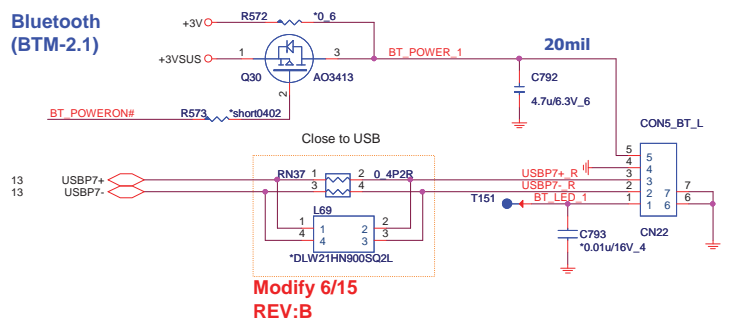
4/21 change footprint andy(ZYD) H=7.0



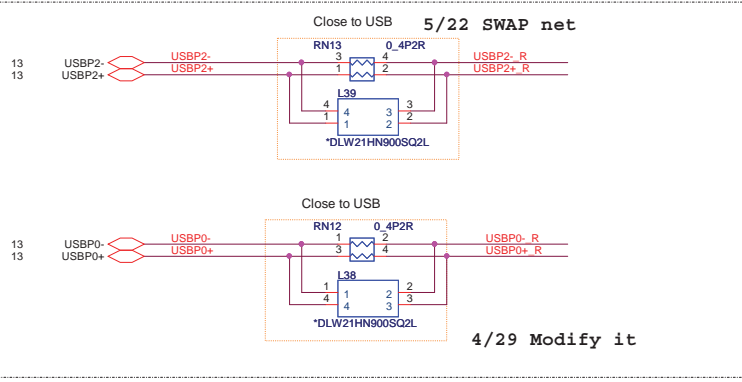
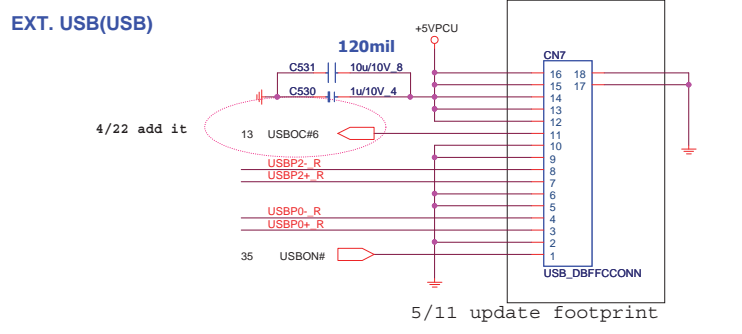
## Bluetooth (BTM-3.0)



## Bluetooth (BTM-2.1)

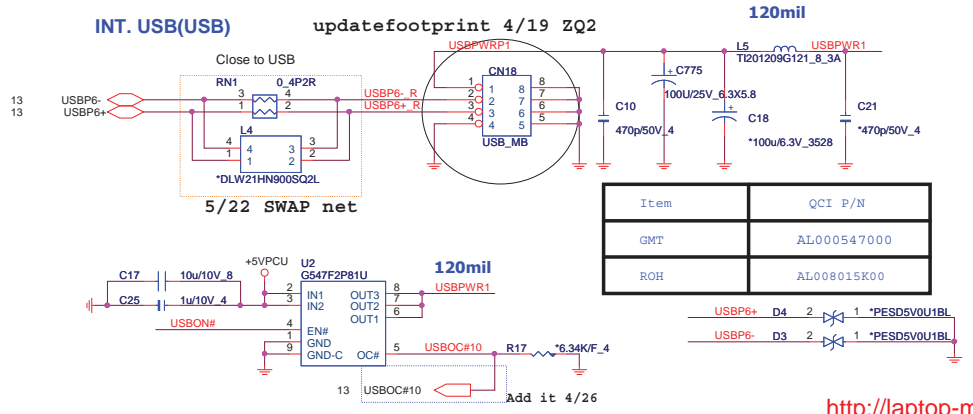


## EXT. USB(USB)



## INT. USB(USB)

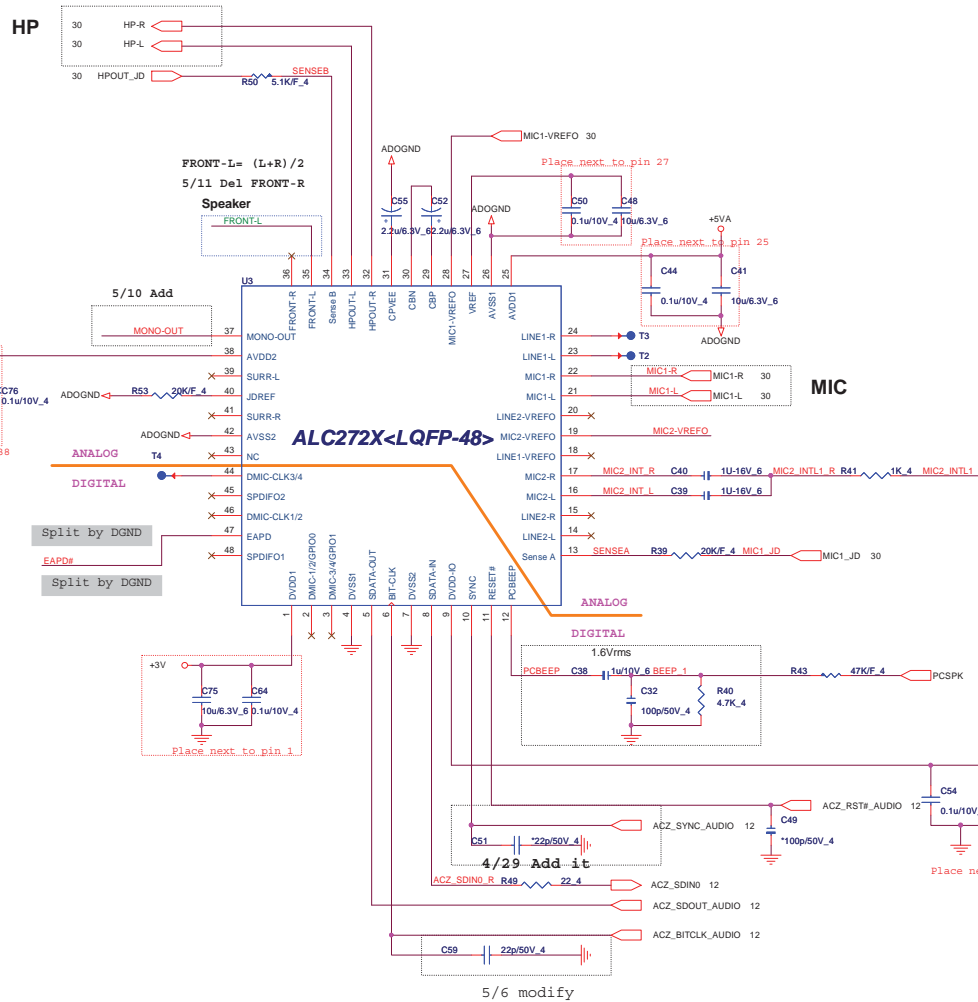
update footprint 4/19 ZQ2



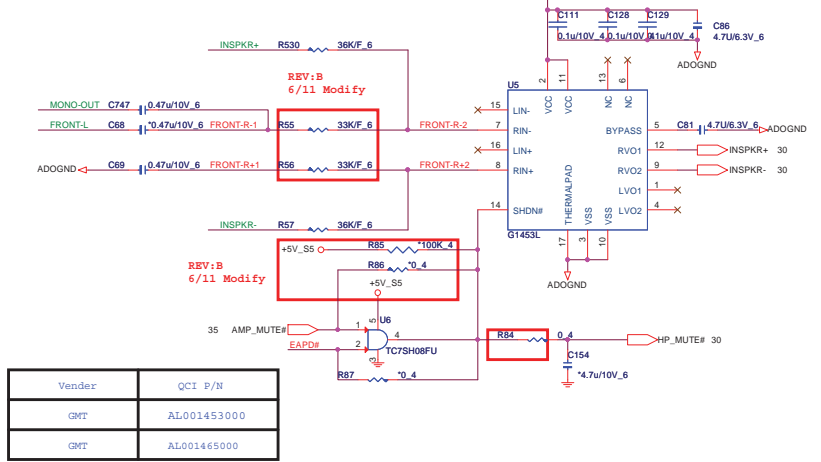
**PROJECT : ZQ5**  
 Quanta Computer Inc.

Size	Document Number	Rev
Date	MINI/USB/BT/HOLE	1A
Monday, July 12, 2010	Sheet	28 of 43

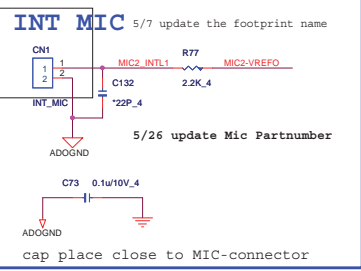
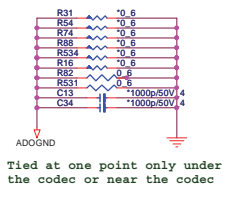
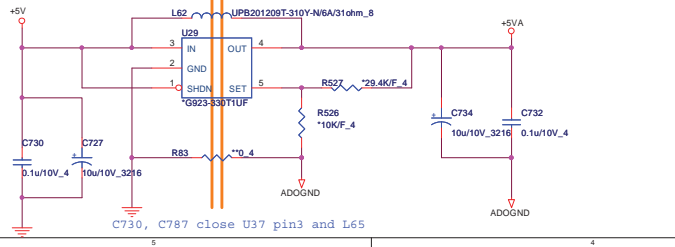
Codec(ADO)



MUTE(AMP)  
5/11 Modfiy it

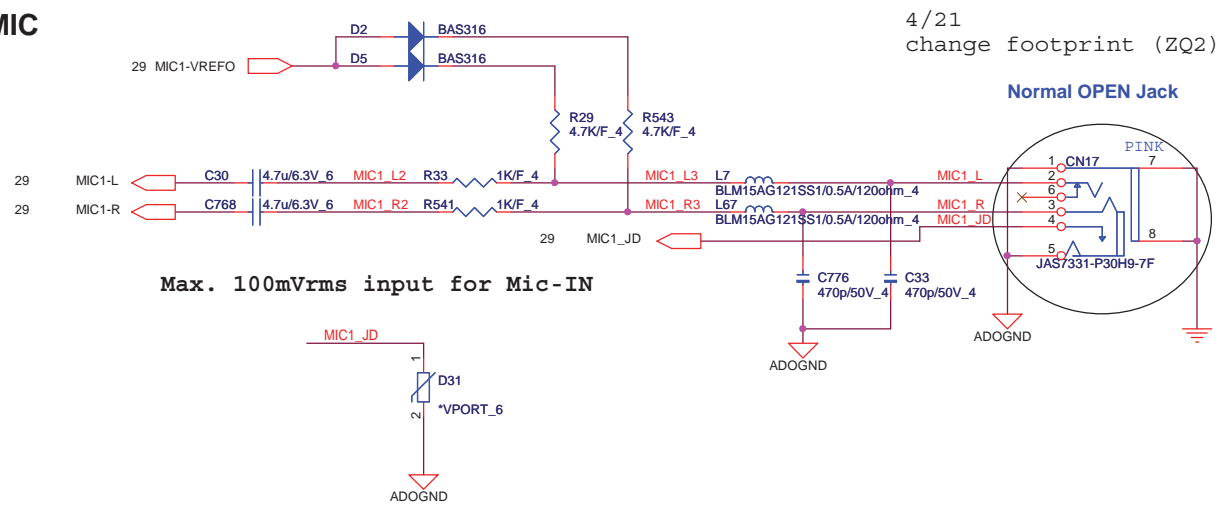


Power (ADO)

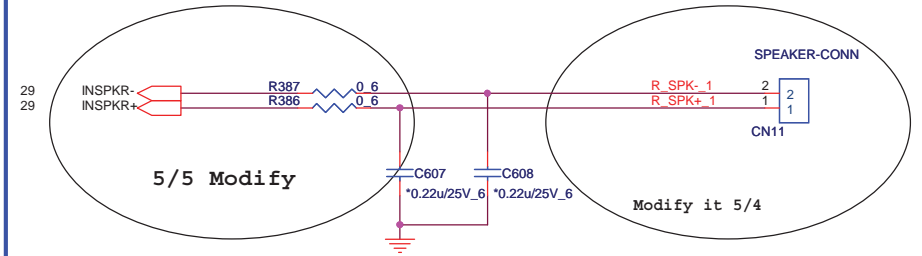


**PROJECT : ZQ5**  
Quanta Computer Inc.

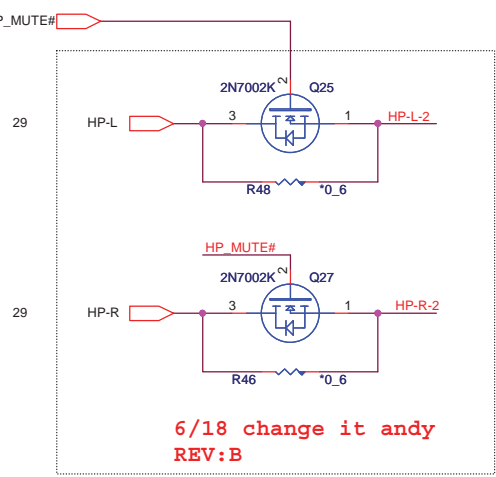
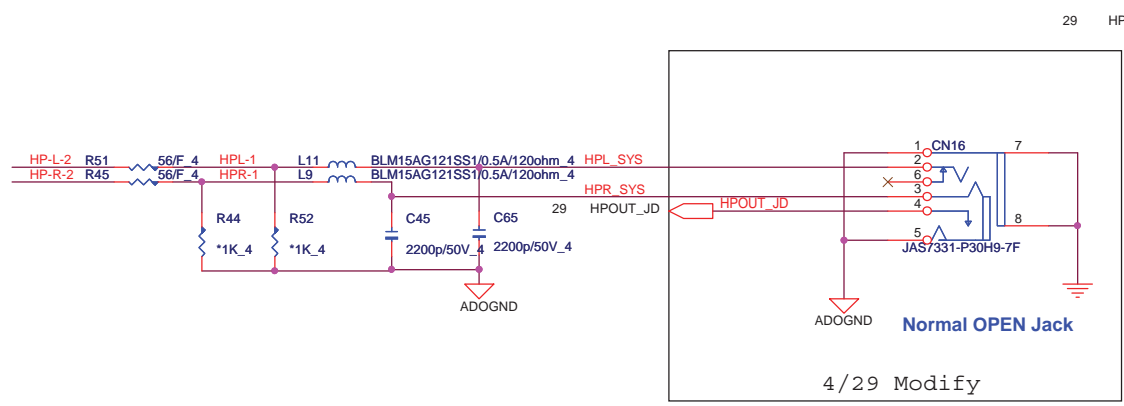
Size: Document Number: REALTEK ALC663&888/MDC Rev 1A  
Date: Monday, July 12, 2010 Sheet 29 of 43



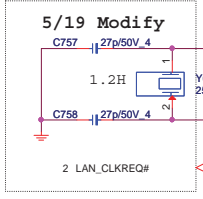
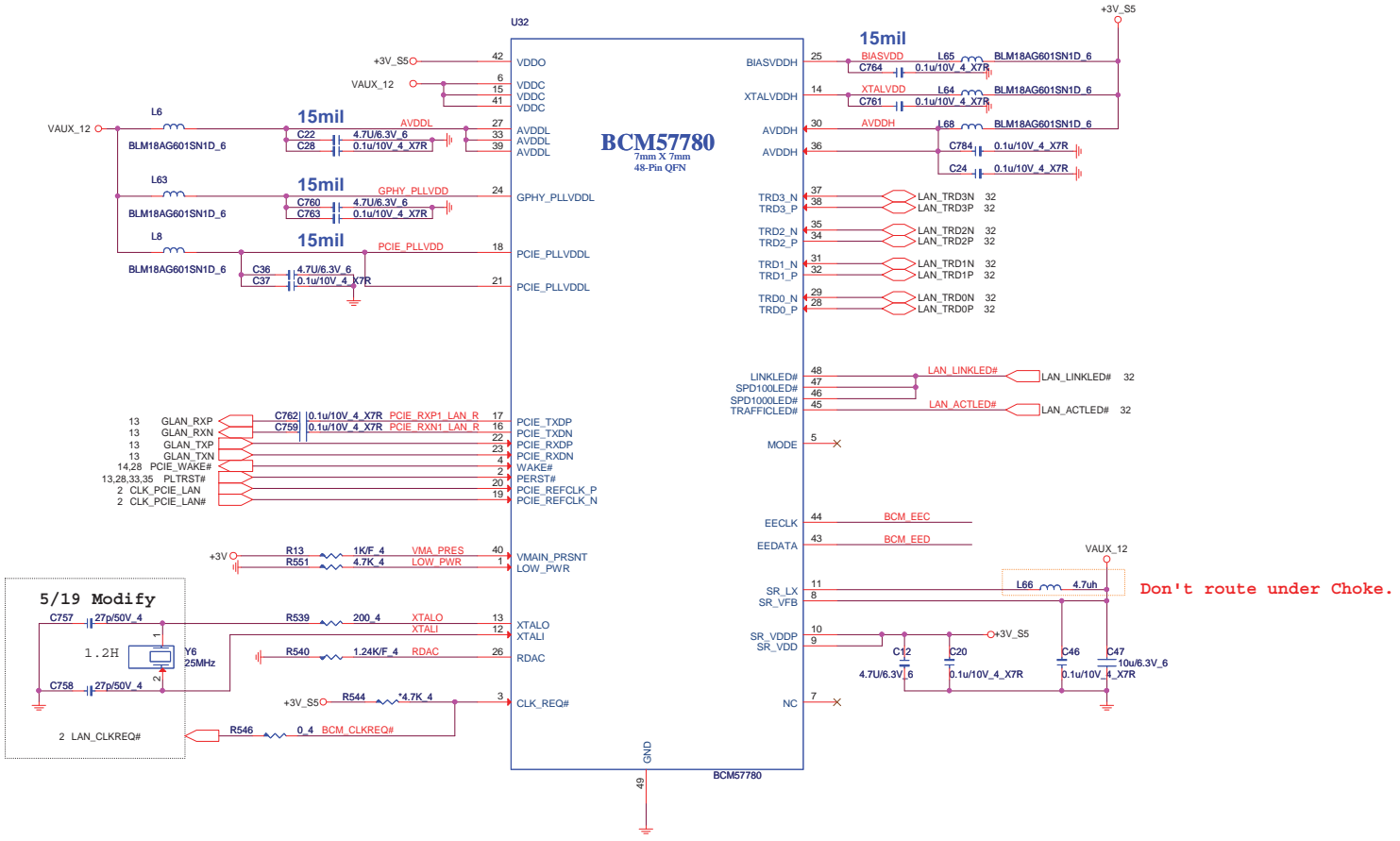
Internal Speaker



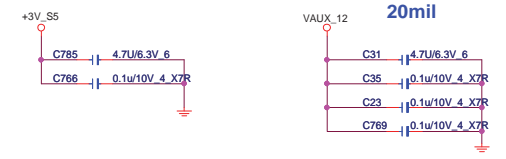
HP/SPDIF



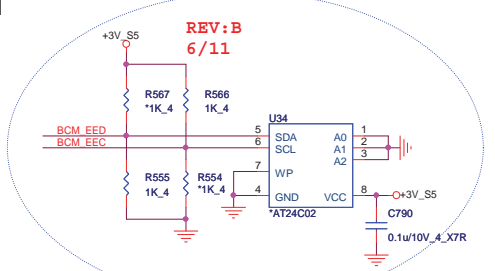
			<b>PROJECT : ZQ5</b>		
			Quanta Computer Inc.		
Size	Document Number		Rev		
	<b>AMP /AUDIO JACK CONN</b>		1A		
Date:	Monday, July 12, 2010		Sheet	30	of 43



**LAN POWER**



**EEPROM**



**EEPROM Strapping**

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

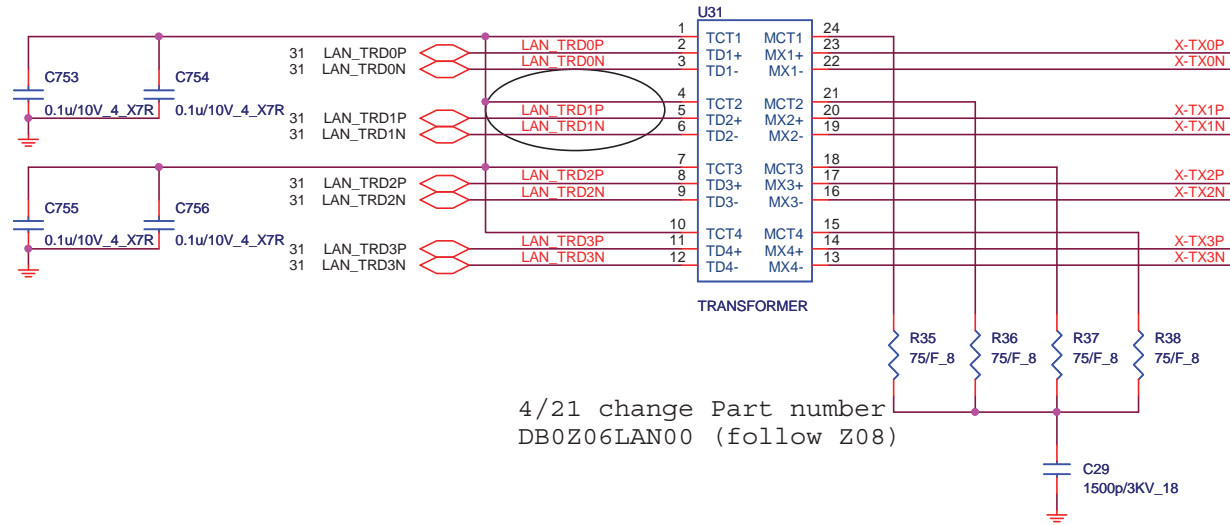
<http://laptop-motherboard-schematic.blogspot.com/>

**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>GLAN BCM57780</b>	1A
Date:	Monday, July 12, 2010	Sheet 31 of 43

# TRANSFORMER

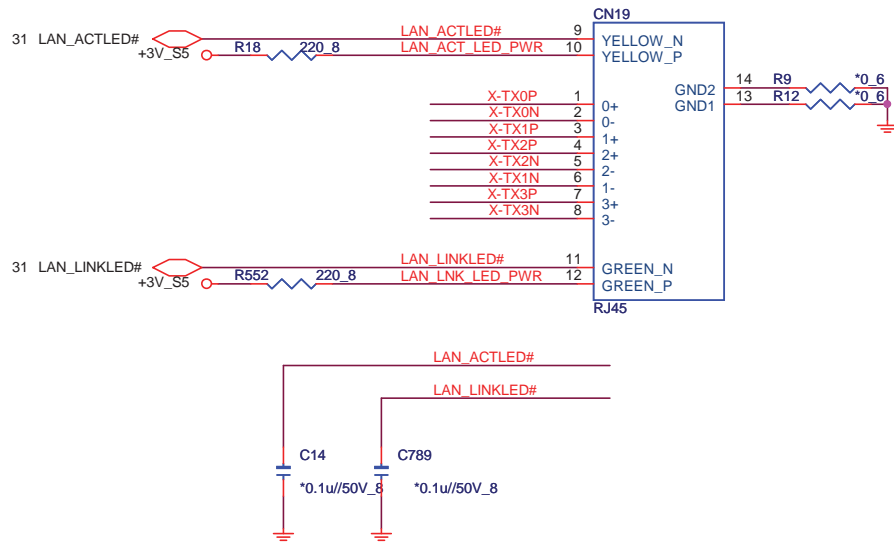
4/27 modify it



4/21 change Part number  
DB0Z06LAN00 (follow Z08)

# RJ45 Conn

For EMI



LAN_TRD0P	C765	*10p/50V_4
LAN_TRD0N	C767	*10p/50V_4
LAN_TRD1P	C772	*10p/50V_4
LAN_TRD1N	C770	*10p/50V_4
LAN_TRD2P	C773	*10p/50V_4
LAN_TRD2N	C778	*10p/50V_4
LAN_TRD3P	C782	*10p/50V_4
LAN_TRD3N	C783	*10p/50V_4



**PROJECT : ZQ5**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>LAN Transformer and RJ45</b>	1A
Date:	Monday, July 12, 2010	Sheet 32 of 43

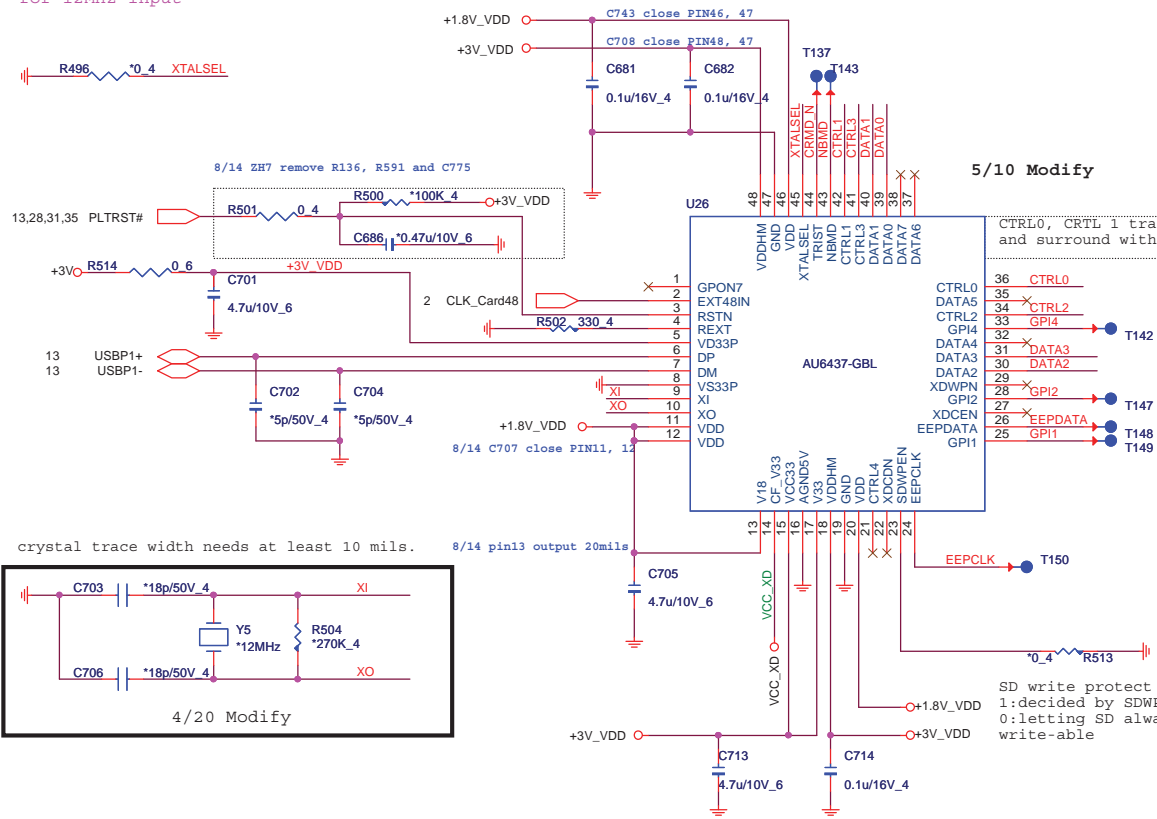


# CARD READER Controller

# 2 IN 1 CARD READER (SD/MMC)

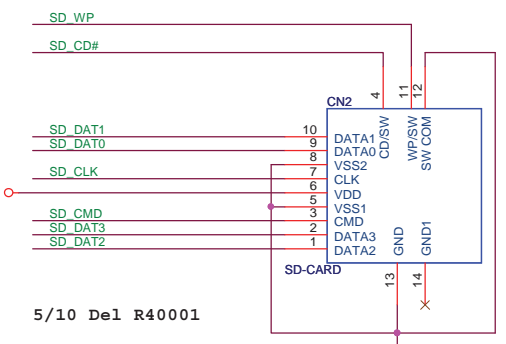
# 33

Clock input selection  
 '1' for 48MHz input [Default, Internal PU]  
 '0' for 12MHz input

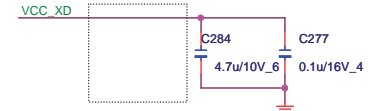


5/10 modify

Main	DFHS11FR011
Second	DFHS11FR033

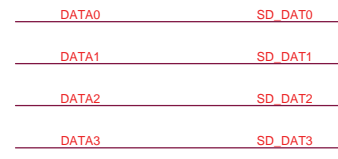


5/10 Del R40001

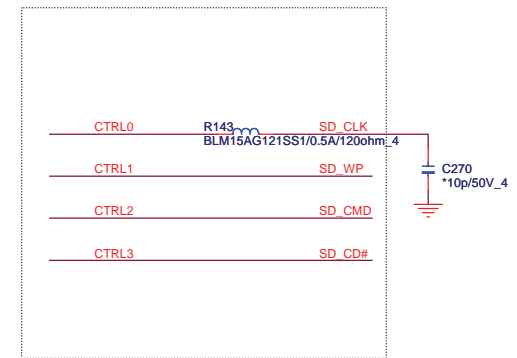


Close to CN14 pin 14 & pin23  
 4.7u CAP close to pin23

5/10 change Card Redaer conn  
 footprint sdcard-sdsn09-08-xa-11p-smt



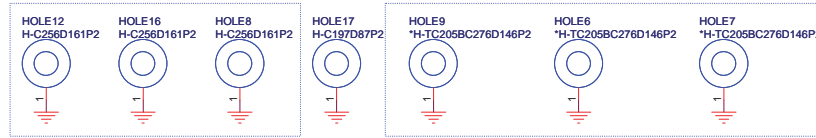
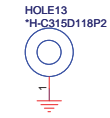
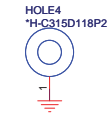
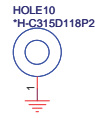
Close to connector



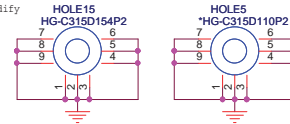
**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size	Document Number <b>AU6433 CardReader</b>	Rev 1A
Date:	Monday, July 12, 2010	Sheet 33 of 43

(OTH)

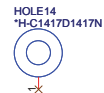
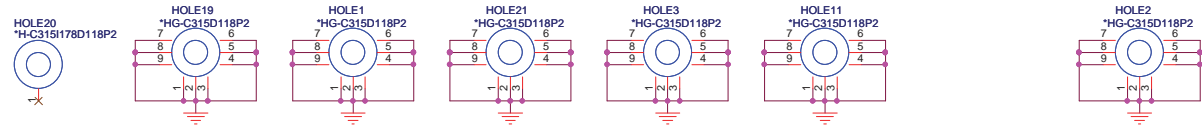


5/21 Modify

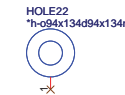


5/25 Modify

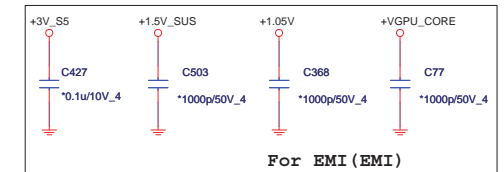
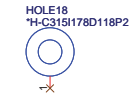
5/21 Modify



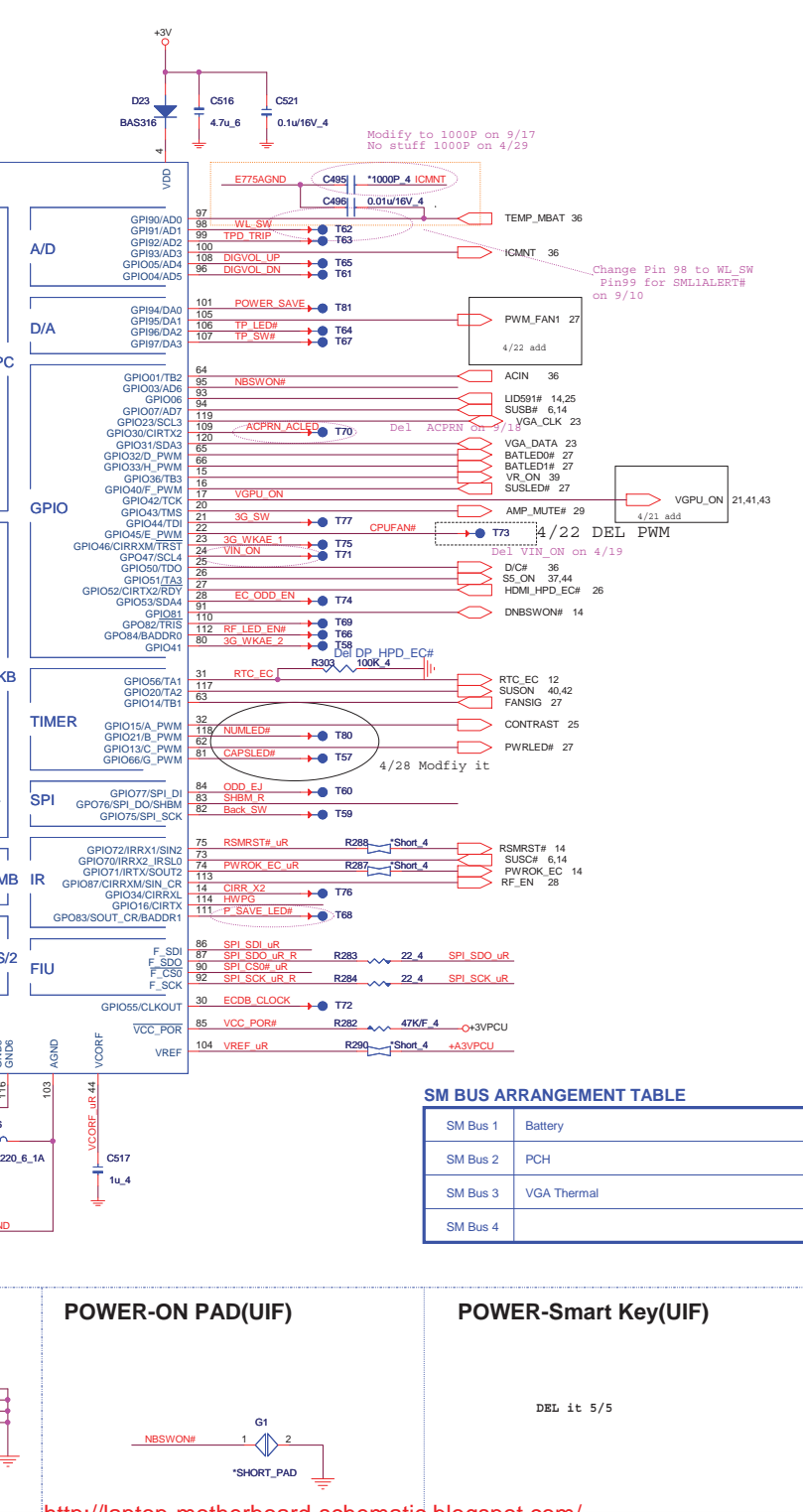
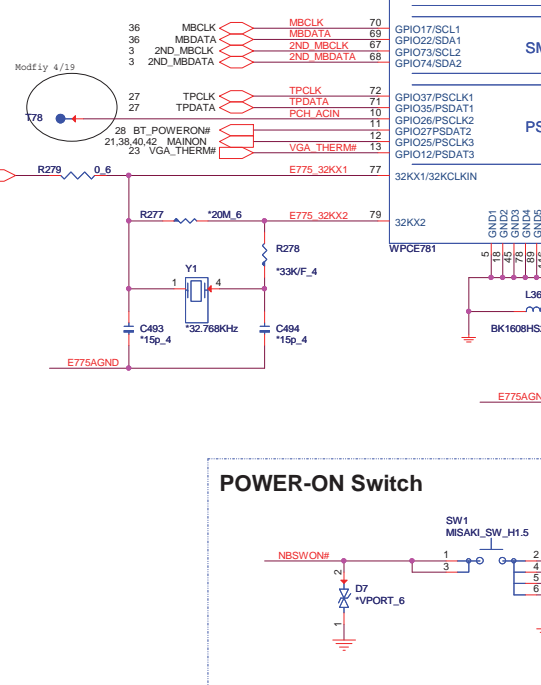
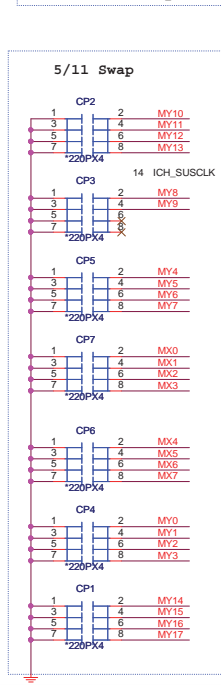
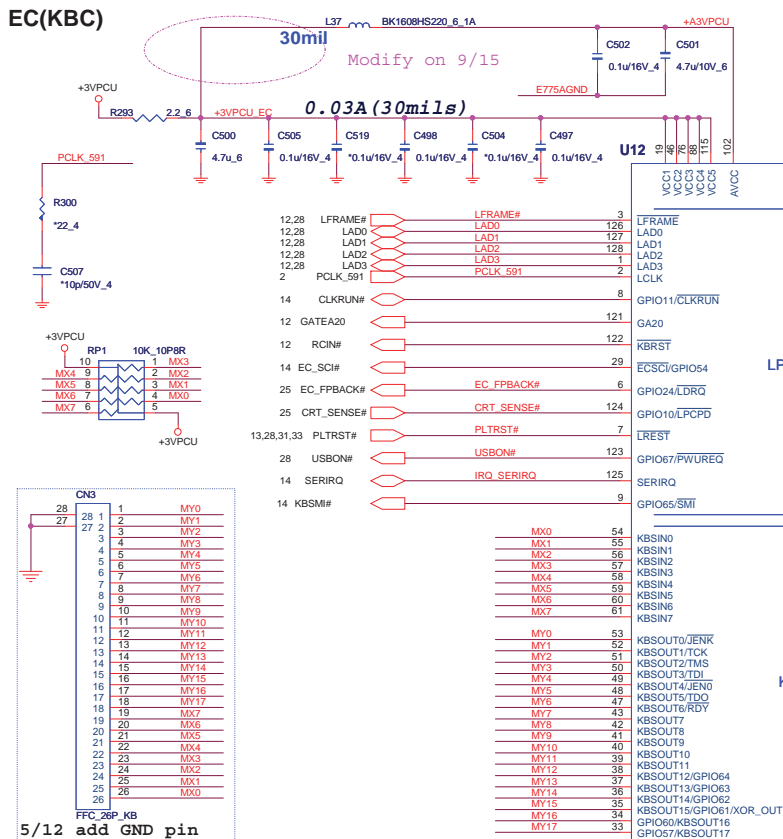
7/08 Add for ME.



7/08 Modify for ESD issue.

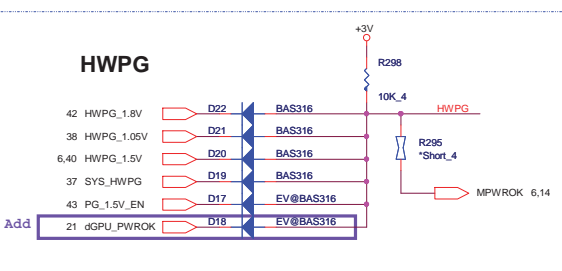
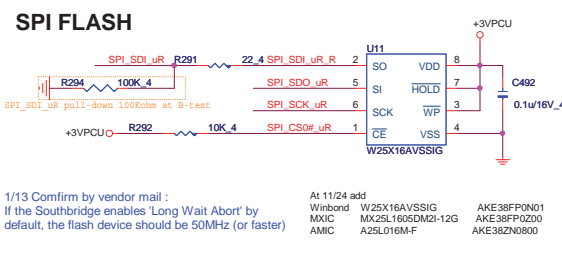
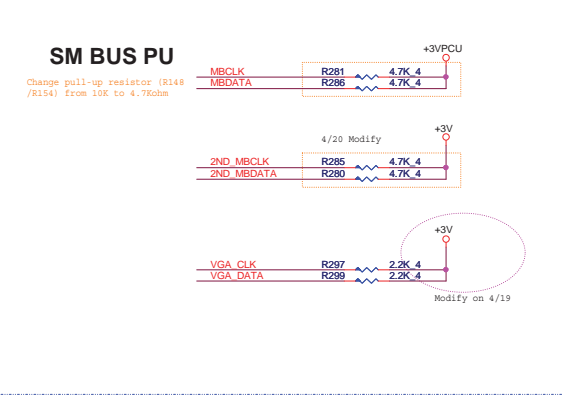
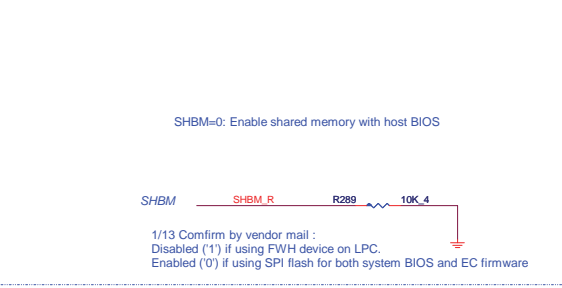


	<b>PROJECT : ZQ5</b> Quanta Computer Inc.		
	Size	Document Number	Rev
Date:	Monday, July 12, 2010	Sheet 34 of 43	Rev 1A



SM BUS ARRANGEMENT TABLE

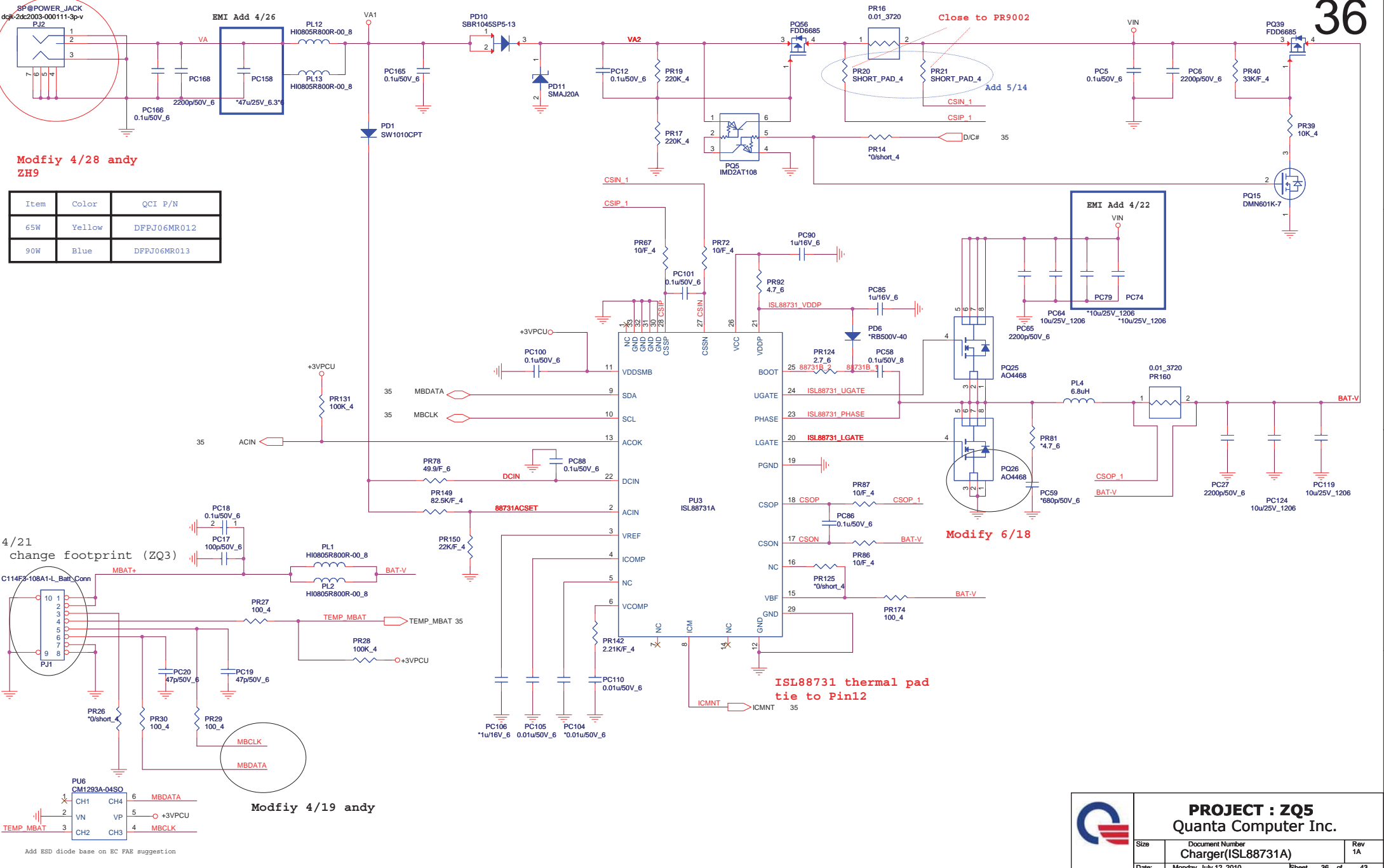
SM Bus	Function
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	



INTERNAL KEYBOARD STRIP SET

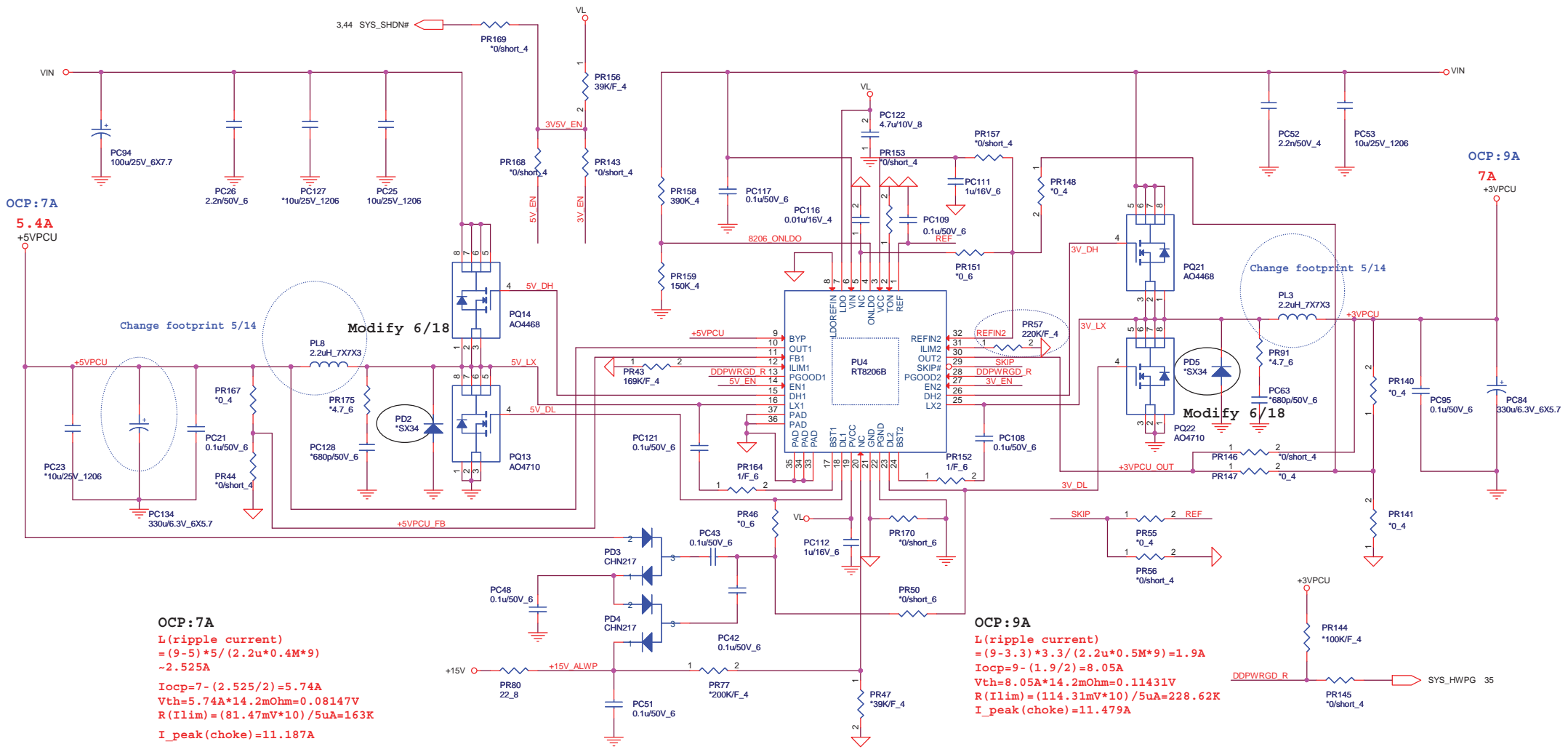
PROJECT : ZQ5  
Quanta Computer Inc.

Size: Document Number WPCE81 & FLASH  
Date: Monday, July 12, 2010  
Sheet 35 of 43



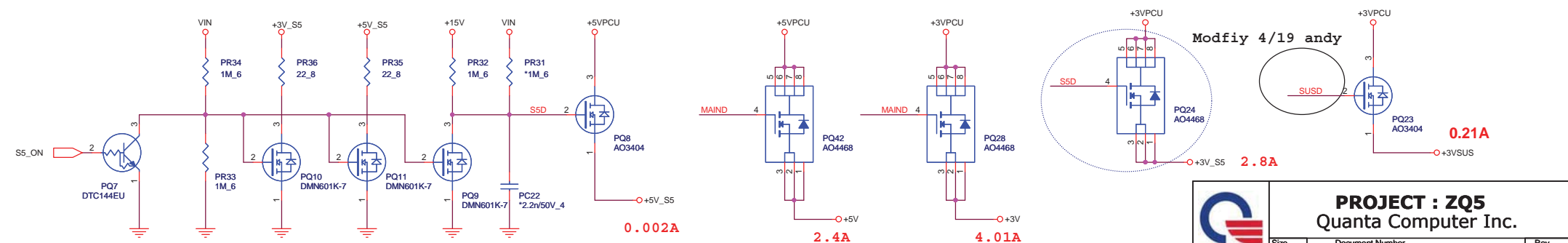
	<b>PROJECT : ZQ5</b>		Rev 1A
	Quanta Computer Inc.		
	Size	Document Number	
Date:	Monday, July 12, 2010	Sheet 36 of 43	

SUSD → SUSD 42  
 MAIND → MAIND 40,42



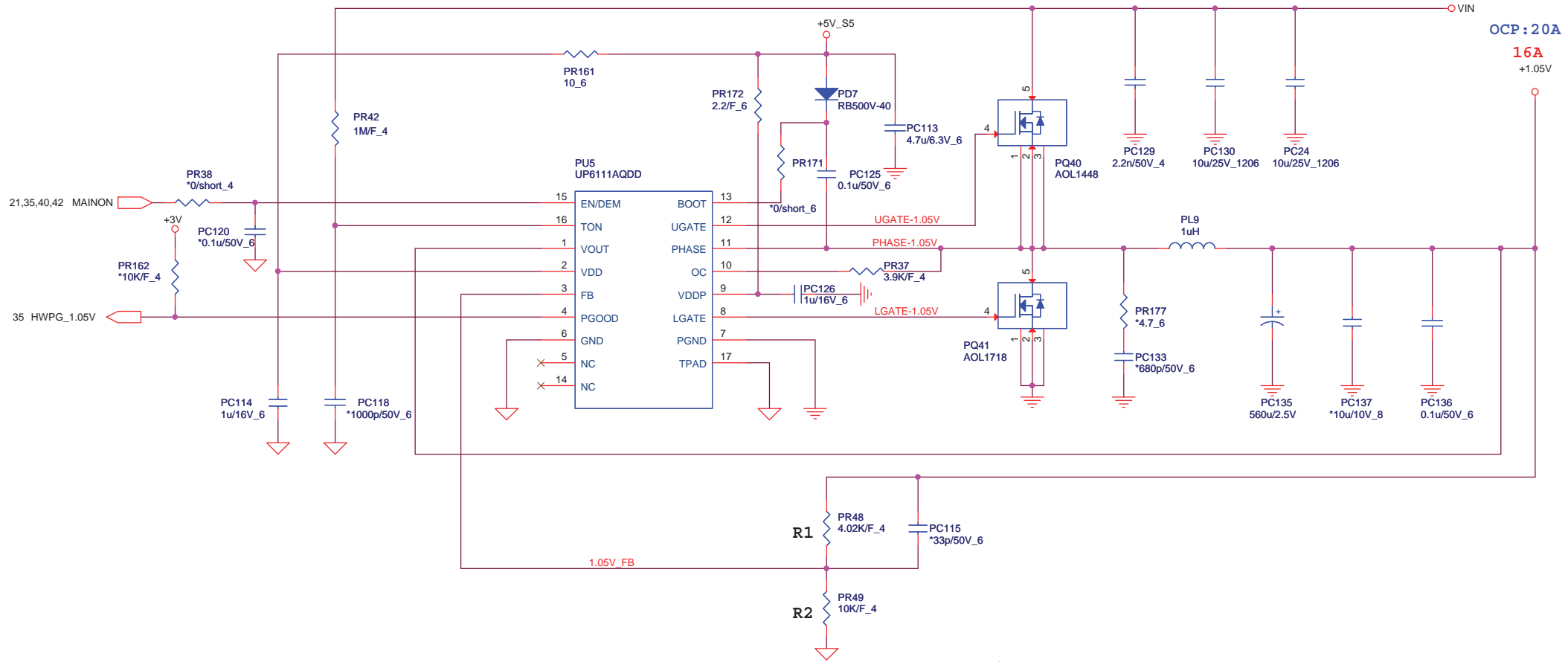
**OCP: 7A**  
 L(ripple current)  
 = (9-5) \* 5 / (2.2u \* 0.4M \* 9)  
 ~ 2.525A  
 Iocp = 7 - (2.525/2) = 5.74A  
 Vth = 5.74A \* 14.2mOhm = 0.08147V  
 R(ILim) = (81.47mV \* 10) / 5uA = 163K  
 I\_peak(choke) = 11.187A

**OCP: 9A**  
 L(ripple current)  
 = (9-3.3) \* 3.3 / (2.2u \* 0.5M \* 9) = 1.9A  
 Iocp = 9 - (1.9/2) = 8.05A  
 Vth = 8.05A \* 14.2mOhm = 0.11431V  
 R(ILim) = (114.31mV \* 10) / 5uA = 228.62K  
 I\_peak(choke) = 11.479A



	<b>PROJECT : ZQ5</b>	
	Quanta Computer Inc.	
Size	Document Number	Rev
	<b>SYSTEM 5V/3V (RT8206)</b>	1A
Date:	Monday, July 12, 2010	Sheet 37 of 43

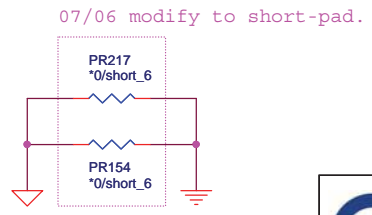
[PWM]




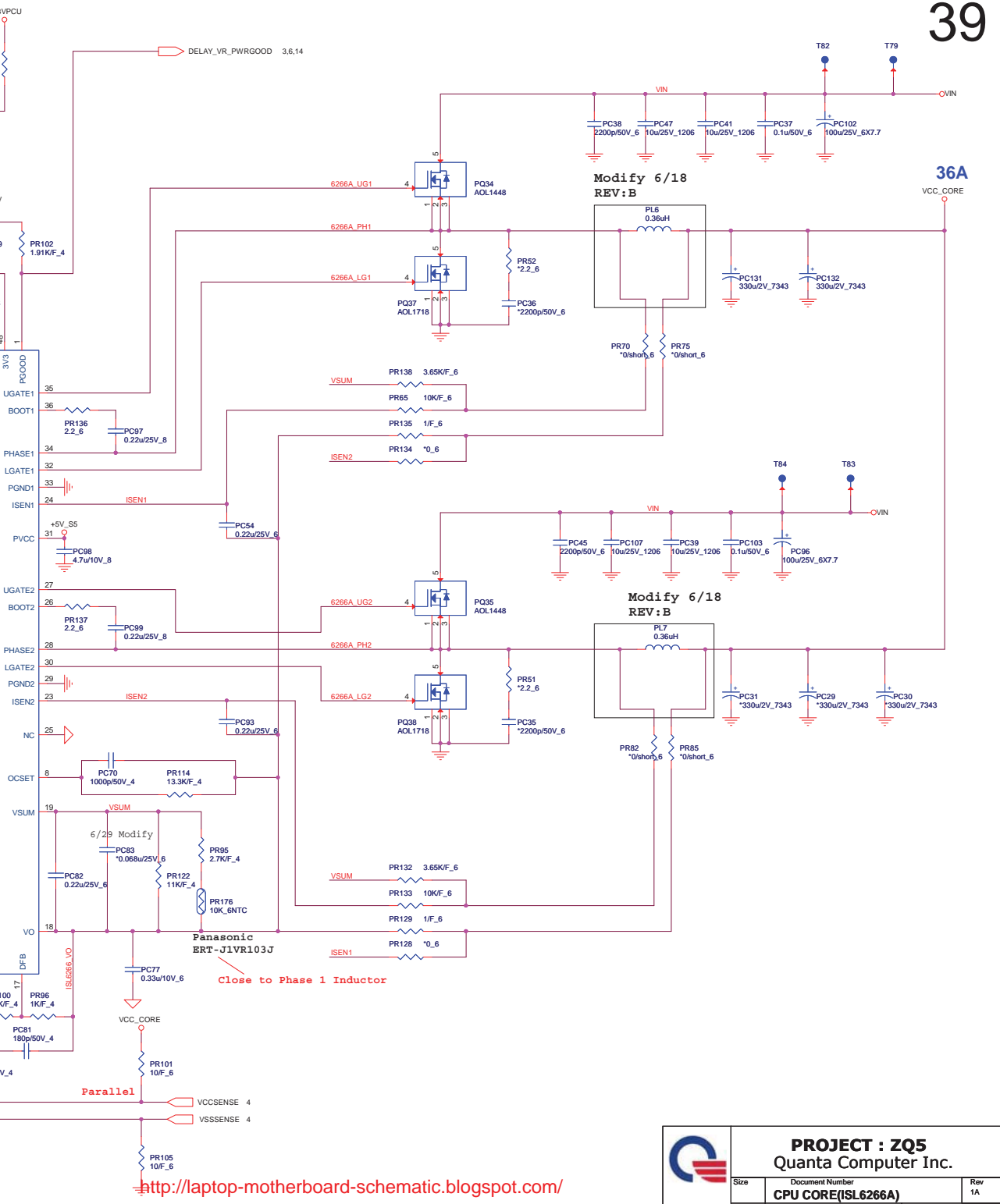
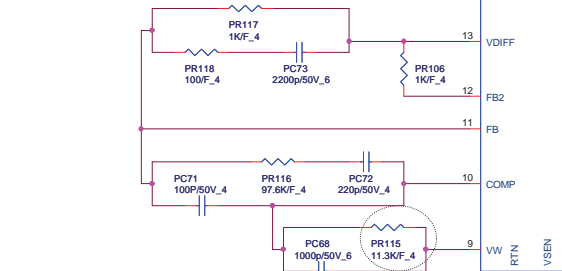
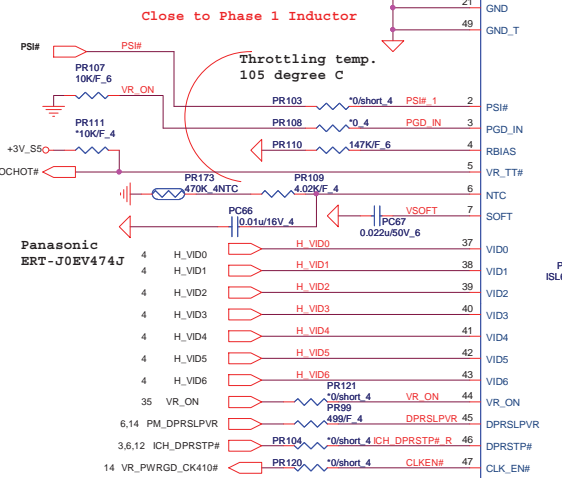
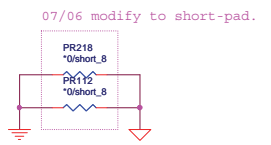
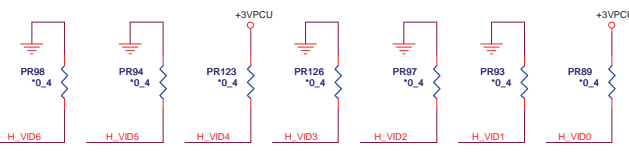
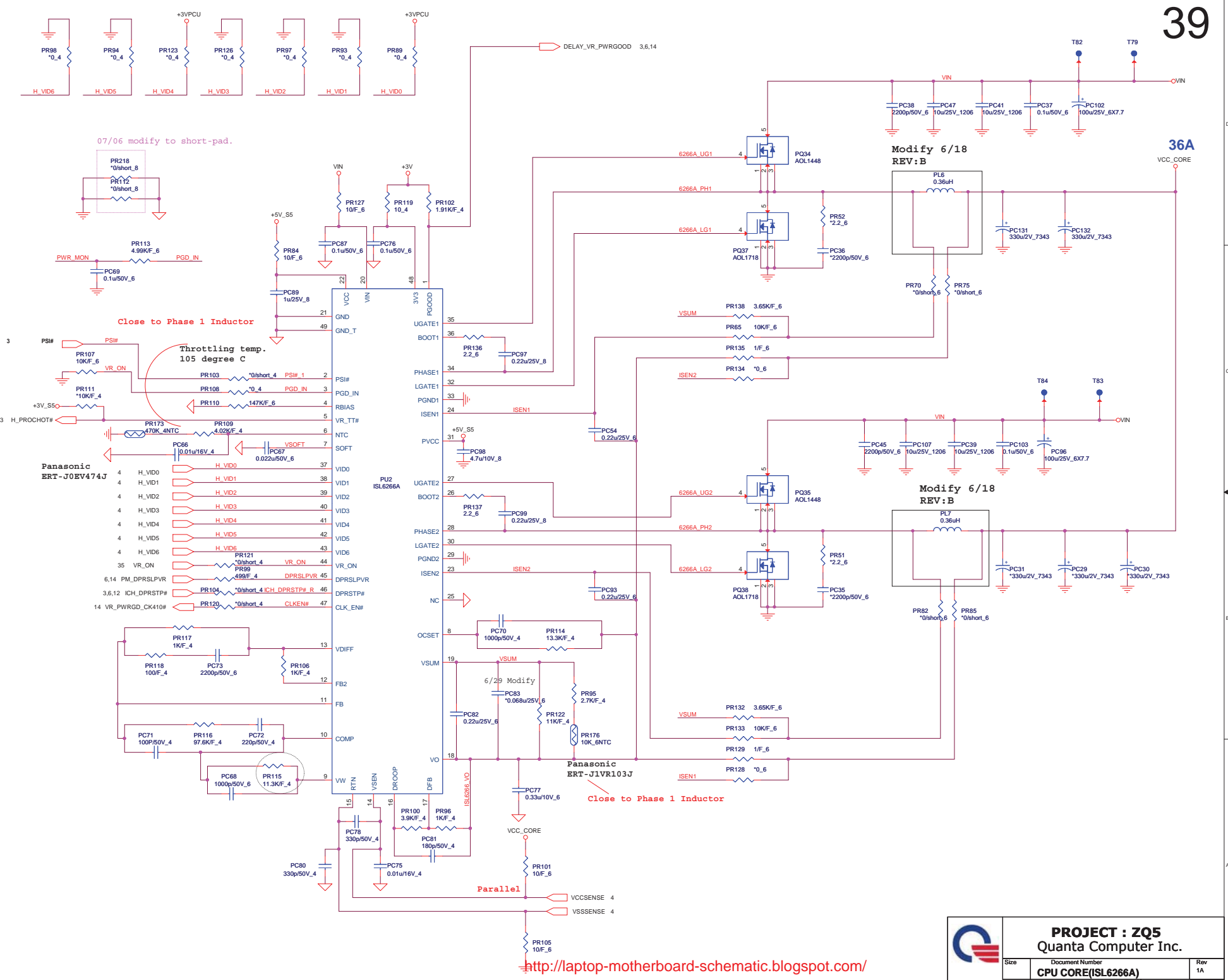
OCP: 20A  
16A  
+1.05V

$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$   
 $Frequency = Vout / (Vin \cdot TON)$   
 $TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$   
 $Frequency = 1 / (0.0036767) = 272K$

**L(ripple current)**  
 $= (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19)$   
 $\sim 3.647A$   
**RILIM = 4.3mohm \* 20 - 1.823 / 20uA = 3.907Kohm**  
**I(choke)peak = 23.647A**

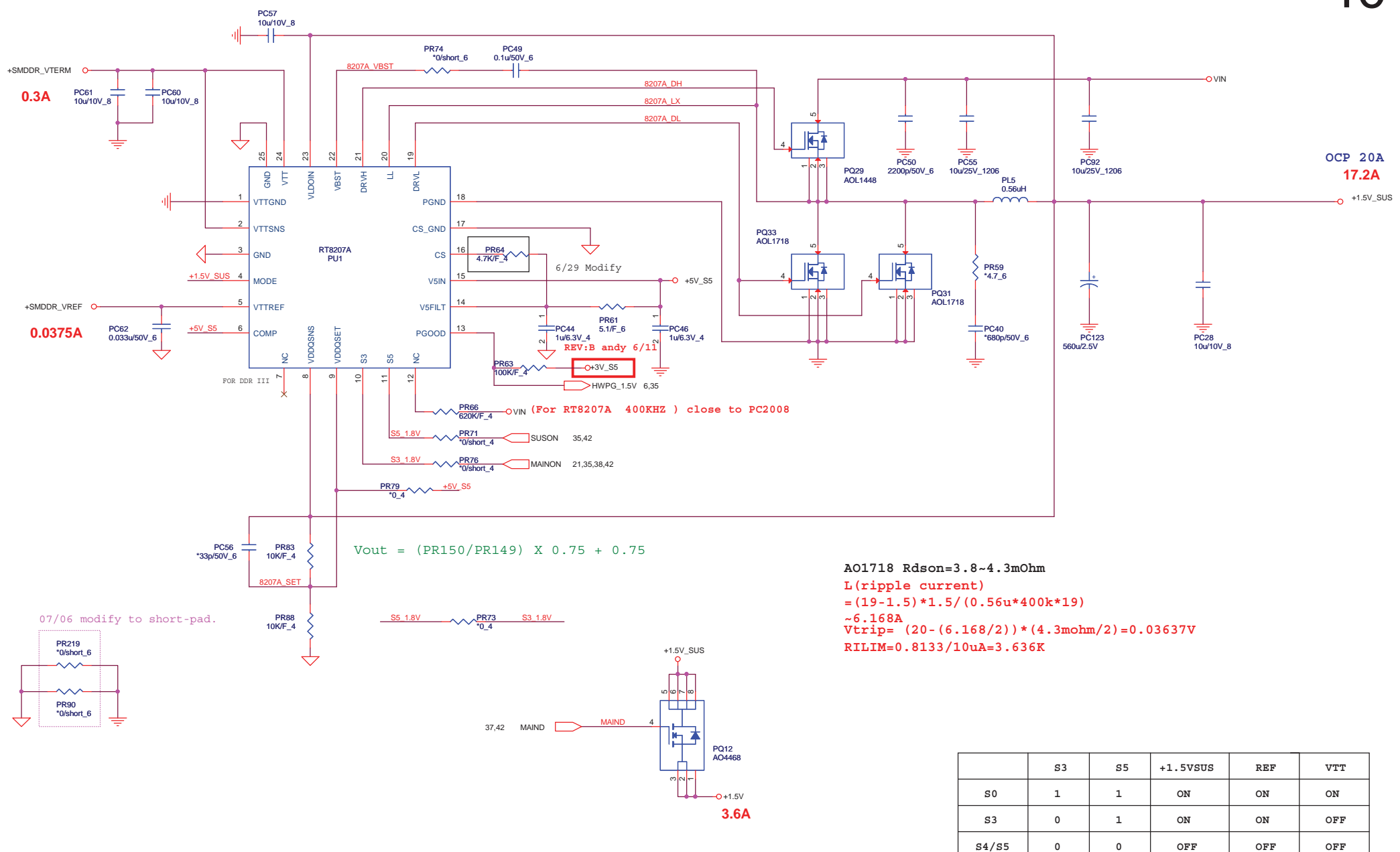


		
<b>PROJECT : ZQ5</b> <b>Quanta Computer Inc.</b>		
Size	Document Number	Rev
	<b>+1.05V (UP6111A)</b>	1A
Date:	Monday, July 12, 2010	Sheet 38 of 43



Size	Document Number	Rev
	<b>CPU CORE(ISL6266A)</b>	<b>1A</b>
Date:	Monday, July 12, 2010	Sheet 39 of 43

[PWM]



$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

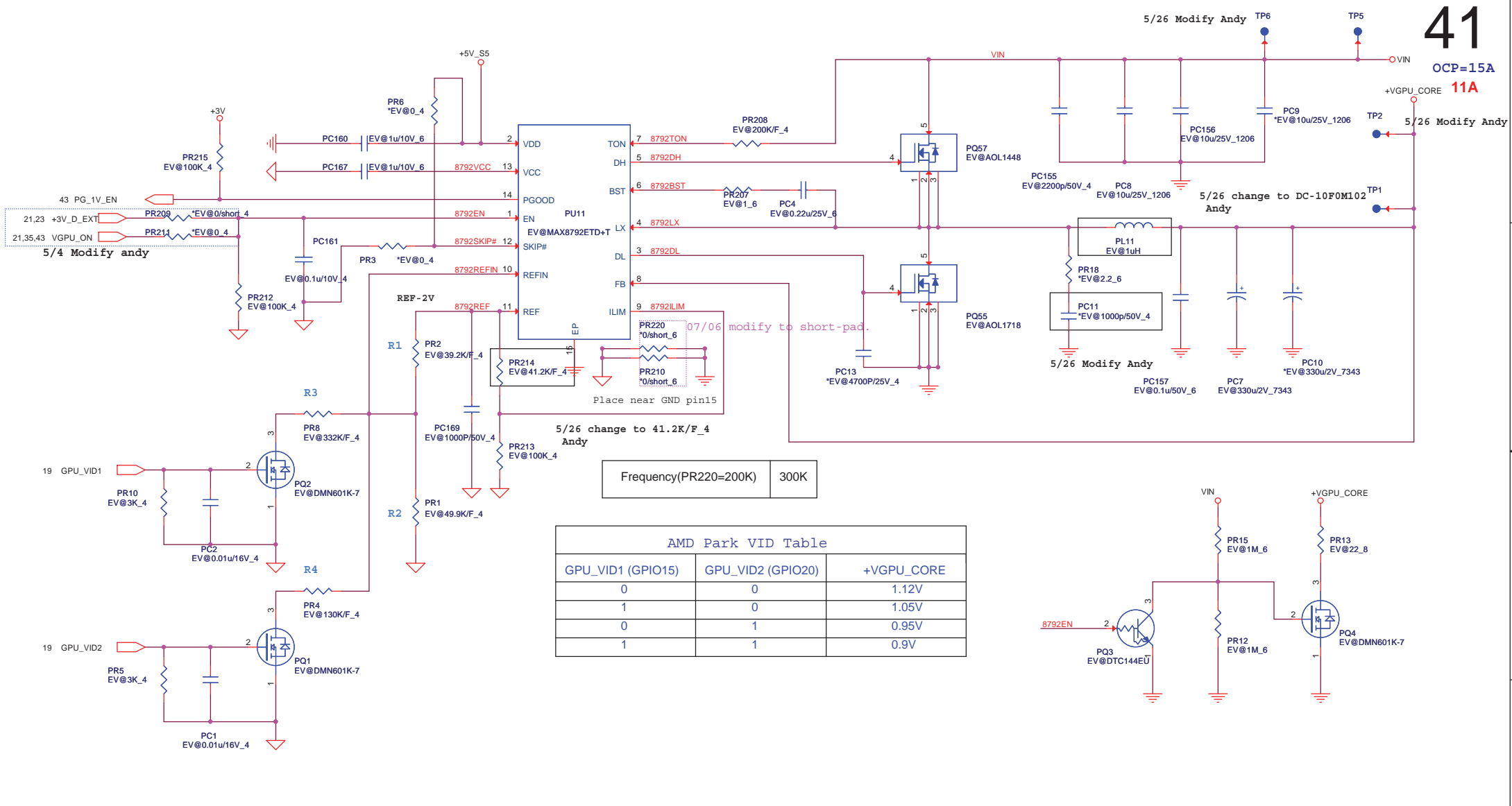
AO1718  $R_{dson} = 3.8 \sim 4.3m\Omega$   
 $L$  (ripple current)  
 $= (19 - 1.5) \times 1.5 / (0.56 \mu s \times 400k \times 19)$   
 $\sim 6.168A$   
 $V_{trip} = (20 - (6.168/2)) \times (4.3m\Omega/2) = 0.03637V$   
 $RILIM = 0.8133 / 10\mu A = 3.636K$

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

**PROJECT : ZQ5**  
 Quanta Computer Inc.

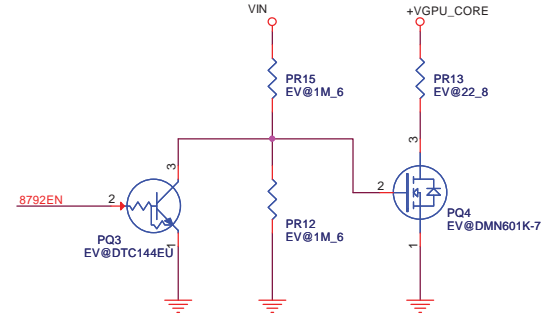
Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date:	Monday, July 12, 2010	Sheet 40 of 43





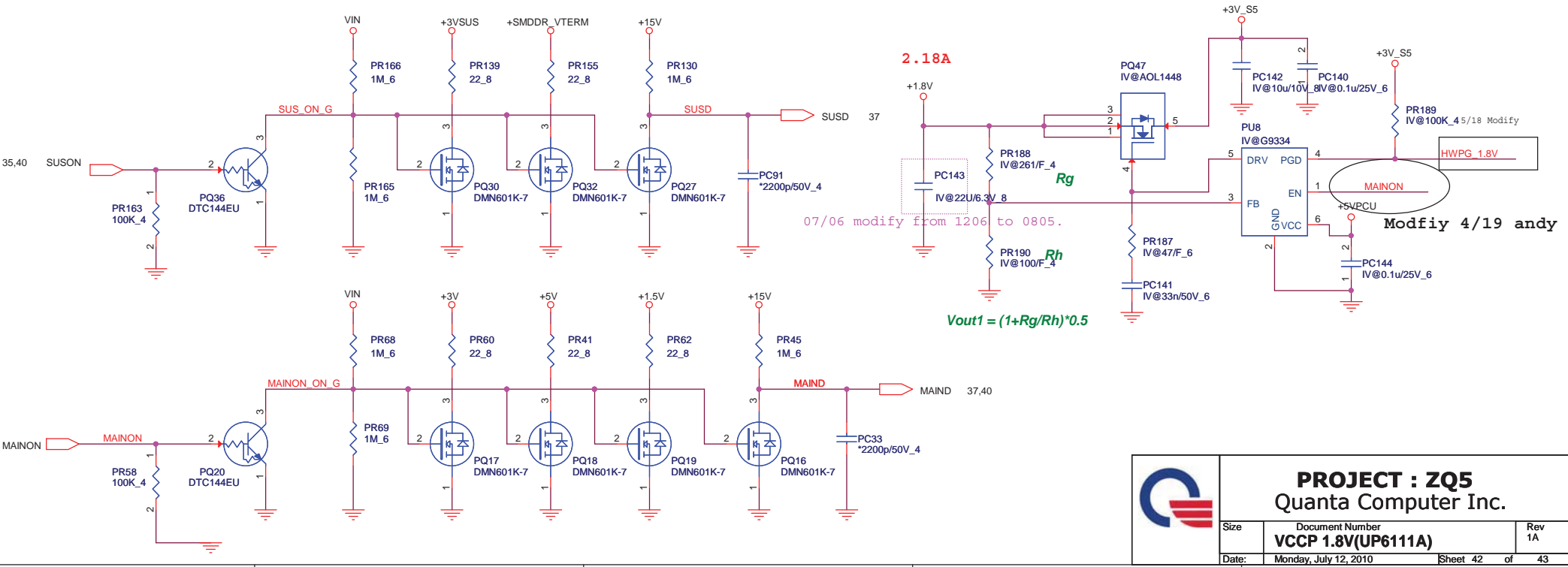
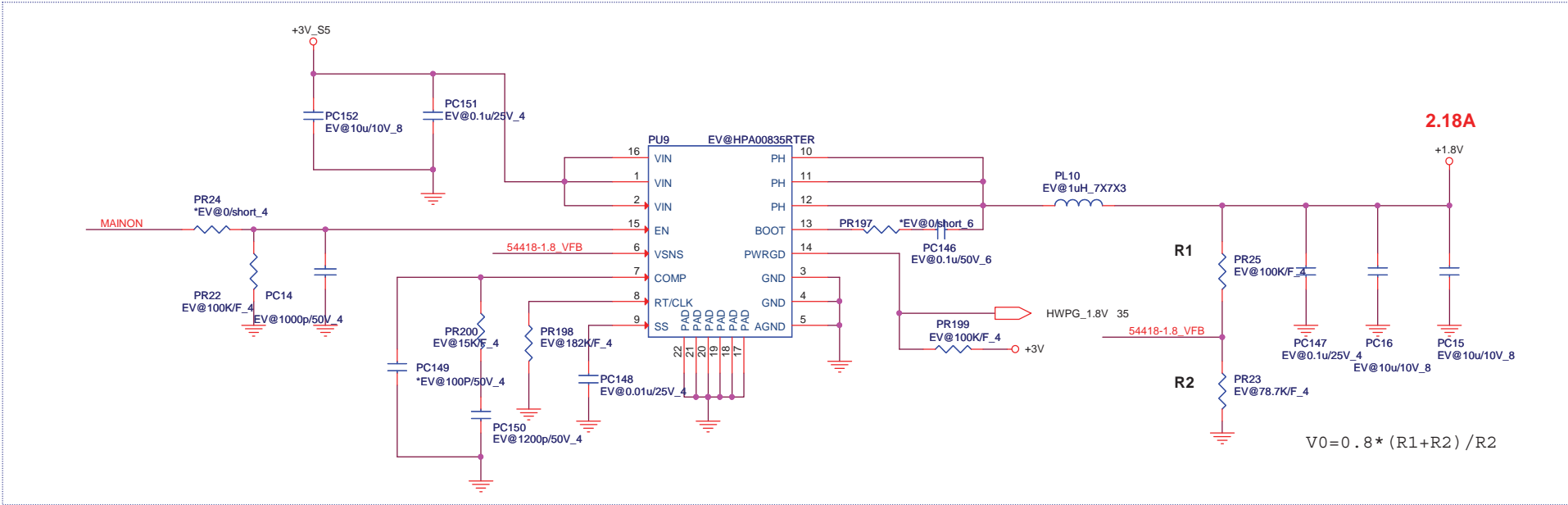
Frequency(PR220=200K) 300K


GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

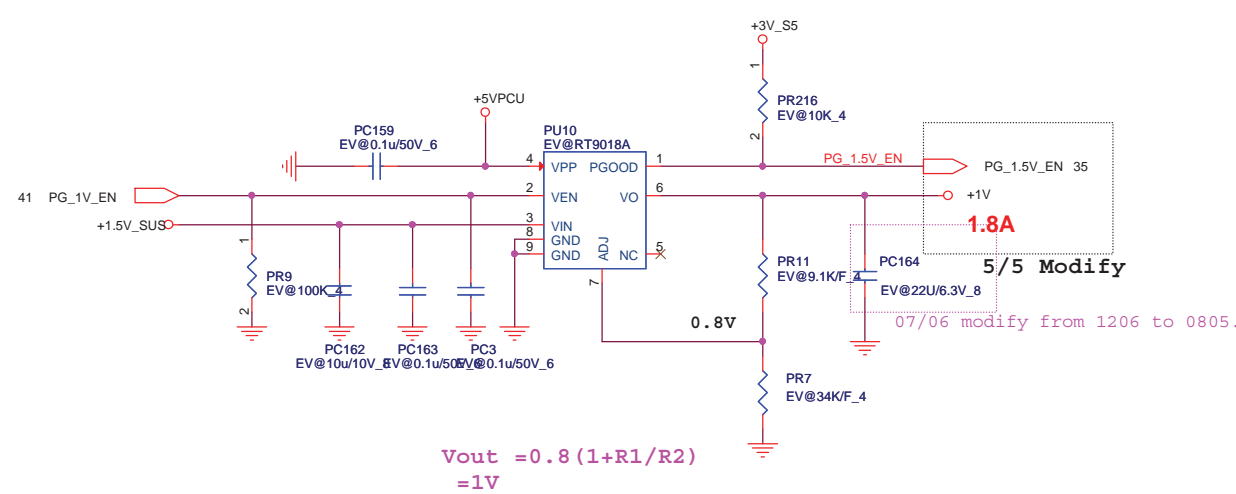
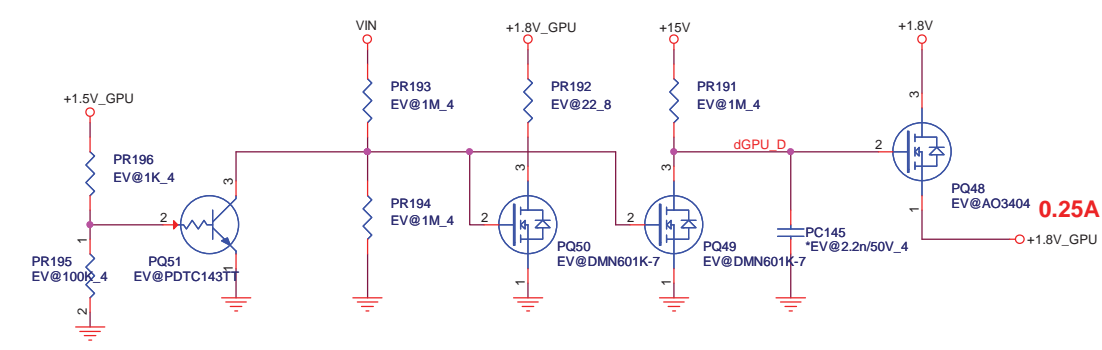
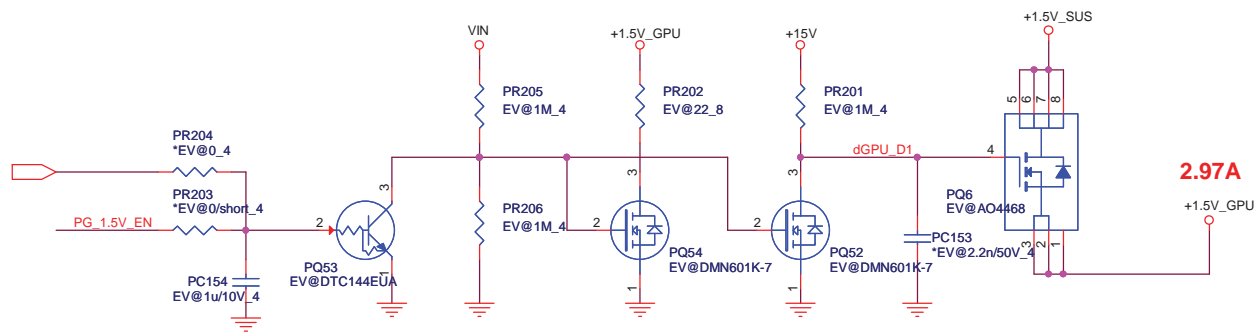



**PROJECT : ZQ5**  
Quanta Computer Inc.

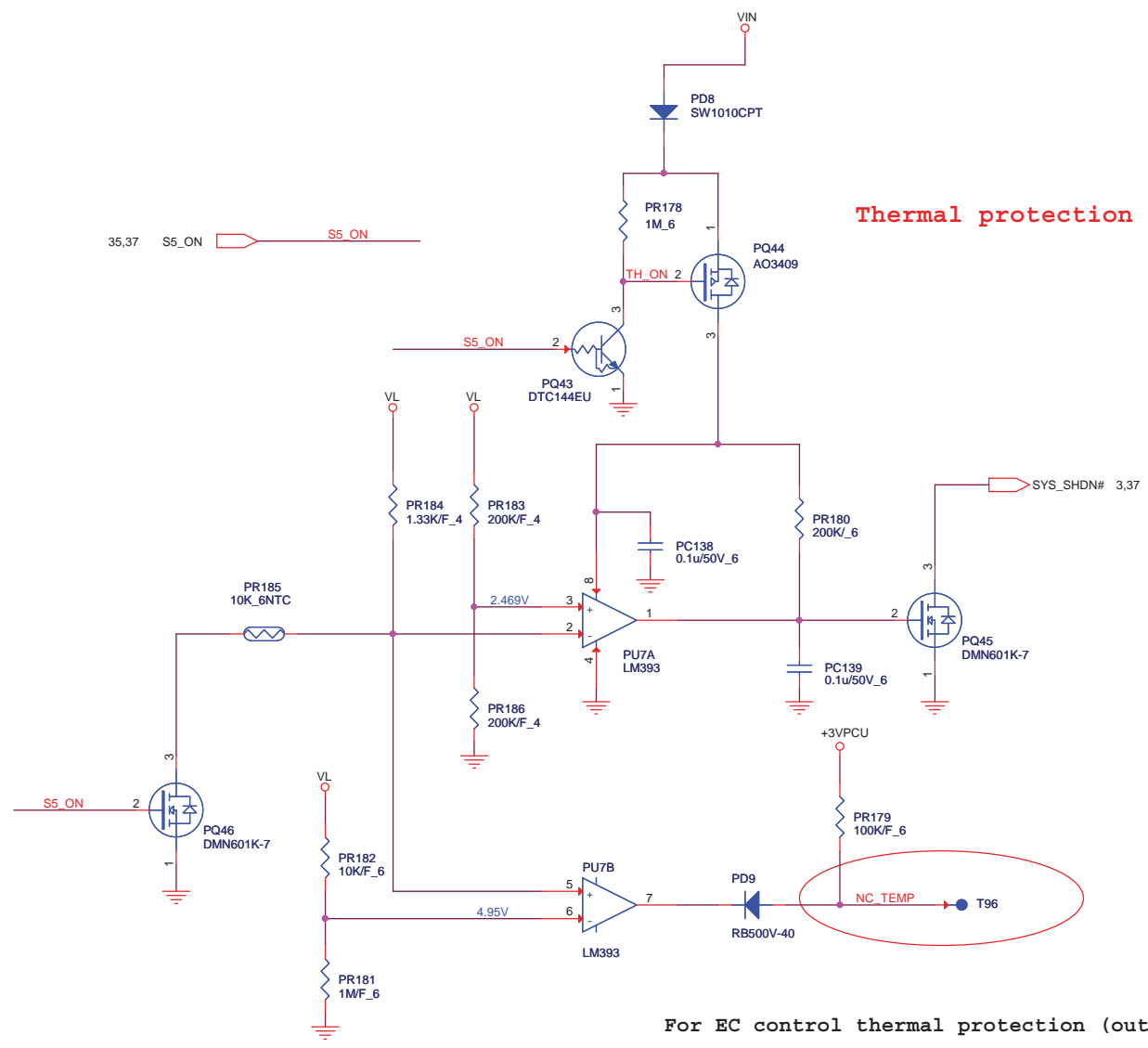
Size	Document Number <b>GPU CORE(MAX8792)</b>	Rev 1A
Date:	Monday, July 12, 2010	Sheet 41 of 43



			<b>PROJECT : ZQ5</b>	
			Quanta Computer Inc.	
Size	Document Number		Rev	
	<b>VCCP 1.8V(UP6111A)</b>		1A	
Date:	Monday, July 12, 2010	Sheet 42	of 43	




 <b>PROJECT : ZQ5</b> Quanta Computer Inc.			
			Size
		<b>GPU_POWER</b>	1A
Date:	Monday, July 12, 2010	Sheet 43	of 43



Thermal protection

For EC control thermal protection (output 3.3V)

	<b>PROJECT : ZQ5</b>	
	Quanta Computer Inc.	
Size	Document Number	Rev
	<b>Thermal Protection</b>	1A
Date:	Monday, July 12, 2010	Sheet 44 of 43

CHANGE LIST

PAGE	MODEL	
	FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	

A First release

ZQ5 MB

1. Page40: change HWPg 1.5V pull up to +3V\_S5 for S3 issue
2. Page29: Add R570 pull up +1.5V for uma Audio I/O
3. Page26: Swap HDMI Lane2 for HDMI issue
4. Page31: U34 and R567 no stuff ,R555 stuff it for LAN ID issue
5. Page02: Q12 and Q13 change Part number from BAM700200F6 to BAM700200H2
6. Page29: R55 and R56 change Part number to CS33303F911(33K) for Audio
7. Page29: change R86 and U6 Pin5 pull up to +5V\_S5
8. Page29: change R84 value to 0 ohm
9. Page30: change Q25 and Q27 Part number to BAM70020002 as ZYB
10. Page25: L1,L2,L3 change to CX8LL680001
11. Page25: C1,C2,C3,C5,C6,C7 change to CH-5006JBD4
12. Page25: R11,R14 change to CS01502JB12
13. Page28: Add another BT circuit (USB port5), Add Q30,RN37,C792,CN22
14. Page07: Change R425,R426 to CS02492FB29 for CRT issue
15. Page13: Change BT 2.1 to USB port 7
16. Page28: Change BT 2.1 to USB port 7
17. Page25: change 0805 to SHORT Pad R71,R72,R98,R146
18. Page29: Stuff R84 U6 and no stuff R86 for Audio bobo noise
19. Page10: change R171 and R429 to bead CX8PG181001
20. Page30: stuff Q25 and Q27 and no stuff R46 R48 for Audio bobo noise
21. Page40: Add PR219
22. Page38: Add PR217
23. Page41: Add PR220
24. Page39: Add PR218
25. Page36: Change PR16 (0.01/F\_7520) to CS+0108GL13 (0.01\_3720)
26. Page41: DEL JP1 and JP4
27. Page39: DEL JP2 and JP3
28. Page38: change PR171,PR38 to short Pad
29. Page36: change PR125,PR14,PR26 to short Pad
30. Page37: change PR143,PR145,PR146,PR153,PR157,PR168,PR169,PR170,PR50,PR44,PR56 to short Pad
31. Page39: change PR120,PR121,PR104,PR103,PR70,PR75,PR82,PR85 to short Pad
32. Page40: change PR71,PR76,PR74 to short Pad
33. Page41: change PR209 to short Pad (EV@)
34. Page42: change PR24,PR197 to short Pad (EV@)
35. Page43: change PR203 to short Pad (EV@)
36. Page36: Change PQ26 to AO4468 (P/N: BAM44680003)
37. Page37: PD2 and PD5 no stuff
38. Page39: PC29 and PC31 no stuff
39. Page36: PJ1 change Part number to DFHD08MR140

C

01. Page39: PC83 no stuff
02. Page39: Change PR64 to CS24702FB10
03. Page16: Del C539 (\*10U/6.3V\_6).
04. Page17: Del C538 (\*10U/6.3V\_6).
05. Page38: Change AGND (0 ohm) to Short Pad(0603): PR154、PR217.
06. Page40: Change AGND (0 ohm) to Short Pad(0603): PR219、PR90.
07. Page41: Change AGND (0 ohm) to Short Pad(0603): PR210、PR220.
08. Page39: Change AGND (0 ohm) to Short Pad(0805): PR112,PR218.
09. Page43: Change PC164 (22uF/10V\_1206) to CH6221M9A07 (22uF/6.3V\_0805)
10. Page42: Change PC143 (22uF/10V\_1206) to CH6221M9A07 (22uF/6.3V\_0805)
11. Page34: Modify HOLE18 to dummy net.
12. Page34: Add HOLE22 for ME.

D

