

# Compal Confidential

## NBLG0 Schematics Document

AMD Tigris (JV40-TR) : Caspian Processor with RS880M/SB710/M92-M2 XT

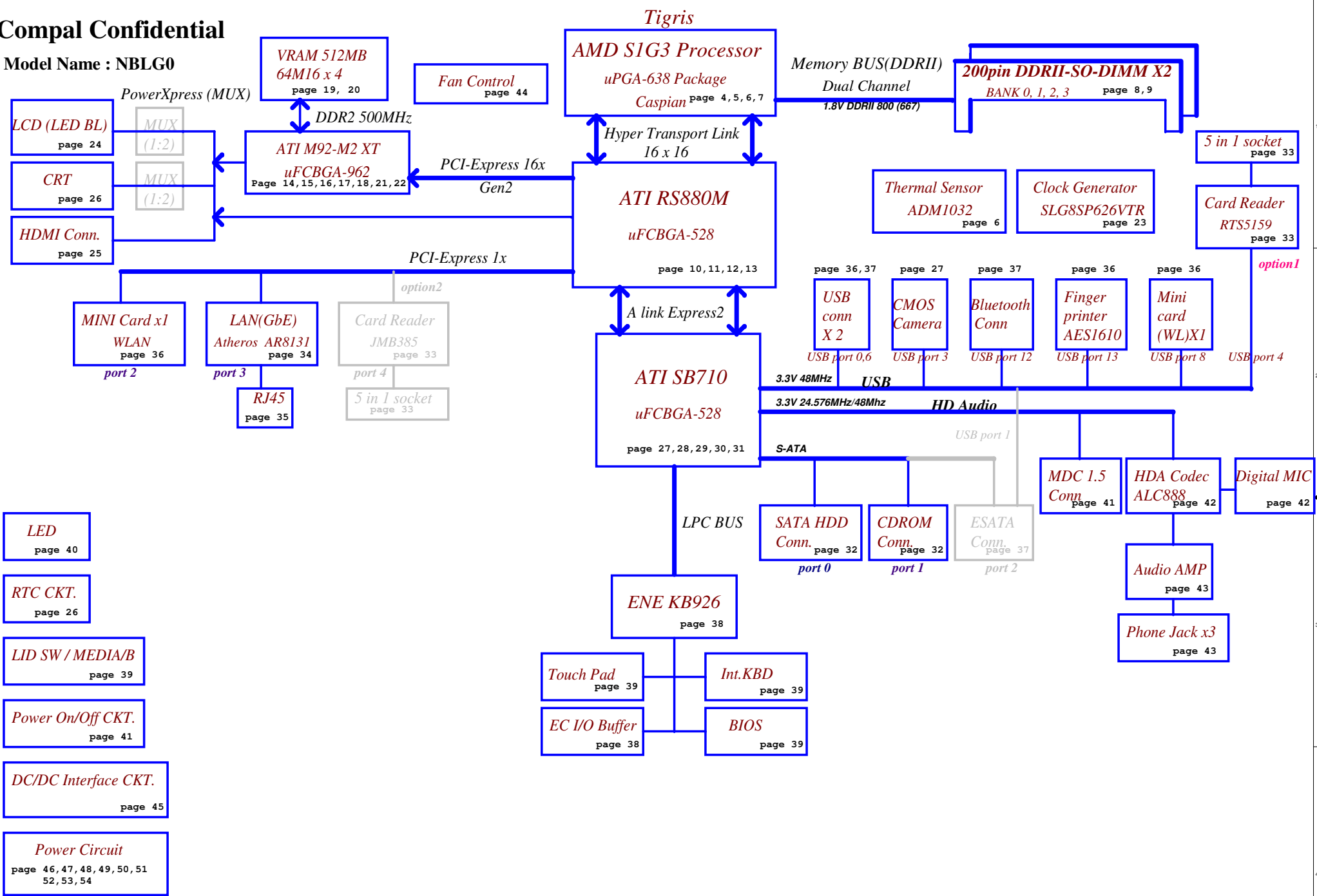
2009-06-04

REV: 0.2

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Model Name : NBLG0



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Smart Battery	0001 011X b	16H	98H
ADI ADM1032 (CPU)	1001 100X b		9AH
GMT G781-1 (GPU)	1001 101X b		9CH
SB-Temp Sensor			

## EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

## SB700

### SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8P626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

## SB700

### SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	
1	0.1(DVT)
2	0.2(PVT)
3	1.0(MP)
4	
5	
6	
7	

## BTO Option Table

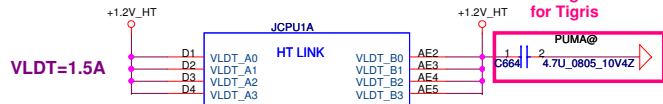
BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

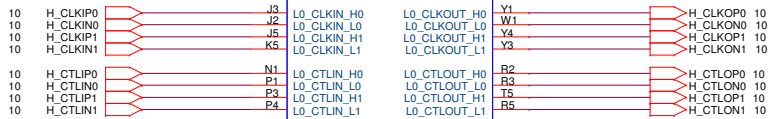
KB926						
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

KB926	
	PX_GPIO1_SB
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)
IGP only mode	X
PowerXpress mode	H : Enable

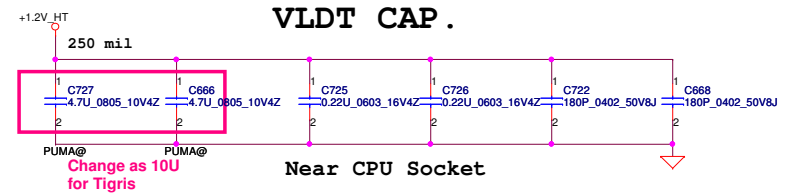
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H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	L1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	E5	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	Y4	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15



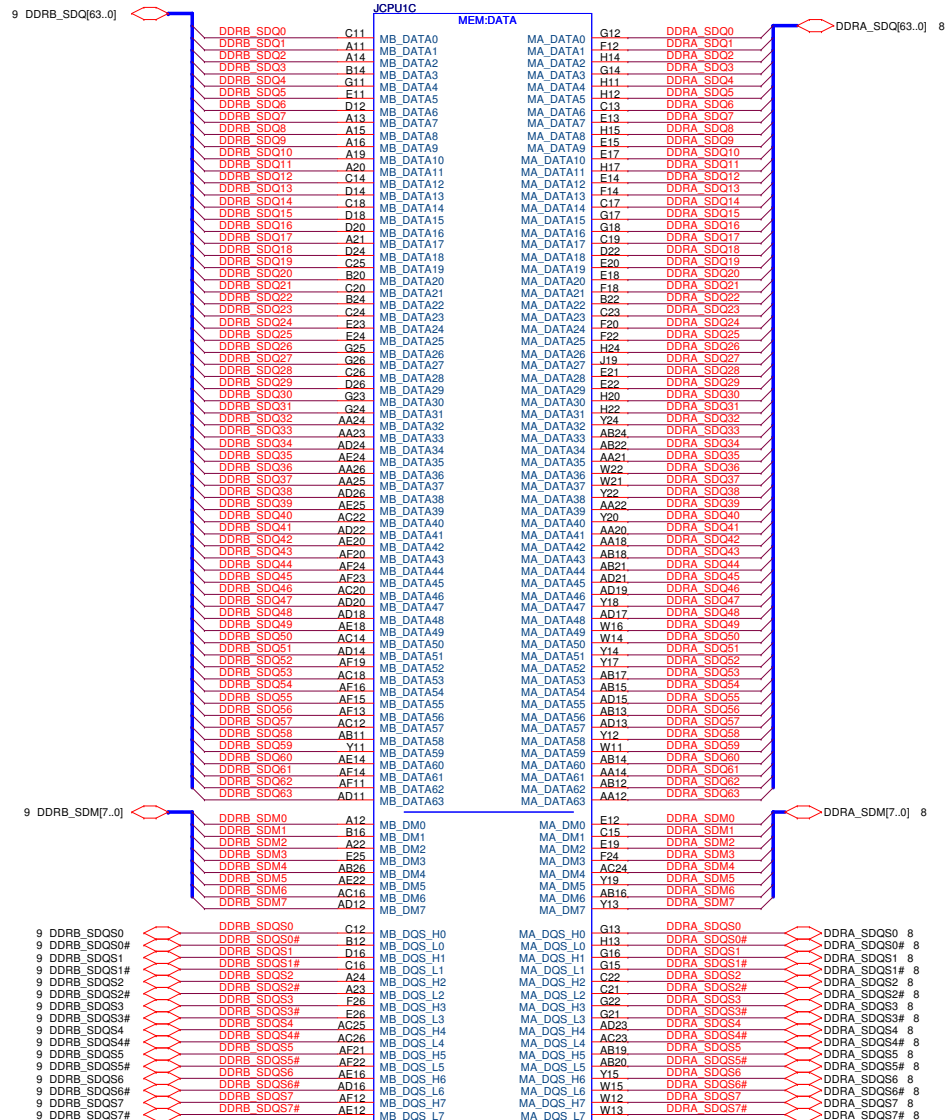
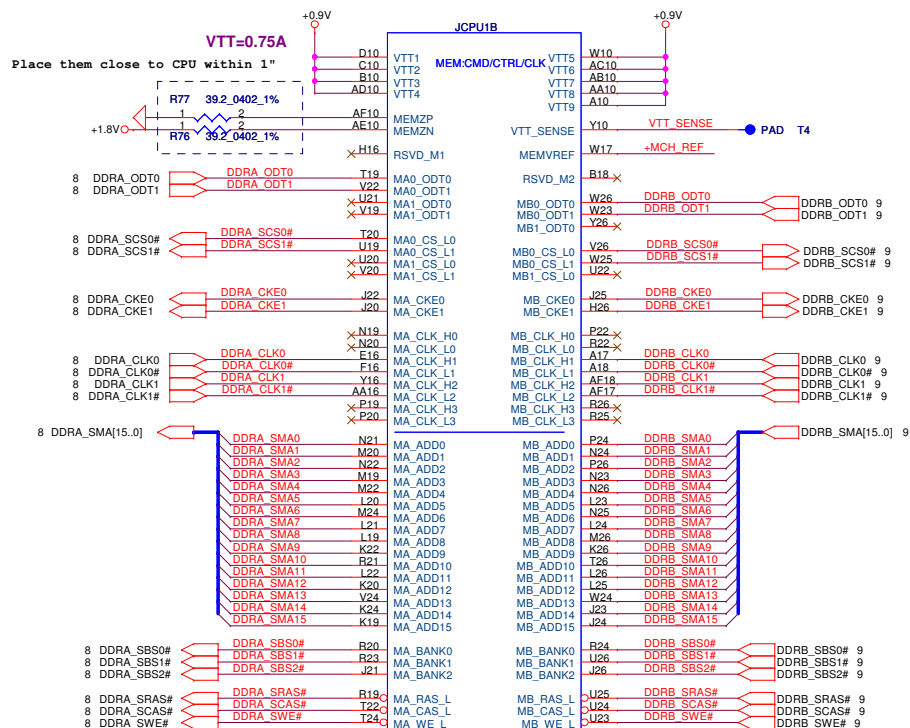
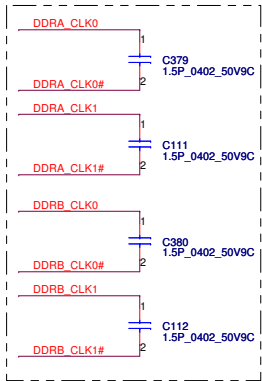
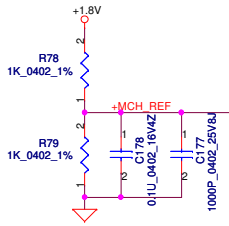
6090022100G\_B conn@



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# Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH

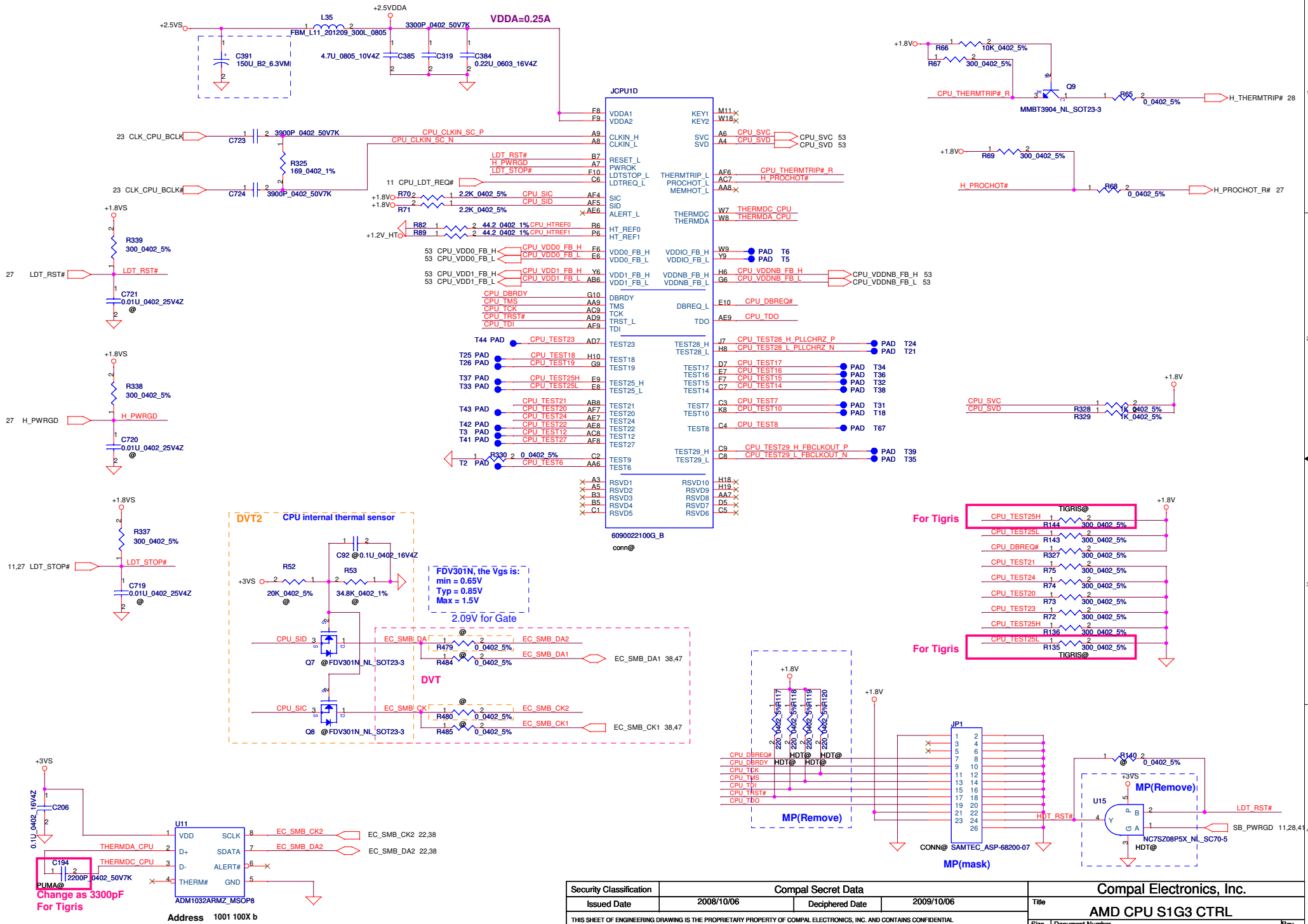


6090022100G\_B  
conn@

6090022100G\_B  
conn@

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Title			
AMD CPU S1G3 DDR2 I/F			
AMD CPU S1G3 DDR2 I/F			
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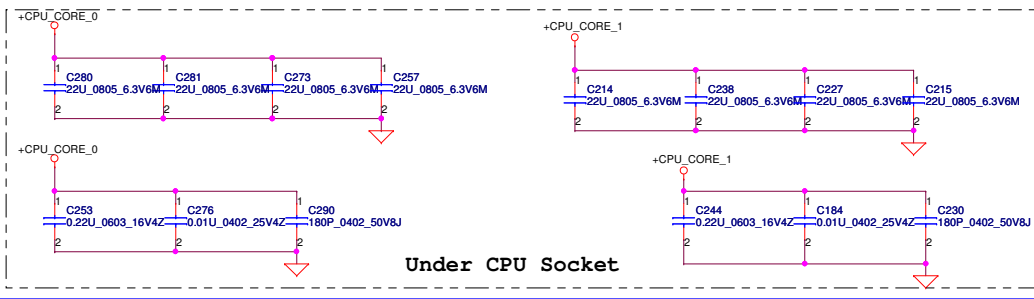
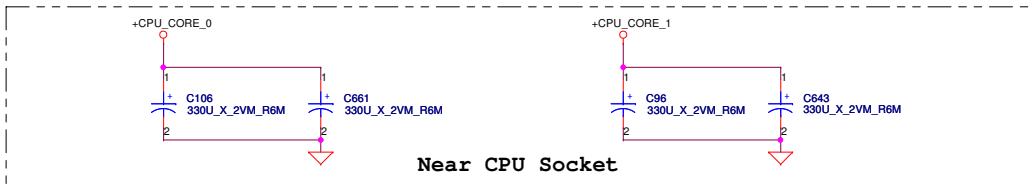


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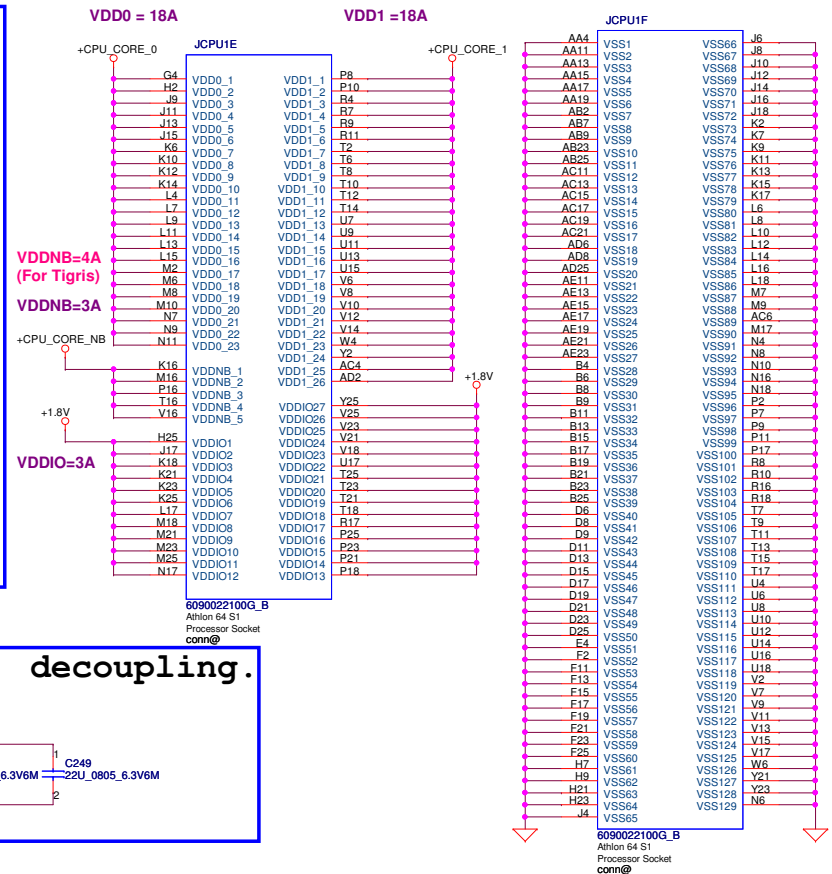
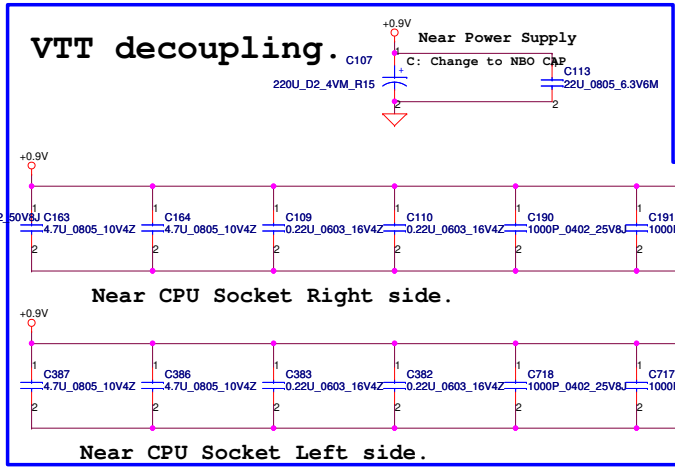
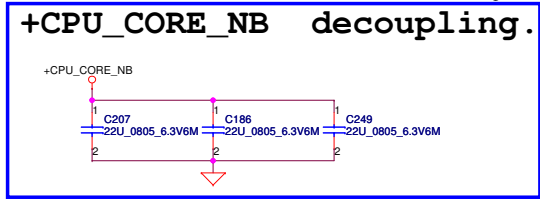
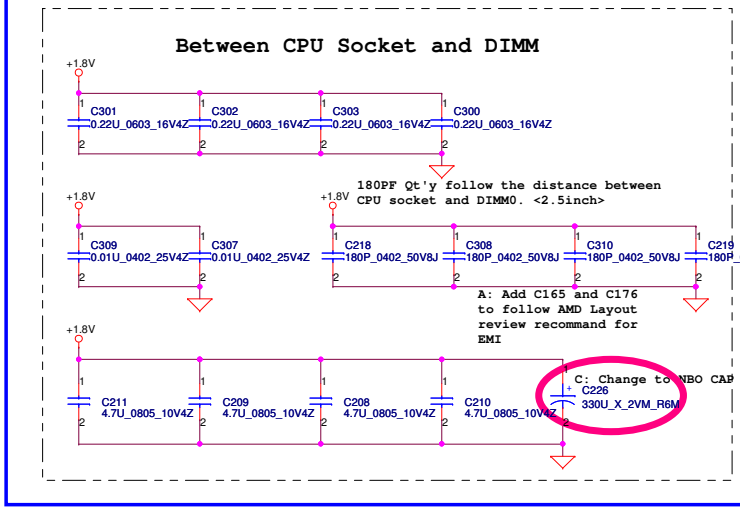
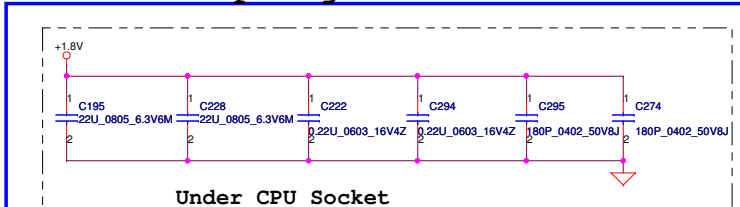
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AMD CPU S1G3 CTRL		
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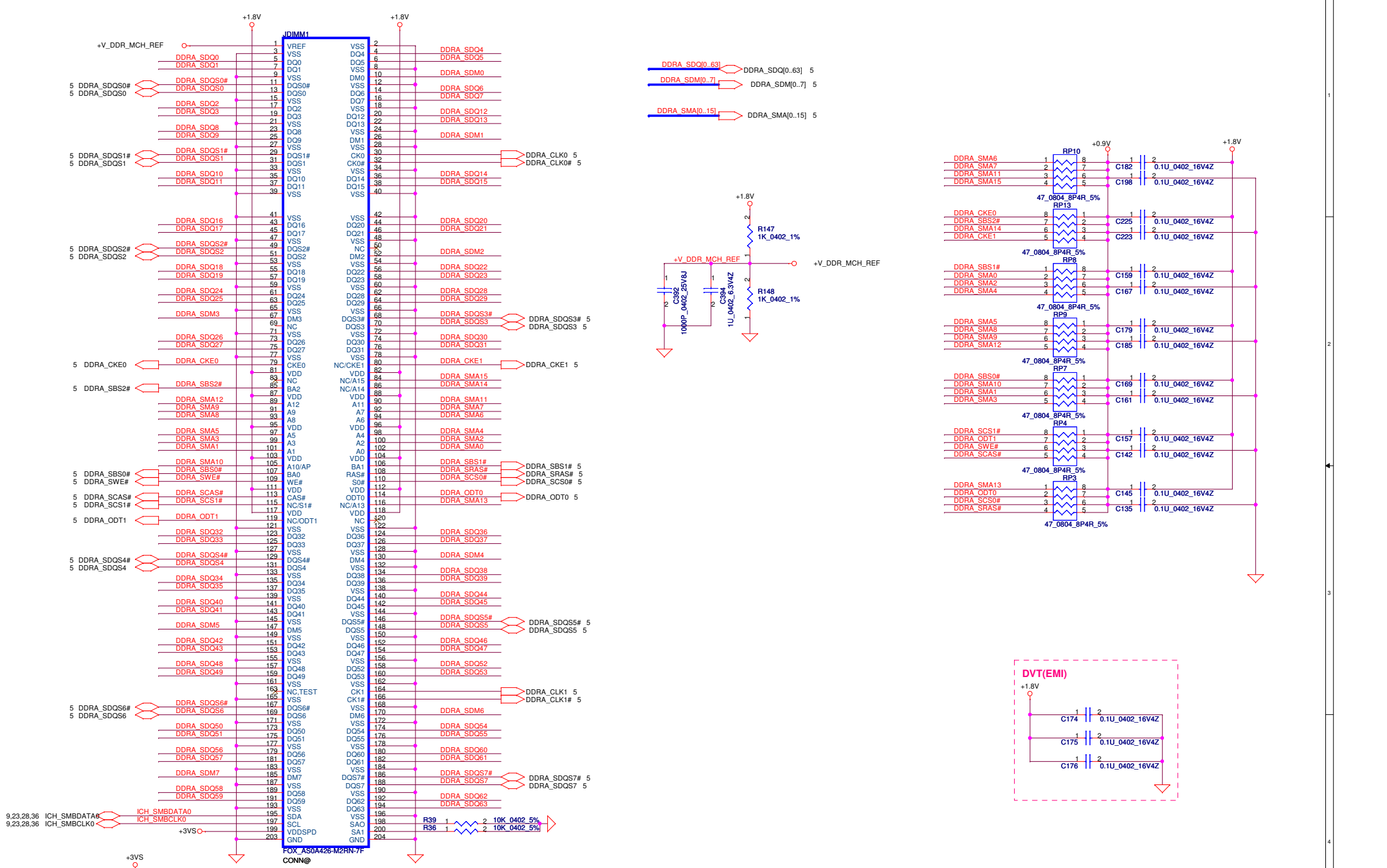
# VDD (+CPU\_CORE) decoupling.



# VDDIO decoupling.



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				AMD CPU S1G3 PWR & GND		
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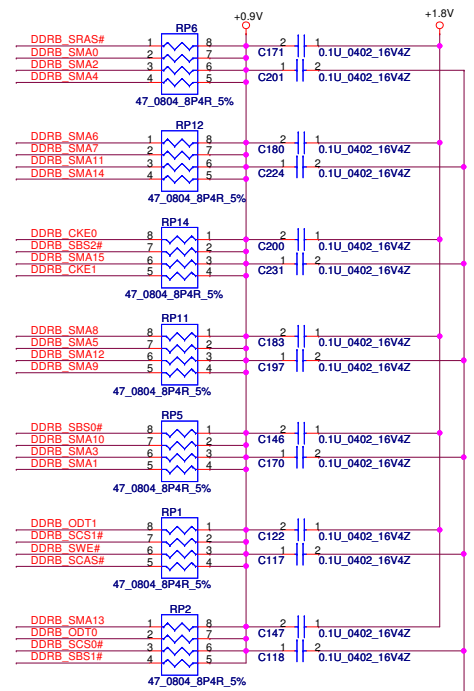
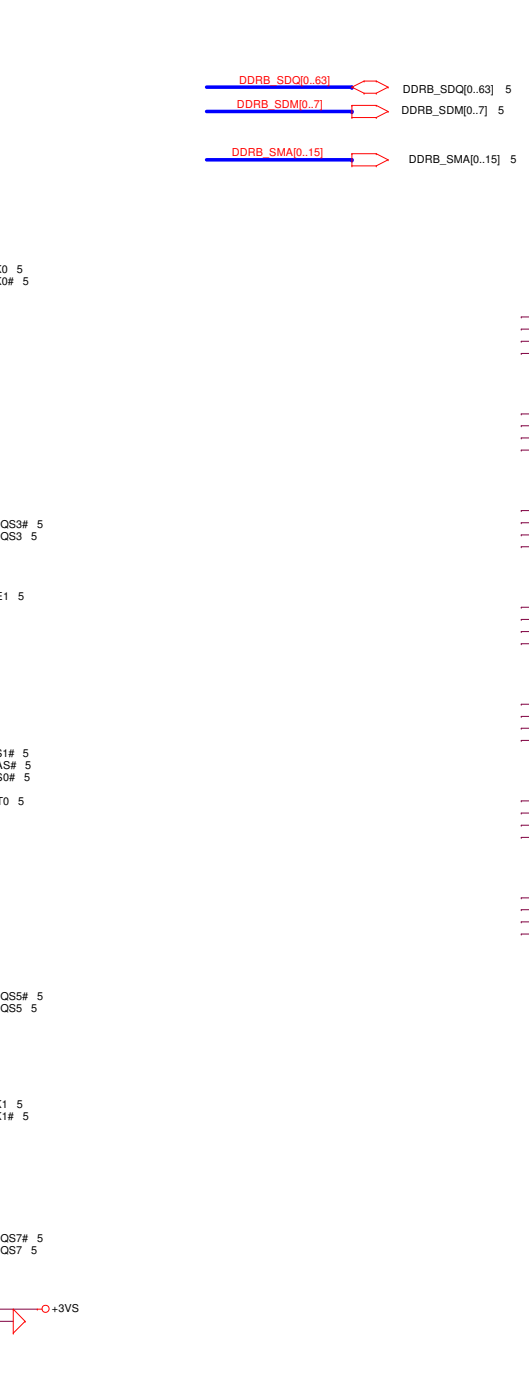
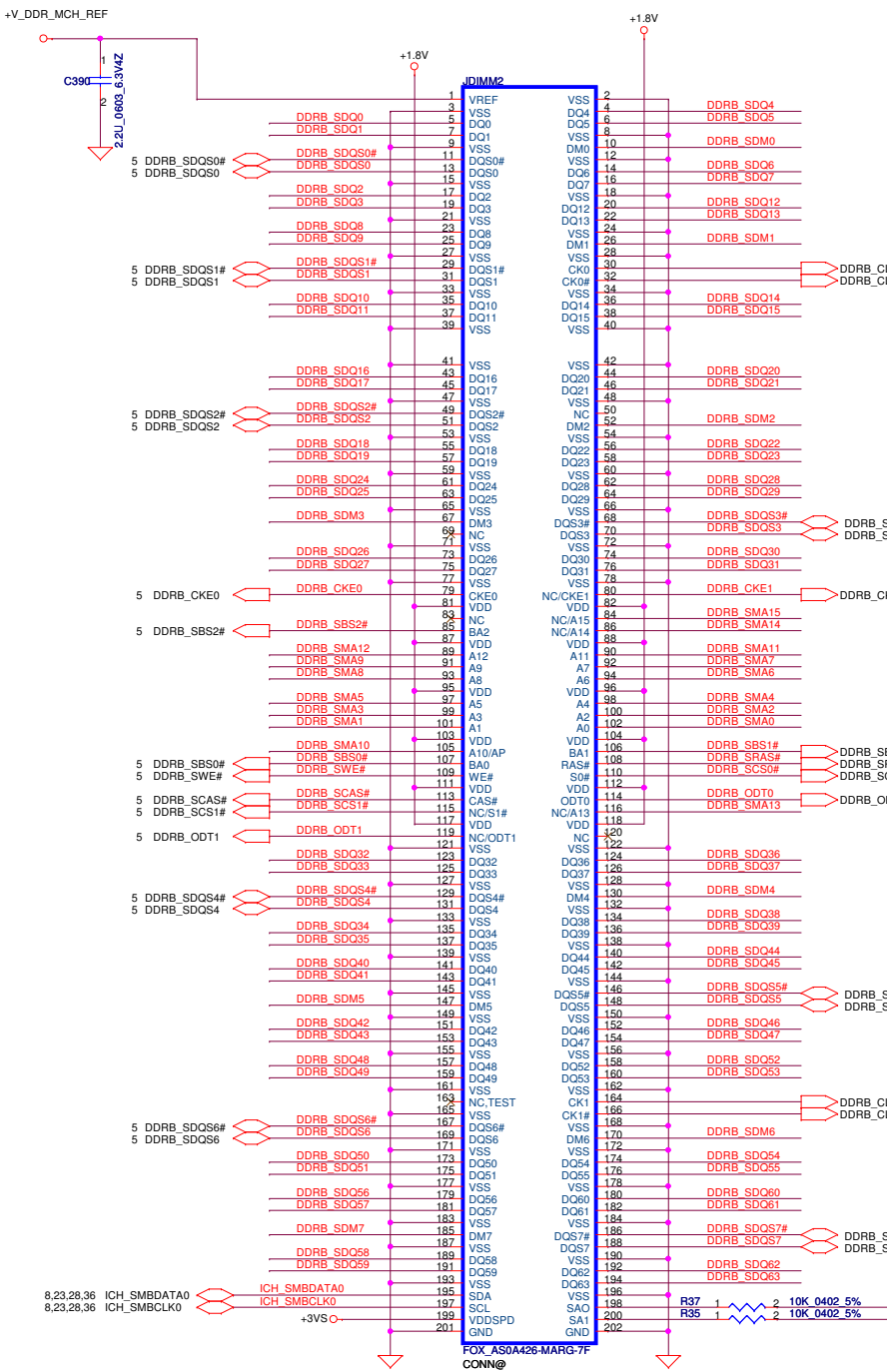
**DIMM1 REV H:5.2mm (BOT)**

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DDRII SO-DIMM 1		
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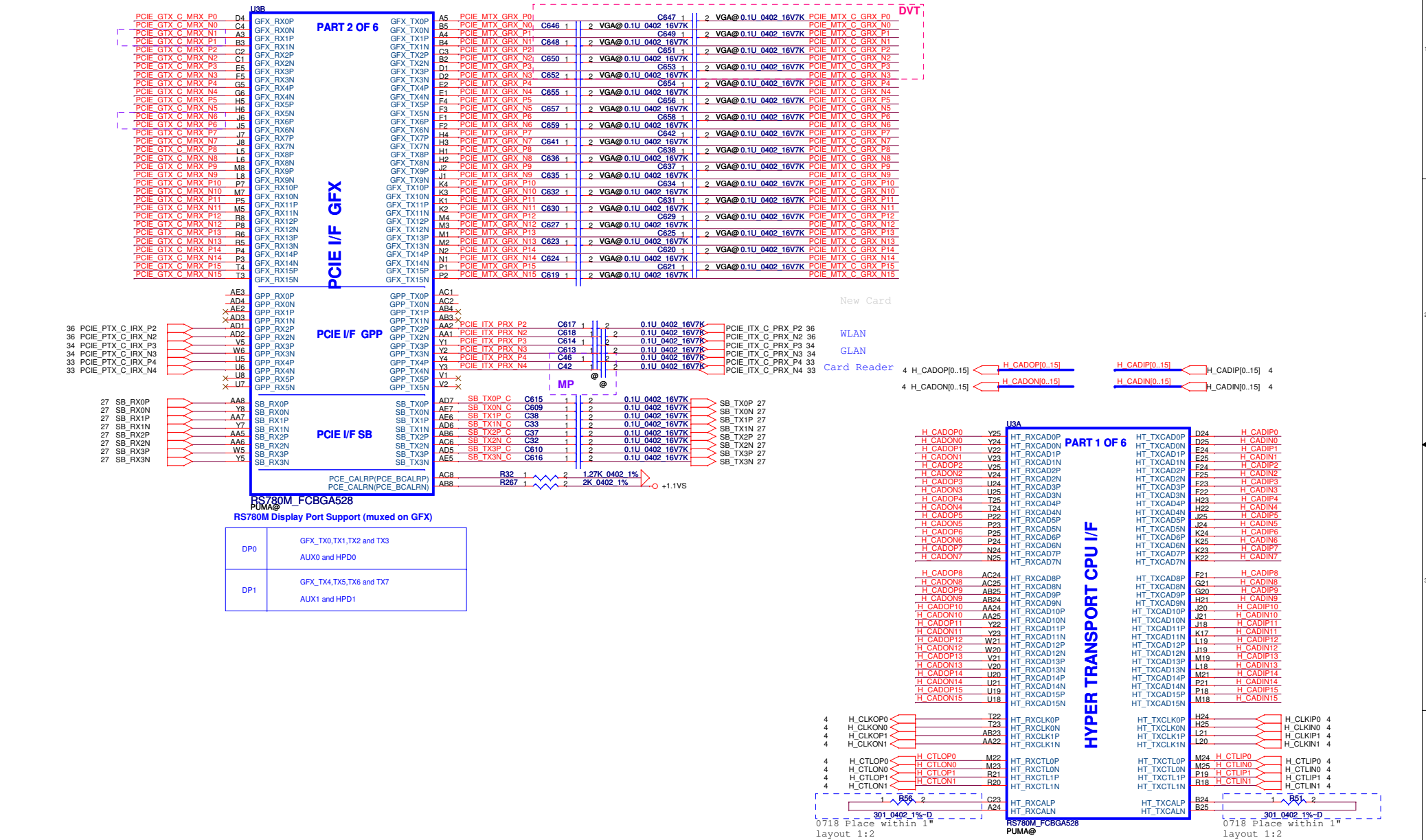
**DIMM2 REV H:9.2mm (BOT)**

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14 PCIE GTX\_C\_MRX\_P[0..15] ↔ PCIE GTX\_C\_MRX\_P[0..15]  
 14 PCIE GTX\_C\_MRX\_N[0..15] ↔ PCIE GTX\_C\_MRX\_N[0..15]

PCIE MTX\_C\_GRX\_P[0..15] ↔ PCIE MTX\_C\_GRX\_P[0..15] 14  
 PCIE MTX\_C\_GRX\_N[0..15] ↔ PCIE MTX\_C\_GRX\_N[0..15] 14

PCIE MTX\_GRX\_N[0..3] ↔ PCIE MTX\_GRX\_N[0..3] 25  
 PCIE MTX\_GRX\_P[0..3] ↔ PCIE MTX\_GRX\_P[0..3] 25



**RS780M\_FCBGA528**  
PUMA®

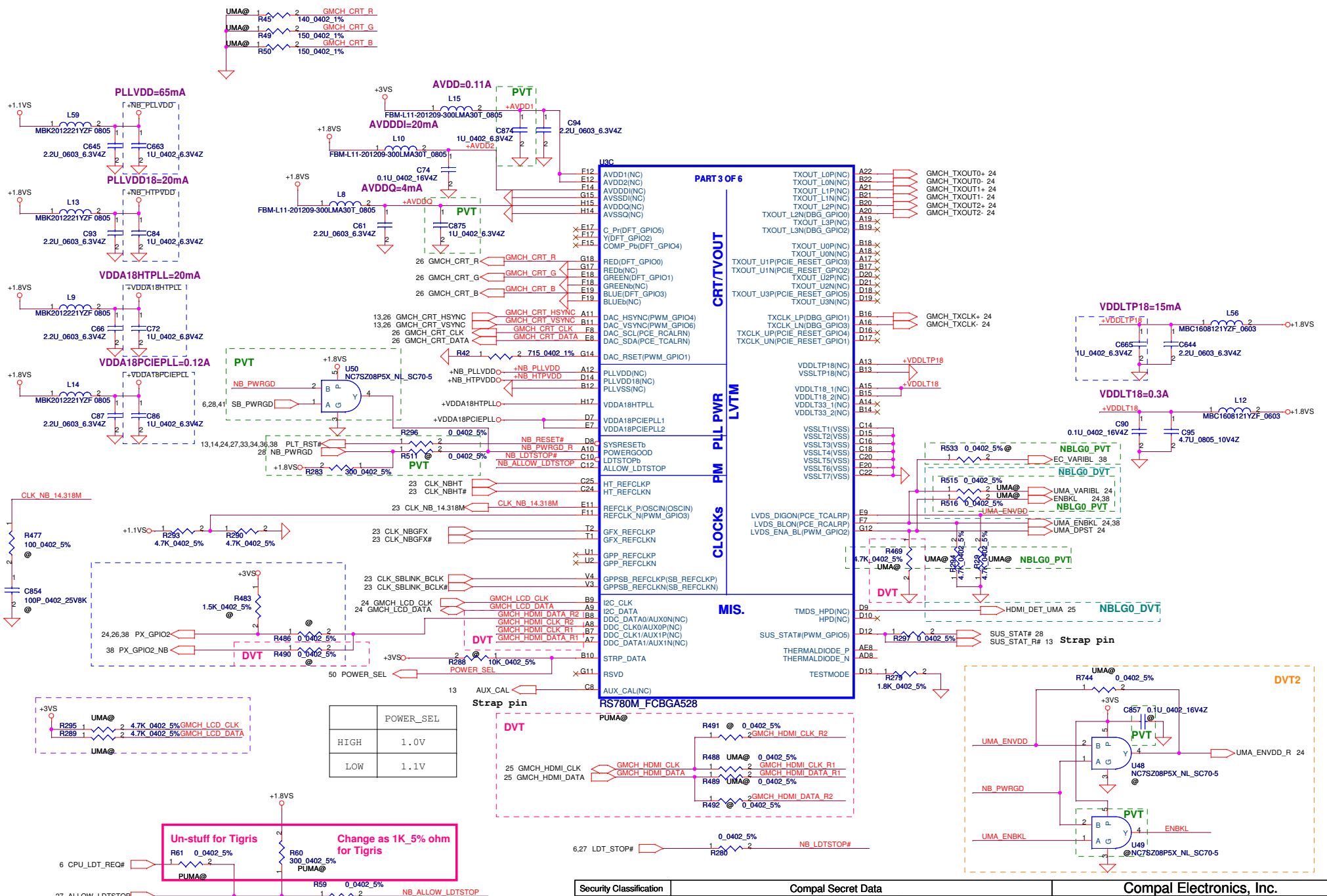
**RS780M Display Port Support (muxed on GFX)**

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

SA00002DR30 S IC 216-0674026 A13 RS780M FCBGA 0FA  
 SA000032T10 S IC 216-0752001 A11 RS80M FCBGA528 0FA

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				<b>RS800-HT/PCIE</b>
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For RS780M A13  
 RED: Connected to GND through two separate 140ohm 1% resistor



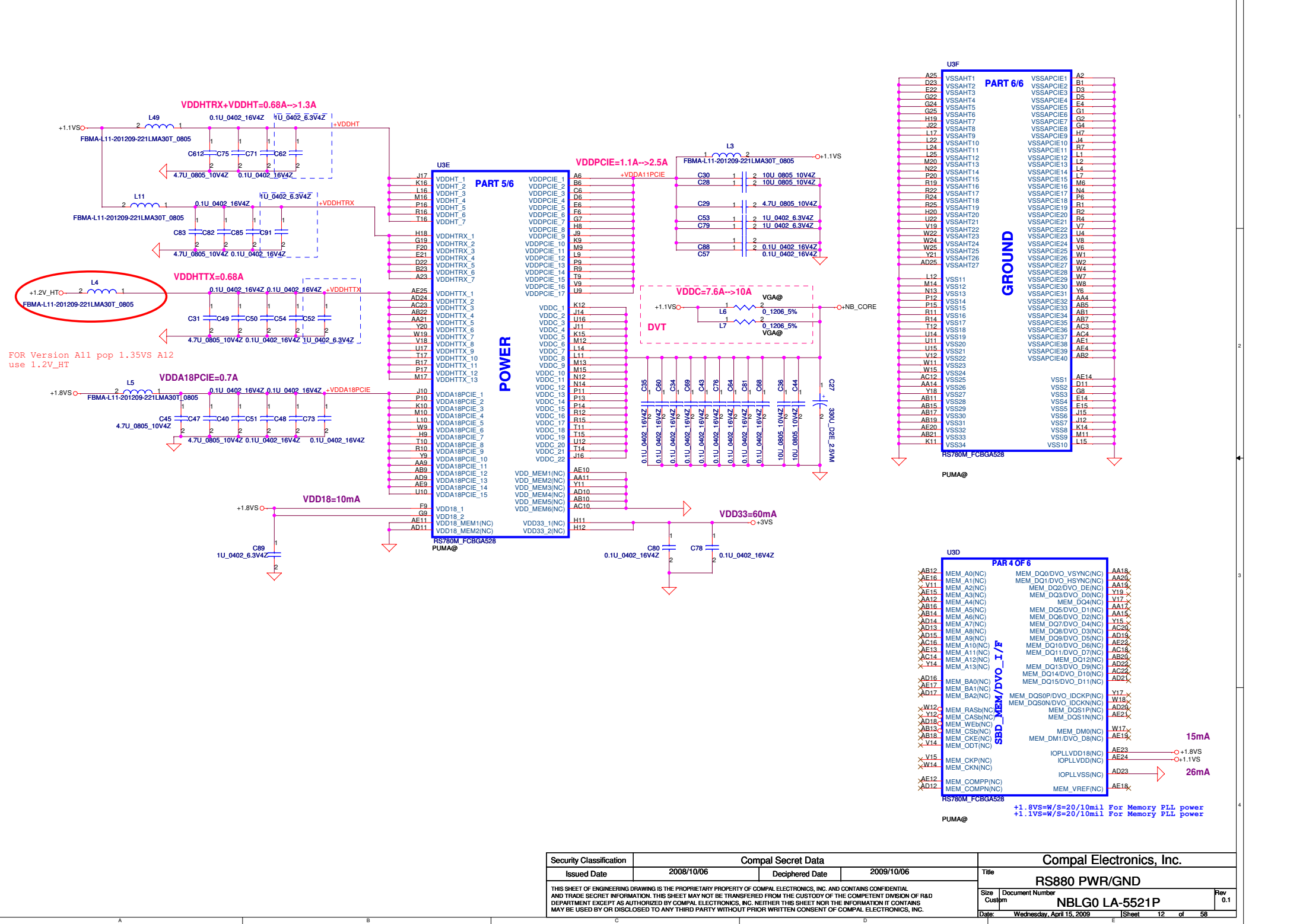
POWER_SEL	POWER_SEL
HIGH	1.0V
LOW	1.1V

Un-stuff for Tigris  
 Change as 1K\_5% ohm for Tigris

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Compal Electronics, Inc.		
RS880 VEDIO/CLK GEN		
NBLG0 LA-5521P		
Date:	Thursday, June 04, 2009	Sheet 11 of 58



FOR Version All pop 1.35VS A12 use 1.2V\_HT

**GROUND**

**POWER**

U3F

U3D

**PART 6/6**

A25	VSSAHT1	VSSAPCIE1	A2
D23	VSSAHT2	VSSAPCIE2	B1
E22	VSSAHT3	VSSAPCIE3	D3
G24	VSSAHT4	VSSAPCIE4	D5
G25	VSSAHT5	VSSAPCIE5	G1
H19	VSSAHT6	VSSAPCIE6	G2
J22	VSSAHT7	VSSAPCIE7	G4
L17	VSSAHT8	VSSAPCIE8	H1
L22	VSSAHT9	VSSAPCIE9	H4
L24	VSSAHT10	VSSAPCIE10	H7
L25	VSSAHT11	VSSAPCIE11	R7
M20	VSSAHT12	VSSAPCIE12	L1
M22	VSSAHT13	VSSAPCIE13	L4
P20	VSSAHT14	VSSAPCIE14	L7
R19	VSSAHT15	VSSAPCIE15	M6
R22	VSSAHT16	VSSAPCIE16	N4
R24	VSSAHT17	VSSAPCIE17	P8
R25	VSSAHT18	VSSAPCIE18	R1
H20	VSSAHT19	VSSAPCIE19	R2
U22	VSSAHT20	VSSAPCIE20	R4
Y19	VSSAHT21	VSSAPCIE21	R7
W22	VSSAHT22	VSSAPCIE22	U4
W24	VSSAHT23	VSSAPCIE23	U4
W25	VSSAHT24	VSSAPCIE24	U8
Y21	VSSAHT25	VSSAPCIE25	U8
AD25	VSSAHT26	VSSAPCIE26	W2
	VSSAHT27	VSSAPCIE27	W4
	VSSAHT28	VSSAPCIE28	W4
	VSSAHT29	VSSAPCIE29	W7
L12	VSS11	VSS11	W8
M14	VSS12	VSS12	Y6
N13	VSS13	VSS13	Y6
P12	VSS14	VSS14	AA4
P15	VSS15	VSS15	AA5
R14	VSS16	VSS16	AB7
T12	VSS17	VSS17	AC3
U11	VSS18	VSS18	AC4
U14	VSS19	VSS19	AC4
U15	VSS20	VSS20	AE1
V12	VSS21	VSS21	AE4
W11	VSS22	VSS22	AE4
W15	VSS23	VSS23	AE8
AA14	VSS24	VSS24	AE14
AA14	VSS25	VSS25	D11
Y18	VSS26	VSS26	G8
AB11	VSS27	VSS27	G14
AB17	VSS28	VSS28	E14
AB19	VSS29	VSS29	E15
AE20	VSS30	VSS30	J15
AB21	VSS31	VSS31	J12
	VSS32	VSS32	K14
	VSS33	VSS33	M11
	VSS34	VSS34	L15

PUMA@

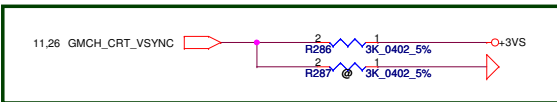
PUMA@

**PAR 4 OF 6**

>AB12	MEM_A0(NC)	MEM_D0Q/DVQ_VSYNC(NC)	AA18X
>AE16	MEM_A1(NC)	MEM_D01/DVQ_HSYNC(NC)	AA20X
>Y11	MEM_A2(NC)	MEM_D02/DVQ_DE(NC)	AA18X
>AE15	MEM_A3(NC)	MEM_D03/DVQ_D0(NC)	Y18X
>AA12	MEM_A4(NC)	MEM_D04(NC)	V17X
>AB16	MEM_A5(NC)	MEM_D05/DVQ_D1(NC)	AA17X
>AB14	MEM_A6(NC)	MEM_D06/DVQ_D2(NC)	AA15X
>AD14	MEM_A7(NC)	MEM_D07/DVQ_D4(NC)	Y15X
>AD13	MEM_A8(NC)	MEM_D08/DVQ_D3(NC)	AC20X
>AD15	MEM_A9(NC)	MEM_D09/DVQ_D5(NC)	AD19X
>AC16	MEM_A10(NC)	MEM_D010/DVQ_D6(NC)	AE22X
>AE13	MEM_A11(NC)	MEM_D011/DVQ_D7(NC)	AC18X
>AC14	MEM_A12(NC)	MEM_D012(NC)	AE20X
>Y14	MEM_A13(NC)	MEM_D013/DVQ_D9(NC)	AD22X
>AD16	MEM_BA0(NC)	MEM_D014/DVQ_D10(NC)	AC22X
>AE17	MEM_BA1(NC)	MEM_D015/DVQ_D11(NC)	AD21X
>AD17	MEM_BA2(NC)		
>W12	MEM_DQS0P/DVQ_IDCKP(NC)		Y17X
>Y12	MEM_DQS0N/DVQ_IDCKN(NC)		W13X
>AD18	MEM_DQS1P(NC)		AD20X
>AB13	MEM_DQS1(NC)		AE21X
>AB18	MEM_DM0(NC)		W17X
>Y14	MEM_DM1/DVQ_D8(NC)		AE19X
>Y15	MEM_CKP(NC)		
>W14	MEM_CKN(NC)		
>AE12	MEM_COMP1(NC)		
>AD12	MEM_COMP2(NC)		
	MEM_VREF(NC)		

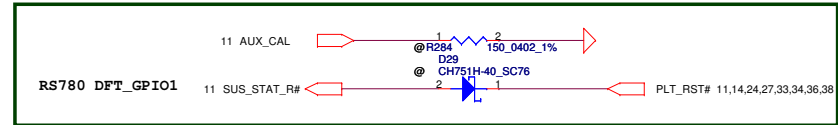
+1.8VS=W/S=20/10mil For Memory PLL power  
+1.1VS=W/S=20/10mil For Memory PLL power

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Custom	NBLG0 LA-5521P					



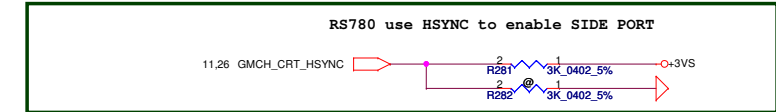
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO. (VSYNC)  
 1 : Disable (RS780)  
 0 : Enable (Rs780)



**DFT\_GPIO1:LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**RS780 use HSYNC to enable SIDE PORT**

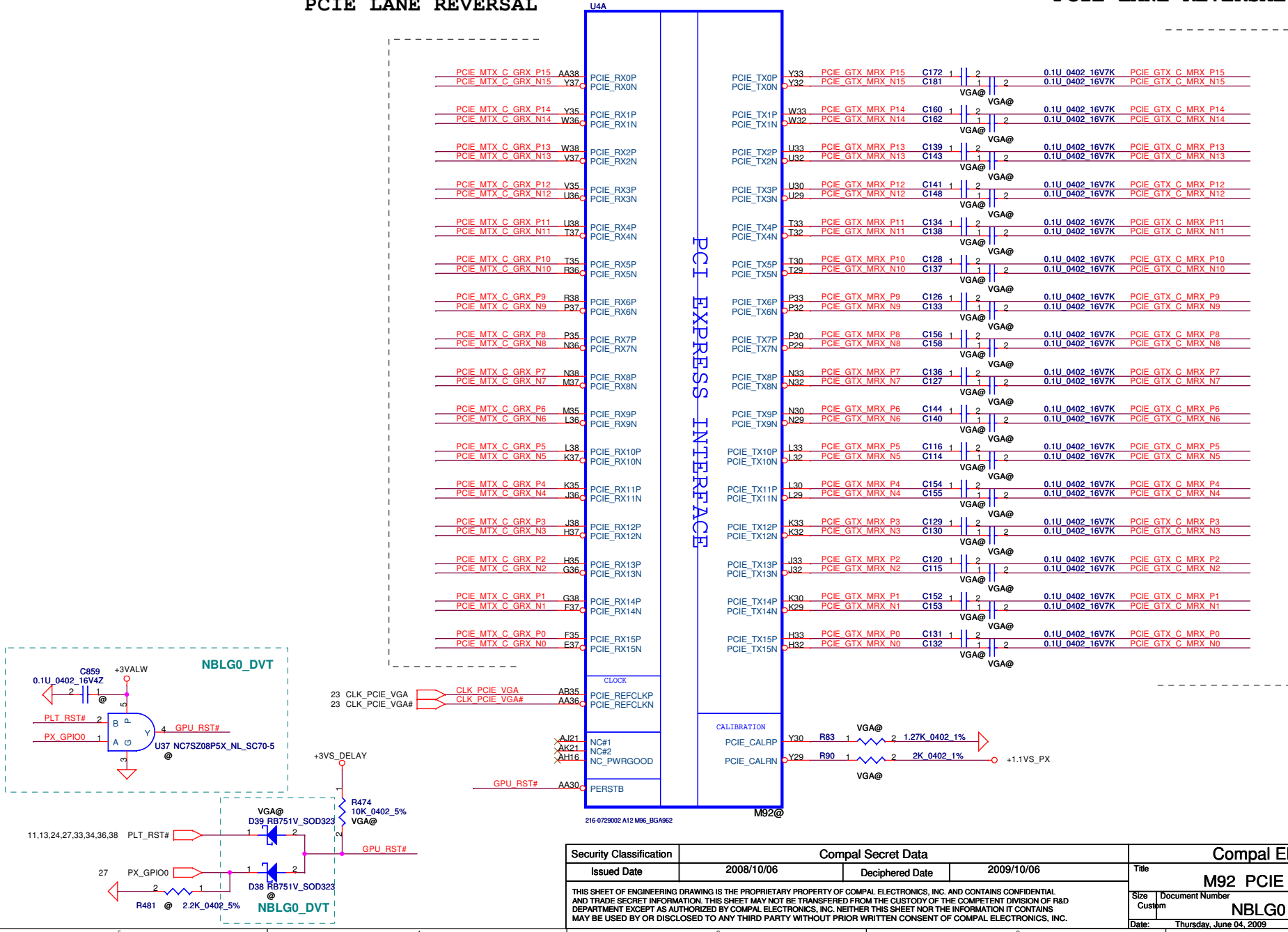
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 0 : Enable (RS780)  
 1 : Disable(RS780)

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				Custom	NBLG0 LA-5521P
				Date:	Thursday, June 04, 2009
				Sheet	13 of 58
				Rev	0.1

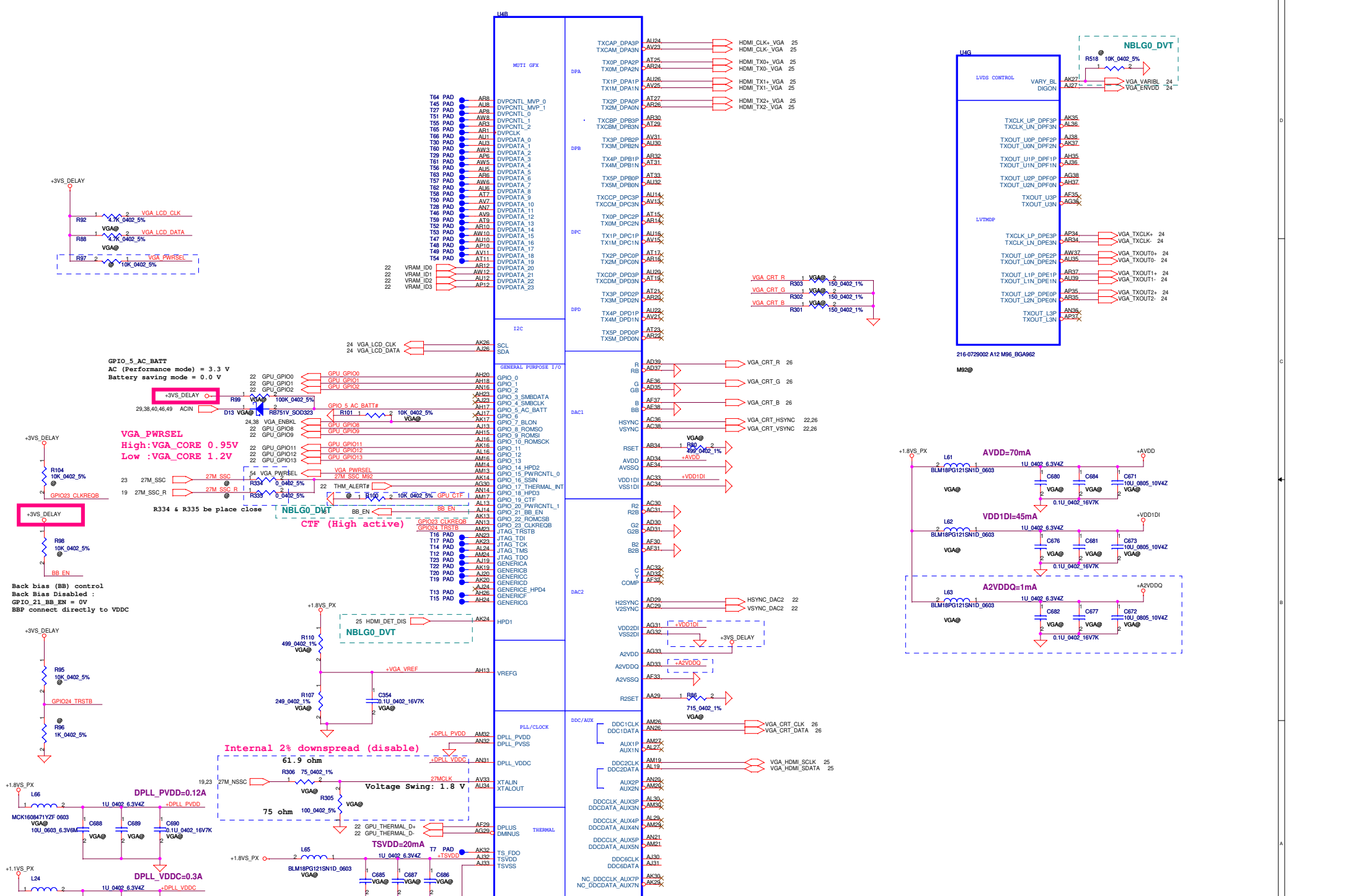
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- 10 PCIE\_GTX\_C\_MRX\_N[0..15] ← PCIE GTX C MRX N[0..15]
- 10 PCIE\_MTX\_C\_GRX\_P[0..15] ← PCIE MTX C GRX P[0..15]
- 10 PCIE\_MTX\_C\_GRX\_N[0..15] ← PCIE MTX C GRX N[0..15]

**PCIE LANE REVERSAL**

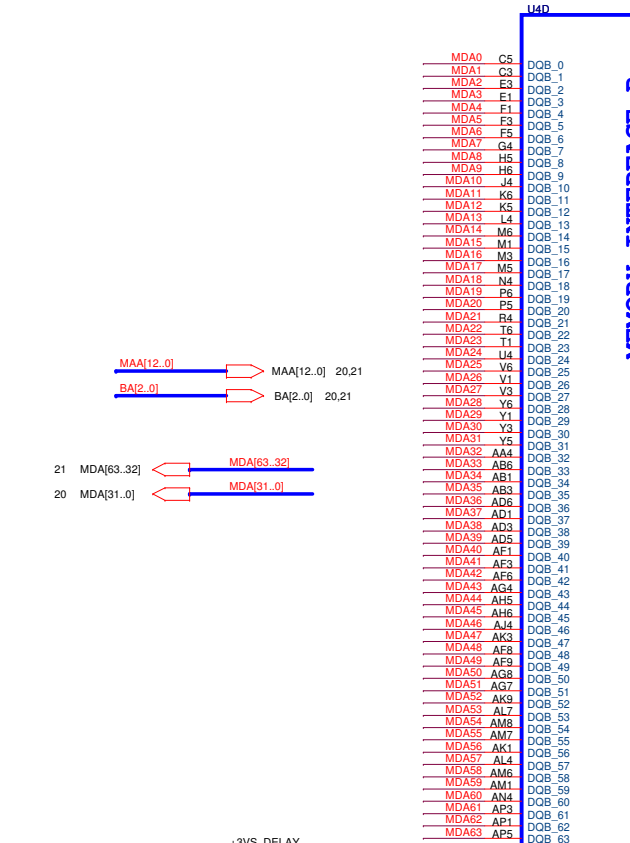
**PCIE LANE REVERSAL**



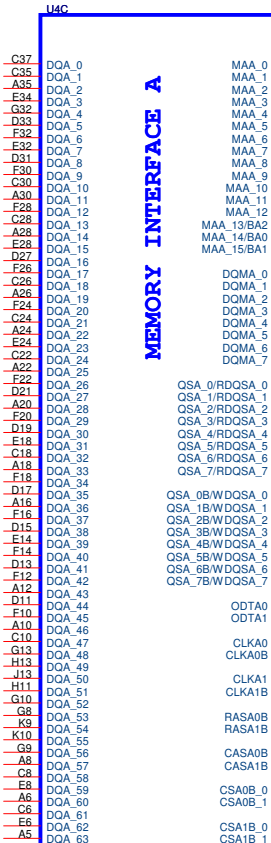
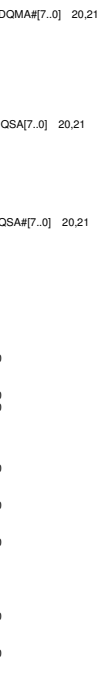
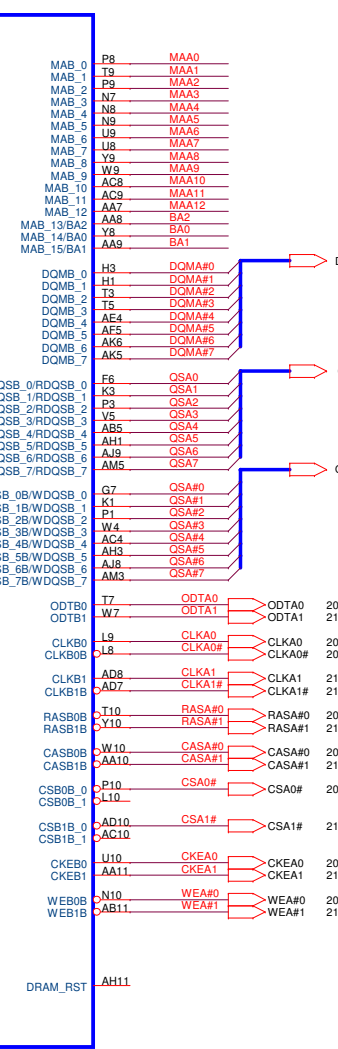
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Size	Document Number	NBLG0 LA-5521P		Rev	0.1
Customer	Date: Thursday, June 04, 2009				Sheet 14 of 58



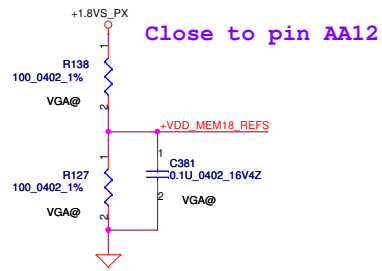
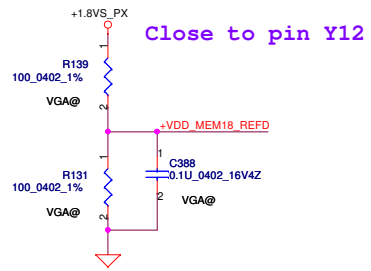
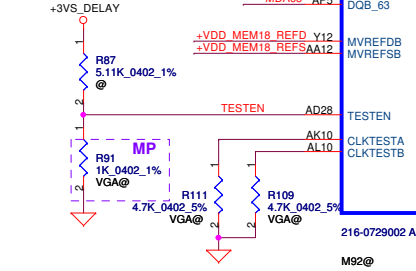
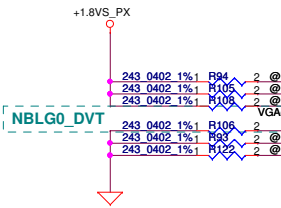
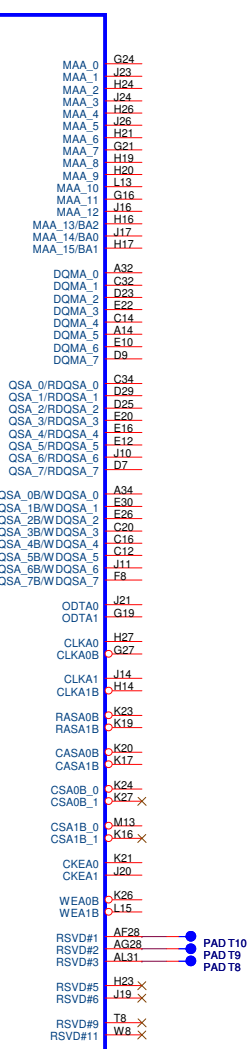
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Size	Document Number	NBLG0 LA-5521P		Rev	0.1
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**MEMORY INTERFACE B**



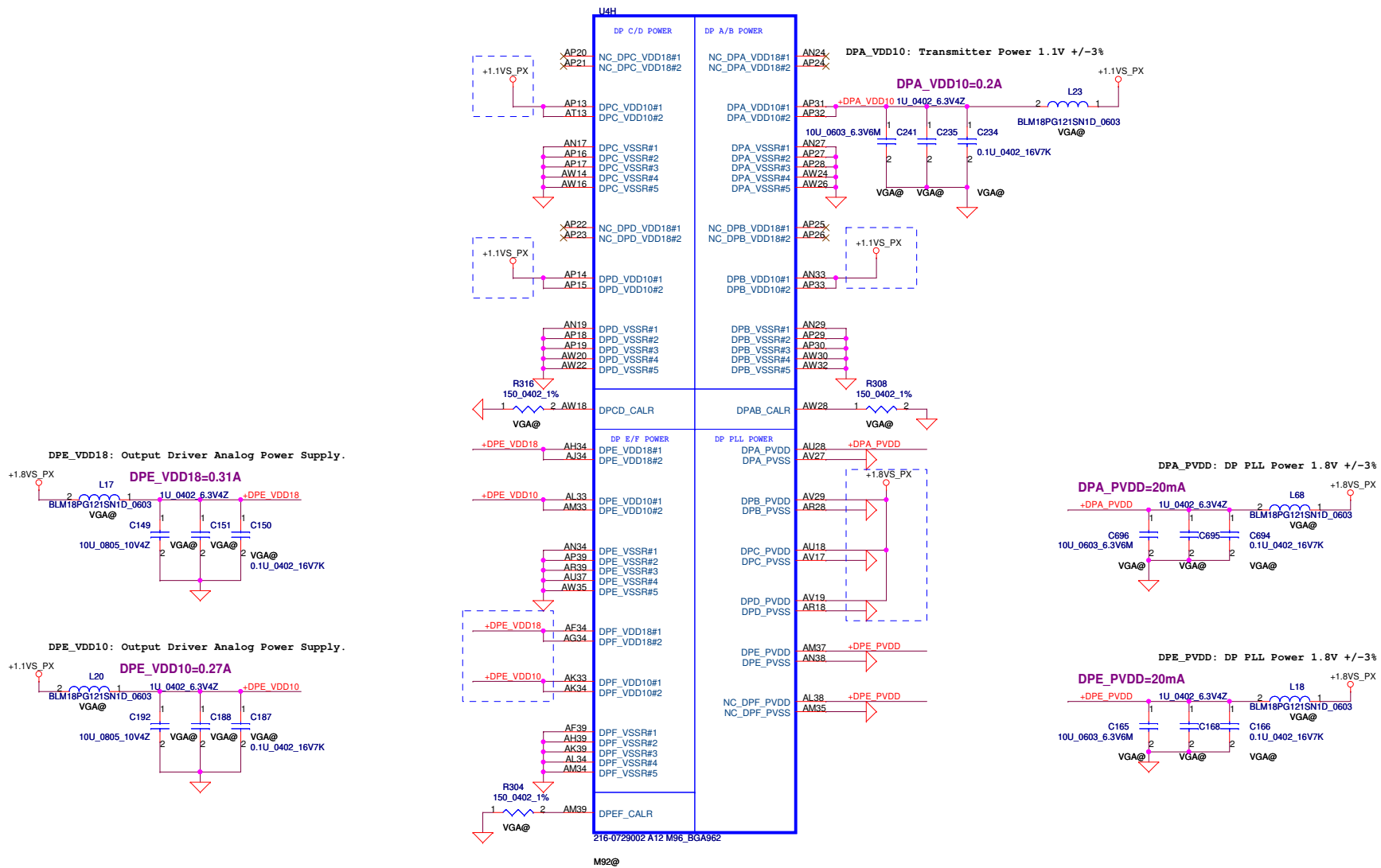
**MEMORY INTERFACE A**



M92-S2 and M92-M use memory group A only while M92-M2 uses memory group B only.

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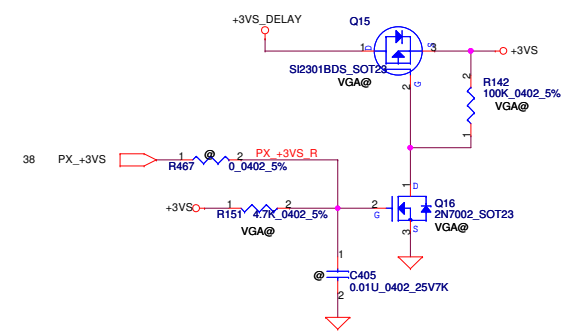
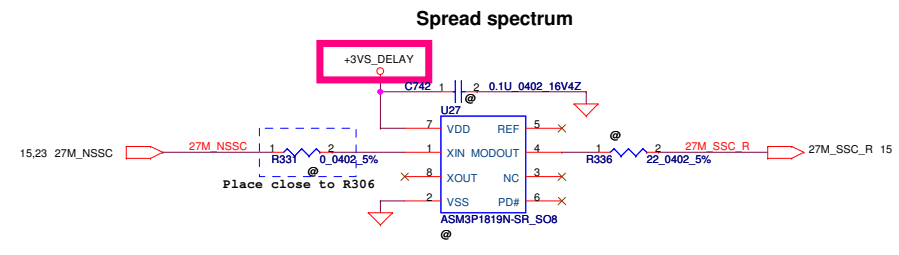
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AB39	PCIE_VSS#1	A3	GND#1
E39	PCIE_VSS#2	A37	GND#2
F34	PCIE_VSS#3	AA16	GND#3
F39	PCIE_VSS#4	AA18	GND#4
G33	PCIE_VSS#5	AA2	GND#5
G34	PCIE_VSS#6	AA21	GND#6
H31	PCIE_VSS#7	AA23	GND#7
H34	PCIE_VSS#8	AA26	GND#8
H39	PCIE_VSS#9	AA28	GND#9
J1	PCIE_VSS#10	AA6	GND#10
J4	PCIE_VSS#11	AB12	GND#11
K31	PCIE_VSS#12	AB15	GND#12
K34	PCIE_VSS#13	AB17	GND#13
K39	PCIE_VSS#14	AB20	GND#14
L31	PCIE_VSS#15	AB22	GND#15
L34	PCIE_VSS#16	AB24	GND#16
M34	PCIE_VSS#17	AB27	GND#17
M39	PCIE_VSS#18	AC11	GND#18
N31	PCIE_VSS#19	AC13	GND#19
N34	PCIE_VSS#20	AC16	GND#20
P31	PCIE_VSS#21	AC18	GND#21
P34	PCIE_VSS#22	AC2	GND#22
P39	PCIE_VSS#23	AC21	GND#23
R34	PCIE_VSS#24	AC23	GND#24
T31	PCIE_VSS#25	AC26	GND#25
T34	PCIE_VSS#26	AC28	GND#26
T39	PCIE_VSS#27	AC6	GND#27
U31	PCIE_VSS#28	AD15	GND#28
U34	PCIE_VSS#29	AD17	GND#29
V34	PCIE_VSS#30	AD20	GND#30
V39	PCIE_VSS#31	AD22	GND#31
W31	PCIE_VSS#32	AD24	GND#32
W34	PCIE_VSS#33	AD27	GND#33
Y34	PCIE_VSS#34	AD9	GND#34
Y39	PCIE_VSS#35	AE2	GND#35
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		AE18	GND#39
		AF21	GND#40
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		AG2	GND#42
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		AH29	GND#48
		AJ10	GND#49
		AJ11	GND#50
		AJ2	GND#51
		AJ28	GND#52
		AJ6	GND#53
		AK11	GND#54
		AK31	GND#55
		AK7	GND#56
		AL11	GND#57
		AL14	GND#58
		AL17	GND#59
		AL2	GND#60
		AL20	GND#61
		AL21	GND#62
		AL23	GND#63
		AL26	GND#64
		AL32	GND#65
		AL6	GND#66
		AL8	GND#67
		AM11	GND#68
		AM31	GND#69
		AM9	GND#70
		AN11	GND#71
		AN2	GND#72
		AN30	GND#73
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		AP11	GND#76
		AP7	GND#77
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		B31	GND#91
		B33	GND#92
		B7	GND#93
		B9	GND#94
		C1	GND#95
		C39	GND#96
		E35	GND#97
		E5	GND#98
		F11	GND#99
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		AW39	VSS_MECH#3

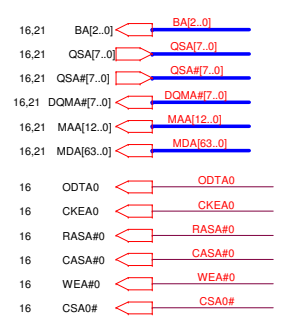
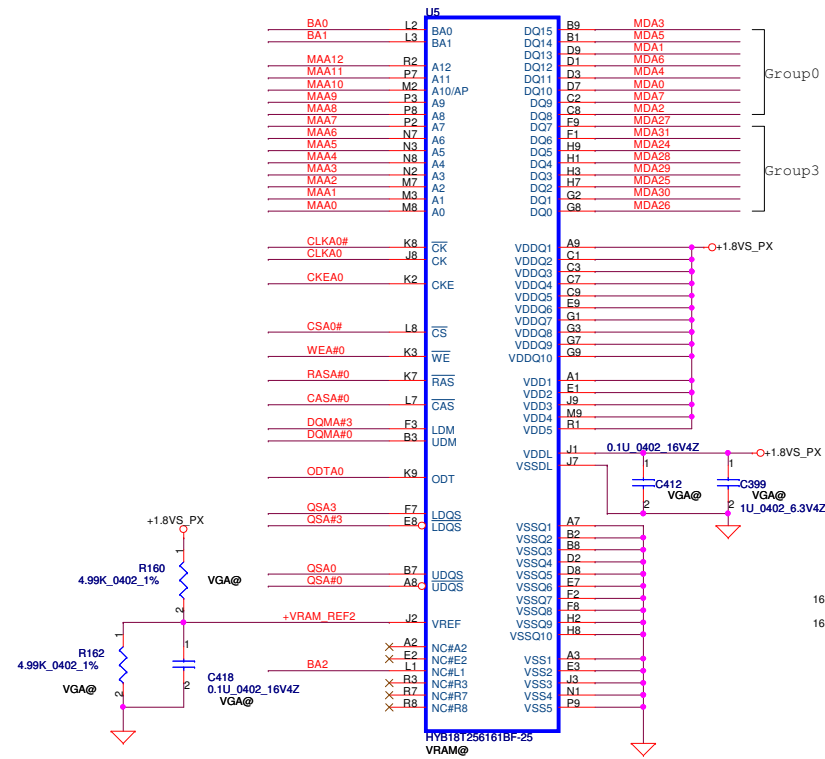
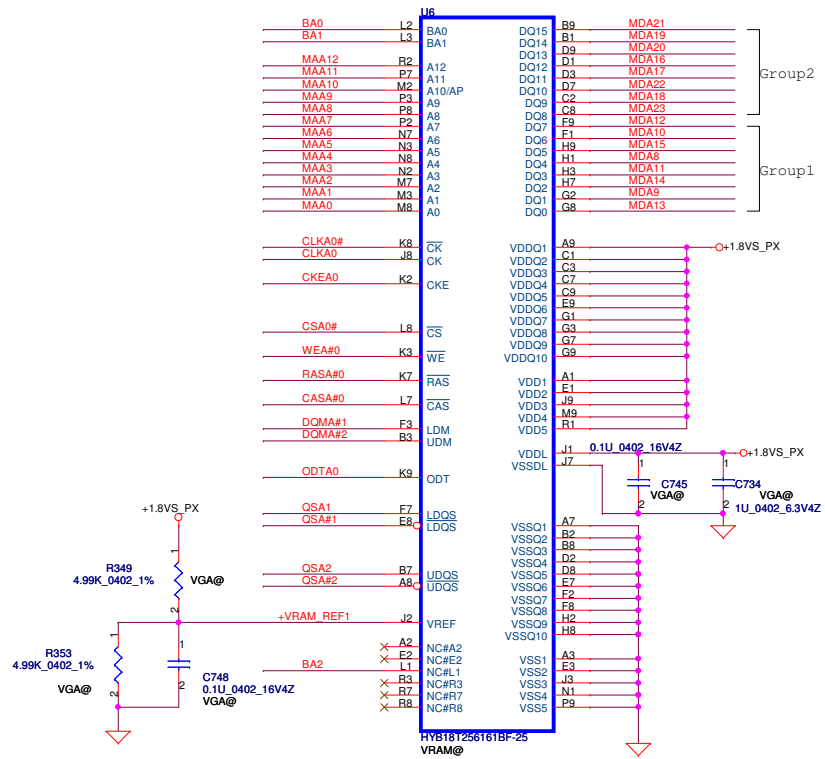
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M92@

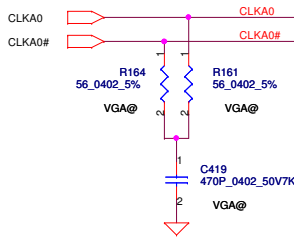
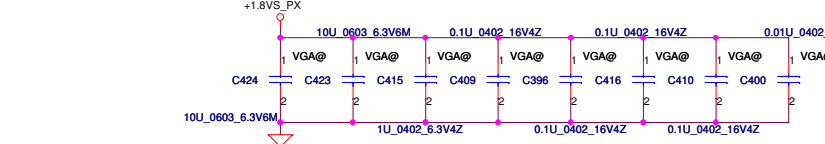
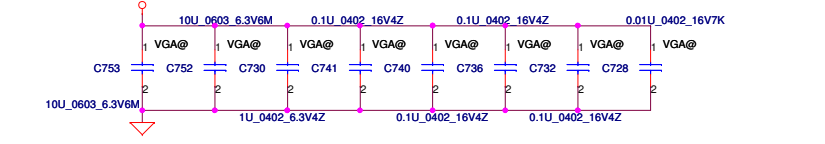


Use Delay 3.3V BUS (VDDR3) for GPIO/DCC Pull up to reduce Leakage to VDDR3 Bus.

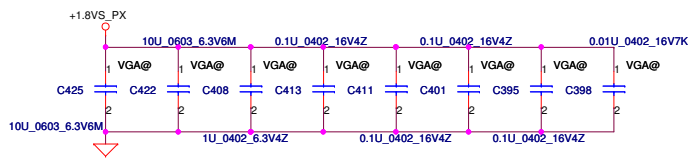
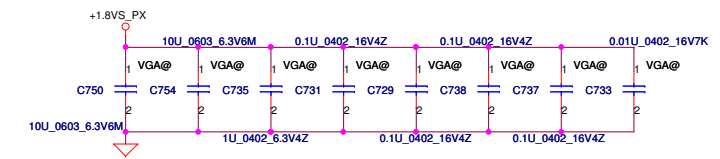
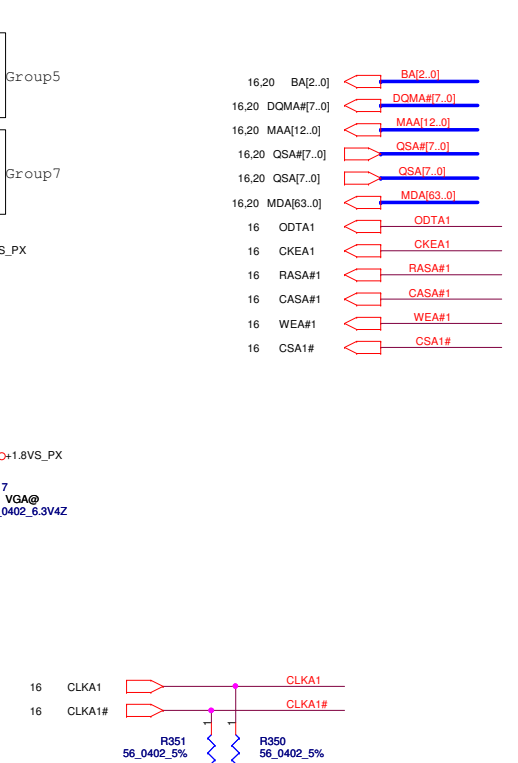
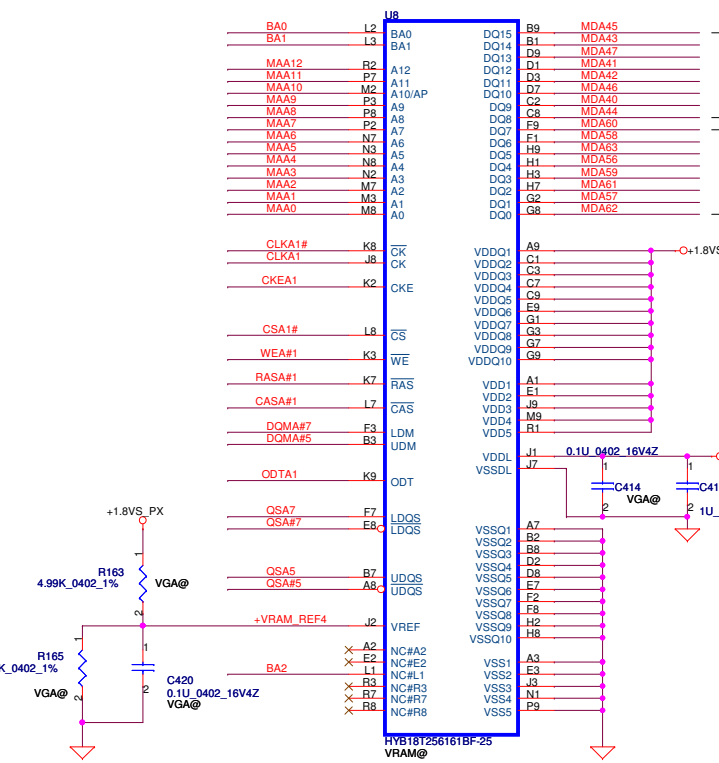
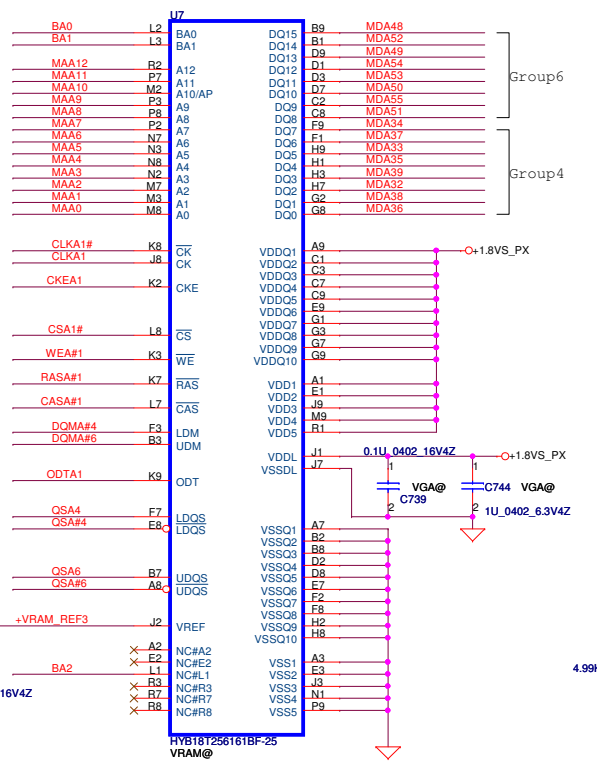
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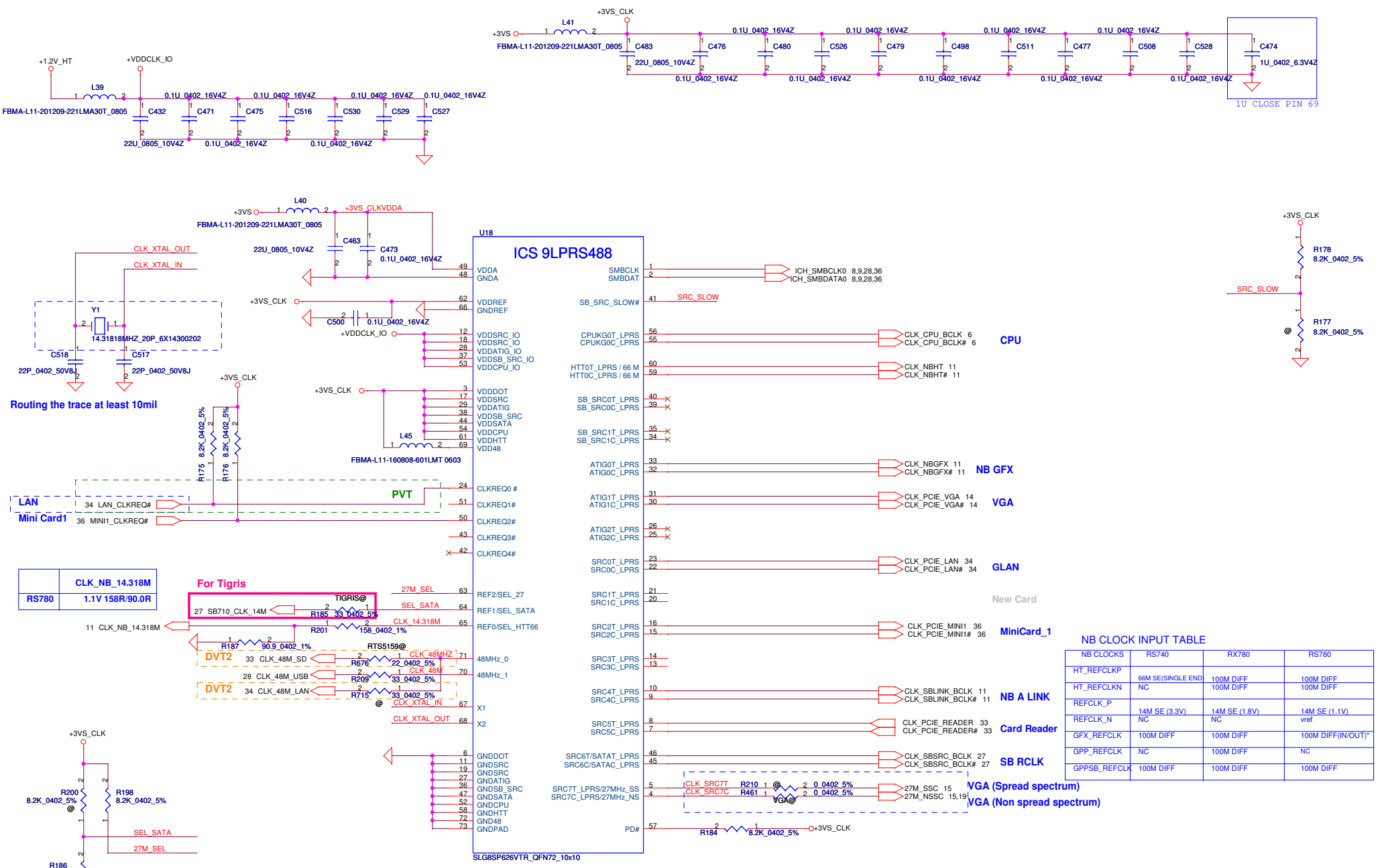


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Issued Date	2008/10/06	Deciphered Date	2009/10/06	M92 VRAM	
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Date: Thursday, June 04, 2009				Sheet	20 of 56



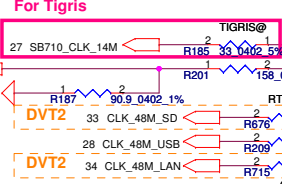
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				M92 VRAM	
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Routing the trace at least 10mil

CLK_NB_14.318M	
RS780	1.1V 158R/90.0R



**NB CLOCK INPUT TABLE**

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V) vref
REFCLK_N	NC	NC	
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF('N/OUT')
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

1st (SILEGO) : SA00001Z310 S IC SGL8SP626VTR QFN 72P CLK GEN  
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

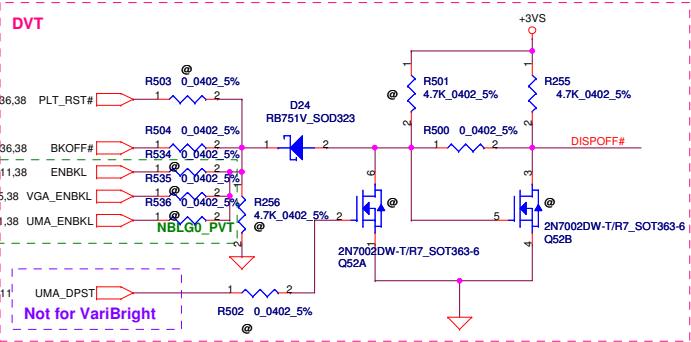
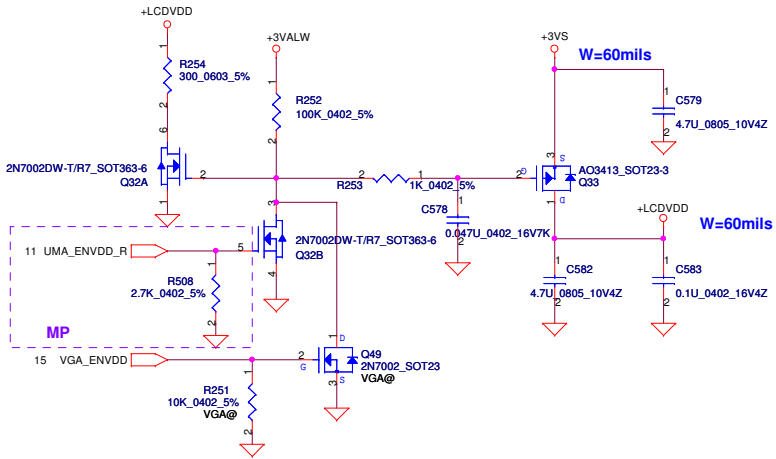
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

\* default

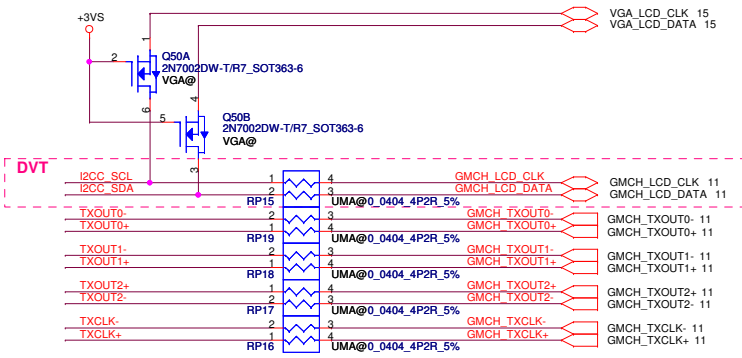
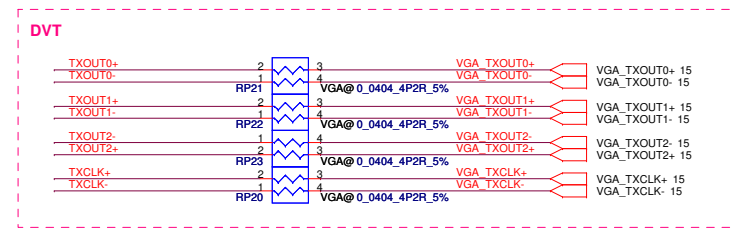
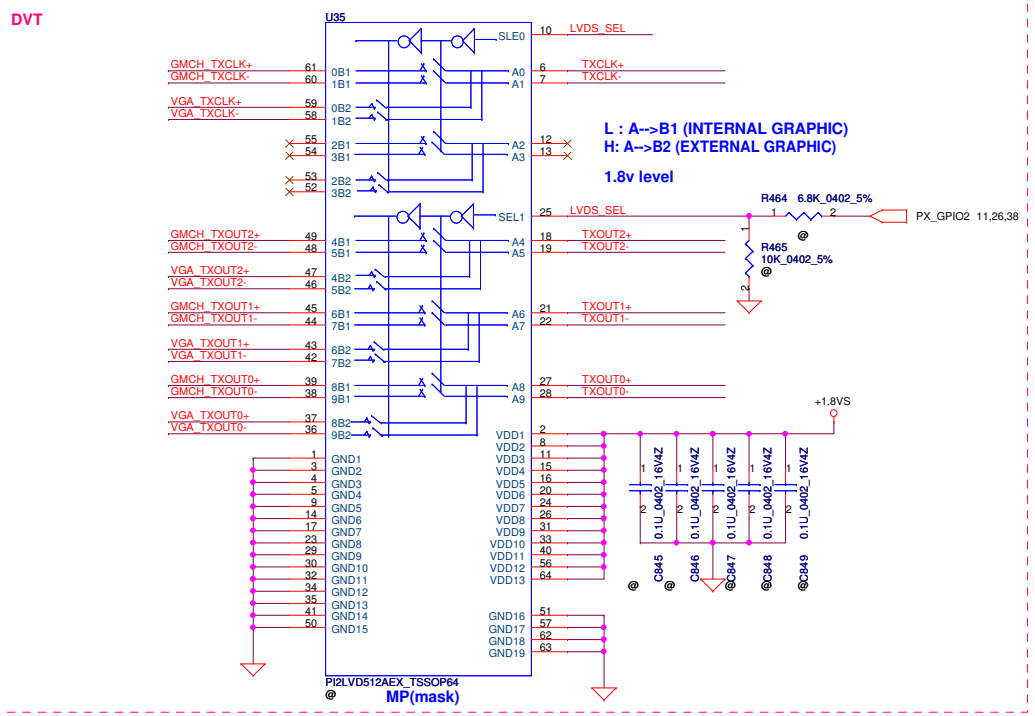
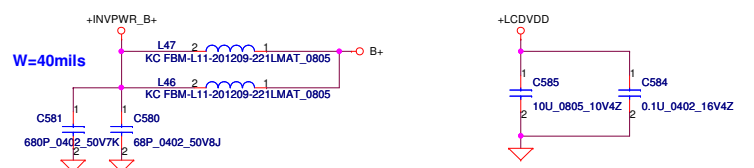
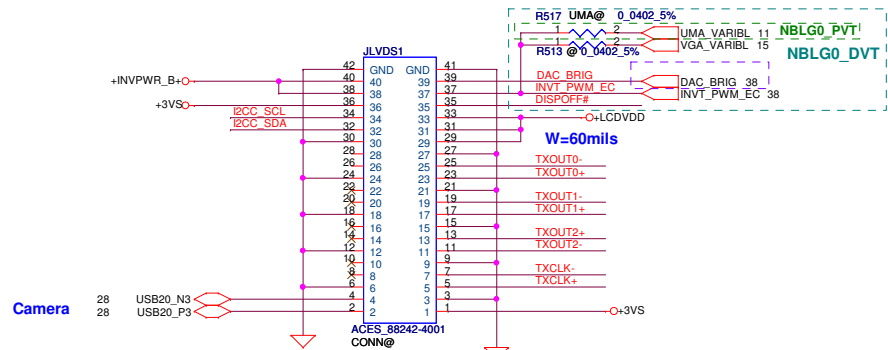
27M_SEL	1*	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

<b>Security Classification</b>	<b>Compal Secret Data</b>			<b>Compal Electronics, Inc.</b>		
<b>Issued Date</b>	2008/10/06	<b>Deciphered Date</b>	2009/10/06	<b>Title</b>		
				<b>Clock generator</b>		
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				Custom	<b>NBLG0 LA-5521P</b>	0.1
				<b>Date:</b>	Thursday, June 04, 2009	<b>Sheet</b> 23 <b>of</b> 58

# LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.

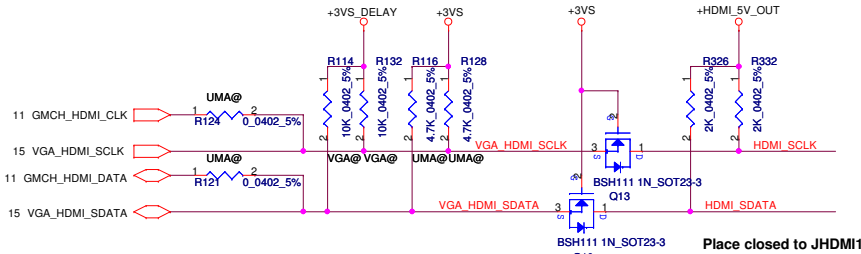


Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Compal Electronics, Inc.	
				LVDS Connector	
Size	Document Number	NBLG0 LA-5521P		Rev	0.1
B				Date:	Thursday, June 04, 2009
				Sheet	24 of 58

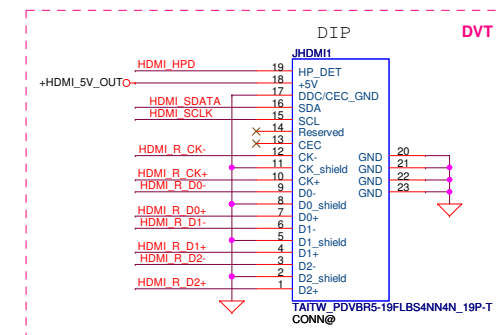
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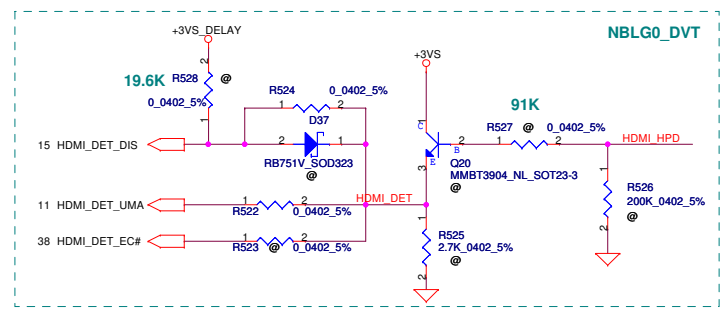
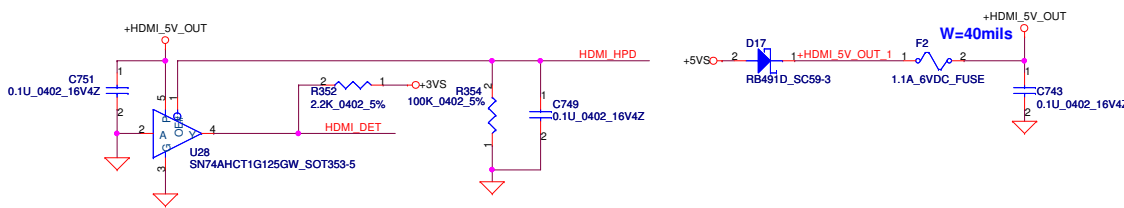
**DDC to HDMI CONN**



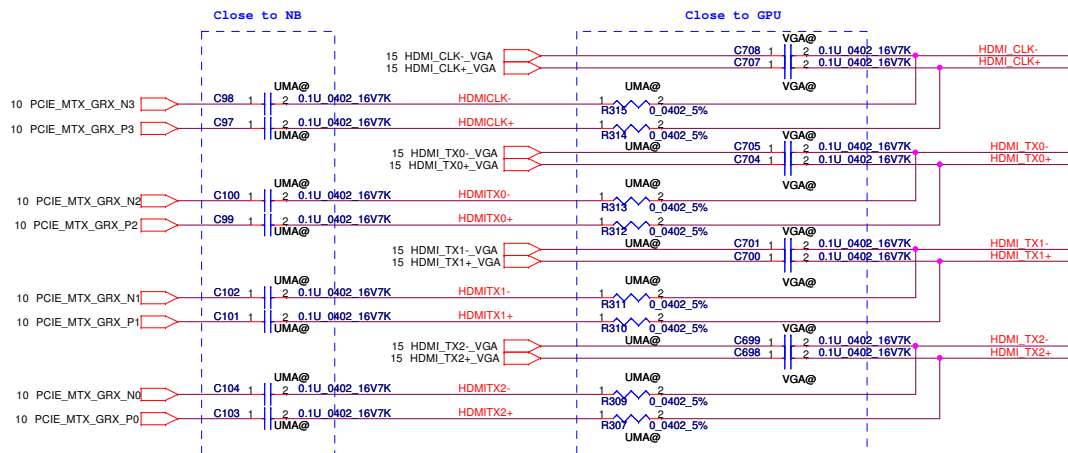
Place closed to JHDMI1



DVT

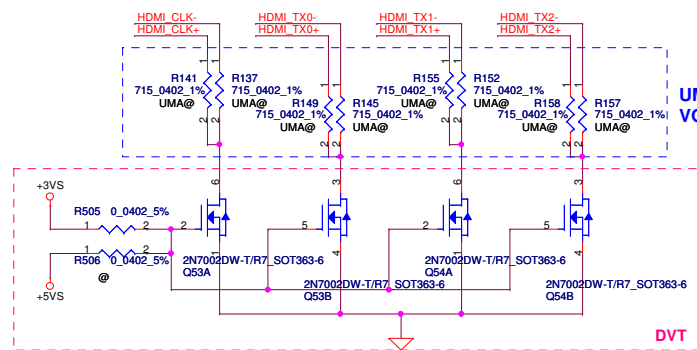


NBLGO\_DVT

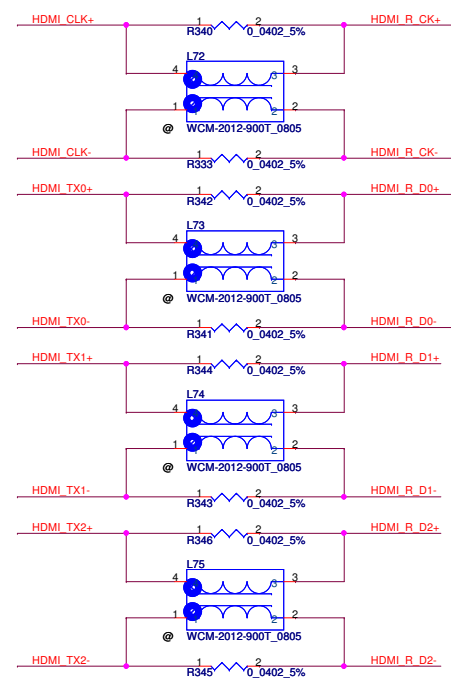


Update (For Puma / Tigris default value)

UMA use 715 ohm  
VGA use 499 ohm



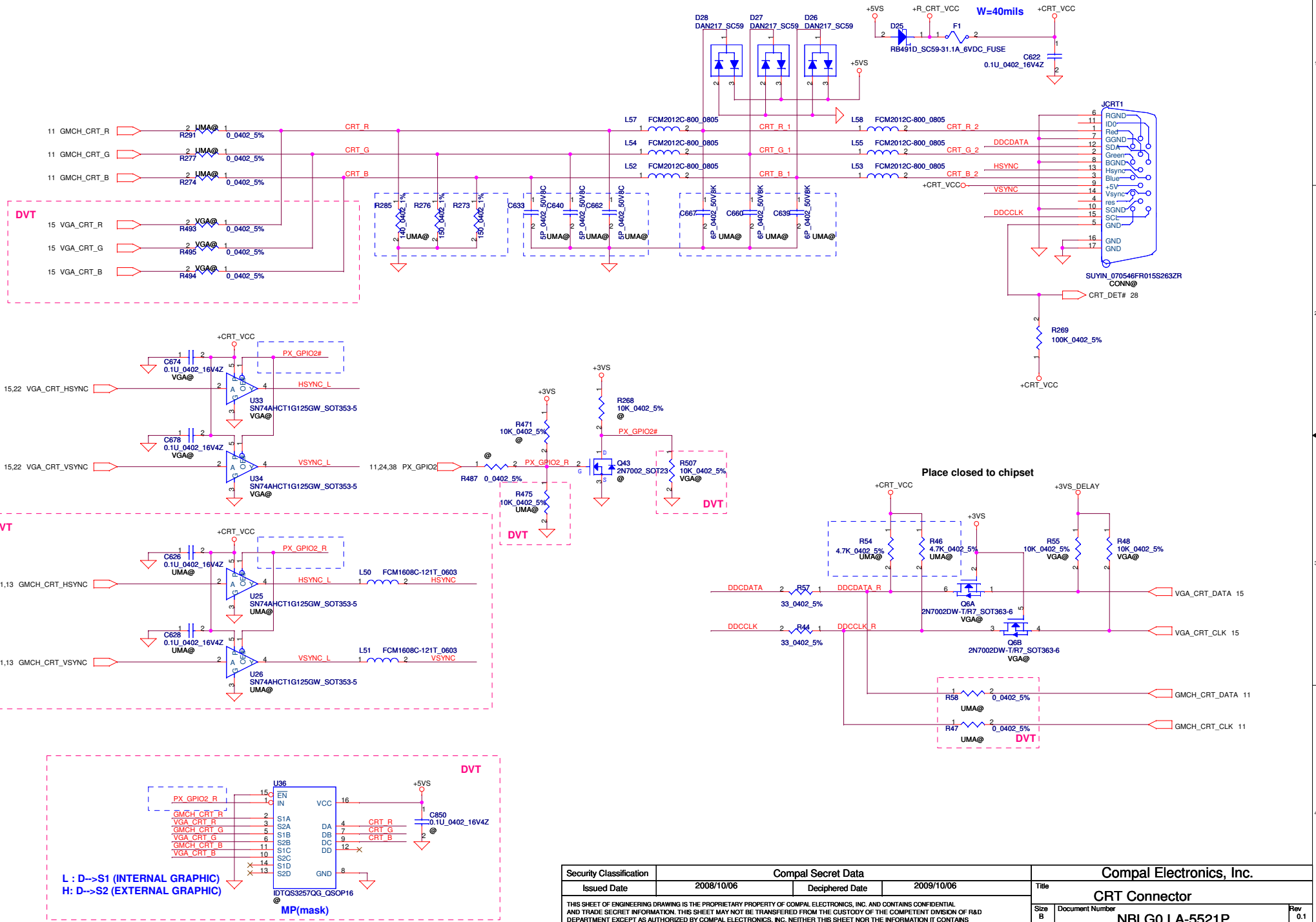
DVT



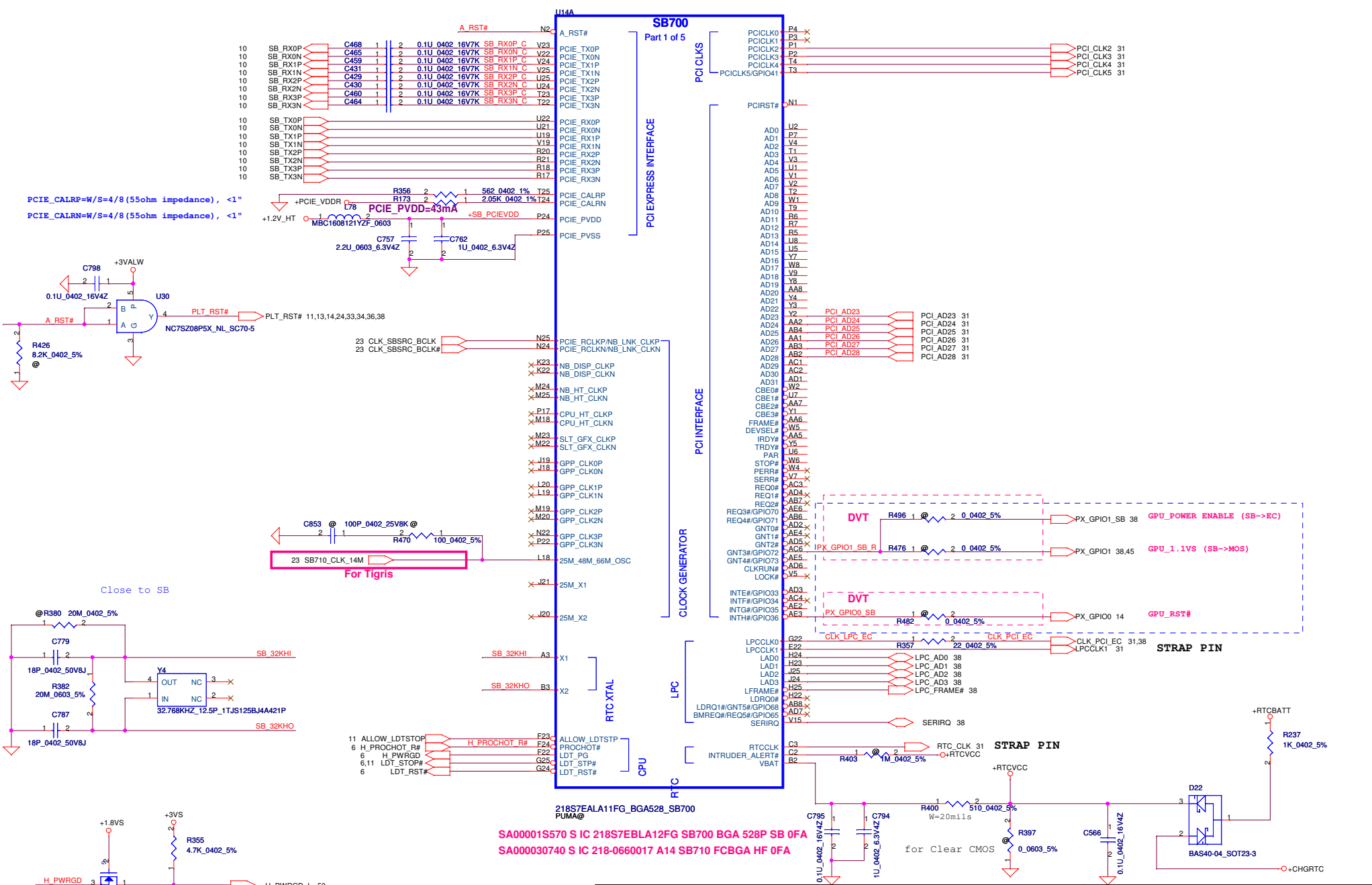
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				HDMI Connector	
				Size	Document Number
				Custom	NBLGO LA-5521P
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				Rev	0.1

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# CRT CONNECTOR



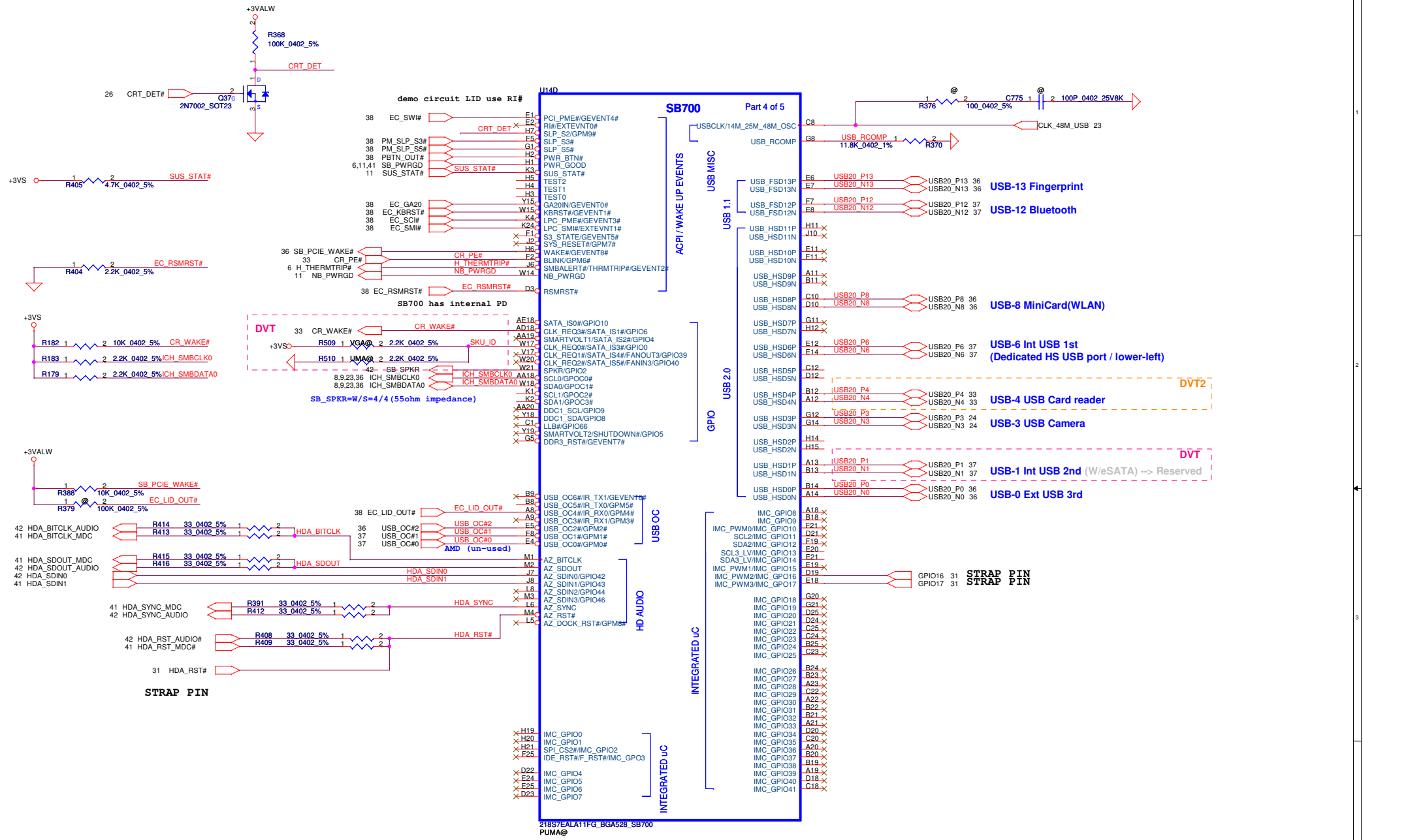
Security Classification	Compal Secret Data			Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	CRT Connector	
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				Date: Thursday, June 04, 2009	Sheet 26 of 58



Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	SB710-PCI/PCI/ACPI/LPC/RTC
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Size	Document Number	NBLG0 LA-5521P		Rev
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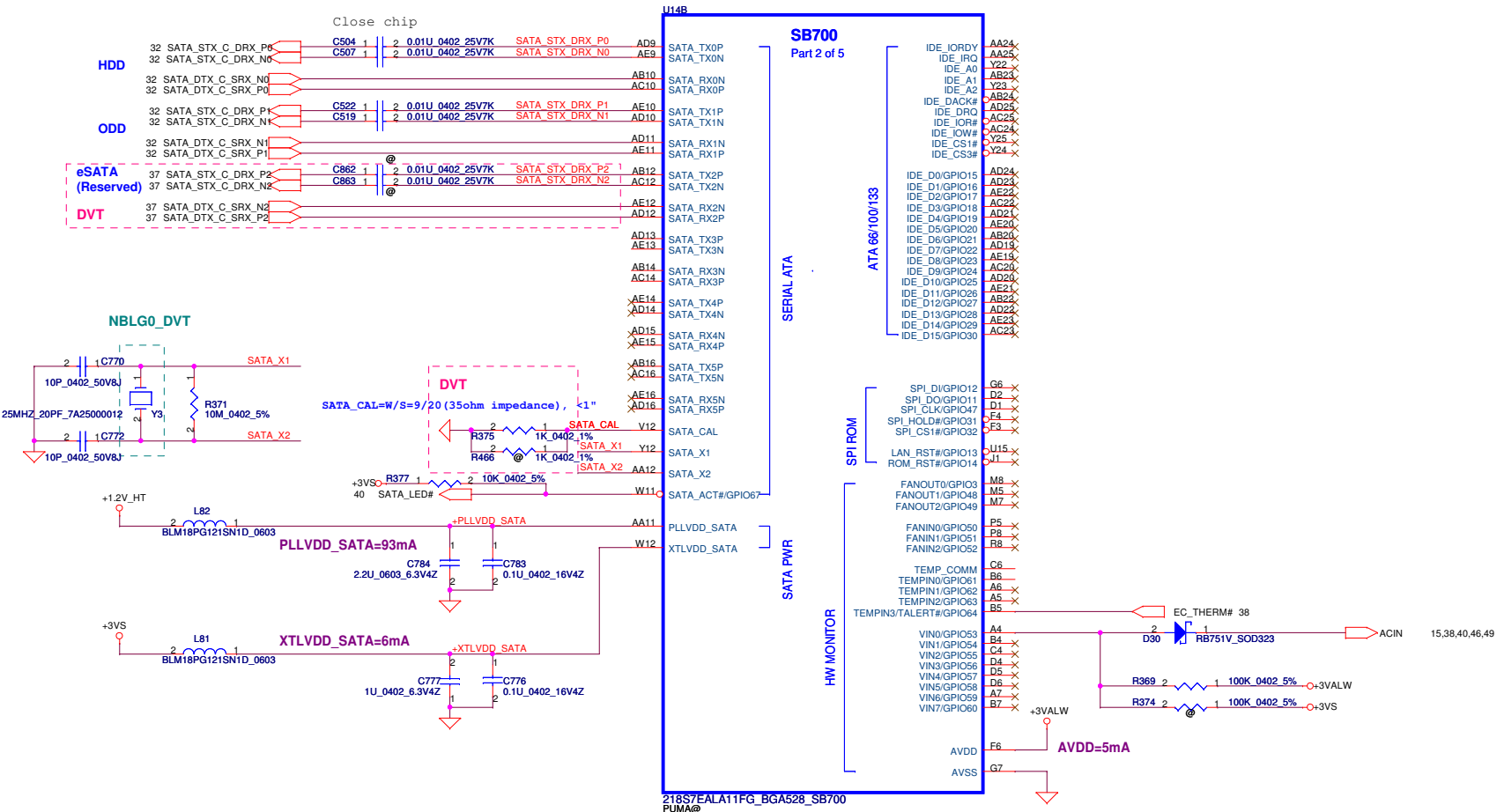
level shift to ISL6265

SA000015570 S IC 218S7EBLA12FG SB700 BGA 528P SB 0FA  
 SA000030740 S IC 218-0660017 A14 SB710 FCBGA HF 0FA

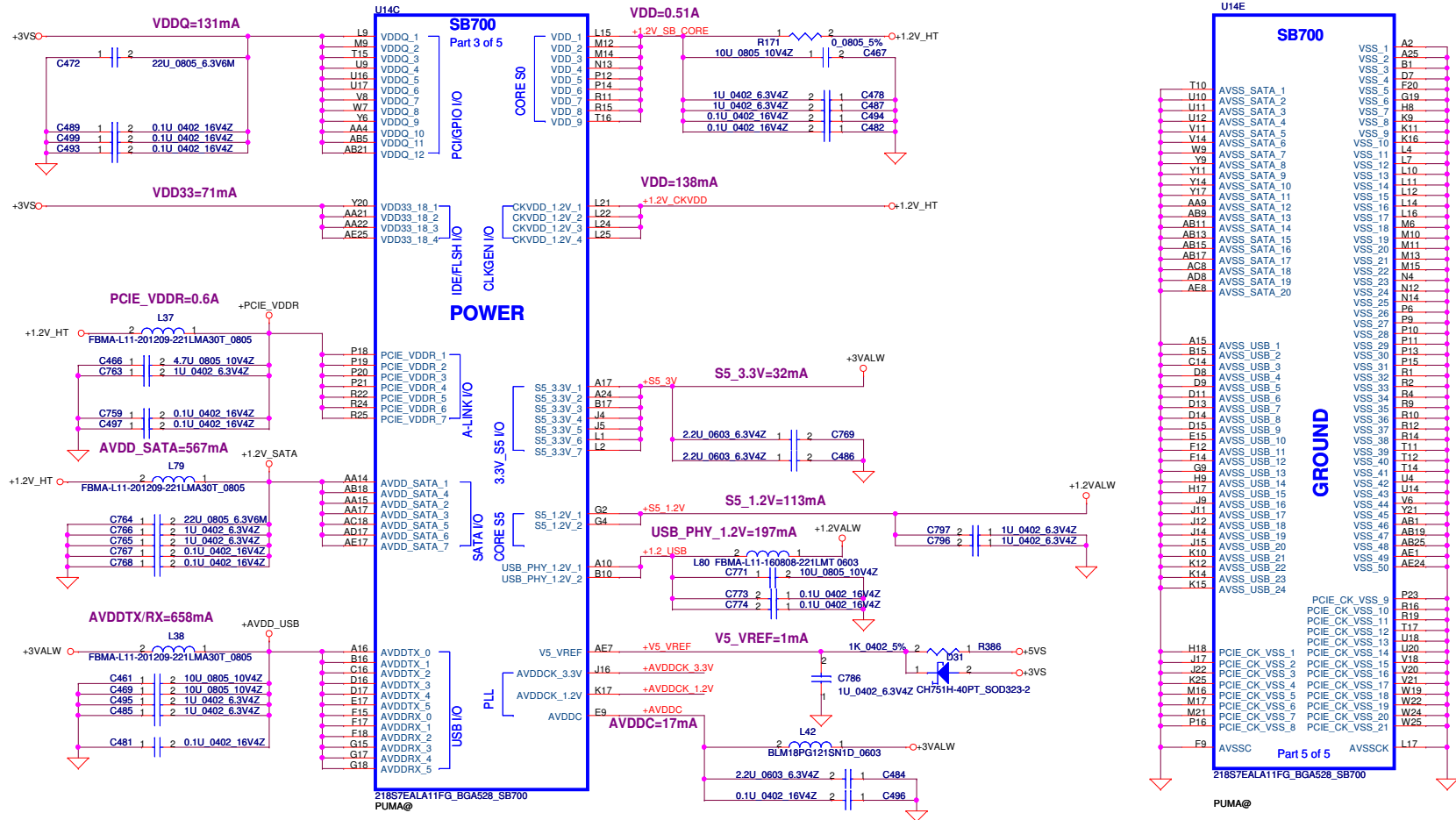


218S7EAL11FG\_BGA528\_SB700  
PUMA

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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				SB710 USB/HD audio	
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Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller



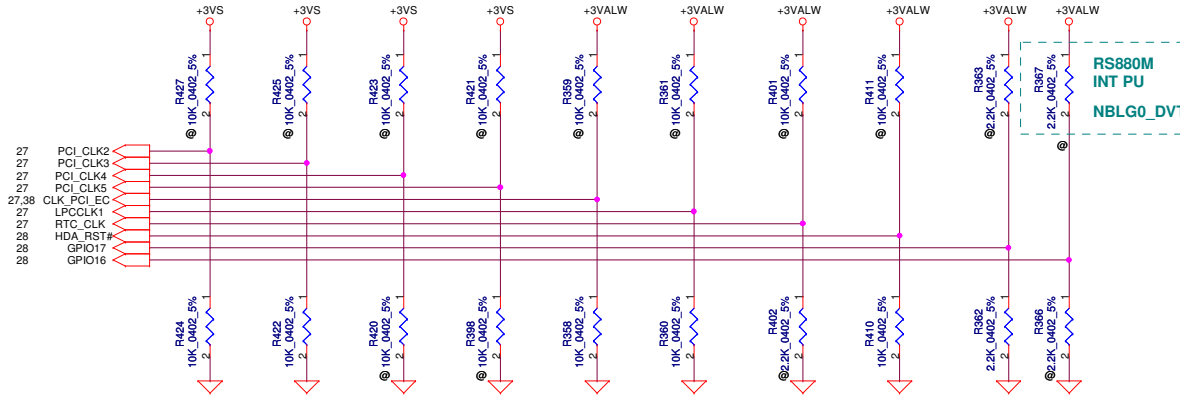
Security Classification	Compal Secret Data	
Issued Date	2008/10/06	Deciphered Date 2009/10/06
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Compal Electronics, Inc.		
Title <b>SB710 power/GND</b>		
Size	Document Number	Rev
Custom	<b>NBLG0 LA-5521P</b>	0.1
Date:	Sunday, April 12, 2009	E   Sheet 30 of 58

# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

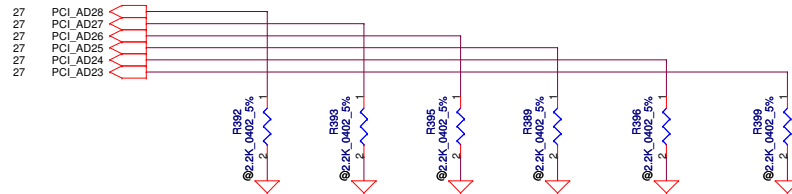
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	<b>INTERNAL RTC</b>  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) LL = FWH ROM	

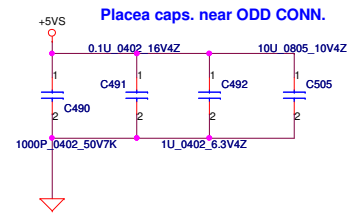
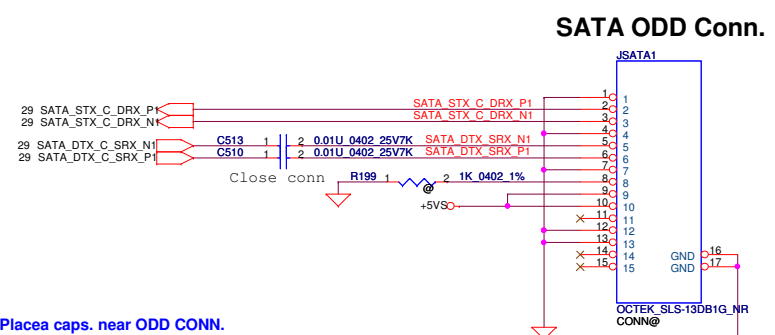


# DEBUG STRAPS

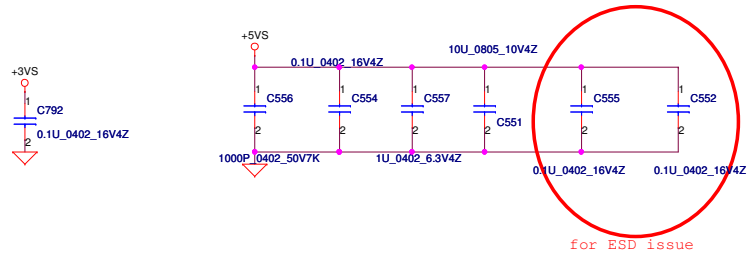
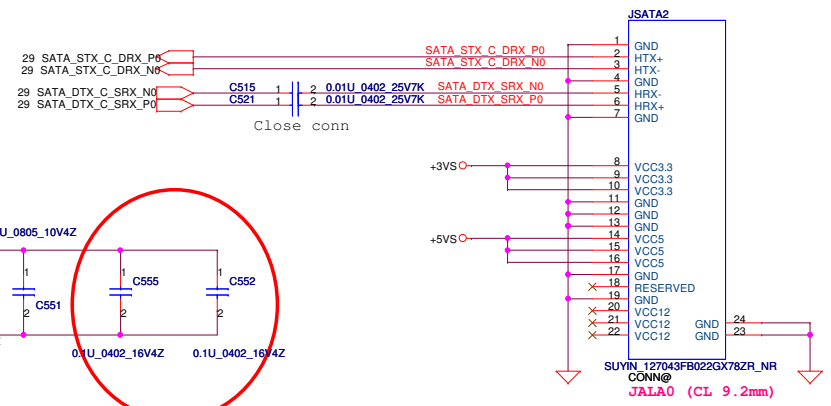
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	





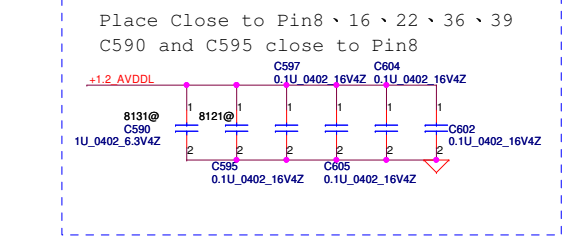
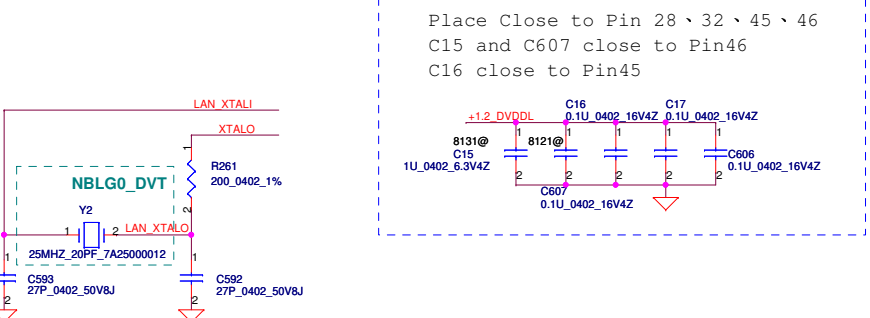
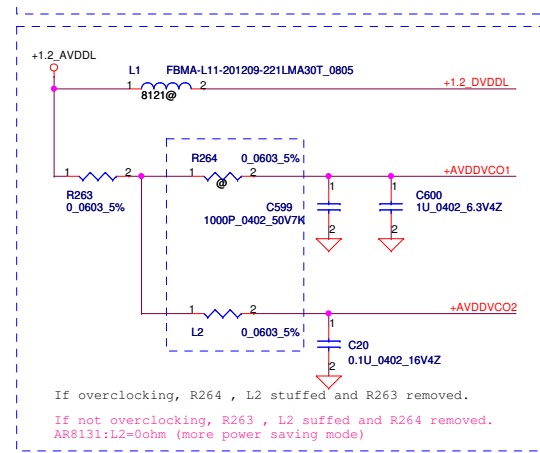
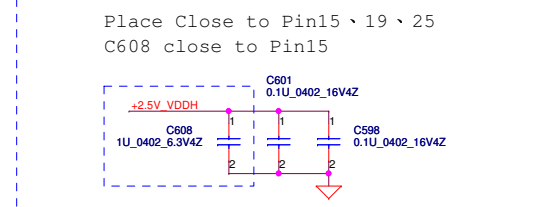
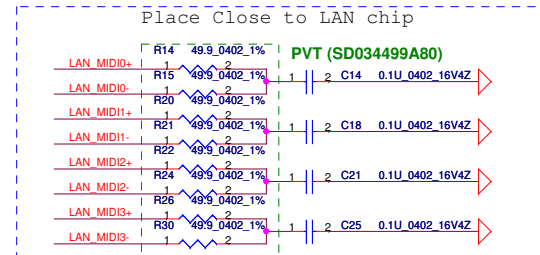
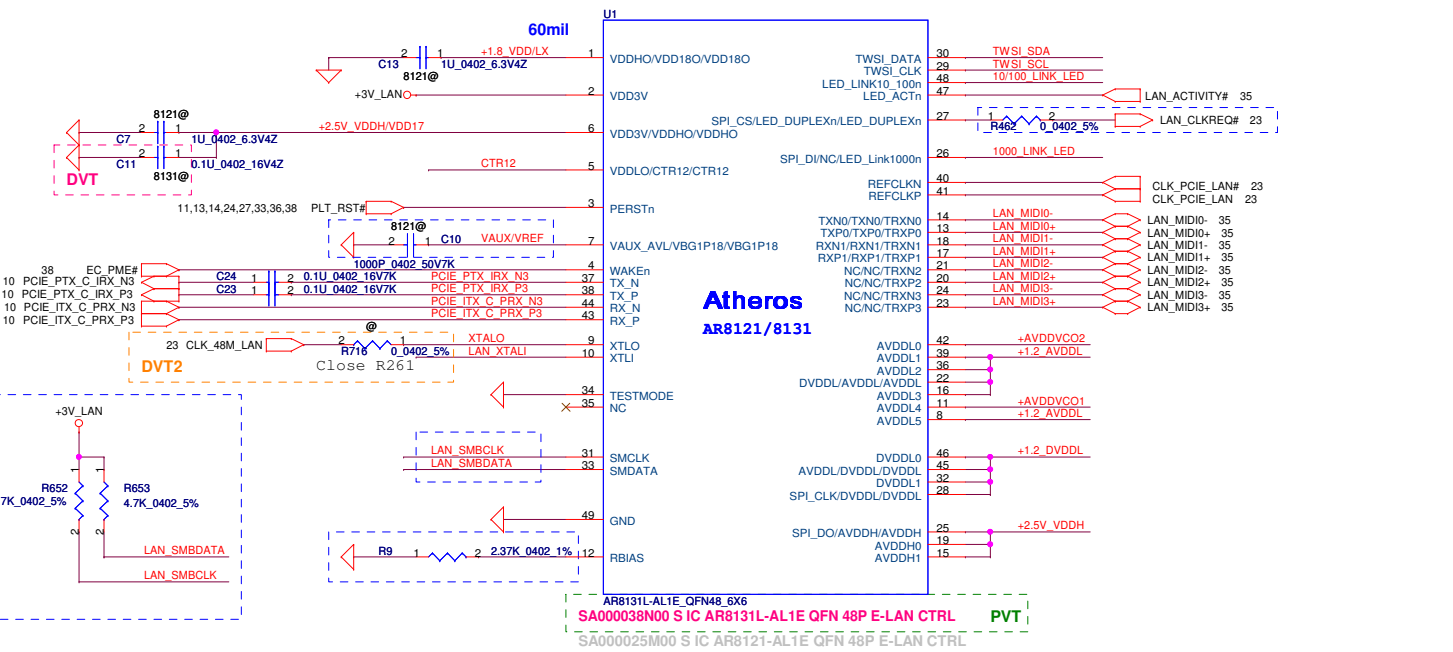
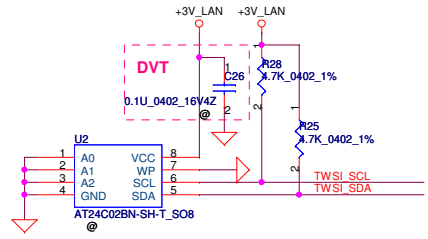
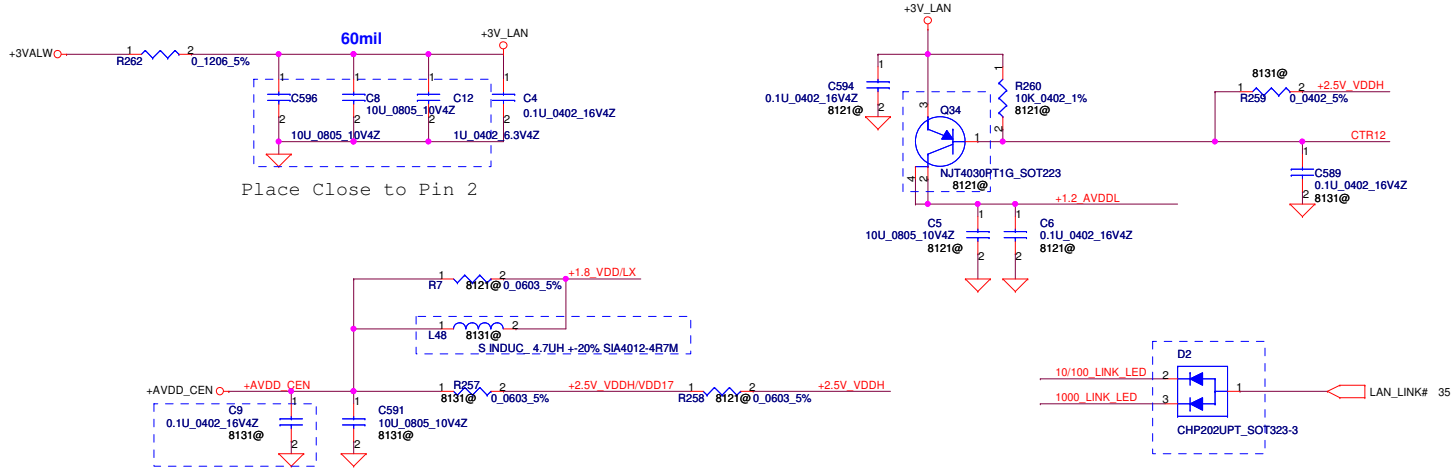
### SATA HDD Conn.



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Size B	Document Number	NBLG0 LA-5521P		Rev	0.1
Date:	Thursday, June 04, 2009	Sheet	32	of	58







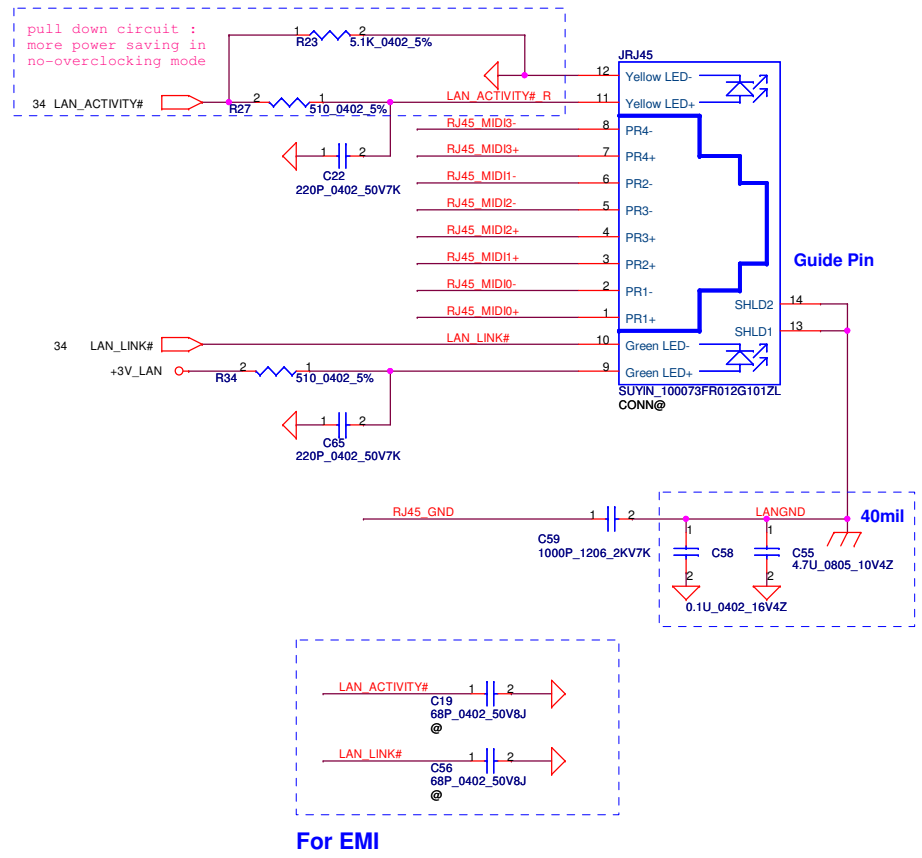
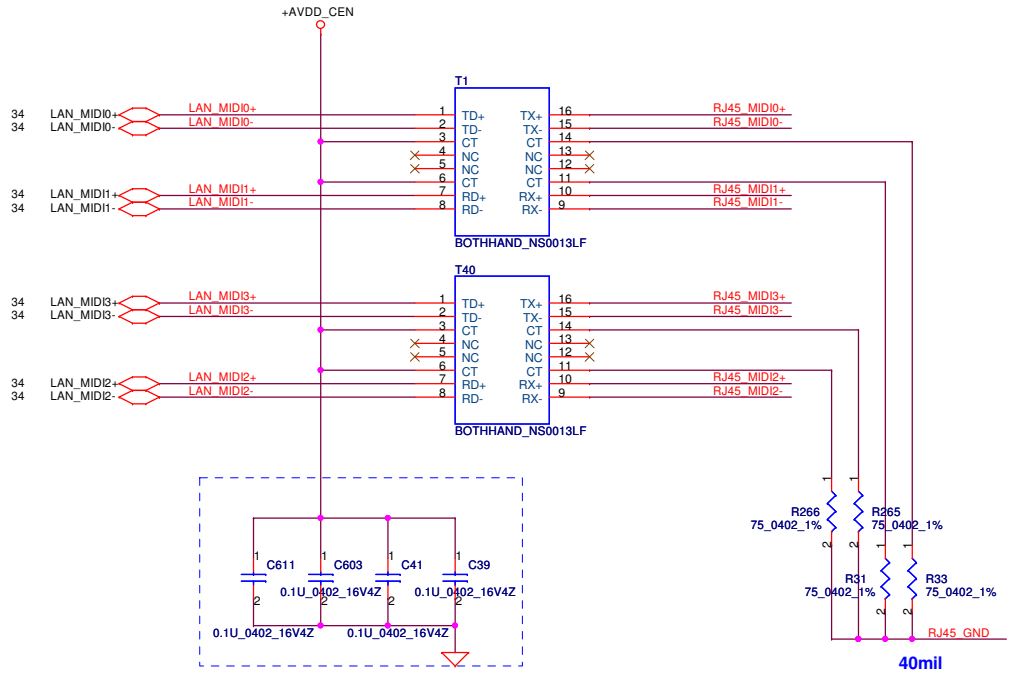
If overclocking, R264, L2 stuffed and R263 removed.  
 If not overclocking, R263, L2 stuffed and R264 removed.  
 AR8131:L2=0ohm (more power saving mode)

**Atheros**  
AR8121/8131

AR8131L-AL1E\_QFN48\_6X6  
 SA000038N00 S IC AR8131L-AL1E\_QFN 48P E-LAN CTRL PVT  
 SA000025M00 S IC AR8121T-AL1E\_QFN 48P E-LAN CTRL

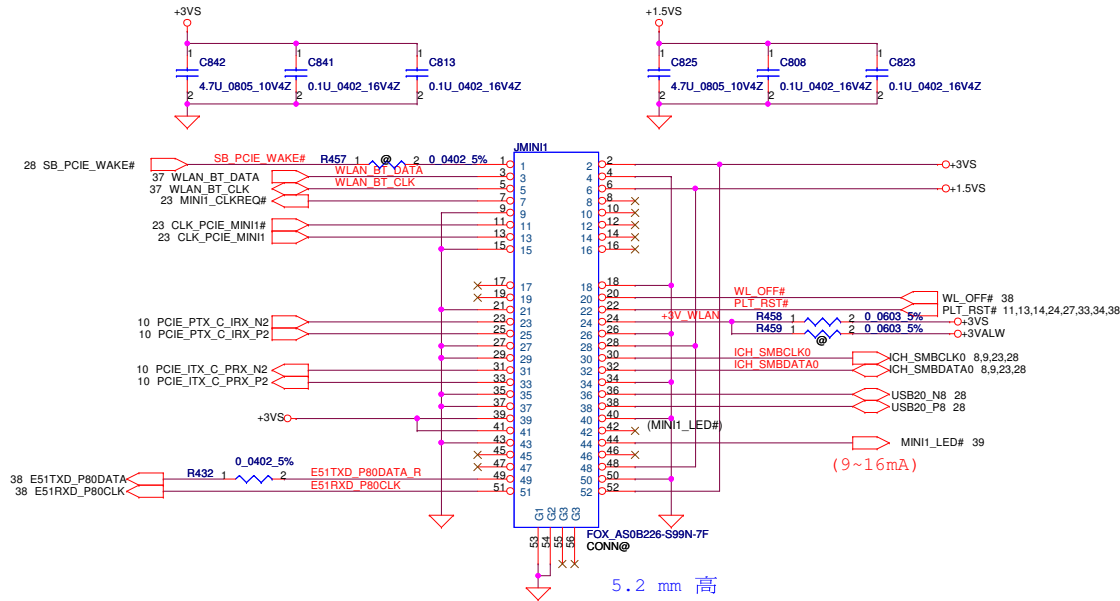
Security Classification		Compal Secret Data	
Issued Date	2008/04/16	Deciphered Date	2009/04/16
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Compal Electronics, Inc.			
Title <b>Atheros AR8131</b>			
Size	Document Number	Rev	
Custom	<b>NBLG0 LA-5521P</b>	0.1	
Date:	Thursday, June 04, 2009	Sheet	34 of 58



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Size B	Document Number	NBLG0 LA-5521P		Rev	0.1
Date:	Thursday, June 04, 2009	Sheet	35	of	58

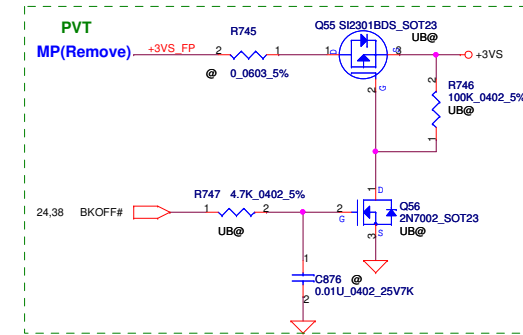
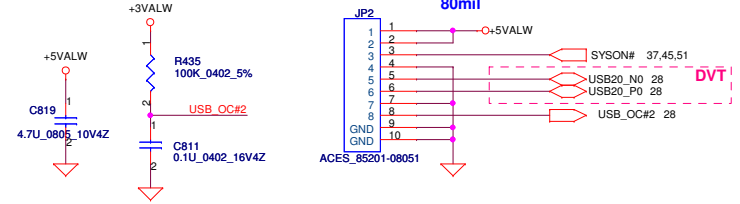
### For Wireless LAN



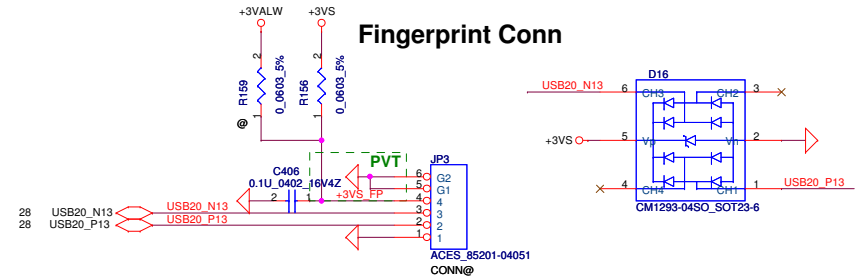
5.2 mm 高

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

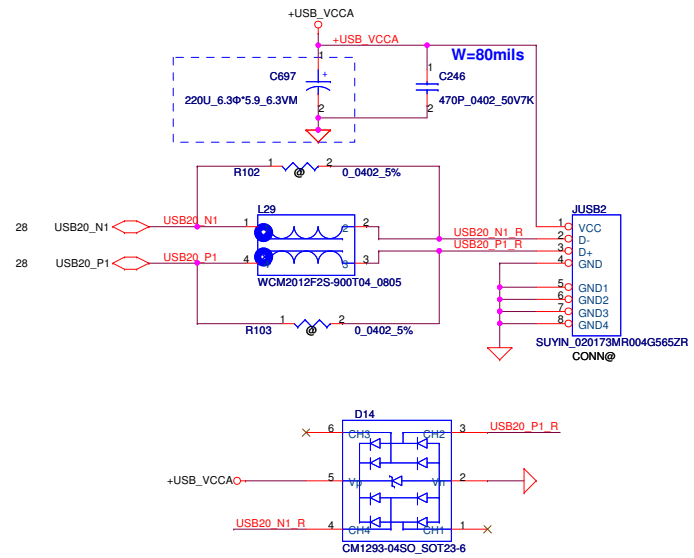
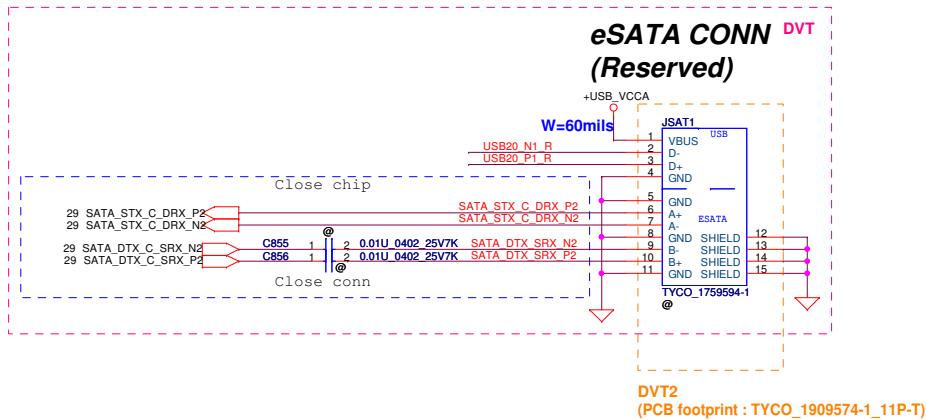
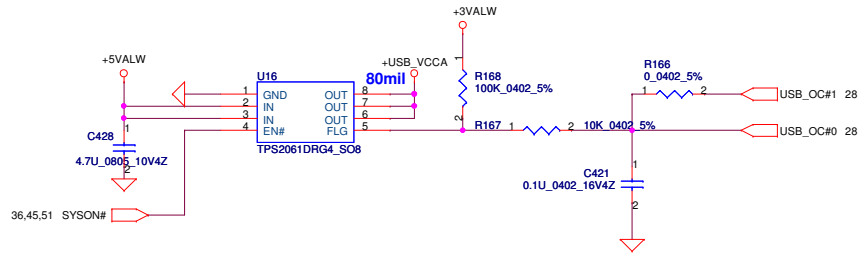
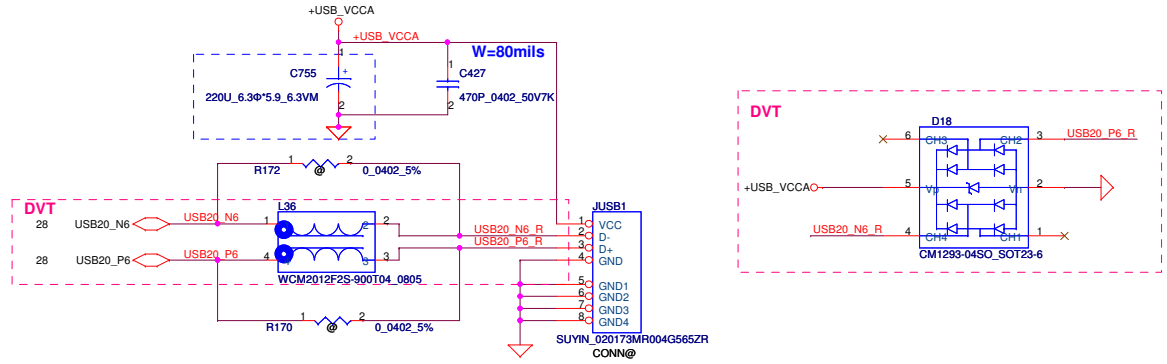
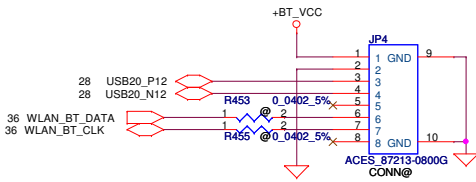
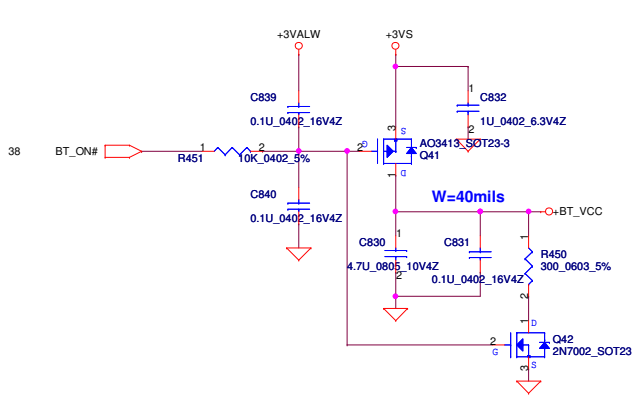
### To USB/B Connector



### Fingerprint Conn



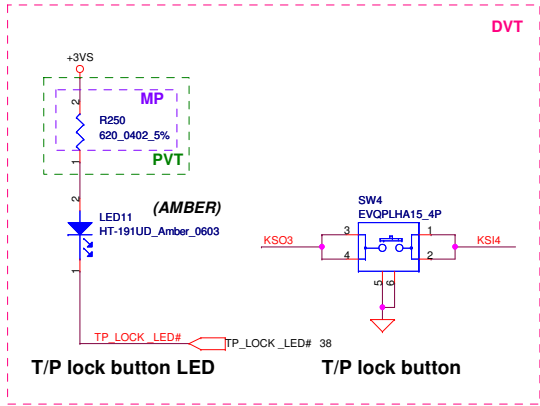
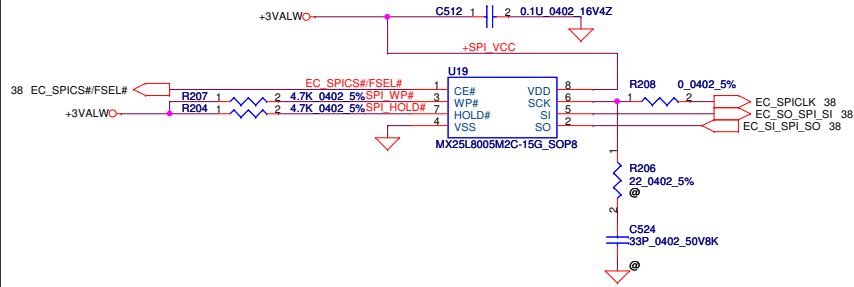
# Bluetooth Conn.



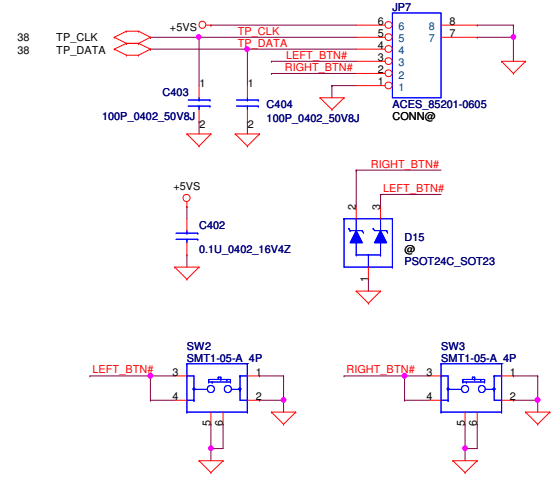
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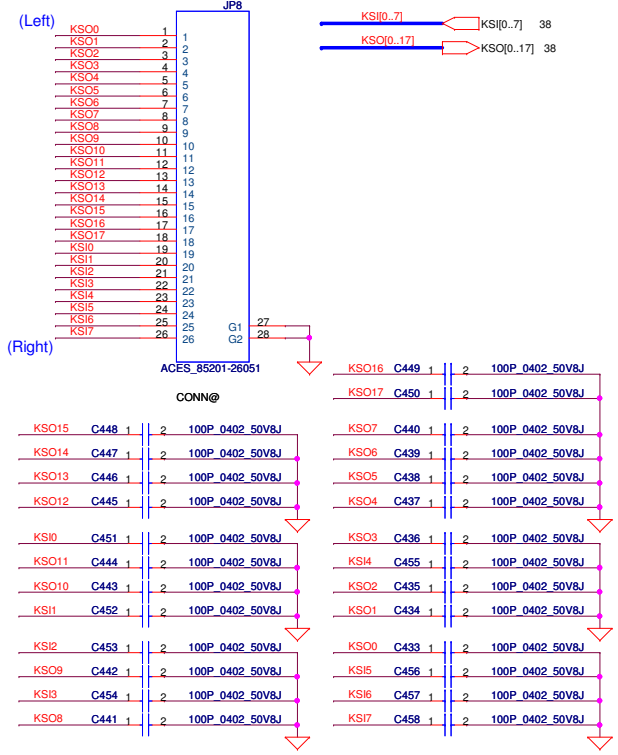
# BIOS(SYS / EC / VGA)



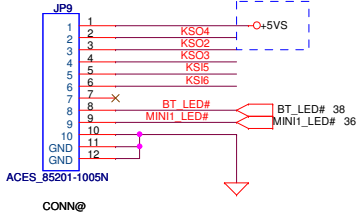
## To TP/B Conn.



## INT\_KBD Conn.

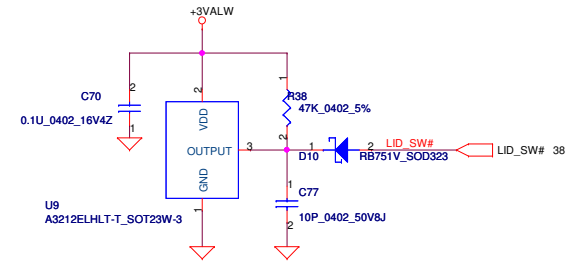


## To FUN/B Conn (10PIN)

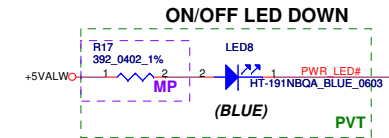
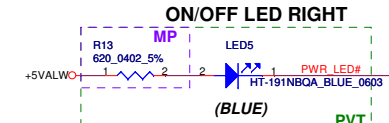
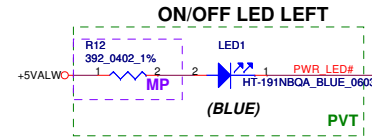
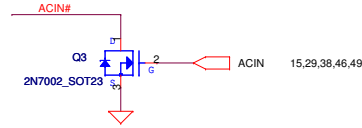
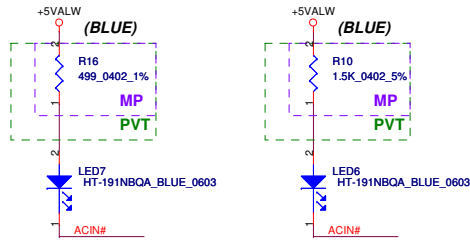


	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

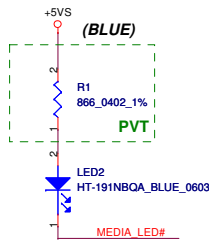
## Lid Switch (Hall Effect Switch)



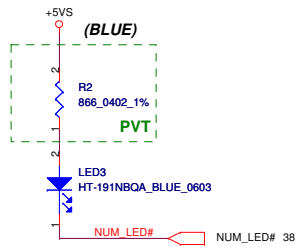
### Enlightener LED



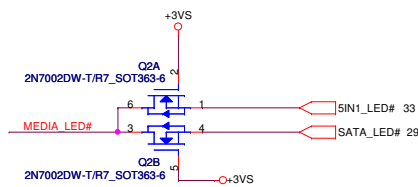
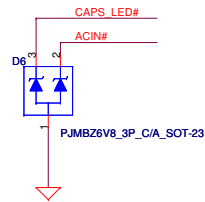
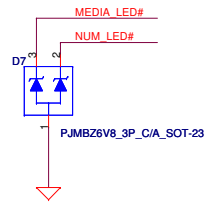
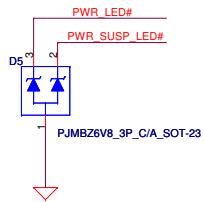
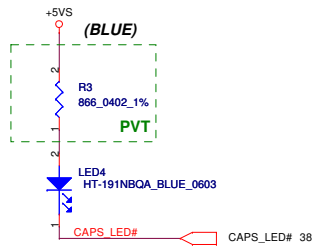
### MEDIA\_LED



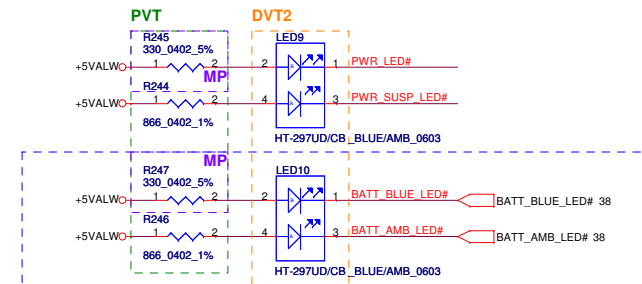
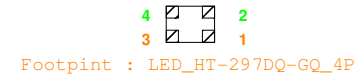
### NUM\_LED



### CAPS\_LED



### Compal Footprint



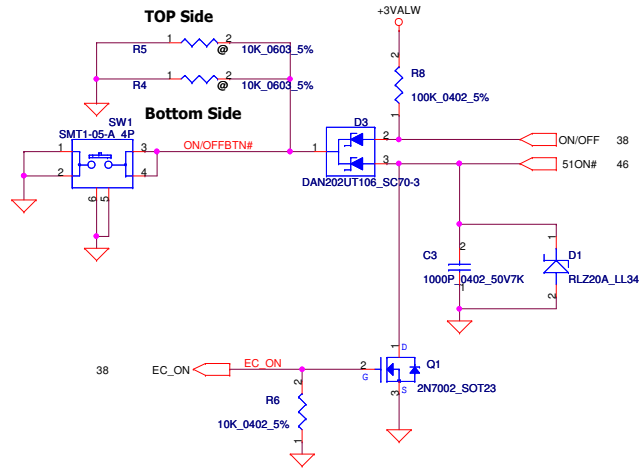
### BLUE/AMBER

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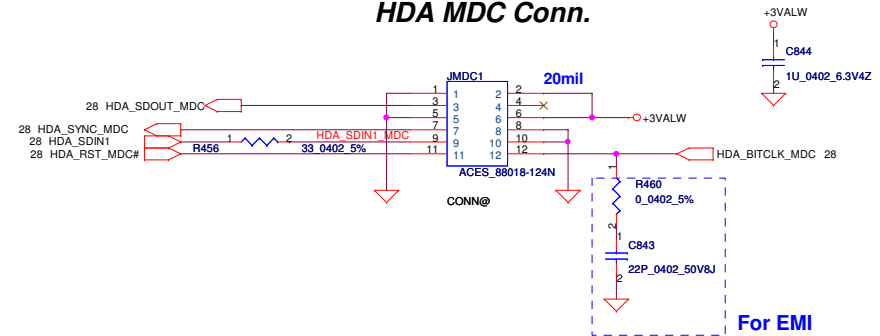


# Power Button

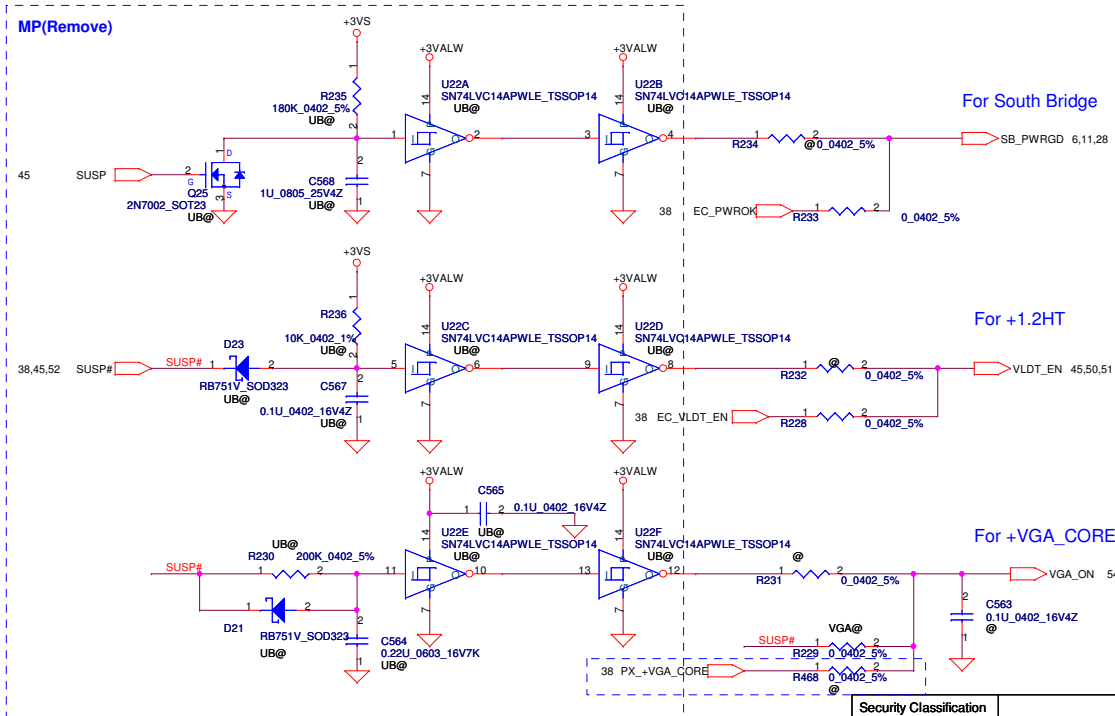
ON/OFF switch



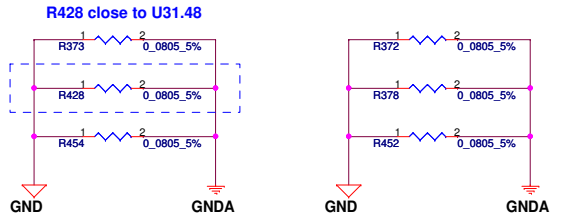
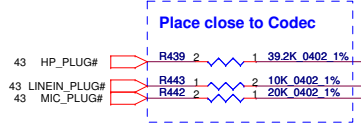
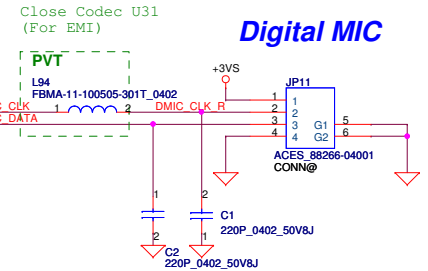
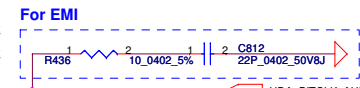
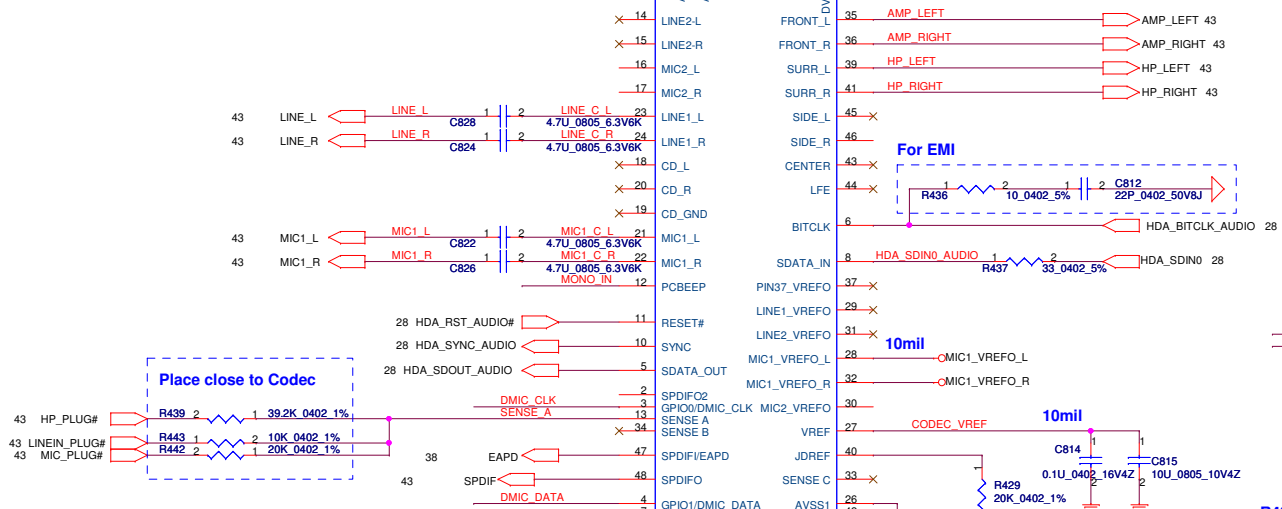
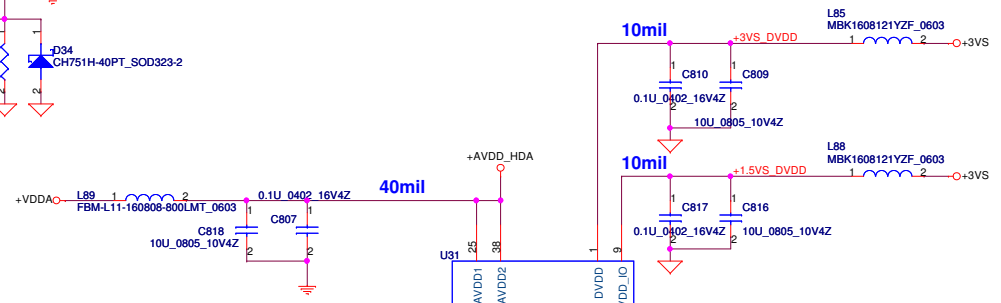
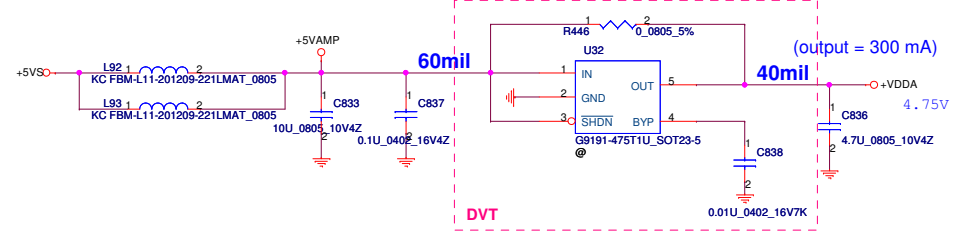
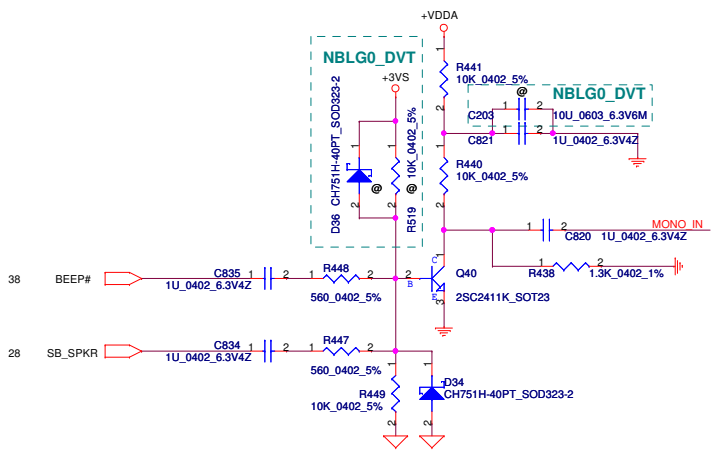
# HDA MDC Conn.



# Power ON Circuit



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Size B	Document Number	Date		Rev	0.1
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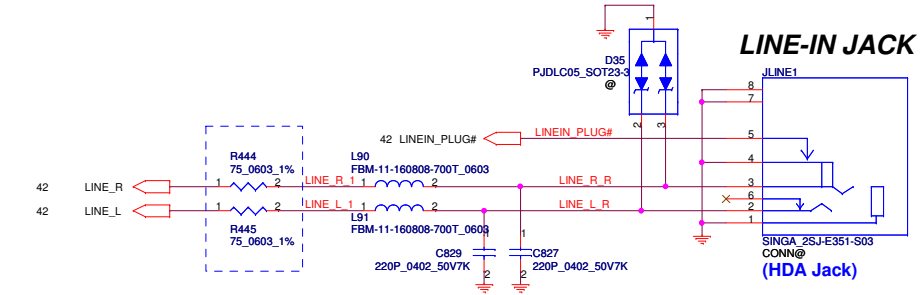
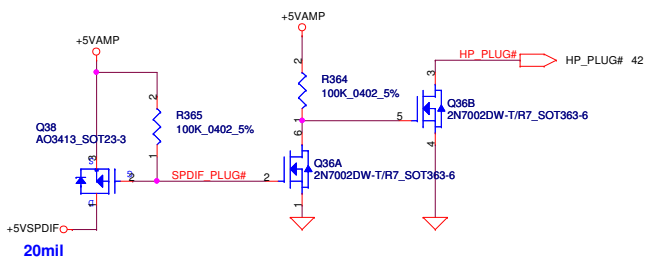
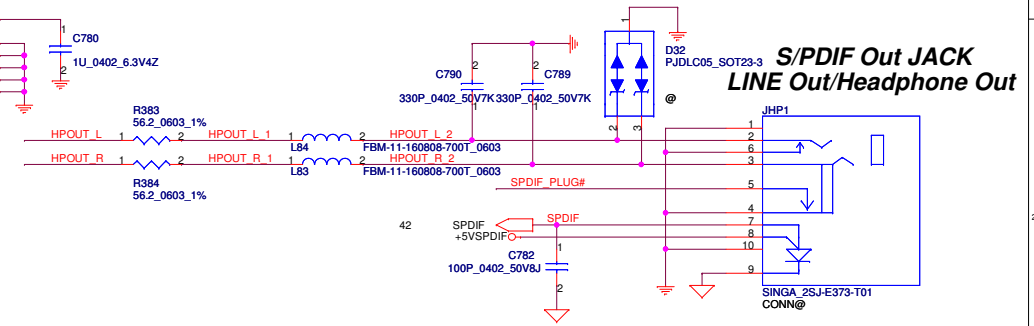
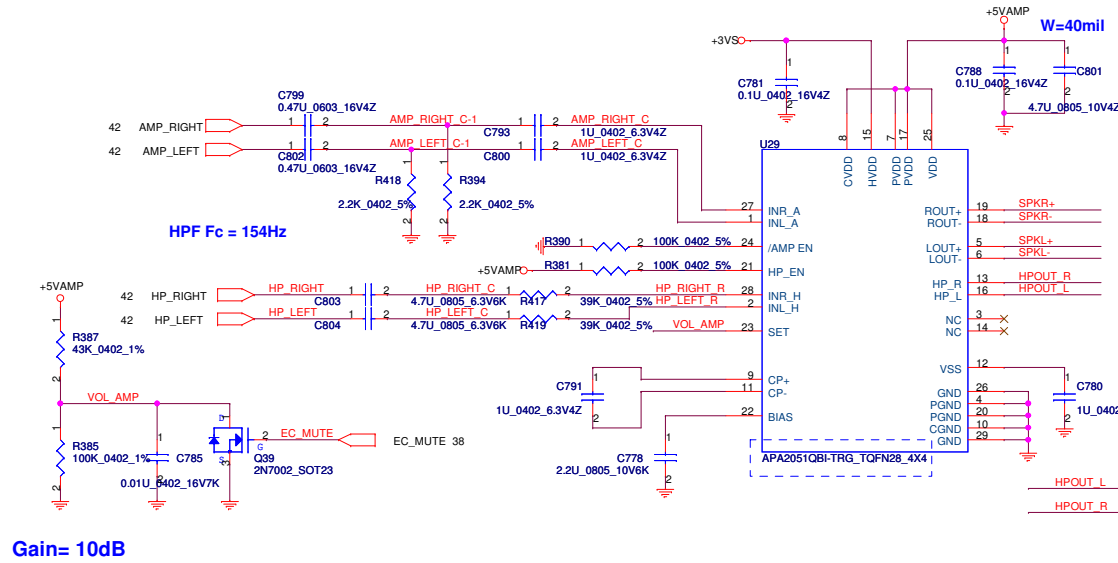


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

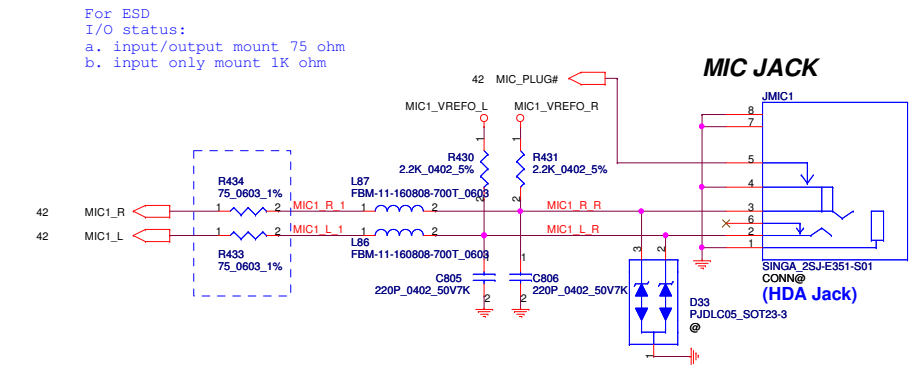
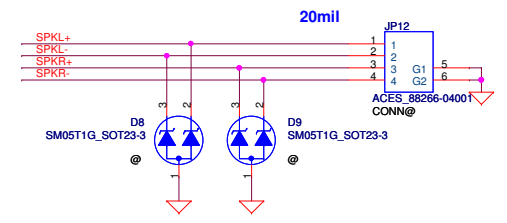
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Compal Electronics, Inc.		
Title		
HD Audio Codec ALC888S-VC		
Size	Document Number	Rev
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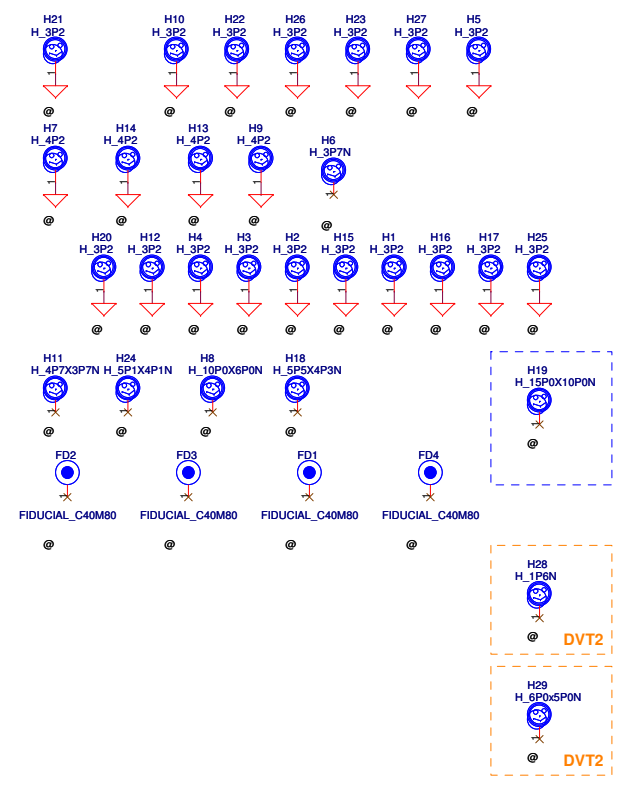
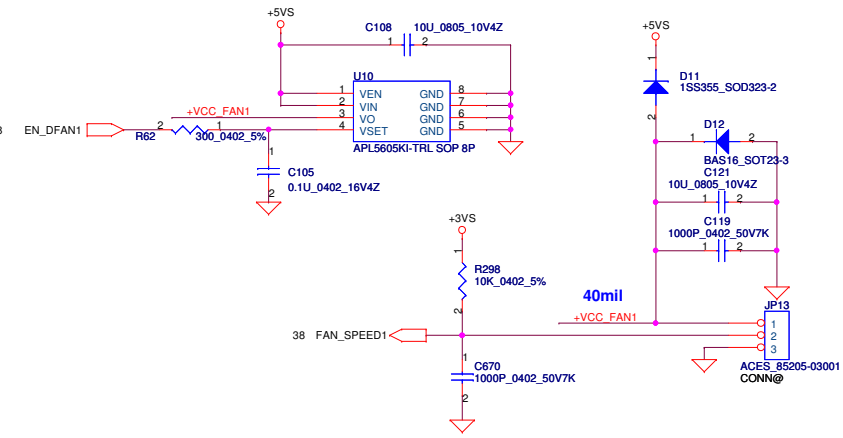
**Int. Speaker Conn.**



For ESD I/O status:  
 a. input/output mount 75 ohm  
 b. input only mount 1K ohm

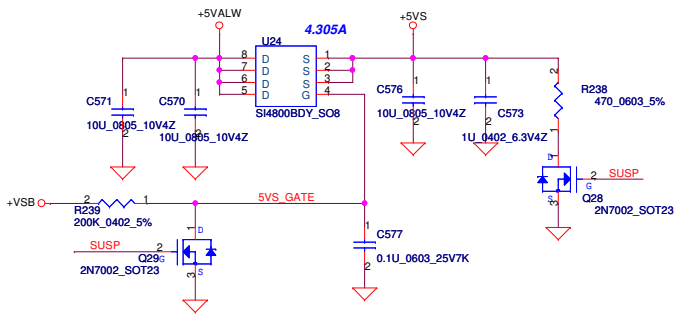
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Amplifier & Audio Jack
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### FAN1 Conn

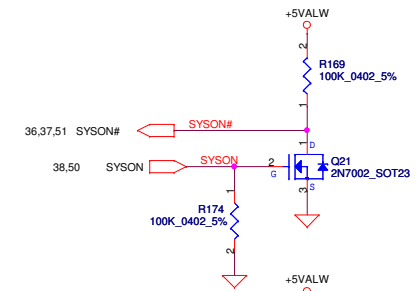
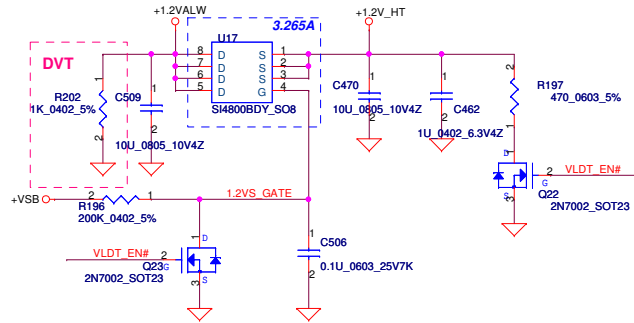


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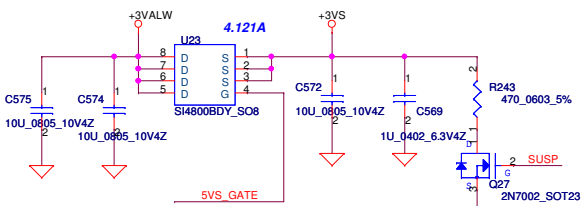
**+5VALW TO +5VS**



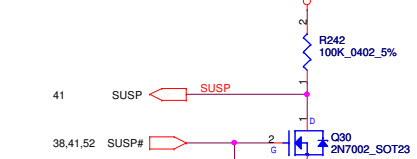
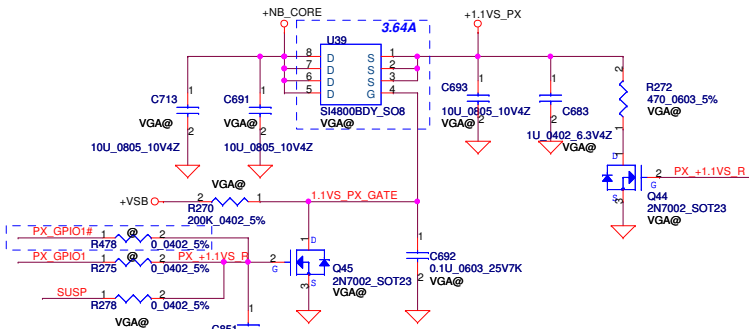
**+1.2VALW TO +1.2V\_HT**



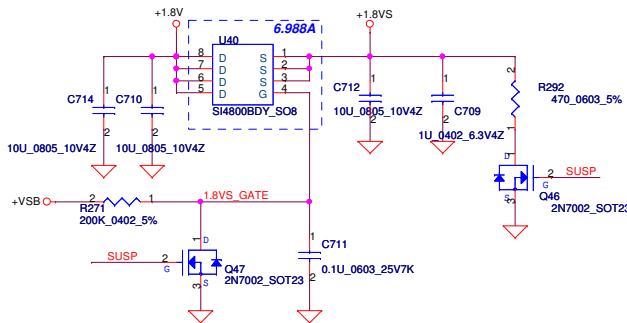
**+3VALW TO +3VS**



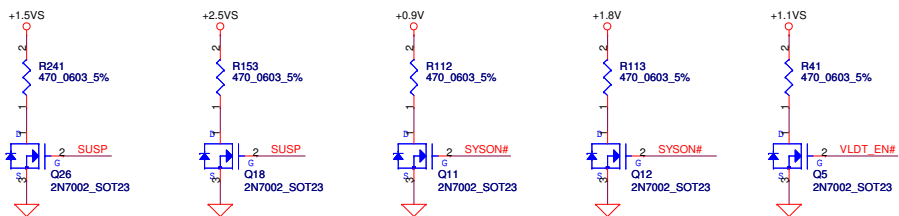
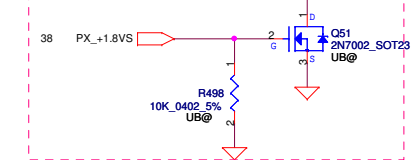
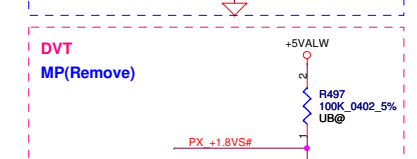
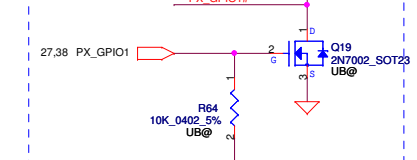
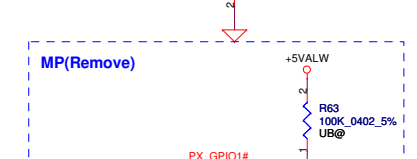
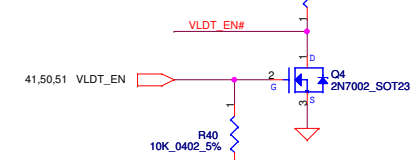
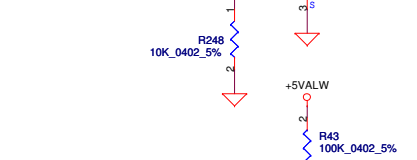
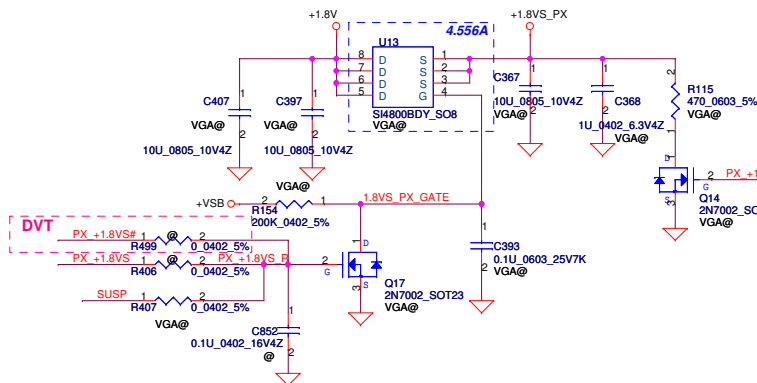
**+NB\_CORE TO +1.1VS\_PX**



**+1.8V to +1.8VS**



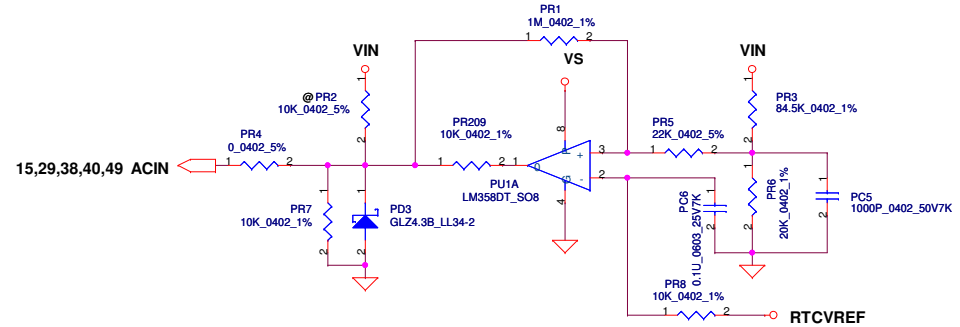
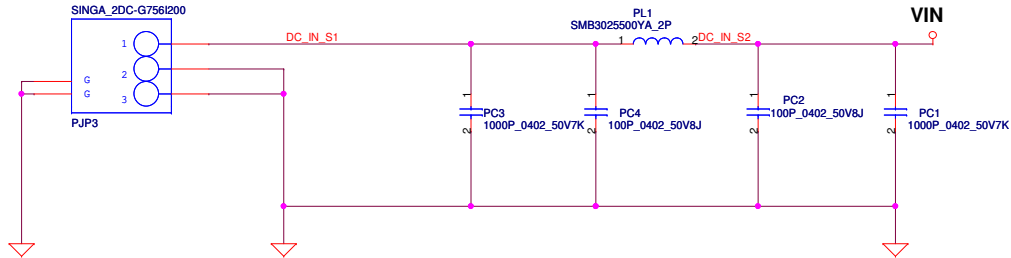
**+1.8V to +1.8VS\_PX**



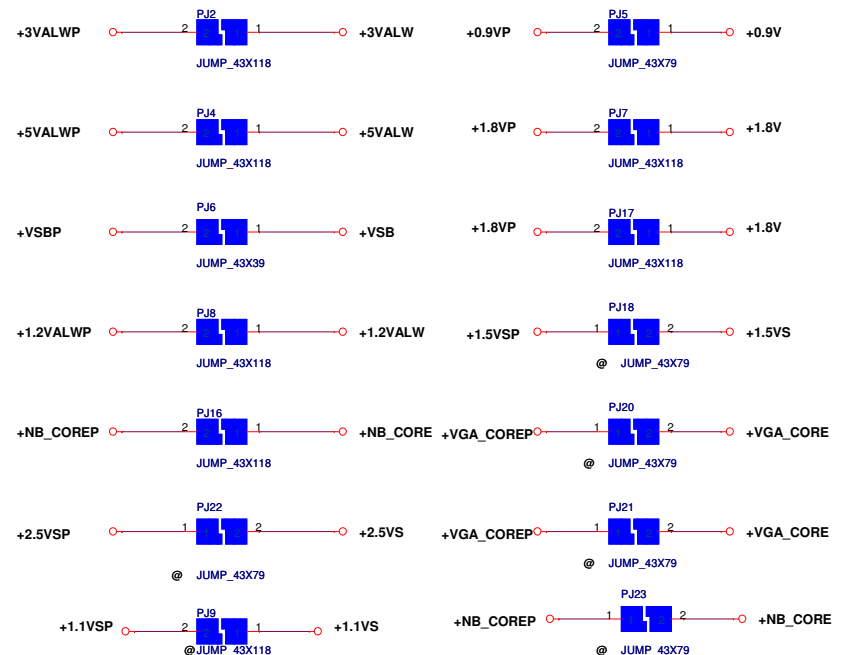
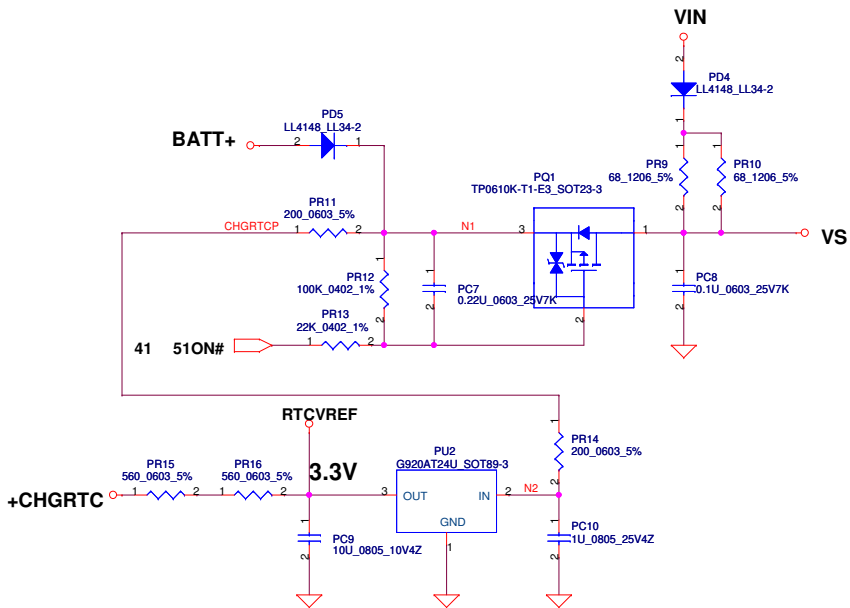
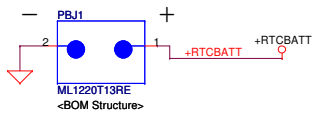
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	DC Interface	
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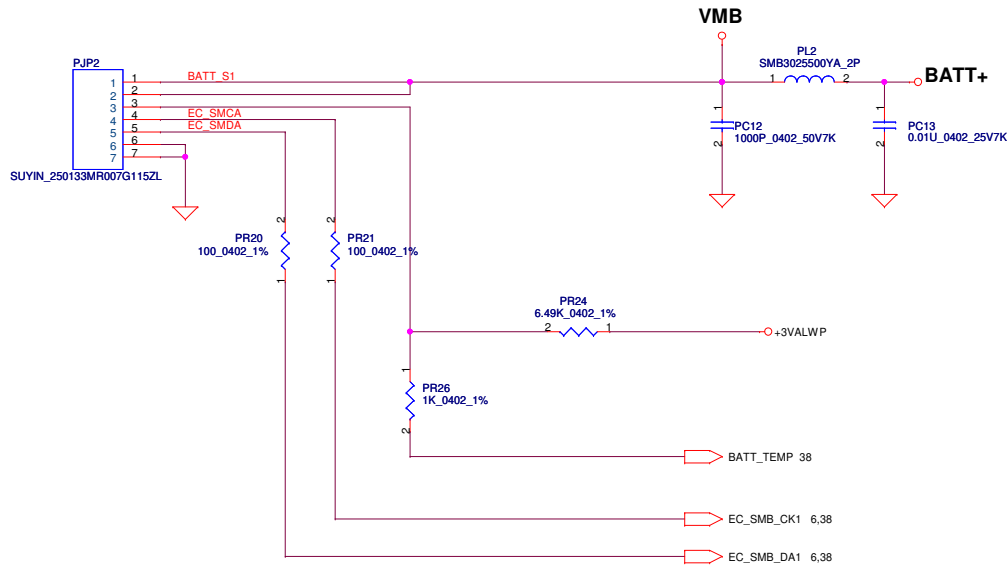
**DC231000500**

<BOM Structure>  
SINGA\_2DC-G756I200

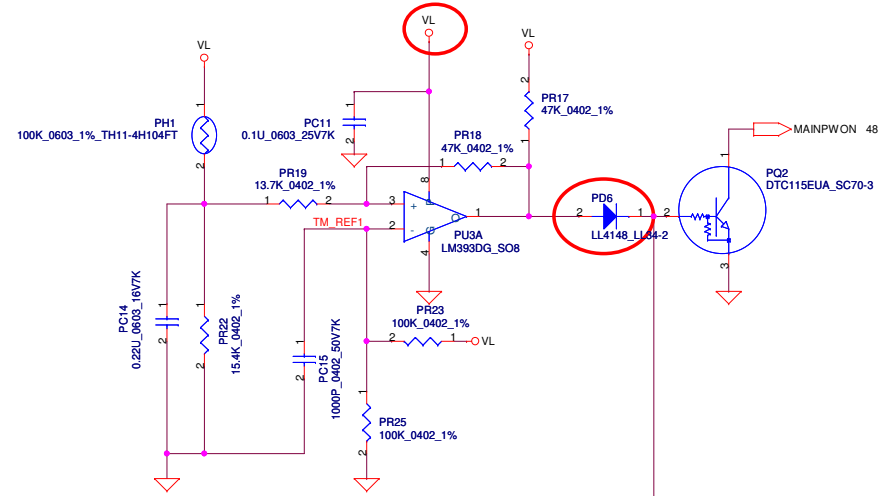


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

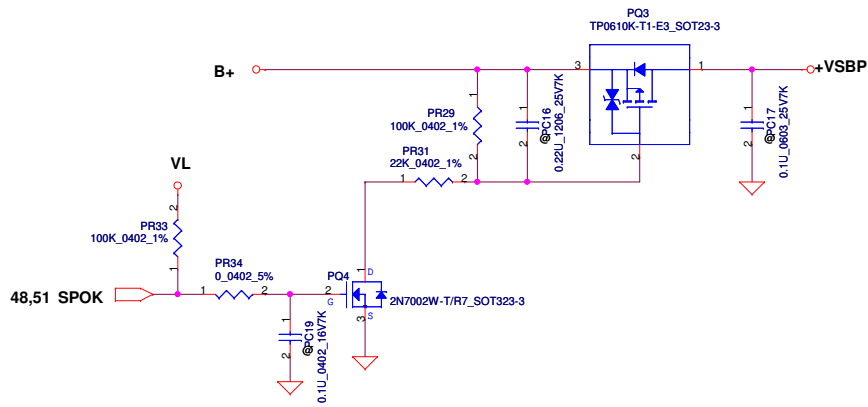
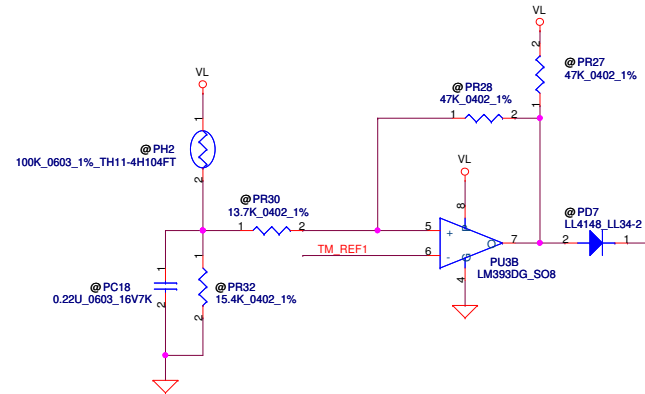




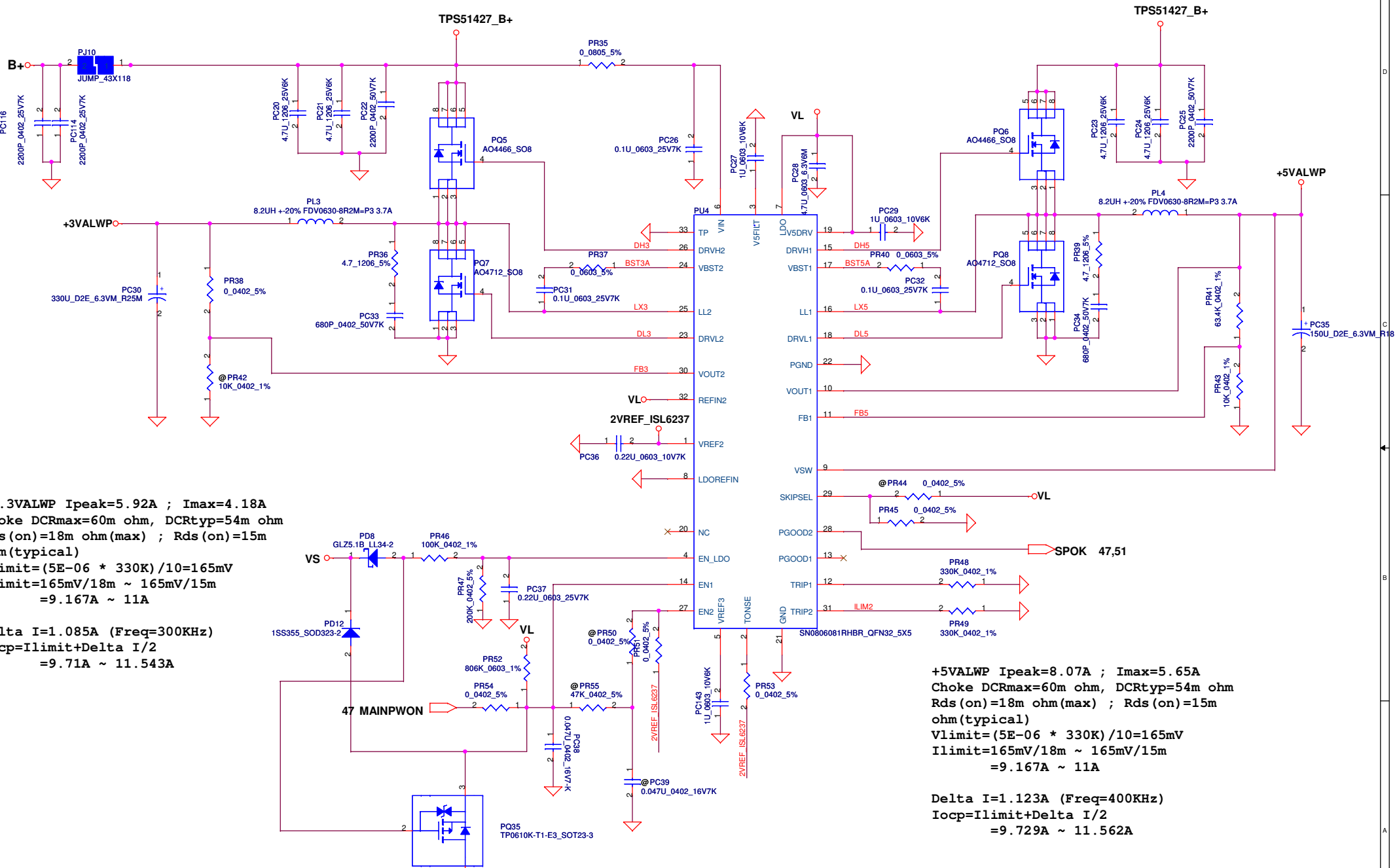
PH1 under CPU botten side :  
 CPU thermal protection at 93 degree C  
 Recovery at 57 degree C



PH2 near Battery CONN :  
 BAT. thermal protection at 79 degree C  
 Recovery at 47 degree C



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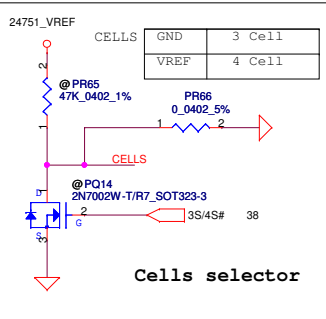
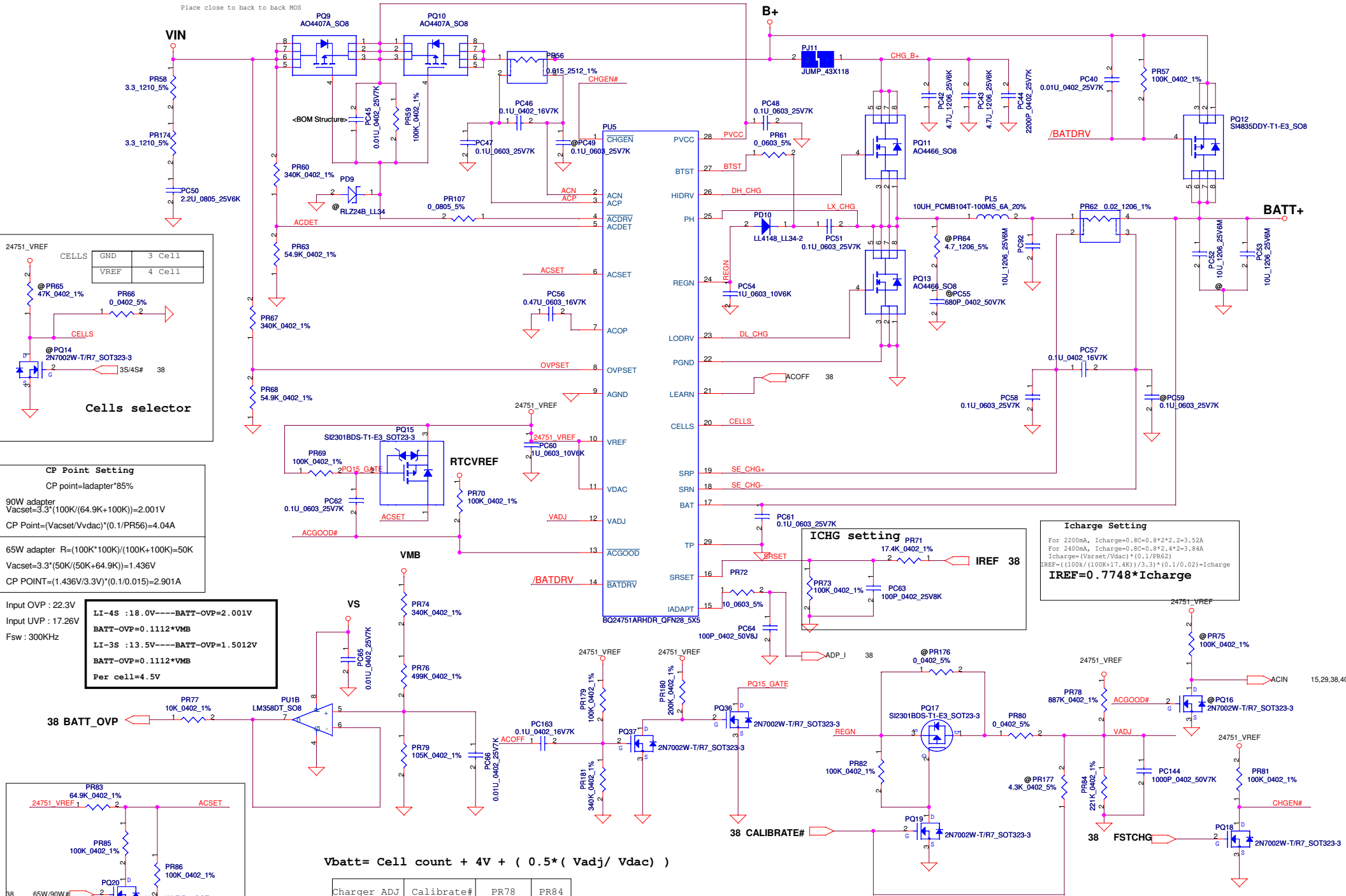
**+3.3VALWP** Ipeak=5.92A ; I<sub>max</sub>=4.18A  
 Choke DCR<sub>max</sub>=60m ohm, DCR<sub>typ</sub>=54m ohm  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>limit</sub>=(5E-06 \* 330K)/10=165mV  
 I<sub>limit</sub>=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
  
 Delta I=1.085A (Freq=300KHz)  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =9.71A ~ 11.543A

**+5VALWP** Ipeak=8.07A ; I<sub>max</sub>=5.65A  
 Choke DCR<sub>max</sub>=60m ohm, DCR<sub>typ</sub>=54m ohm  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>limit</sub>=(5E-06 \* 330K)/10=165mV  
 I<sub>limit</sub>=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
  
 Delta I=1.123A (Freq=400KHz)  
 I<sub>ocp</sub>=I<sub>limit</sub>+Delta I/2  
 =9.729A ~ 11.562A

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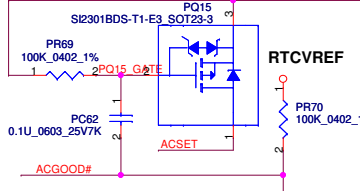
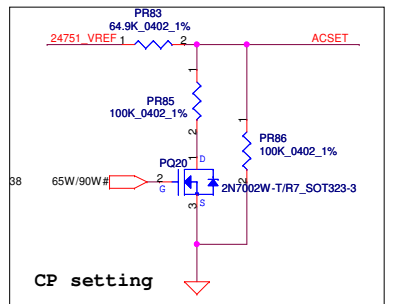
Place close to back to back MOS



**CP Point Setting**  
 CP point=ladapler\*85%  
 90W adapter  
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$   
 $CP\ Point = (V_{acset} / V_{dacc}) \cdot (0.1 / PR56) = 4.04A$   
 65W adapter  $R = (100K \cdot 100K) / (100K + 100K) = 50K$   
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$   
 $CP\ POINT = (1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$

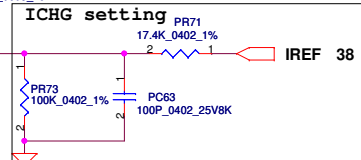
Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz

LI-4S : 18.0V ---- BATT-OVP=2.001V  
 BATT-OVP=0.1112 \* VMB  
 LI-3S : 13.5V ---- BATT-OVP=1.5012V  
 BATT-OVP=0.1112 \* VMB  
 Per cell=4.5V



$$V_{batt} = \text{Cell count} + 4V + (0.5 * (V_{adj} / V_{dacc}))$$

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V (1.32)	H	@	@

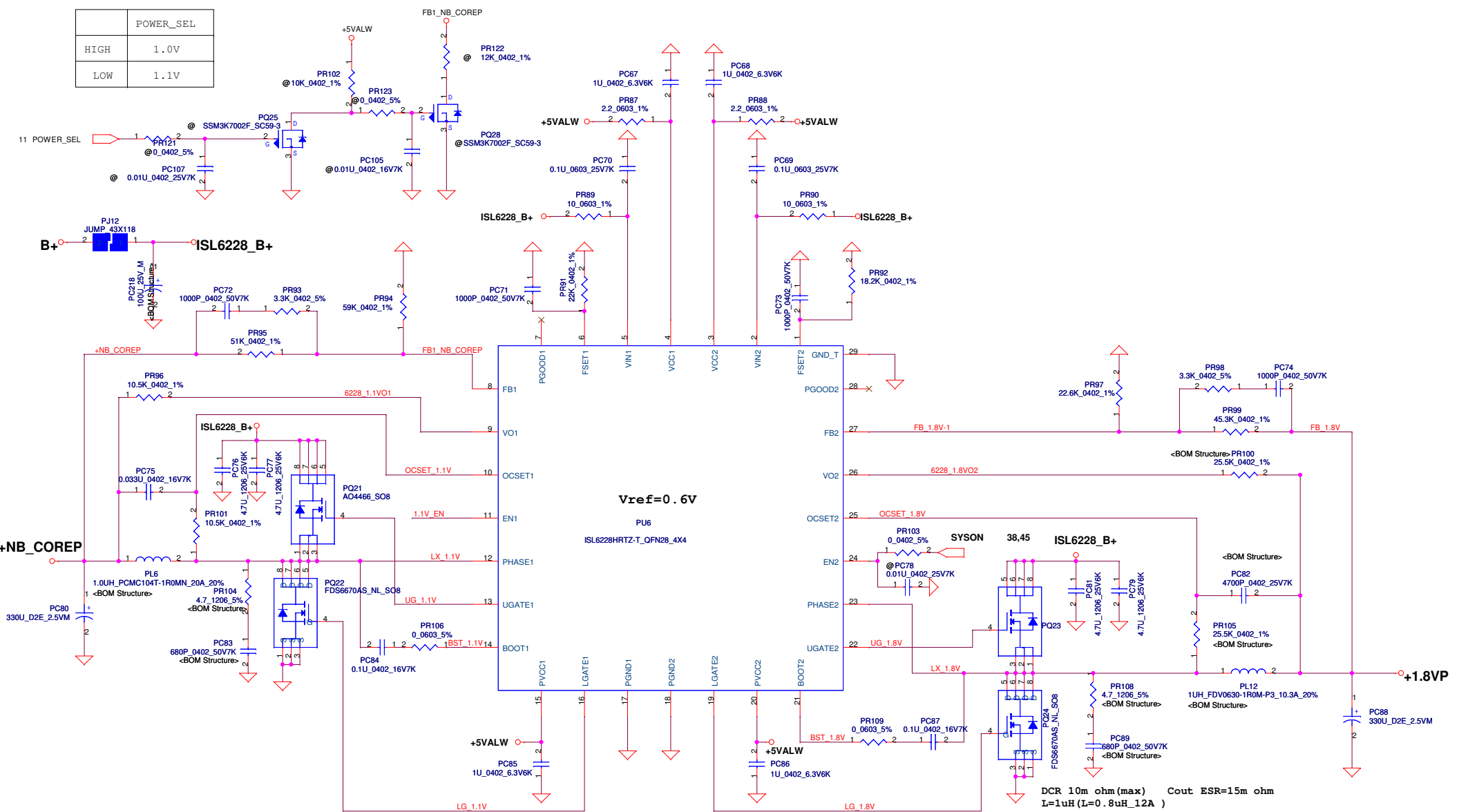


**Icharge Setting**  
 For 2200mA,  $I_{charge} = 0.8C = 0.8 * 2 * 2.2 = 3.52A$   
 For 2400mA,  $I_{charge} = 0.8C = 0.8 * 2.4 * 2 = 3.84A$   
 $I_{charge} = (V_{acset} / V_{dacc}) * (0.1 / PR62)$   
 $I_{REF} = (100K / (100K + 17.4K)) / 3.3 * (0.1 / 0.02) = I_{charge}$   
 **$I_{REF} = 0.7748 * I_{charge}$**

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Compal Electronics, Inc.			
<b>CHARGER</b>			
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	POWER_SEL
HIGH	1.0V
LOW	1.1V



DCR3.5m ohm(max) Cout ESR=15m ohm

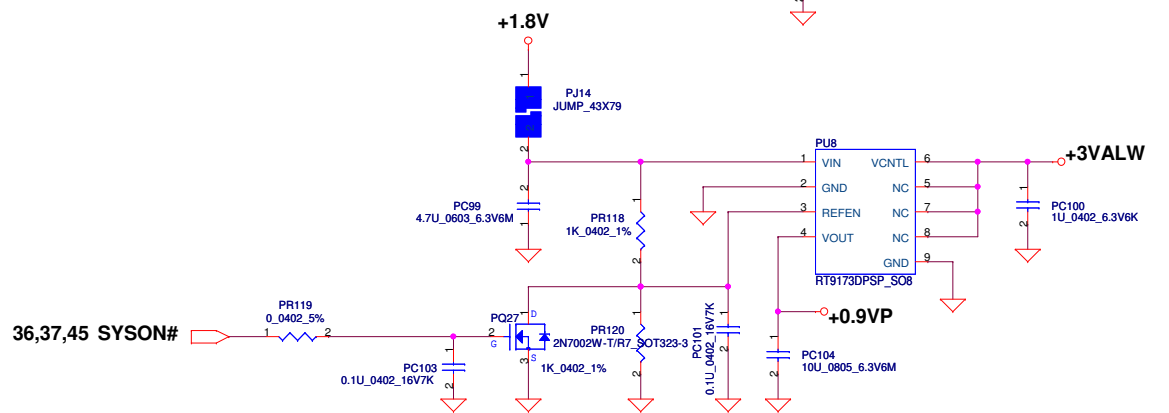
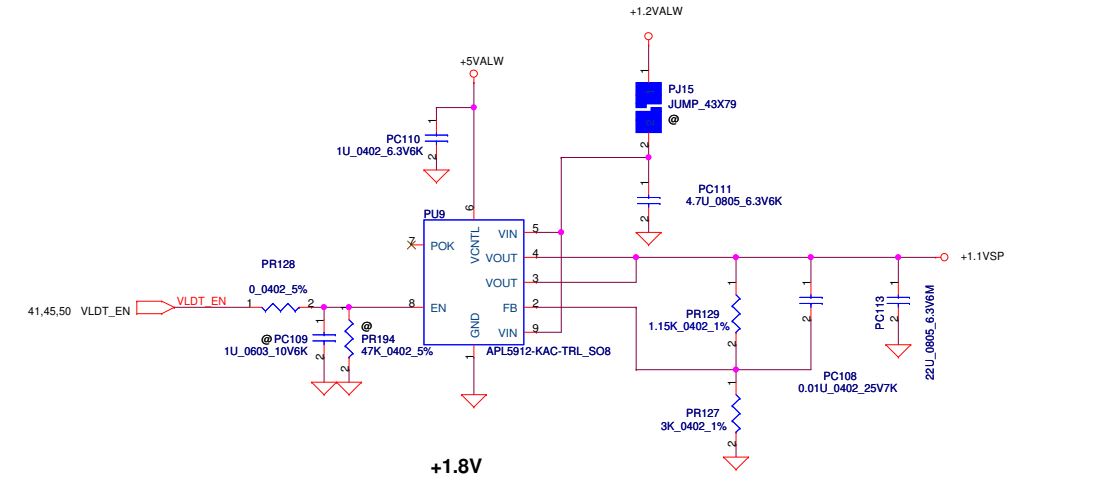
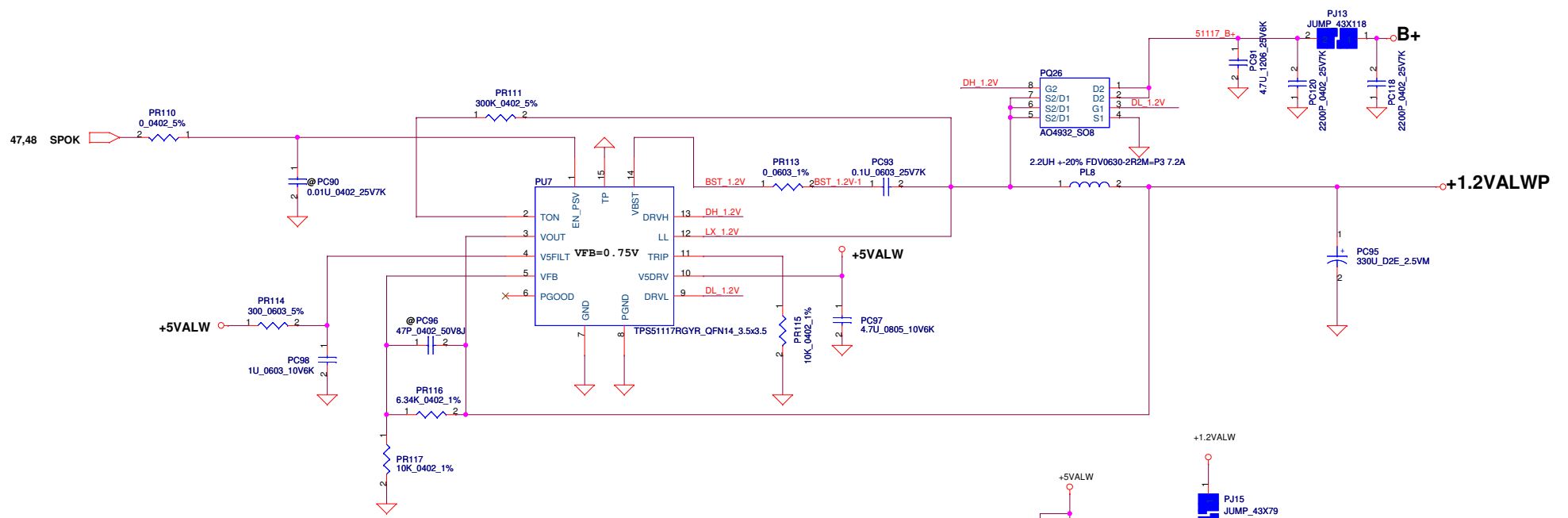
**NB\_CORE (1.1VSP) OCP Setting**  
 $Fsw=1/1.5E-10*22k=303K$   
 $Vo=Vref*((PR95+PR94)/PR94)$   
 $Ipeak=17.53A, Imax=12.27A$   
 $Iocp=17.53*1.2=21.04A$   
 $Delta I=3.838A$   
 $Iocp*DCR=(Rocset*9.5uA)=(21.04+1.92)*3.5m; Roset=8.44k$   
 now chose Roset=10.5K  
 $Csen=L/(DCR*Roset)=0.9uH/(3.5m*8.44k); Csen=0.031uF$   
 now chose Csen=0.033uF  
 $Iocp\_min=(10.5K*9.5uA)/(3.5m\ ohm*1.3)=21.92A$   
 $Iocp\_max=(10.5*10.5uA)/(3.5m\ ohm)=28.86A$

41,45,51 VLDI\_EN

DCR 10m ohm(max) Cout ESR=15m ohm  
L=1uH (L=0.8uH\_12A)

**1.8VP Ipeak=15.51A, Imax=10.86A**  
 $Fsw=1/1.5E-10*18.2k=366K$   
 $Vo=Vref*((PR97+PR99)/PR97)$   
 $Ipeak=15.51A, Imax=10.86A$   
 $Iocp=15.51*1.2=18.61A$   
 $Delta I=5.565A$   
 $Iocp*DCR=(Rocset*9.5uA)=(18.61+2.7825)*10m; Roset=22.5K$   
 now chose Roset=25.5K  
 $Csen=L/(DCR*Roset)=0.8uH/(10m*22.5k); Csen=3.56nF$   
 now chose Csen=3300pF  
 $Iocp\_min=(25.5K*9.5uA)/(10m\ ohm*1.3)=18.63A$   
 $Iocp\_max=(25.5*10.5uA)/(10m\ ohm)=26.78A$

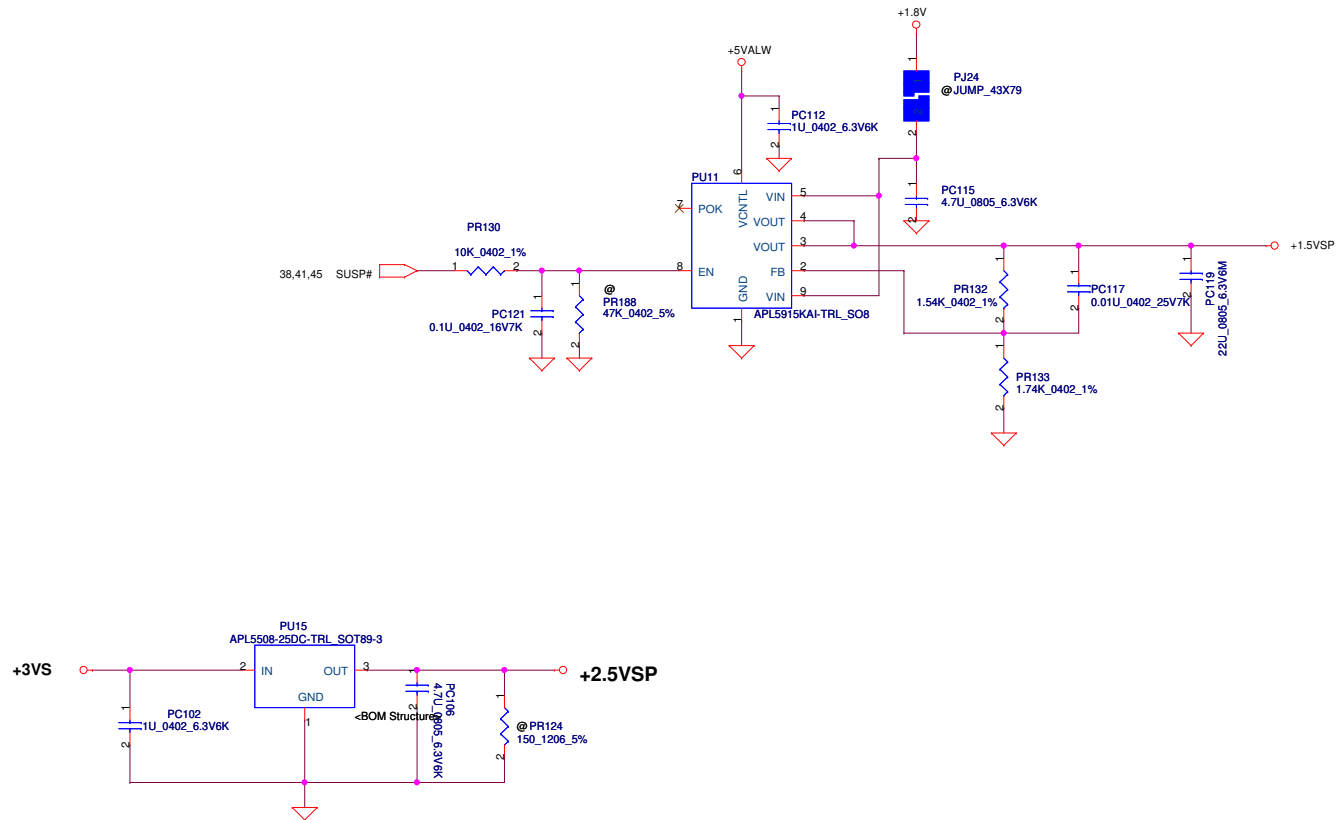
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	1.8VP / 1.1VSP
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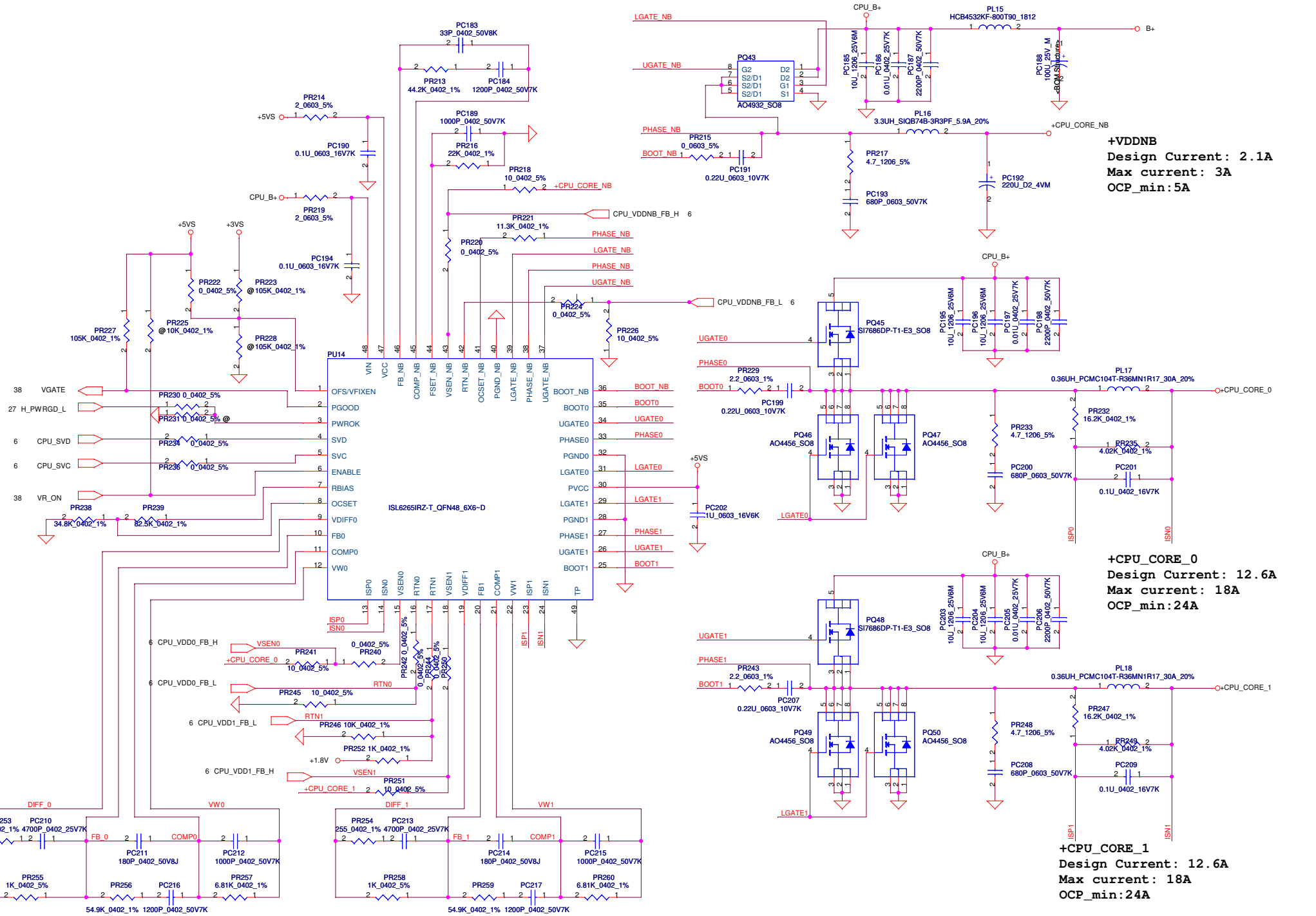
VFB=0.75V  
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / v_{in} + 50ns = 3.2E-7$   
 $F_{sw} = 200KHz$

$C_{out} ESR = 15m\ \Omega$   
 $I_{peak} = 3.58A, I_{max} = 2.51A$   
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw}) = 2.59A$   
 $\Rightarrow 1/2 \Delta I = 1.295A$   
 $V_{trip} = R_{trip} * I_{0uA} = 10K * 10uA = 0.1V$   
 $I_{ocp\_min} = V_{trip} / R_{dsonmax} * 1.4 + 1.295A = 4.939A$   
 $I_{ocp\_max} = (0.1 / (0.016 * 1.2)) + 1.1.295A = 5.208A + 1.295A = 6.503A$   
 $I_{ocp} = 6.503A \sim 4.939A$

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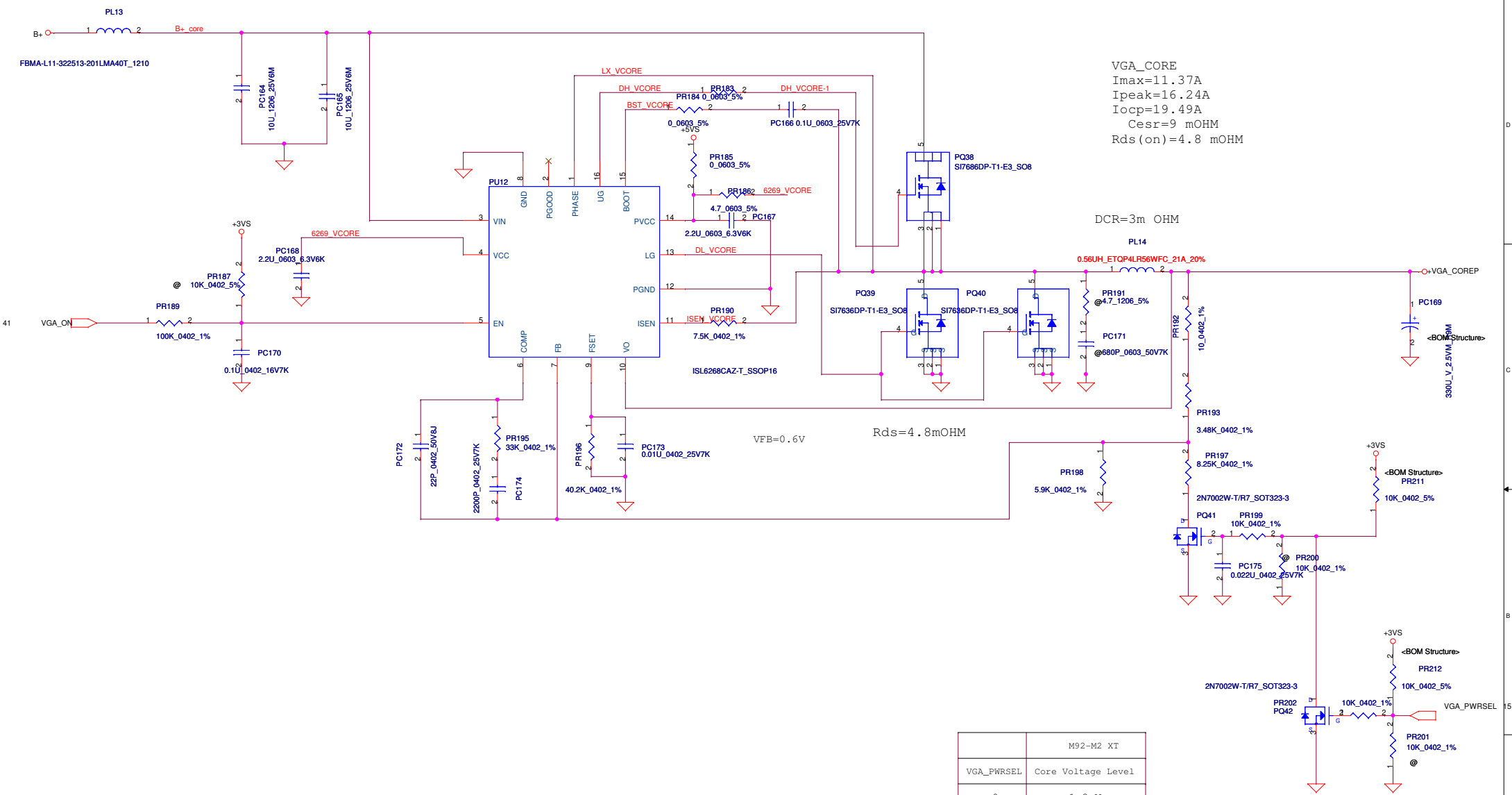


**+VDDNB**  
 Design Current: 2.1A  
 Max current: 3A  
 OCP\_min: 5A

**+CPU\_CORE\_0**  
 Design Current: 12.6A  
 Max current: 18A  
 OCP\_min: 24A

**+CPU\_CORE\_1**  
 Design Current: 12.6A  
 Max current: 18A  
 OCP\_min: 24A

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Issued Date	2008/04/16	Deciphered Date	2009/04/16	+CPU_CORE
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VGA\_CORE  
 I<sub>max</sub>=11.37A  
 I<sub>peak</sub>=16.24A  
 I<sub>ocp</sub>=19.49A  
 C<sub>esr</sub>=9 mOHM  
 R<sub>ds(on)</sub>=4.8 mOHM

DCR=3m OHM

VFB=0.6V

R<sub>ds</sub>=4.8mOHM

	M92-M2 XT
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT_KBLG0
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT_KBLG0
3	ADD snubber	EMI requestmnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT_KBLG0
4	ADD snubber	EMI requestmnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT_KBLG0
5	ADD CPU boot	EMI requestmnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT_KBLG0
6	ADD CPU boot	EMI requestmnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT_KBLG0
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT_KBLG0
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT_KBLG0
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT_KBLG0
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT_KBLG0
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT_KBLG0
12	Add Diode at back to back gate pin	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	Add PD9 zener diode 24V 1/2W	2009/04/09	DVT_NBLG0
13	Add resistance at back to back gate pin	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	Add PR107 150 ohm, size is 0805	2009/04/09	DVT_NBLG0
14	change capacitance value at PVCC	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	change value from 0.1uF to 1uF	2009/04/09	DVT_NBLG0
15	reserve capacitance at source to gate of back to back	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	reserve PC45 0.01uF at source to gate of back to back	2009/04/09	DVT_NBLG0
16	reserve resistance at CPU_VDD1_FB_L	for tigris design change, and add 1.8V net at PR252 pin2	0.1	53	reserve PR252 that it value is 1K(0402,1%) at CPU_VDD1_FB_L	2009/04/09	DVT_NBLG0
17	change resistance value at CPU_VDD1_FB_L	for tigris design change	0.1	53	change PR246's value to 10K(0402,1%)	2009/04/09	DVT_NBLG0

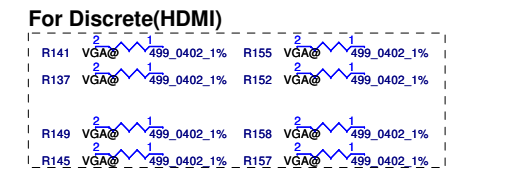
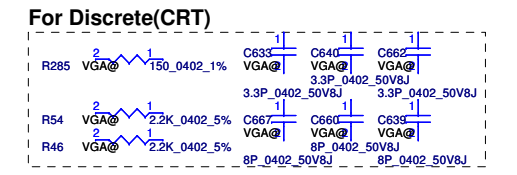
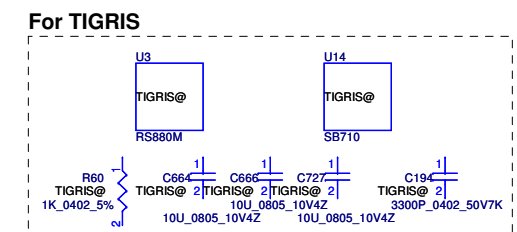
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor	Reserved EC SMBUS1 due to +3VS leakage when S3 entry with SMBUS2
	P.8	Add C174/C175/C176 (0.1u_0402)	EMI request
	P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@	BOM error
	P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)	UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0
	P.11	Reserve R490(0ohm_0402)	NA
	P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@	For DIS +1.1VS power source from fixed +NB_CORE
	P.22	Remove VRAM Samsung(Q-die) & Qimonda type	Customer request
	P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@	Separately as DIS sku only & UMA sku only
	P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@	For DIS sku only
	P.24	Reserve Q52/R501/R502/R503	Reserve for UMA sku white screen flash when boot issue check
	P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)	DFX request
	P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506	NA (Just no need to modify)
	P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@	Separately as DIS sku only & UMA sku only
	P.27	Add R496 with @ & R476/R482 with @	NA
	P.28	Add R509 with VGA@ & R510 with UMA@	Reserve SKU ID for SW even SW check device ID instead currently
	P.29	Reserve C862/C863/C855/C856	Reserve eSATA function for future request
	P.37	Change JUSB1 as SB700 USB port6	Dedicated HS port on lower-left position
	P.38	Change U20 as KB926 D3 version (SA00001J580)	NA
	P.38	D41 with VGA@ & D42 with UMA@	Separately as DIS sku only & UMA sku only
	P.38	U20.85 defined as TP_LOCK_LED# feature	LED control simultaneously with Tutch-Pad locked function
	P.38	Change R194 as 8.2kohm_0402	Change board ID as 1 (PCB revision : 0.2)

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PHASE	PAGE	MODIFICATION LIST	PURPOSE
	P.39	Add R250/LED11/SW4	Add T/P lock button & T/P lock button LED
	P.45	Reserve R499 , R497/R498/Q51	NA
	P.45	Stuff R202	+1.2VALW leakage 640mv pulse when AC insertion & then might cause OVP
	P.34	C26 with @ & C11 as SE070104Z80	NA
	P.42	Stuff R446(0ohm_0805) & un-stuff U32(Audio LDO)	NA
DVT2	P.6	Remove CPU side-band(internal) temp sensor function	NA
	P.11/38	Add U49/C857/R744 (Reserve U48) & D42 with @, remove D42	NA
	P.23/34	Add R676 for CLK_48M_SD , reserve R715 / R716 for CLK_48M_LAN	NA
	P.24	Add R508(2.7K_0402) for ENVDD of UMA sku	NA
	P.28	SB700 USB port 4 for Realtek RTS5159 card reader	NA
	P.33	Add(co-layout) Realtek RTS5159 card reader	NA
	P.37	Change JSAT1 PCB footprint as TYCO_1909574-1_11P-T	NA
	P.38	R194 change as 18K_0402	Change board ID as 2 (PCB revision : 0.3)
	P.40	LED1 / 5 / 8 / 9 /10 PCB footprint change as LED_HT-297DQ-GQ_4P	For DFX
	P.44	Add H28 & H29	For thermal
PVT	P.11	Add R511 with @ & U50	For LCD white screen flash when coldboot issue
	P.11	Add C874 / C875 (1u_0402)	For CRT(acer lab) flicker
	P.11/38	C857 / U49 with @ , R744 / D42 with UMA@	NA
	P.42	Add L94(SM010027780) close to audio codec	For EMI
	P.40	Modify LED 1 / 5 / 8 from dual Blue/Amber LED as single Blue LED	Follow acer spec
	P.39/40	Modify R12/R13/R17/R16 (300->220ohm) , modify R1/R2/R3 (1.2K->866ohm) , modify R10 (300->715ohm) , modify R245/R247 (4.99K->750ohm) , modify R244/R246 (4.99K->866ohm) , modify R250 (1.2K->5.1K)	For LED brightness test
	P.23	Change LAN_CLKREQ# from U18.51 to U18.24 output	NA
	NA	Change test pad (except T8/T13/T15/T17/T18/T24/T28 /T29/T33/T45/T46/T48/T50/T56/T57/T12) from TPC12 to TPC24	NA
	P.36	Reserve Q55 / Q56 / R745 / R746 / R747 / C876 to turn off power of finger printer	NA
	P.38	R194 change as 18K_0402 for change board ID as 3 (PCB revision : 0.4)	NA
MP		Search for MP font	NA



**PCB**

PCB 047 LA-5521P REV0 M/B

LA5521MB Rev0 : DA80000FI00  
 LA5521MB Rev1 : DA80000FI10  
 LA5521MB with Sub/B Rev1:TBD

<b>Security Classification</b>		<b>Compal Secret Data</b>		<b>Compal Electronics, Inc.</b>	
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
NBLG0_DVT	P.11	Reserve R515 / R516 / R517 & add R514	Reserve for UMA(RS880M) LCD varibright feature
	P.14	Change dual diode as single diode x 2	NA
	P.14	Reserve U37 / C859	Reserve for AMD cross display feature
	P.15	Reserve R518 / R513	Reserve for DIS(M92) LCD varibright feature
	P.18	Add R512 / Q57 / Q58 / R219 / C858 & reserve L64	For DIS(M92) backbias power saving feature
	P.22	Reserve R529 / R530	NA
	P.25	Add R522 / R524 & reserve R523 / R525 / R526 / R527 / R528 / D37 / Q20	NA
	P.29 P.34	Change Y2 / Y3 part from SJ125P0M200 (25MHz_20PF_+/-25PPM , 8.0x4.5x1.5mm) as SJ100003300 (25MHz_20PF_+/-30PPM , 5.0x3.2x1.2mm)	For cost down
	P.42	Reserve R519 / D36 / C203	NA
	P.31	R367 with @	RS880M internal PU already
	P.18	M92 decoupling power cap with @ (C355,C389,C237,C333,C202,C312,C313,C263,C264,C265,C343,C286,C247,C337,C353,C267)	NA

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