V6J SCHEMATIC V2.0

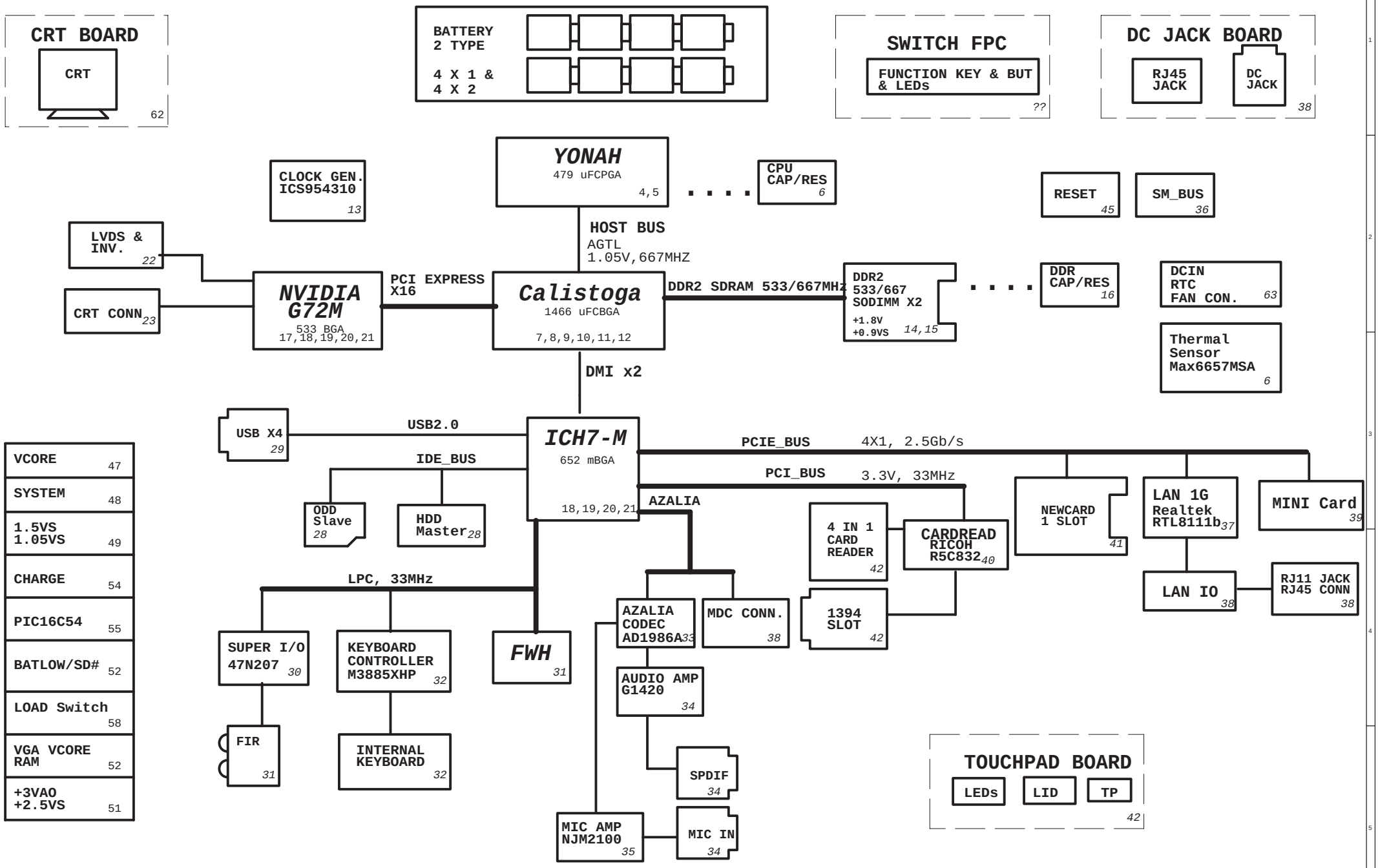
PAGE	Content
	SYSTEM PAGE REF.
4	YONAH CPU-1
5	YONAH CPU-2
6	CPU CAP & THERMAL SENSOR
7	Calistoga: CPU
8	Calistoga: DDR2 & DMI & PCIE
9	Calistoga: DDR2
10	Calistoga: POWER & Caps
11	Calistoga: GND & NCTF
12	Calistoga: Straps
13	CLOCK: ICS954310
14	DDR2 SODIMM (0) & Caps
15	DDR2 SODIMM (1) & Caps
16	DDR2 TERMINATOR
17	G72M: PCIE
18	G72M: FB
19	G72M: VRAM
20	G72M: RGB/LCD/ROM/GPIO
21	G72M: MIOB/CRSTAL/TMDS
22	LVDS & INVERTER CONNECTOR
23	CRT & LID SW & TPM CONNECTOR
24	ICH7: IDE & LPC & RTC & AC97
25	ICH7: PCI & INT & USB & DMI
26	ICH7: SMB & PWR & CLK & GPIO
27	ICH7: PWR & Caps
28	HDD & ODD CONNECTOR
29	USB CONNECTOR
30	SIO: LPC47N207
31	FIR & FWH
32	KBC: M38857
33	AUDIO AD1986A
34	AUDIO AMP GMT01420 & JACK
35	MIC AMP
36	SMBUS & POWER CONNECTION
37	GIGA LAN: REALTEK 8111B
38	LAN TRANSFORMER & JACK & MDC
39	MINI Card
40	RICOH: R5C832
41	NEWCARD
42	4 IN 1 MEMORY CARD & 1394
43	FAN CONTROLLER & DC IN
44	INSTANT KEY & TP BRD & SW FPC

PAGE	Content
	POWER PAGE REF.
45	POWER ON SEQUENCE
46	DISCHARGE & HOLES & EMI
47	POWER_VCORE
48	POWER_SYSTEM
49	POWER_I/O_1.5VS & 1.05VS
50	POWER_I/O_DDR & VTT
51	POWER_I/O_+3VAO & +2.5VS
52	POWER_VGA_CORE & RAM
53	POWER_+1.2VSP
54	POWER_CHARGER
55	POWER_PIC
56	POWER_SELECTOR
57	POWER_PROTECT
58	POWER_LOAD SWITCH
59	POWER_FLOWCHART
60	POWER_SIGNAL

PROJECT: V6J	REVISION: 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: Content & History	SCHEMATIC FILE NAME :
		SHEET 1 OF 63		RELEASE DATE :

DESIGN ENGINEER : Feng Lin

V6J: YONAH/Calistoga/G72M BLOCK DIAGRAM



PROJECT: V6J	REVISION: 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Feng Lin
		SHEET 2 OF 63		RELEASE DATE:	

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN --88E8001	AD16	0	B	
CardBus	AD17	1	B	
1394	AD17	1	A	
4 IN 1		1	C	

AZALIA : PCI_INTB#
USB 0,1 : PCI_INTA#
USB 2,3 : PCI_INTD#
USB 4,5 : PCI_INTC#

SMBUS ADDRESS :

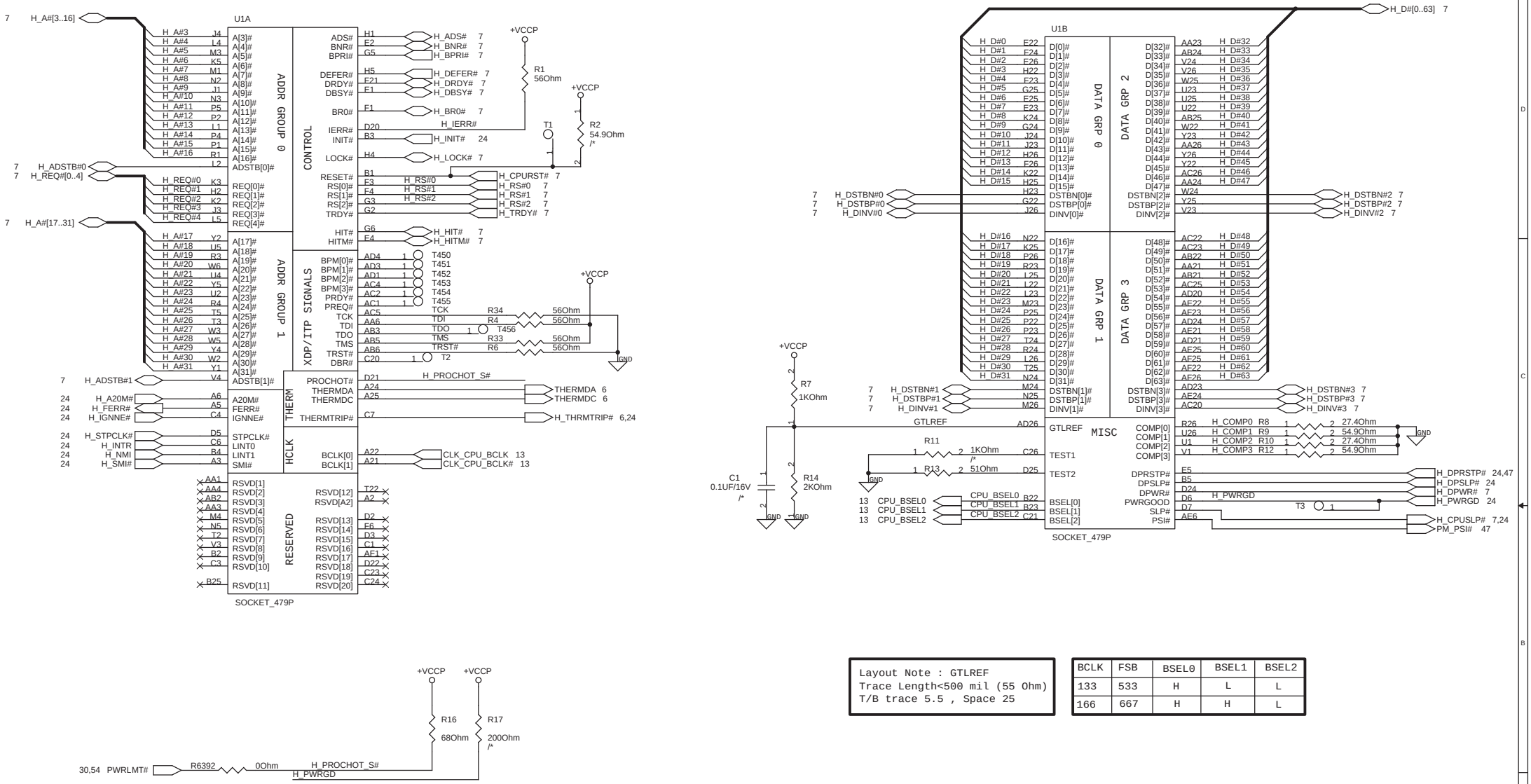
CLK = 1101001x (D2)
DDR_SODIMM0 = 1010010x (A4)
DDR_SODIMM1 = 1010000x (A0)
THERMAL = 1001100x (98)
TPM = TBD

ICH7M_GPIO	Use As	Signal Name	Power
GPIO00	GPI	PM_BMBUSY#	+3VS
GPIO01	GPI	PCI_REQ#5	+3VS
GPIO02	GPI	G72M_THRM#(reserve)	+3VS
GPIO[3:5]	GPI	PCI_INT[E:H]	+3VS
GPIO06	GPO	BACK_OFF#	+3VS
GPIO07	GPI	WIRLESS_#	+3VS
GPIO08	GPI	EXTSMI#_3A	+3VSUS
GPIO09	GPI	ACIN_OC_ICH(reserve)	+3VSUS
GPIO10	GPI	CHG_FULL_OC	+3VSUS
GPIO11	NATIVE	SMBALERT#	+3VSUS
GPIO12	GPI	KBCSCI_3	+3VSUS
GPIO13	GPI	BATIN_OC#_ICH(reserve)	+3VSUS
GPIO14	GPO	LID_ICH#_3A(reserve)	+3VSUS
GPIO15	GPI	802_LED#	+3VSUS
GPIO16	GPO	PM_DPRSLPVR	+3VSUS
GPIO17	GPO	PCI_GNT#5	+3VSUS
GPIO18	GPO	STP_PCI#	+3VSUS
GPIO19	GPI	SATA_DET_#1	+3VSUS
GPIO20	GPO	STP_CPU#	+3VS
GPIO21	GPI	BATSEL_2P(reserve)	+3VS
GPIO22	NATIVE	PCI_REQ#4	+3VS
GPIO23	NATIVE	LDRQ1#	+3VS
GPIO24	GPO		+3VSUS
GPIO25	GPO		+3VSUS
GPIO26	GPO	OP_SD#	+3VSUS
GPIO27	GPO	**WLAN_ON**	+3VSUS
GPIO28	GPO	**PWR_1HZ**	+3VSUS
GPIO29	NATIVE	USB_OC#45	+3VSUS
GPIO30	NATIVE	USB_OC#67	+3VSUS
GPIO31	NATIVE	USB_OC#67	+3VSUS
GPIO32	GPO	PM_CLKRUN#	+3VSUS
GPIO33	GPO	BT_ON	+3VS
GPIO34	GPO	FWH_WP#	+3VS
GPIO35	GPO		+3VS
GPIO36	GPO	BT_LED#	+3VS
GPIO37	GPI	PCB_VID0	+3VS
GPIO38	GPI	PCB_VID1	+3VS
GPIO39	GPI	PCB_VID2	+3VS
GPIO[40:47]	N/A	N/A	N/A
GPIO48	NATIVE	**FWH_TBL#**	+3VS
GPIO49	NATIVE	H_PWRGD	+3VS

M38857_GPIO	Use As	Signal Name
P20	GPO	KBCRSM
P21	GPI	
P22	GPO	BAT_LEARN
P23	GPO	**CPPE_EN**
P24	GPO	SET_PCIRSTNS#
P25	GPO	CAP_LED#
P26	GPO	NUM_LED#
P27	GPO	SCROLL_LED#
P40	GPO	KBC_EXTSMI
P41	GPO	**PANLOCK_LED#**
P42	GPO	WATCHDOG
P43	GPO	CHG_FULL_KBC(reserve)
P44	GPO	KBDCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LOW#_KBC
P51	GPO	
P52	GPI	KBDDT0
P53	GPI	KBDDT1
P54	GPI	LID_ICH#_3A
P55	GPI	BAT_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	**BLUETOOTH_#**
P61	GPI	INTERNET#
P62	GPI	**CPPE#**
P63	GPI	
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPI	PANLOCK_#
P67	GPI	
P76	GPI/O	SMD_BAT
P77	GPI/O	SMC_BAT

G72M_GPIO	Use As	Signal Name
GPIO00	GPI	
GPIO01	GPI	
GPIO02	GPO	
GPIO03	GPO	LCD_VDD_EN#
GPIO04	GPO	LCD_BACKEN
GPIO05	GPO	
GPIO06	GPO	
GPIO07	GPO	
GPIO08	GPI	GPIO8/ALERT#
GPIO09	GPO	
GPIO10	GPIO	G72M_GPIO12
GPIO11	GPO	
GPIO12	GPO	

47N207_GPIO	Use As	Signal Name
GP10	GPIO	
GP11	GPIO	
GP12	GPO	
GP13	GPO	
GP14	GPO	FIR_SEL
GP15	GPIO	**PWR_THRO#**
GP16	GPIO	**ODD_DIS#**
GP17	GPIO	**RST#_XCARD**
GP30	GPIO	PID0
GP31	GPIO	
GP32	GPIO	**G72M_THRO#**
GP33	GPIO	CPUFAN_SPD_A
GP34	GPIO	SW_RST#
GP35	GPIO	
GP36	GPIO	
GP37	GPIO	



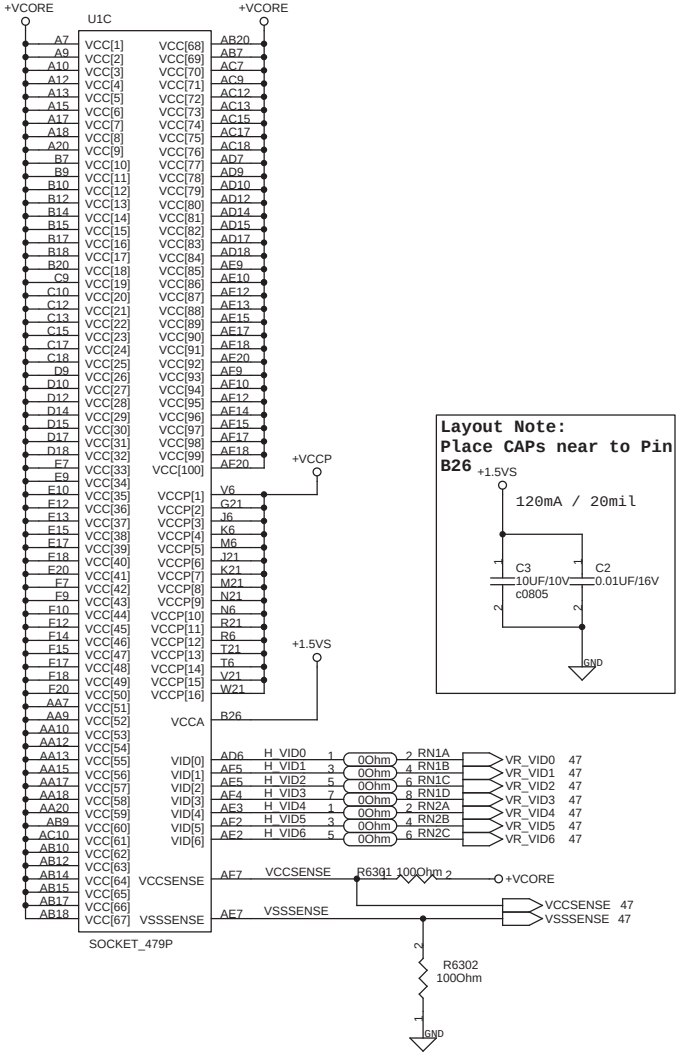
Layout Note : GTLREF
Trace Length<500 mil (55 Ohm)
T/B trace 5.5 , Space 25

BCLK	FSB	BSEL0	BSEL1	BSEL2
133	533	H	L	L
166	667	H	H	L

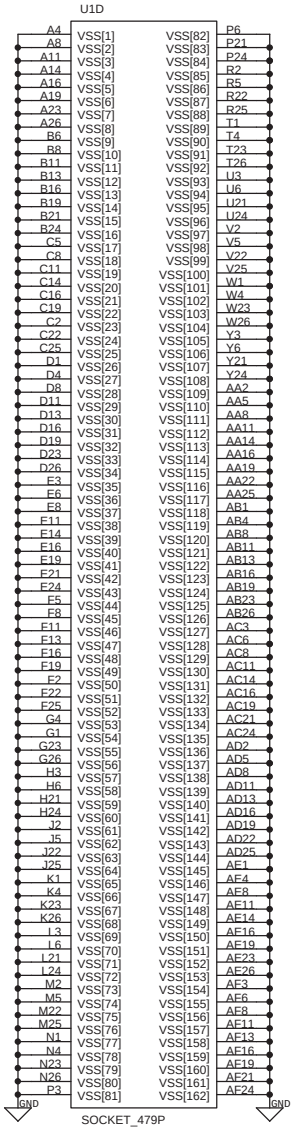
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: YONAH CPU (1)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 4 OF 63		RELEASE DATE :	

YONAH FSB667			
	LFM	TYP	HFM
CPU State	C4	C3	C0
VCC	1.14V	1.2V	1.356V
ICC	0.9A	7.59A	27A

YONAH FSB667			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
ICCP			2.5A



Layout Note:
Place CAPs near to Pin B26



MOBILE YONAH VID TABLE

VID[6..0]	Voltage	VID[6..0]	Voltage	VID[6..0]	Voltage	VID[6..0]	Voltage
0 0 0 0 0 0 0	1.5000V	0 1 0 0 0 0 0	1.1000V	1 0 0 0 0 0 0	0.7000V	1 1 0 0 0 0 0	0.3000V
0 0 0 0 0 0 1	1.4875V	0 1 0 0 0 0 1	1.0875V	1 0 0 0 0 0 1	0.6875V	1 1 0 0 0 0 1	0.2875V
0 0 0 0 0 1 0	1.4750V	0 1 0 0 0 1 0	1.0750V	1 0 0 0 0 1 0	0.6750V	1 1 0 0 0 1 0	0.2750V
0 0 0 0 0 1 1	1.4625V	0 1 0 0 0 1 1	1.0625V	1 0 0 0 0 1 1	0.6625V	1 1 0 0 0 1 1	0.2650V
0 0 0 0 1 0 0	1.4500V	0 1 0 0 1 0 0	1.0500V	1 0 0 0 1 0 0	0.6500V	1 1 0 0 1 0 0	0.2500V
0 0 0 0 1 0 1	1.4375V	0 1 0 0 1 0 1	1.0375V	1 0 0 0 1 0 1	0.6375V	1 1 0 0 1 0 1	0.2375V
0 0 0 0 1 1 0	1.4250V	0 1 0 0 1 1 0	1.0250V	1 0 0 0 1 1 0	0.6250V	1 1 0 0 1 1 0	0.2250V
0 0 0 0 1 1 1	1.4125V	0 1 0 0 1 1 1	1.0125V	1 0 0 0 1 1 1	0.6125V	1 1 0 0 1 1 1	0.2125V
0 0 0 1 0 0 0	1.4000V	0 1 0 1 0 0 0	1.0000V	1 0 0 1 0 0 0	0.6000V	1 1 0 1 0 0 0	0.2000V
0 0 0 1 0 0 1	1.3875V	0 1 0 1 0 0 1	0.9875V	1 0 0 1 0 0 1	0.5875V	1 1 0 1 0 0 1	0.1875V
0 0 0 1 0 1 0	1.3750V	0 1 0 1 0 1 0	0.9750V	1 0 0 1 0 1 0	0.5750V	1 1 0 1 0 1 0	0.1750V
0 0 0 1 0 1 1	1.3625V	0 1 0 1 0 1 1	0.9625V	1 0 0 1 0 1 1	0.5625V	1 1 0 1 0 1 1	0.1625V
0 0 0 1 1 0 0	1.3500V	0 1 0 1 1 0 0	0.9500V	1 0 0 1 1 0 0	0.5500V	1 1 0 1 1 0 0	0.1500V
0 0 0 1 1 0 1	1.3375V	0 1 0 1 1 0 1	0.9375V	1 0 0 1 1 0 1	0.5375V	1 1 0 1 1 0 1	0.1375V
0 0 0 1 1 1 0	1.3250V	0 1 0 1 1 1 0	0.9250V	1 0 0 1 1 1 0	0.5250V	1 1 0 1 1 1 0	0.1250V
0 0 0 1 1 1 1	1.3125V	0 1 0 1 1 1 1	0.9125V	1 0 0 1 1 1 1	0.5125V	1 1 0 1 1 1 1	0.1125V
0 0 1 0 0 0 0	1.3000V	0 1 1 0 0 0 0	0.9000V	1 0 1 0 0 0 0	0.5000V	1 1 1 0 0 0 0	0.1000V
0 0 1 0 0 0 1	1.2875V	0 1 1 0 0 0 1	0.8875V	1 0 1 0 0 0 1	0.4875V	1 1 1 0 0 0 1	0.0875V
0 0 1 0 0 1 0	1.2750V	0 1 1 0 0 1 0	0.8750V	1 0 1 0 0 1 0	0.4750V	1 1 1 0 0 1 0	0.0750V
0 0 1 0 0 1 1	1.2625V	0 1 1 0 0 1 1	0.8625V	1 0 1 0 0 1 1	0.4625V	1 1 1 0 0 1 1	0.0625V
0 0 1 0 1 0 0	1.2500V	0 1 1 0 1 0 0	0.8500V	1 0 1 0 1 0 0	0.4500V	1 1 1 0 1 0 0	0.0500V
0 0 1 0 1 0 1	1.2375V	0 1 1 0 1 0 1	0.8375V	1 0 1 0 1 0 1	0.4375V	1 1 1 0 1 0 1	0.0375V
0 0 1 0 1 1 0	1.2250V	0 1 1 0 1 1 0	0.8250V	1 0 1 0 1 1 0	0.4250V	1 1 1 0 1 1 0	0.0250V
0 0 1 0 1 1 1	1.2125V	0 1 1 0 1 1 1	0.8125V	1 0 1 0 1 1 1	0.4125V	1 1 1 0 1 1 1	0.0125V
0 0 1 1 0 0 0	1.2000V	0 1 1 1 0 0 0	0.8000V	1 0 1 1 0 0 0	0.4000V	1 1 1 1 0 0 0	0.0000V
0 0 1 1 0 0 1	1.1875V	0 1 1 1 0 0 1	0.7875V	1 0 1 1 0 0 1	0.3875V	1 1 1 1 0 0 1	0.0000V
0 0 1 1 0 1 0	1.1750V	0 1 1 1 0 1 0	0.7750V	1 0 1 1 0 1 0	0.3750V	1 1 1 1 0 1 0	0.0000V
0 0 1 1 0 1 1	1.1625V	0 1 1 1 0 1 1	0.7625V	1 0 1 1 0 1 1	0.3625V	1 1 1 1 0 1 1	0.0000V
0 0 1 1 1 0 0	1.1500V	0 1 1 1 1 0 0	0.7500V	1 0 1 1 1 0 0	0.3500V	1 1 1 1 1 0 0	0.0000V
0 0 1 1 1 0 1	1.1375V	0 1 1 1 1 0 1	0.7375V	1 0 1 1 1 0 1	0.3375V	1 1 1 1 1 0 1	0.0000V
0 0 1 1 1 1 0	1.1250V	0 1 1 1 1 1 0	0.7250V	1 0 1 1 1 1 0	0.3250V	1 1 1 1 1 1 0	0.0000V
0 0 1 1 1 1 1	1.1125V	0 1 1 1 1 1 1	0.7125V	1 0 1 1 1 1 1	0.3125V	1 1 1 1 1 1 1	0.0000V

YONAH VID TABLE

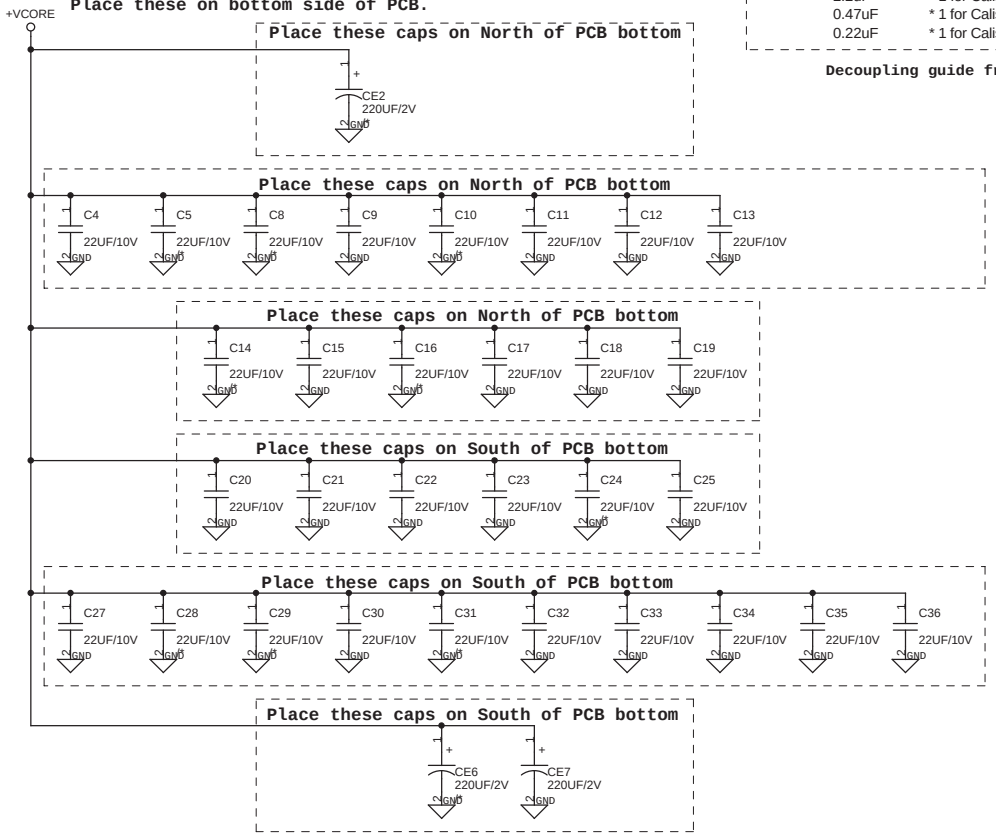
CPU FREQ.	HFM VOLTAGE	1.6G	1.4G	1.2G	1G	LFM 0.8G	C3/C4
2.13G/B1	1.372V					0.988V	0.726V
2.0G/B1	1.356V					0.988V	0.726V
1.87G/B1	1.356V					0.988V	0.726V
1.73G/B1	1.356V					0.988V	0.726V
1.6G/B1	1.356V					0.988V	0.726V
1.6G/A2	1.308V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V

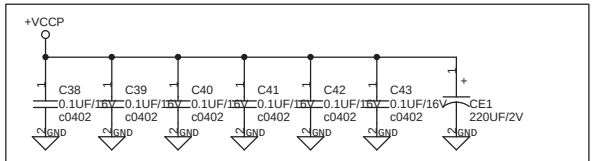
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: YONAH CPU (2)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 5 OF 63		RELEASE DATE :	

VCORE	22uF/6.3V	* 20
	330uF/2V	* 6
VCCP	0.1uF	* 5 for CPU
	220uF	* 1 for CPU
	220uF	* 1 for Calistoga
	4.7uF	* 1 for Calistoga
	2.2uF	* 1 for Calistoga
	0.47uF	* 1 for Calistoga
	0.22uF	* 1 for Calistoga

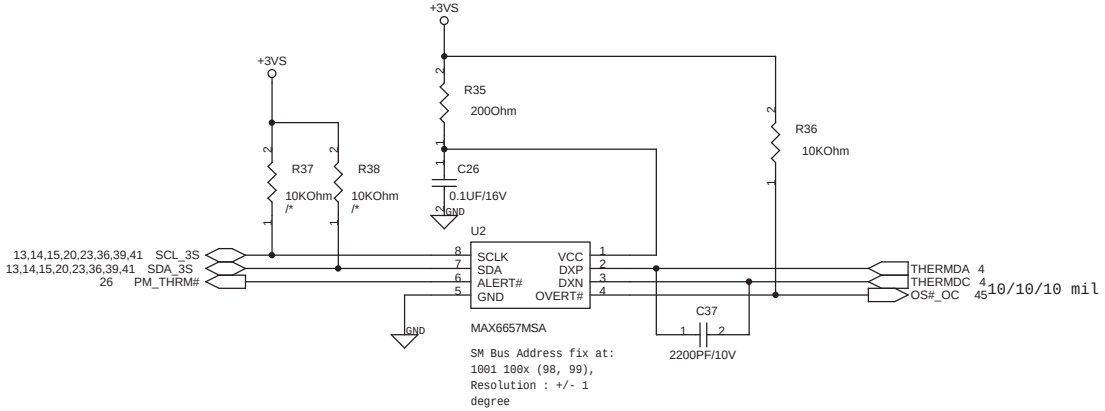
Decoupling guide from INTEL

Layout Note :
All of VCore Decoupling Caps
Place these on bottom side of PCB.

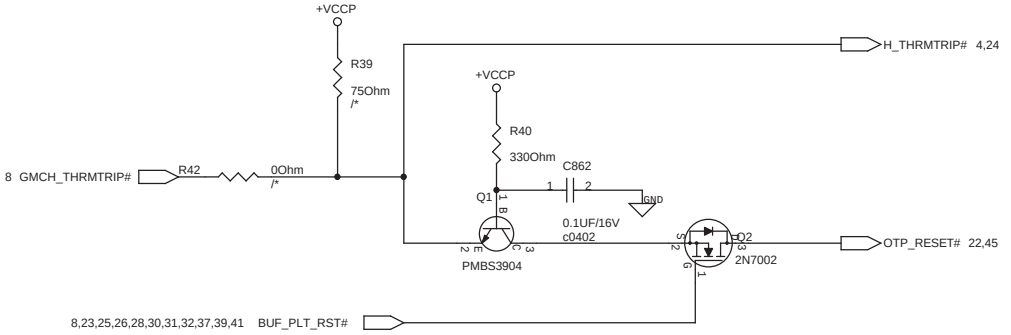




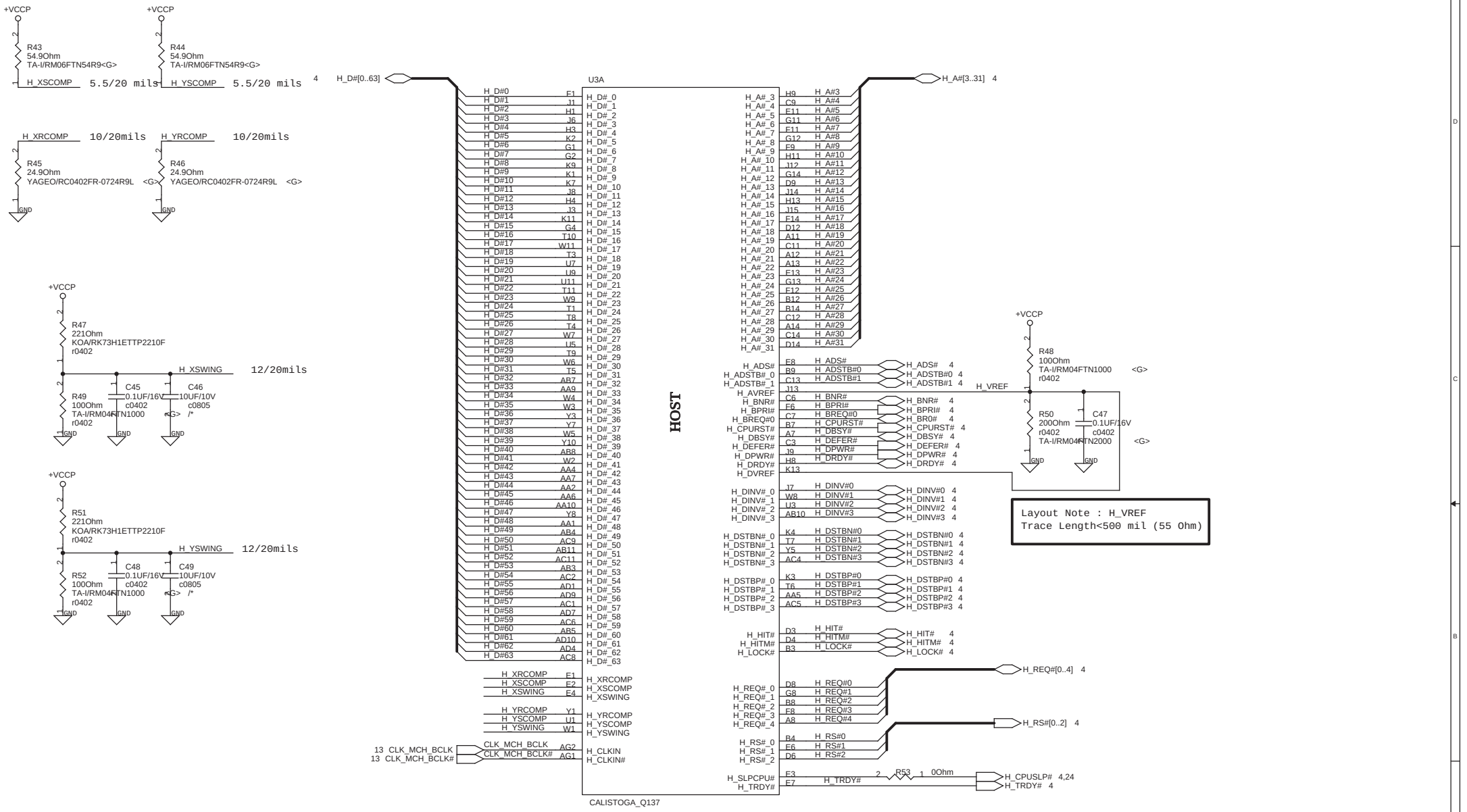
Layout Note :
+V1.05S (VCCP) Decoupling Capacitor
(Place near CPU)



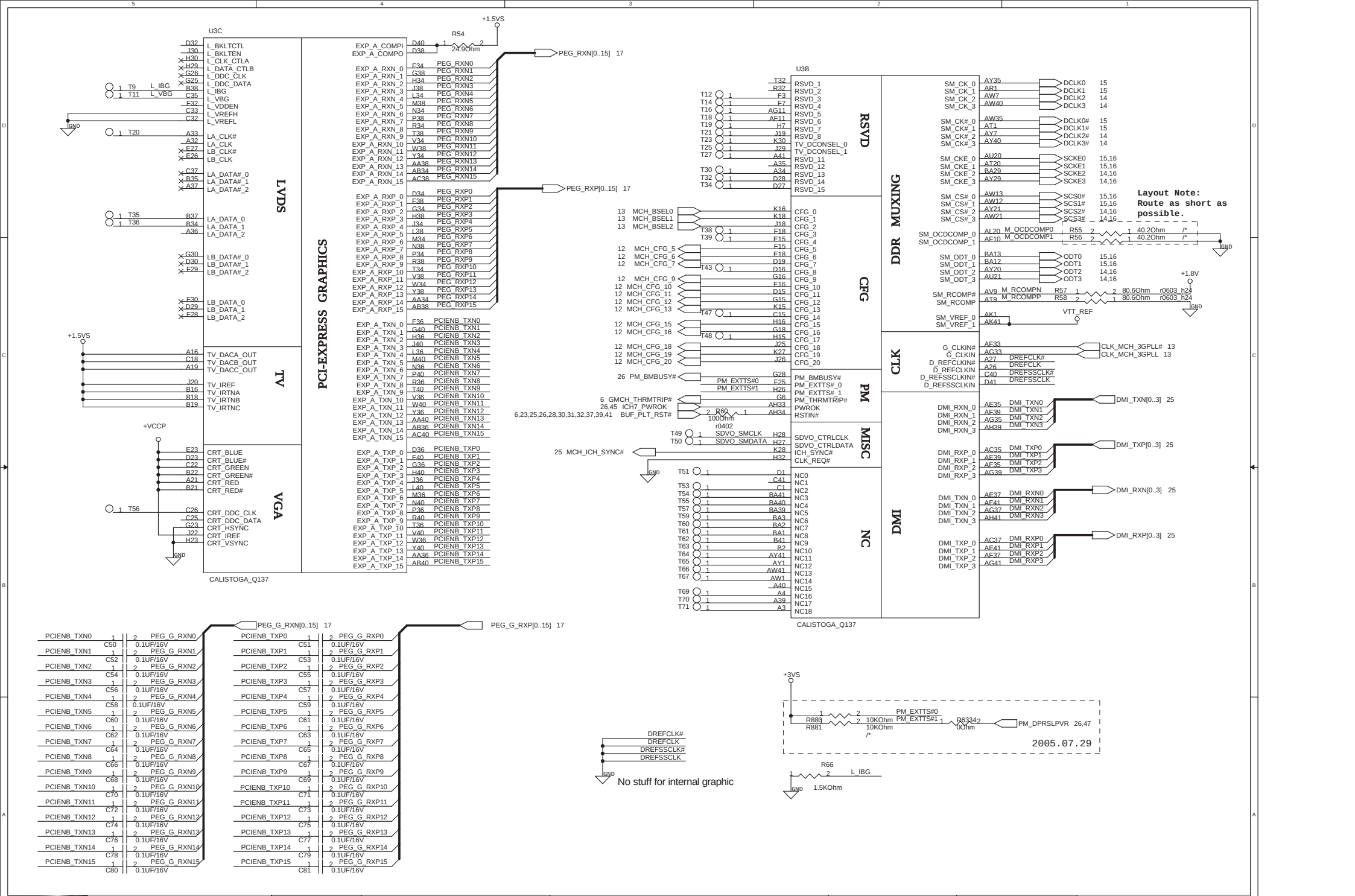
THERMAL SENSOR



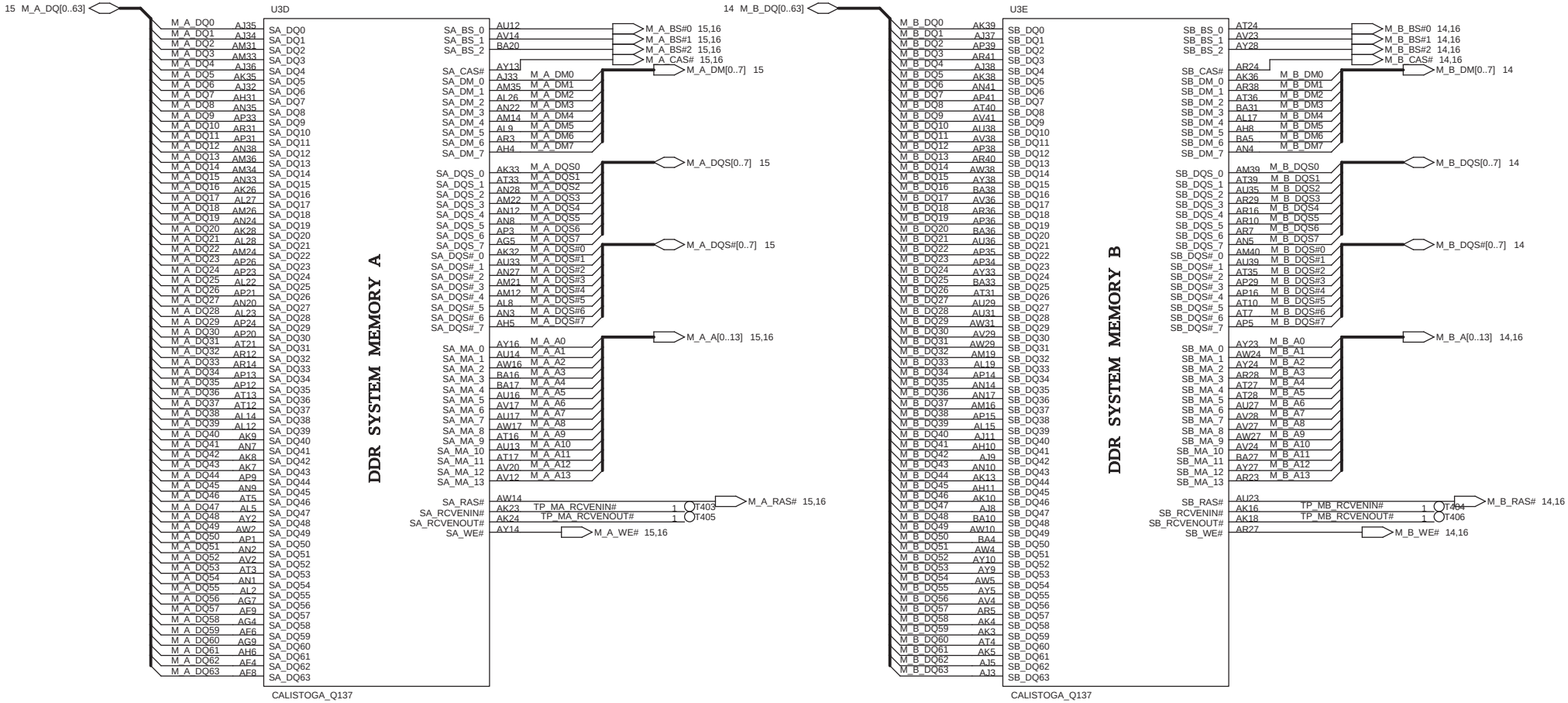
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***Caps & THERMAL & ITP***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **6** OF **63**		RELEASE DATE :	



PROJECT: V6J	REVISION: 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: MCH : CPU	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: Feng Lin
		SHEET 7 OF 63		RELEASE DATE:	



PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: MCH: PCIE/DMI/DDR2	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 8 OF 63		RELEASE DATE :	



PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***Calistoga DDR2 (3)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **9** OF **63**		RELEASE DATE :	

NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

+1.5VS
R69 1 2 0Ohm /*
+1.5VS_DPLLA
R70 1 2 0Ohm /*
+1.5VS_DPLLB
L1 120Ohm/100Mhz l0603
C87 0.1UF/16V c0402
C864 22UF/10V
+1.5VS_HPLL
L3 120Ohm/100Mhz l0603
C91 0.1UF/16V c0402
C865 22UF/10V
+1.5VS_MPLL
L4 90nH
CE8 220UF/2V
C92 10UF/10V c0805
C93 10UF/10V c0805
+1.5VS_PCIE
GND

OLD: 09G028901110IN
NEW: 09G028901110

+1.5VS l0603 120Ohm/100Mhz L5 +1.5VS_IOAUX
C94 0.1UF/16V c0402

+2.5VS C100 0.1UF/16V c0402
+3VS C101 4.7UF/6.3V c0603
C102 10UF/10V c0805
C103 0.1UF/16V c0402
+1.5VS C104 0.1UF/16V c0402
C105 10UF/10V c0805

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

PLACE IN CAVITY
C106 4.7UF/6.3V c0603
C107 2.2UF/6.3V c0603

PLACE ON THE EDGE FOR VTT
+VCCP
C866 0.47UF/16V
C108 0.22UF/16V c0603
CE9 220UF/2V

U3H — POWER

H22	VCCSYNC	
C30	VCC_TXLVDS0	
B30	VCC_TXLVDS1	
A30	VCC_TXLVDS2	
AJ41	VCC3G0	
AB41	VCC3G1	
Y41	VCC3G2	
V41	VCC3G3	
R41	VCC3G4	
N41	VCC3G5	
L41	VCC3G6	
AC33	VCCA_3GPLL	
G41	VCCA_3GBG	
H41	VSSA_3GBG	
F21	VCCA_CRTDAC0	
F21	VCCA_CRTDAC1	
G21	VSSA_CRTDAC	
B26	VCCA_DPLLA	
C39	VCCA_DPLLB	
AF1	VCCA_HPLL	
A38	VCCA_LVDS	
B39	VSSA_LVDS	
AF2	VCCA_MPLL	
H20	VCCA_TVBG	
G20	VSSA_TVBG	
E19	VCCA_TVDACA0	
F19	VCCA_TVDACA1	
C20	VCCA_TVDACB0	
D20	VCCA_TVDACB1	
E20	VCCA_TVDACC0	
F20	VCCA_TVDACC1	
AH1	VCCD_HMPLL0	
AH2	VCCD_HMPLL1	
A28	VCCD_LVDS0	
B28	VCCD_LVDS1	
C28	VCCD_LVDS2	
D21	VCCD_TVDAC	
A23	VCC_HV0	
B23	VCC_HV1	
B25	VCC_HV2	
H19	VCCD_QTVDAC	
AK31	VCCAUX0	
AF31	VCCAUX1	
AE31	VCCAUX2	
AC31	VCCAUX3	
AL30	VCCAUX4	
AK30	VCCAUX5	
AJ30	VCCAUX6	
AH30	VCCAUX7	
AG30	VCCAUX8	
AF30	VCCAUX9	
AE30	VCCAUX10	
AD30	VCCAUX11	
AC30	VCCAUX12	
AG29	VCCAUX13	
AF29	VCCAUX14	
AE29	VCCAUX15	
AD29	VCCAUX16	
AC29	VCCAUX17	
AG28	VCCAUX18	
AF28	VCCAUX19	
AE28	VCCAUX20	
AH22	VCCAUX21	
AJ21	VCCAUX22	
AH21	VCCAUX23	
AJ20	VCCAUX24	
AH20	VCCAUX25	
AH19	VCCAUX26	
P19	VCCAUX27	
P16	VCCAUX28	
AH15	VCCAUX29	
P15	VCCAUX30	
AH14	VCCAUX31	
AG14	VCCAUX32	
AF14	VCCAUX33	
AE14	VCCAUX34	
Y14	VCCAUX35	
AF13	VCCAUX36	
AE13	VCCAUX37	
AF12	VCCAUX38	
AE12	VCCAUX39	
AD12	VCCAUX40	

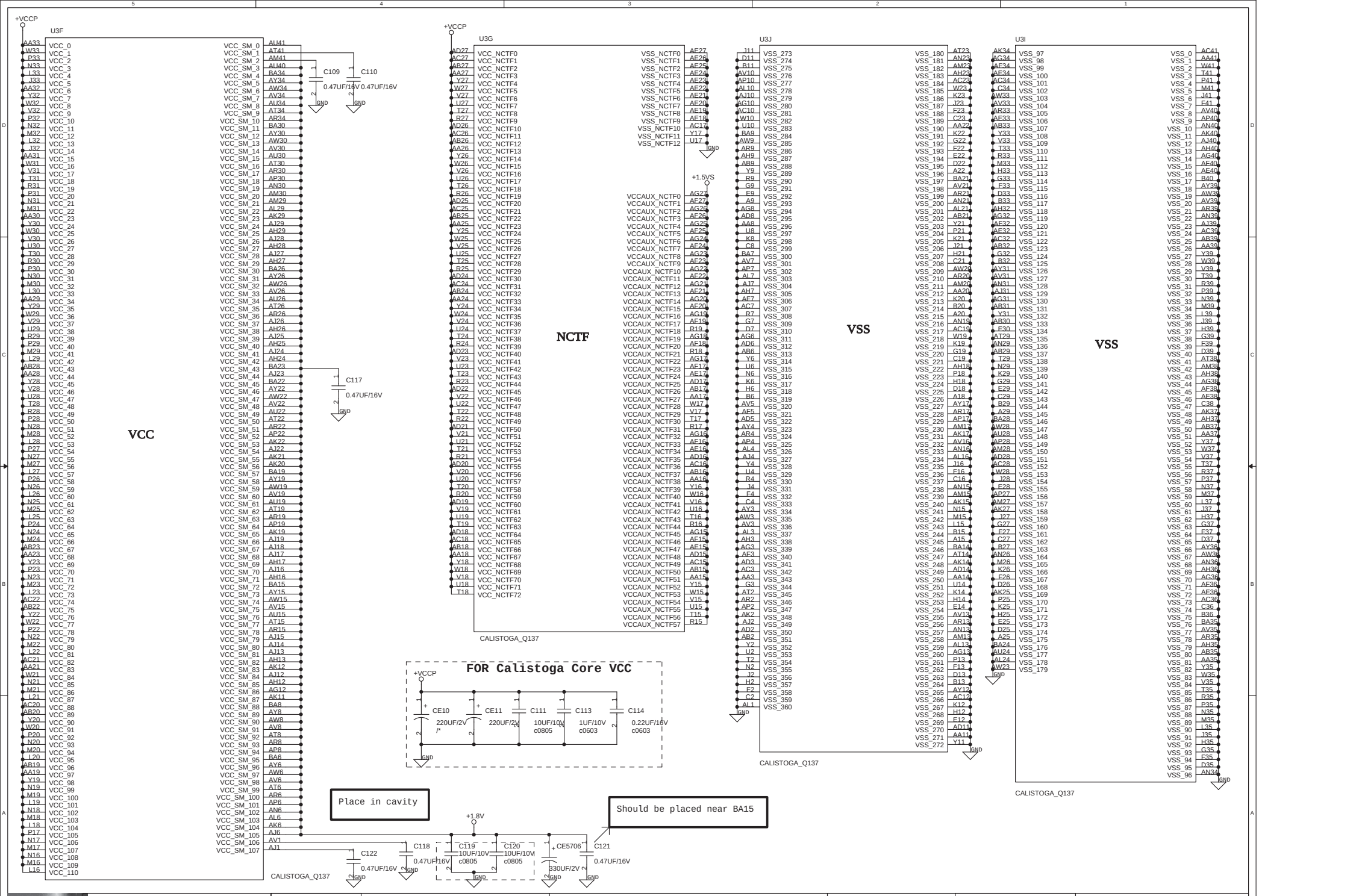
CALISTOGA_Q137

+1.5VS L85 1UH R6362 0.5Ohm
+2.5VS C84 0.1UF/16V c0402 C85 10UF/10V c0805
+VCCP C863 0.1UF/16V c0402
+1.5VS_PCIE
+1.5VS_DPLLA +1.5VS_DPLLB +1.5VS_HPLL
T72
+1.5VS_MPLL
+1.5VS
+3VS C95 0.1UF/16V c0402 C96 10UF/10V c0805
+1.5VS_IOAUX

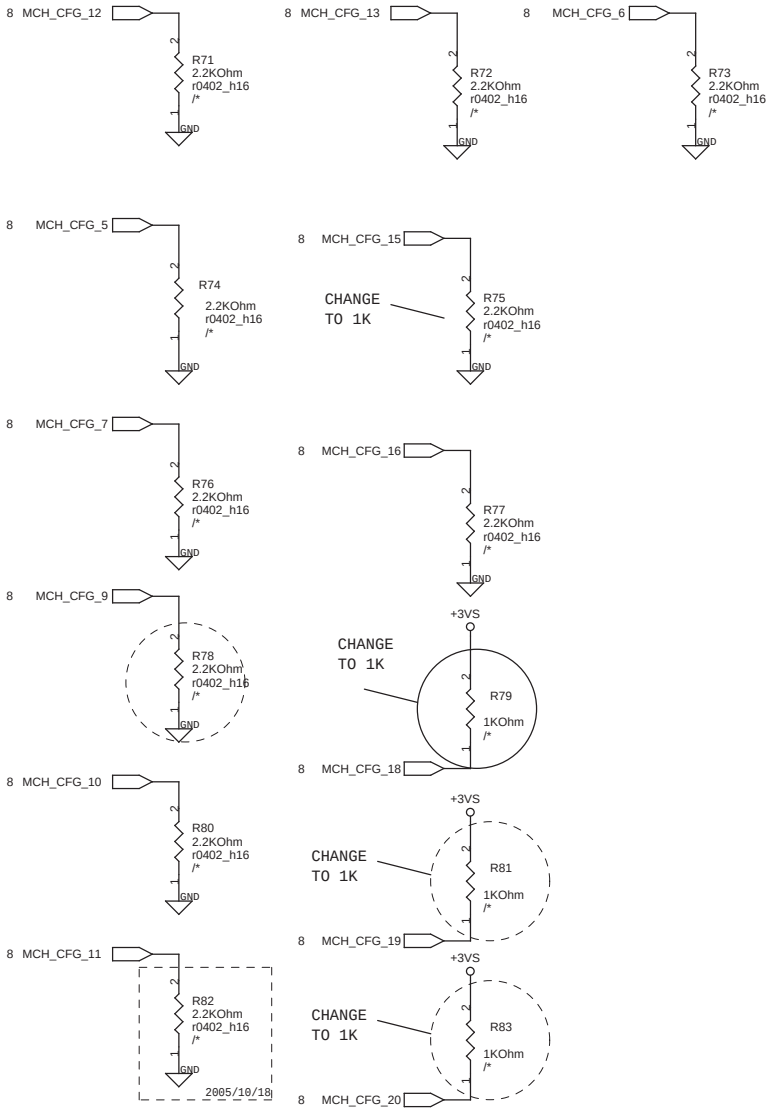
+VCCP

VTT_0	AC14
VTT_1	AB14
VTT_2	W14
VTT_3	V14
VTT_4	T14
VTT_5	R14
VTT_6	P14
VTT_7	N14
VTT_8	M14
VTT_9	L14
VTT_10	AD13
VTT_11	AC13
VTT_12	AB13
VTT_13	AA13
VTT_14	Y13
VTT_15	W13
VTT_16	V13
VTT_17	U13
VTT_18	T13
VTT_19	R13
VTT_20	N13
VTT_21	M13
VTT_22	L13
VTT_23	AB12
VTT_24	AA12
VTT_25	Y12
VTT_26	W12
VTT_27	V12
VTT_28	U12
VTT_29	T12
VTT_30	R12
VTT_31	P12
VTT_32	N12
VTT_33	M12
VTT_34	L12
VTT_35	R11
VTT_36	P11
VTT_37	N11
VTT_38	M11
VTT_39	R10
VTT_40	P10
VTT_41	N10
VTT_42	M10
VTT_43	P9
VTT_44	N9
VTT_45	M9
VTT_46	R8
VTT_47	P8
VTT_48	N8
VTT_49	M8
VTT_50	P7
VTT_51	N7
VTT_52	M7
VTT_53	R6
VTT_54	P6
VTT_55	M6
VTT_56	A6
VTT_57	R5
VTT_58	P5
VTT_59	N5
VTT_60	M5
VTT_61	P4
VTT_62	N4
VTT_63	M4
VTT_64	R3
VTT_65	P3
VTT_66	N3
VTT_67	M3
VTT_68	R2
VTT_69	P2
VTT_70	M2
VTT_71	D2
VTT_72	AB1
VTT_73	R1
VTT_74	P1
VTT_75	N1
VTT_76	M1

VTTLF_CAP3 C97 0.47UF/16V
VTTLF_CAP2 VTTLF_CAP1 C98 0.47UF/16V C99 22UF/16V



PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***MCH: GND/NCTF***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Feng Lin***
		SHEET **11** OF **63**		RELEASE DATE:	



Signal Name	Configuration	Notes
CFG[2:0]	011= 667 FSB 001= 533 FSB	Selection the FSB freqency
CFG5	0= DMIx2 1= DMIx4	Selection between DMIx2 and DMIx4
CFG7	0= Reserved 1= Mobil Yonah	Control the target processor
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG[13:12]	01= XOR 10= Z 11= Normal Operation	
CFG16	0= Dynamic ODT DIS 1= Dynamic ODT EN	Control FSB Dynamic ODT
CFG18	0= 1.05V 1= 1.5V	Control GMCH Vcore level
CFG19	0= Normal Operation 1= DMI Lane Revesal EN	
SDVOCTRL_DATA	0= No SDVO device 1= SDVO device present	

Intel Demo Circuit

CFG6	0= Moby Dick 1= Calistoga	
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG11	0= Reserved 1= 8x Enable	PSB 4x CLK Enable
CFG20	0= Only SDVO or PCIE x1 (Default) 1= SDVO and PCIE x1 are operating	

CFG[2..0] need external pullup resistors.
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

PLACE termination close to source IC

CLK_CPU_BCLK R91 49.9Ohm
CLK_CPU_BCLK# R92 49.9Ohm
CLK_MCH_BCLK R96 49.9Ohm
CLK_MCH_BCLK# R97 49.9Ohm
CLK_PCIE_ICH R98 49.9Ohm
CLK_PCIE_ICH# R100 49.9Ohm
CLK_MCH_3GPLL R102 49.9Ohm
CLK_MCH_3GPLL# R103 49.9Ohm
CLK_PCIE_NEWCARD R6376 49.9Ohm
CLK_PCIE_NEWCARD# R6377 49.9Ohm
CLK_PCIE_LAN R110 49.9Ohm
CLK_PCIE_LAN# R111 49.9Ohm
CLK_PCIE_MINICARD R112 49.9Ohm
CLK_PCIE_MINICARD# R114 49.9Ohm
CLK_PCIE_PEG R115 49.9Ohm
CLK_PCIE_PEG# R116 49.9Ohm

CPU_BSEL0 R99 1KOhm MCH_BSEL0 8
CPU_BSEL1 R101 1KOhm MCH_BSEL1 8
CPU_BSEL2 R104 1KOhm MCH_BSEL2 8

R93 R94 R95 1KOhm /*
R885 R886 R887 0Ohm /*

+3VS +3VS_CLK +3VS_VDDPCI +3VS_VDD48 +3VS_VDDA +3VS_VDDREF

L6 120Ohm/100Mhz
L7 120Ohm/100Mhz

C123 C124 0.1UF/16V
C125 10UF/10V
C126 C127 C128 C129 0.1UF/16V
C130 10UF/10V
C131 C132 0.1UF/16V
C133 10UF/10V
C134 0.1UF/16V
C135 10UF/10V
C136 0.1UF/16V
C137 0.1UF/16V
C138 C139 22PF/25V
X1 14.318Mhz

R107 10KOhm /* PCICLK2
R113 2.2Ohm
R888 0Ohm /*
R895 10KOhm /*
R108 2.2Ohm
R109 1Ohm

U4 ICS954310BGLFT

VDDPCIEX1 VDDPCIEX2 VDDPCIEX3 VDDPCI1 VDDPCI2 VDD VDDCPU VDDA GNDA X1 X2
VDD48 VDDREF PCI/PCIEX_STOP# CPU_STOP#
CPUCLKT1 CPUCLKC1 CPUCLKT0 CPUCLKC0 CPUCLKT2_ITP/PCIEXT8 CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7 PEREQ2#/PCIEXC7
PCIEXT6 PCIEXC6 PCIEXT5 PCIEXC5 PCIEXT4 PCIEXC4 PCIEXT3 PCIEXC3 PCIEXT2 PCIEXC2 PCIEXT1 PCIEXC1
SATACLKT SATACLKC DOTT_96MHz DOTC_96MHz
PEREQ3# PEREQ4# Vt_PwrGd#/PD REF1/FSLC/TEST_SEL REF0
27FIX/LCD_SSCGT/PCIEX0T 27SS/LCD_SSCGC/PCIEX0C FSLA/USB_48MHz FSLB/TEST_MODE SELPCIEX0_LCD#PCICLK5 PCICLK4 PCICLK3 PCICLK2/REQ_SEL SELLCD_27#/PCICLK_F1 ITP_EN/PCICLK_F0 SCLK SDATA IREF
GND1 GND2 GND3 GND4 GND5 GND6 GND7

21 CLK_G72M_27FIX
21 CLK_G72M_27SS
26 CLK_USB48
4 CPU_BSEL0
4 CPU_BSEL1
R125 33Ohm FSA
R126 2.2KOhm
23 CLK_TPMPCI
40 CLK_CBPCI
32 CLK_KBCPCI
30 CLK_SIOPCI
23,39,41 CLK_DBPCI
31 CLK_FWHPCI
25 CLK_ICHPCI
6,14,15,20,23,36,39,41 SCL_3S
6,14,15,20,23,36,39,41 SDA_3S
R128 39Ohm PCICLK5
R130 10KOhm
R131 33Ohm PCICLK4
R134 33Ohm PCICLK3
R136 33Ohm PCICLK2
R138 33Ohm
R139 10KOhm SELLCD_27#
R141 33Ohm
R143 33Ohm PCICLK0
R145 10KOhm
+3VS R891 10KOhm
C140 C141 C142 C143 C144 C145 C146 15PF/50V
R147 475Ohm

CPU_STOP# STP_CPU# 26
PCI/PCIEX_STOP# STP_PCI# 26
CLK_MCH CLK_MCH# 33Ohm R117 R118 CLK_MCH_BCLK 7 CLK_MCH_BCLK# 7
CLK_CPU CLK_CPU# 33Ohm R119 R120 CLK_CPU_BCLK 4 CLK_CPU_BCLK# 4
T459 T460
PEREQ1# PEREQ2# 10KOhm R123 R124 R939 0Ohm CLK_NEWCARD_REQ# 41
10KOhm R994 0Ohm CLK_MINICARD_REQ# 39
PCIE6 PCIE#6 R940 R941 33Ohm CLK_PCIE_NEWCARD 41 CLK_PCIE_NEWCARD# 41
PCIE5 PCIE#5 R127 R129 33Ohm CLK_PCIE_PEG 17 CLK_PCIE_PEG# 17
PCIE4 PCIE#4 R132 R133 33Ohm CLK_PCIE_LAN 37 CLK_PCIE_LAN# 37
PCIE3 PCIE#3 R135 R137 33Ohm CLK_MCH_3GPLL 8 CLK_MCH_3GPLL# 8
PCIE2 PCIE#2 R140 R142 33Ohm CLK_PCIE_ICH 25 CLK_PCIE_ICH# 25
PCIE1 PCIE#1 R144 R146 33Ohm CLK_PCIE_MINICARD 39 CLK_PCIE_MINICARD# 39
SATACLKT SATACLKC T75 T76
DOT96 DOT96# T77 T78
10KOhm R148 10KOhm R150
CLK_EN# CLK_EN# 47 R6395 442Ohm
REF1 REF0 R151 R153 2.2KOhm 10KOhm CPU_BSEL2 4 CLK_ICH14 26
10KOhm R154 CLK_SIO14 30 R6396 442Ohm

PEREQ1# R889 10KOhm +3VS
PEREQ2# R890 10KOhm

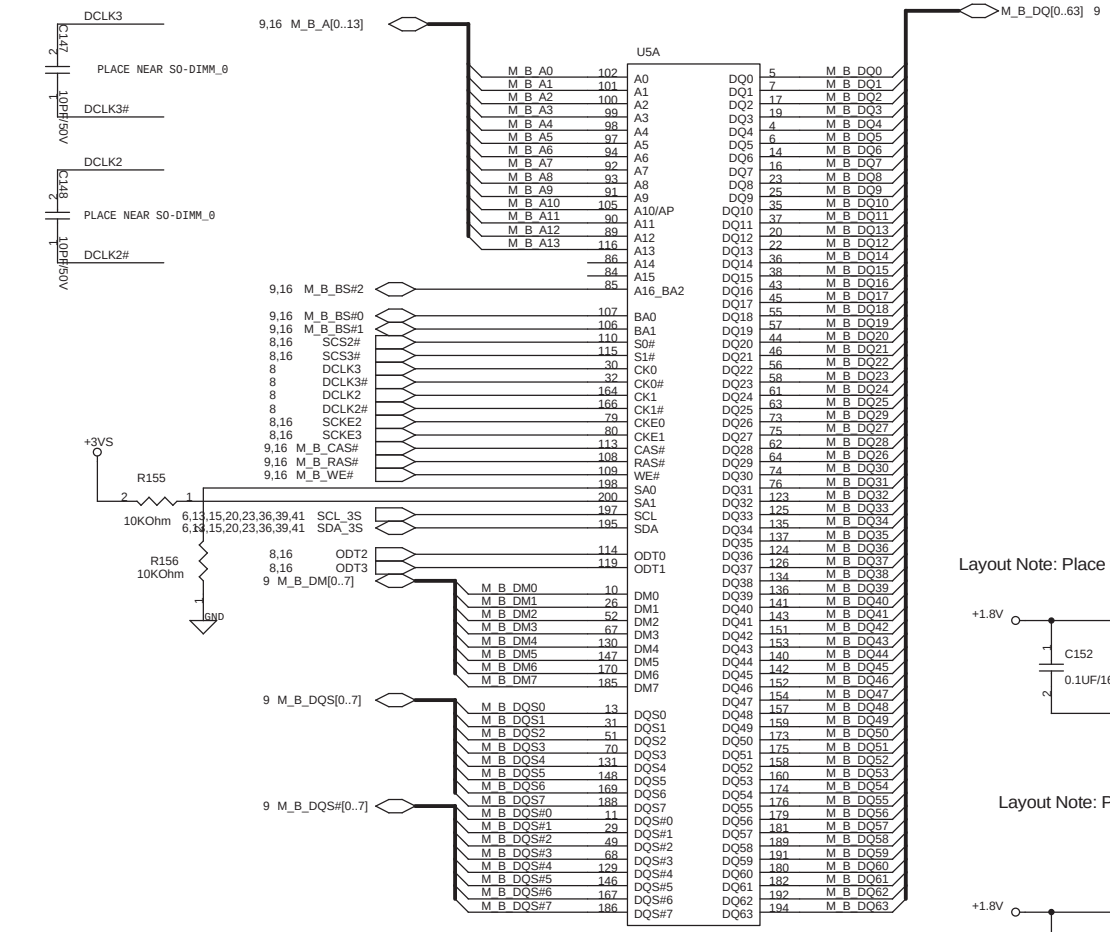
ICS 954310 FREQUENCY TABLE

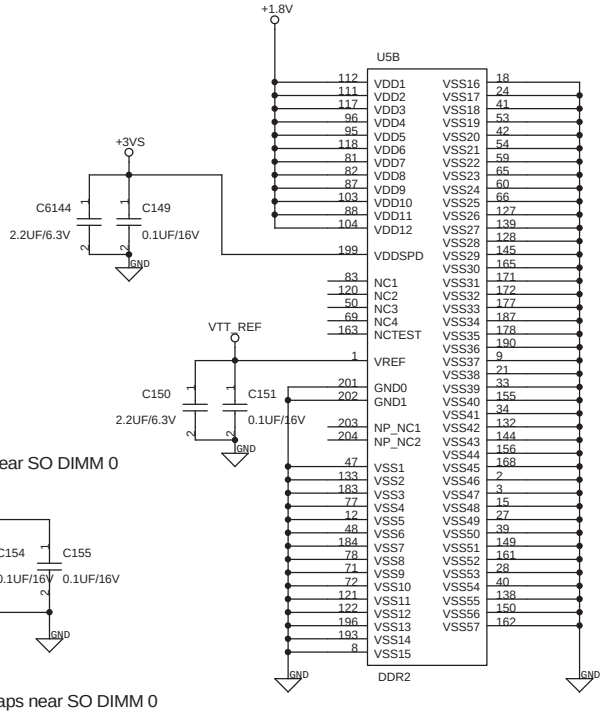
FS_C	FS_B	FS_A	CPU MHz	PCIE MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266	100	33.33	14.318	48.00	96.00
0	0	1	133	100	33.33	14.318	48.00	96.00
0	1	0	200	100	33.33	14.318	48.00	96.00
0	1	1	166	100	33.33	14.318	48.00	96.00
1	0	0	333	100	33.33	14.318	48.00	96.00
1	0	1	100	100	33.33	14.318	48.00	96.00
1	1	0	400	100	33.33	14.318	48.00	96.00
1	1	1	200	100	33.33	14.318	48.00	96.00

Internal Pull-Up
PIN 5,9,32,33,34
Internal Pull-Down
PIN 64

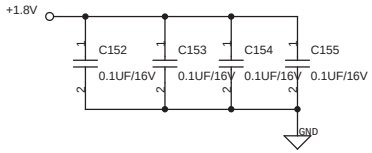
Pin9	Pin8	Pin17	Pin18
0	x	27FIX	27SS
1	0	96MSS_T	96MSS_C
1	1	PCIEX0T	PCIEX0C

PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: CLOCK GEN.	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 13 OF 63		RELEASE DATE :		

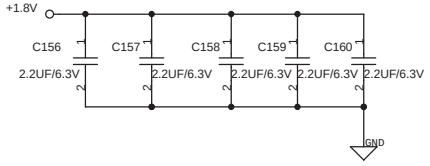




Layout Note: Place these Caps near SO DIMM 0

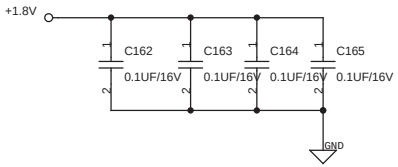


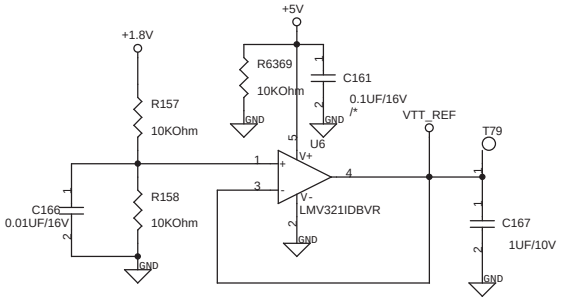
Layout Note: Place these Caps near SO DIMM 0



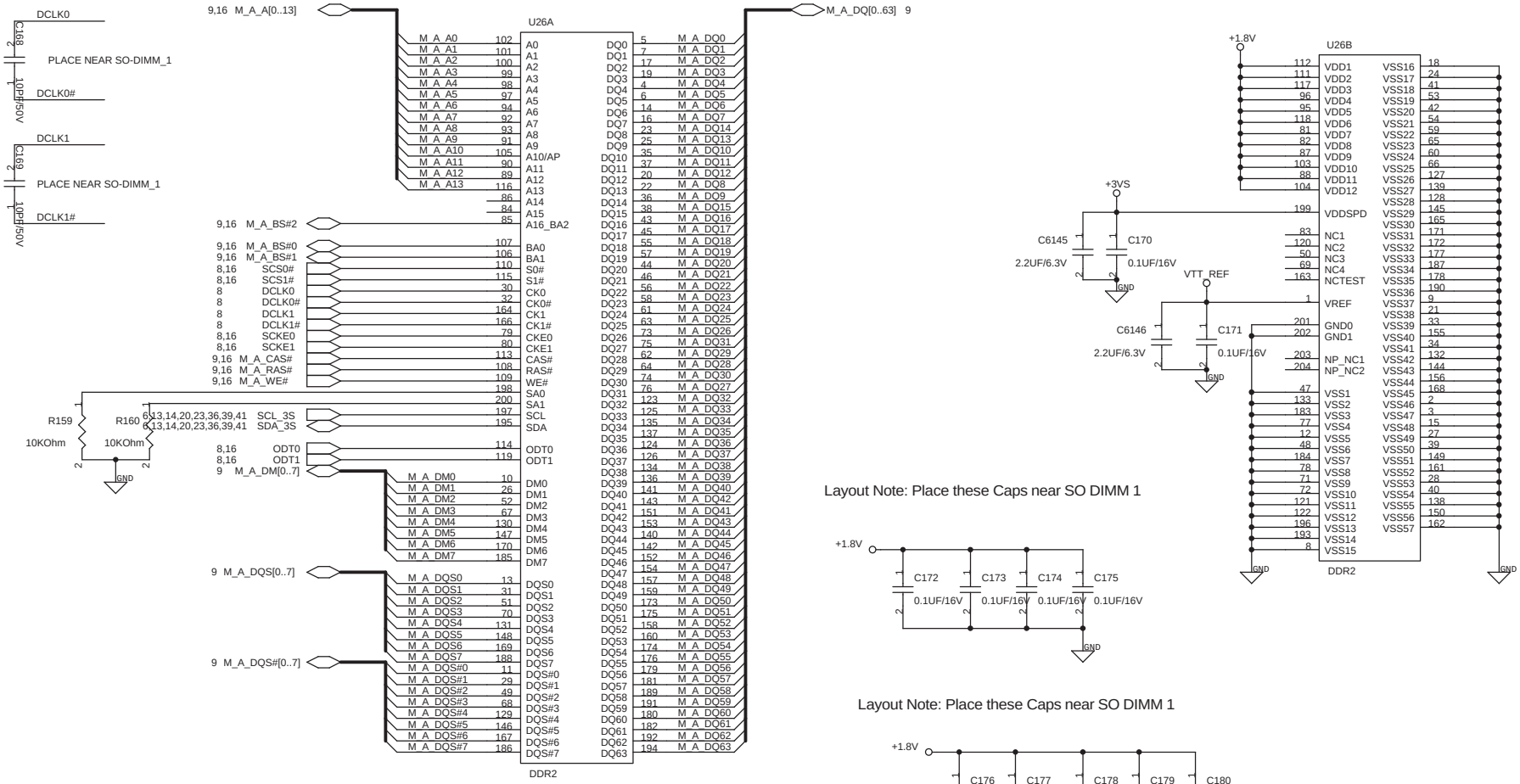
SO-DIMM Part is QUASAR
BOM is TYCO

Layout Note: Place these High-Freq decoupling Caps near the GMCH





PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***DDR2 SO-DIMM (1)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **14** OF **63**		RELEASE DATE :	

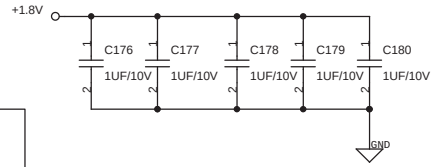


SO-DIMM Part is QUASAR
BOM is TYCO

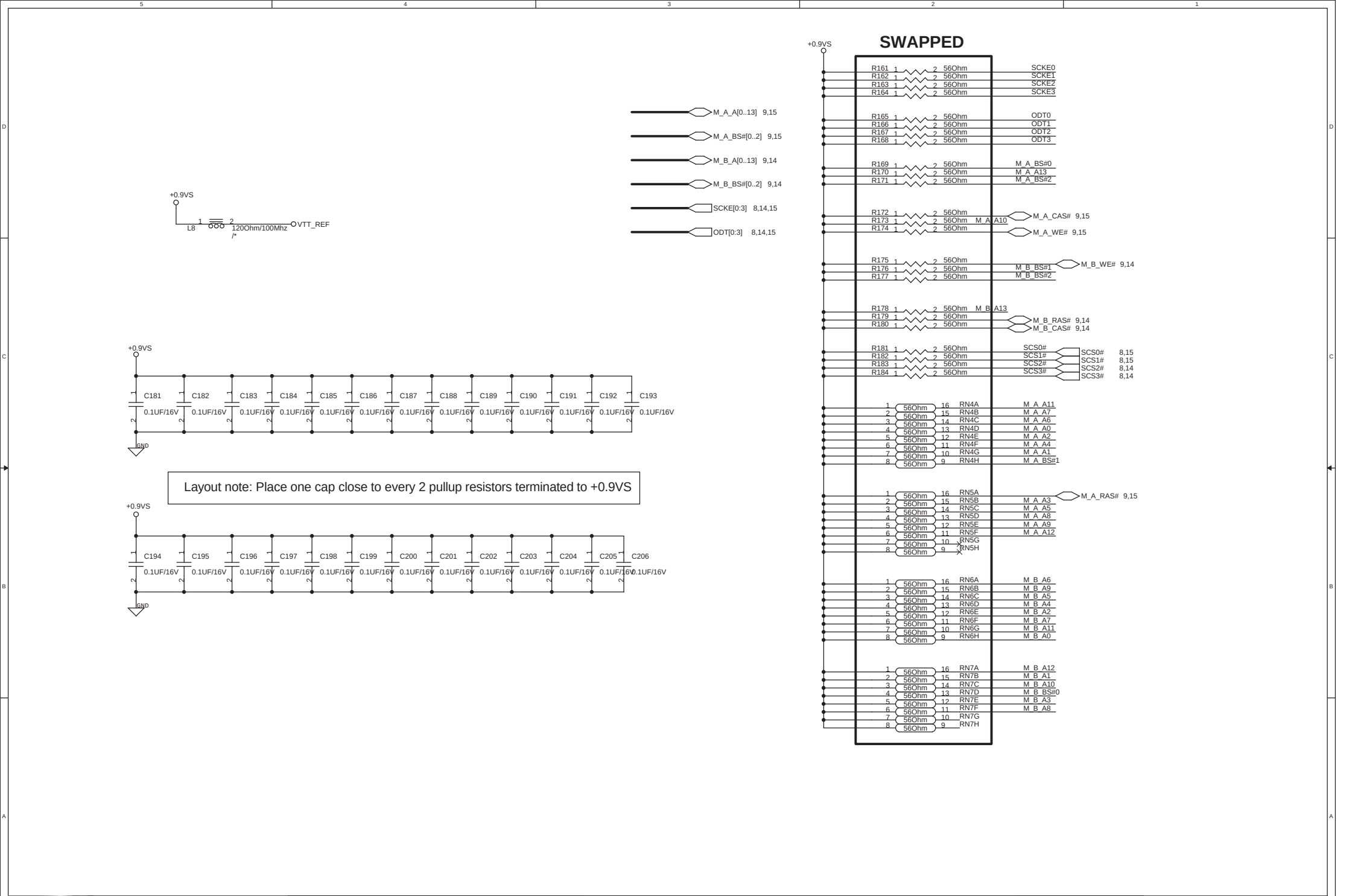
SO-DIMM 1 is placed farther
from the GMCH than SO-DIMM 0

Layout Note: Place these Caps near SO DIMM 1

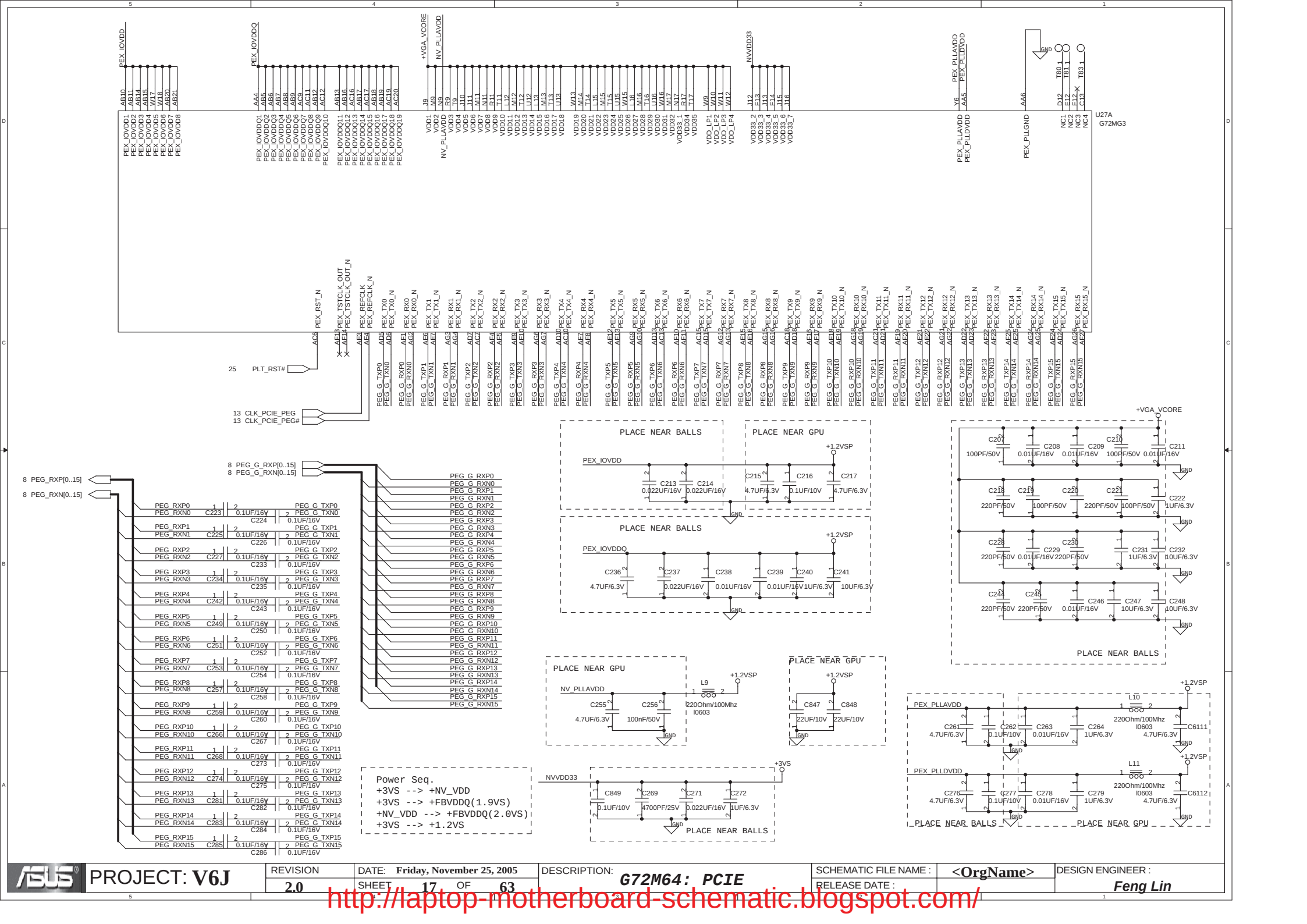
Layout Note: Place these Caps near SO DIMM 1



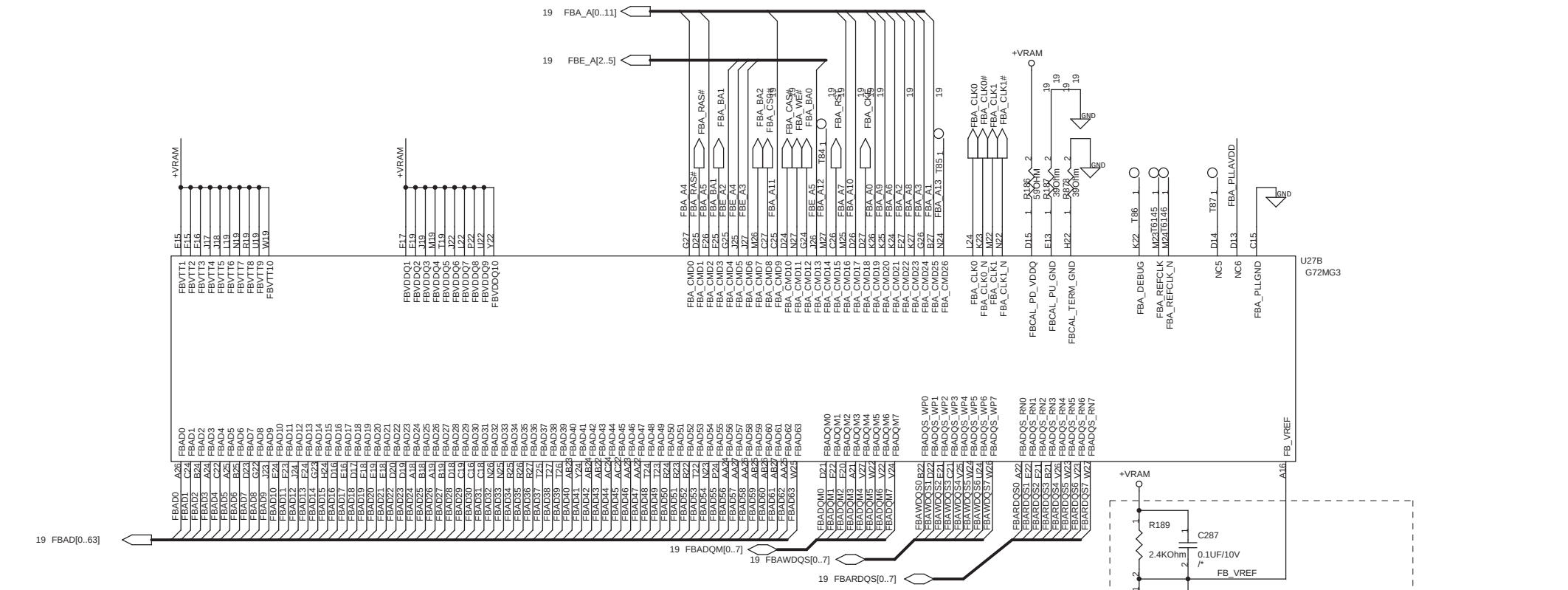
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **15** OF **63**	DESCRIPTION: ***DDR2 SO-DIMM (2)***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Feng Lin***



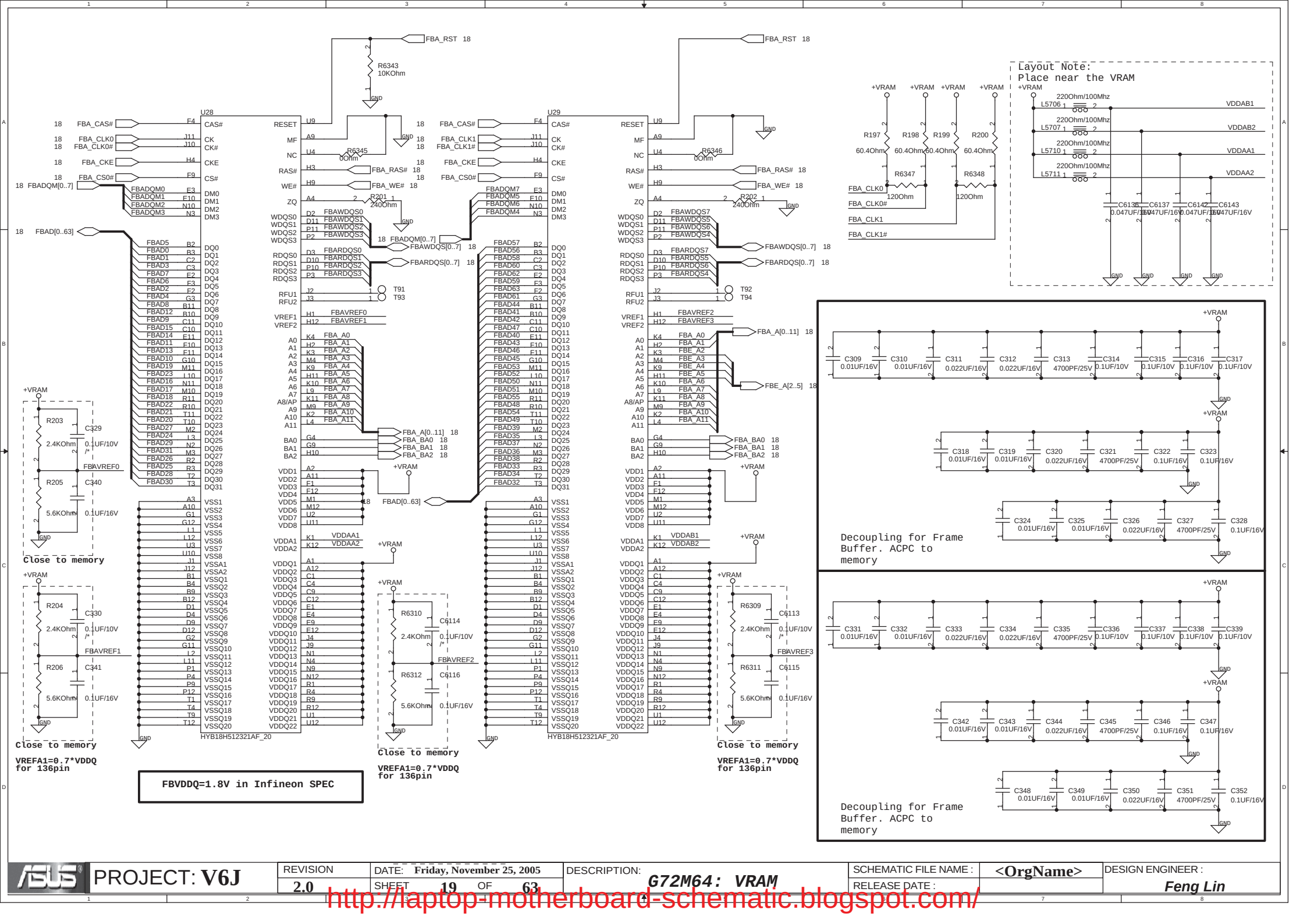
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **16** OF **63**	DESCRIPTION: ***DDR2 Res***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Feng Lin***



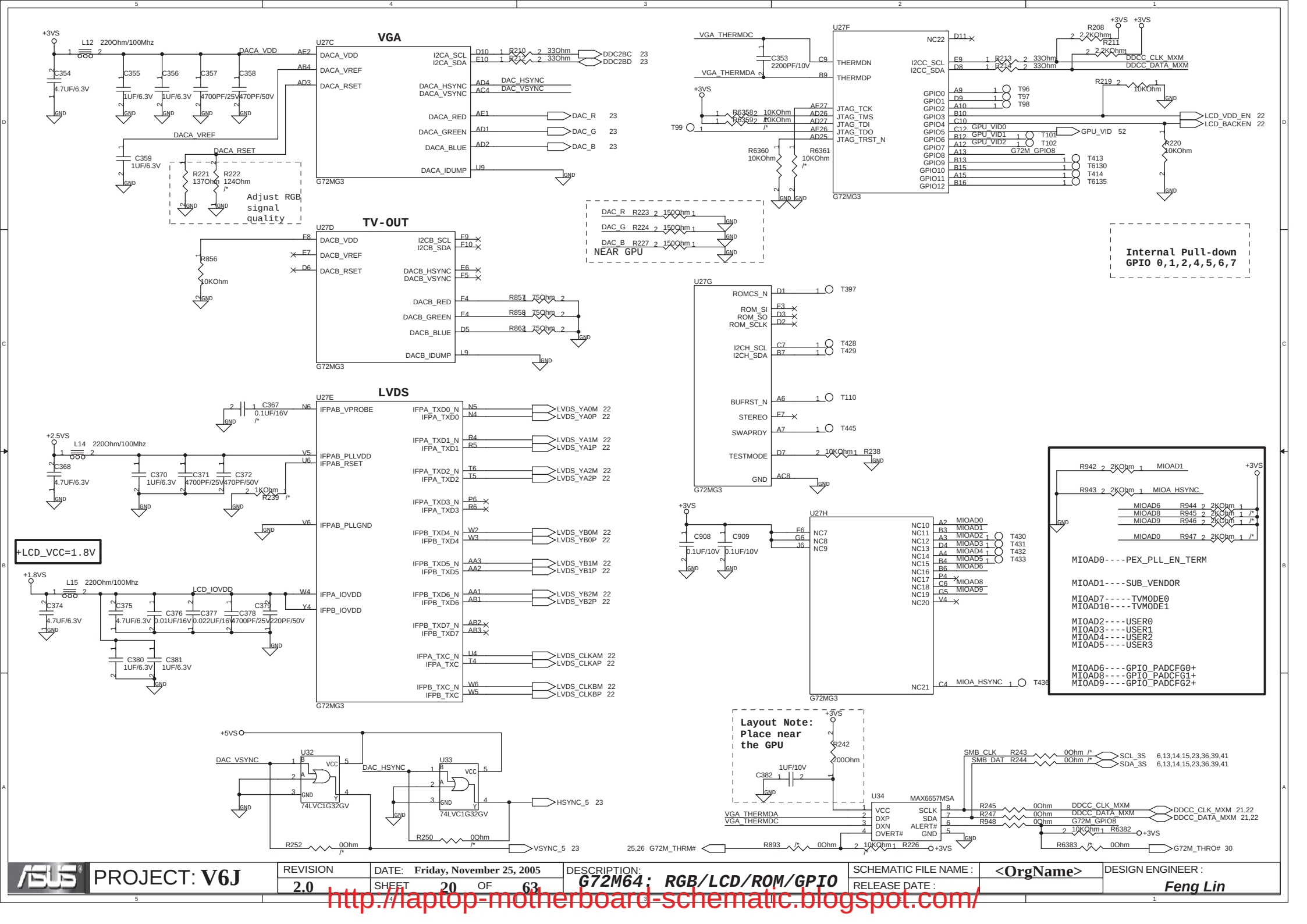
PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***G72M64: PCIE***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Feng Lin***
		SHEET **17** OF **63**		RELEASE DATE:	



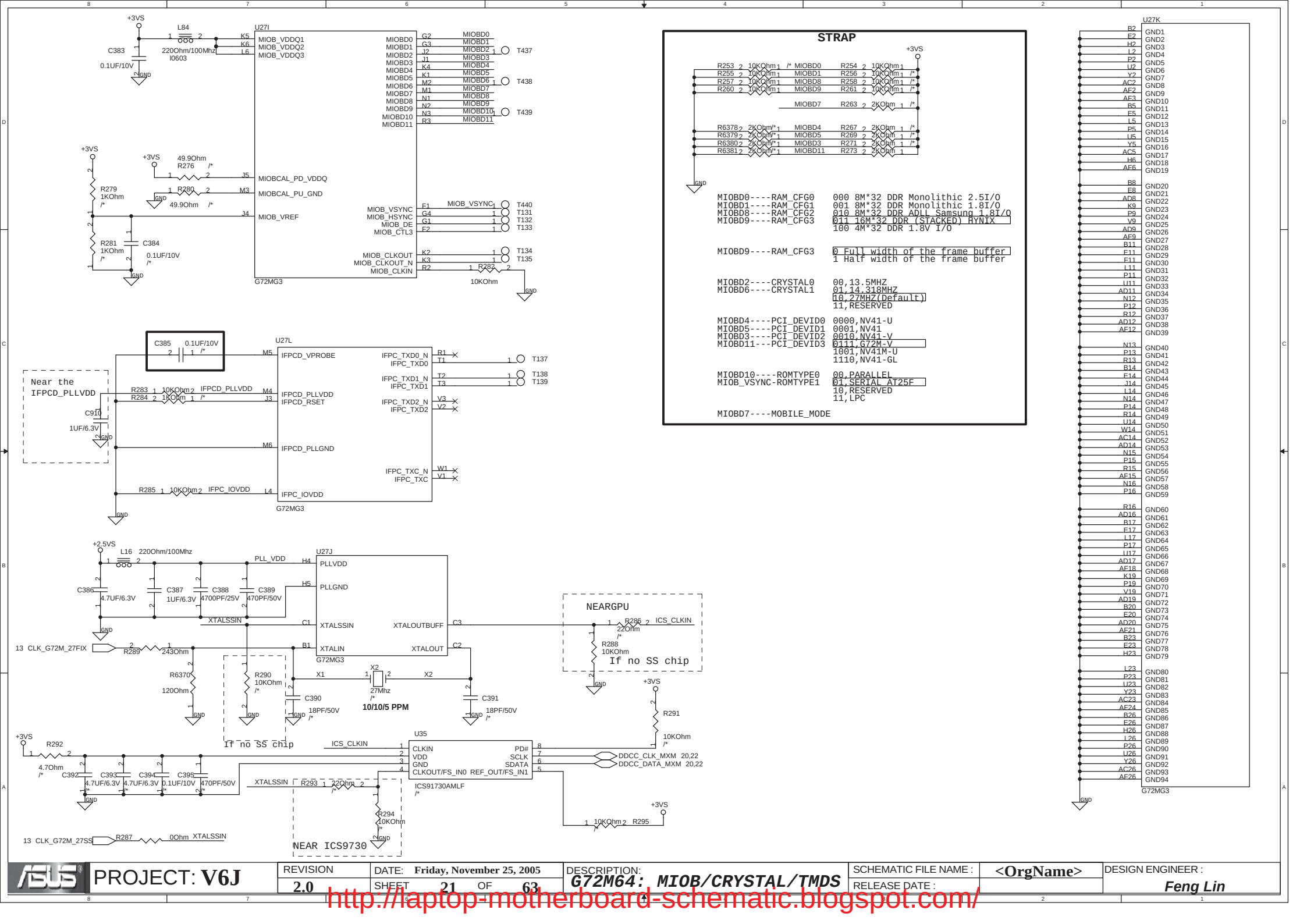
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: G72M64: FB	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 18 OF 63		RELEASE DATE :	



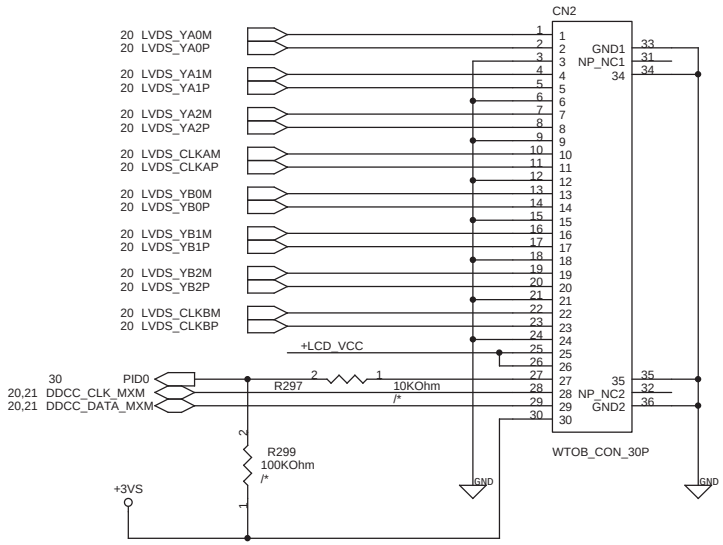
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: G72M64: VRAM	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 19 OF 63		RELEASE DATE :	

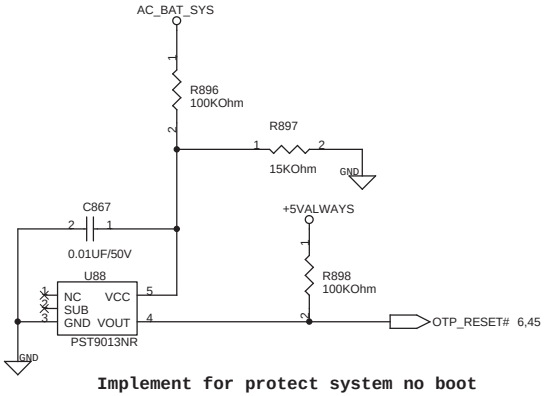


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***G72M64: RGB/LCD/ROM/GPIO***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **20** OF **63**		RELEASE DATE :	

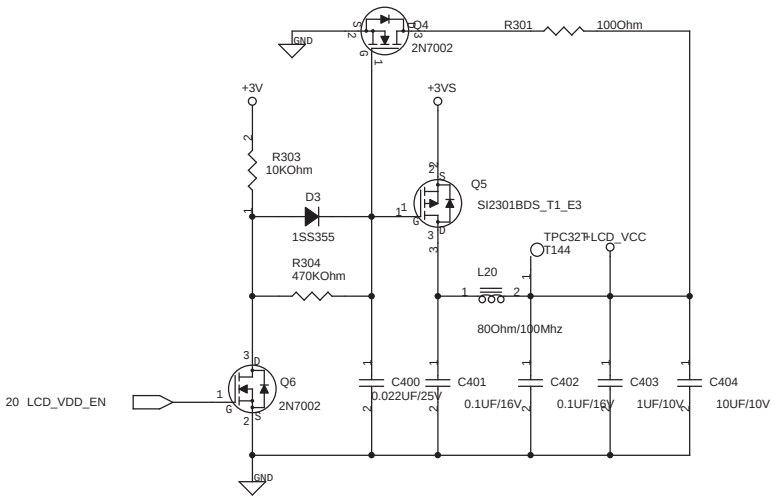


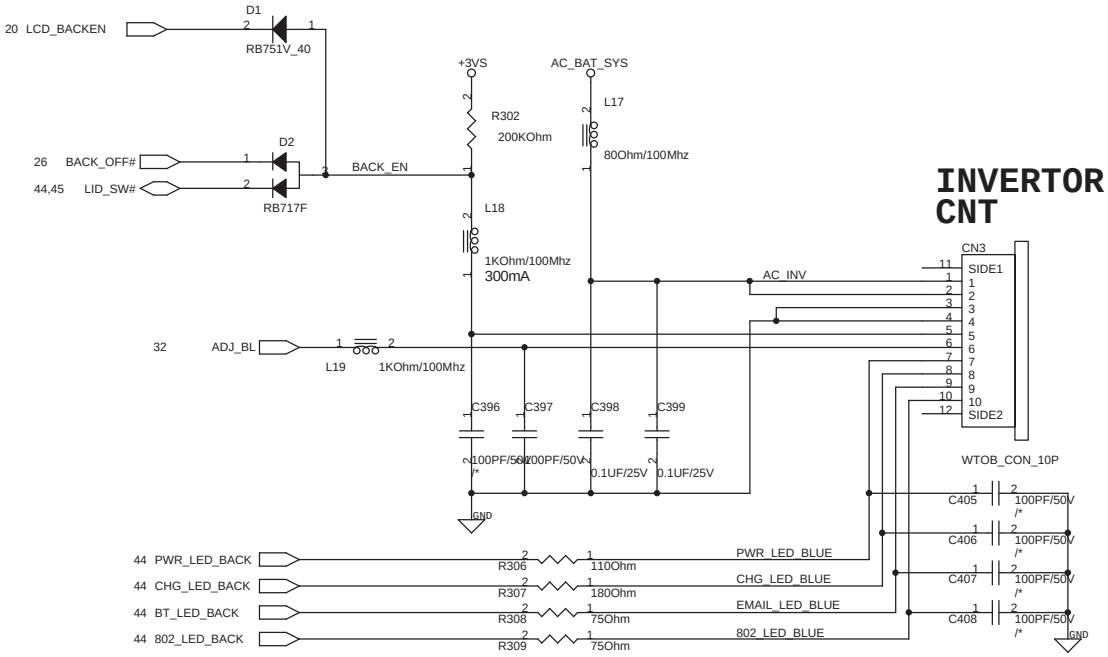
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: G72M64: MIOB/CRYSTAL/TMDS	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 21 OF 63		RELEASE DATE :	





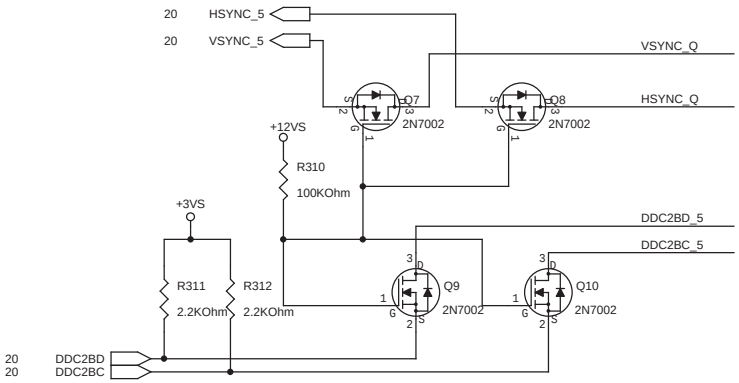
Implement for protect system no boot

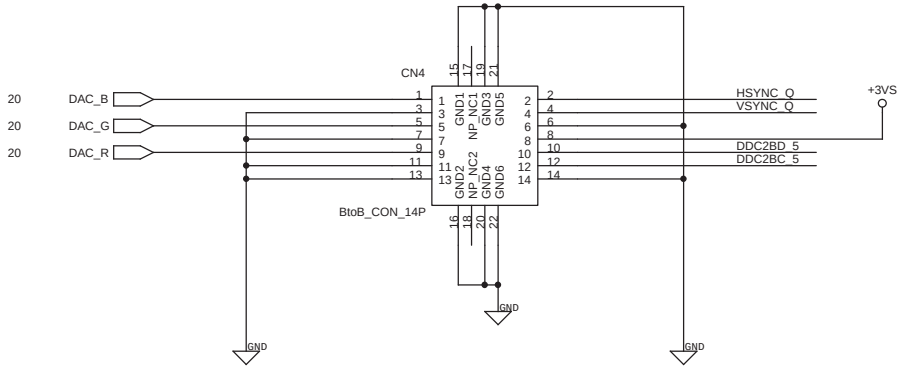


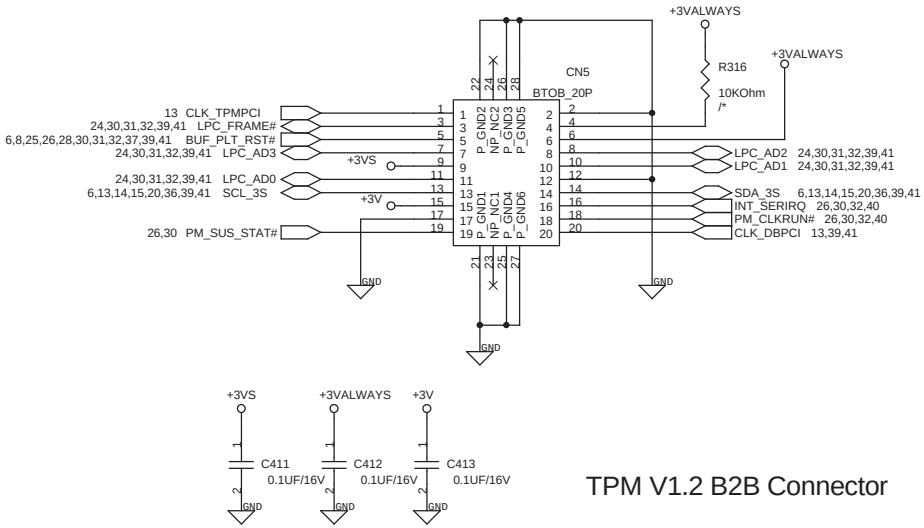


INVERTOR CNT

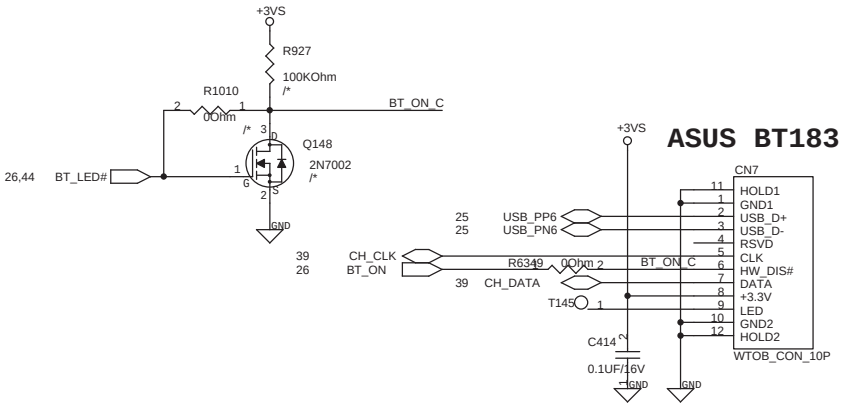
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***LVDS & INVERTER***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **22** OF **63**		RELEASE DATE :	





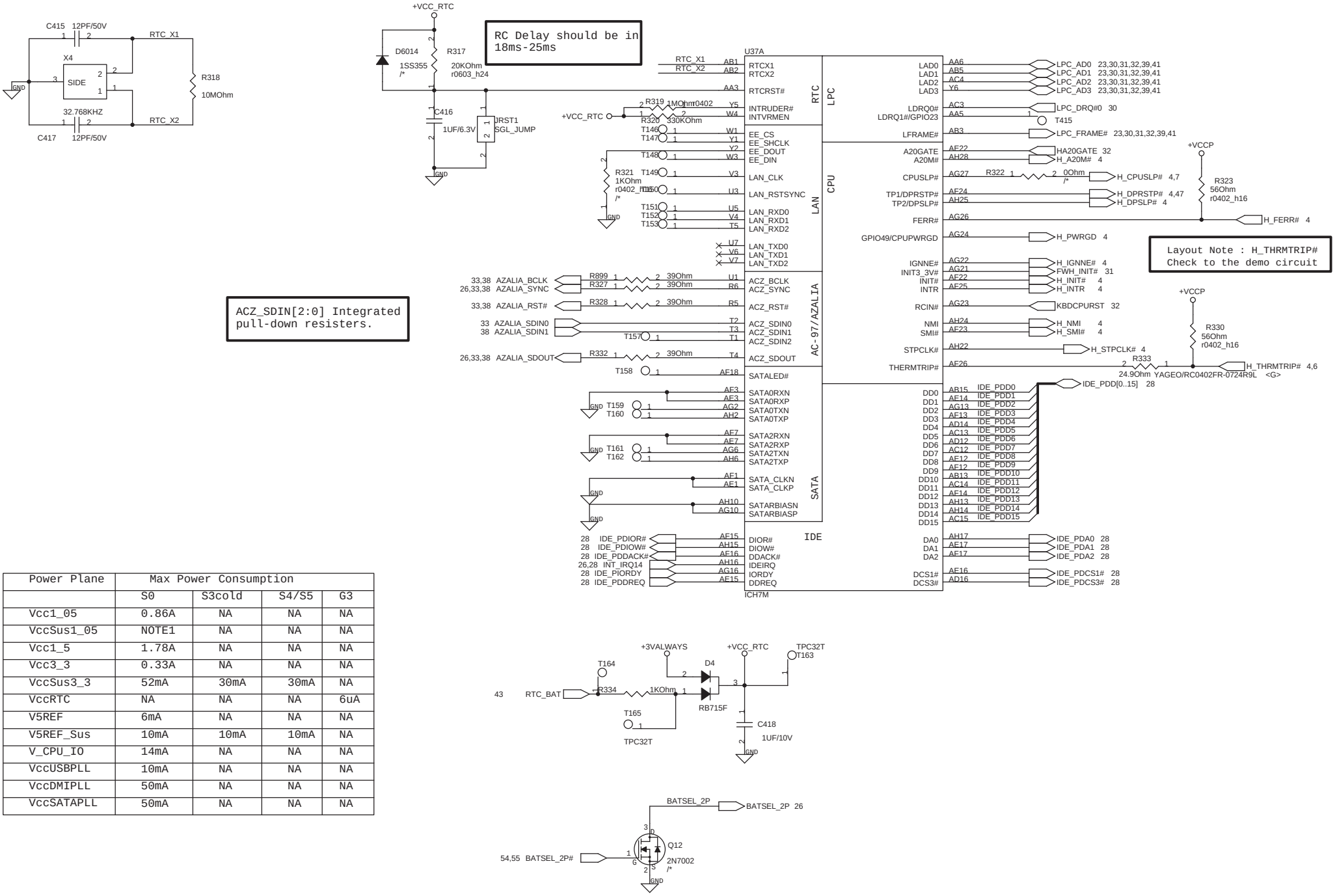


TPM V1.2 B2B Connector



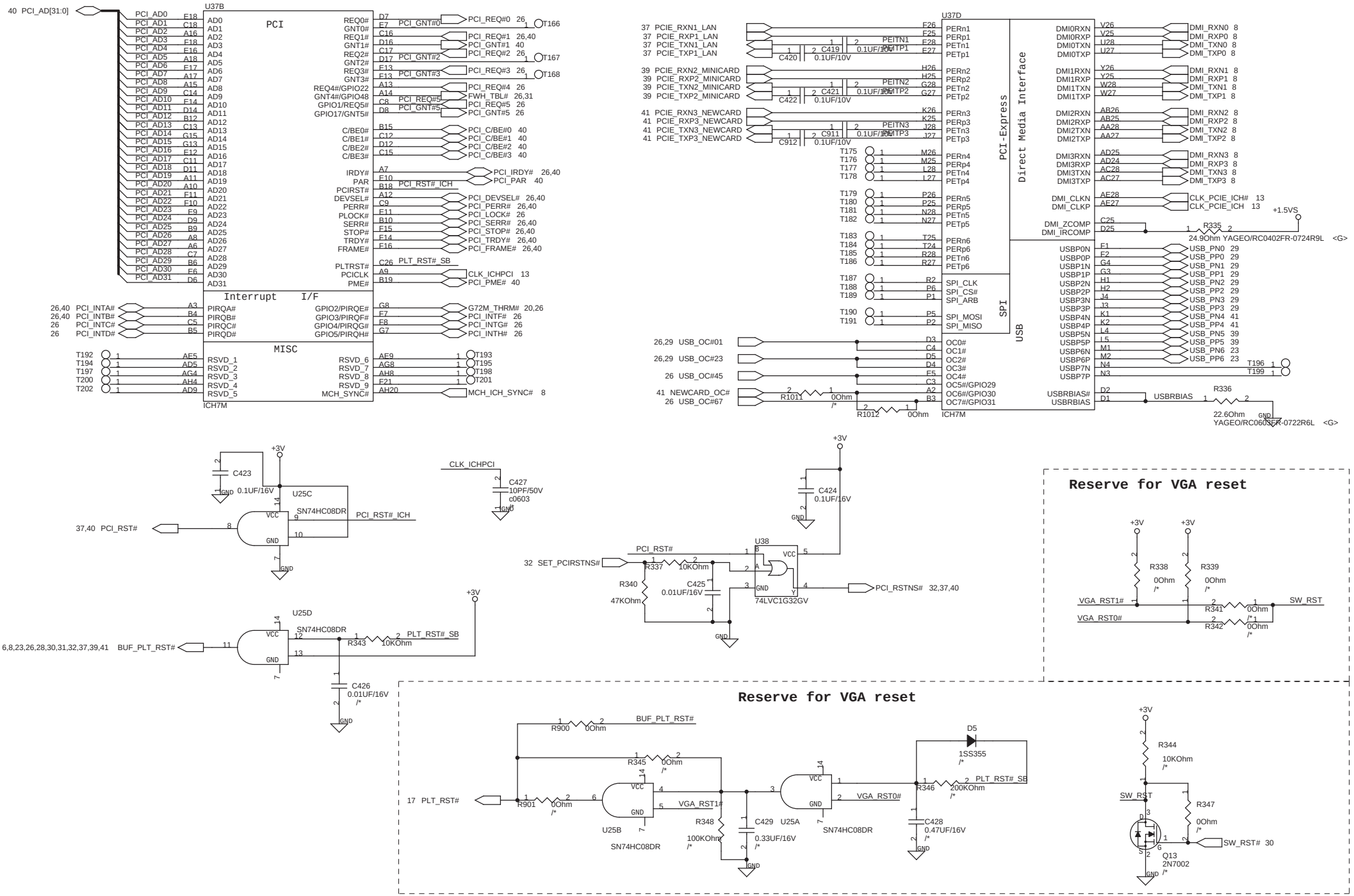
BT B2B Connector

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***CRT & TPM & BT***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **23** OF **63**		RELEASE DATE :	

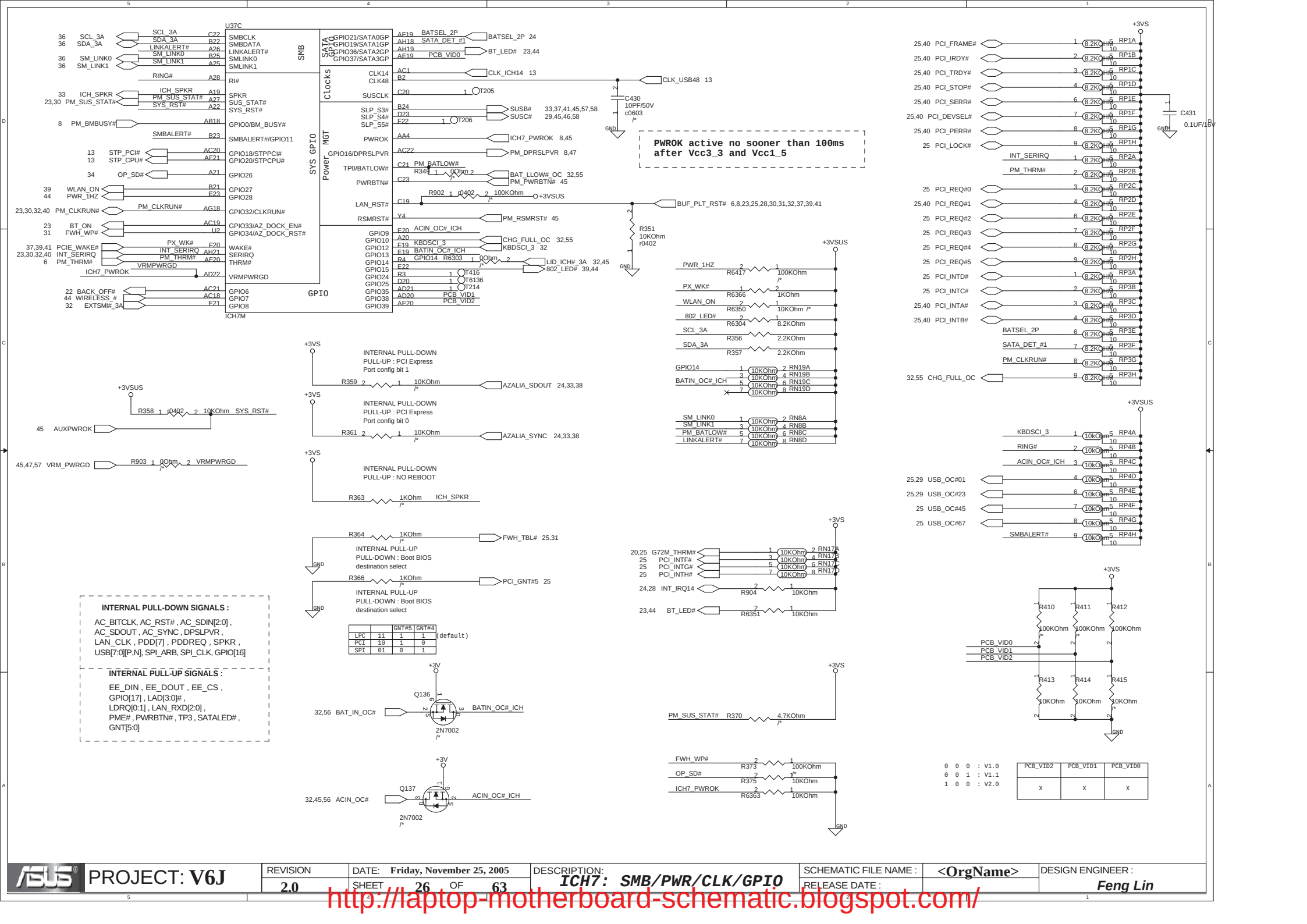


Power Plane	Max Power Consumption			
	S0	S3cold	S4/S5	G3
Vcc1_05	0.86A	NA	NA	NA
VccSus1_05	NOTE1	NA	NA	NA
Vcc1_5	1.78A	NA	NA	NA
Vcc3_3	0.33A	NA	NA	NA
VccSus3_3	52mA	30mA	30mA	NA
VccRTC	NA	NA	NA	6uA
V5REF	6mA	NA	NA	NA
V5REF_Sus	10mA	10mA	10mA	NA
V_CPU_IO	14mA	NA	NA	NA
VccUSBPLL	10mA	NA	NA	NA
VccDMIPLL	50mA	NA	NA	NA
VccSATAPLL	50mA	NA	NA	NA

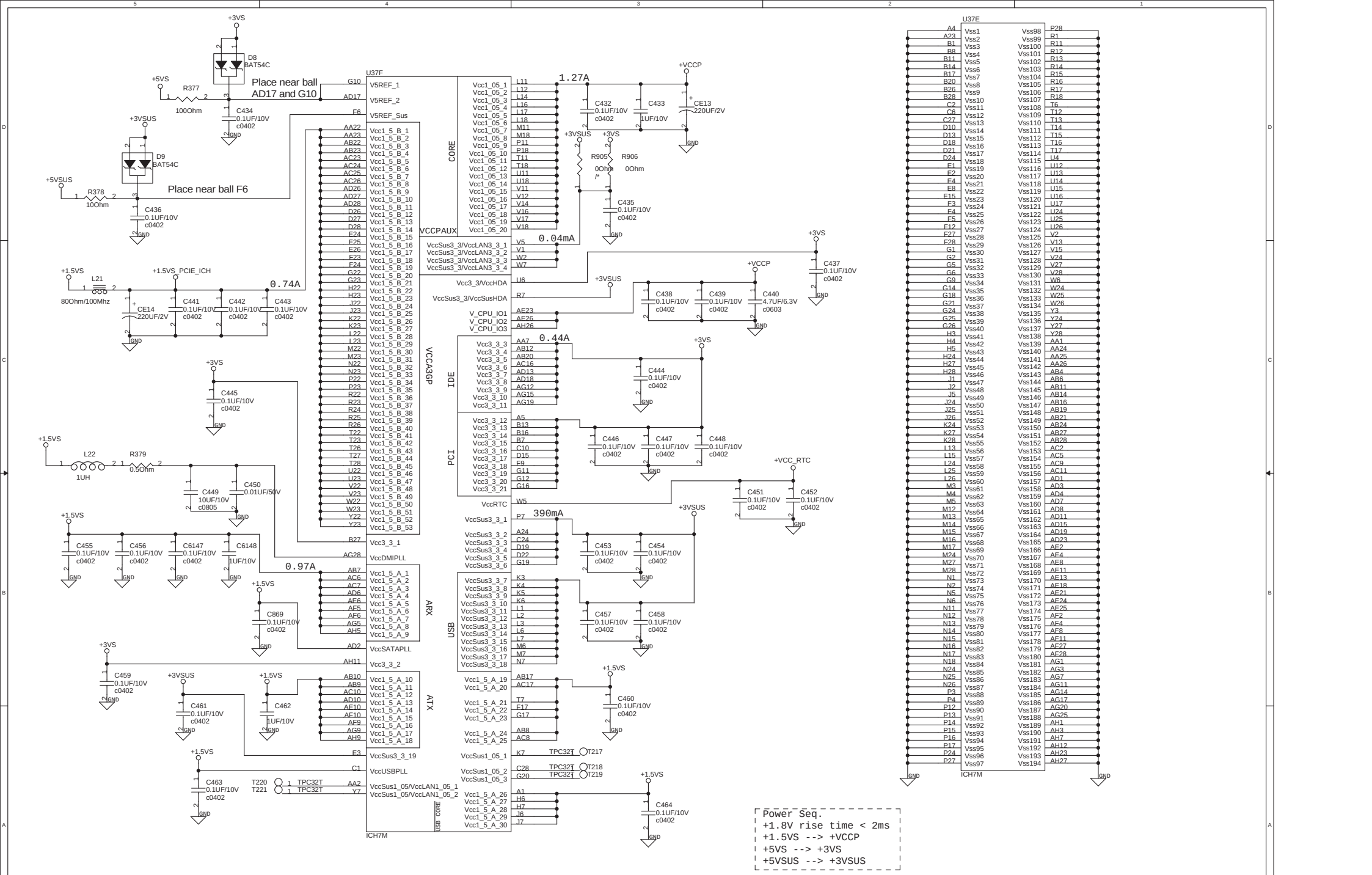
PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005** SHEET **24** OF **63**	DESCRIPTION: ***ICH7: IDE/AC97/LPC/RTC***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Feng Lin***



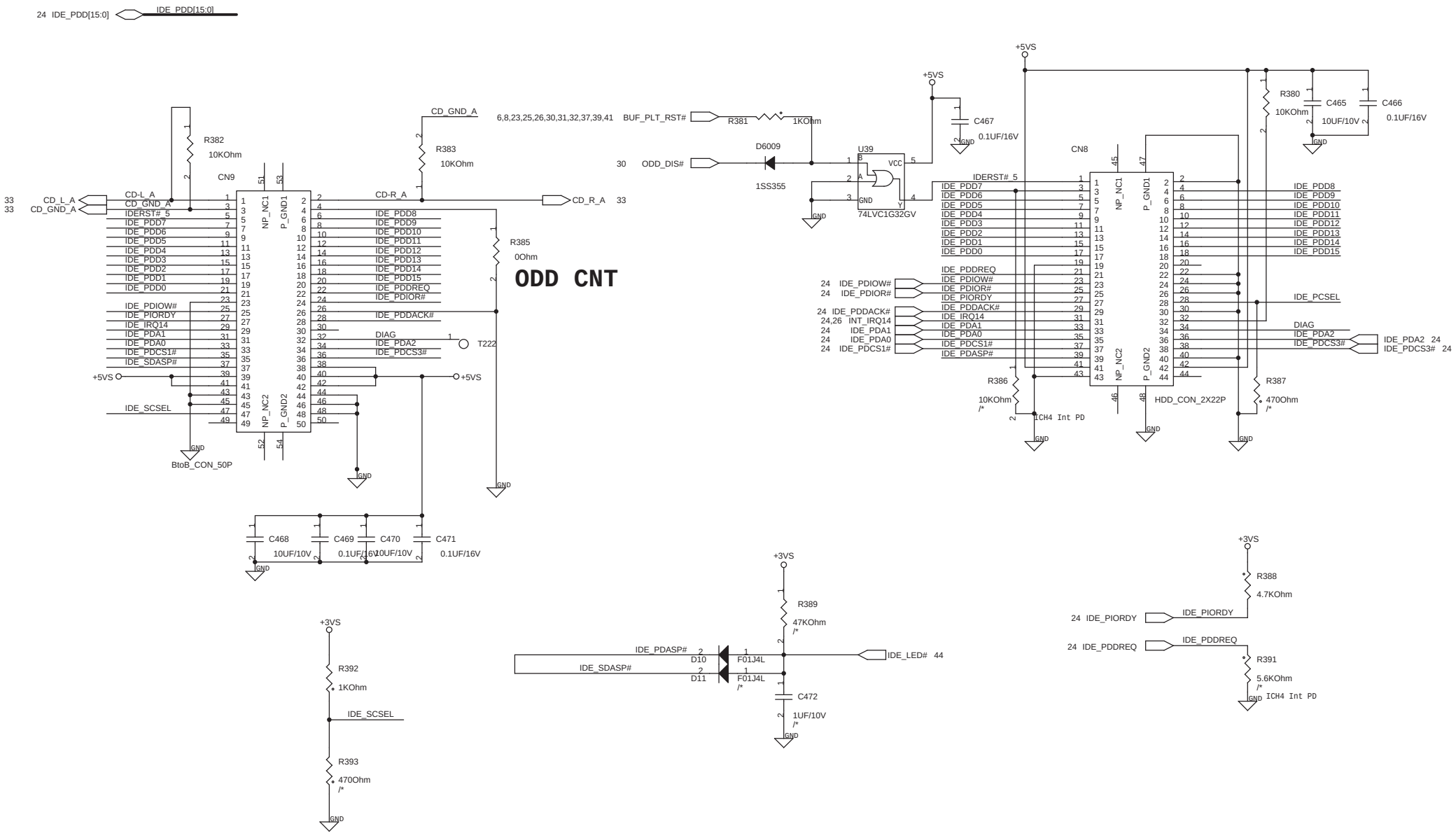
PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***ICH7: PCI/INT/DMI/USB***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Feng Lin***
		SHEET **25** OF **63**		RELEASE DATE:	



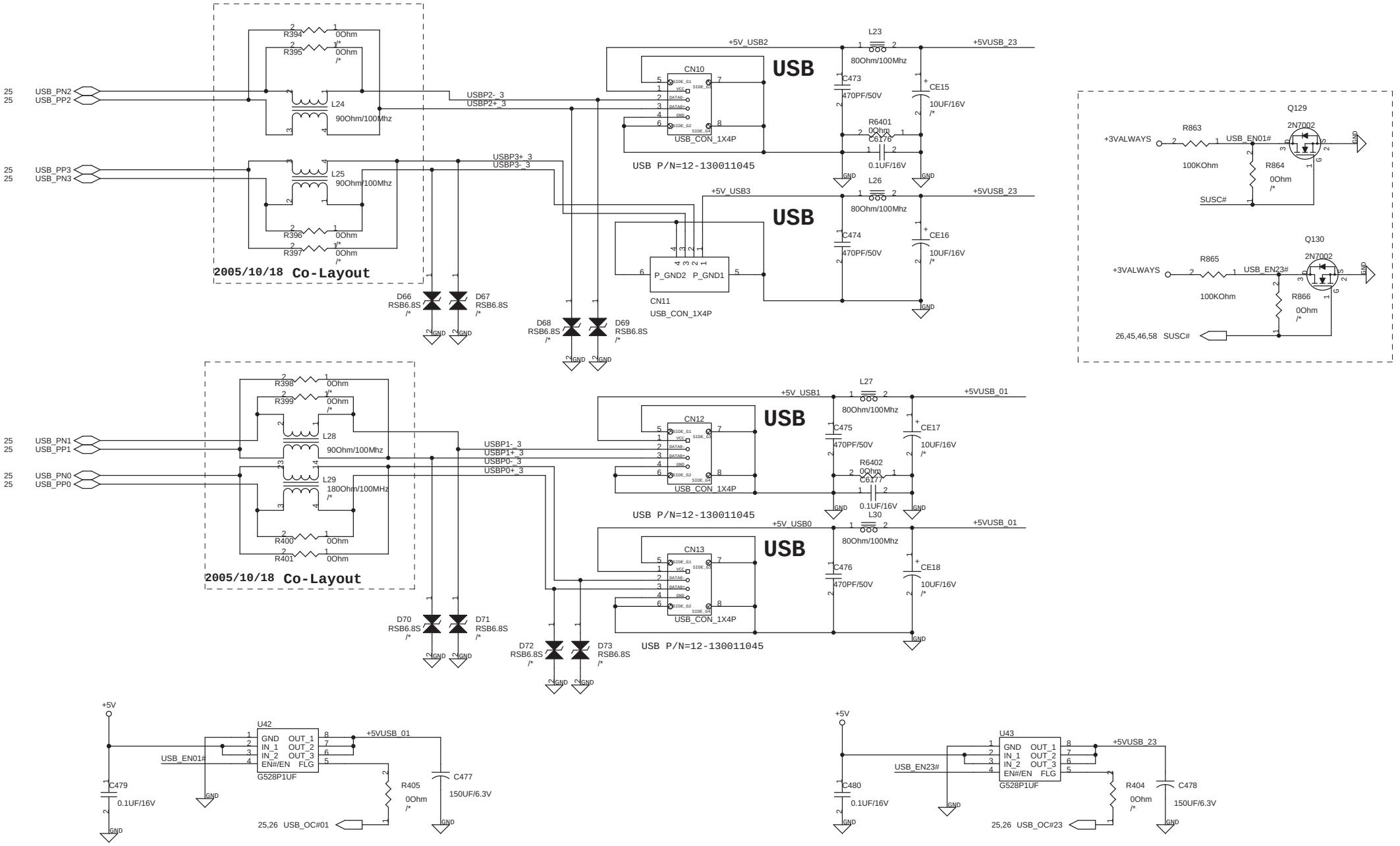
PROJECT: V6J	REVISION: 2.0	DATE: Friday, November 25, 2005	SHEET 26 OF 63
DESCRIPTION: ICH7: SMB/PWR/CLK/GPIO	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : Feng Lin



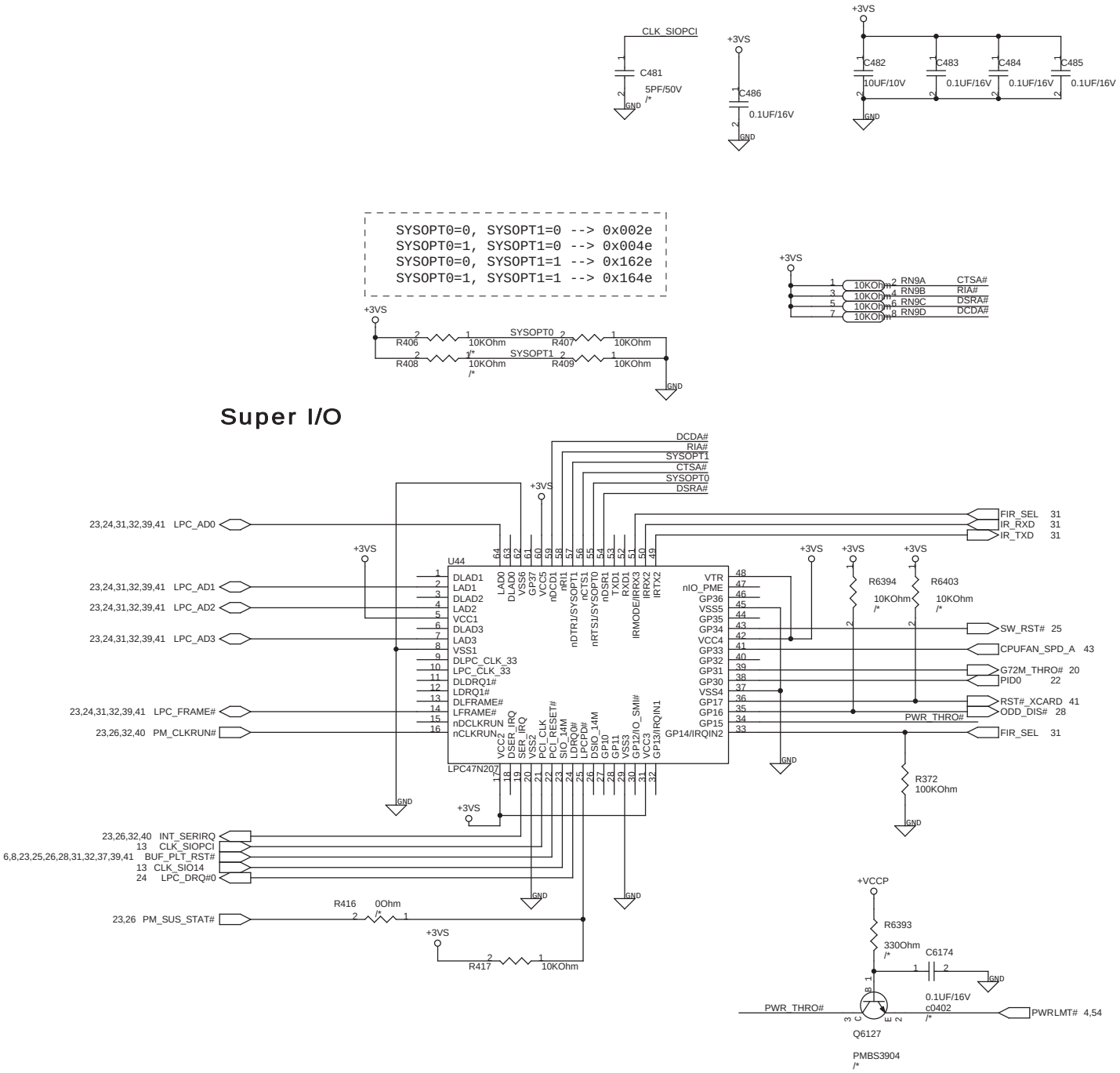
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: ICH7: PWR/Caps	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 27 OF 63		RELEASE DATE :	



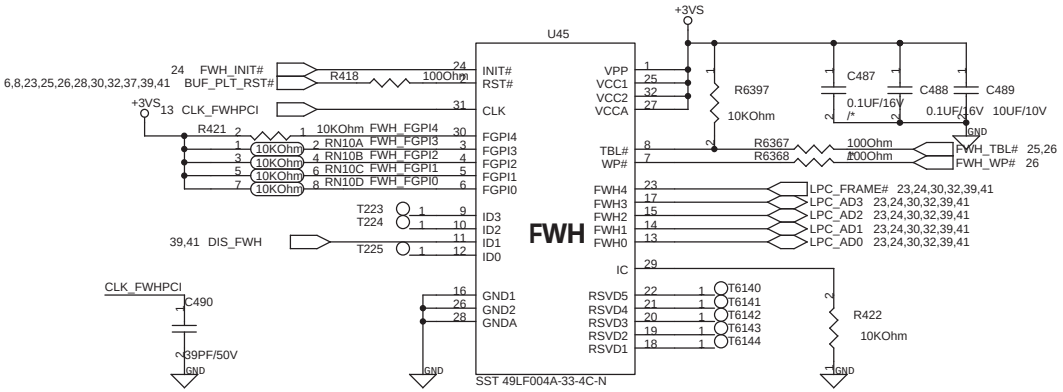
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***HDD & ODD CONN.***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **28** OF **63**		RELEASE DATE :	



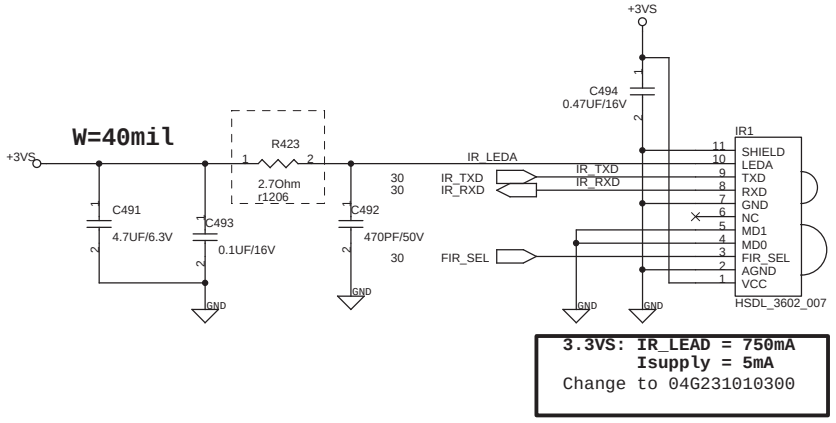
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***USB PORTS***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **29** OF **63**		RELEASE DATE :	



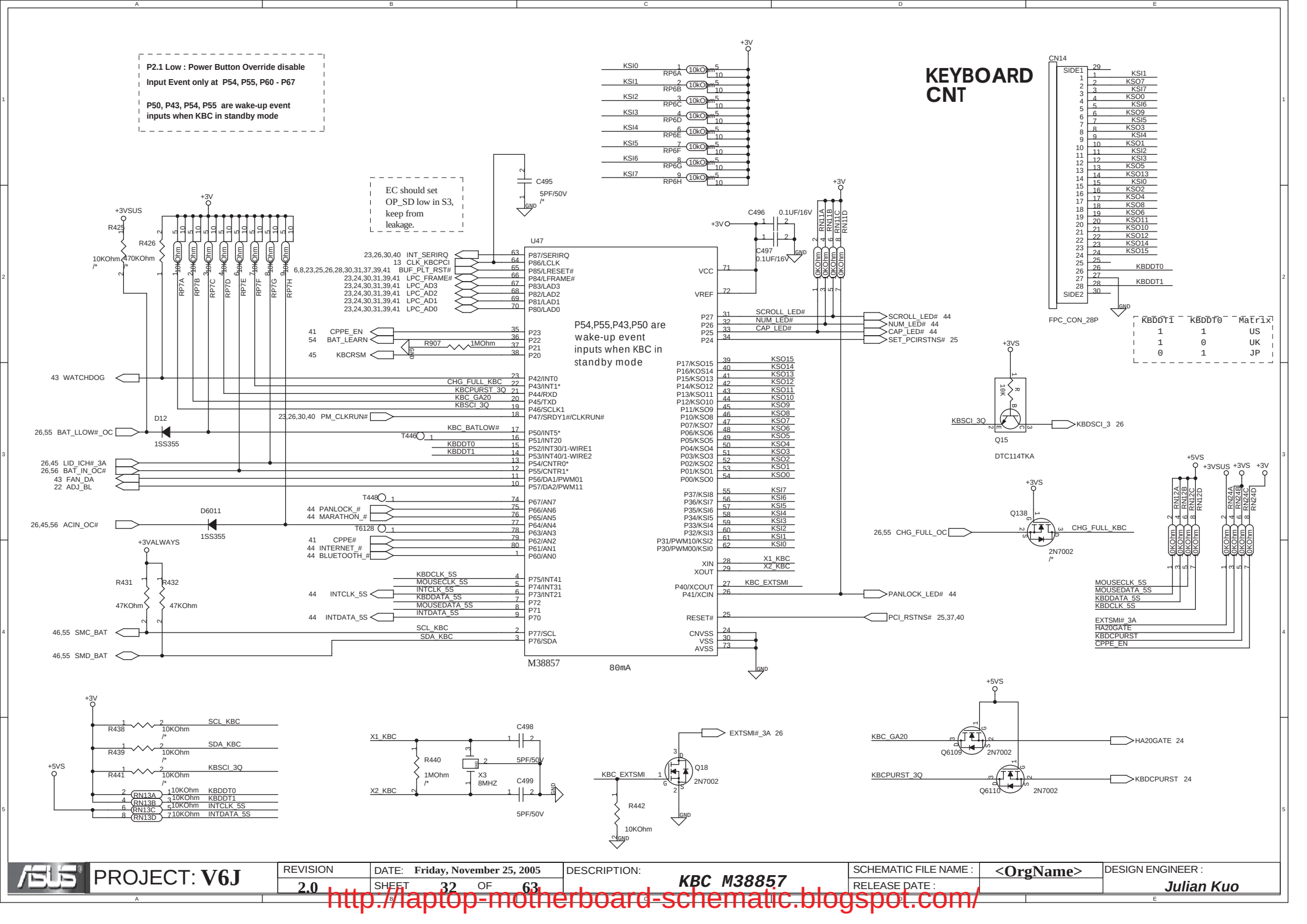
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***SUPER I/O 47N207***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **30** OF **63**		RELEASE DATE :	



PLCC32 Socket Part Number :
12G04300032F,12-043000321
,12-043000323,12-04300032J



PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: FIR & FWH	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Julian Kuo
		SHEET 31 OF 63		RELEASE DATE :	



PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: KBC M38857	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Julian Kuo
		SHEET 32 OF 63		RELEASE DATE :	

Internal pull low: SDATA-IN
Internal pull up: JD0, JD1, JD2, XTLSEL

Vo=Vref(=1.250)*(1+R428/R429) - G913C

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***AUDIO AD1986***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **33** OF **63**		RELEASE DATE :	

AUDIO OUT AMP

Change to 12-140111081-TYCO

HEADPHONE/ SPDIF

OPTIC_HP#	JACK_IN#	STATE
0	0	LINE_OUT : OPTIC VCC OFF
1	0	SPDIF_OUT : OPTIC VCC ON
1	1	NC : OPTIC VCC OFF

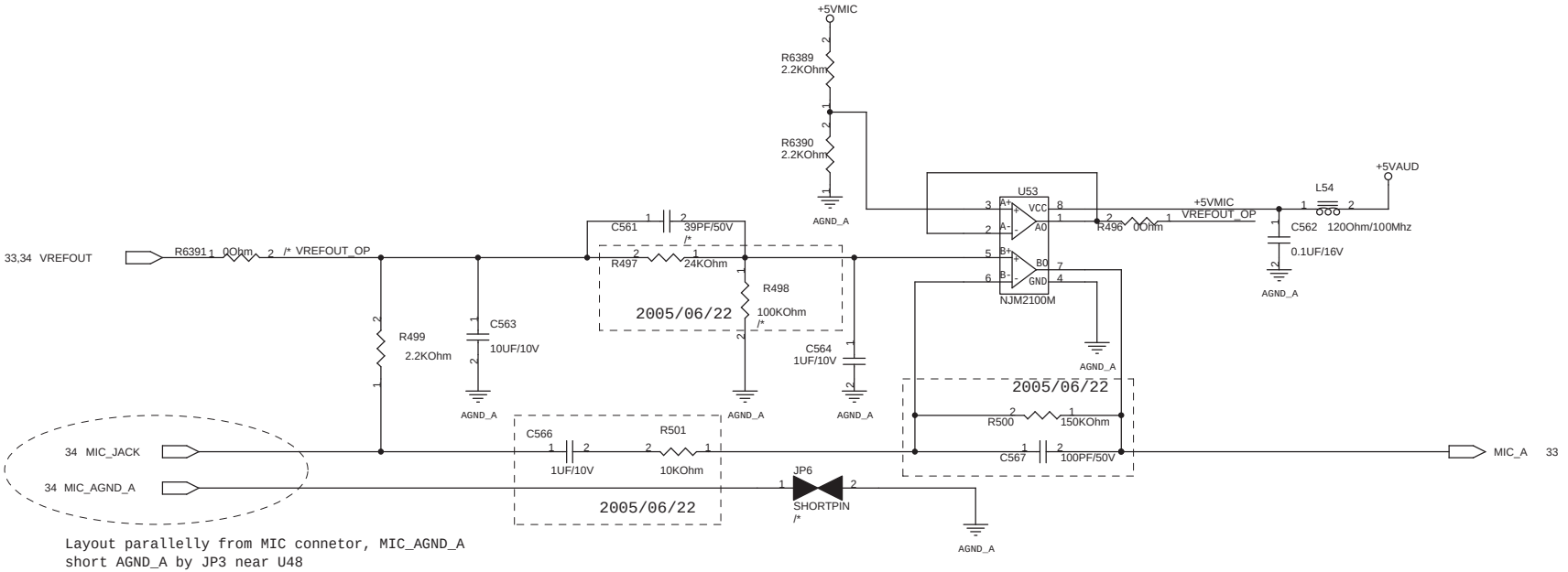
CN28 P/N=12-140001087
12-140001088

MIC

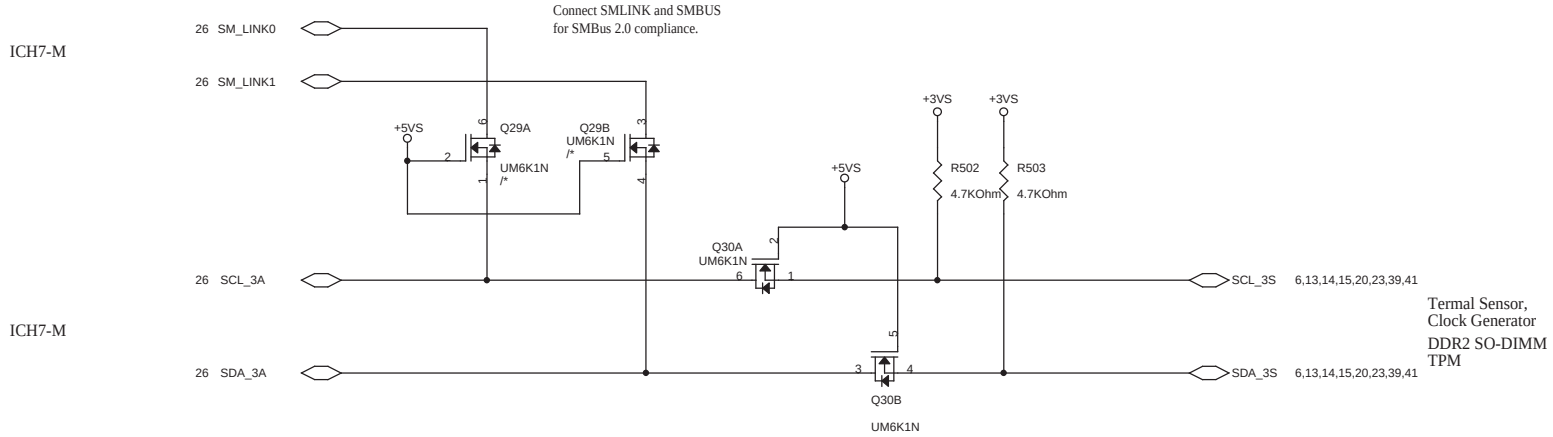
INTERNAL SPEAKER CNT

INTERNAL MIC CNT

PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: AUDIO AMP & JACKS	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 34 OF 63		RELEASE DATE :	



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***MIC AMP***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **35** OF **63**		RELEASE DATE :	



YONAH

+VCCP	+VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+VCORE	+VCORE	5,6,46,47
+1.5VS	+1.5VS	5,8,10,11,25,27,39,41,46,49

Calistoga

+VCCP	+VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+1.5VS	+1.5VS	5,8,10,11,25,27,39,41,46,49
+3VS	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+1.8VS	+1.8VS	20,46,58
VTT_REF	VTT_REF	8,14,15,16
+2.5VS	+2.5VS	10,20,21,46,51
+1.8V	+1.8V	8,11,14,15,46,50

G72M G3-64

+VGA_VCORE	+VGA_VCORE	17,46,52
+1.2VSP	+1.2VSP	17,18,46,53
+3VS	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+VRAM	+VRAM	18,19,46,52
+2.5VS	+2.5VS	10,20,21,46,51
+1.8VS	+1.8VS	20,46,58
+5VS	+5VS	20,27,28,32,34,39,43,44,45,46,47,58

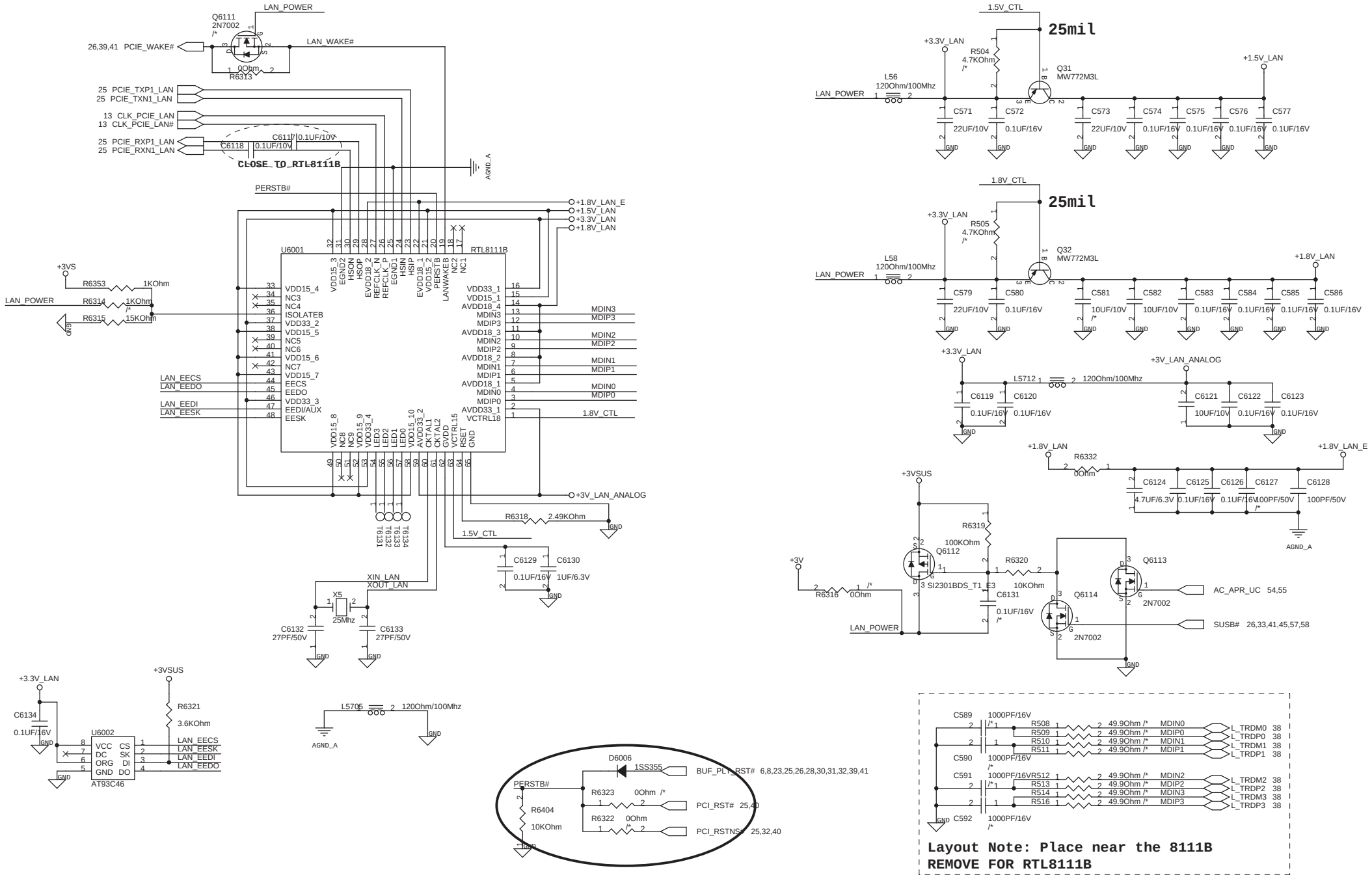
ICH7

+VCC_RTC	+VCC_RTC	24,27
+VCCP	+VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+3V	+3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+1.5VS	+1.5VS	5,8,10,11,25,27,39,41,46,49
+3VSUS	+3VSUS	26,27,32,37,41,45,48
+5VSUS	+5VSUS	27,44,48

+3VALWAYS	+3VALWAYS	23,24,29,32,44,45,46,51,60
+3VSUS	+3VSUS	26,27,32,37,41,45,48
+5VALWAYS	+5VALWAYS	22,48,51,54
+5VSUS	+5VSUS	27,44,48
+3V	+3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+5V	+5V	14,29,33,41,44,46,56,58
+12V	+12V	34,42,58
+3VS	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+5VS	+5VS	20,27,28,32,34,39,43,44,45,46,47,58
+12VS	+12VS	23,44,58
VTT_REF	VTT_REF	8,14,15,16
+2.5VS	+2.5VS	10,20,21,46,51
+1.8VS	+1.8VS	20,46,58
+0.9VS	+0.9VS	16,50
+1.5VS	+1.5VS	5,8,10,11,25,27,39,41,46,49
+VCC_RTC	+VCC_RTC	24,27
+1.8V	+1.8V	8,11,14,15,46,50
+3VA	+3VALWAYS	23,24,29,32,44,45,46,51,60
+5VA	+5VALWAYS	22,48,51,54
+5VAUD	+5VAUD	33,34,35
VTT_REF	VTT_REF	8,14,15,16
A/D_DOCK_IN	A/D_DOCK_IN	43,54,56,57
+3VSUS_PE	+3VSUS_PE	41
+3VS_PE	+3VS_PE	41
+1.5VS_PE	+1.5VS_PE	41

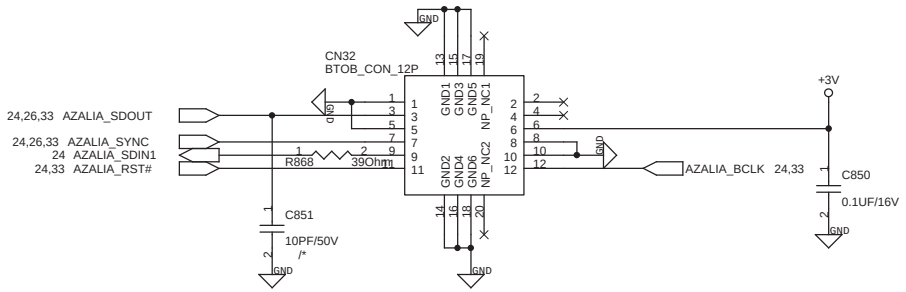
NEWCARD

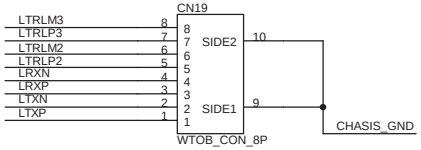
PROJECT: V6J	REVISION	DATE: Friday, November 25, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	2.0	SHEET 36 OF 63	SMBUS	RELEASE DATE :		Julian Kuo



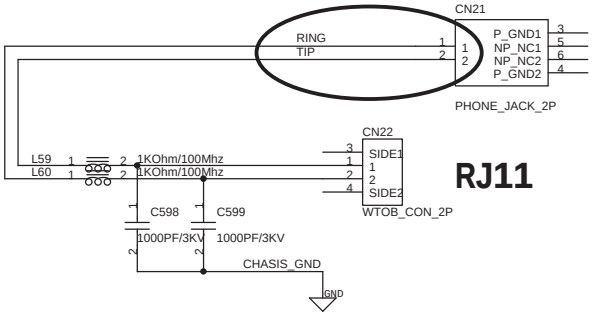
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: LAN_RTL8111B	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 37 OF 63		RELEASE DATE :	

MDC CNT

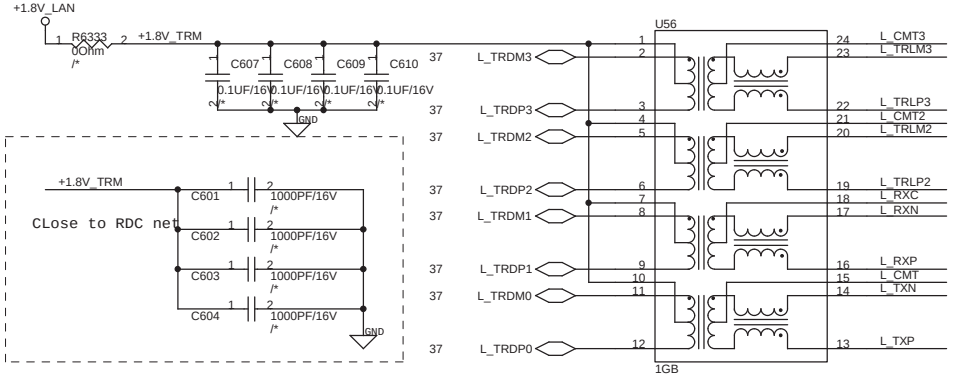




RJ45



RJ11

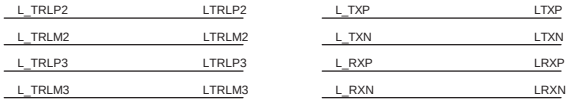


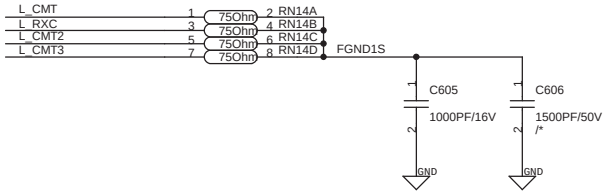
Change to LFE9209A

09-051023007 is BOTHHAND

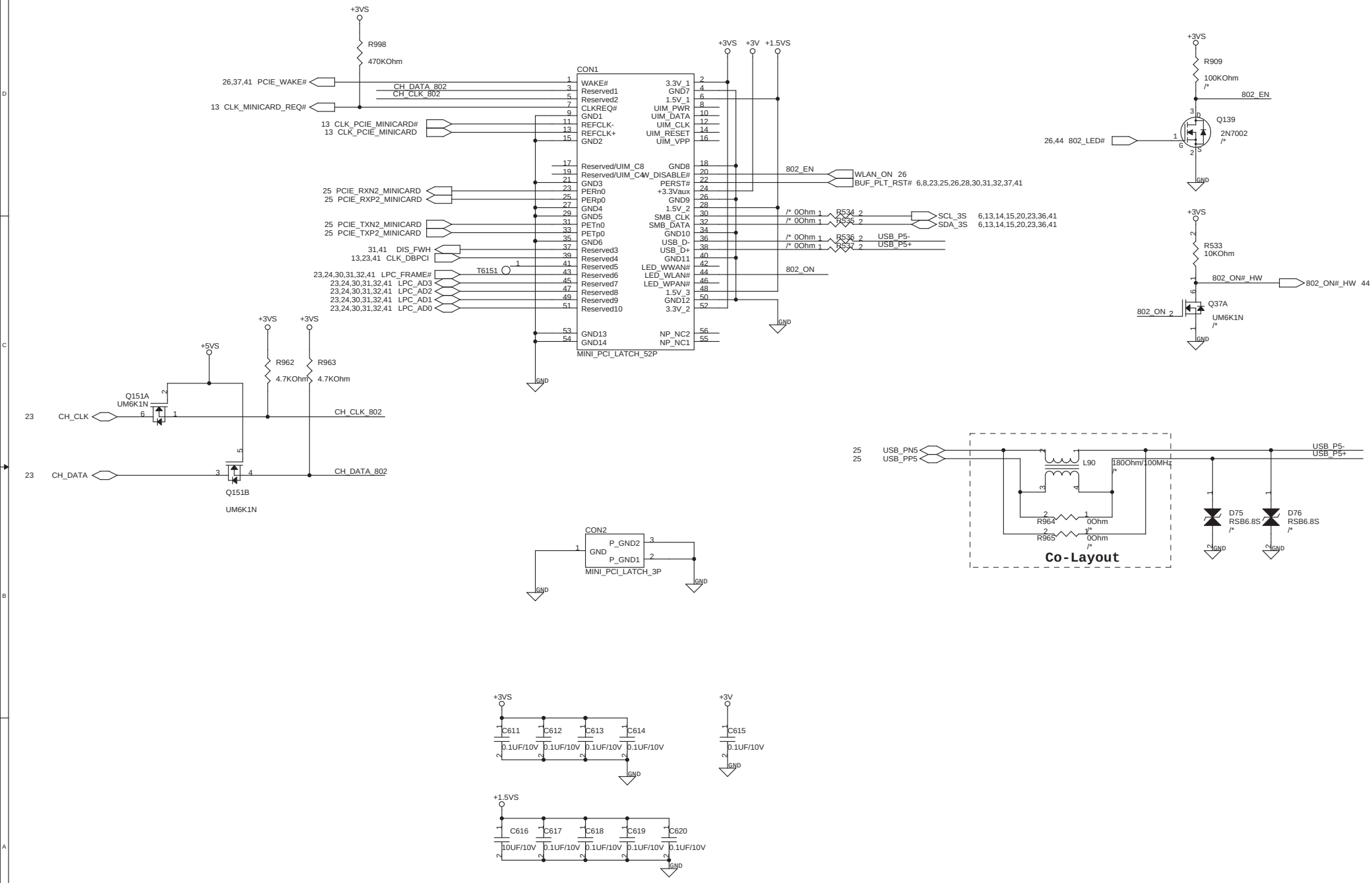
24HST1041-2

PLACE NEAR TRANSFORMER

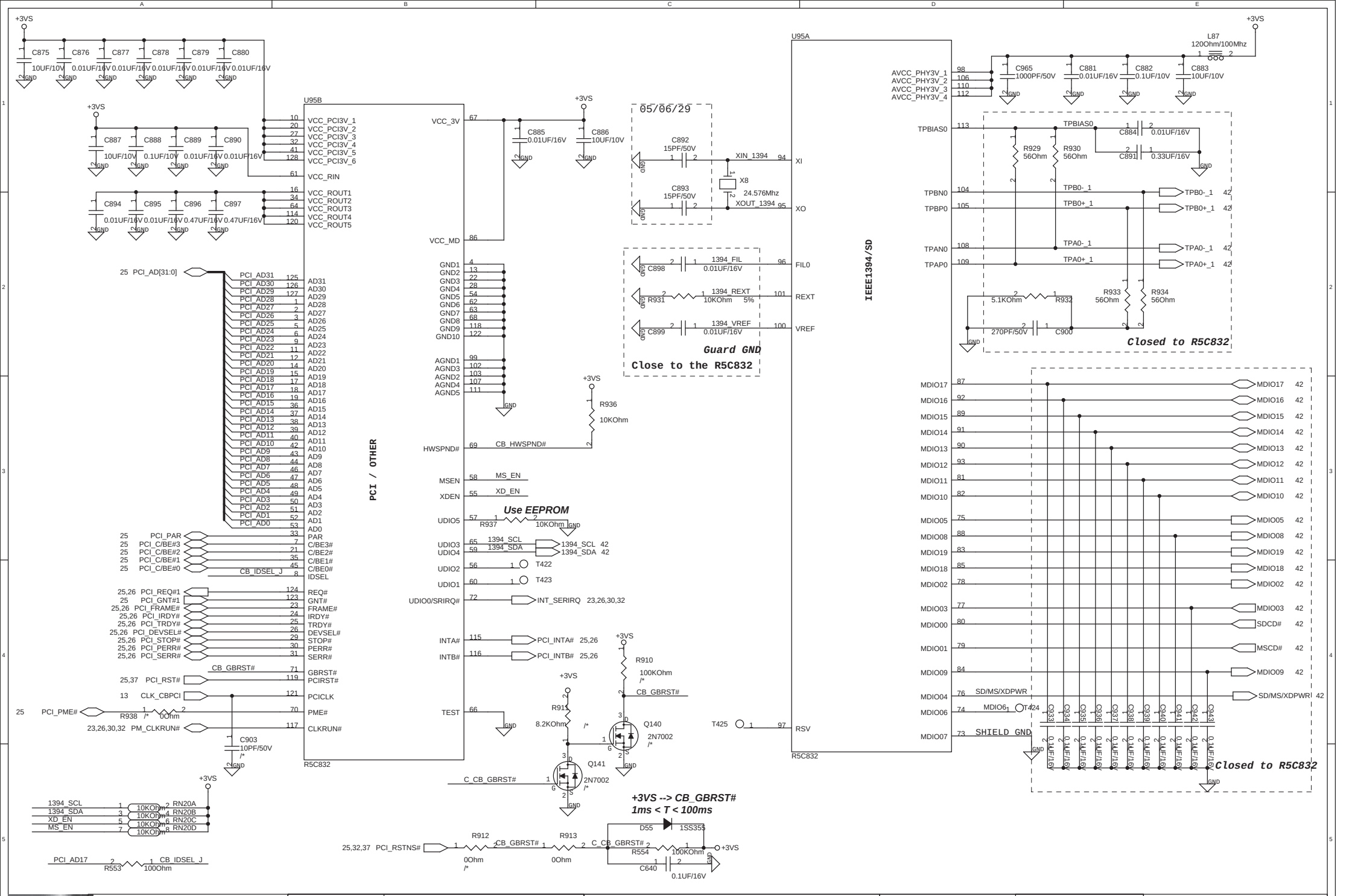




PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***RJ45/RJ11/MDC***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **38** OF **63**		RELEASE DATE :	

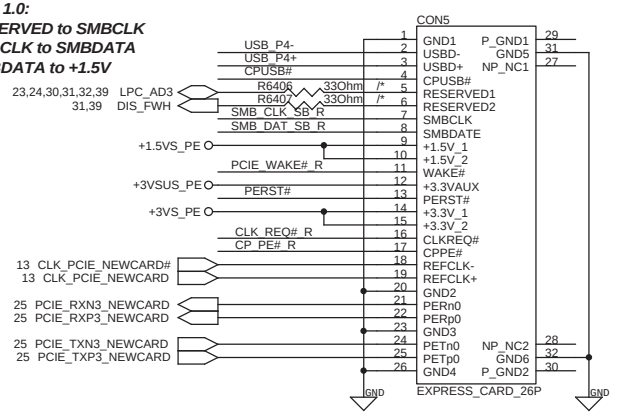


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***MINICARD***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
	SHEET **39** OF **63**			RELEASE DATE :	

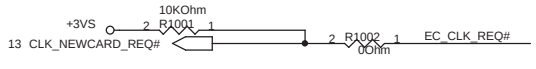


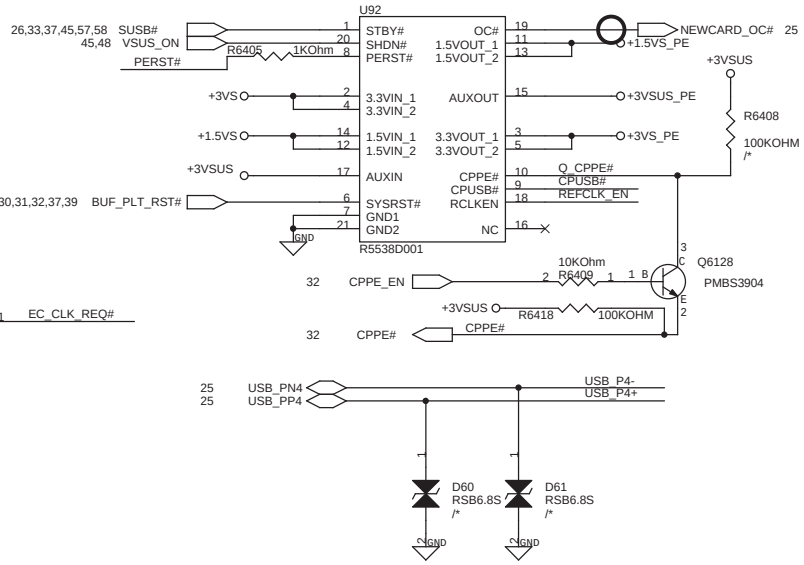
PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: RICOH R5C832	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 40 OF 63		RELEASE DATE :	

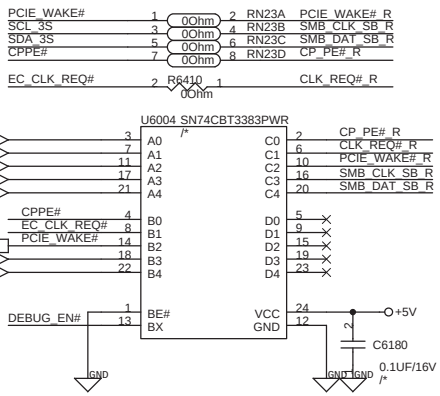
!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

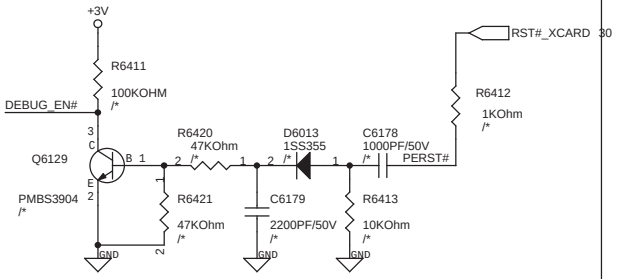


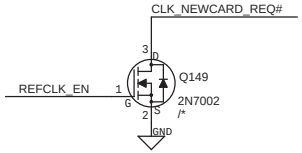
NEWCARD

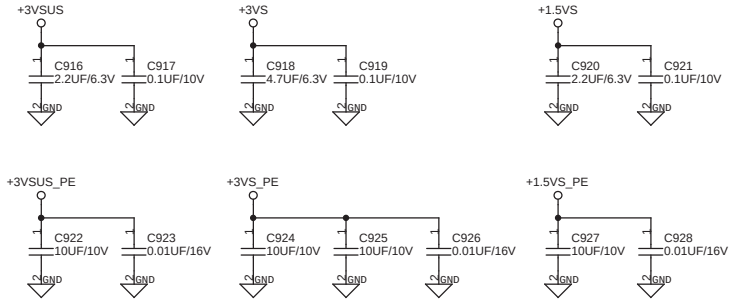






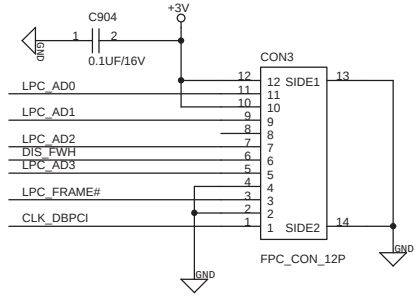






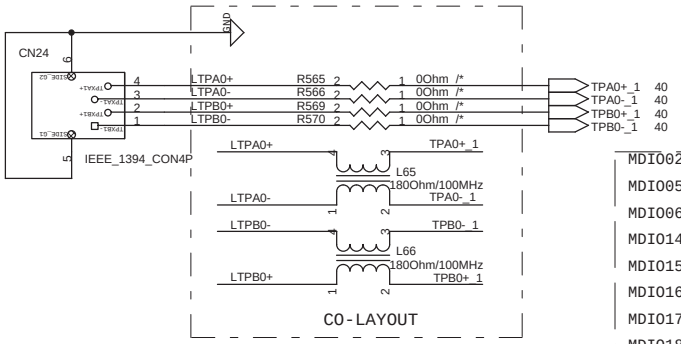
LPC Connector (Debug)

Note: Layout defined
Pin1--->Pin12



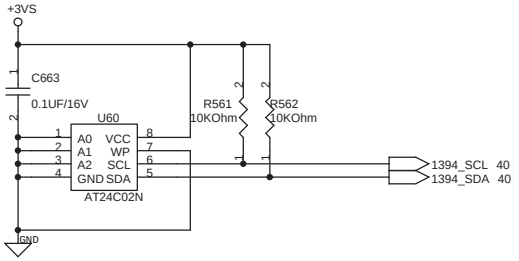
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***NEWCARD***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **41** OF **63**		RELEASE DATE :	

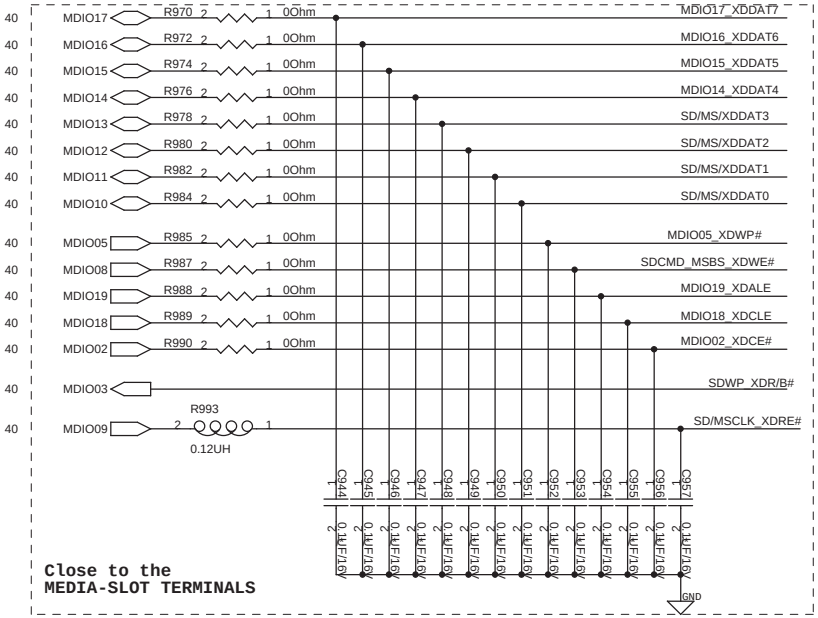
1394A

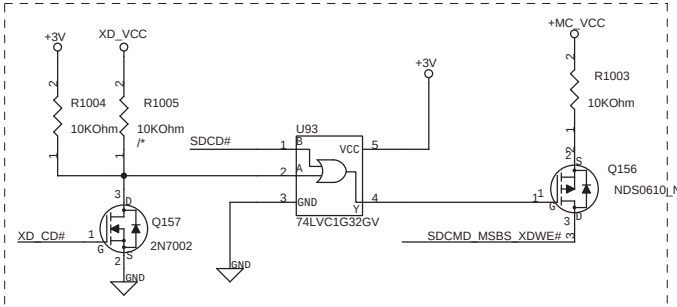


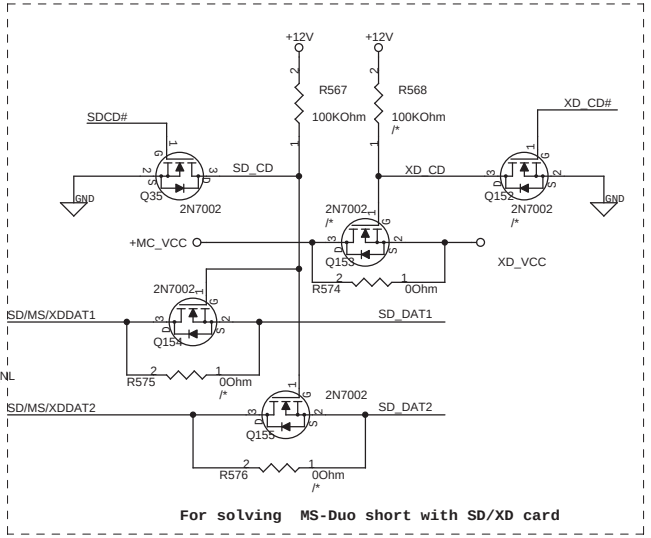
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

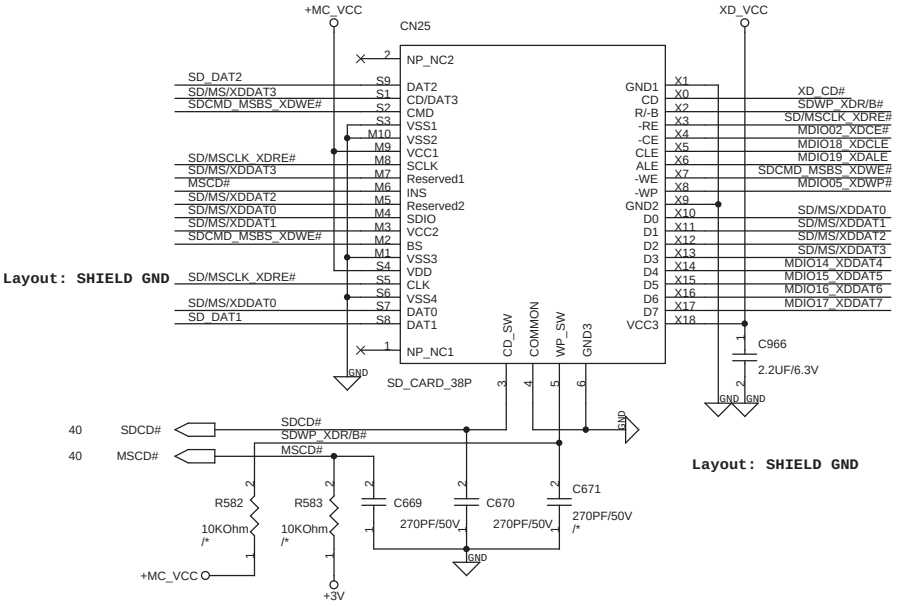
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

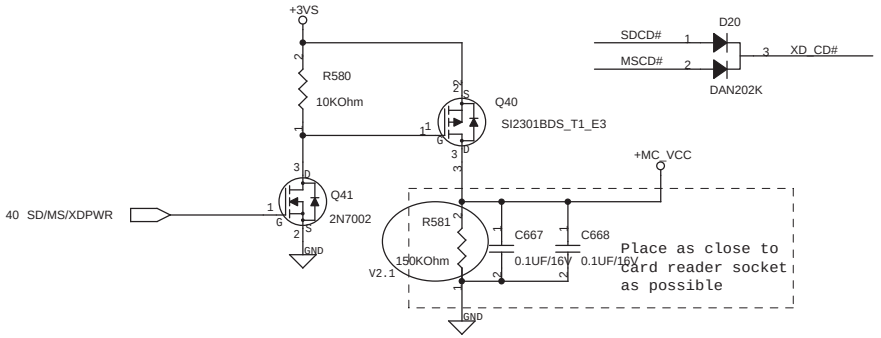


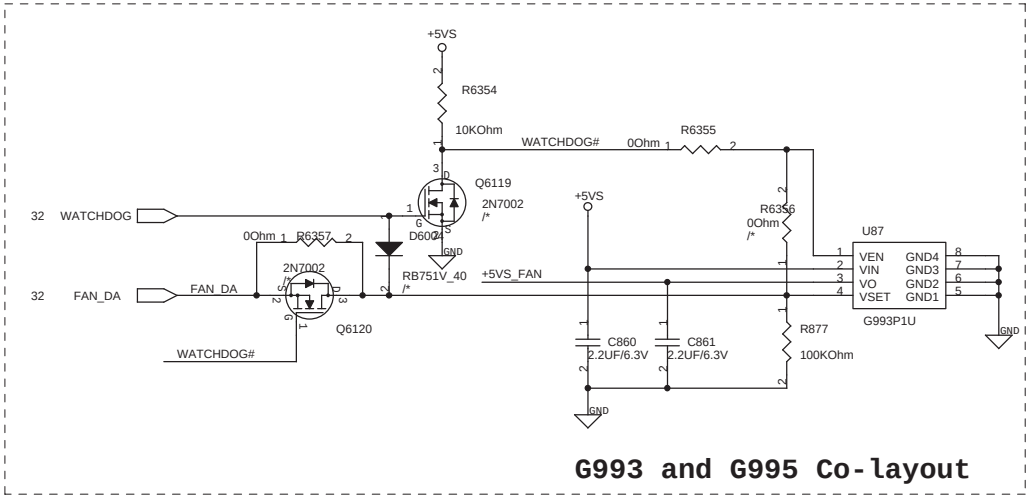


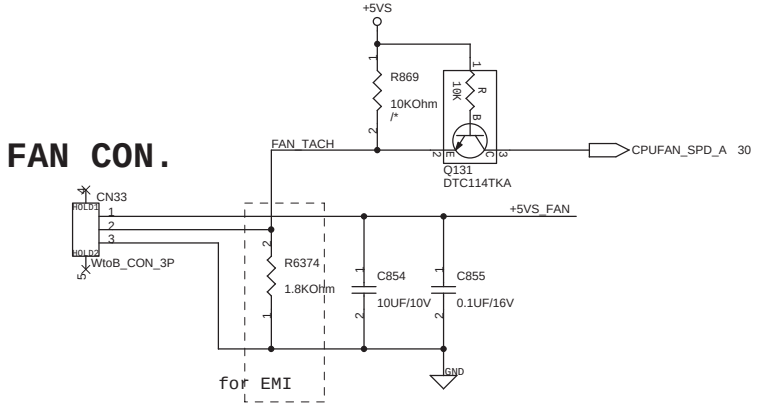


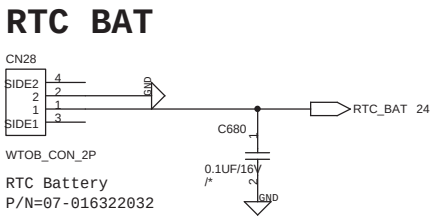


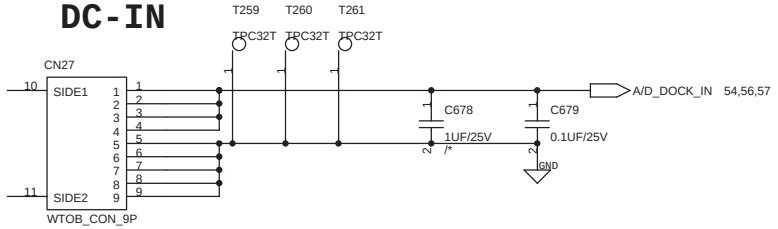




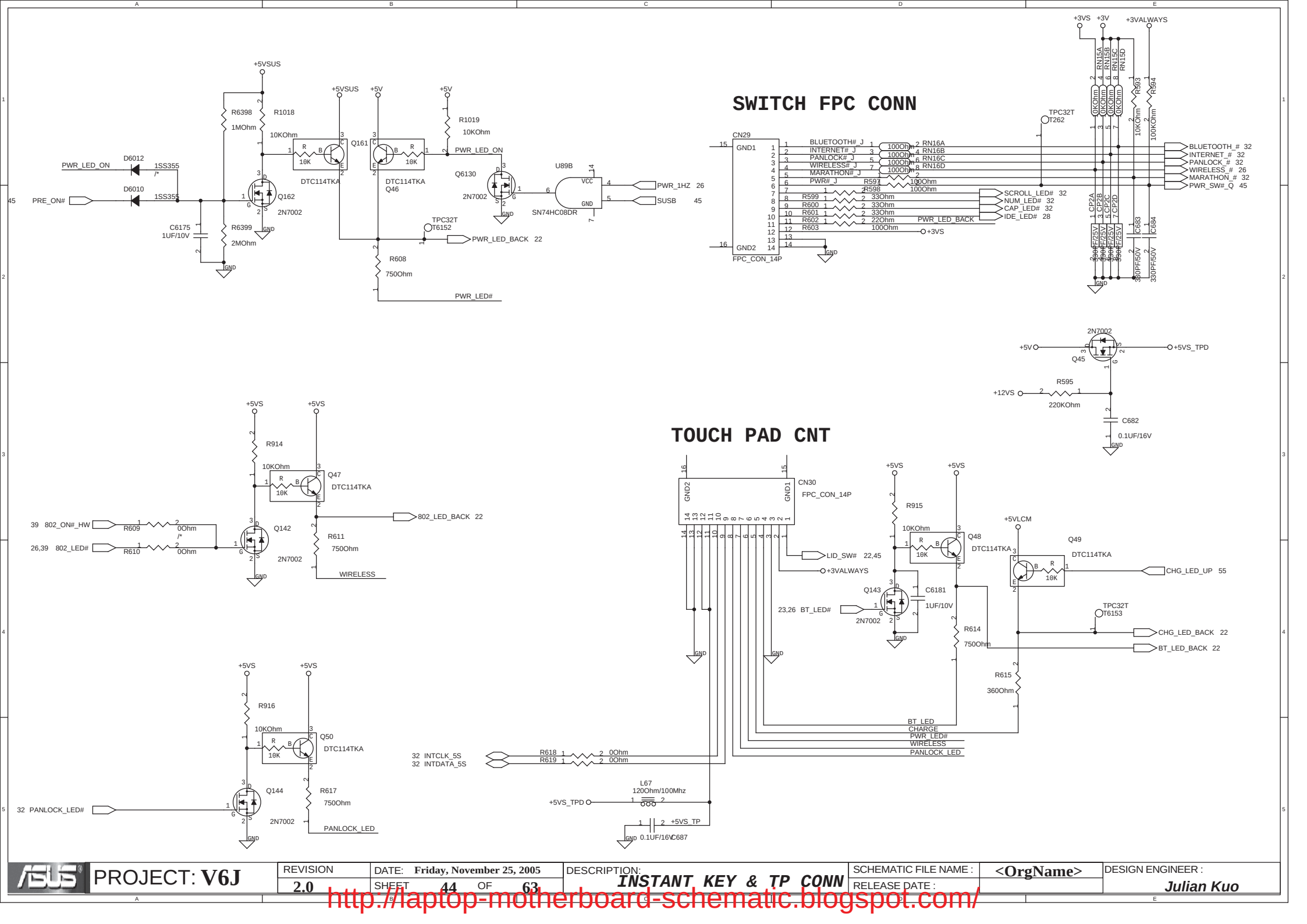




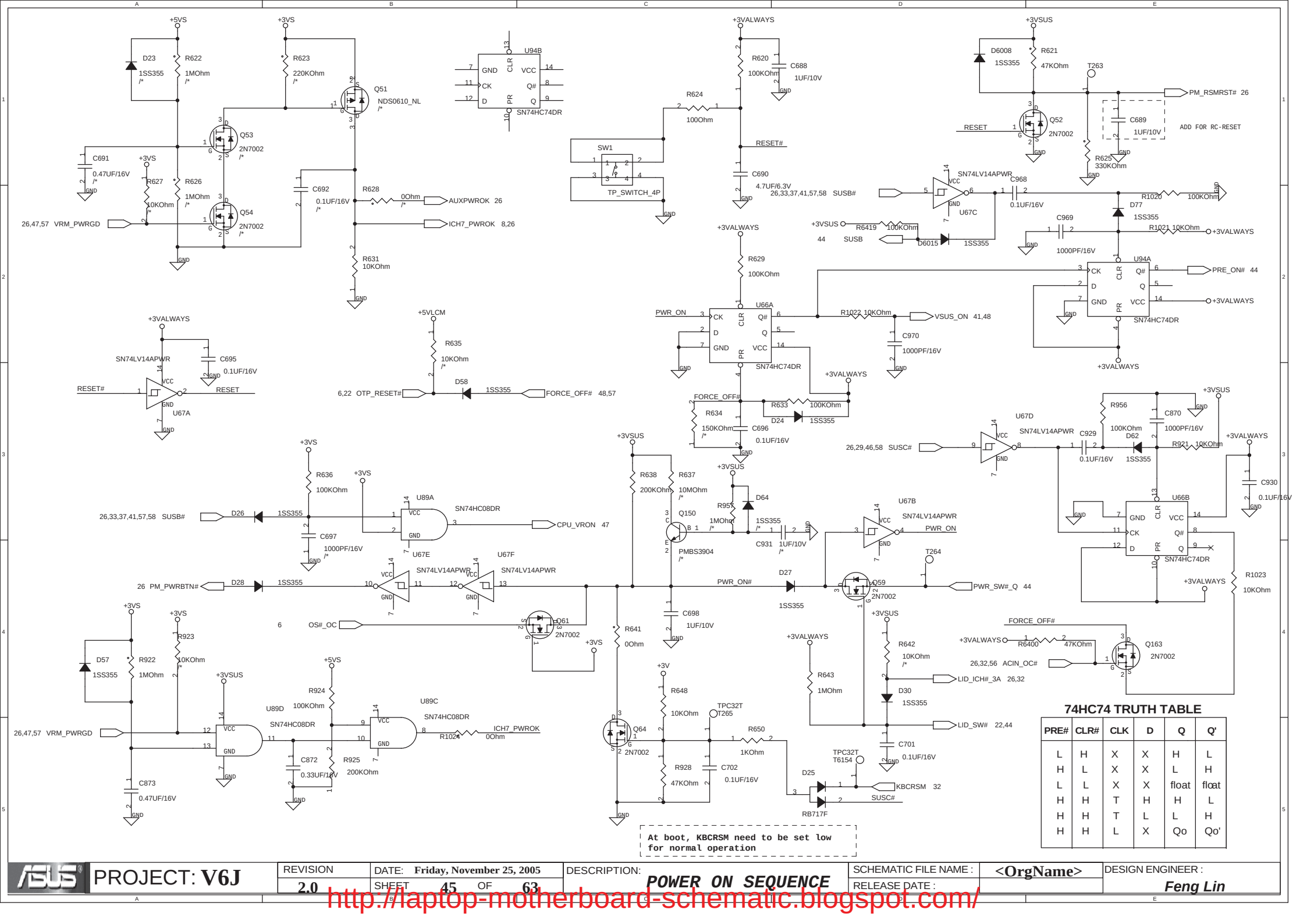




PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: FAN CONTROL & DC IN	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Julian Kuo
		SHEET 43 OF 63		RELEASE DATE :	



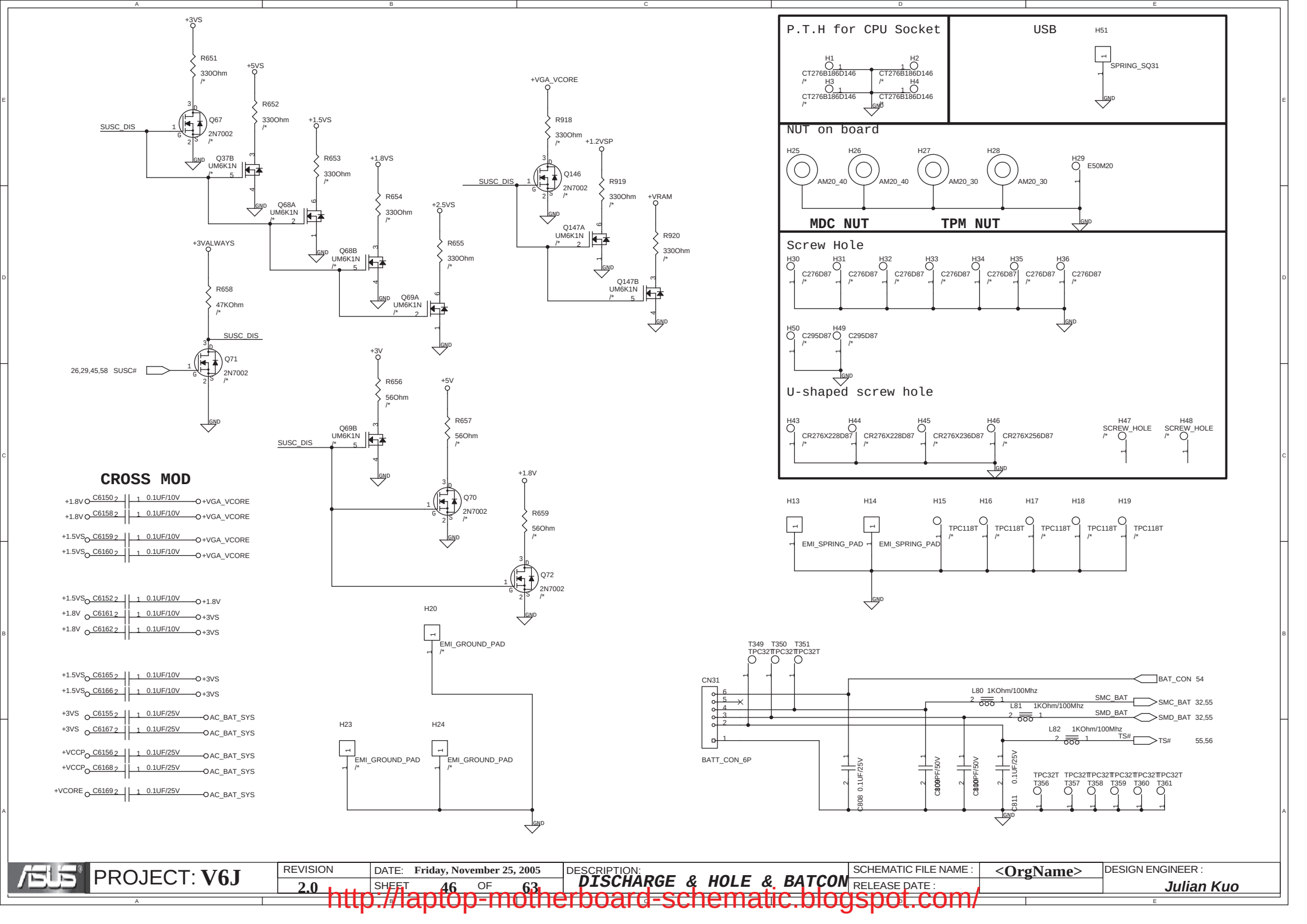
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***INSTANT KEY & TP CONN***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **44** OF **63**		RELEASE DATE :	



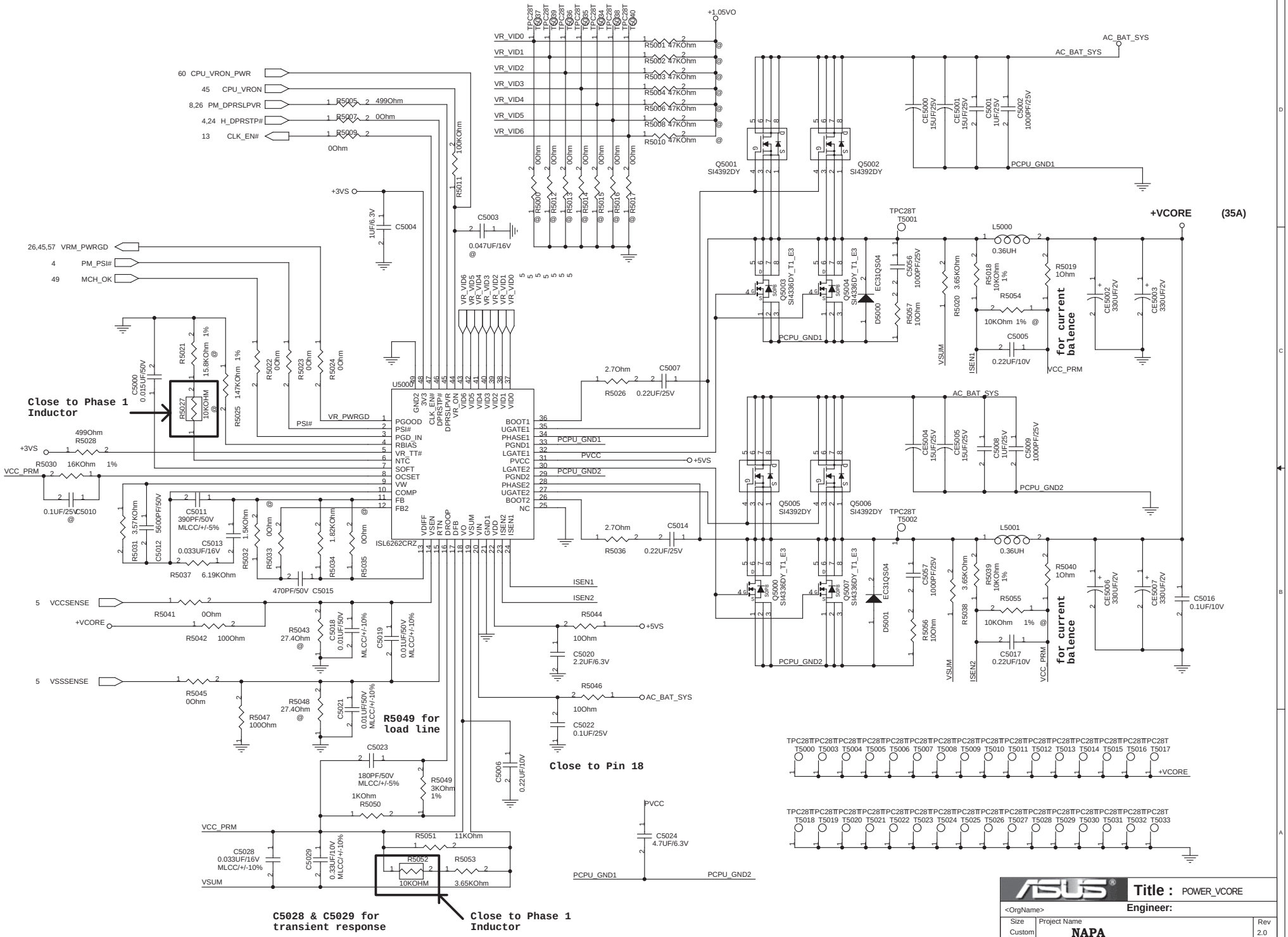
74HC74 TRUTH TABLE

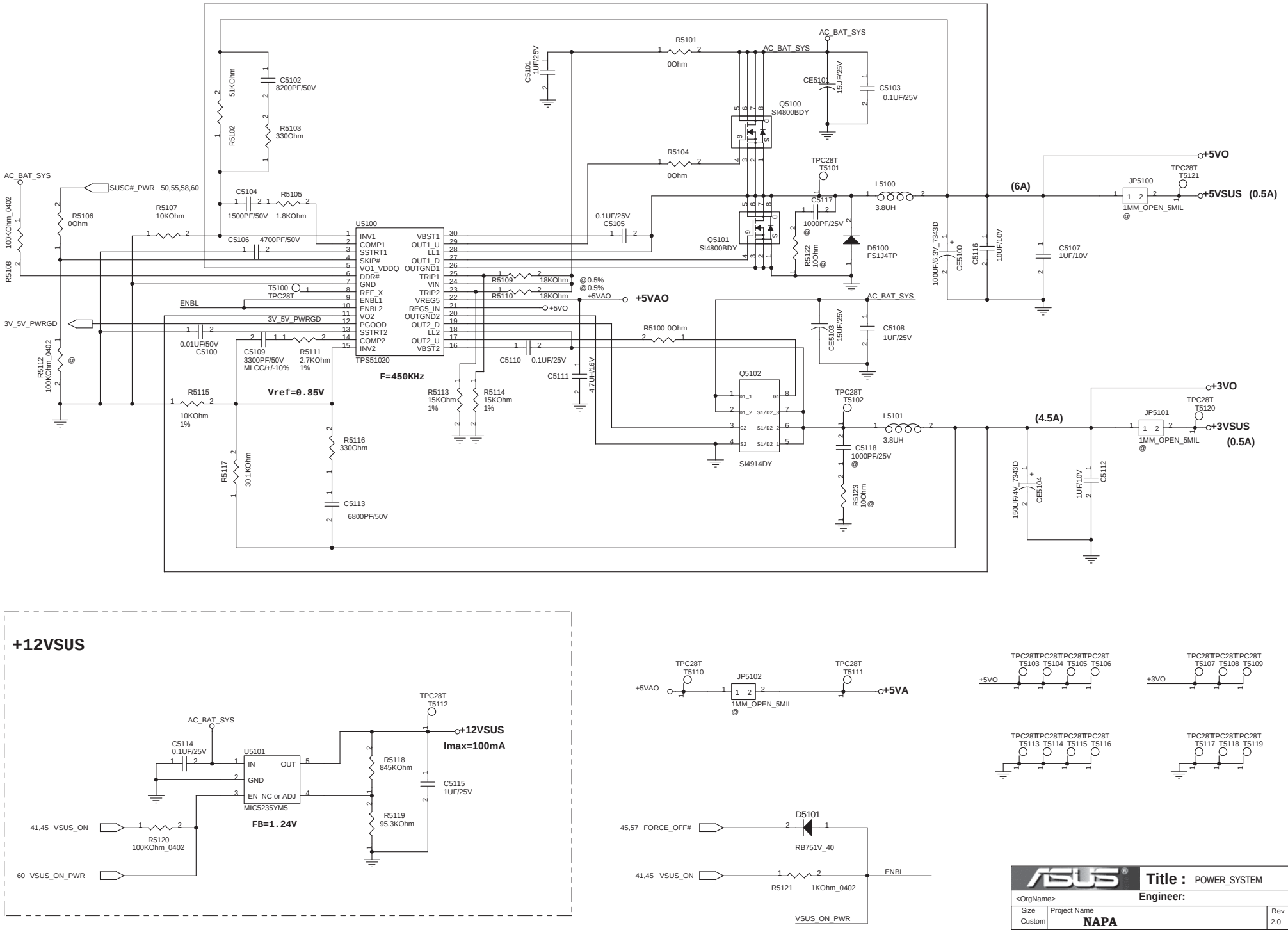
PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***POWER ON SEQUENCE***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **45** OF **63**		RELEASE DATE :	



PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: DISCHARGE & HOLE & BATCON	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Julian Kuo
		SHEET 46 OF 63		RELEASE DATE :	


+VCORE (35A)
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
for current balence
for current balence
ISL6262CRZ
U5000
Q5001 SI4392DY
Q5002 SI4392DY
Q5005 SI4392DY
Q5006 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5000 SI4336DY_T1_E3
Q5007 SI4336DY_T1_E3
L5000 0.36UH
L5001 0.36UH
D5000 EC31QS04
D5001 EC31QS04
Title : POWER_VCORE
Engineer:
Project Name NAPA
Date: Friday, November 25, 2005
Sheet 47 of 63
http://laptop-motherboard-schematic.blogspot.com/



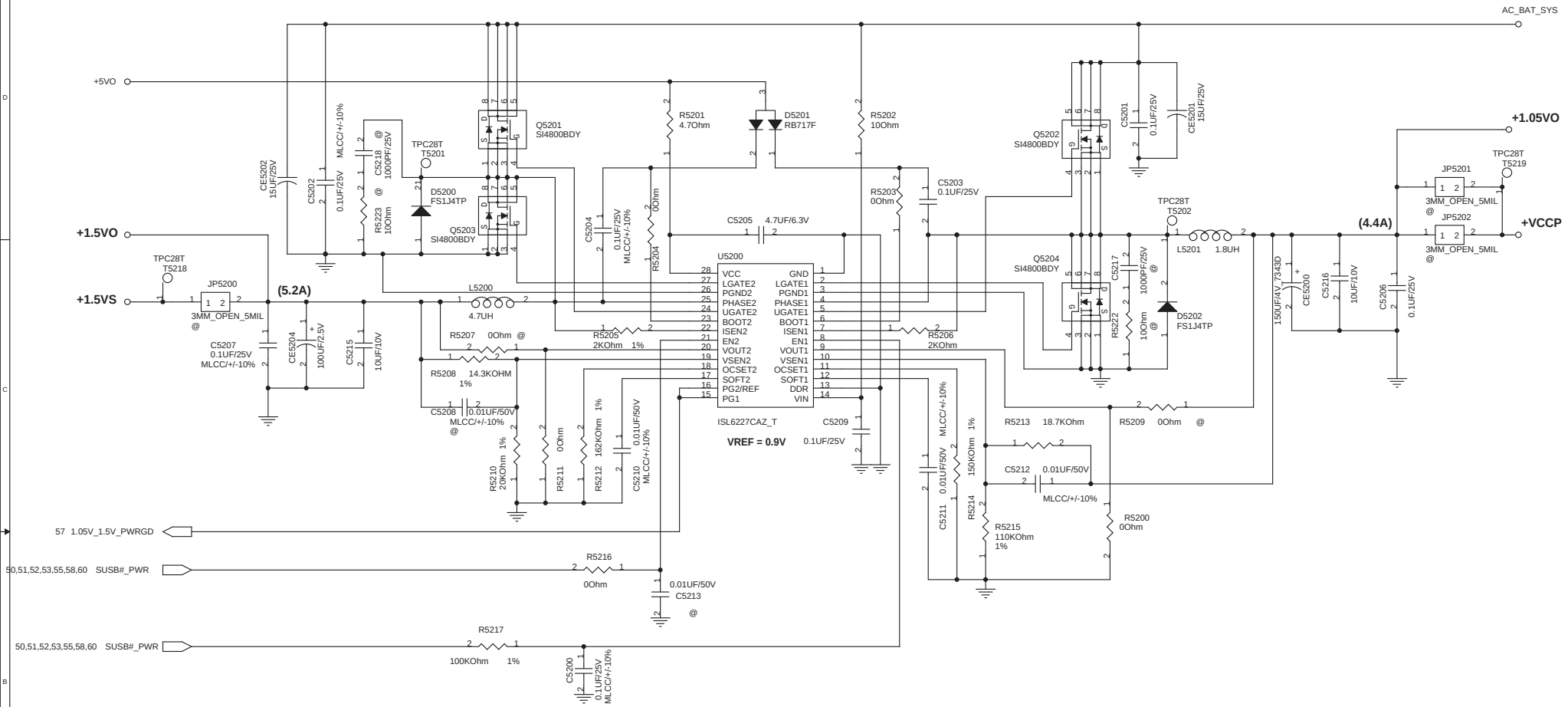
ASUS

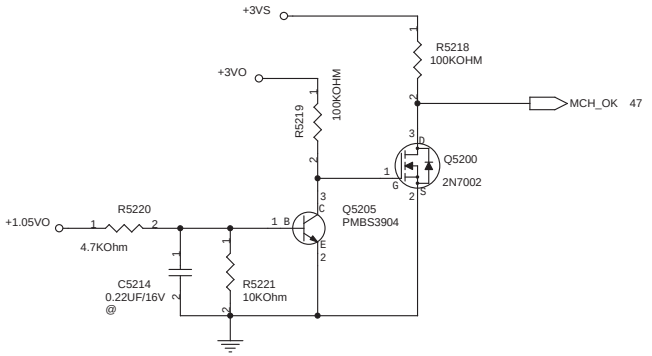
Title : POWER_SYSTEM

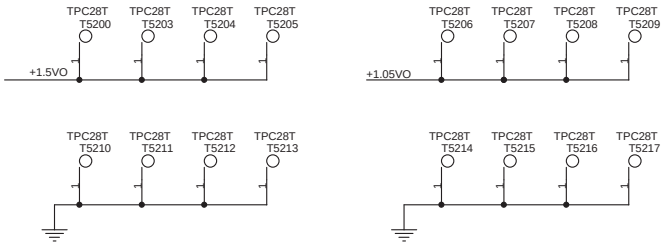
<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

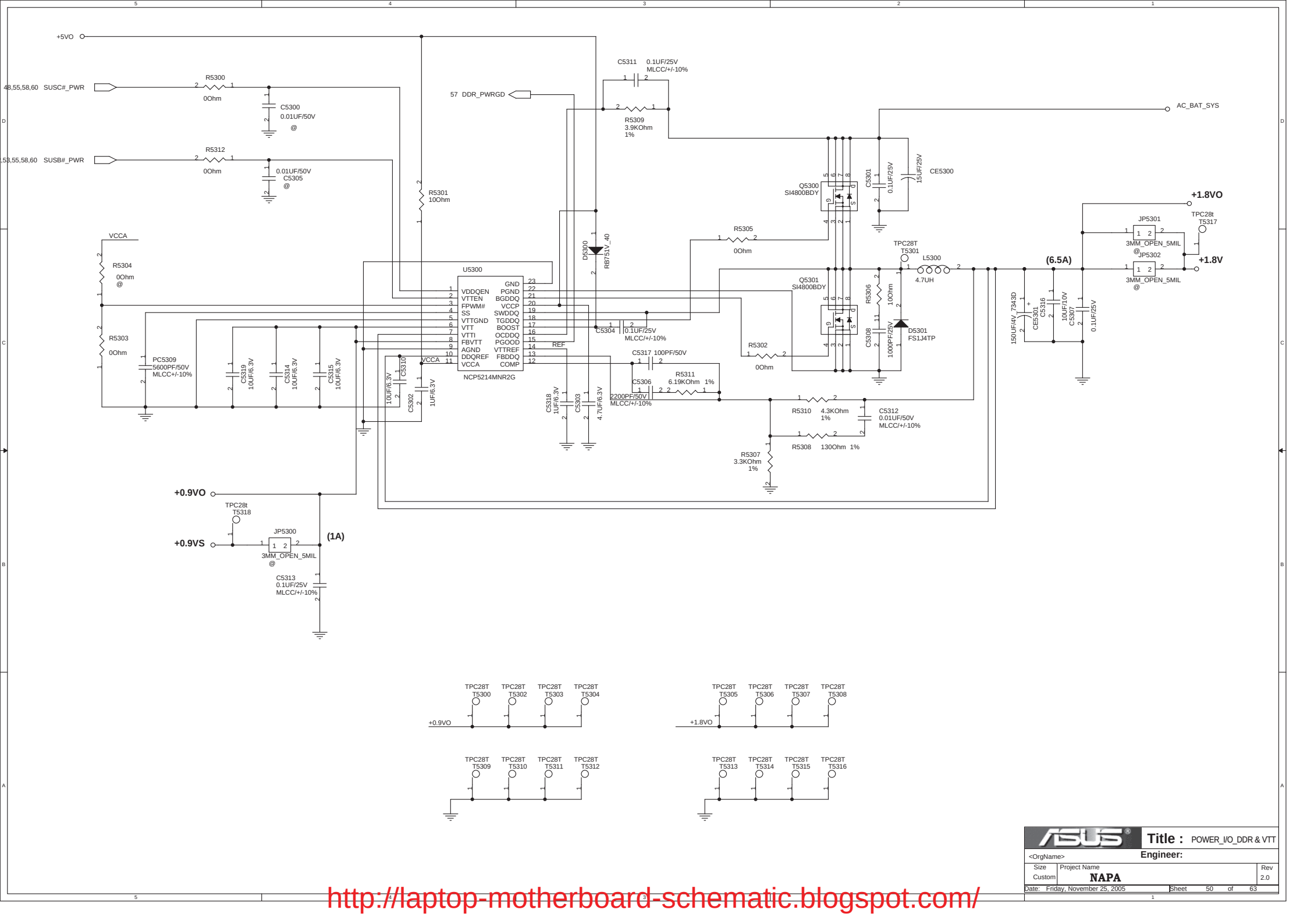
Date: Friday, November 25, 2005 Sheet 48 of 63







ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 49 of 63	



ASUS

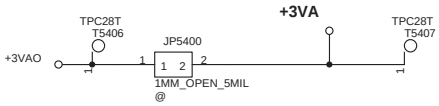
Title : POWER_I/O_DDR & VTT

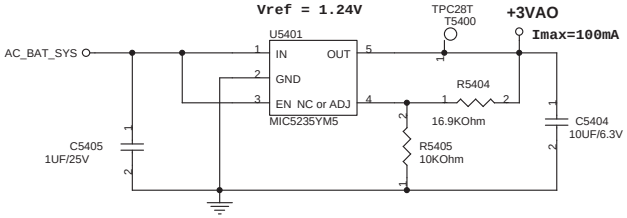
<OrgName> **Engineer:**

Size	Project Name	Rev
Custom	**NAPA**	2.0

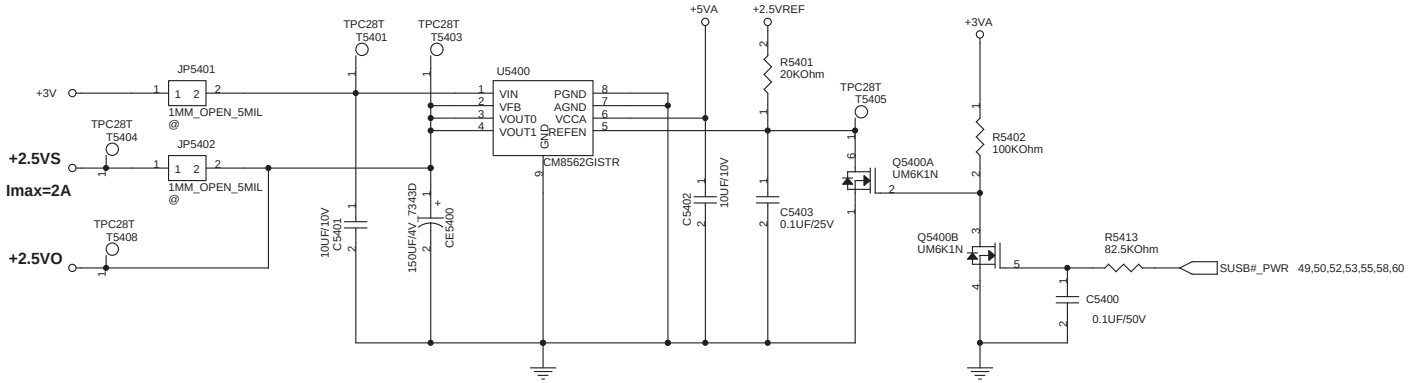
Date: Friday, November 25, 2005 Sheet 50 of 63

+3VA0

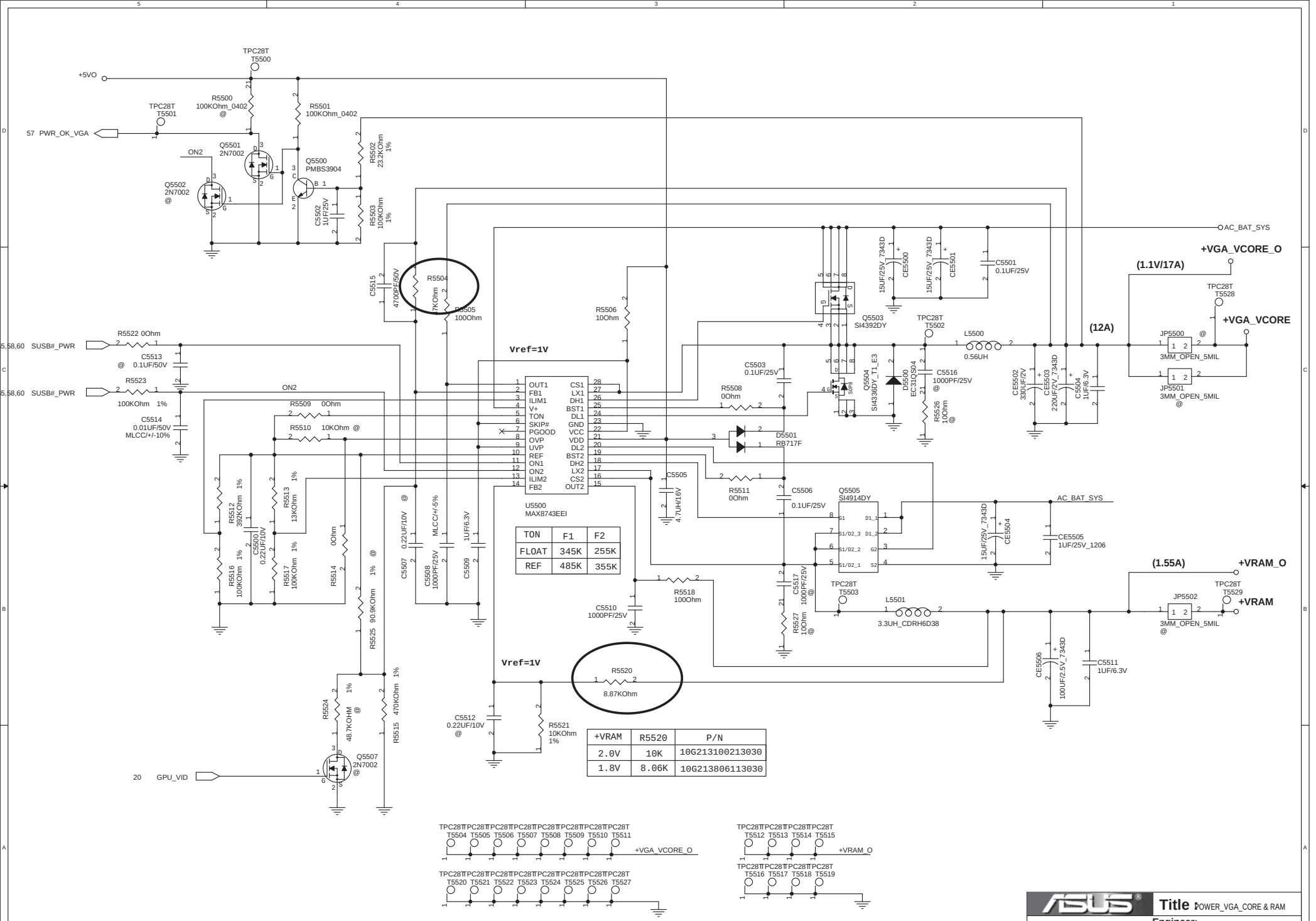




+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 51 of 63	



ASUS

Title: POWER_VGA_CORE & RAM

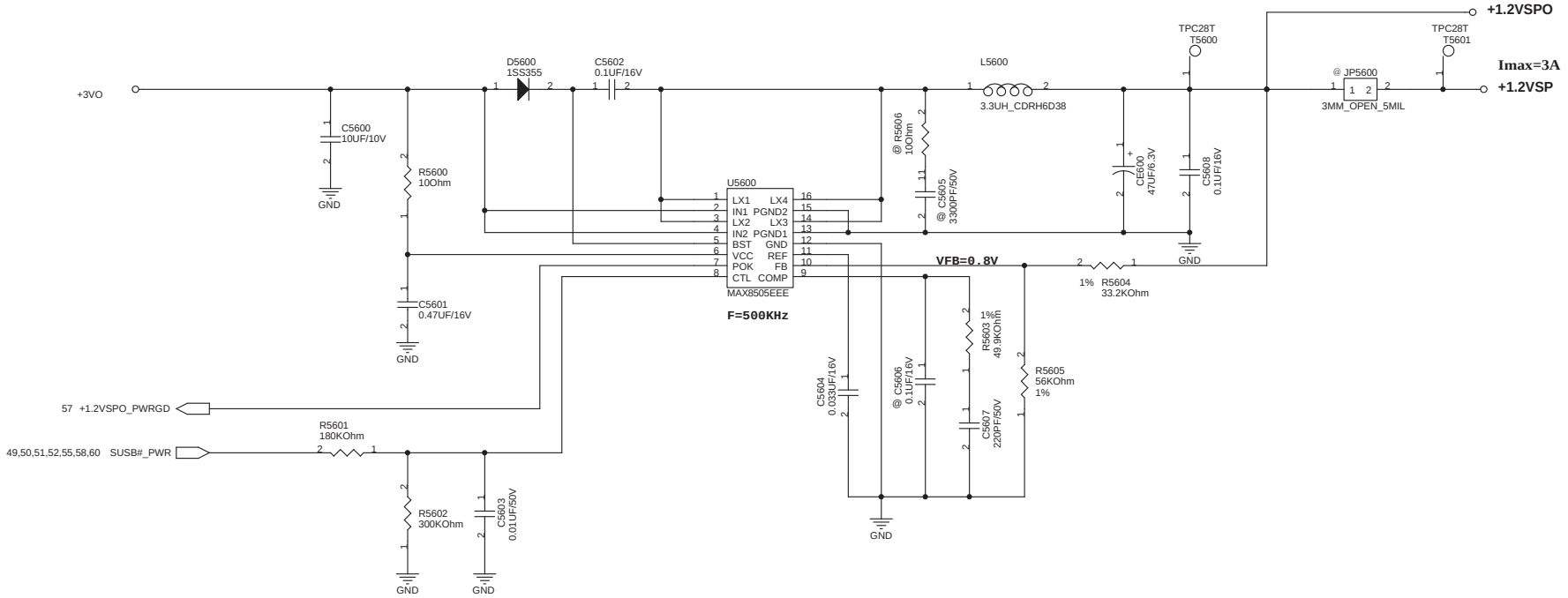
<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: Friday, November 25, 2005 Sheet 52 of 63

+1.2VSP



<Variant Name>

ASUS	Title : POWER_VGA_+1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 53 of 63	

TOTAL POWER=65W
-->3.42A

Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A

Vref = 4.096V
VLDO = 5.4V

Vbatt = Cell * { 4V +[0.4 X (VCTL/REFIN)] }
VCTL= LDO
=> Vbatt = 4.2V X CELLS

VICTL= 1.728V

VREFIN = 3.54V

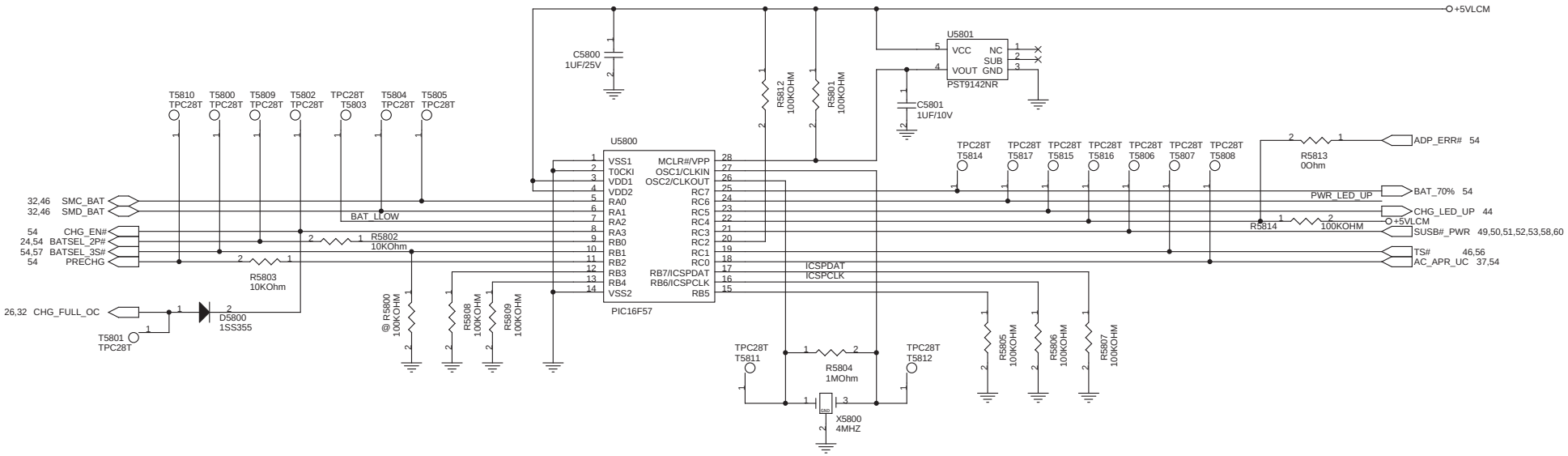
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

PRE_CHARGE CIRCUIT

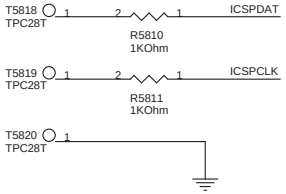
Pre-charge voltage 10V@3S
Pre-charge voltage 13.04V@4S

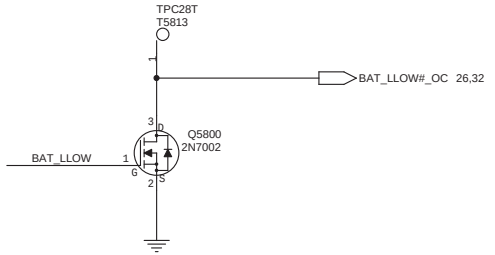
Title :	POWER_CHARGER
<OrgName>	Engineer:
Size: C	Project Name: NAPA
Rev: 2.0	
Date: Friday, November 25, 2005	Sheet 54 of 63

PIC16F57



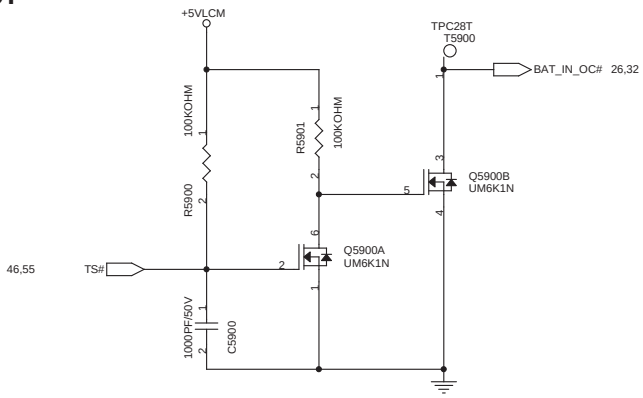
For PIC reflash



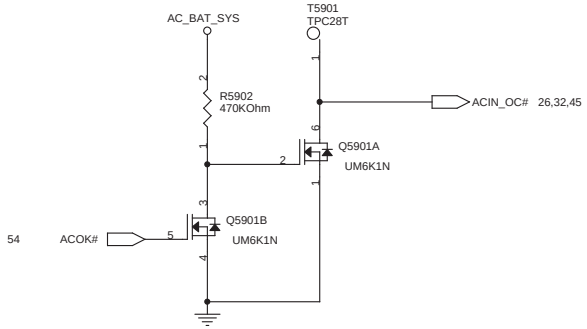


ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 55 of 63	

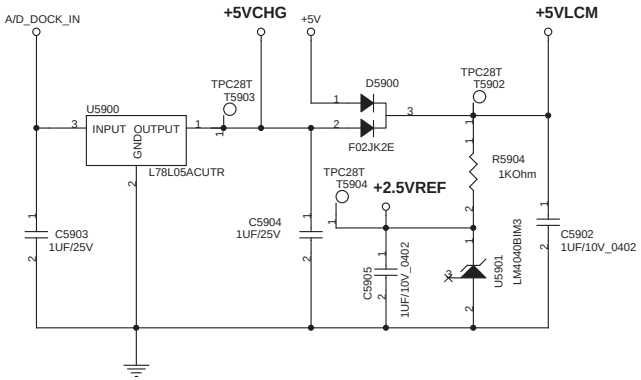
BATTERY IN DETECT



ADAPTER IN DETECT

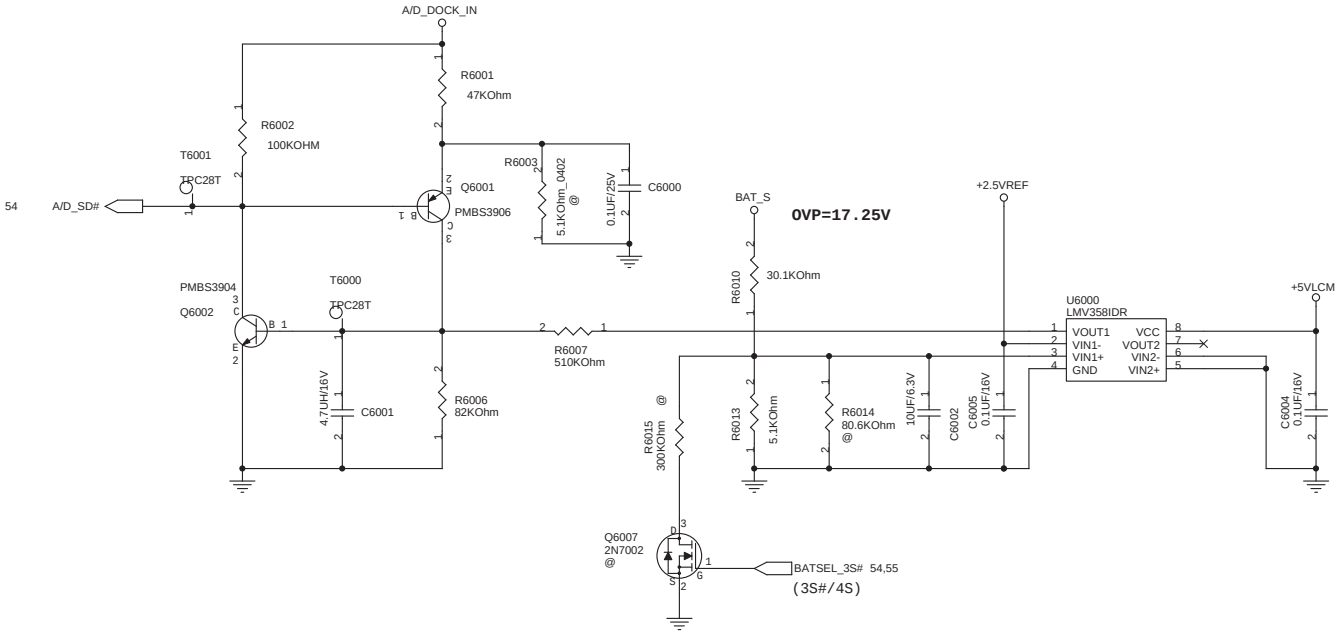


+5VLCM, +5VCHG & +2.5VREF

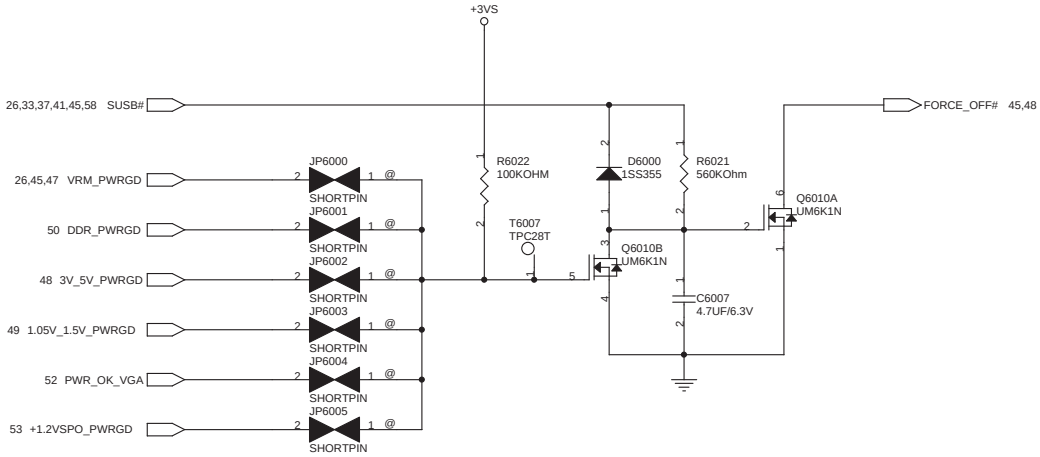


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 56 of 63	

BATTERY A/D_SD# (OVP)



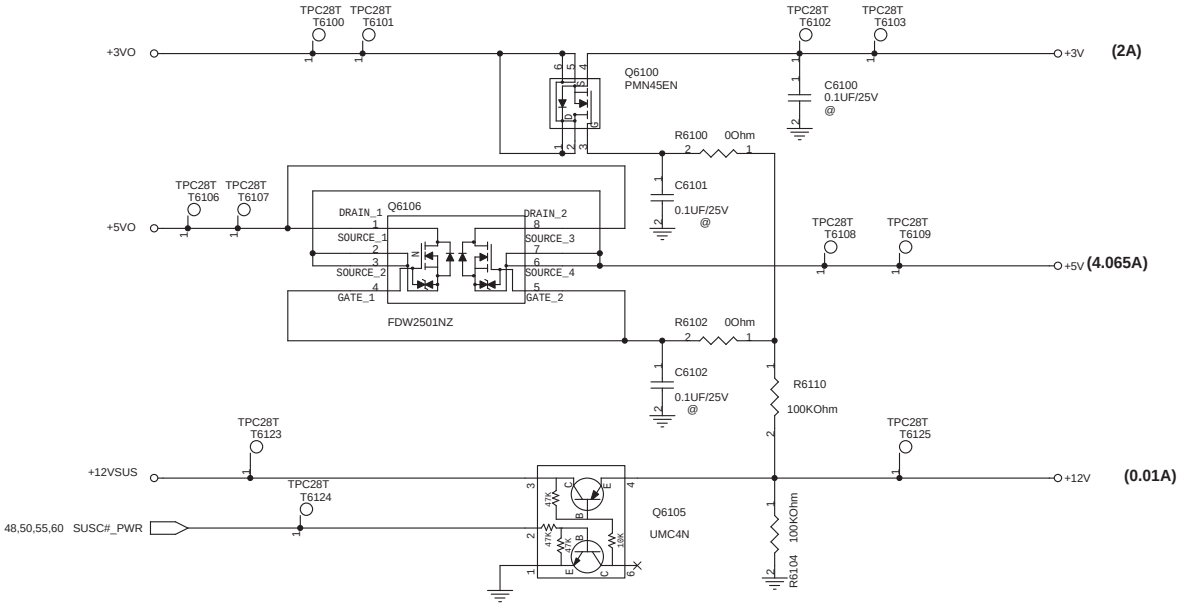
POWER GOOD DETECTER

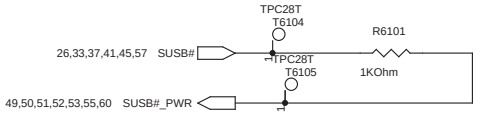


TPC28T T6003 — VRM_PWRGD
TPC28T T6004 — DDR_PWRGD
TPC28T T6005 — 3V_5V_PWRGD
TPC28T T6006 — 1.05V_1.5V_PWRGD

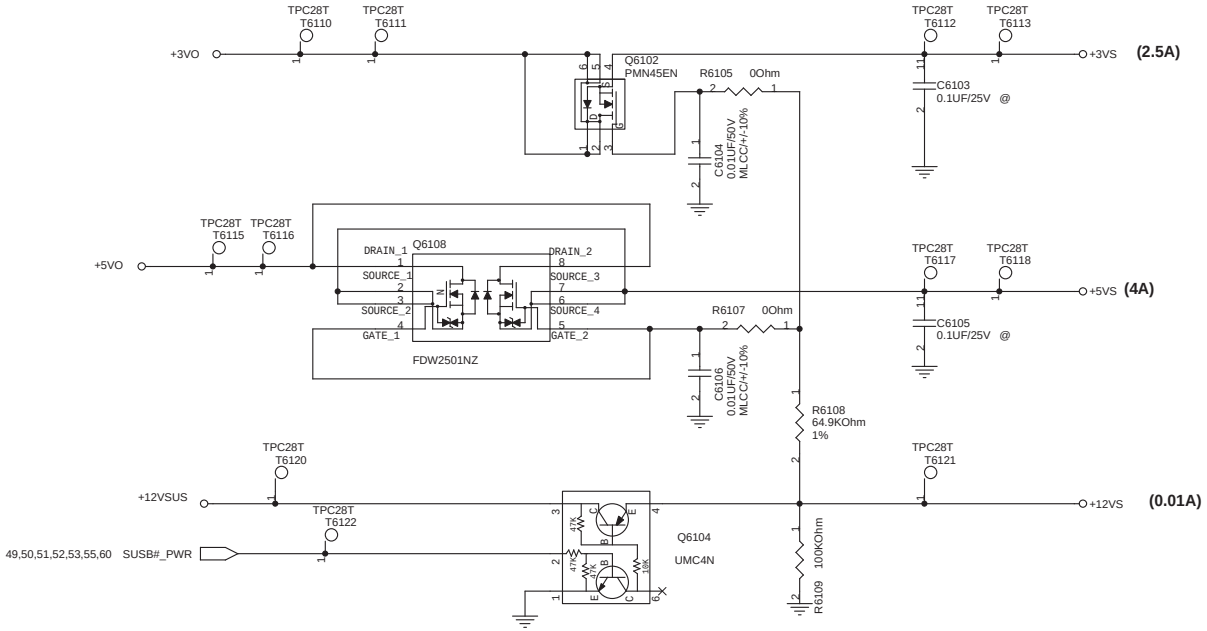
ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 57 of 63	

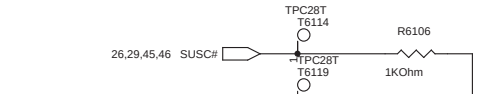
SUSC#_PWR POWER

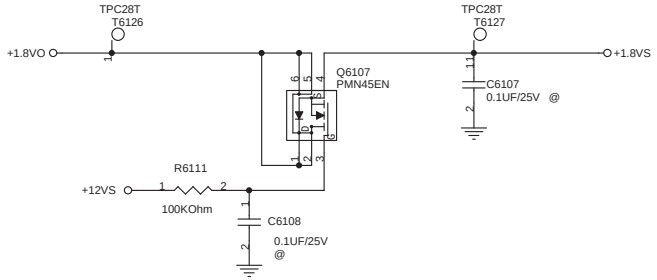




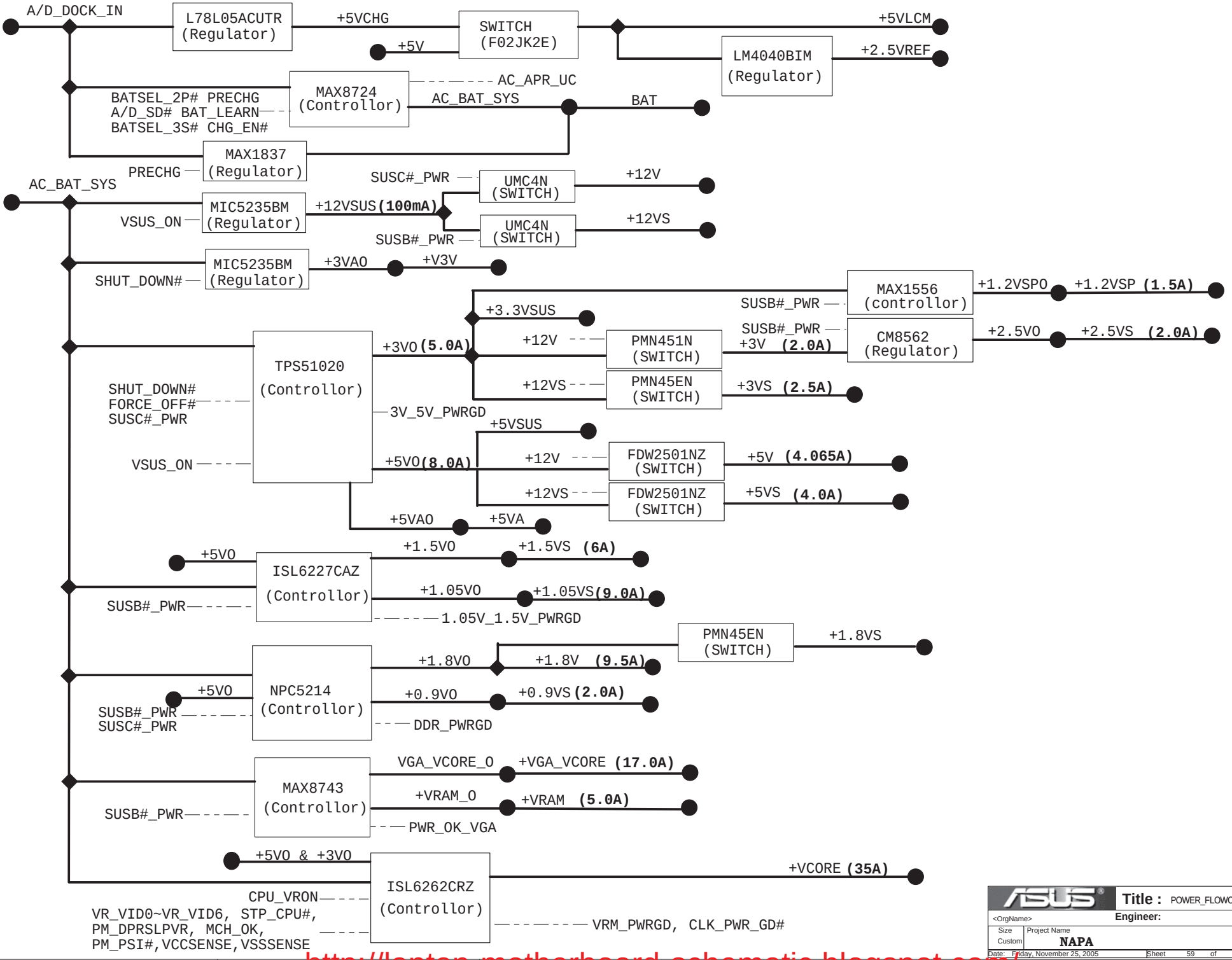
SUSB#_PWR POWER







ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 58 of 63	



ASUS

Title : POWER_FLOWCHART

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: Friday, November 25, 2005 Sheet 59 of 63

AC_BAT_SYS → AC_BAT_SYS 22,46,47,48,49,50,51,52,54,56

+3VA → +3VA 23,24,29,32,44,45,46,51

+5VA → +5VA 22,48,51,54

+5VO → +5VO 48,49,50,52,58

+3VO → +3VO 48,49,53,58

+3VSUS → +3VSUS 26,27,32,37,41,45,48

+5VSUS → +5VSUS 27,44,48

+3V → +3V 22,23,25,26,32,37,38,39,41,42,44,45,46,51,58

+3VS → +3VS 6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,36,37,39,40,41,42,44,45,46,47,49,57,58

+12VSUS → +12VSUS 48,58

+12V → +12V 34,42,58

+12VS → +12VS 23,44,58

+5V → +5V 14,29,33,41,44,46,56,58

+5VS → +5VS 20,27,28,32,34,36,39,43,44,45,46,47,58

+2.5VO → +2.5VO 51

+2.5VS → +2.5VS 10,20,21,46,51

+1.8VO → +1.8VO 50,58

+1.8V → +1.8V 8,11,14,15,46,50

+1.8VS → +1.8VS 20,46,58

+0.9VS → +0.9VS 16,50

BAT → BAT 54

+5VCHG → +5VCHG 54,56

+5VLCM → +5VLCM 44,45,54,55,56,57

+2.5VREF → +2.5VREF 51,54,56,57

+VCORE → +VCORE 5,6,46,47

+VGA_VCORE → +VGA_VCORE 17,46,52

+VRAM → +VRAM 18,19,46,52

+1.2VSP → +1.2VSP 17,18,46,53

BAT_CON → BAT_CON 46,54

FOR POWER TEST

+3VA

JP6300 (1 2) SGL_JUMP @ → CPU_VRON_PWR 47

JP6301 (1 2) SGL_JUMP @ SUSB#_PWR → SUSB#_PWR 49,50,51,52,53,55,58

JP6302 (1 2) SGL_JUMP @ SUSC#_PWR → SUSC#_PWR 48,50,55,58

JP6303 (1 2) SGL_JUMP @ VSUS_ON → VSUS_ON_PWR 48

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 60 of 63	

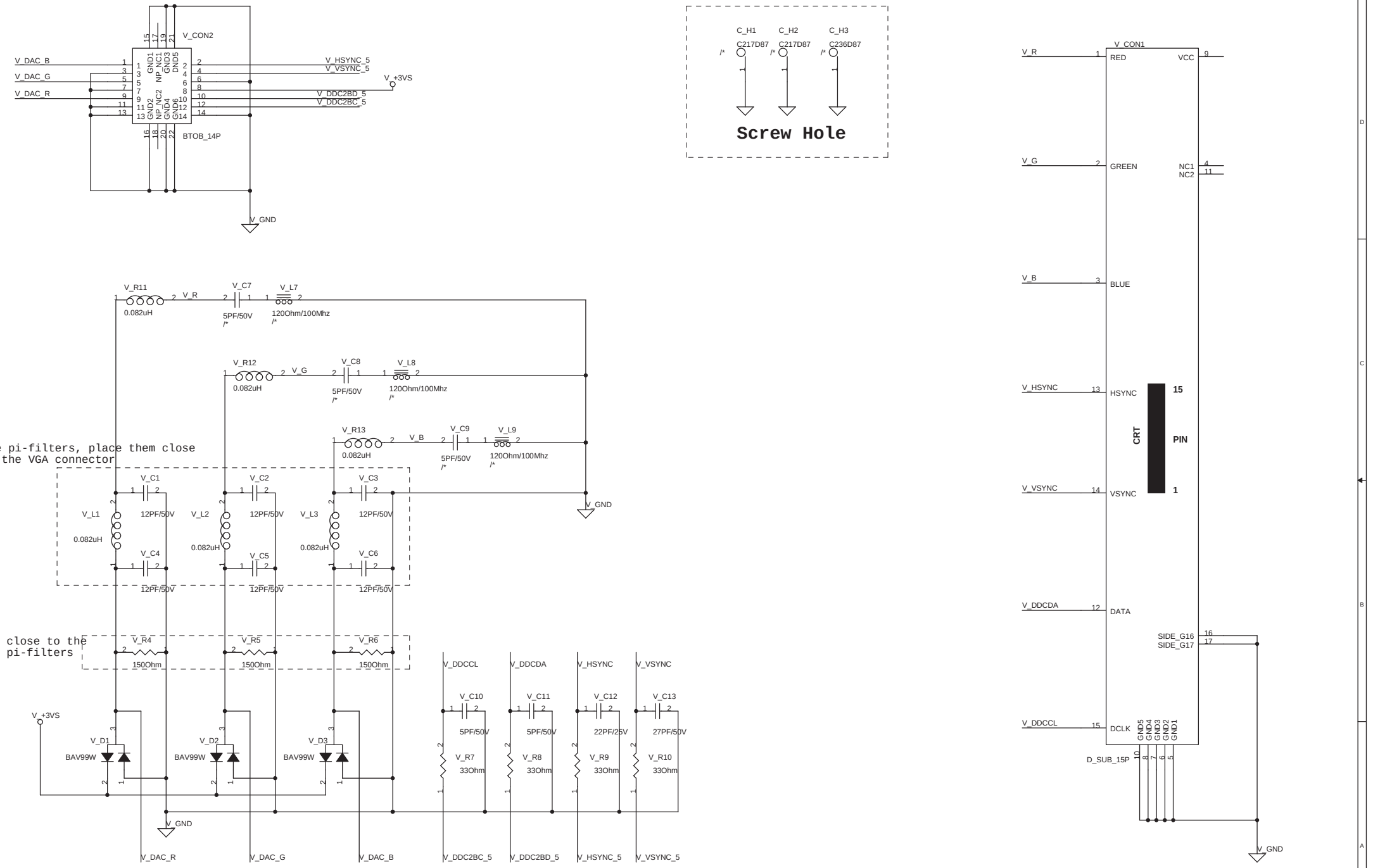
Revision History

V1.0 to V1.1

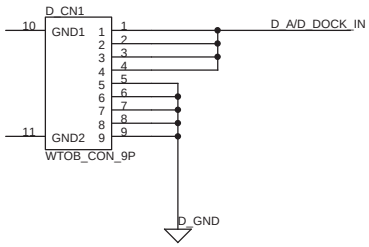
1. D58 change from DAP202 to 1ss355
2. Panel detection chagne from PID to EDID method.
3. Reserve panel dectection by PID method.
4. Tuning power sequence by power circuitry.
5. TP_MA_RCVEN* net can't connect with TP_MB_RCVEN*, so cut it.
6. CPU address A14 and A15 is swap for booting.
7. Populate R6347 = R6348 =120 Ohm by nVDIDA recommend.
8. Change VGA chip from G72M-V to G72M, so change device ID strapping.
9. CHG_FULL_OC net has doubled pull-up to +3vs and +3vsus, so remove +3vsus pull-up for leakage.
10. CLK_EN# pull-up to +3vs will has leakage current from cpu vcore controller. so remove it.
11. Lan chip reset signal has leakage current output to system reset signal, so add D6006 to solve it.
12. +1.5VS power trace is too small from source to calistoga IC, so increase trace width.
13. Remove R639 because system has no shutdown signal from POWER.
14. R638 change to 200k and C698 change to 1uF for power on button feeling.
15. CFG18, 16, 15 has wrong connection, correct it.
16. C138=C139=22pF for tunning 14.318MHz crystal freauency.
17. RN15 pin 2 pull-up power change from +3V to +3VS for solving leakage current at S3 state.
18. Change audio circuitry for solving pop noise.
19. Change pci-express decoupling caps from 0.1uF/Y5V to 0.1uF/X5R.
20. Microphone pull-up power source change to OP AMP generate.
21. R287=0 Ohm and R290 remove for G72M need +3VS level input about 27MHz spread spectrum input pin.
22. MAX6649 be used on G72M has wrong connection, so correct it.
23. Populate R574=0 Ohm for XD card work fine.
24. Remove R6360, R6361, R6358, R6359 for JTAG pin pull-up/down on G72M.
25. Populate C563, C566 for improve microphone quality.
26. Add D6008 for PM_RSMRST# discharge quickly.
27. Tunning C141~C146, R128, C490 value base on EVT report about clk signal quality issue.
28. Add ODD disable function support.

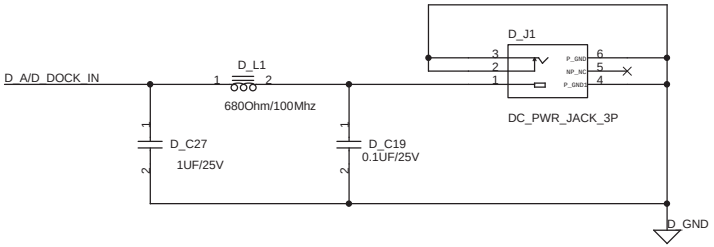
V1.1 to V2.0

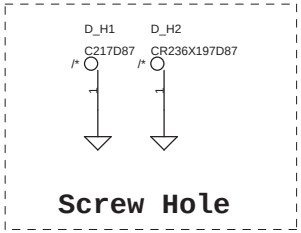
1. Calistoga CRT disable guide change, so IREF pin connect to power directly.
2. Add circuitry for newcard disable support.
3. R381 change to 1K Ohm for ODD disable support.
4. Reserve newcard type debug card support circuitry.
5. Add mini card type debug card support circuitry.
6. MAX6649 be used on G72M change to MAX6657.
7. Add TPM connector debug card support.
8. The reset signal of lan chip pull-down 10K Ohm.
9. RTCRST# delay time control add diode for quick discharge.
10. Populate R6351, C? for solving led will flash once when system power on.
11. Add usb spring and beas on agnd and dgnd for EMI request.
12. Disable audio jack sense feature.
13. Add Q6130 for 1HZ flash

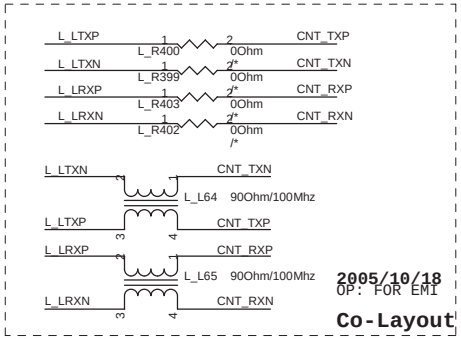


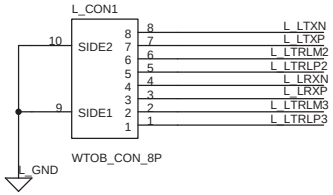
ASUS	Title : CRT OUT	
<OrgName>	Engineer: *Feng Lin*	
Size: Custom	Project Name: **V6J**	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 62 of 63	

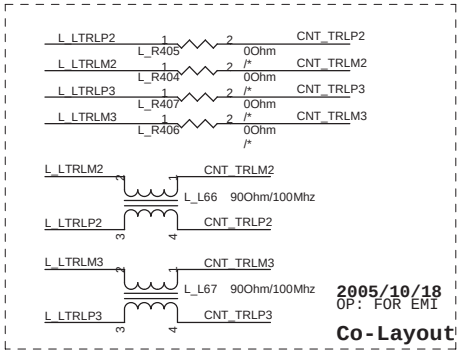


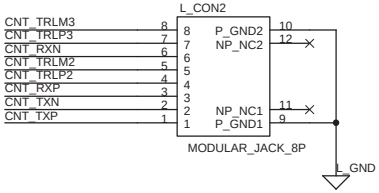












PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***DC IN***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **63** OF **63**		RELEASE DATE :	