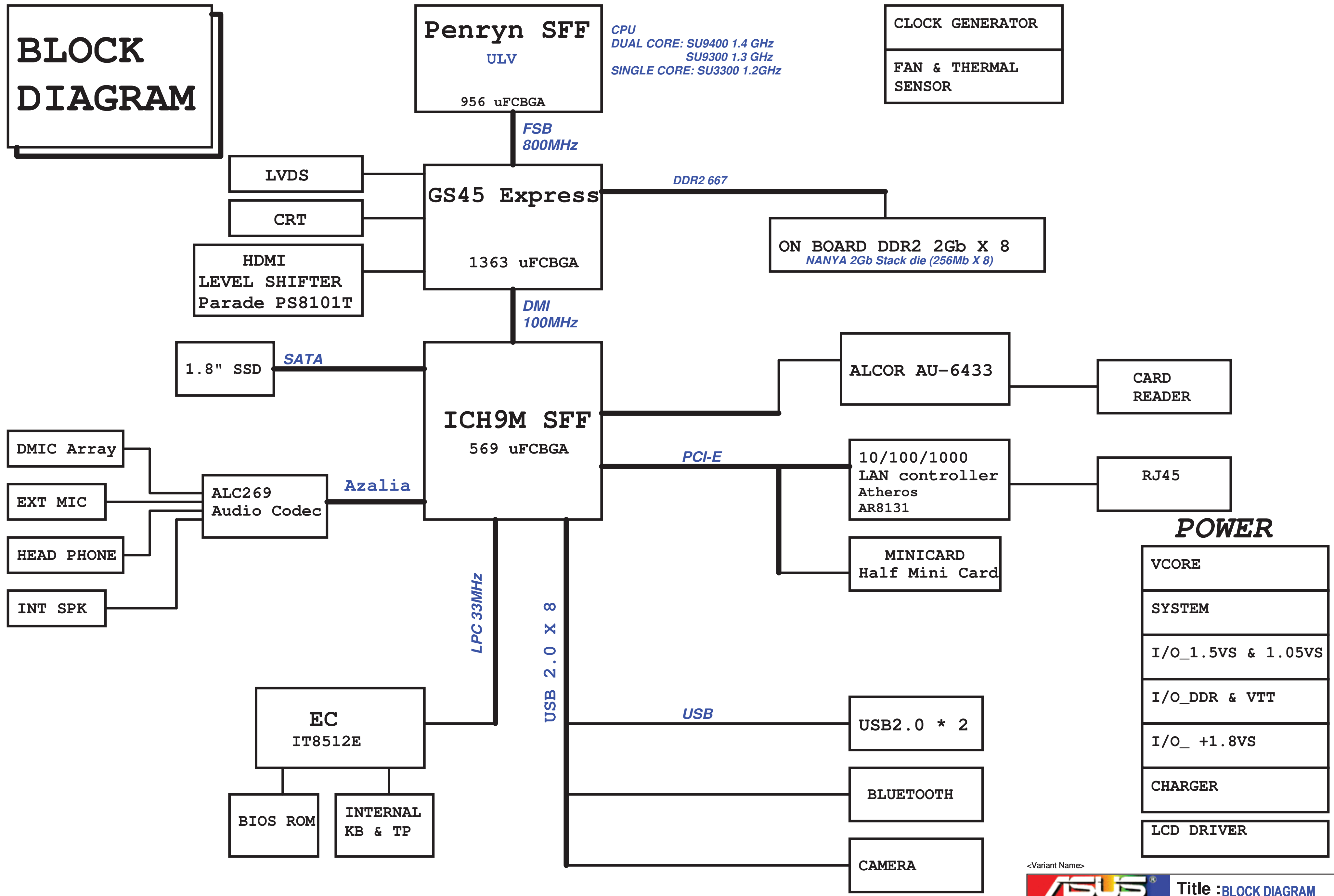
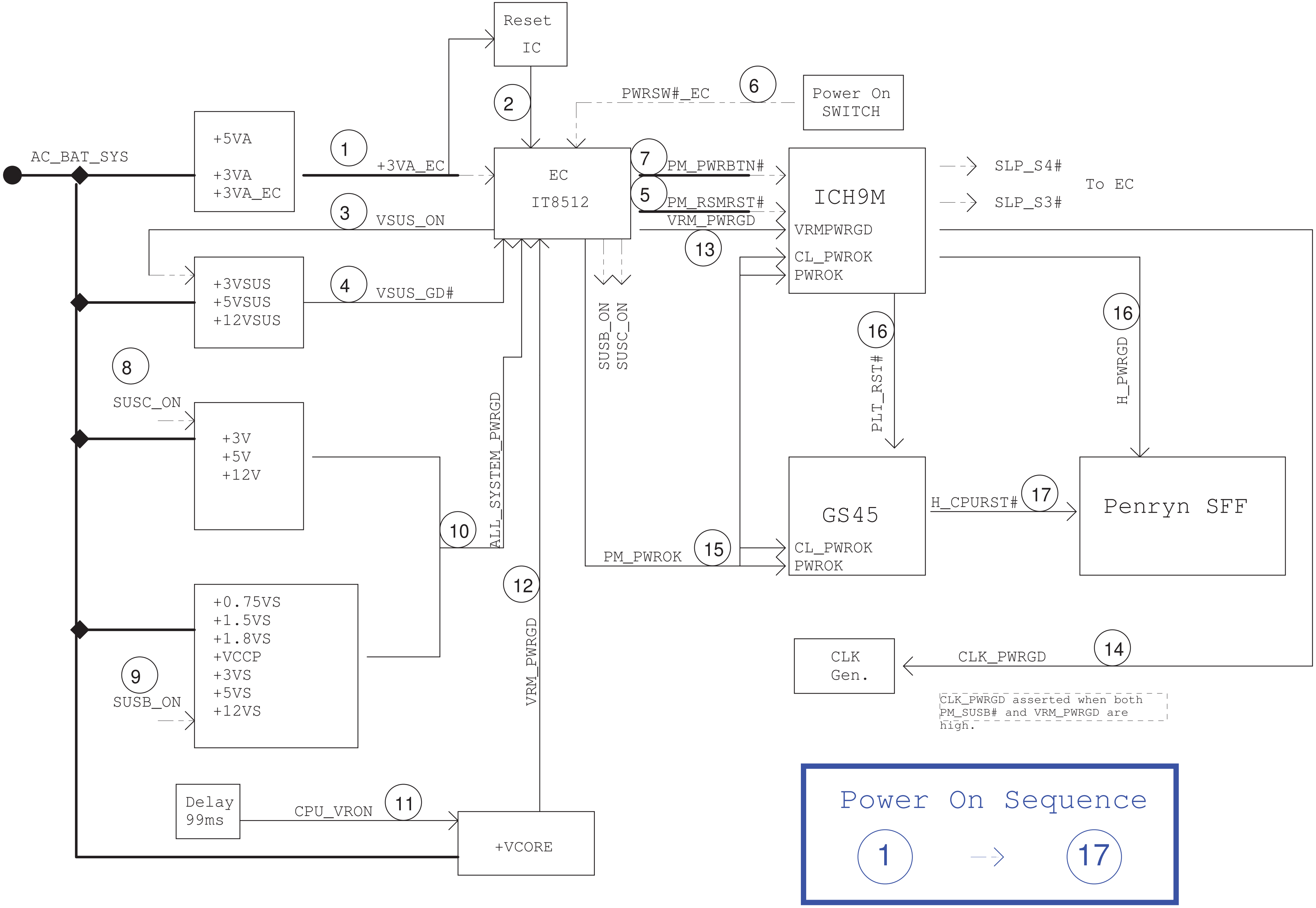
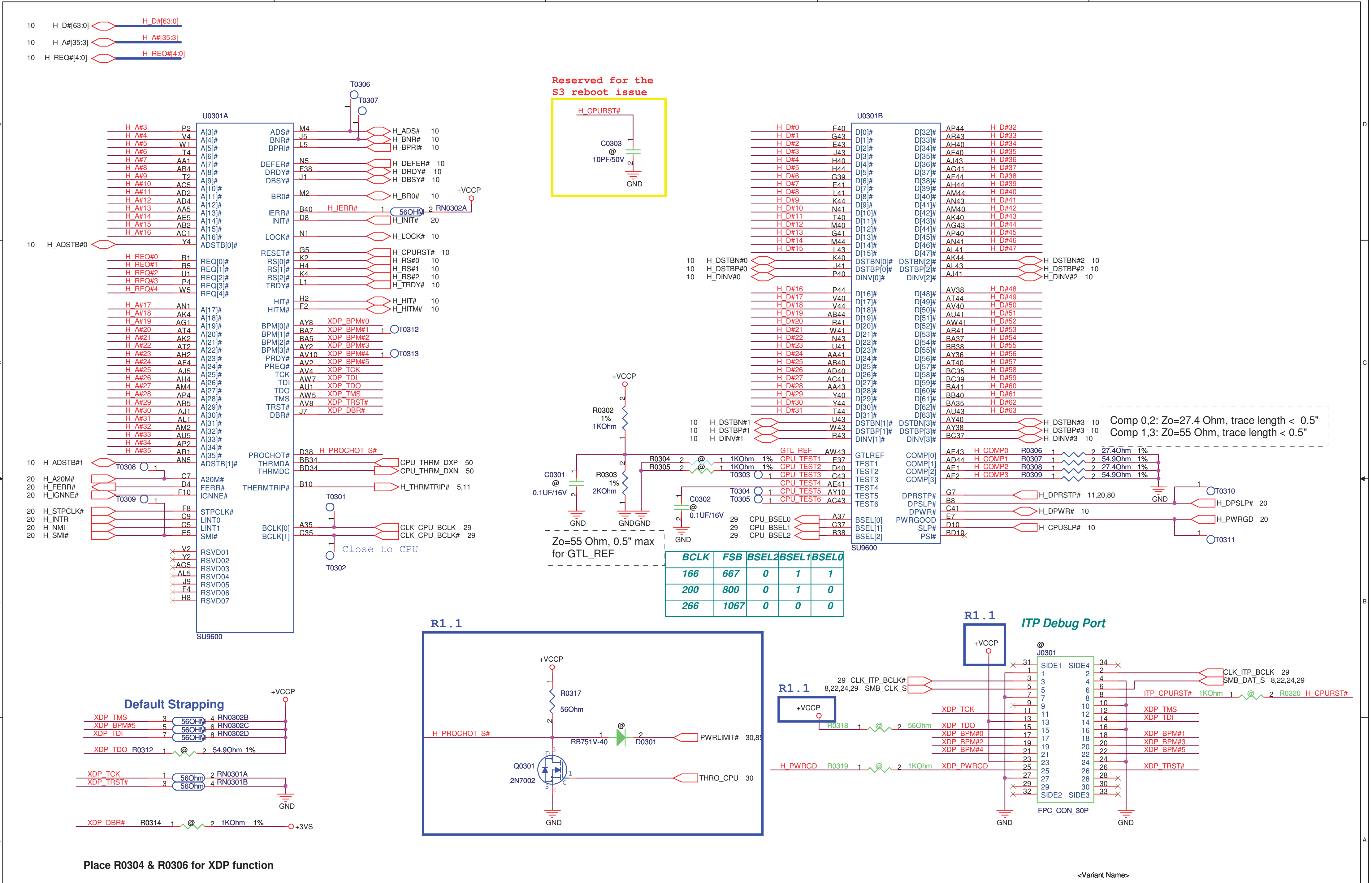


<Variant Name>

ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 1 of 94	



ASUS	Title :	POWER SEQUENCE		
<OrgName>	Engineer:	Uei Lee & Hacken		
Size: Custom	Project Name: UX30 MB			Rev: 2.0
Date: Friday, June 05, 2009		Sheet 2	of 94	



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

<Variant Name>

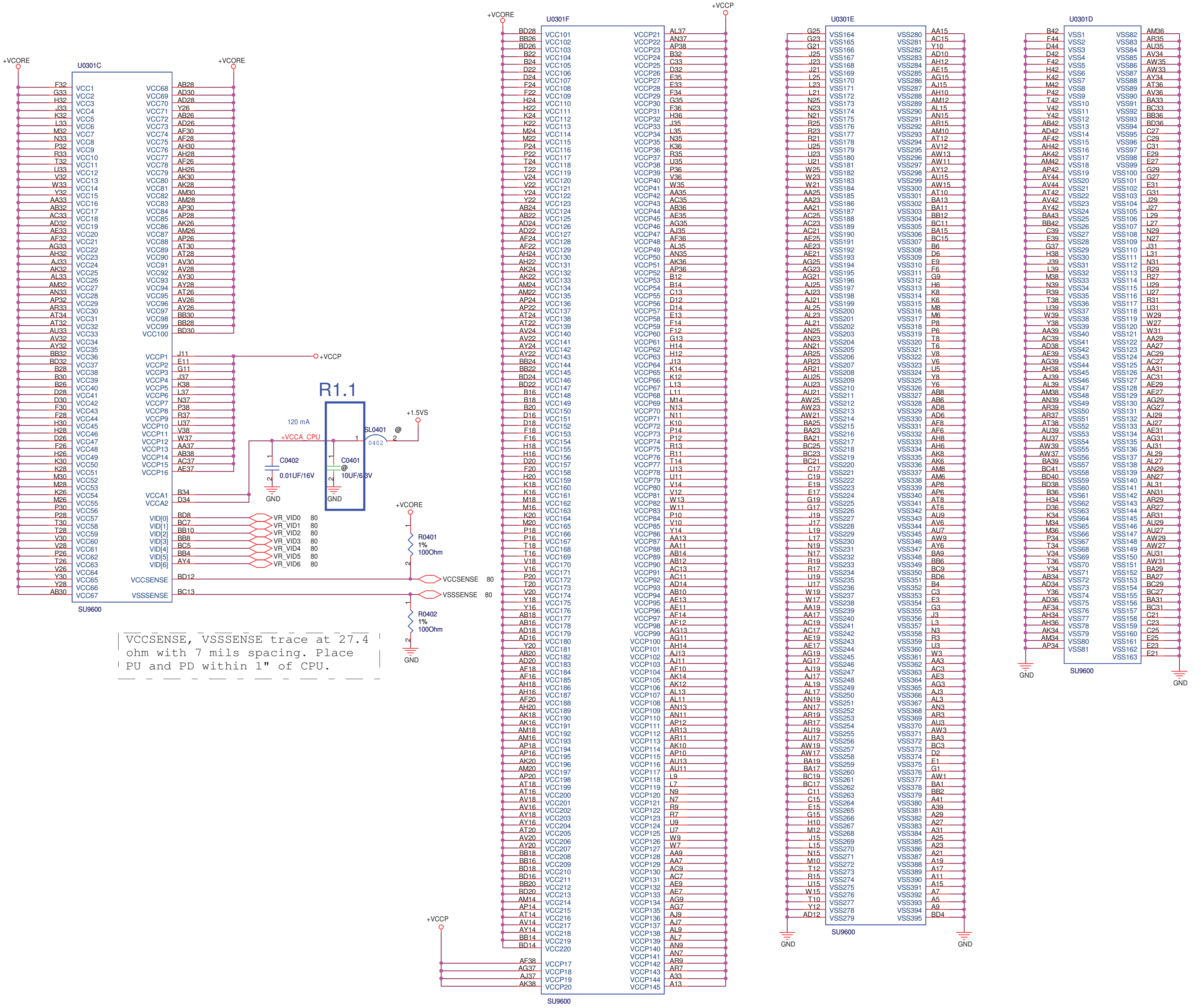
ASUSTeK COMPUTER INC

Title : CPU PENRYN ULV FSB

Engineer: Uei Lee & Hacken

Size: Custom | Project Name: UX30 MB | Rev: 2.0

Date: Wednesday, June 10, 2009 | Sheet 3 of 94



http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU PENRYN ULV POWER

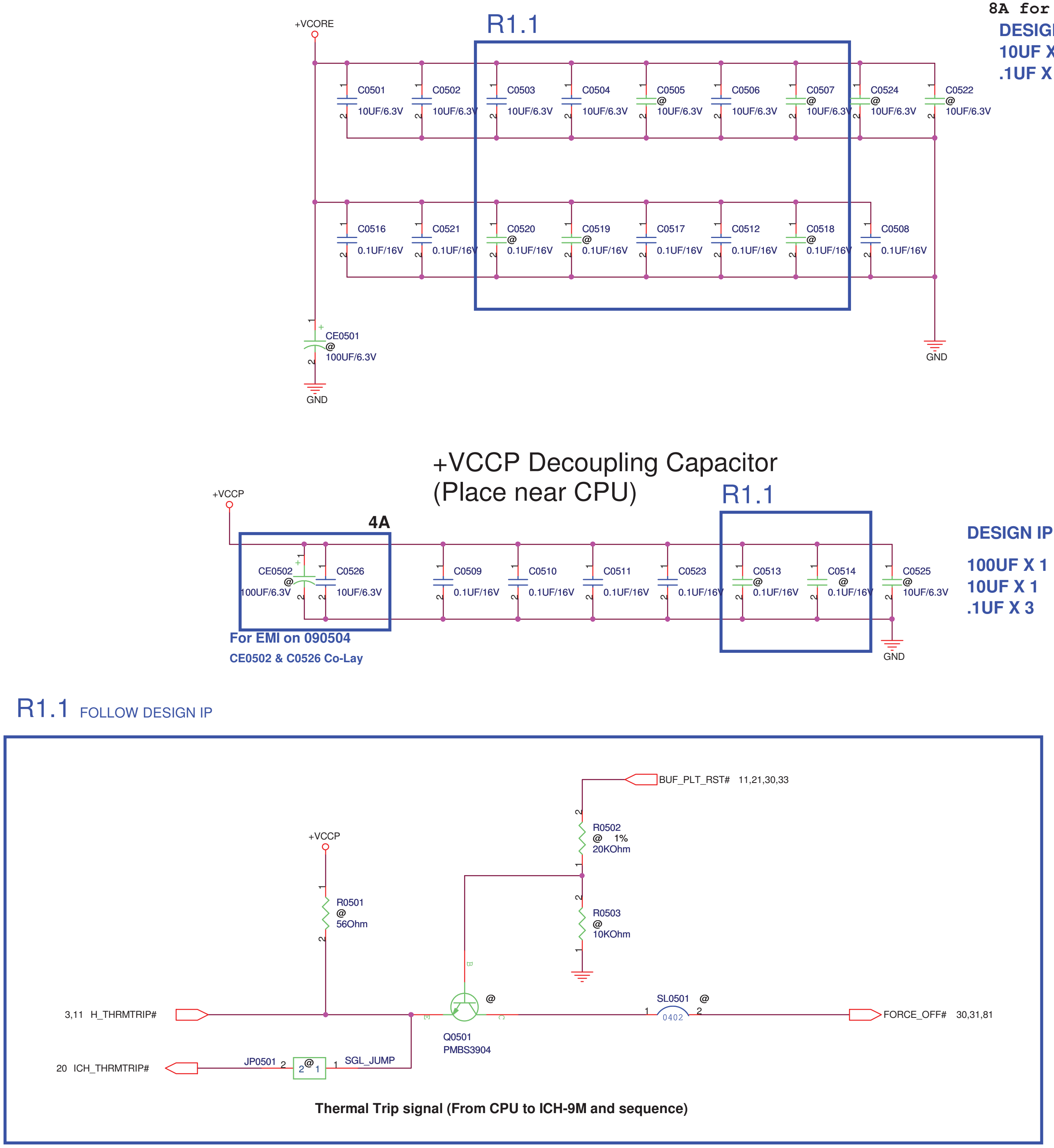
Engineer: Uei Lee & Hacken

Size	Project Name	Rev
C	UX30 MB	2.0

Date: Wednesday, June 10, 2009 Sheet 4 of 94

8A for Ultra Low Voltage CPU TDP 10W

DESIGN IP VCORE
10UF X10
.1UF X 0



DESIGN IP VCCP

100UF X 1
10UF X 1
.1UF X 3

Decoupling guide from Intel

VCORE	10uF mount	*	4pcs
	0.1uF mount	*	5pcs
VCCP	1uF	*	12pcs
	270uF	*	1pcs
VCCA	0.01uF	*	1 pcs
	10uF	*	1 pcs

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU CAPACITORS

Engineer: Uei Lee & Hacken

Size: Custom | Project Name: UX30 MB | Rev: 2.0

Date: Friday, June 05, 2009 | Sheet 5 of 94

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 6 of 94	

<Variant Name>

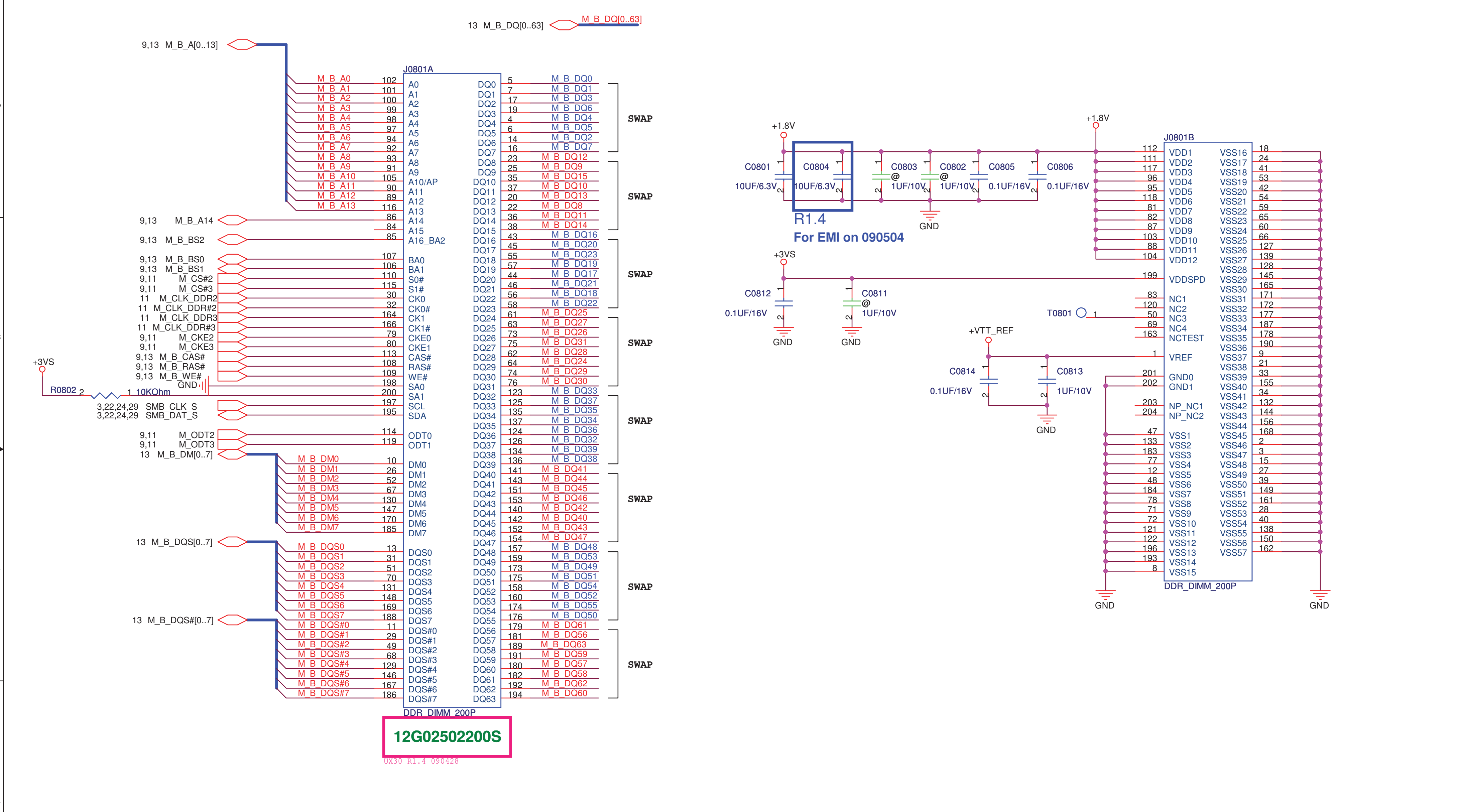
Title : SODIMM

ASUSTeK COMPUTER INC

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
C	UX30 MB	1.4

Date: Friday, June 05, 2009 Sheet 7 of 94



<Variant Name>

ASUSTeK COMPUTER INC

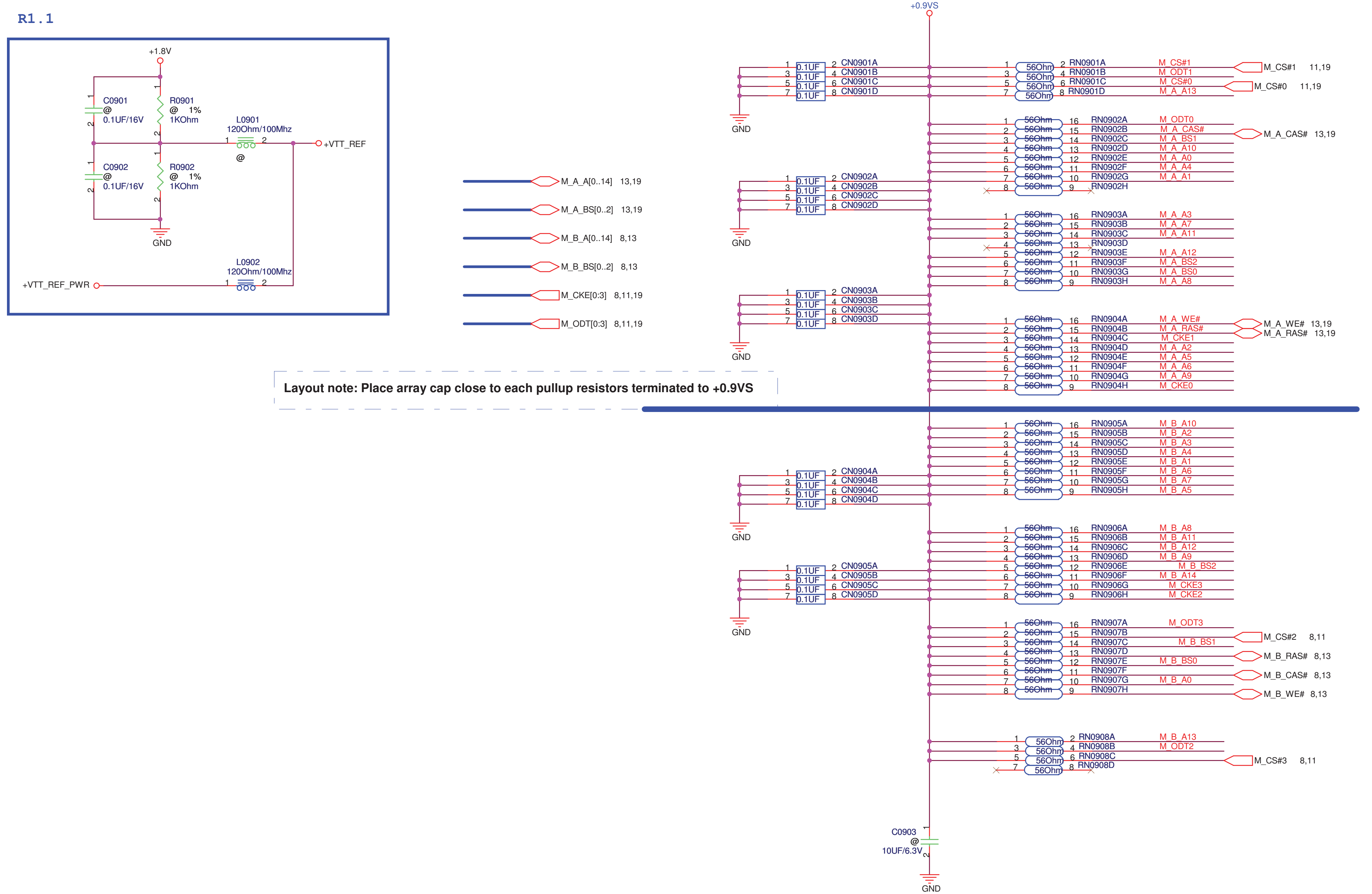
Title : M-DDR3 SP-DIMM CHANNEL B

Engineer: UEI

Size	Project Name	Rev
B	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 8 of 94

R1.1



<Variant Name>

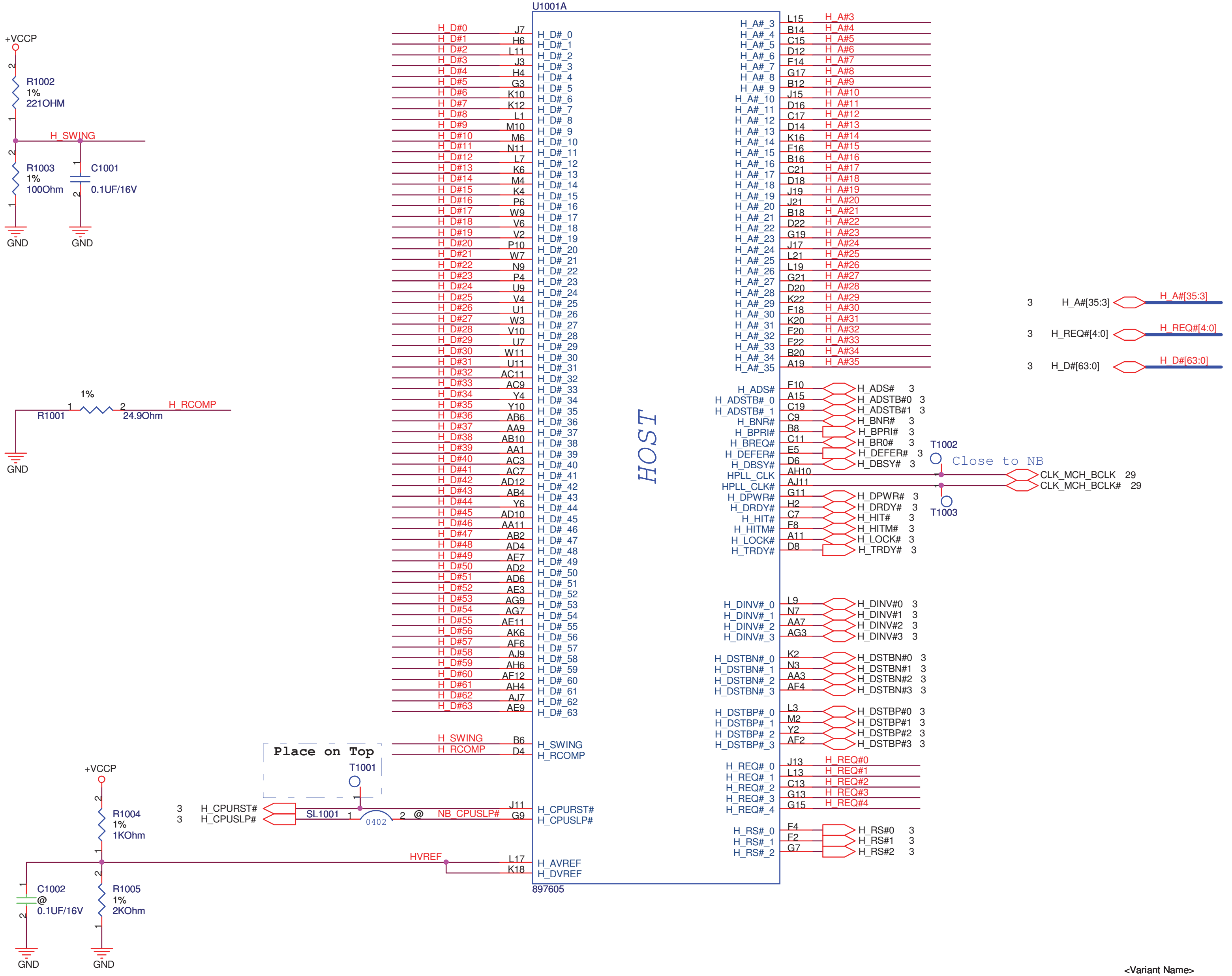
ASUSTeK COMPUTER INC

Title : DIM DDR2 VREF

Engineer: Uei Lee & Hacken

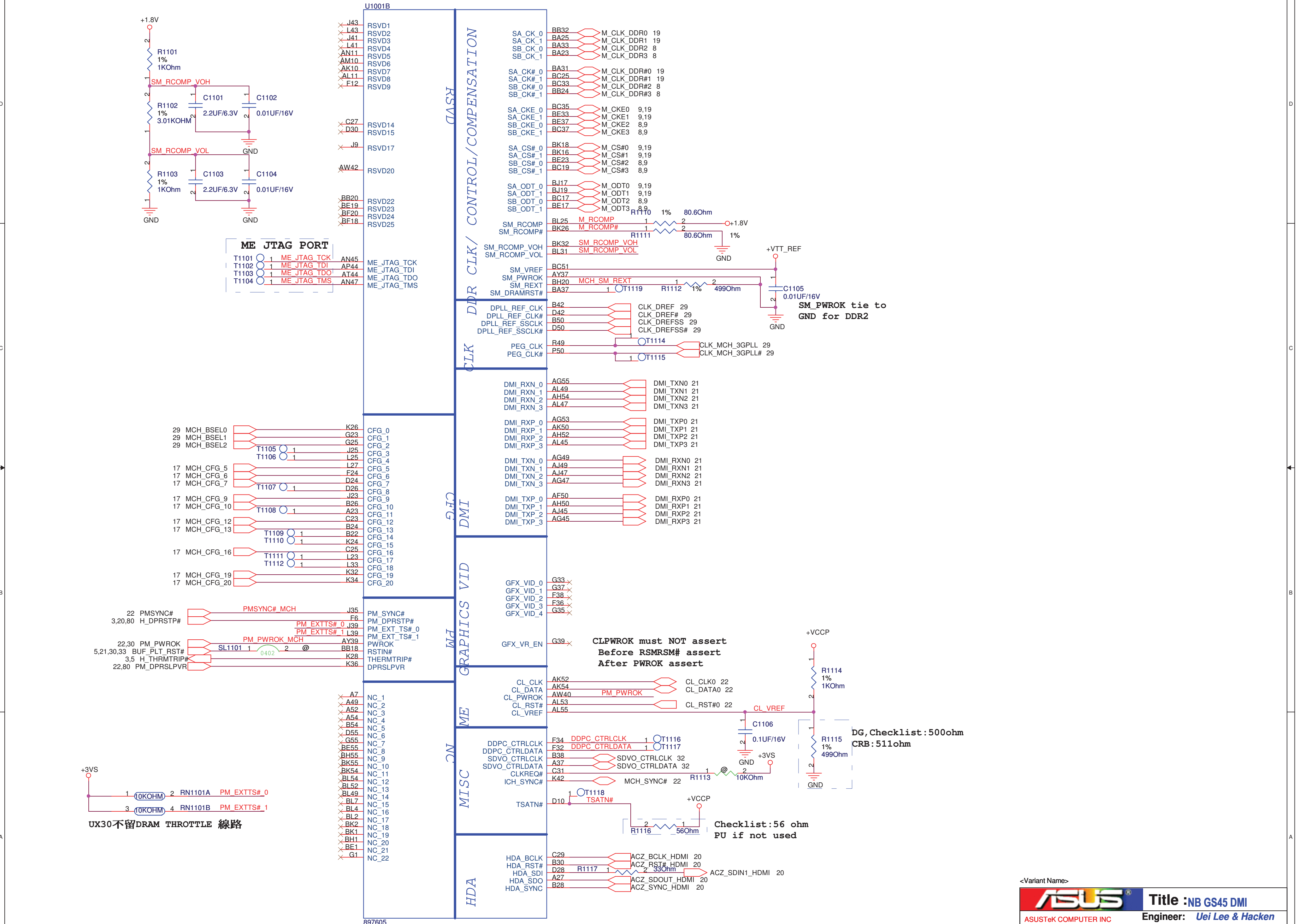
Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 9 of 94



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 HOST		
	Engineer: Uei Lee & Hacken		
Size: Custom	Project Name: UX30 MB		Rev: 2.0
Date: Friday, June 05, 2009	Sheet 10 of 94		



<Variant Name>

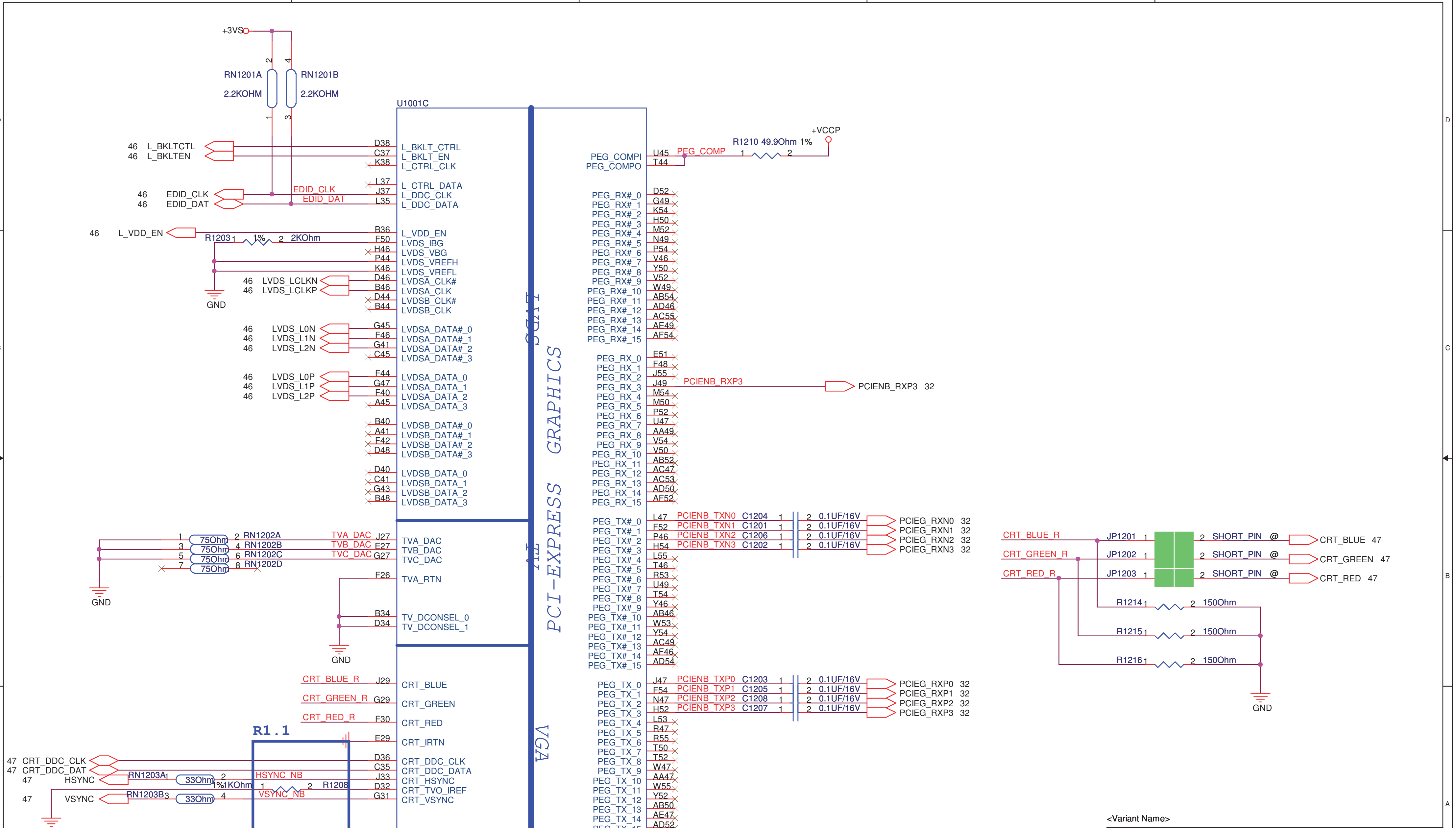
ASUSTeK COMPUTER INC

Title : NB GS45 DMI

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 11 of 94



<Variant Name>

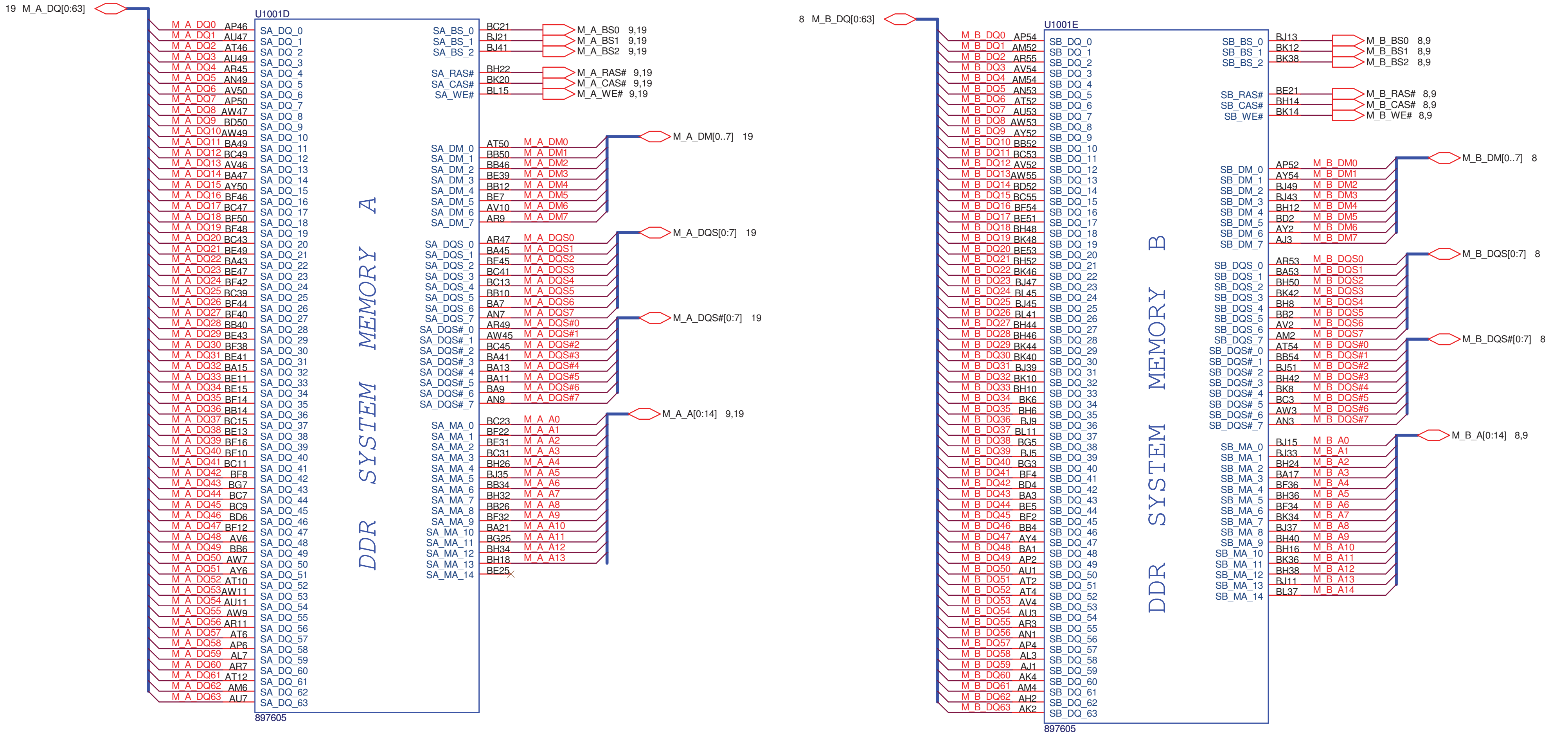
Title : NB GS45 DISPLAY

ASUSTeK COMPUTER INC

Engineer: Uei Lee & Hacken

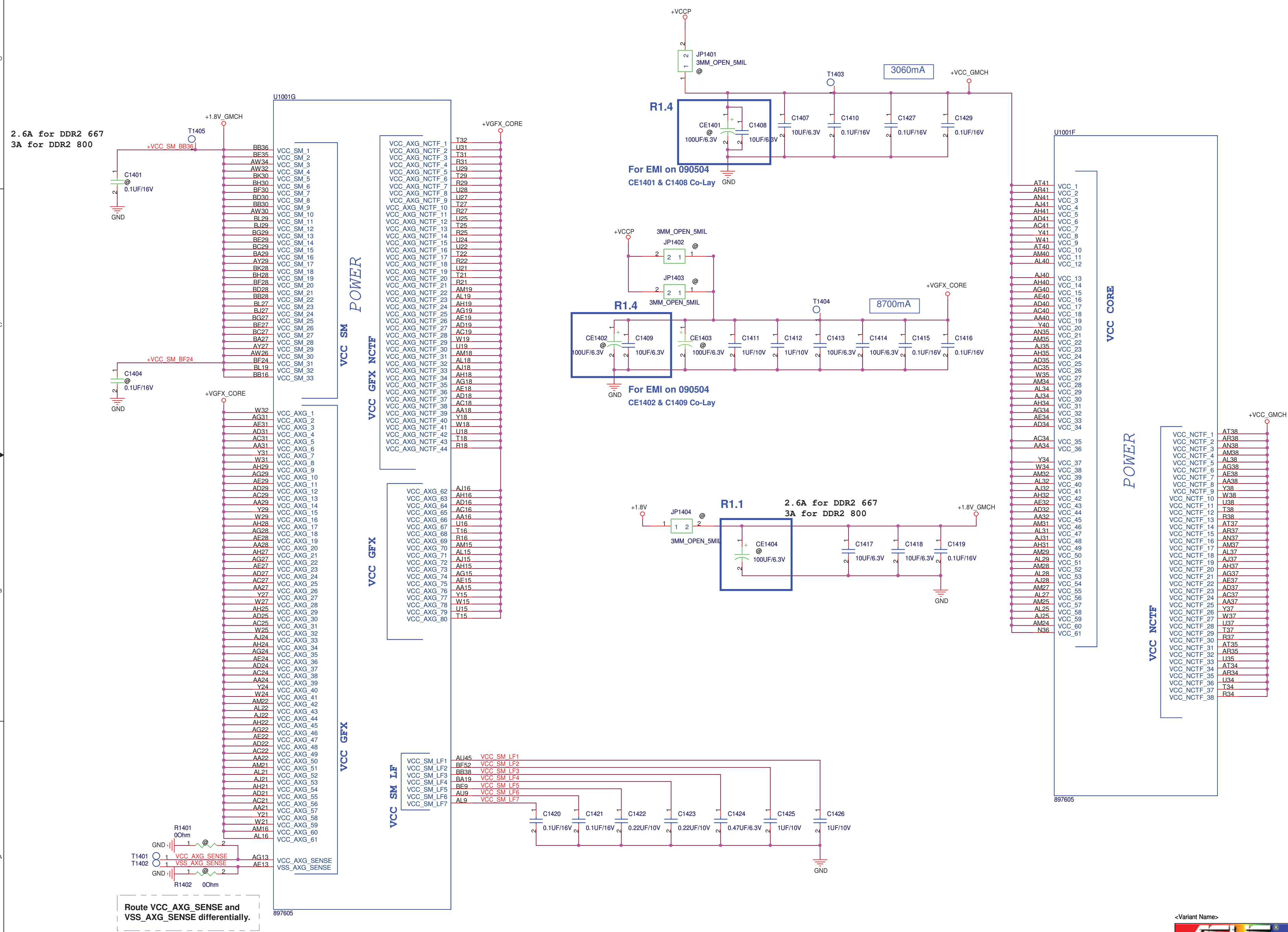
Size	Project Name	Rev
B	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 12 of 94



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 DDR3 BUS	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 13 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

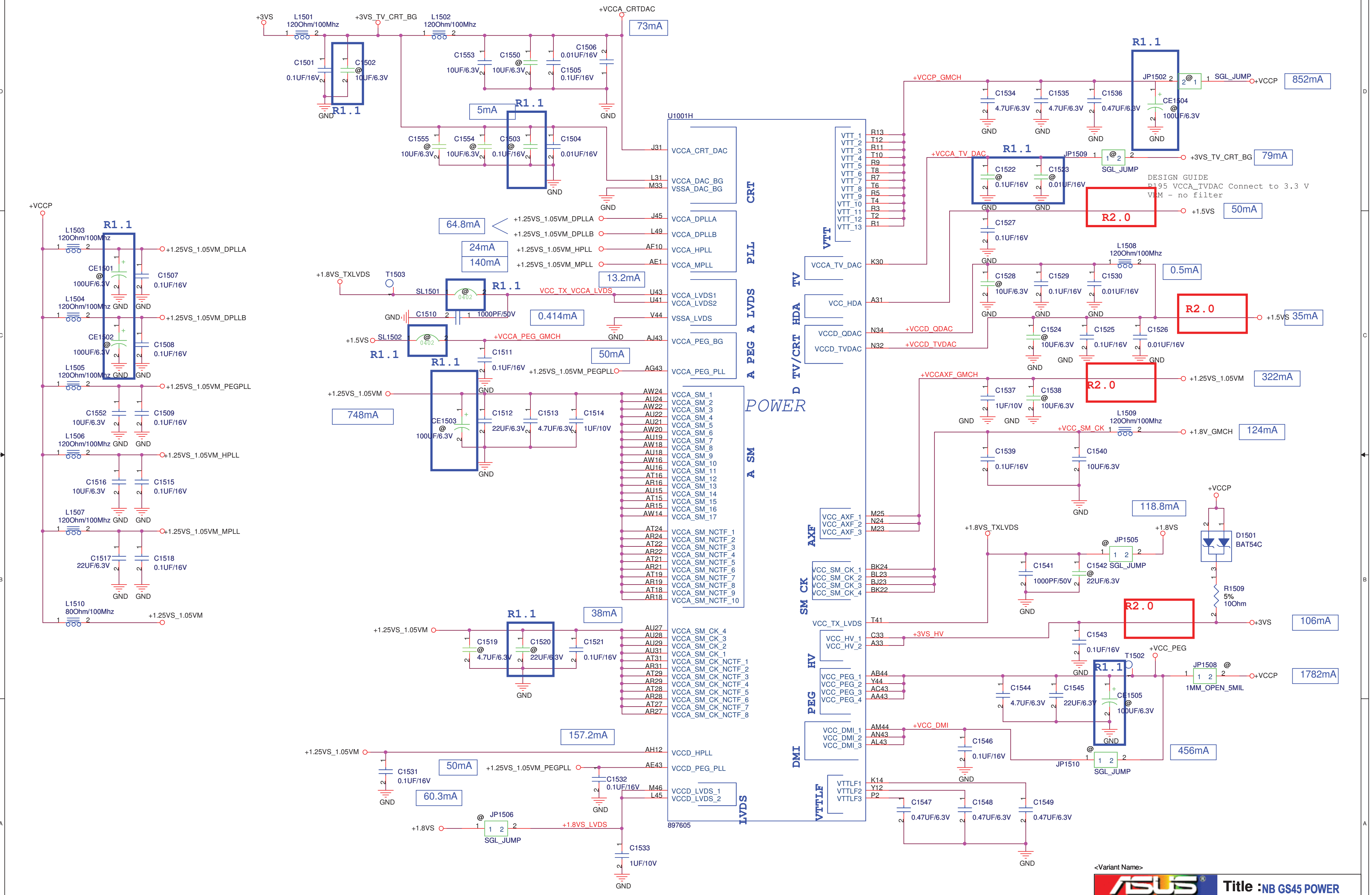
Title : NB GS45 POWER

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
C	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 14 of 94

http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

ASUS

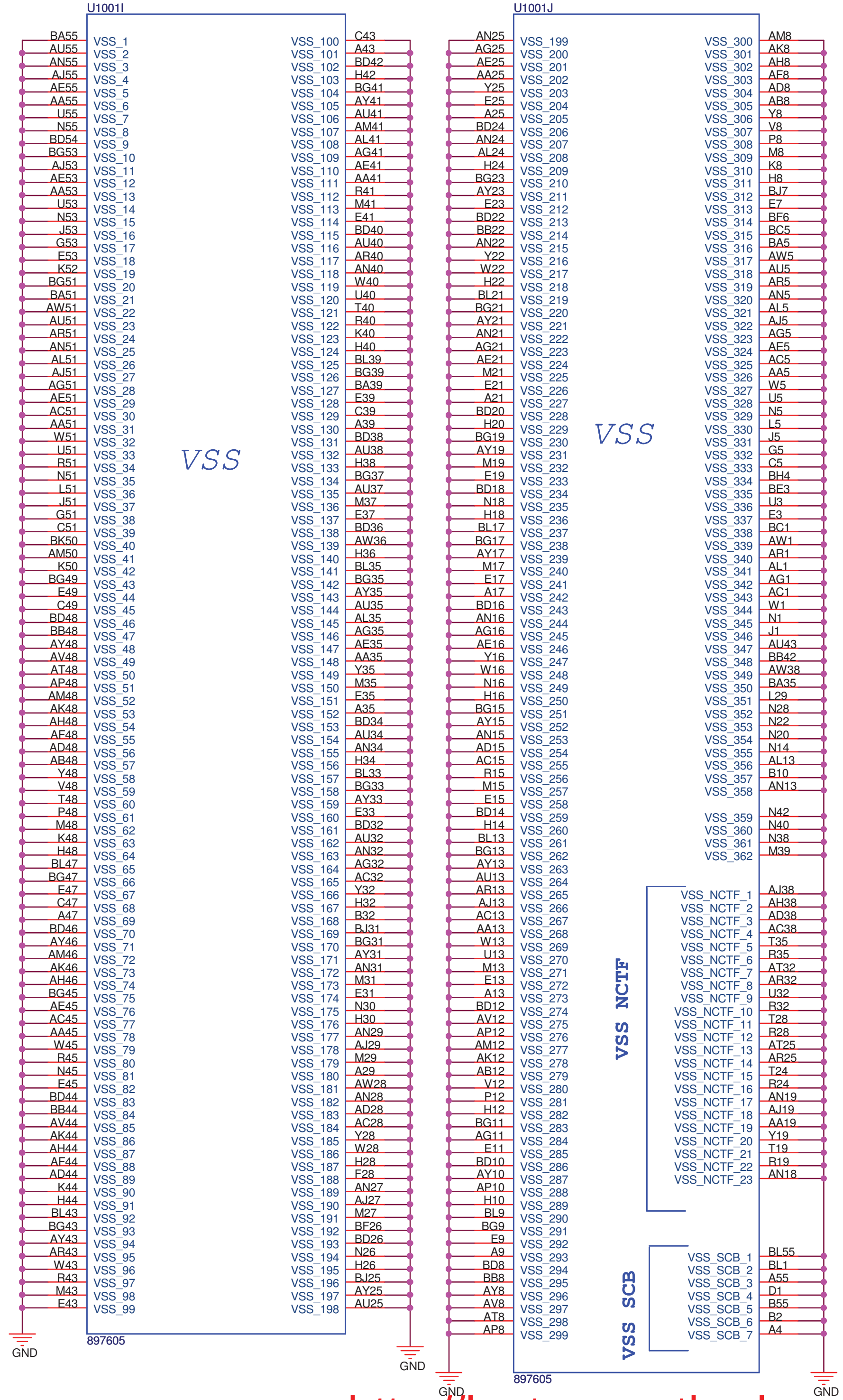
ASUSTeK COMPUTER INC

Title : NB GS45 POWER

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 12, 2009 Sheet 15 of 94



<Variant Name>

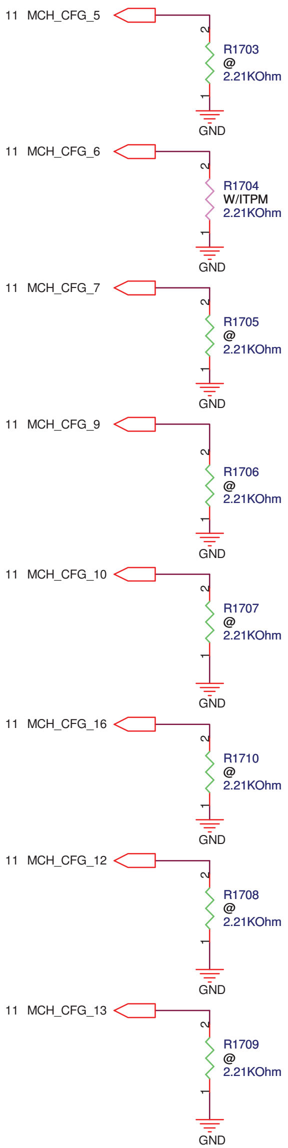
Title : NB GS45 GND

ASUSTeK COMPUTER INC

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 16 of 94



CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface
(Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

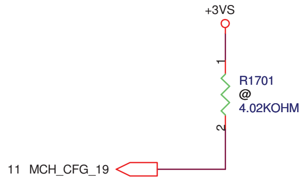
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

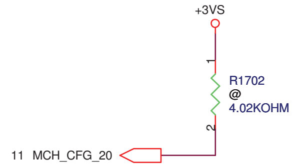
CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 STRAPPING	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 17 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 18 of 94	

<Variant Name>

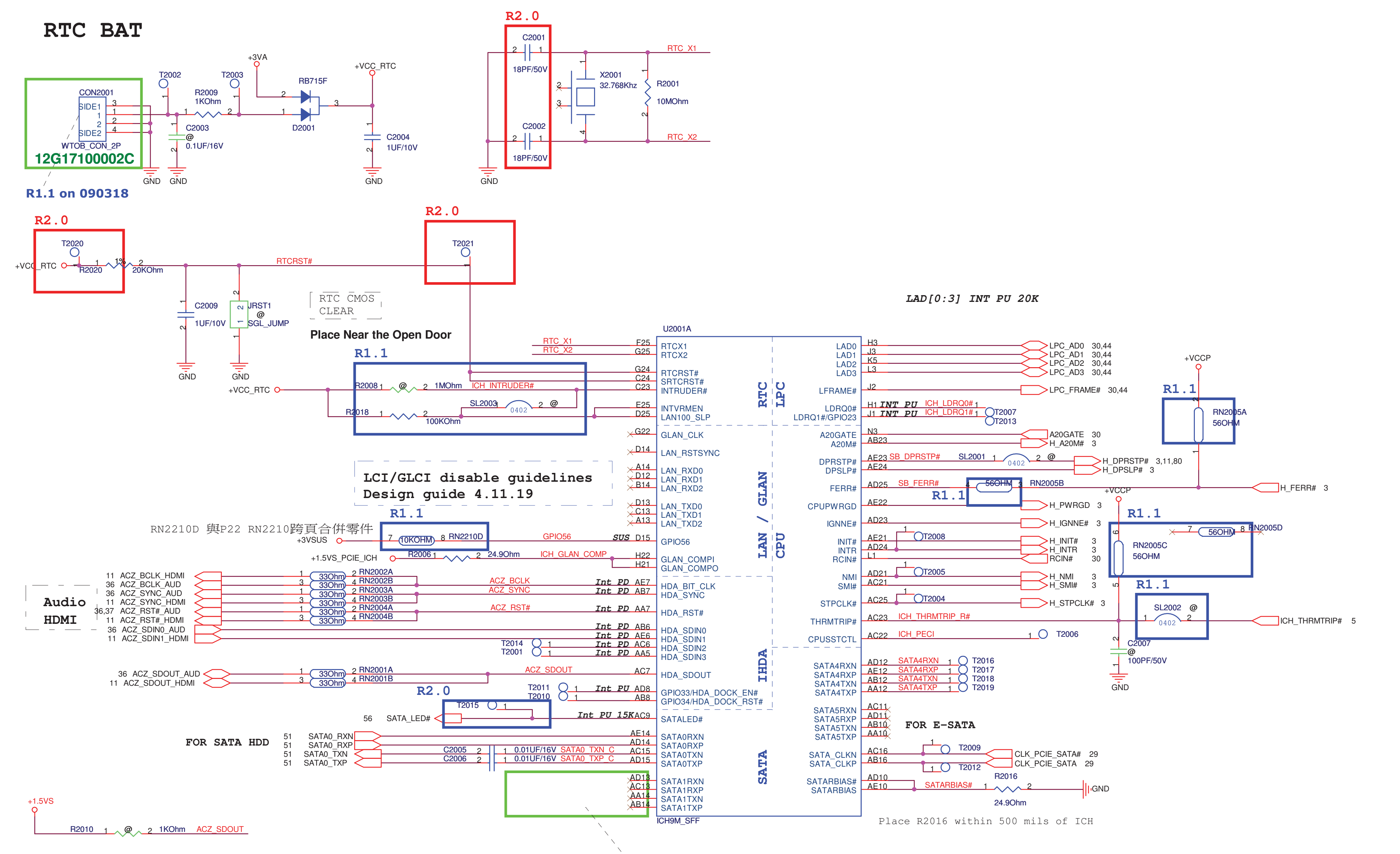
ASUSTeK COMPUTER INC

Title : On Board RAM

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
C	UX30 MB	2.0

Date: Wednesday, June 10, 2009 Sheet 19 of 94



R1.1 on 090401

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1

GPIO33:Flash Descriptor Security Override

High = Enable (Default)
Low = Overridden

<Variant Name>

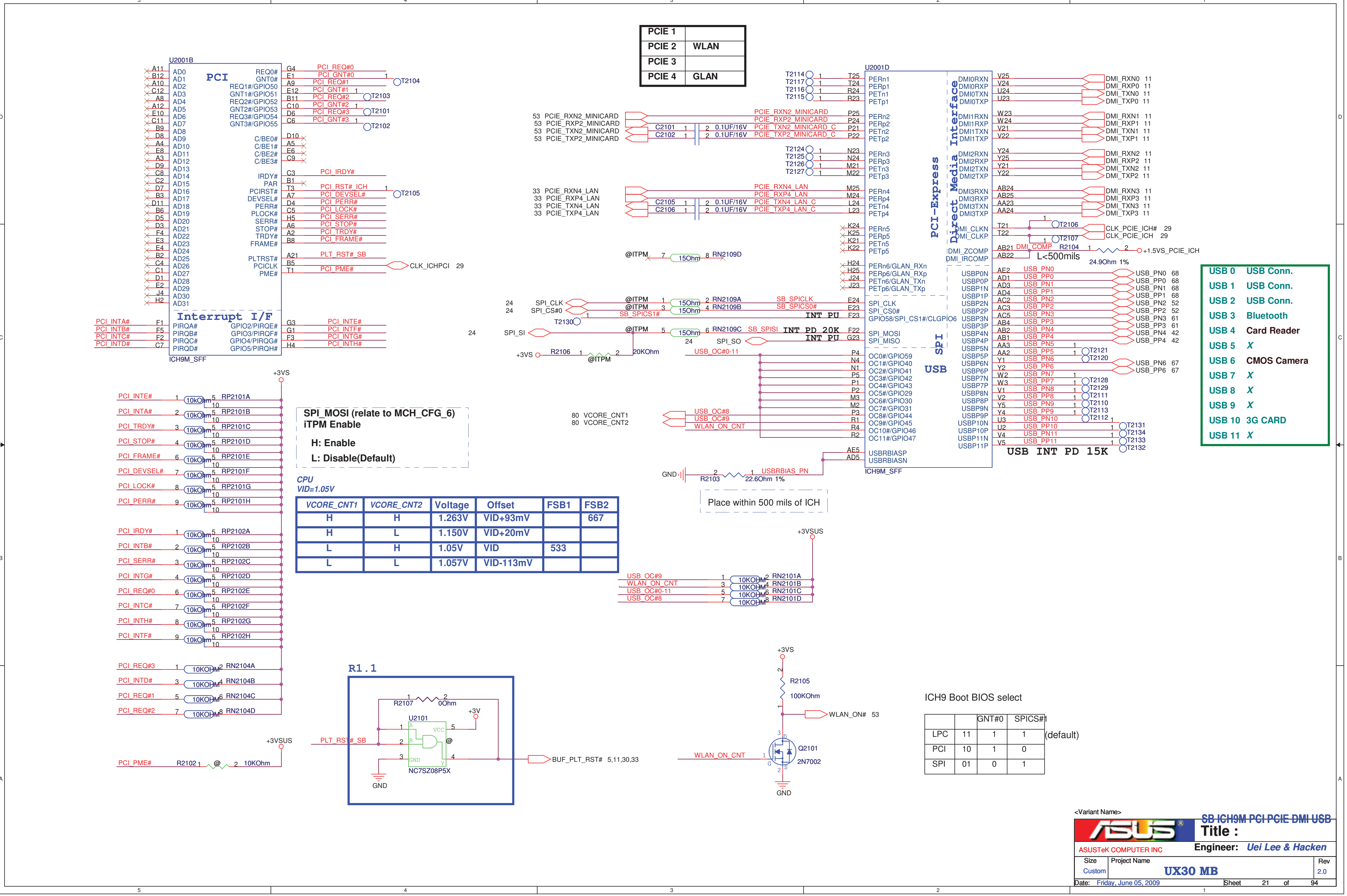
ASUSTeK COMPUTER INC

Title : SB ICH9M PCI PCIE DMI USB

Engineer: *Uei Lee & Hacken*

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Saturday, June 06, 2009 Sheet 20 of 94



PCIE 1	
PCIE 2	WLAN
PCIE 3	
PCIE 4	GLAN

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	Bluetooth
USB 4	Card Reader
USB 5	X
USB 6	CMOS Camera
USB 7	X
USB 8	X
USB 9	X
USB 10	3G CARD
USB 11	X

CPU
VID=1.05V

VCORE_CNT1	VCORE_CNT2	Voltage	Offset	FSB1	FSB2
H	H	1.263V	VID+93mV		667
H	L	1.150V	VID+20mV		
L	H	1.05V	VID	533	
L	L	1.057V	VID-113mV		

ICH9 Boot BIOS select

		GNT#0	SPICS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

<Variant Name>

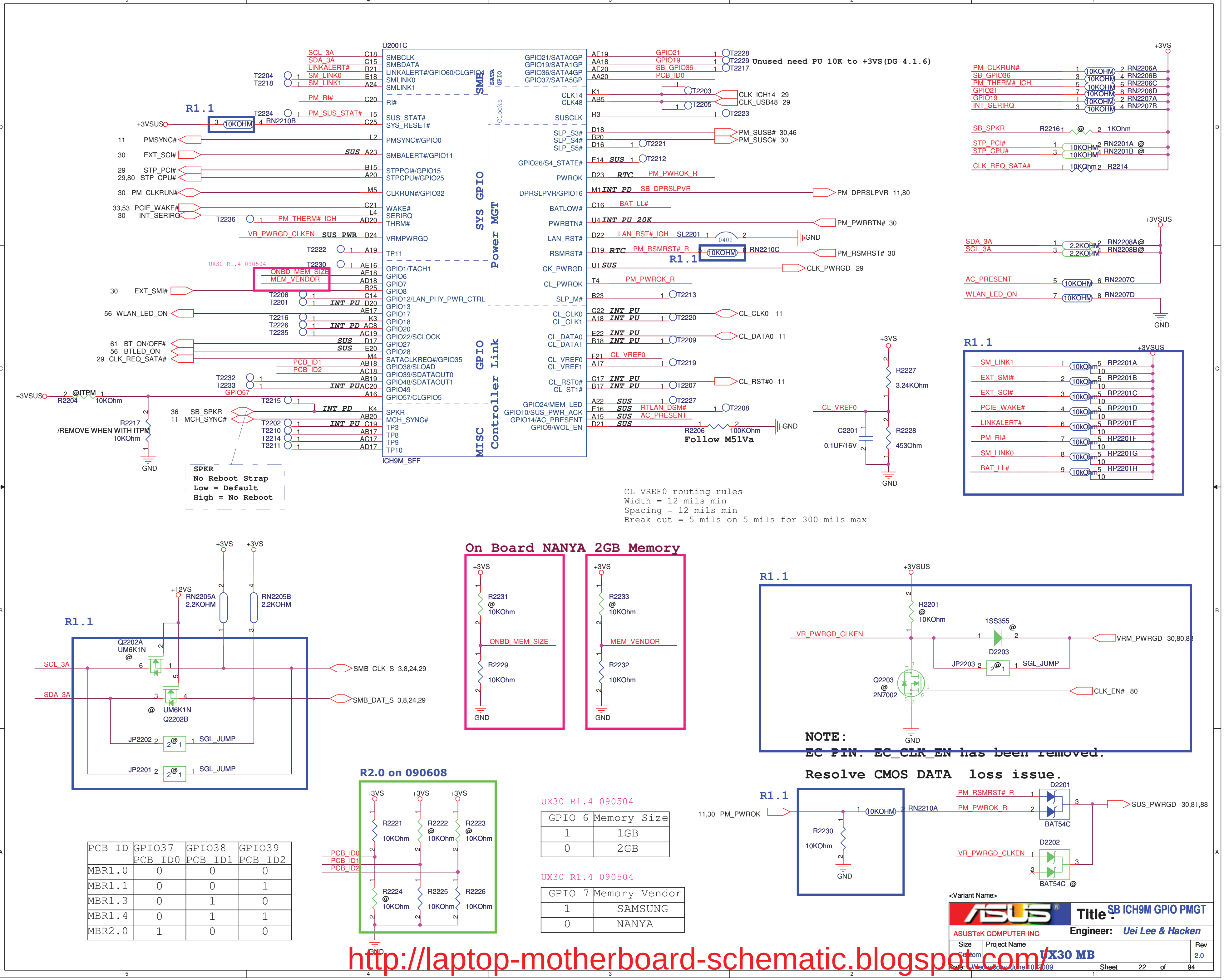
ASUSTeK COMPUTER INC

Title : SB ICH9M PCI PCIE DMI USB

Engineer: Uei Lee & Hacken

Size: Custom | Project Name: UX30 MB | Rev: 2.0

Date: Friday, June 05, 2009 | Sheet 21 of 94



UX30 R1.4 090504

GPIO 6	Memory Size
1	1GB
0	2GB

UX30 R1.4 090504

GPIO 7	Memory Vendor
1	SAMSUNG
0	NANYA

PCB ID	GPIO37 PCB_ID0	GPIO38 PCB_ID1	GPIO39 PCB_ID2
MBR1.0	0	0	0
MBR1.1	0	0	1
MBR1.3	0	1	0
MBR1.4	0	1	1
MBR2.0	1	0	0

<Variant Name>

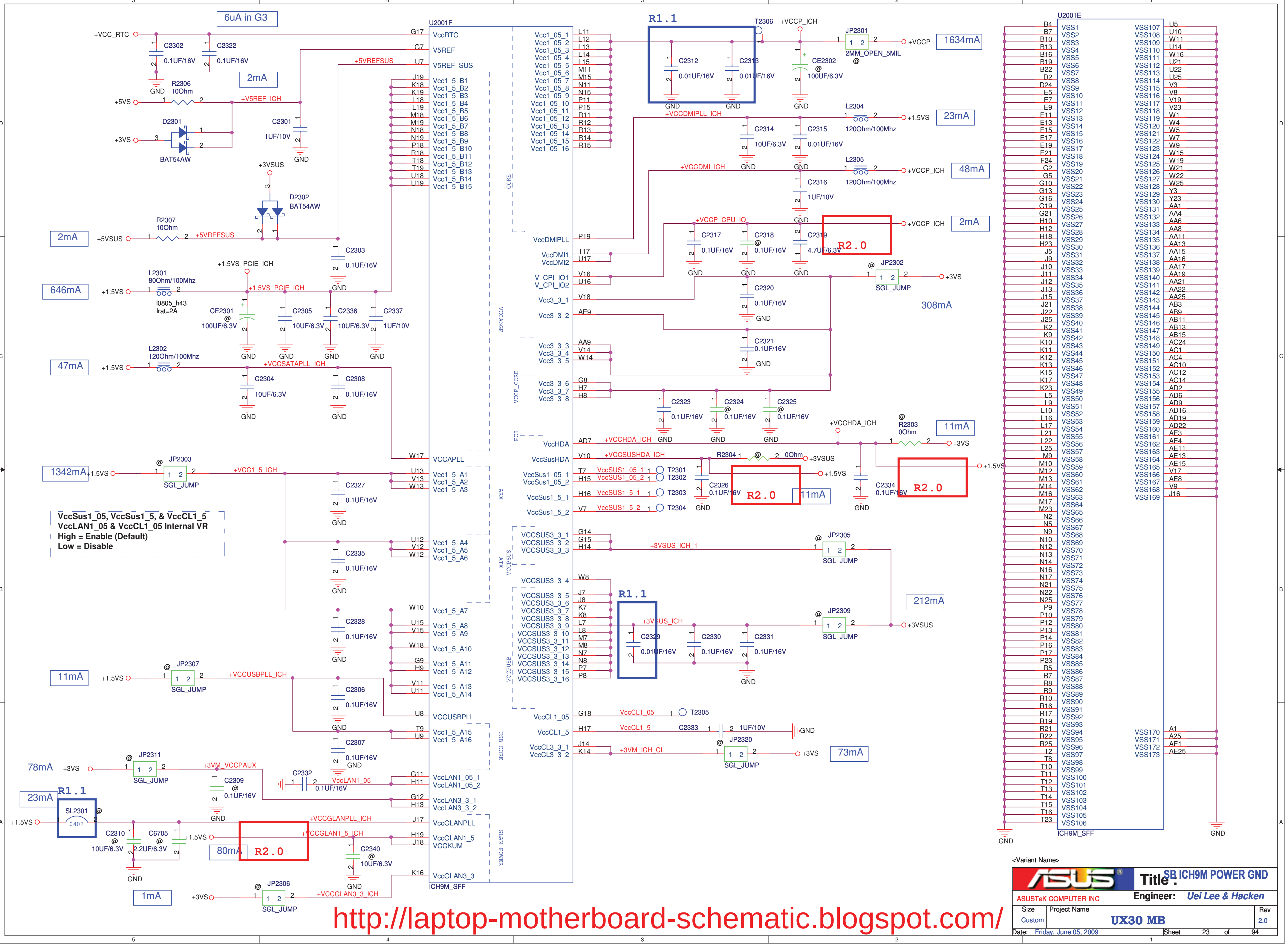
ASUSTeK COMPUTER INC

Title: SB ICH9M GPIO PMGT

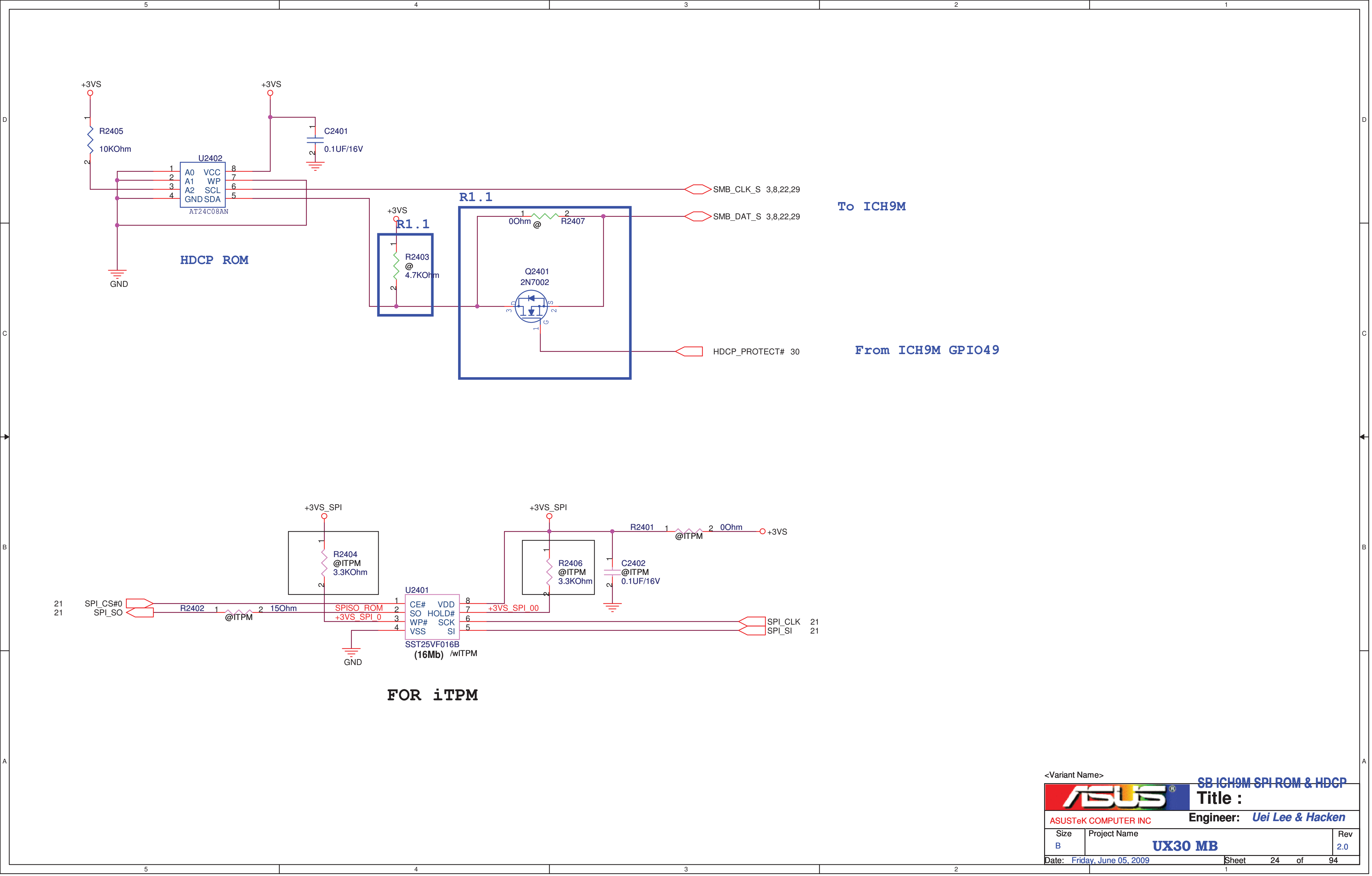
Engineer: Uei Lee & Hacken

Size: Custom | Project Name: UX30 MB | Rev 2.0

Date: Wednesday, June 10, 2009 | Sheet 22 of 94



6uA in G3
+VCC_RTC
C2302 0.1UF/16V
C2322 0.1UF/16V
2mA
R2306 10Ohm
+5VS
+V5REF_ICH
D2301 BAT54AW
+3VS
C2301 1UF/10V
+3VSUS
D2302 BAT54AW
R2307 10Ohm
2mA
+5VSUS
+5VREFSUS
C2303 0.1UF/16V
+1.5VS_PCIE_ICH
L2301 80Ohm/100Mhz
646mA
+1.5VS
l0805_h43
Irat=2A
CE2301 100UF/6.3V
C2305 10UF/6.3V
C2336 10UF/6.3V
C2337 1UF/10V
L2302 120Ohm/100Mhz
47mA
+VCCSATAPLL_ICH
C2304 10UF/6.3V
C2308 0.1UF/16V
JP2303 SGL_JUMP
1342mA
+VCC1_5_ICH
C2327 0.1UF/16V
VccSus1_05, VccSus1_5, & VccCL1_5
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
C2335 0.1UF/16V
C2328 0.1UF/16V
JP2307 SGL_JUMP
11mA
+VCCUSBPLL_ICH
C2306 0.1UF/16V
C2307 0.1UF/16V
JP2311 SGL_JUMP
78mA
+3VM_VCCPAUX
C2309 0.1UF/16V
C2332 0.1UF/16V
VccLAN1_05
23mA
R1.1
SL2301 0402
+1.5VS
C2310 10UF/6.3V
C6705 2.2UF/6.3V
+VCCGLANPLL_ICH
+VCCGLAN1_5_ICH
80mA
R2.0
C2340 10UF/6.3V
1mA
JP2306 SGL_JUMP
+VCCGLAN3_3_ICH
U2001F
VccRTC
V5REF
V5REF_SUS
+5VREFSUS
Vcc1_5_B1 … Vcc1_5_B15
VCCAPLL
Vcc1_5_A1 … Vcc1_5_A16
VCCUSBPLL
VccLAN1_05_1
VccLAN1_05_2
VccLAN3_3_1
VccLAN3_3_2
VccGLANPLL
VccGLAN1_5
VCCKUM
VccGLAN3_3
ICH9M_SFF
Vcc1_05_1 … Vcc1_05_16
VccDMIPLL
VccDMI1
VccDMI2
V_CPI_IO1
V_CPI_IO2
Vcc3_3_1 … Vcc3_3_8
VccHDA
VccSusHDA
VccSus1_05_1
VccSus1_05_2
VccSus1_5_1
VccSus1_5_2
VCCSUS3_3_1 … VCCSUS3_3_16
VccCL1_05
VccCL1_5
VccCL3_3_1
VccCL3_3_2
CORE
VCCA3GP
VCCP_CORE
PCI
ARX
ATX
VCCPSUS
VCCPUSB
USB CORE
GLAN POWER
R1.1
T2306
+VCCP_ICH
C2312 0.01UF/16V
C2313 0.01UF/16V
CE2302 100UF/6.3V
JP2301 2MM_OPEN_5MIL
+VCCP
1634mA
+VCCDMIPLL_ICH
L2304 120Ohm/100Mhz
+1.5VS
23mA
C2314 10UF/6.3V
C2315 0.01UF/16V
+VCCDMI_ICH
L2305 120Ohm/100Mhz
+VCCP_ICH
48mA
C2316 1UF/10V
+VCCP_CPU_IO
+VCCP_ICH
2mA
C2317 0.1UF/16V
C2318 0.1UF/16V
C2319 4.7UF/6.3V
R2.0
JP2302 SGL_JUMP
+3VS
308mA
C2320 0.1UF/16V
C2321 0.1UF/16V
C2323 0.1UF/16V
C2324 0.1UF/16V
C2325 0.1UF/16V
+VCCHDA_ICH
R2303 0Ohm
11mA
+VCCSUSHDA_ICH
R2304 0Ohm
+3VSUS
VccSUS1_05_1 T2301
VccSUS1_05_2 T2302
VccSUS1_5_1 T2303
VccSUS1_5_2 T2304
C2326 0.1UF/16V
R2.0
11mA
C2334 0.1UF/16V
R2.0
JP2305 SGL_JUMP
+3VSUS_ICH_1
212mA
R1.1
JP2309 SGL_JUMP
+3VSUS_ICH
+3VSUS
C2329 0.01UF/16V
C2330 0.1UF/16V
C2331 0.1UF/16V
VccCL1_05 T2305
VccCL1_5
C2333 1UF/10V
JP2320 SGL_JUMP
+3VM_ICH_CL
73mA
U2001E
VSS1 … VSS173
ICH9M_SFF
GND
<Variant Name>
ASUS
Title : SB ICH9M POWER GND
ASUSTeK COMPUTER INC
Engineer: Uei Lee & Hacken
Size Custom
Project Name UX30 MB
Rev 2.0
Date: Friday, June 05, 2009
Sheet 23 of 94



HDCP ROM
+3VS
R2405
10KOhm
C2401
0.1UF/16V
U2402
A0 VCC
A1 WP
A2 SCL
GND SDA
AT24C08AN
GND
SMB_CLK_S 3,8,22,29
SMB_DAT_S 3,8,22,29
To ICH9M
R1.1
0Ohm @
R2407
R2403
@
4.7KOhm
Q2401
2N7002
HDCP_PROTECT# 30
From ICH9M GPIO49
+3VS_SPI
R2404
@ITPM
3.3KOhm
R2401
0Ohm
@ITPM
R2406
@ITPM
3.3KOhm
C2402
@ITPM
0.1UF/16V
U2401
CE# VDD
SO HOLD#
WP# SCK
VSS SI
SST25VF016B
(16Mb) /wITPM
SPISO_ROM
+3VS_SPI_0
+3VS_SPI_00
SPI_CS#0 21
SPI_SO 21
R2402
15Ohm
SPI_CLK 21
SPI_SI 21
FOR iTPM
<Variant Name>
ASUSTeK COMPUTER INC
Title : SB ICH9M SPI ROM & HDCP
Engineer: Uei Lee & Hacken
Size B
Project Name UX30 MB
Rev 2.0
Date: Friday, June 05, 2009
Sheet 24 of 94

<Variant Name>

ASUS	Title :*	
ASUSTeK COMPUTER INC	Engineer: *Uei Lee & Hacken*	
Size: A	Project Name: **UX30 MB**	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 25 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 26 of 94	

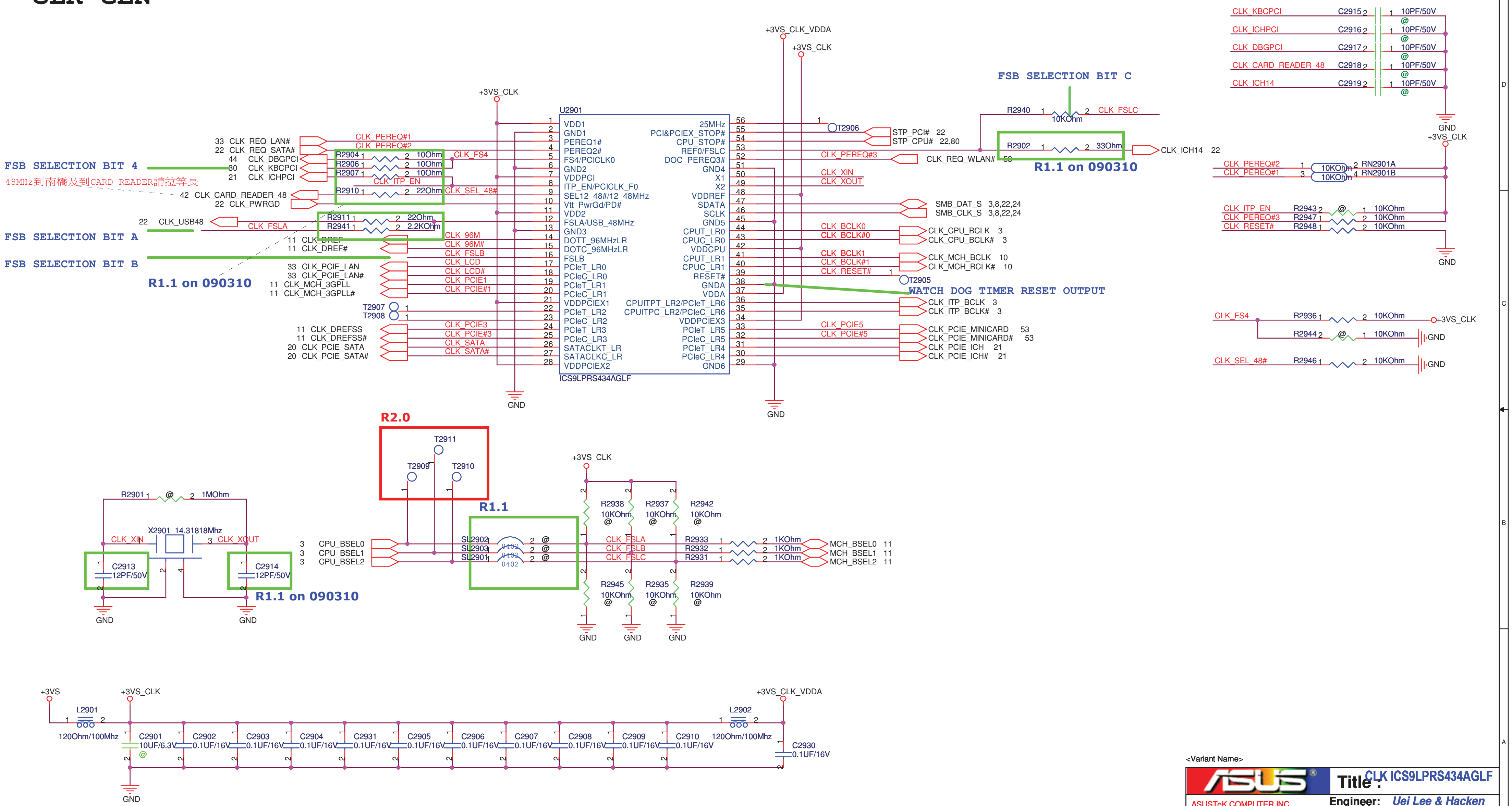
<Variant Name>

ASUS	Title :*		
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 05, 2009	Sheet 27 of 94		

<Variant Name>

ASUS	Title :*		
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 05, 2009		Sheet 28 of 94	

CLK GEN



<Variant Name>

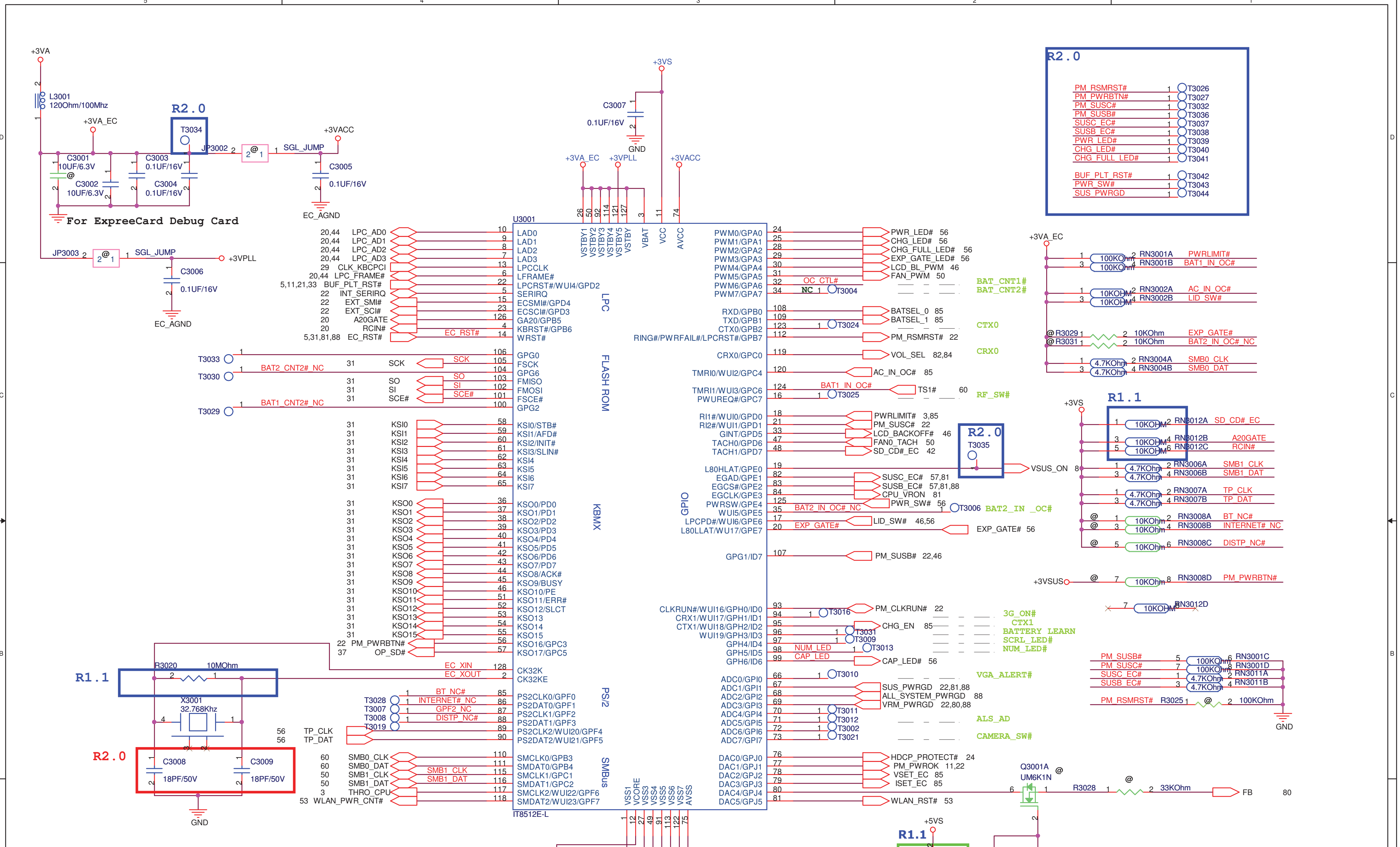
ASUSTeK COMPUTER INC

Title : CLK ICS9LPRS434AGLF

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 29 of 94



EXPRESS GATE 與 PWR4GEAR#共用PIN.移至GPF2

GPJ4 DRAM THROTTE 不支援

改VCORE FEEDBACK 電壓調整,由GPA3控制ON/OFF

<Variant Name>

ASUSTeK COMPUTER INC

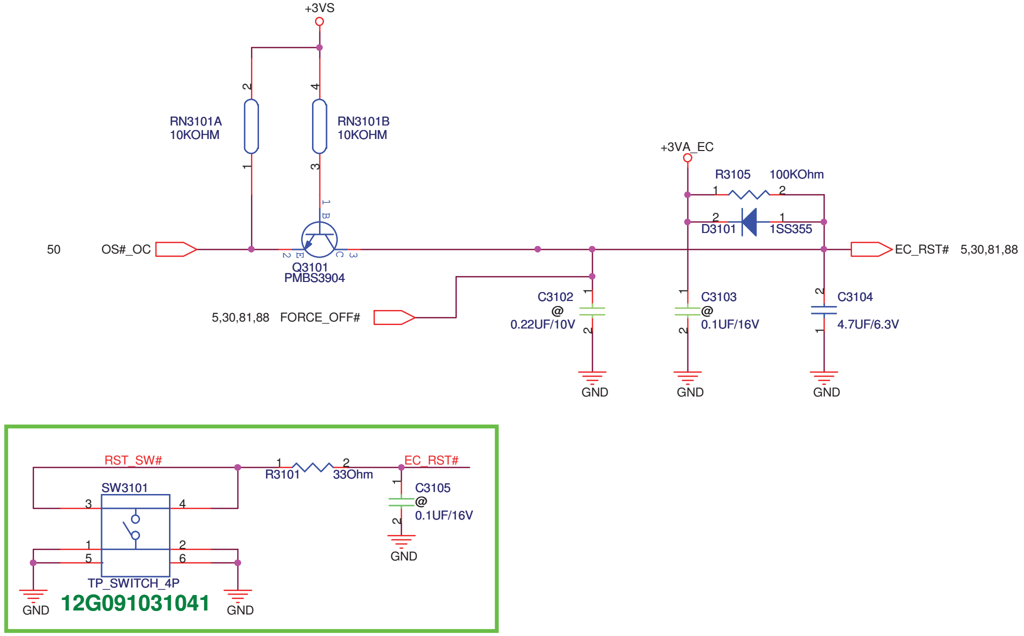
Title : KBC ITE8512

Engineer: Uei Lee & Hacken

Size: Custom | Project Name: UX30 MB | Rev: 2.0

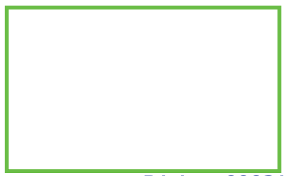
Date: Saturday, June 06, 2009 | Sheet 30 of 94

EC RESET



R2.0 on 090602

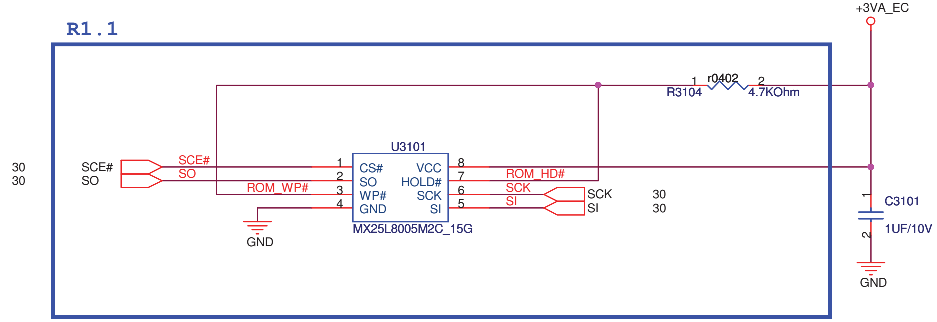
HALL SENSOR



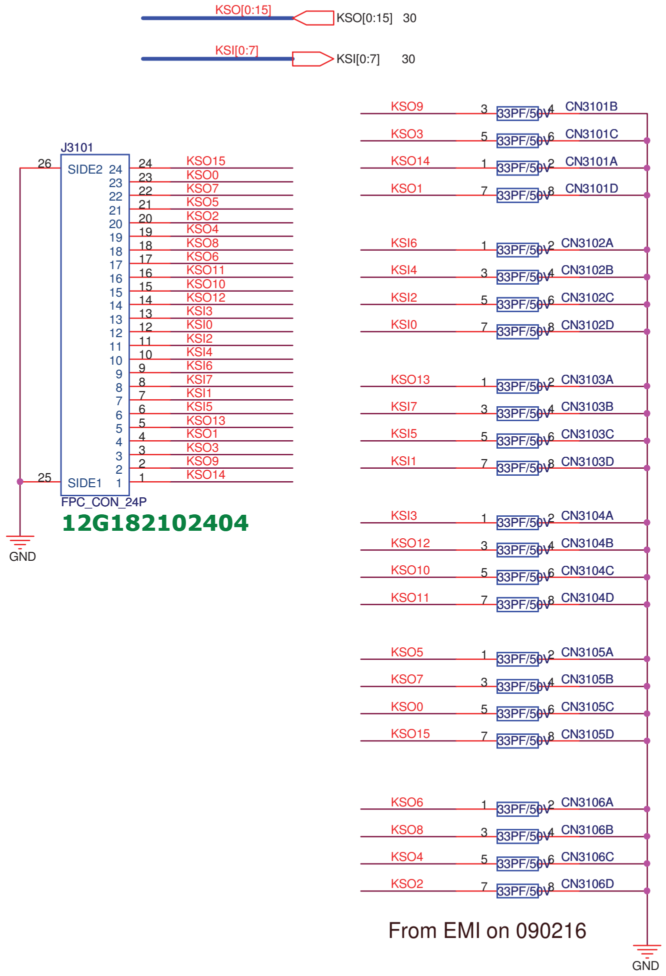
R1.1 on 090310

8Mb SPI ROM

R1.1



Internal Keyboard



From EMI on 090216

<Variant Name>

ROM FLASH ROM TOUCH PAD KB

ASUSTeK COMPUTER INC

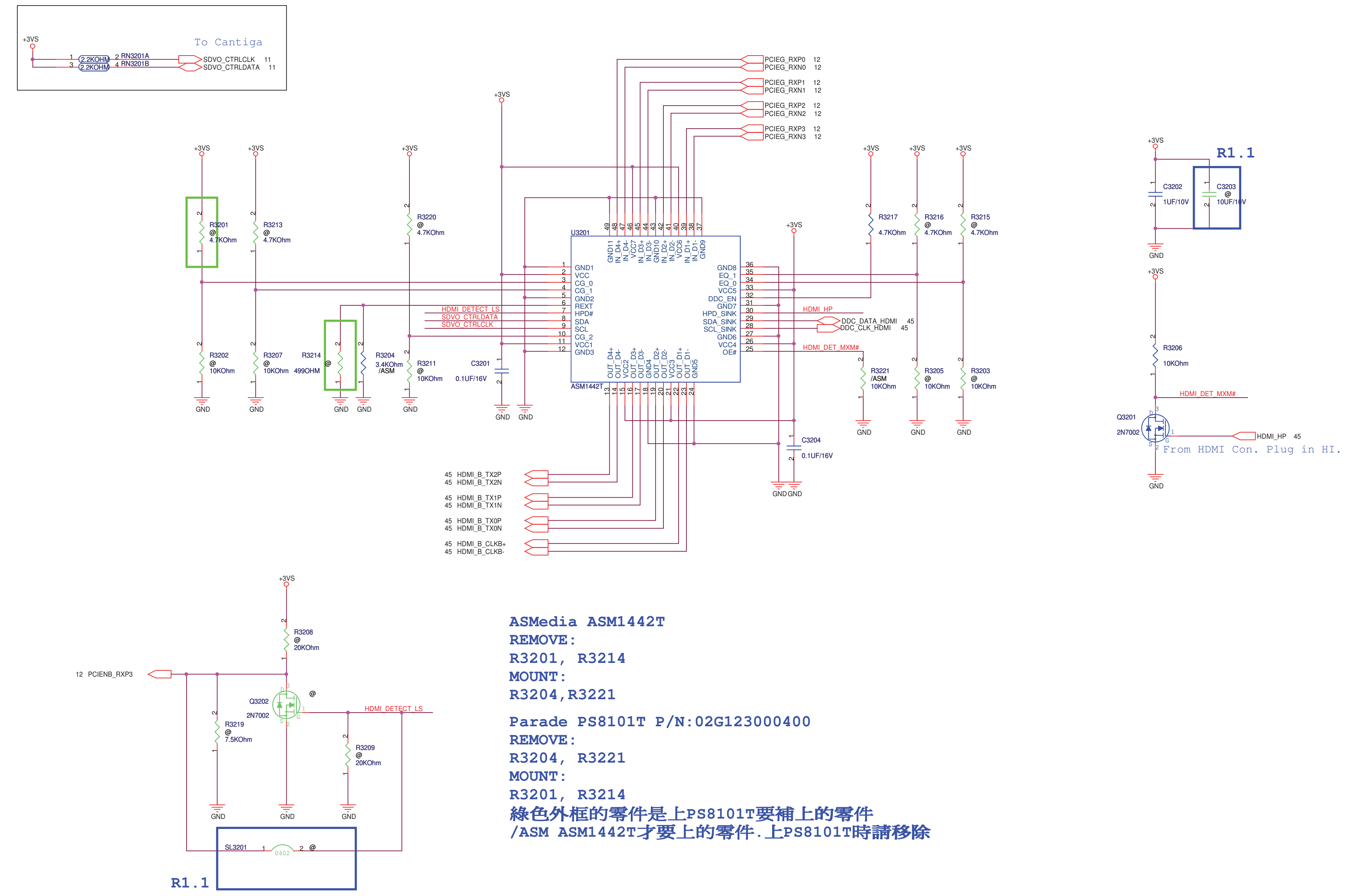
Title :

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Monday, June 08, 2009 Sheet 31 of 94

UMA LEVEL SHIFTERS

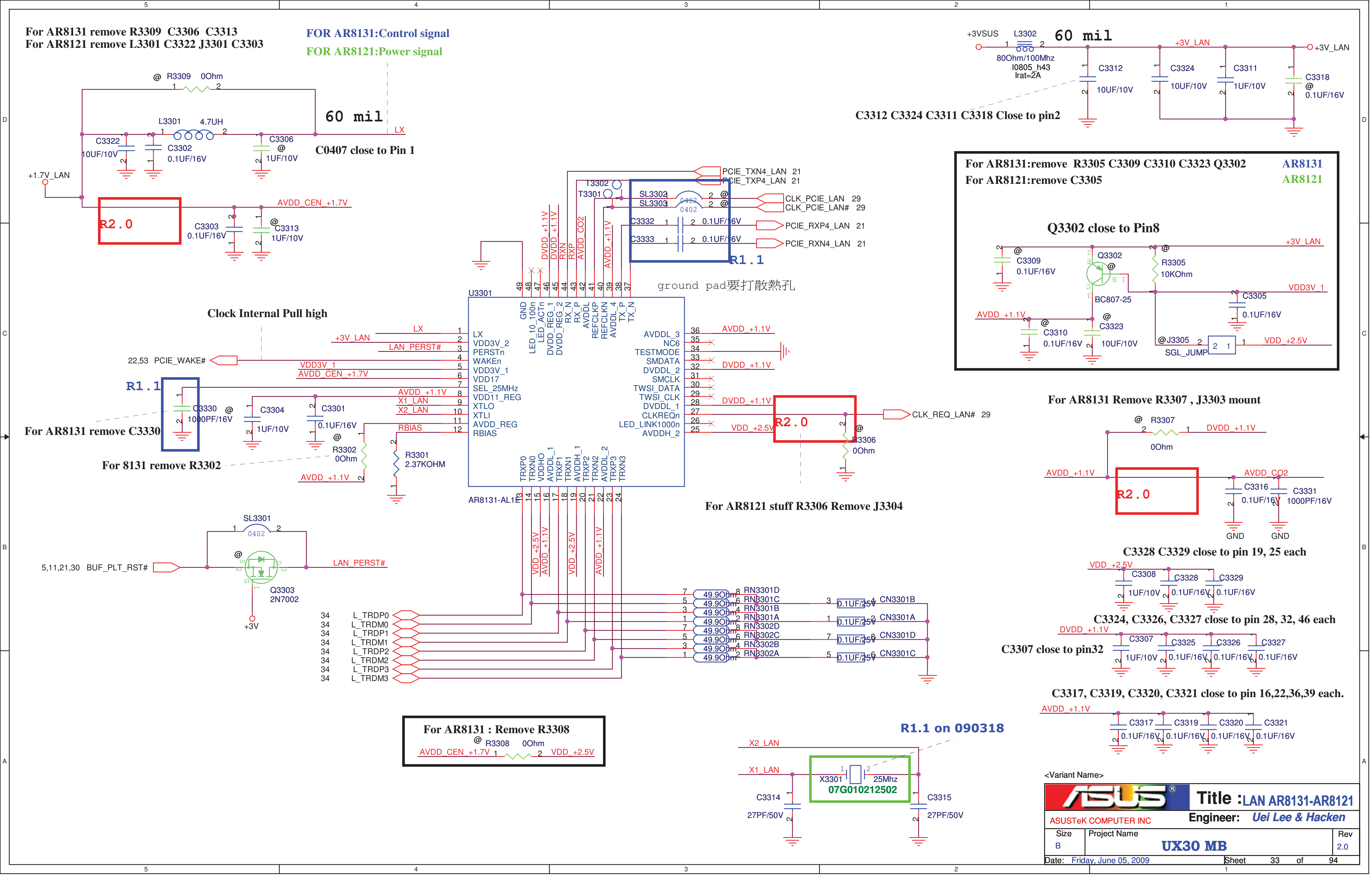


ASMedia ASM1442T
REMOVE:
R3201, R3214
MOUNT:
R3204,R3221

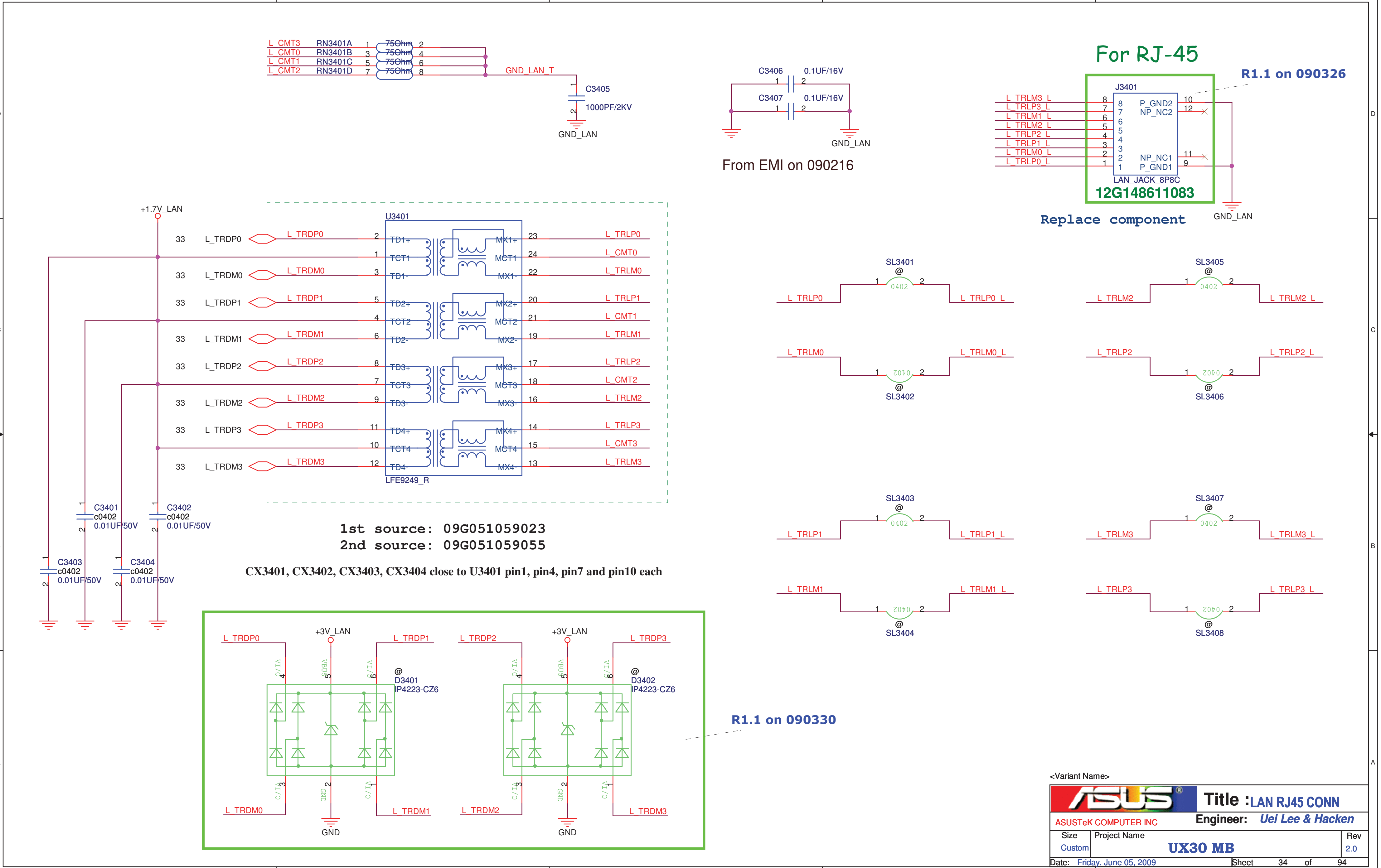
Parade PS8101T P/N:02G123000400
REMOVE:
R3204, R3221
MOUNT:
R3201, R3214
綠色外框的零件是上PS8101T要補上的零件
/ASM ASM1442T才要上的零件.上PS8101T時請移除

<Variant Name>

ASUSTeK COMPUTER INC	Title : UMA LEVEL SHIFTERS		
	Engineer: Uei Lee & Hacken		
Size C	Project Name UX30 MB		Rev 2.0
Date: Wednesday, June 10, 2009	Sheet 32 of 94		



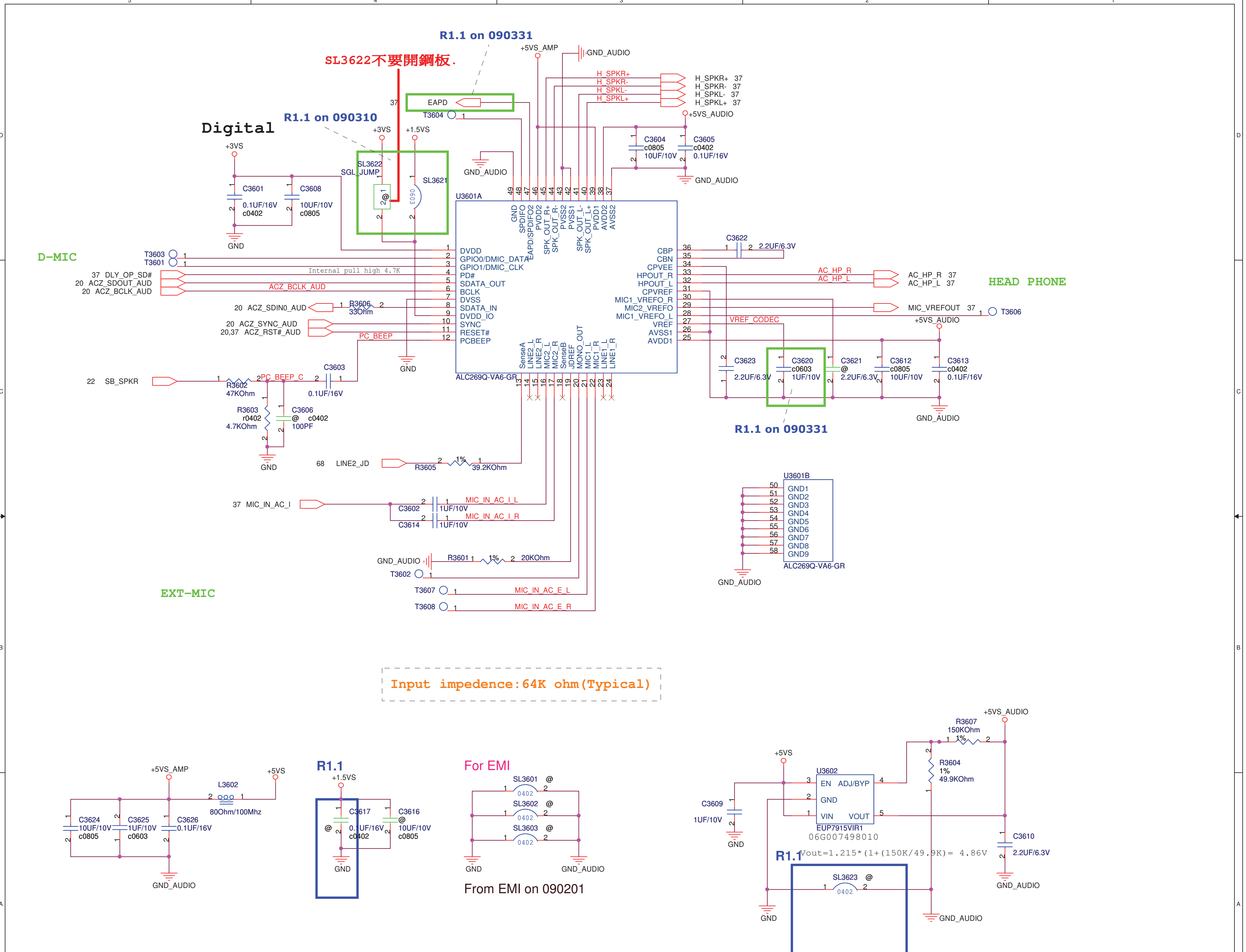
http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer:	Uei Lee & Hacken
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 06, 2008	Sheet 35 of 94	



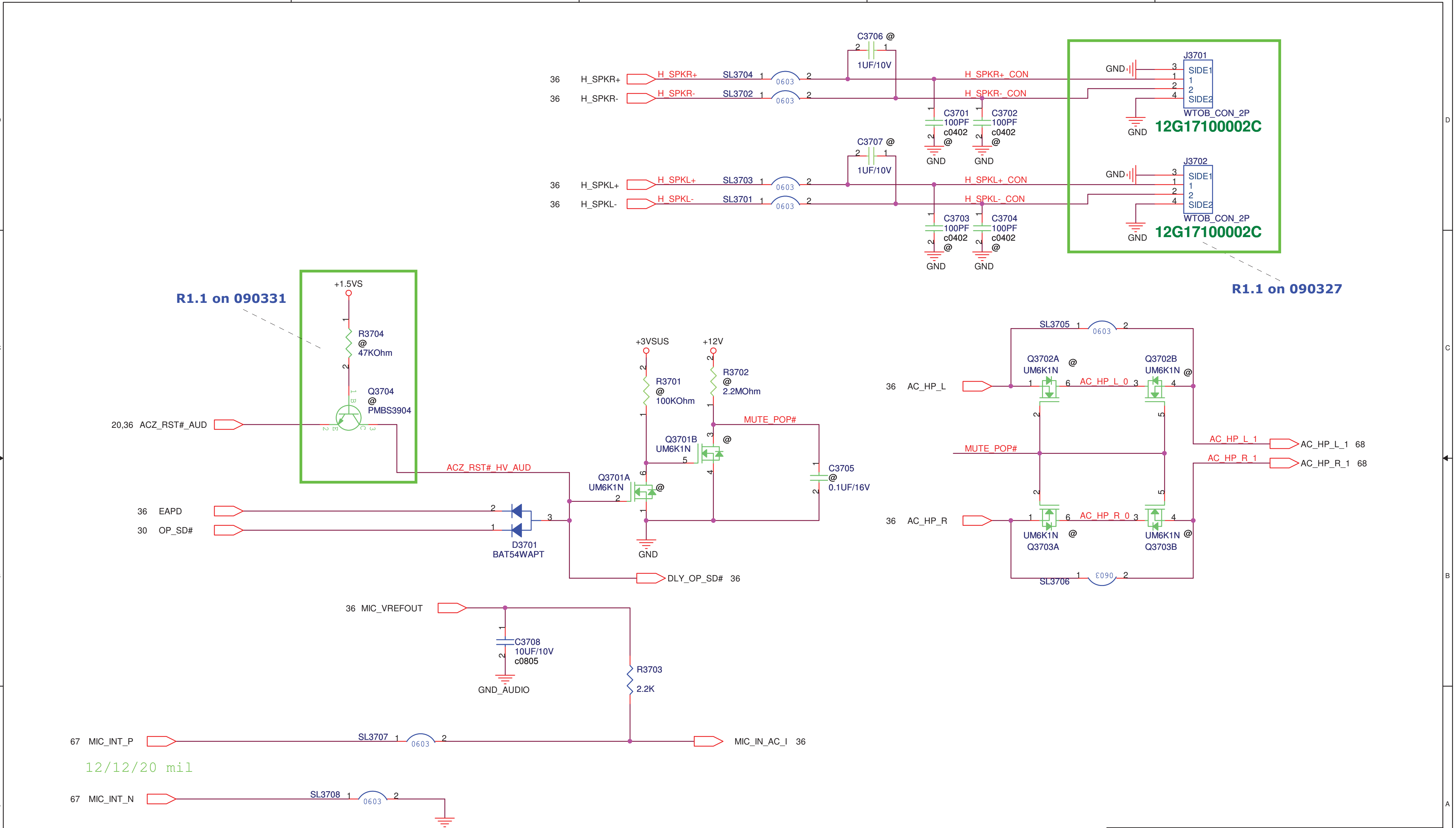
Title : CODEC

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 36 of 94



ASUSTeK COMPUTER INC. NB1	Title : PHONE JACK
	Engineer:
Size: B	Project Name: UX30 MB	Rev: 1.4
Date: Friday, June 05, 2009	Sheet 37 of 94

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

Title :*

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size	Project Name	Rev
A	UX30 MB	2.0

Date: Friday, June 06, 2008 Sheet 38 of 94

5 4 3 2 1

D C B A

<Variant Name>

Title :*

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size	Project Name	Rev
A	**UX30 MB**	2.0

Date: Friday, June 06, 2008 Sheet 39 of 94

5 4 3 2 1

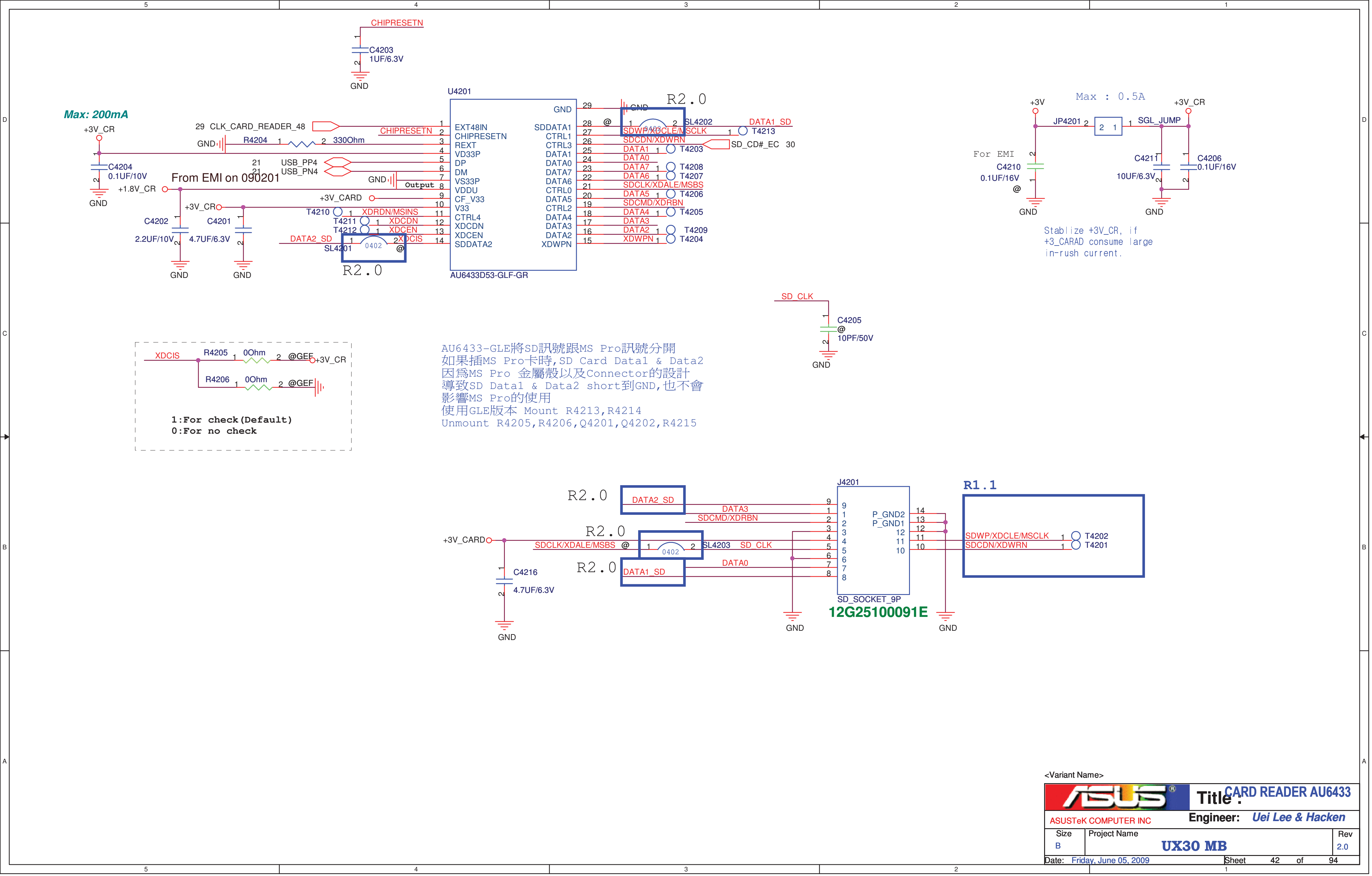
D C B A

<Variant Name>

ASUS	Title :*	
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 2.0
Date: Friday, June 06, 2008	Sheet 40 of 94	

<Variant Name>

ASUS	Title :*		
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 05, 2009	Sheet 41 of 94		

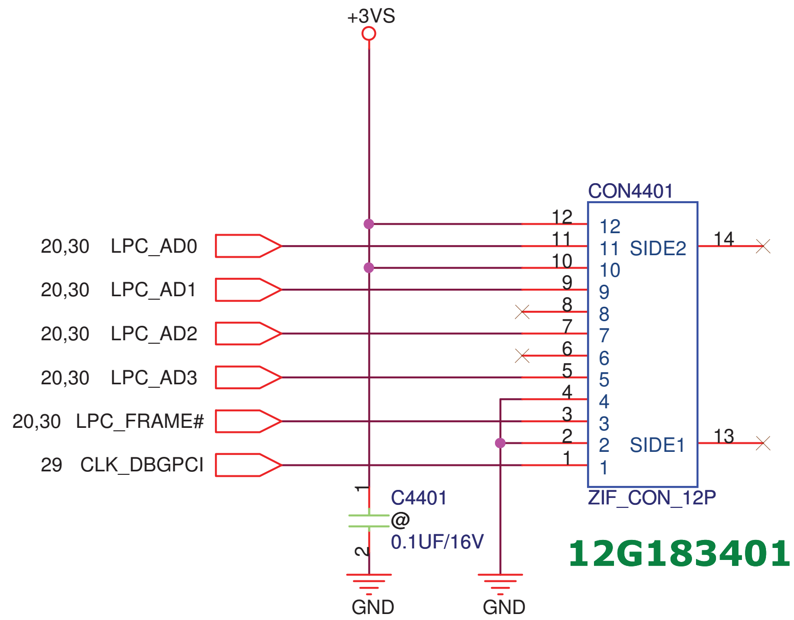


http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 43 of 94	

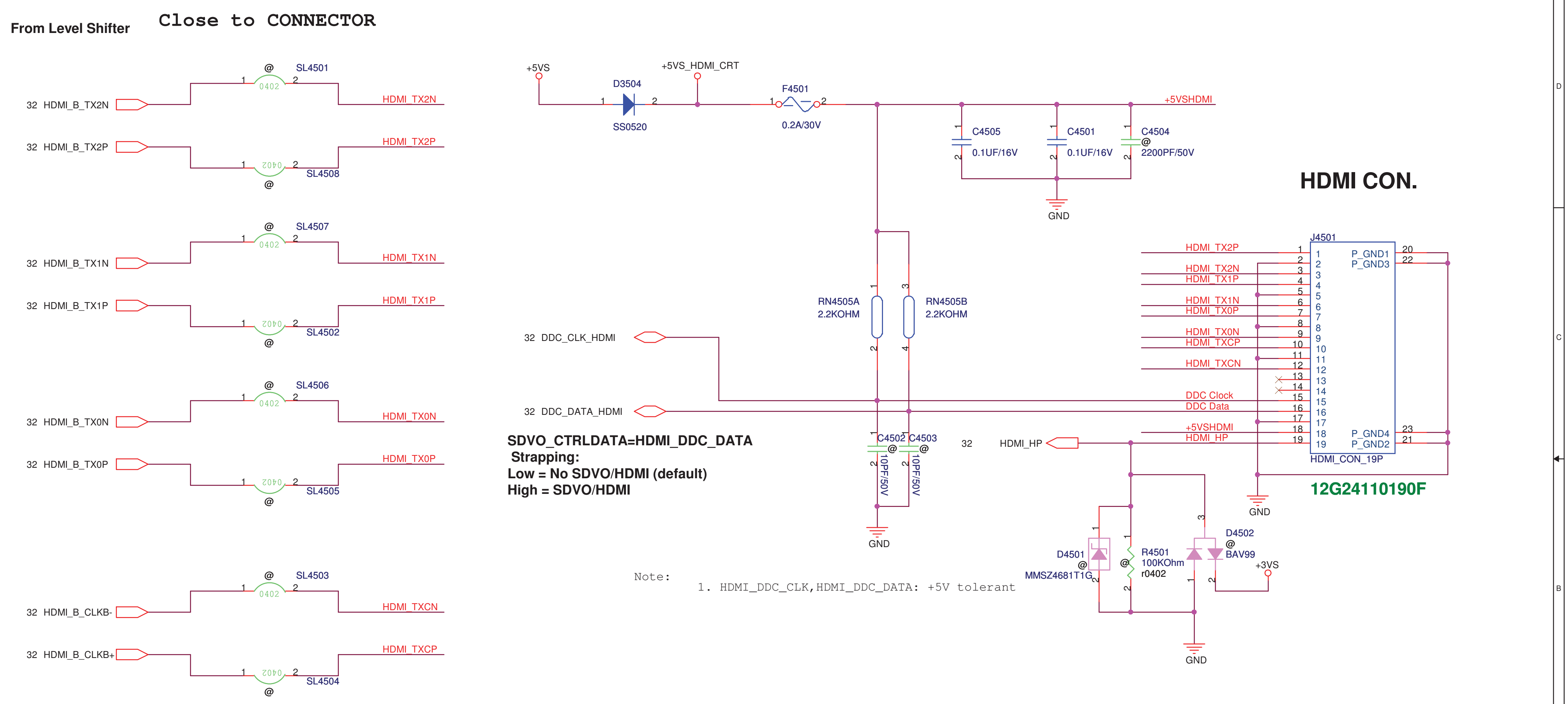
LPC DEBUG PORT



12G18340120S

<Variant Name>

ASUSTeK COMPUTER INC	Title : BUG DEBUG PORT	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 06, 2009	Sheet 44 of 94	



<Variant Name>

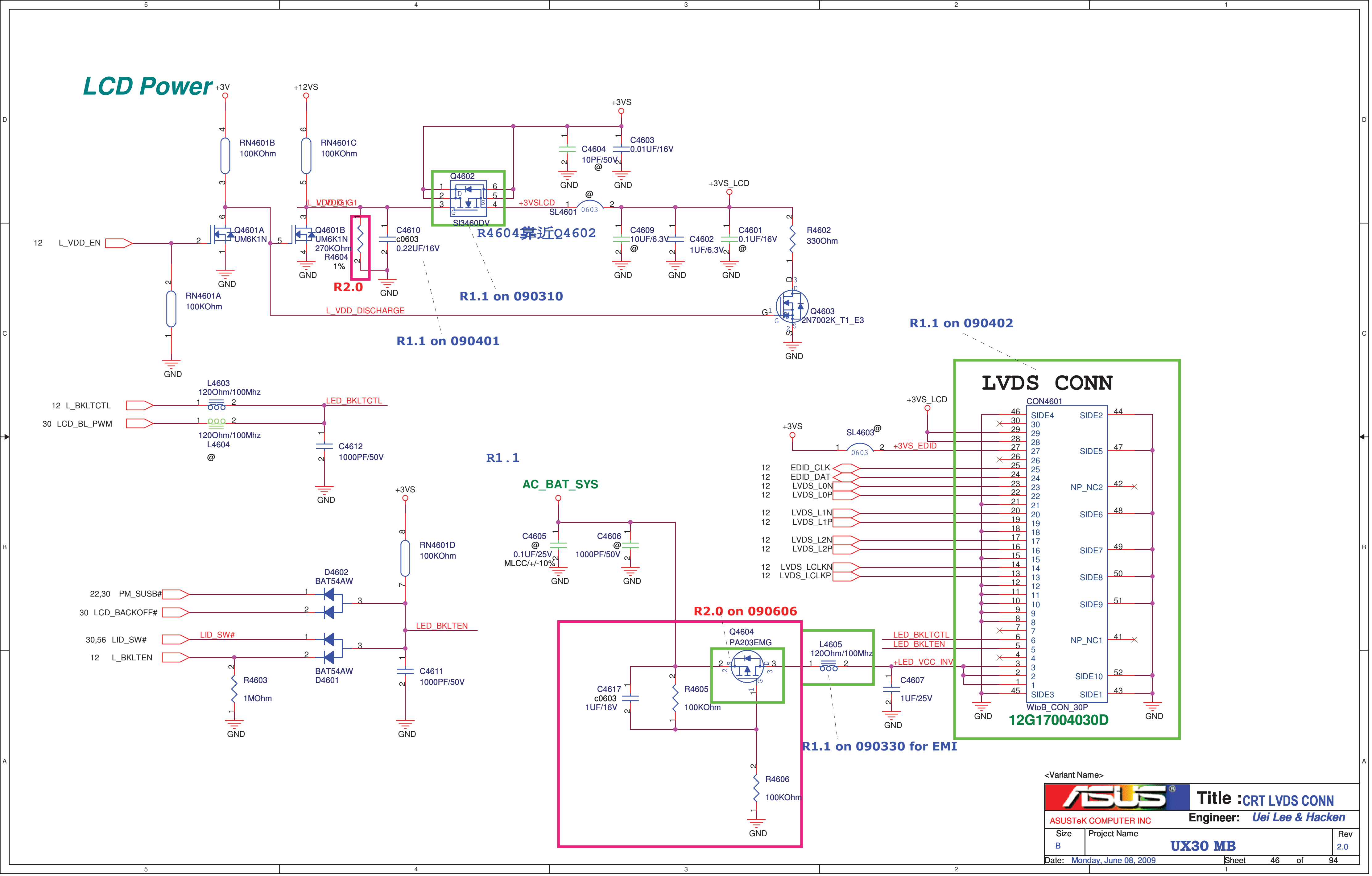
ASUSTeK COMPUTER INC

Title : HDMI CONN

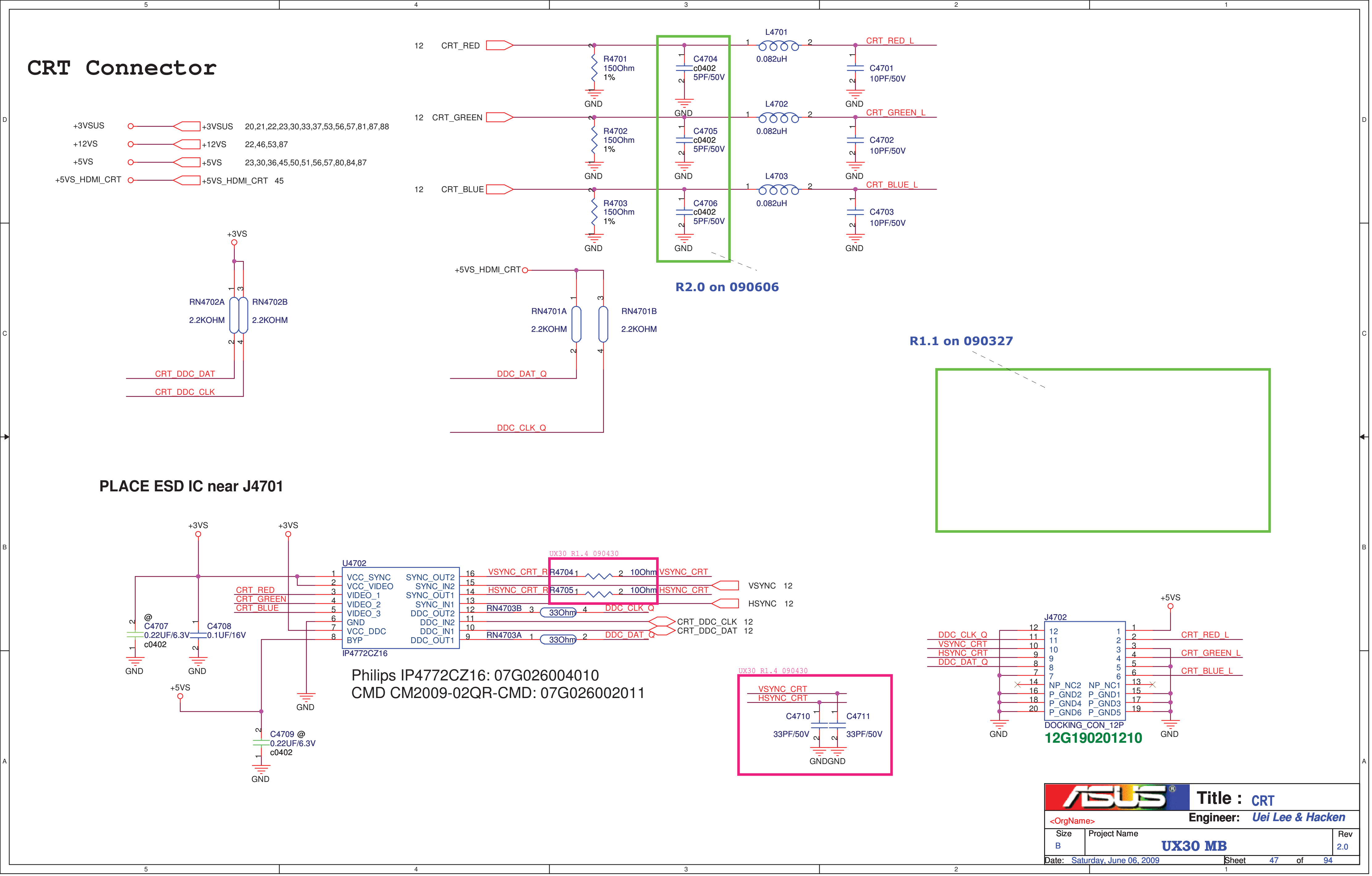
Engineer: Uei Lee & Hacken

Size	Project Name	Rev
B	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 45 of 94



http://laptop-motherboard-schematic.blogspot.com/


CRT Connector
+3VSUS
+3VSUS 20,21,22,23,30,33,37,53,56,57,81,87,88
+12VS
+12VS 22,46,53,87
+5VS
+5VS 23,30,36,45,50,51,56,57,80,84,87
+5VS_HDMI_CRT
+5VS_HDMI_CRT 45
12 CRT_RED
12 CRT_GREEN
12 CRT_BLUE
R4701 150Ohm 1%
R4702 150Ohm 1%
R4703 150Ohm 1%
C4704 c0402 5PF/50V
C4705 c0402 5PF/50V
C4706 c0402 5PF/50V
L4701 0.082uH
L4702 0.082uH
L4703 0.082uH
C4701 10PF/50V
C4702 10PF/50V
C4703 10PF/50V
CRT_RED_L
CRT_GREEN_L
CRT_BLUE_L
GND
R2.0 on 090606
R1.1 on 090327
+3VS
RN4702A 2.2KOHM
RN4702B 2.2KOHM
CRT_DDC_DAT
CRT_DDC_CLK
+5VS_HDMI_CRT
RN4701A 2.2KOHM
RN4701B 2.2KOHM
DDC_DAT_Q
DDC_CLK_Q
PLACE ESD IC near J4701
+3VS
+3VS
U4702
VCC_SYNC
VCC_VIDEO
VIDEO_1
VIDEO_2
VIDEO_3
GND
VCC_DDC
BYP
SYNC_OUT2
SYNC_IN2
SYNC_OUT1
SYNC_IN1
DDC_OUT2
DDC_IN2
DDC_IN1
DDC_OUT1
IP4772CZ16
CRT_RED
CRT_GREEN
CRT_BLUE
@ C4707 0.22UF/6.3V c0402
C4708 0.1UF/16V
+5VS
C4709 @ 0.22UF/6.3V c0402
UX30 R1.4 090430
VSYNC_CRT_R R4704 10Ohm VSYNC_CRT
HSYNC_CRT_R R4705 10Ohm HSYNC_CRT
VSYNC 12
HSYNC 12
RN4703B 33Ohm DDC_CLK_Q
RN4703A 33Ohm DDC_DAT_Q
CRT_DDC_CLK 12
CRT_DDC_DAT 12
Philips IP4772CZ16: 07G026004010
CMD CM2009-02QR-CMD: 07G026002011
UX30 R1.4 090430
VSYNC_CRT
HSYNC_CRT
C4710 33PF/50V
C4711 33PF/50V
GNDGND
+5VS
J4702
DDC_CLK_Q
VSYNC_CRT
HSYNC_CRT
DDC_DAT_Q
NP_NC2
P_GND2
P_GND4
P_GND6
NP_NC1
P_GND1
P_GND3
P_GND5
CRT_RED_L
CRT_GREEN_L
CRT_BLUE_L
DOCKING_CON_12P
12G190201210
Title : CRT
<OrgName>
Engineer: Uei Lee & Hacken
Size B
Project Name UX30 MB
Rev 2.0
Date: Saturday, June 06, 2009
Sheet 47 of 94

<Variant Name>

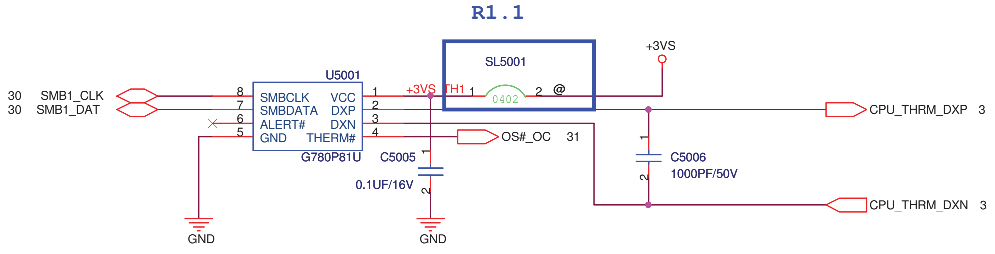
ASUSTeK COMPUTER INC	Title :*		
	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 05, 2009		Sheet 48 of 94	

<Variant Name>

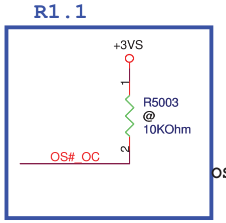
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 49 of 94	

Thermal Seneor

CPU

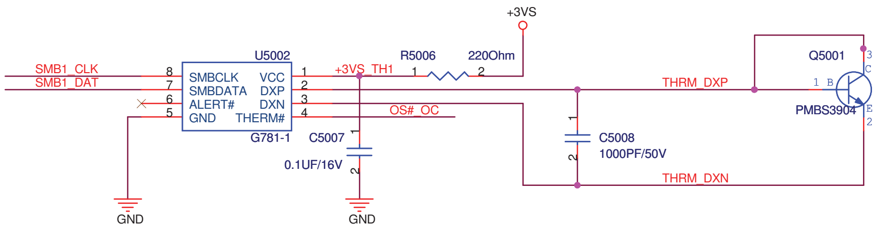


SMBus Address: G780 98H



OS#_OC PULL HIGH AT Page 31.

CHASSIS



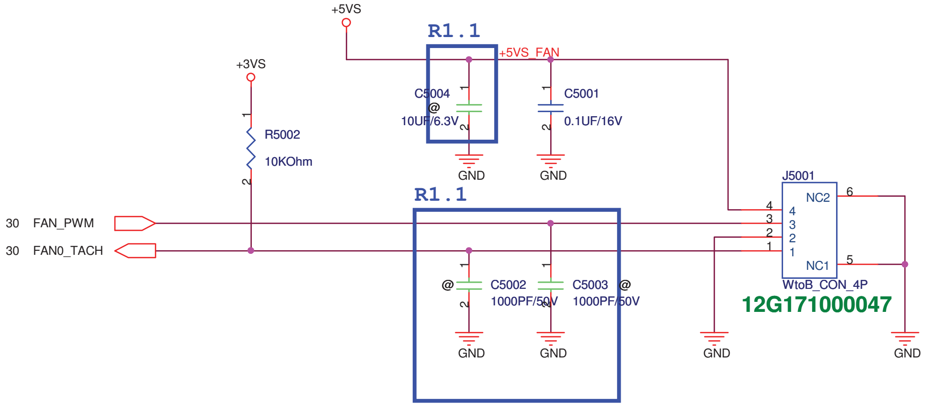
SMBus Address: G780 9AH

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

------------------OTHER SIGNALS
10 mils
===============GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
--------------------OTHER SIGNALS

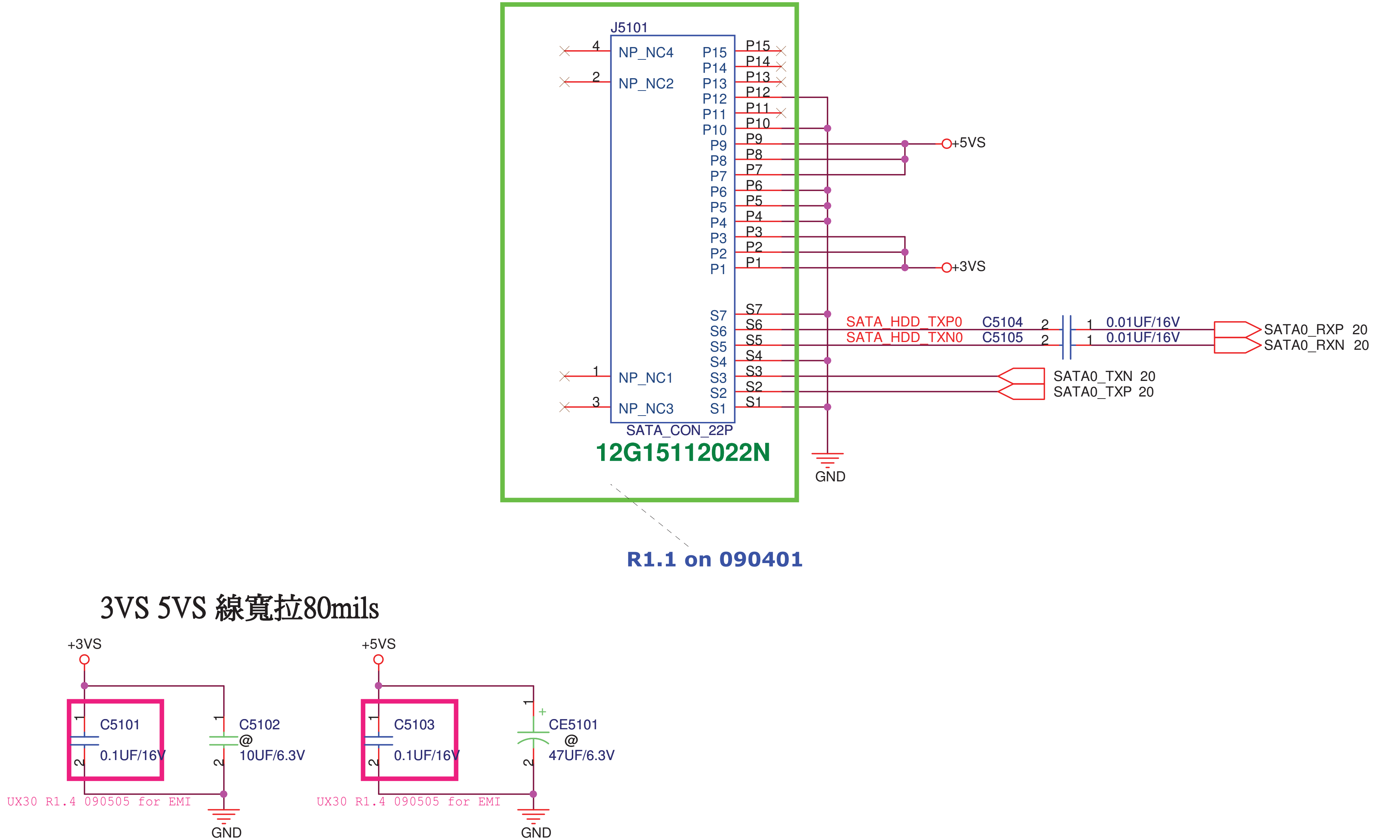
Avoid FSB,Power

FAN CONN



<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN THERMAL SENSOR FAN CONN		
	Engineer: Uei Lee & Hacken		
Size: Custom	Project Name: UX30 MB		Rev: 2.0
Date: Friday, June 05, 2009		Sheet 50 of 94	



<Variant Name>

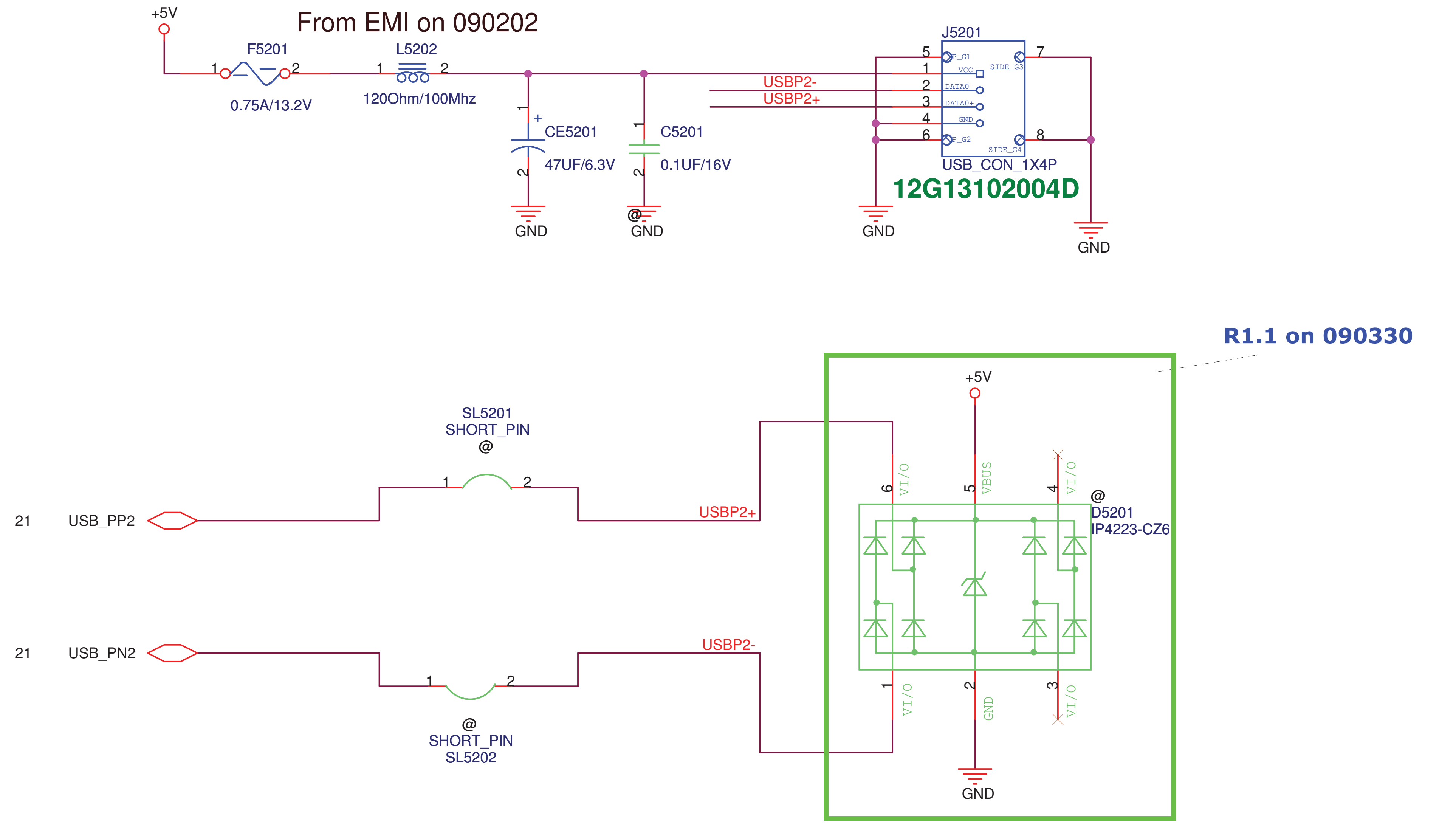
ASUSTeK COMPUTER INC

Title : XDD SATA HDD CONN

Engineer: *Uei Lee & Hacken*

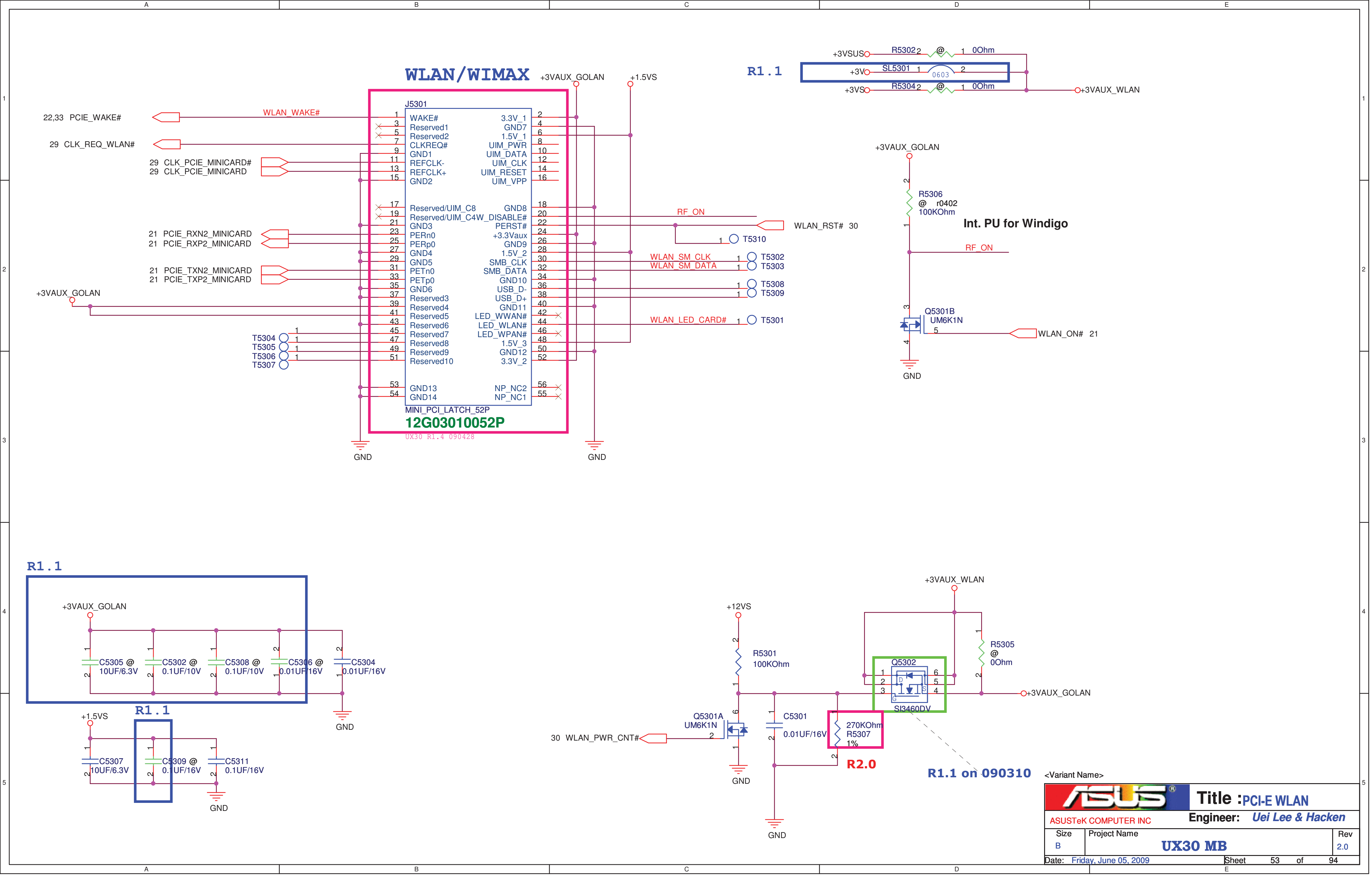
Size	Project Name	Rev
A	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 51 of 94



<Variant Name>

ASUS	Title : USB CONN	
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 52 of 94	

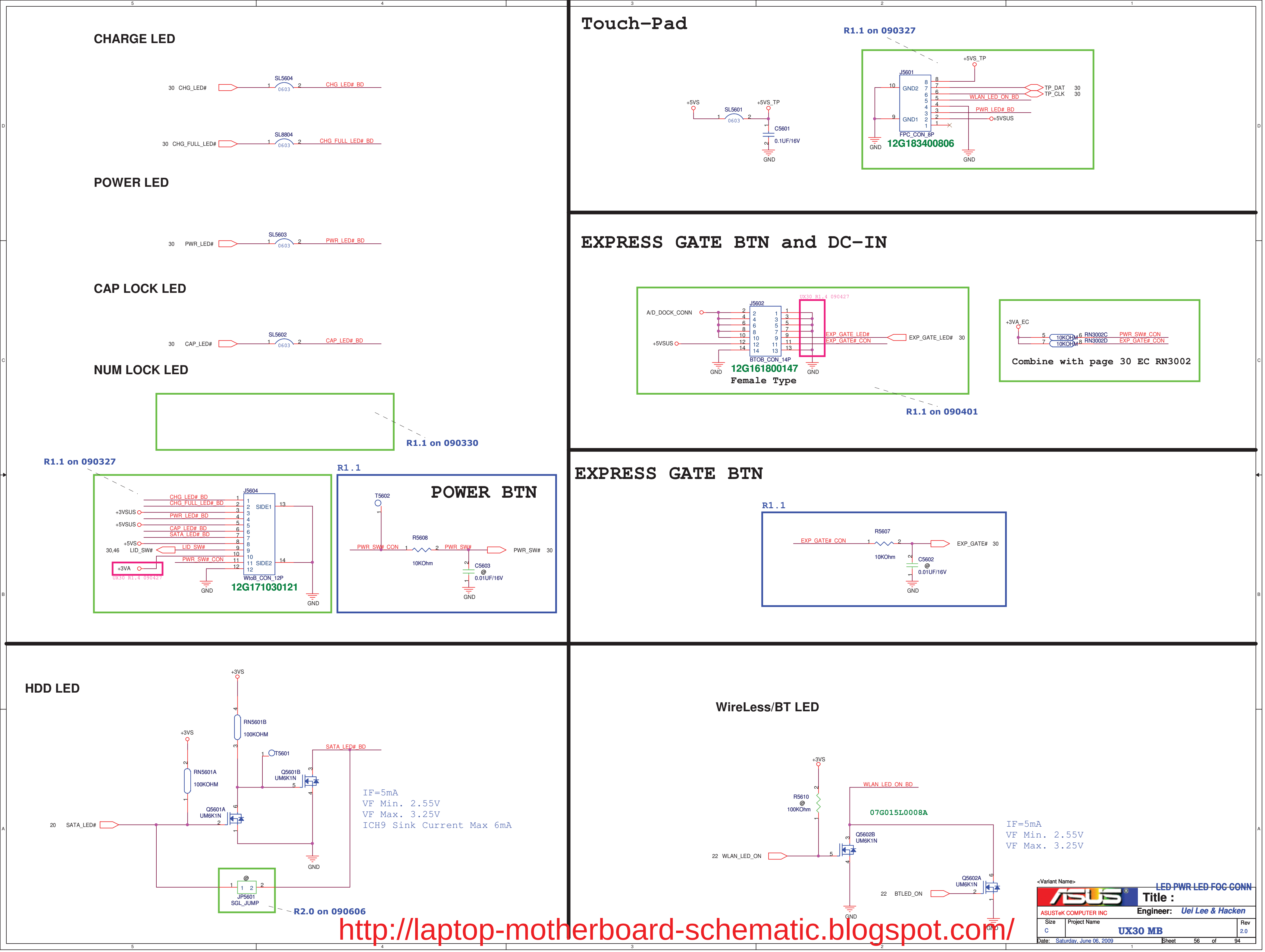

WLAN/WIMAX
J5301
MINI_PCI_LATCH_52P
12G03010052P
UX30 R1.4 090428
WAKE#
Reserved1
Reserved2
CLKREQ#
GND1
REFCLK-
REFCLK+
GND2
Reserved/UIM_C8
Reserved/UIM_C4W_DISABLE#
GND3
PERn0
PERp0
GND4
GND5
PETn0
PETp0
GND6
Reserved3
Reserved4
Reserved5
Reserved6
Reserved7
Reserved8
Reserved9
Reserved10
GND13
GND14
3.3V_1
GND7
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
GND8
W_DISABLE#
PERST#
+3.3Vaux
GND9
1.5V_2
SMB_CLK
SMB_DATA
GND10
USB_D-
USB_D+
GND11
LED_WWAN#
LED_WLAN#
LED_WPAN#
1.5V_3
GND12
3.3V_2
NP_NC2
NP_NC1
22,33 PCIE_WAKE#
WLAN_WAKE#
29 CLK_REQ_WLAN#
29 CLK_PCIE_MINICARD#
29 CLK_PCIE_MINICARD
21 PCIE_RXN2_MINICARD
21 PCIE_RXP2_MINICARD
21 PCIE_TXN2_MINICARD
21 PCIE_TXP2_MINICARD
+3VAUX_GOLAN
+1.5VS
T5304
T5305
T5306
T5307
RF_ON
WLAN_RST# 30
T5310
WLAN_SM_CLK
WLAN_SM_DATA
T5302
T5303
T5308
T5309
WLAN_LED_CARD#
T5301
GND
R1.1
+3VSUS
R5302
0Ohm
+3V
SL5301
0603
+3VS
R5304
0Ohm
+3VAUX_WLAN
R5306
@ r0402
100KOhm
Int. PU for Windigo
Q5301B
UM6K1N
WLAN_ON# 21
C5305 @
10UF/6.3V
C5302 @
0.1UF/10V
C5308 @
0.1UF/10V
C5306 @
0.01UF/16V
C5304
0.01UF/16V
C5307
10UF/6.3V
C5309 @
0.1UF/16V
C5311
0.1UF/16V
+12VS
R5301
100KOhm
Q5301A
UM6K1N
30 WLAN_PWR_CNT#
C5301
0.01UF/16V
270KOhm
R5307
1%
R2.0
Q5302
SI3460DV
R5305
@
0Ohm
R1.1 on 090310
<Variant Name>
Title :PCI-E WLAN
ASUSTeK COMPUTER INC
Engineer: Uei Lee & Hacken
Size
B
Project Name
UX30 MB
Rev
2.0
Date: Friday, June 05, 2009
Sheet 53 of 94

<Variant Name>

ASUS	Title :*	
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 06, 2008	Sheet 54 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*		
	Engineer: Uei Lee & Hacken		
Size: A	Project Name: UX30 MB		Rev: 2.0
Date: Friday, June 06, 2008	Sheet 55 of 94		


CHARGE LED
30 CHG_LED#
SL5604
0603
CHG_LED#_BD
30 CHG_FULL_LED#
SL8804
CHG_FULL_LED#_BD
POWER LED
30 PWR_LED#
SL5603
PWR_LED#_BD
CAP LOCK LED
30 CAP_LED#
SL5602
CAP_LED#_BD
NUM LOCK LED
R1.1 on 090330
R1.1 on 090327
J5604
CHG_LED#_BD
CHG_FULL_LED#_BD
+3VSUS
PWR_LED#_BD
+5VSUS
CAP_LED#_BD
SATA_LED#_BD
+5VS
30,46 LID_SW#
LID_SW#
PWR_SW#_CON
+3VA
UX30 R1.4 090427
SIDE1
SIDE2
WtoB_CON_12P
12G171030121
GND
R1.1
POWER BTN
T5602
R5608
PWR_SW#_CON
PWR_SW#
10KOhm
C5603
0.01UF/16V
PWR_SW# 30
Touch-Pad
R1.1 on 090327
+5VS_TP
J5601
GND2
GND1
TP_DAT 30
TP_CLK 30
WLAN_LED_ON_BD
PWR_LED#_BD
+5VSUS
FPC_CON_8P
12G183400806
+5VS
SL5601
C5601
0.1UF/16V
EXPRESS GATE BTN and DC-IN
UX30 R1.4 090427
A/D_DOCK_CONN
J5602
+5VSUS
EXP_GATE_LED#
EXP_GATE#_CON
EXP_GATE_LED# 30
BTOB_CON_14P
12G161800147
Female Type
R1.1 on 090401
+3VA_EC
RN3002C
RN3002D
10KOHM
PWR_SW#_CON
EXP_GATE#_CON
Combine with page 30 EC RN3002
EXPRESS GATE BTN
R1.1
R5607
EXP_GATE#_CON
10KOhm
EXP_GATE# 30
C5602
0.01UF/16V
HDD LED
+3VS
RN5601B
100KOHM
RN5601A
100KOHM
T5601
SATA_LED#_BD
Q5601B
UM6K1N
Q5601A
UM6K1N
20 SATA_LED#
JP5601
SGL_JUMP
R2.0 on 090606
IF=5mA
VF Min. 2.55V
VF Max. 3.25V
ICH9 Sink Current Max 6mA
WireLess/BT LED
+3VS
R5610
100KOhm
WLAN_LED_ON_BD
07G015L0008A
Q5602B
UM6K1N
22 WLAN_LED_ON
Q5602A
UM6K1N
22 BTLED_ON
IF=5mA
VF Min. 2.55V
VF Max. 3.25V
<Variant Name>
ASUSTeK COMPUTER INC
Title : LED PWR LED FOC CONN
Engineer: Uei Lee & Hacken
Size C
Project Name UX30 MB
Rev 2.0
Date: Saturday, June 06, 2009
Sheet 56 of 94

Discharge Circuit

<Variant Name>
DSG DISCHARHE CIRCUIT

ASUSTeK COMPUTER INC	Title :	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 57 of 94	

<Variant Name>

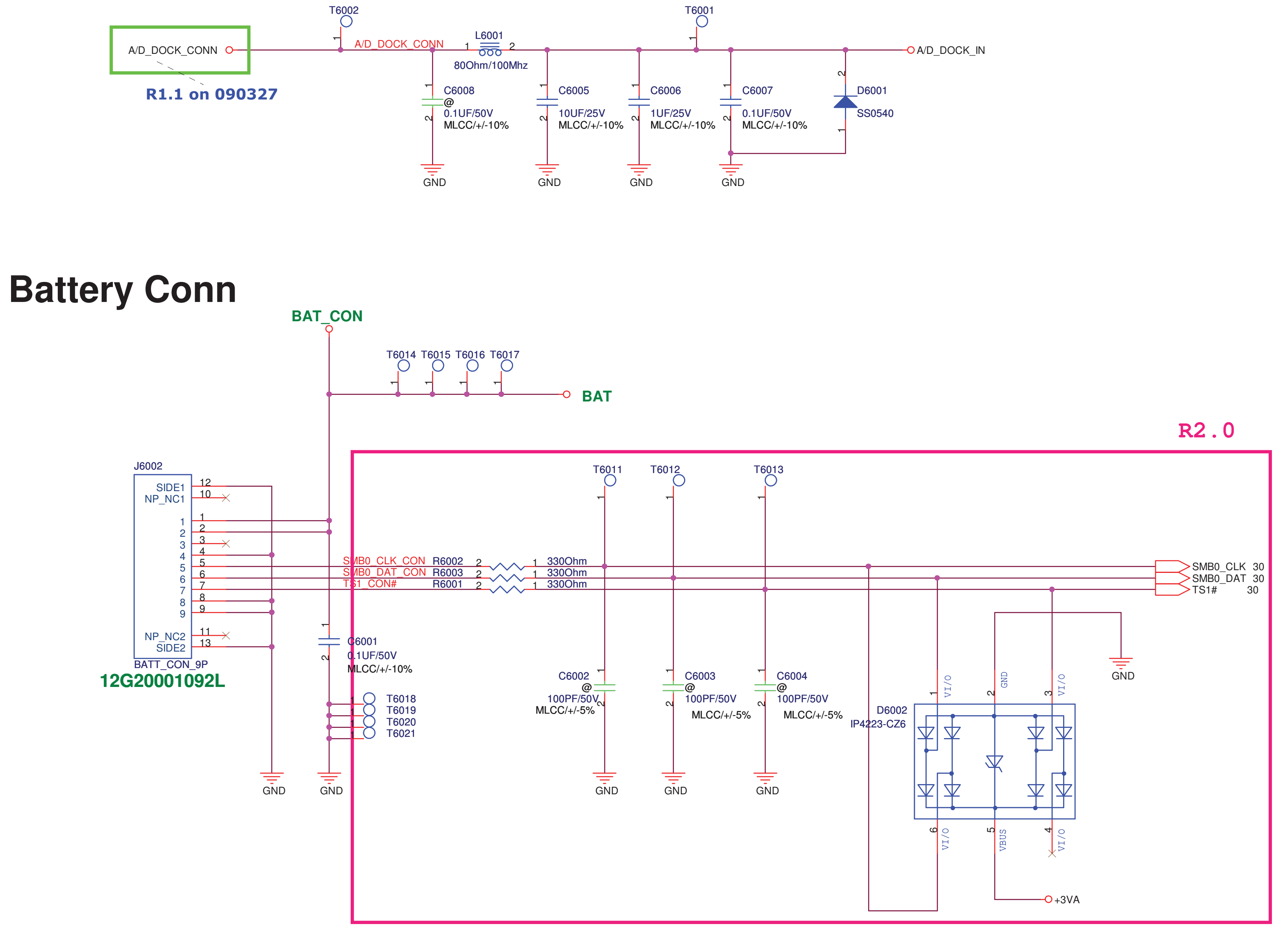
ASUSTeK COMPUTER INC	Title : *	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 06, 2008	Sheet 58 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*		
	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 06, 2008	Sheet 59	of 94	

DC-IN

Battery Conn



<Variant Name>

ASUSTeK COMPUTER INC

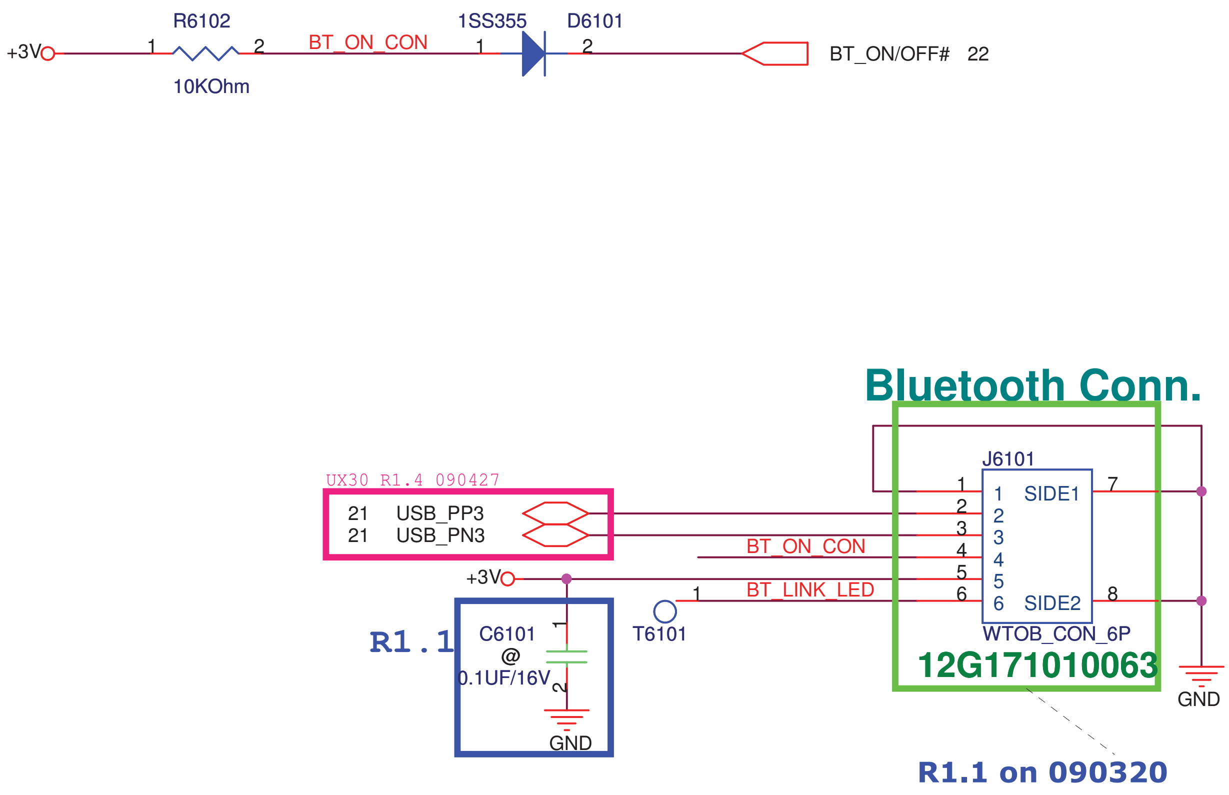
Title : DC DC&BATT CONN

Engineer: Uei Lee & Hacken

Size B | Project Name UX30 MB | Rev 2.0

Date: Friday, June 05, 2009 | Sheet 60 of 93

BT CON



<Variant Name>

ASUSTeK COMPUTER INC

Title : BT BLUETOOTH CONN

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
A	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 61 of 94

<Variant Name>

ASUSTeK COMPUTER INC	Title :*		
	Engineer: Uei Lee & Hacken		
Size: A	Project Name: UX30 MB		Rev: 2.0
Date: Friday, June 05, 2009	Sheet 62 of 94		

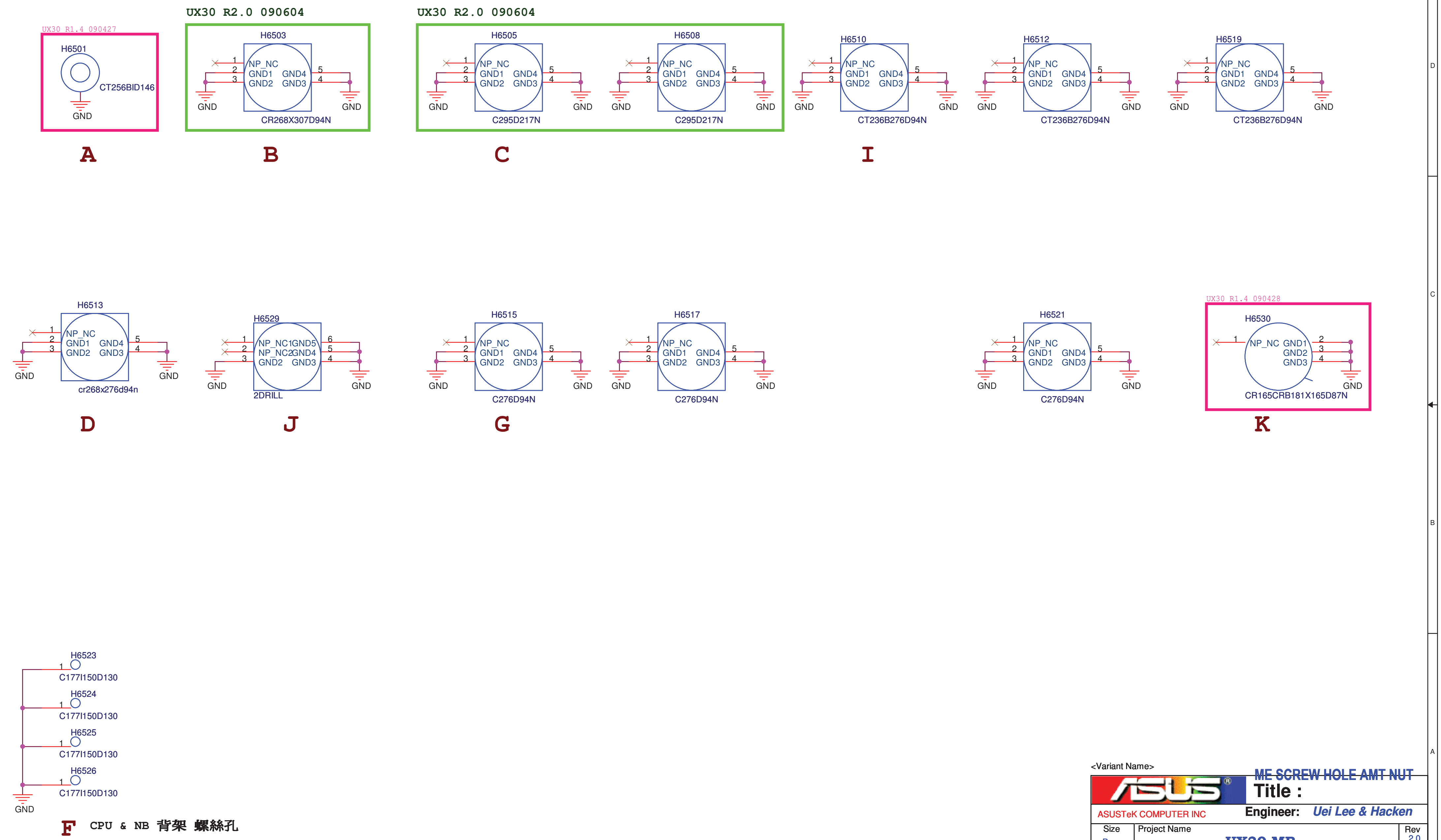
<Variant Name>

ASUS	Title :*	
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 06, 2008	Sheet 63 of 94	

<Variant Name>

ASUS	Title :*		
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 05, 2009	Sheet 64 of 94		

Screw Hole & SMT Nut



<Variant Name>

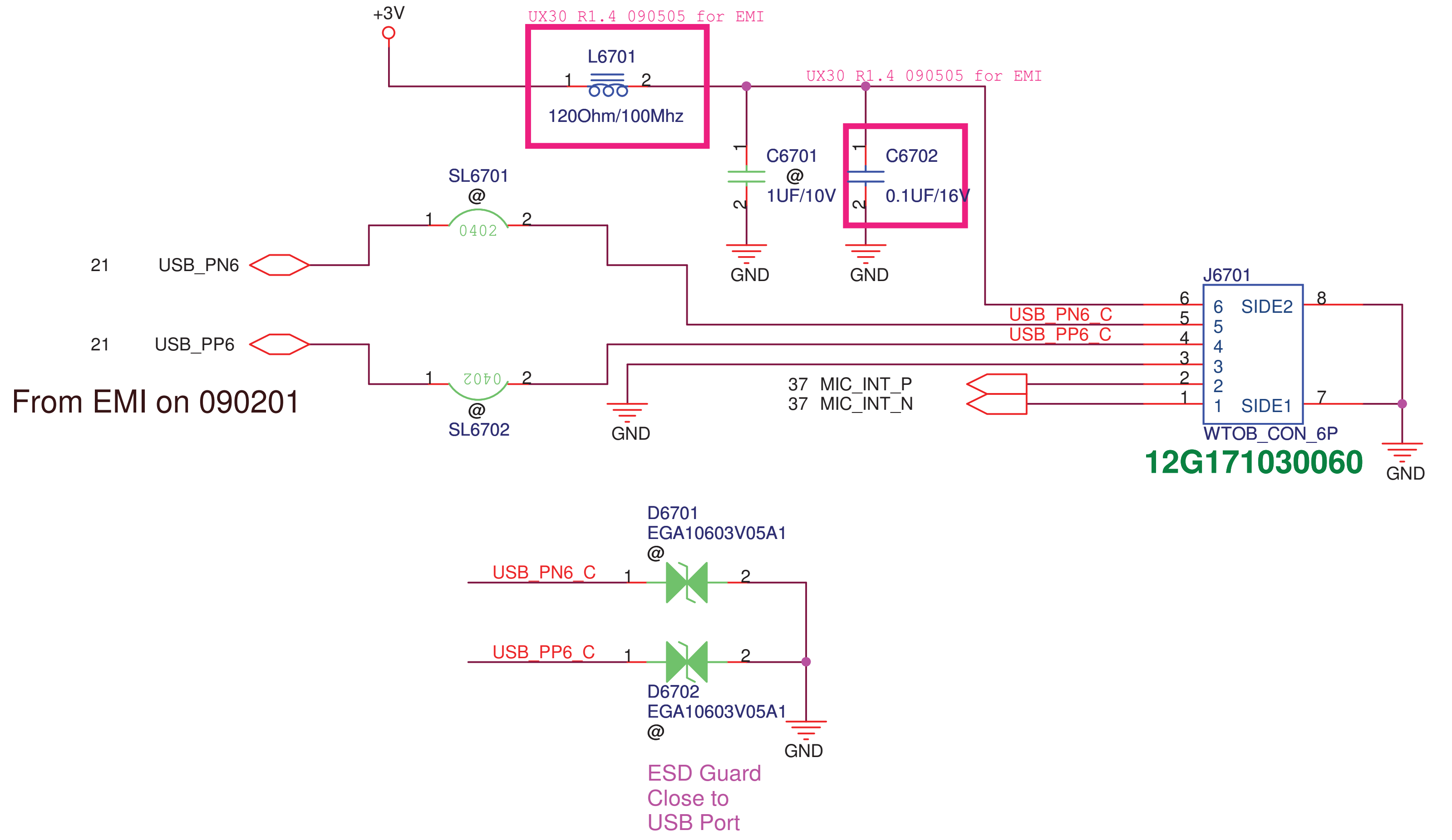
ASUSTeK COMPUTER INC	Title : ME SCREW HOLE AMT NUT	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 65 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*		
	Engineer: *Uei Lee & Hacken*		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 06, 2008	Sheet 66 of 94		

Camera Module

3V CAMERA MODULE



<Variant Name>

ASUS

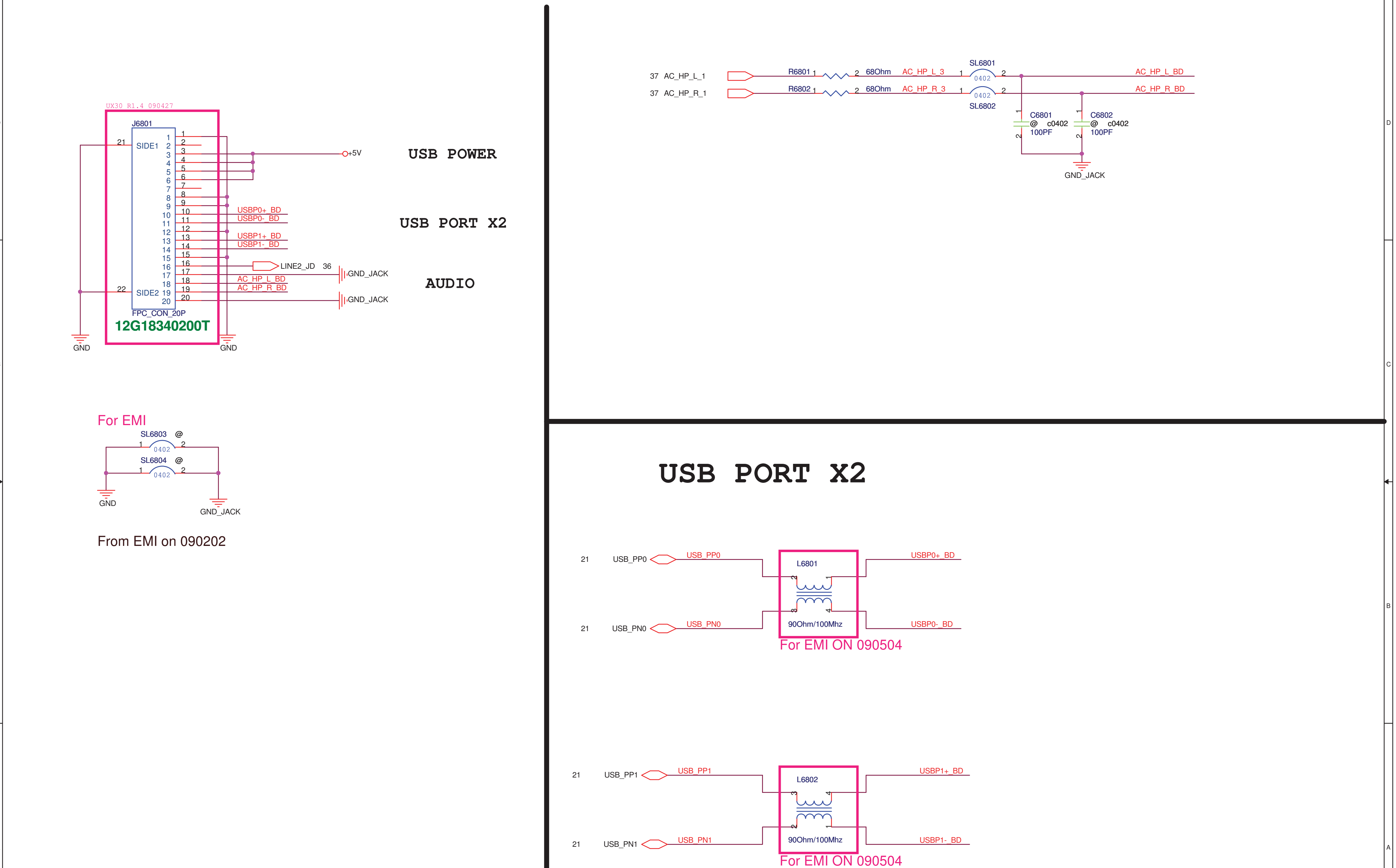
Title : CMOS CAMERA

ASUSTeK COMPUTER INC

Engineer: *Uei Lee & Hacken*

Size	Project Name	Rev
A	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 67 of 94



<Variant Name>

ASUS

Title : I/O BOARD CON

ASUSTeK COMPUTER INC

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 68 of 94

SYSTEM

Net	Net	Pages
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,57,82
+VCC_GMCH	+VCC_GMCH	14
+VGFX_CORE	+VGFX_CORE	14
+3VS	+3VS	3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,57,80,87,88
+VCORE	+VCORE	4,5,80
+1.5VS	+1.5VS	4,15,20,23,36,37,53,57,84
+5V	+5V	52,57,68,87
+5VS	+5VS	23,30,36,45,47,50,51,56,57,80,84,87
+3VA	+3VA	20,30,56,81,85
+VCC_RTC	+VCC_RTC	20,23
+3V	+3V	21,33,42,46,53,57,61,67,87
+3VSUS	+3VSUS	20,21,22,23,30,33,37,53,56,57,81,87,88
+5VSUS	+5VSUS	23,56,81,82,83,85,87
+3VPLL	+3VPLL	30
+3VACC	+3VACC	30
+3VA_EC	+3VA_EC	30,31,56
+5VS_AMP	+5VS_AMP	36
+12V	+12V	37,87
+12VS	+12VS	22,46,53,87
AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,85
BAT	BAT	60,85
+5VA	+5VA	81
A/D_DOCK_IN	A/D_DOCK_IN	60,85
BAT_CON	BAT_CON	60,85

<Variant Name>

ASUSTeK COMPUTER INC

Title : POWER SOURCE

Engineer: Uei Lee & Hacken

Size: A | Project Name: UX30 MB | Rev: 2.0

Date: Friday, June 05, 2009 | Sheet 69 of 94

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 70 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: *Uei Lee & Hacken*	
Size A	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 71 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 06, 2009	Sheet 72 of 94	

<Variant Name>

ASUSTeK COMPUTER INC

Title :*

Engineer: *Uei Lee & Hacken*

Size	Project Name	Rev
A	UX30 MB	2.0

Date: Friday, June 06, 2008 | Sheet 73 of 94

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 74 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 75 of 94	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*		
	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 06, 2008	Sheet 76	of 94	

<Variant Name>

ASUS	Title : *		
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken		
Size A	Project Name UX30 MB		Rev 2.0
Date: Friday, June 06, 2008	Sheet 77 of 94		

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 2.0
Date: Friday, June 06, 2008	Sheet 78 of 94	

5 4 3 2 1

D C B A

<Variant Name>

Title :*

ASUSTeK COMPUTER INC

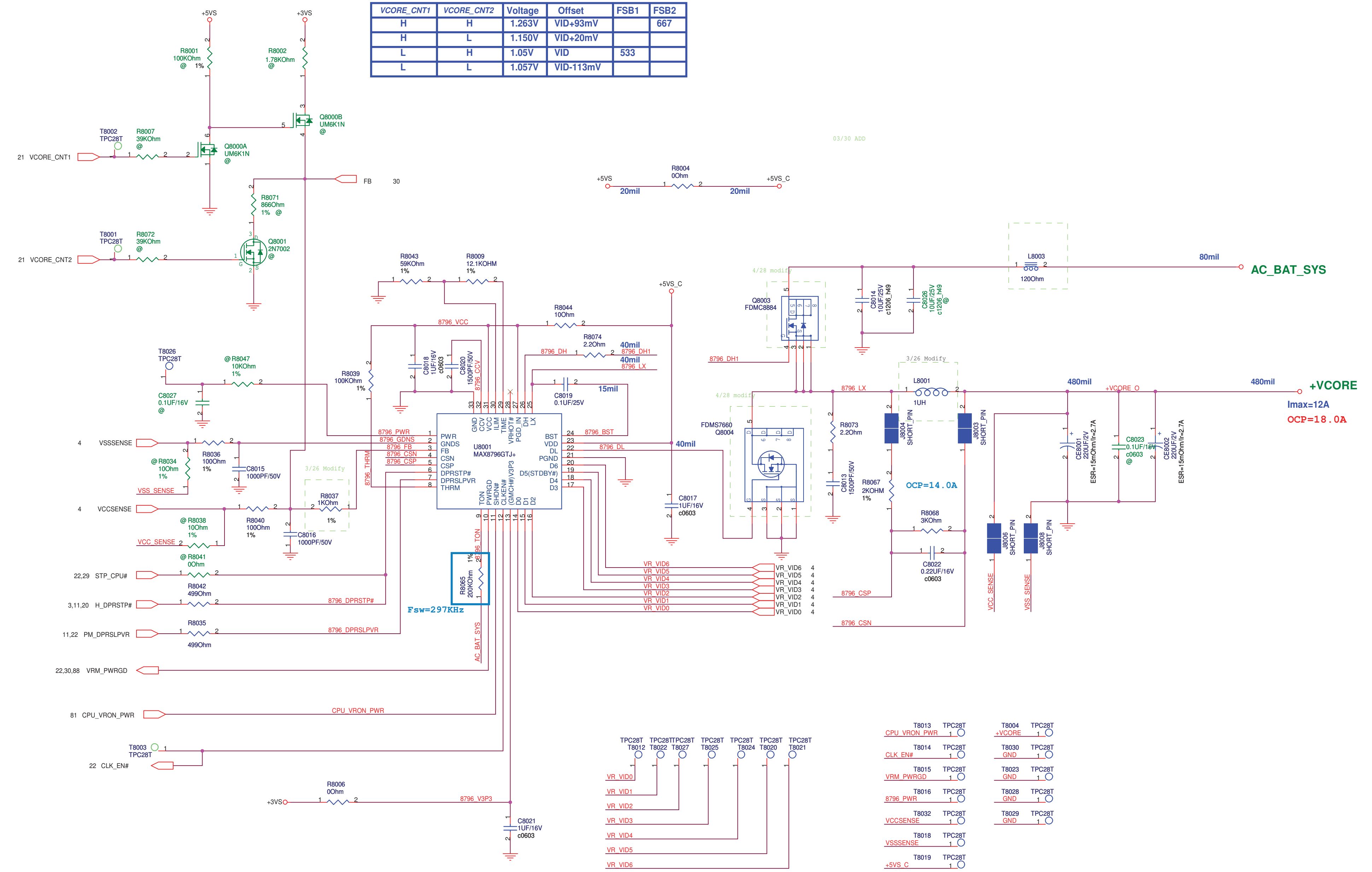
Engineer: *Uei Lee & Hacken*

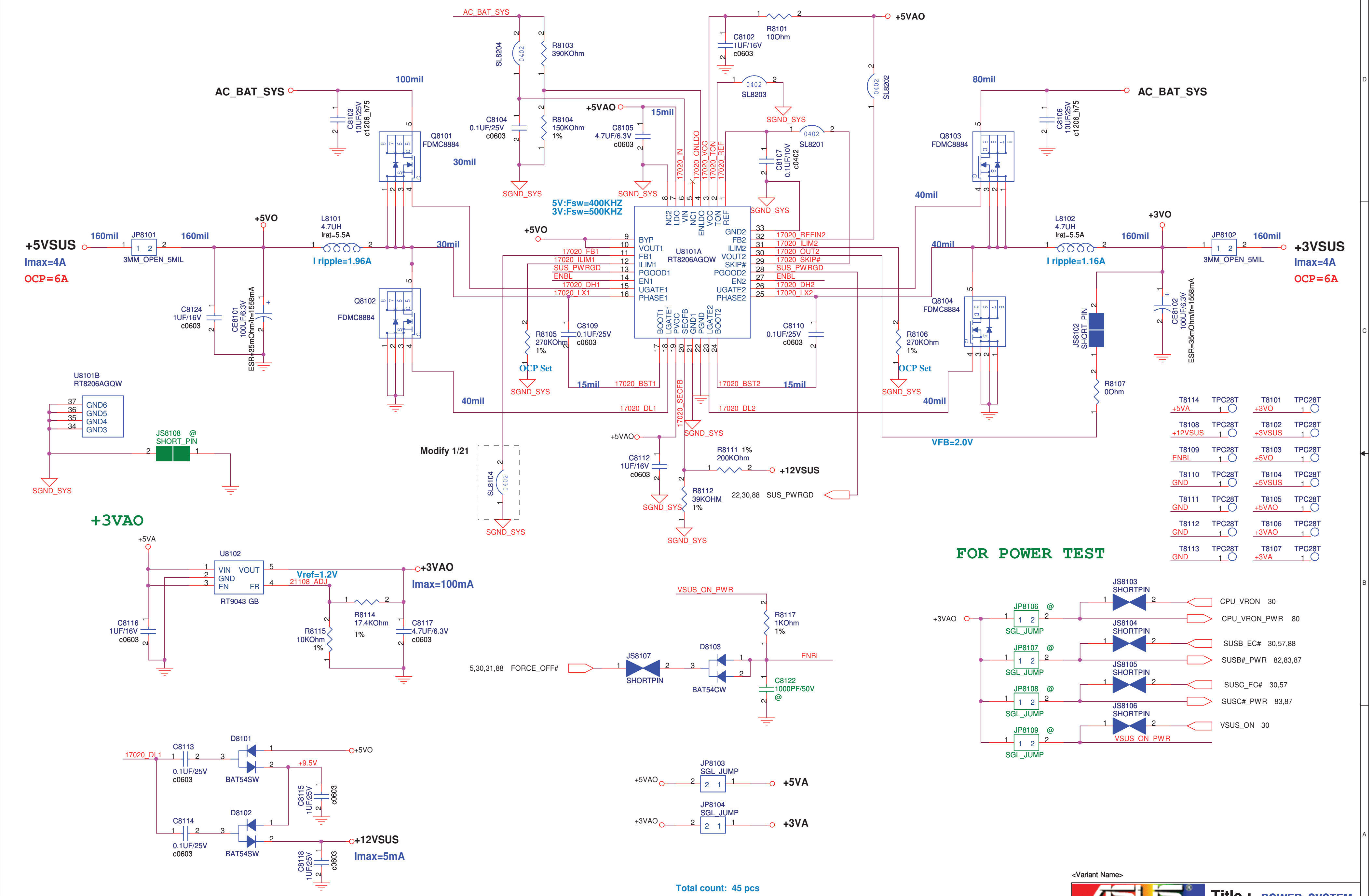
Size	Project Name	Rev
A	UX30 MB	2.0

Date: Friday, June 06, 2008 Sheet 79 of 94

CPU
VID=1.05V

VCORE_CNT1	VCORE_CNT2	Voltage	Offset	FSB1	FSB2
H	H	1.263V	VID+93mV		667
H	L	1.150V	VID+20mV		
L	H	1.05V	VID	533	
L	L	1.057V	VID-113mV		





<Variant Name>

ASUSTeK COMPUTER INC. NB

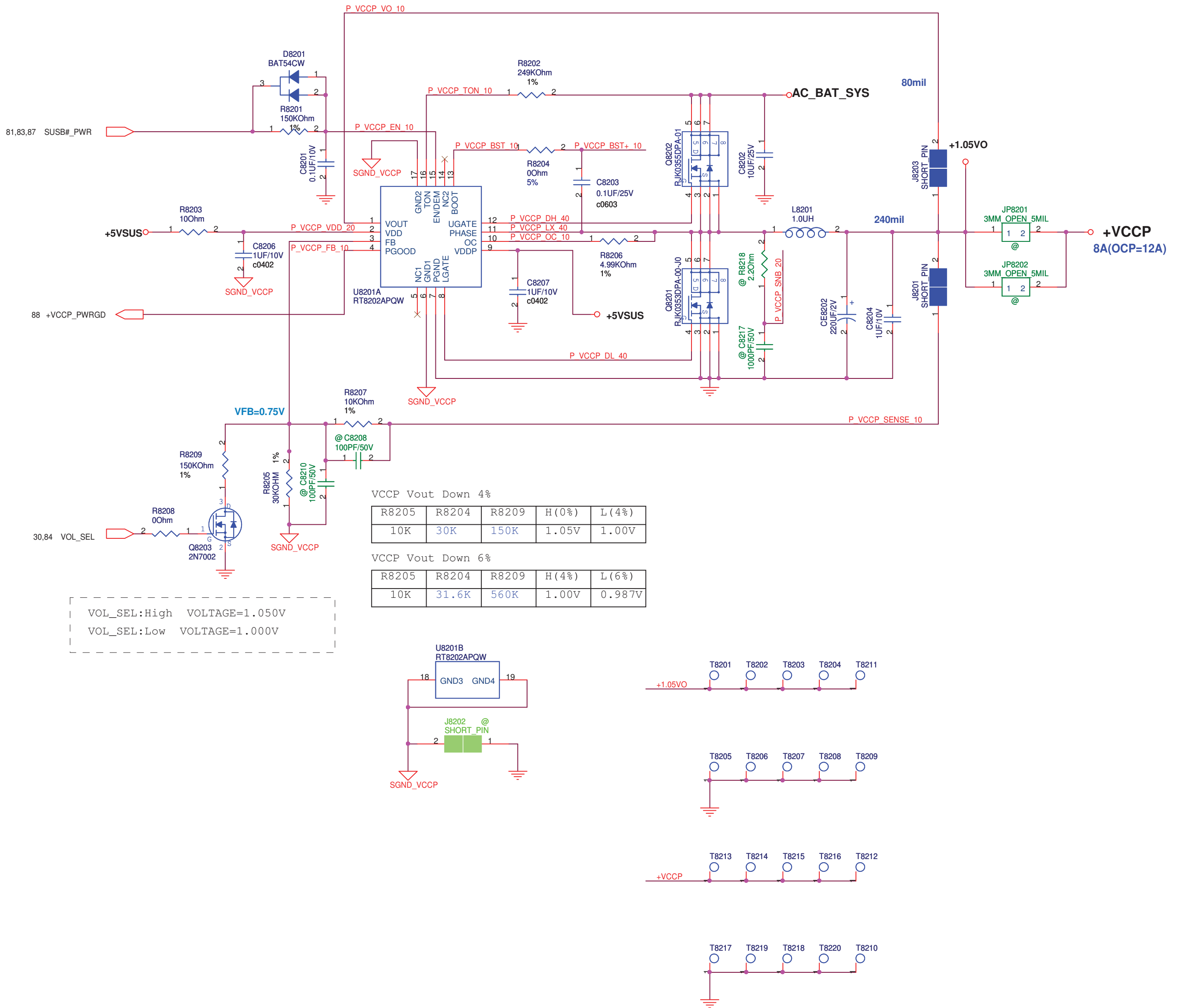
Title : POWER_SYSTEM

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UX30 MB	2.0

Date: Friday, June 05, 2009 Sheet 81 of 93

+VCCP POWER SUPPLY



VCCP Vout Down 4%

R8205	R8204	R8209	H(0%)	L(4%)
10K	30K	150K	1.05V	1.00V

VCCP Vout Down 6%

R8205	R8204	R8209	H(4%)	L(6%)
10K	31.6K	560K	1.00V	0.987V

VOL_SEL:High VOLTAGE=1.050V
VOL_SEL:Low VOLTAGE=1.000V

<Variant Name>

ASUS

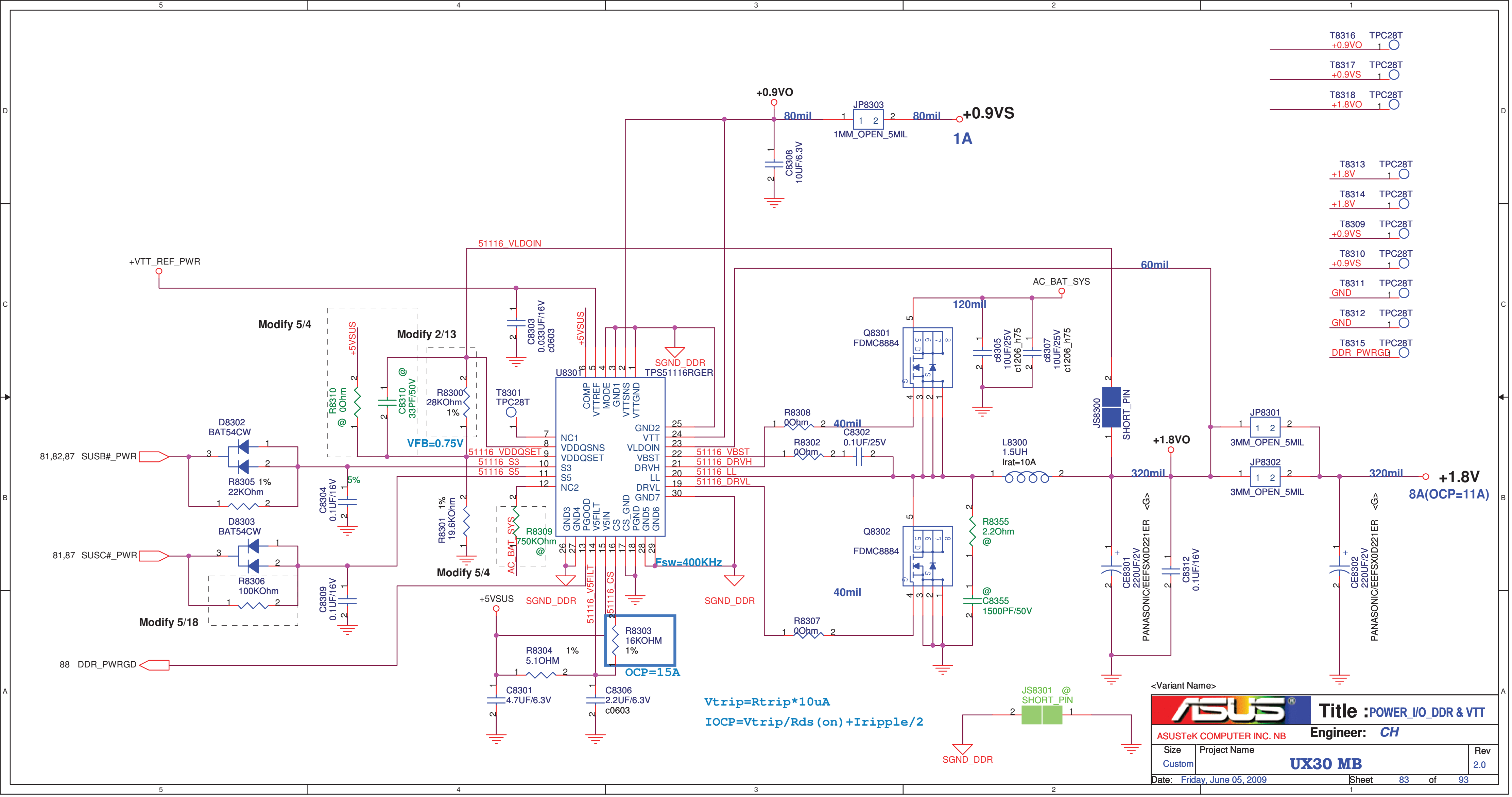
Title : POWER_I/O_+VCCP

ASUSTeK COMPUTER INC. NB

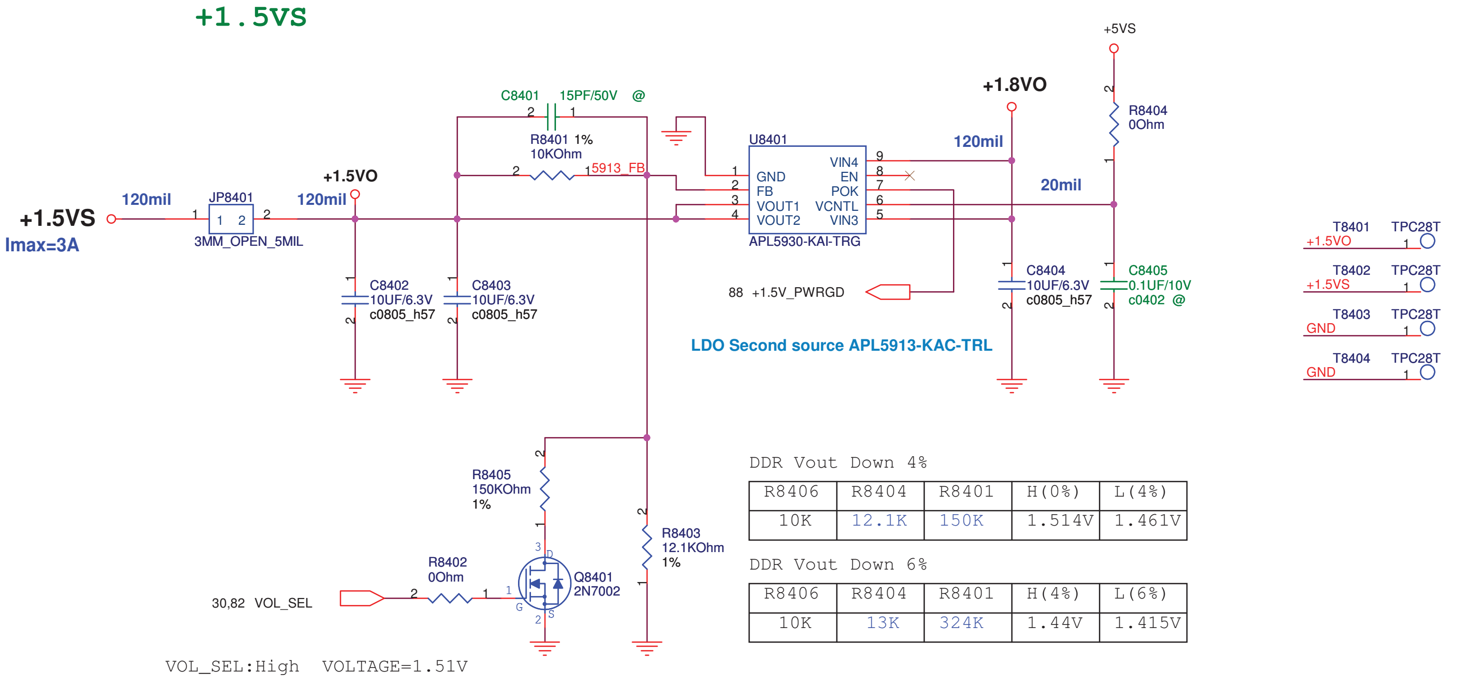
Engineer:

Size	Project Name	Rev
Custom		2.0

Date: Wednesday, June 10, 2009 Sheet 82 of 96



Total count: 29 pcs



VOL_SEL:High VOLTAGE=1.51V

VOL_SEL:Low VOLTAGE=1.46V

DDR Vout Down 4%

R8406	R8404	R8401	H(0%)	L(4%)
10K	12.1K	150K	1.514V	1.461V

DDR Vout Down 6%

R8406	R8404	R8401	H(4%)	L(6%)
10K	13K	324K	1.44V	1.415V

Total count: 7 pcs

<Variant Name>

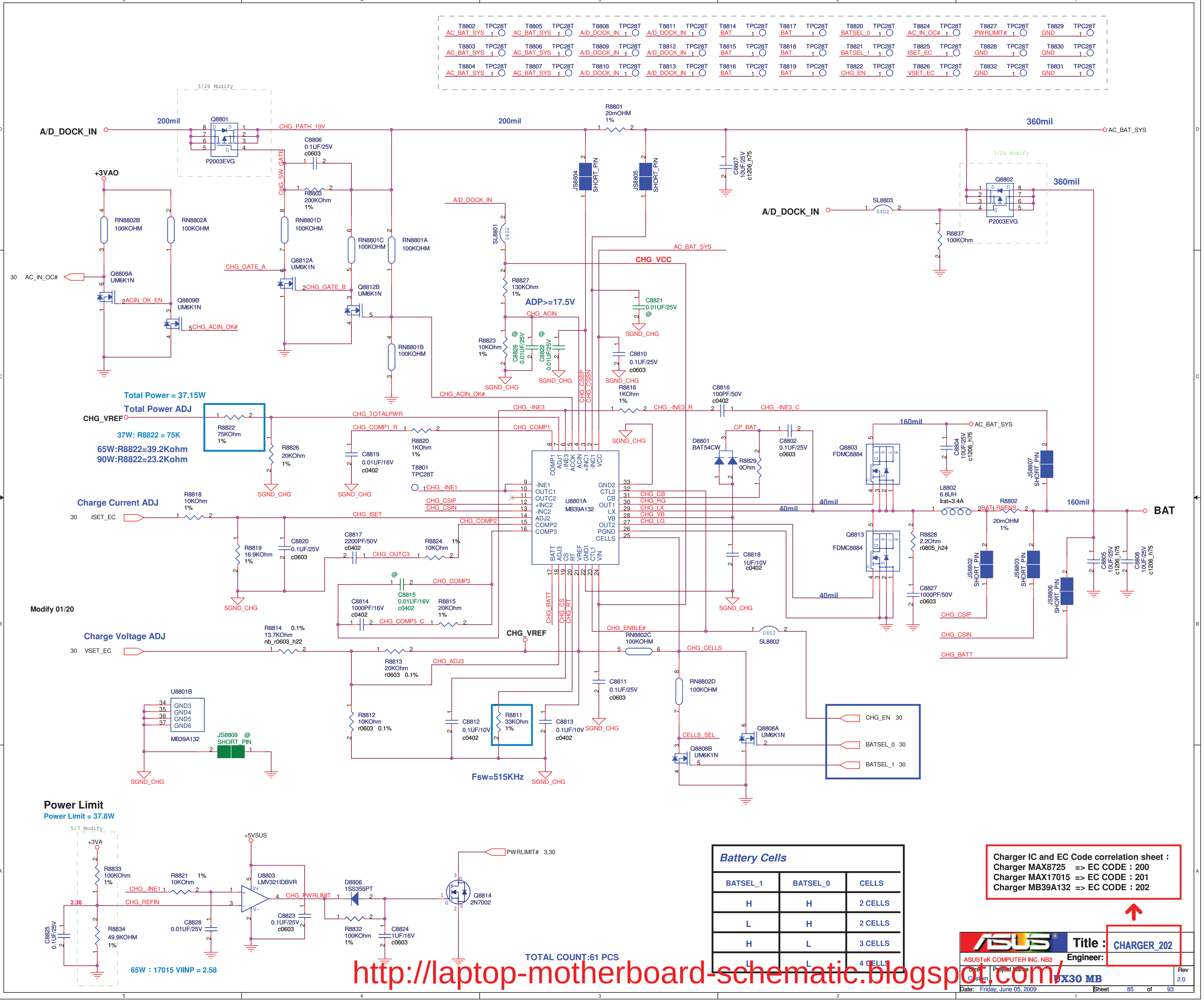
ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_ +1.5VS

Engineer: Aaron_Lin

Size B | Project Name UX30 MB | Rev 2.0

Date: Friday, June 05, 2009 Sheet 84 of 93



Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

ASUSTeK COMPUTER INC. NB3

Title : CHARGER_202

Engineer:

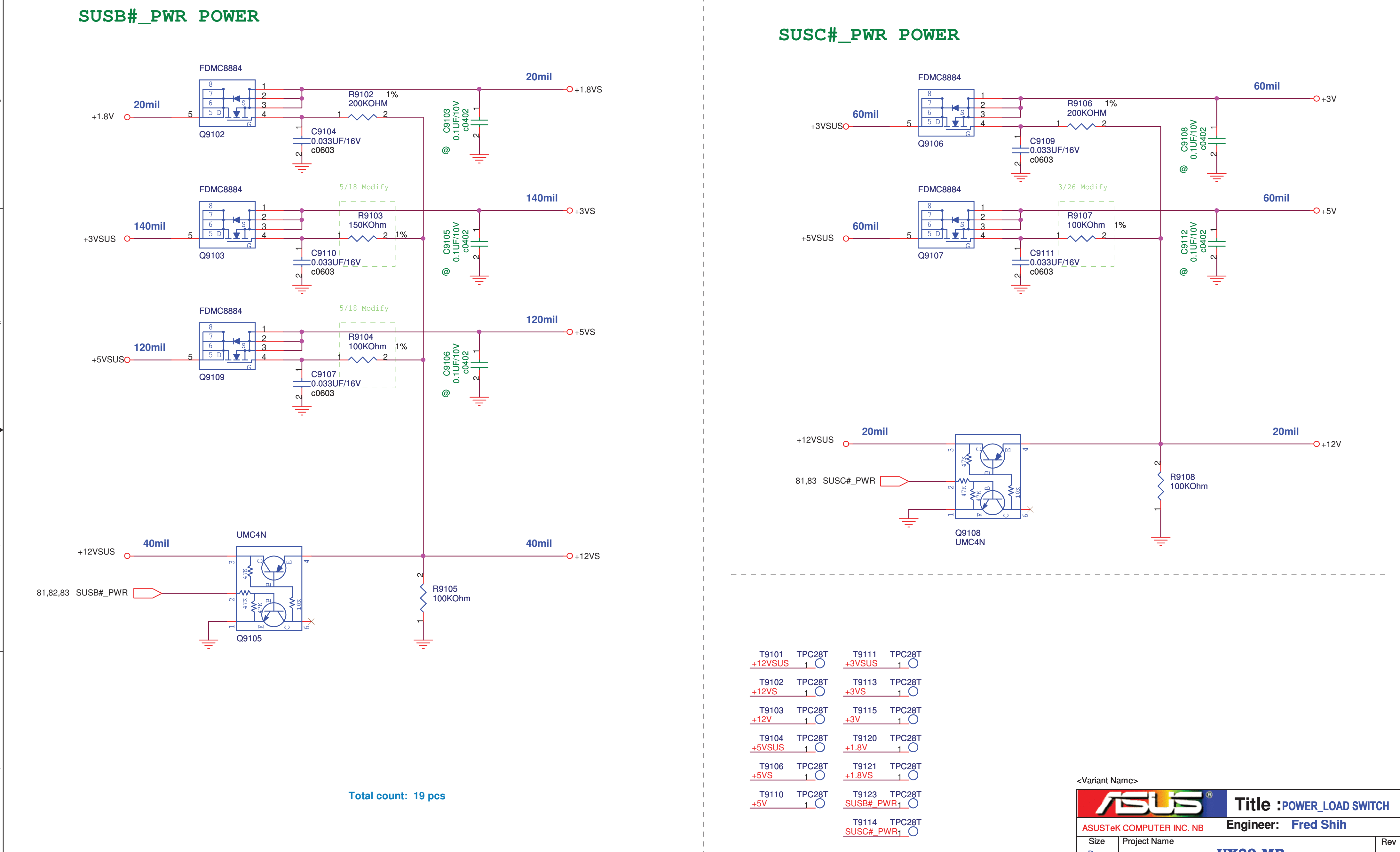
Size: Custom | Project Name: UX30 MB | Rev: 2.0

Date: Friday, June 05, 2009 | Sheet 85 of 93

BATTERY IN DETECT

<Variant Name>

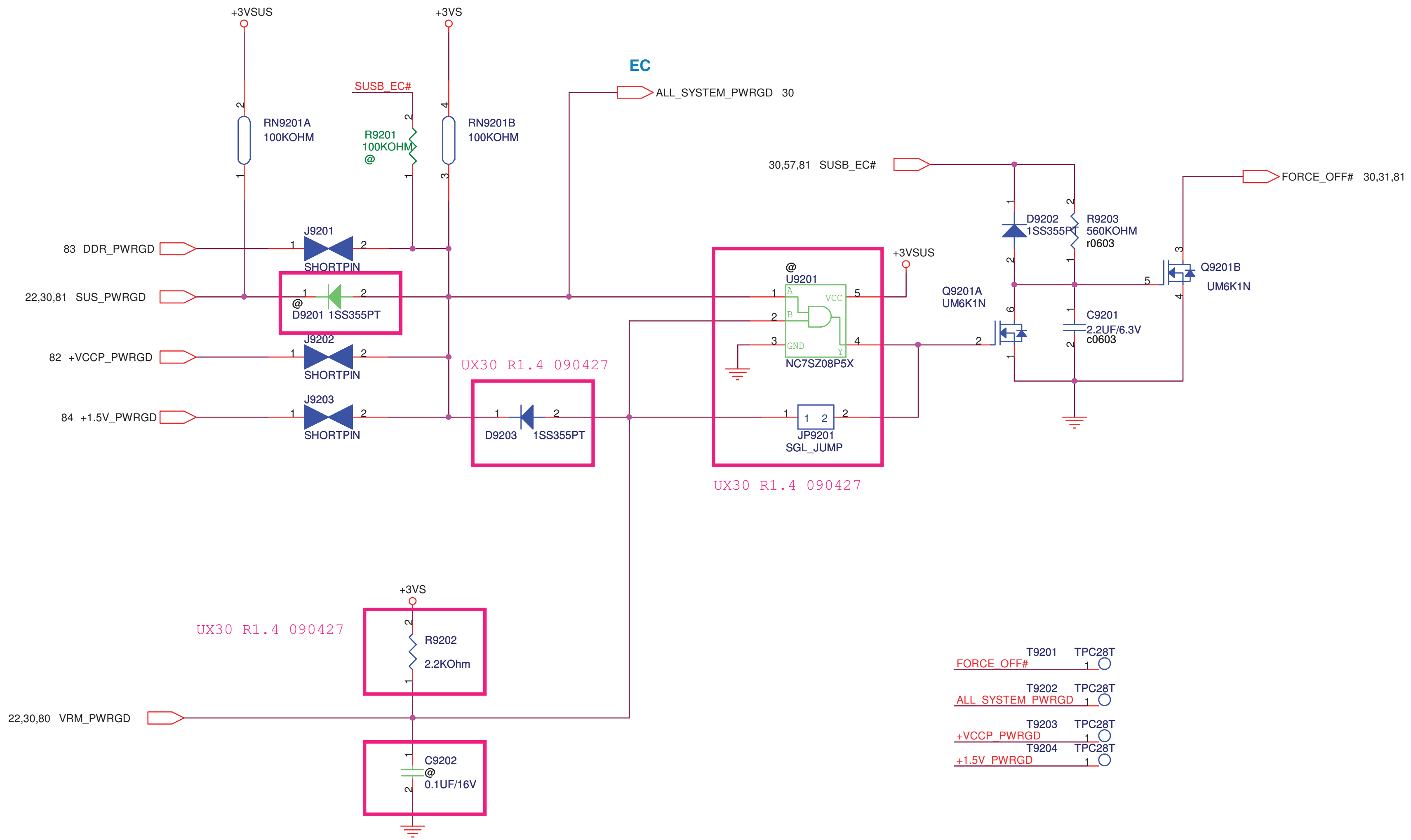
ASUSTeK COMPUTER INC. NB	Title : POWER_DETECT	
	Engineer: Aaron_Lin	
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 86 of 93	



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Fred Shih	
Size B	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 87 of 93	

POWER GOOD DETECTER



Total count: 8 pcs

<Variant Name>

ASUS	Title : POWER_PROTECT	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: B	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 88 of 93	

Net	Off-page connector	Sheets
AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,85
BAT	BAT	60,85
BAT_CON	BAT_CON	60,85
+3VAO	+3VAO	81,85
+5VA	+5VA	81
+3VA	+3VA	20,30,56,81,85
+5VAO	+5VAO	81
+5VO	+5VO	81
+5VSUS	+5VSUS	23,56,81,82,83,85,87
+5V	+5V	52,57,68,87
+5VS	+5VS	23,30,36,45,47,50,51,56,57,80,84,87
+3VO	+3VO	81
+3VSUS	+3VSUS	20,21,22,23,30,33,37,53,56,57,81,87,88
+3V	+3V	21,33,42,46,53,57,61,67,87
+3VS	+3VS	3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,57,80,87,88
+12VSUS	+12VSUS	81,87
+12V	+12V	37,87
+12VS	+12VS	22,46,53,87
+1.8VO	+1.8VO	83,84
+1.8V	+1.8V	8,9,11,14,19,57,83,87
+1.8VS	+1.8VS	15,87
+0.9VS	+0.9VS	9,57,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	82
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,57,82
+1.5VO	+1.5VO	84
+1.5VS	+1.5VS	4,15,20,23,36,37,53,57,84
+VCORE	+VCORE	4,5,80
A/D_DOCK_IN	A/D_DOCK_IN	60,85

Total sum count: 236 pcs

<Variant Name>

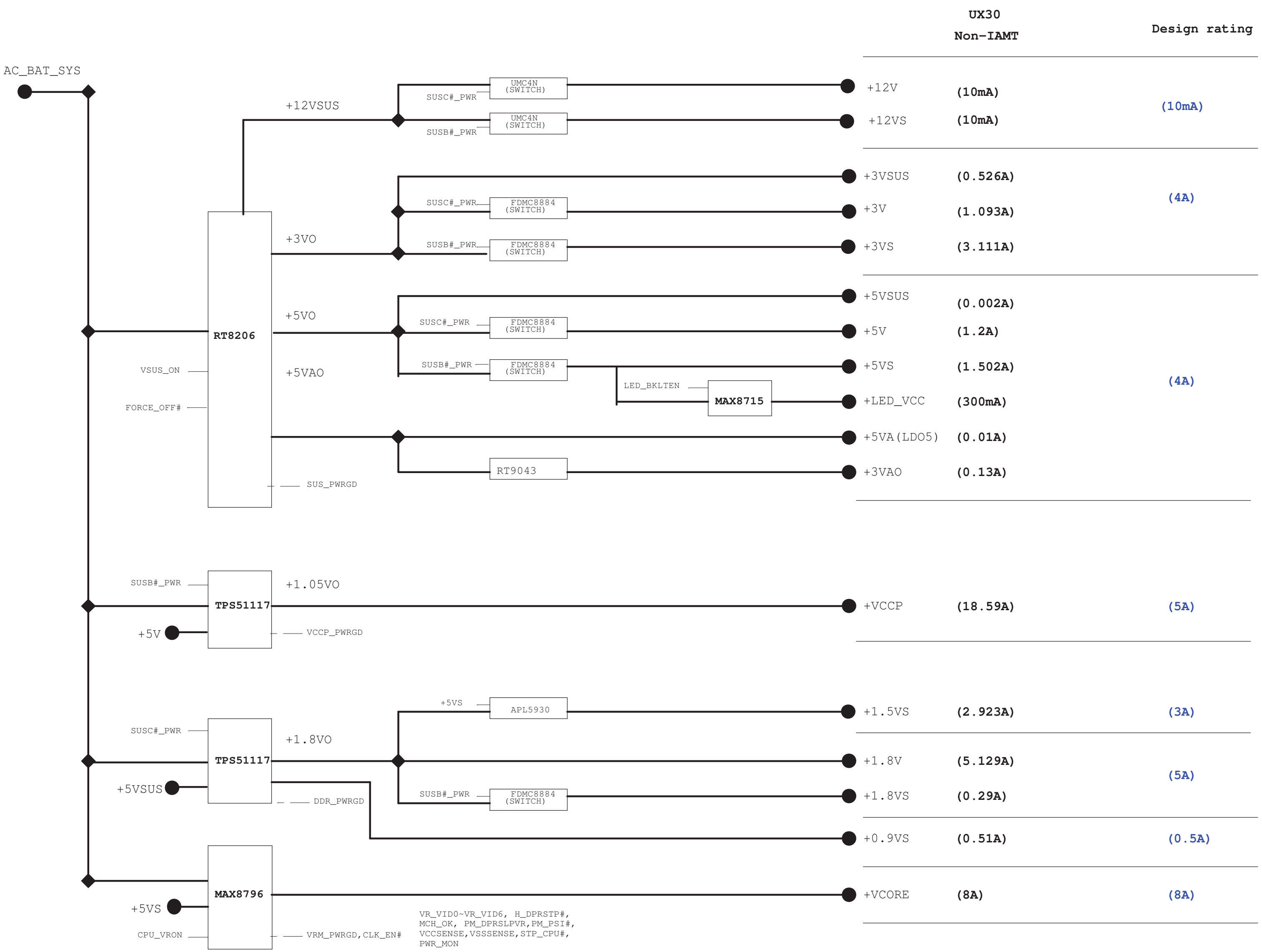
ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Aaron_Lin

Size: Custom | Project Name: **UX30 MB** | Rev: 2.0

Date: Friday, June 05, 2009 | Sheet 89 of 93



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Aaron_Lin

Size: Custom | Project Name: UX30 MB | Rev: 2.0

Sheet 90 of 93

Modify 2/13

AC_BAT_SYS

40mil

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_LED_VCC BOOST		
Engineer: Aaron_Lin		
Size: Custom	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 91 of 93	

E30 MB R1.1 Change List

1. Open Mask of JP3002 , JP3003 , JP8103 , JP8104 for SMT
2. Put on R2902 , C2913 , C2914 , JP3001 for SMT
3. Change R2911 from 22 Ohm to 10 Ohm for EA measure fail
4. Change R2910 from 22 Ohm to 10 Ohm and change net to CLK_SEL_48# for EA measure fail
5. Change Q4602 from SI3456BDV to SI3460BDV and add R4601 with 200K to GND for clear stocks
6. Change Q5302 from SI3456BDV to SI3460BDV and add R5307 with 200K to GND for clear stocks
7. Swap SL3621 and SL3622 for ACZ_Audio level change
8. Swap J4201 Pin 10 / 11 NET Name (SDCDN/XDWRN / SDWP/XDCLE/MSCLK) for SD Detection
9. Remove U3102 and C3105 for LID_SW# function for error design on MB
10. Add Q3704 and R3704 for Audio Level shift from +1.5VS to +3VS
11. Change BT Connector J6101 from 10 Pin to 6 Pin for N10 common use
12. Swap RTC Battery Connector CON2001 Pin Define for RTC common pin define
13. Change X3301 from 07G010S22500 to 07G010212502
14. Change R2904 , R2906 , R2907 from 22 Ohm to 10 Ohm for EA measure
15. Change J5601 from 6 pin to 8 pin and change pin define for PM spec change
16. Remove J4701 and related net for SR2 change
17. Change J3401 from 12G14830108D to 12G148611083 for ID design
18. Change J3701 , J3702 from 12G171030022 to 12G17100002C for Cost down
19. Change CON4601 from 12G170040308 to 12G170040308 for Cost down
20. Add H6530 for ME screw hole
21. Change J5604 from 12G171030140 to 12G171030121 for ID design
22. Remove J5603 , J6001 and change to J5602 on DC-IN BD for ME cost down
23. Change D3401 , D3402 , D5201 from 07G001250010 to 07G028075010 for EE Cost down
24. Change SL4602 to L4605 for EMI test
25. Add L8003 for EMI test
26. Delete Num_LED# function for Spec change

<OrgName>	Title : HISTORY	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 2.0
Date: Friday, June 05, 2009	Sheet 92 of 94	

UX30 MB R1.4 Change List

1. Swap USB D+ , D- of BT on Page 61
2. Add C4710 , R4704 and C4711 , R4705 on Hsync and Vsync to improve CRT display quality on Page 47
3. Modify J5602 Pin 1 , 3 , 5 , 7 to GND for Apater use on Page 56
4. Change J6801 from 12G183402207 to 12G18340200T for cost down on Page 68
5. Change J5604 Pin 10 from +3VSUS to +3VA for Hall sensor on Page 56
6. Change H6501 from Screw Hole to a NUT for ME assembly on Page 65
7. Change PCB ID from R1.1 to R1.4 on Page 22
8. Add R2229 , R2231 on GPIO6 for On Board Memory Size and R2231 , R2232 on GPIO7 for Memory Vendor on Page 22
9. Change J5301 from 12G03010052K to 12G03010052P on Page 53
10. Change J0801 from 12G02502200F to 12G02502200S on Page 8
11. Change U3601 from 02G611005001 to 02G611005006 on Page 36

ASUS	Title : HISTORY_ER	
<OrgName>	Engineer: Uei Lee & Hacken	
Size: B	Project Name: UX30 MB	Rev: 2.0
Date: Friday, June 05, 2009	Sheet 93 of 94	

5 4 3 2 1

D

UX30 MB R2.0 Change List

1. Add SW3101 , R3101 , C3105 for EC Force OFF function on Page 31
2. REMOVE JP1507 JP1501 JP1503 JP1504 JP2304 JP2308 JP2313 JP2312 J3301 J3303 J3304
3. ADD PANEL BACKLIGHT POWER SOFT START CIRCUIT
4. ADD R5307 R4604
5. CHANGE ESD DIODE OF THE BATTERY CONNECTOR.
6. Put on C4704 , C4705 , C4706 for CRT EMI issue on 090606
7. Change C3008 , C3009 , C2001 , C2002 from 7PF to 18PF on090606
8. Add J5601 for Cost down on 090606
9. Change C4617 from 0.1uF to 1uF on090606

C

B

A

	Title : HISTORY_PR		
<OrgName>	Engineer: Uei Lee & Hacken		
Size B	Project Name UX30 MB		Rev 2.0
Date: Friday, June 12, 2009	Sheet 94	of 94	

5 4 3 2 1