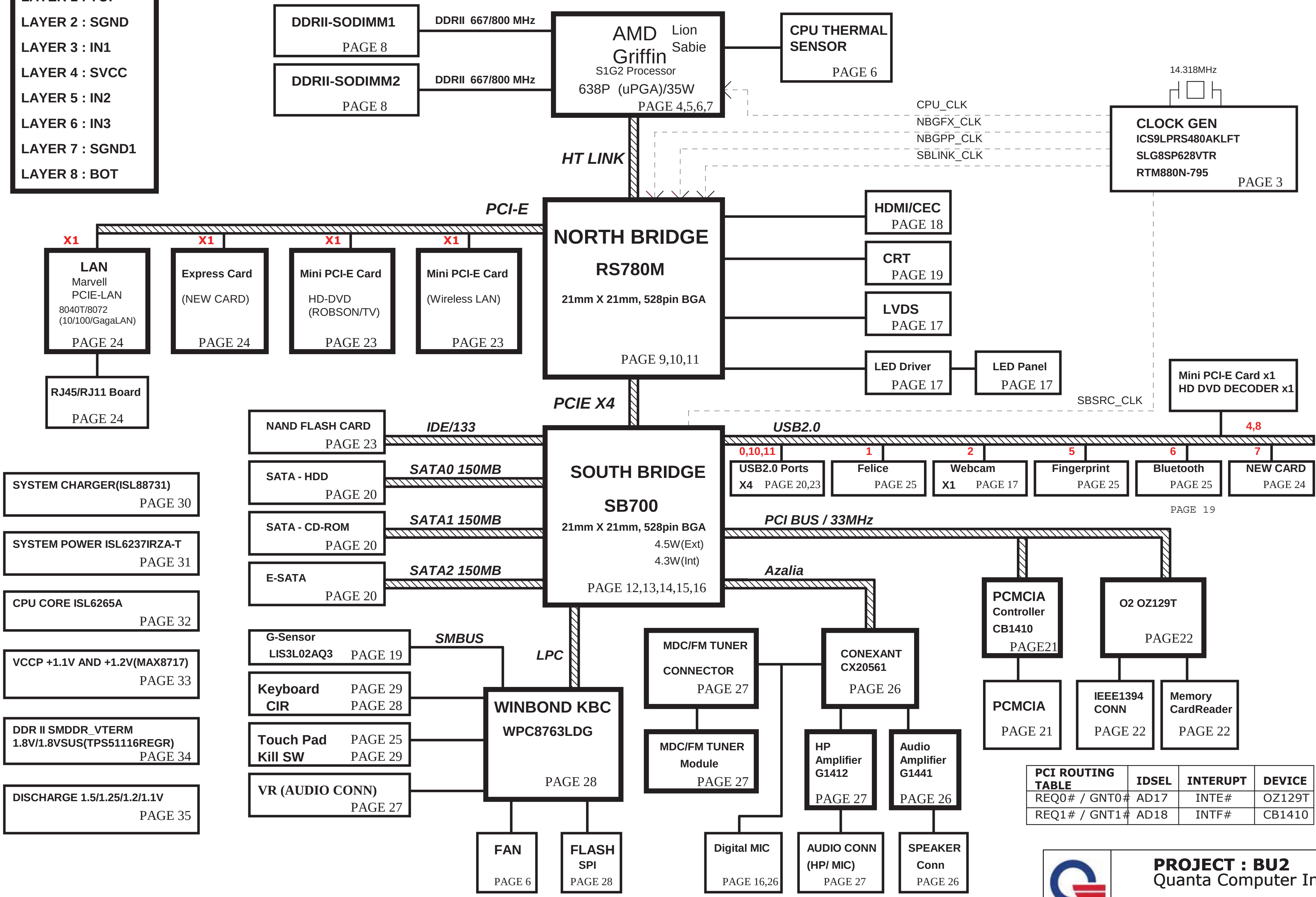
BU2 SYSTEM DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410

PROJECT : BU2
Quanta Computer Inc.

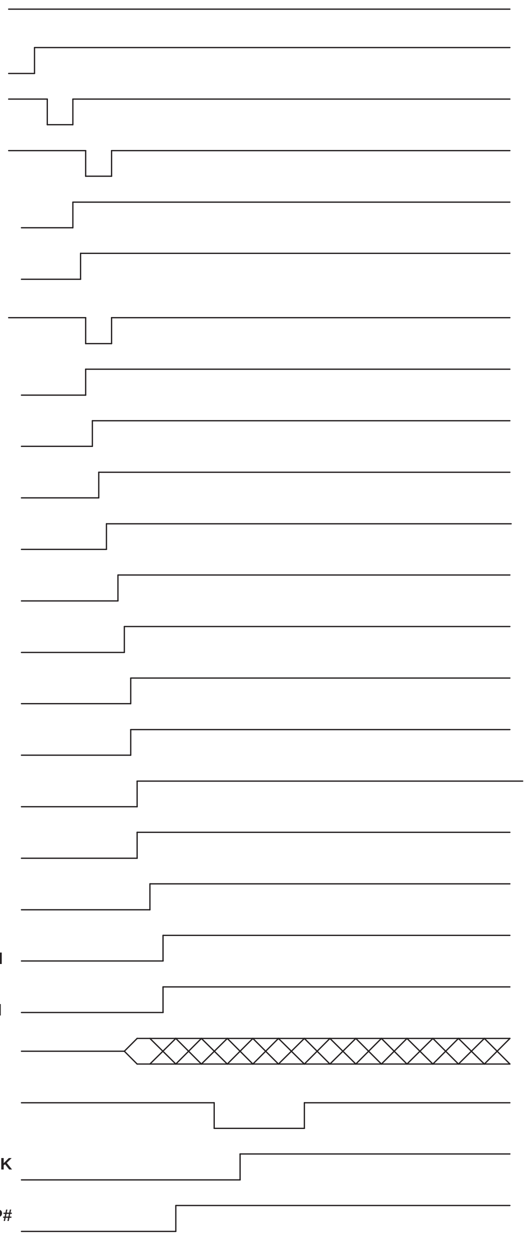
NB4

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, January 30, 2008 Sheet 1 of 35

INDEX

Power Sequence



02

SB700 SM BUS

SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)

PROJECT : BU2
Quanta Computer Inc.

NB4

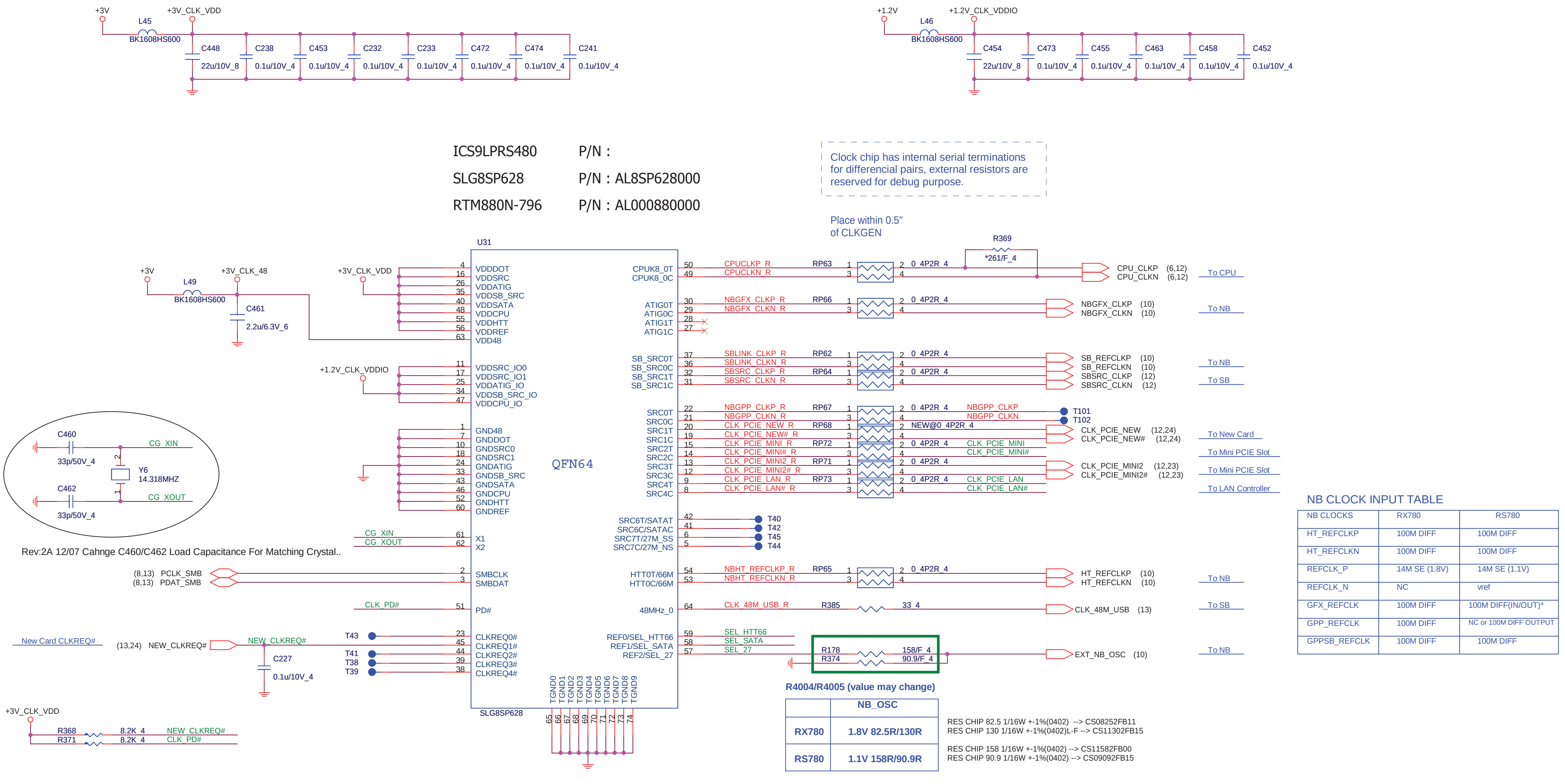
Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

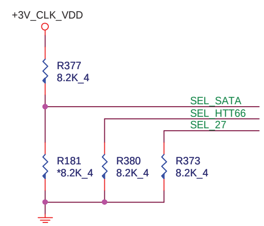
Date: Thursday, November 08, 2007 | Sheet 2 of 35

CLK_GEN_SLG8SP628

ICS9LPRS480	P/N :
SLG8SP628	P/N : AL8SP628000
RTM880N-796	P/N : AL000880000

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.





R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15

RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

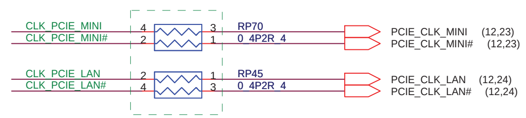
NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

FOR EXTERMAL/INTERNAL CLOCK



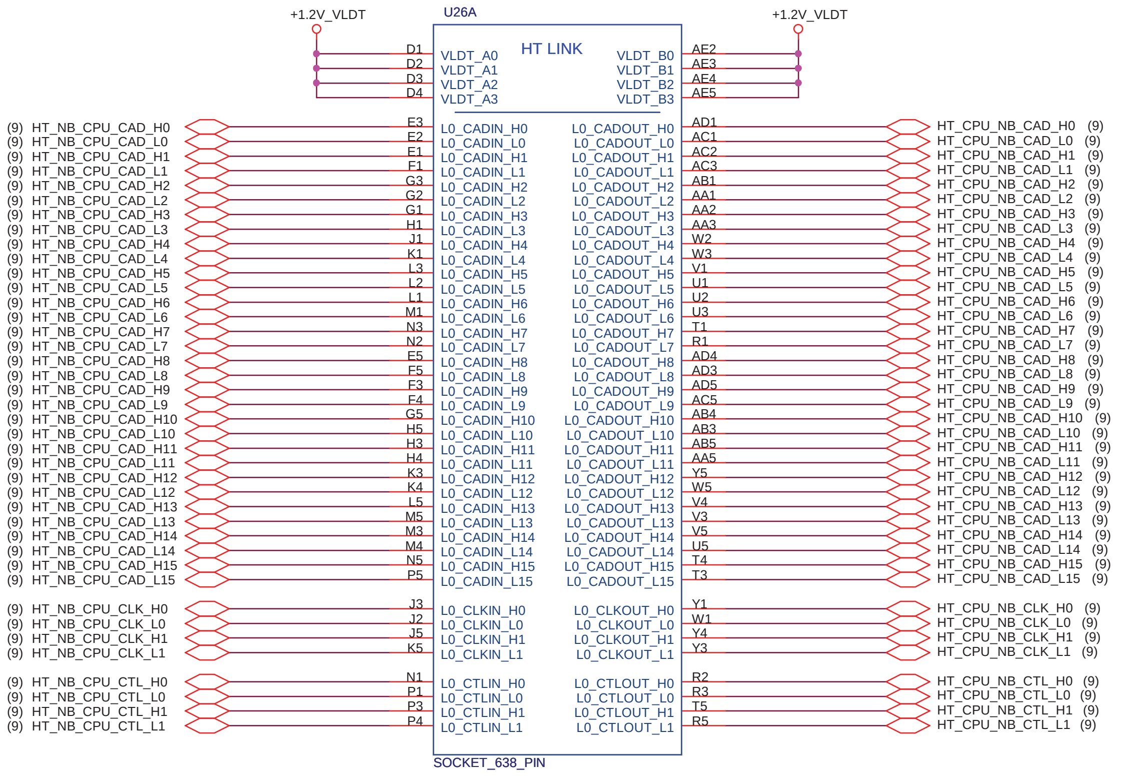
Place Close to Drivers Side

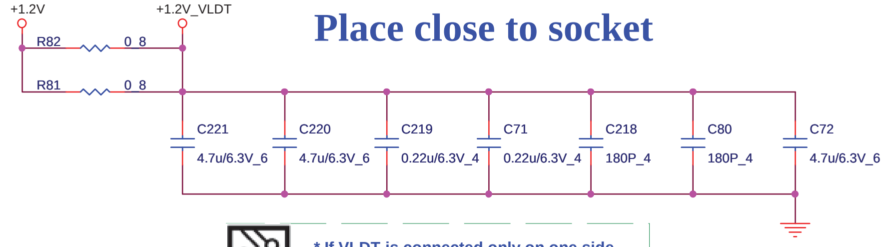
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR_SLG8SP628	1A

Date: Thursday, July 24, 2008 Sheet 3 of 35

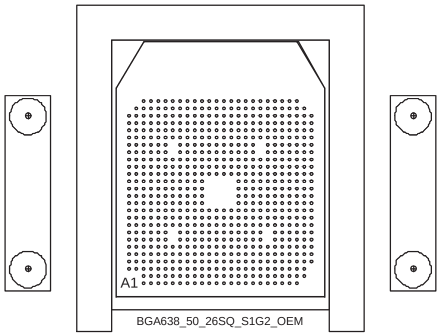
NB4





Place close to socket

* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

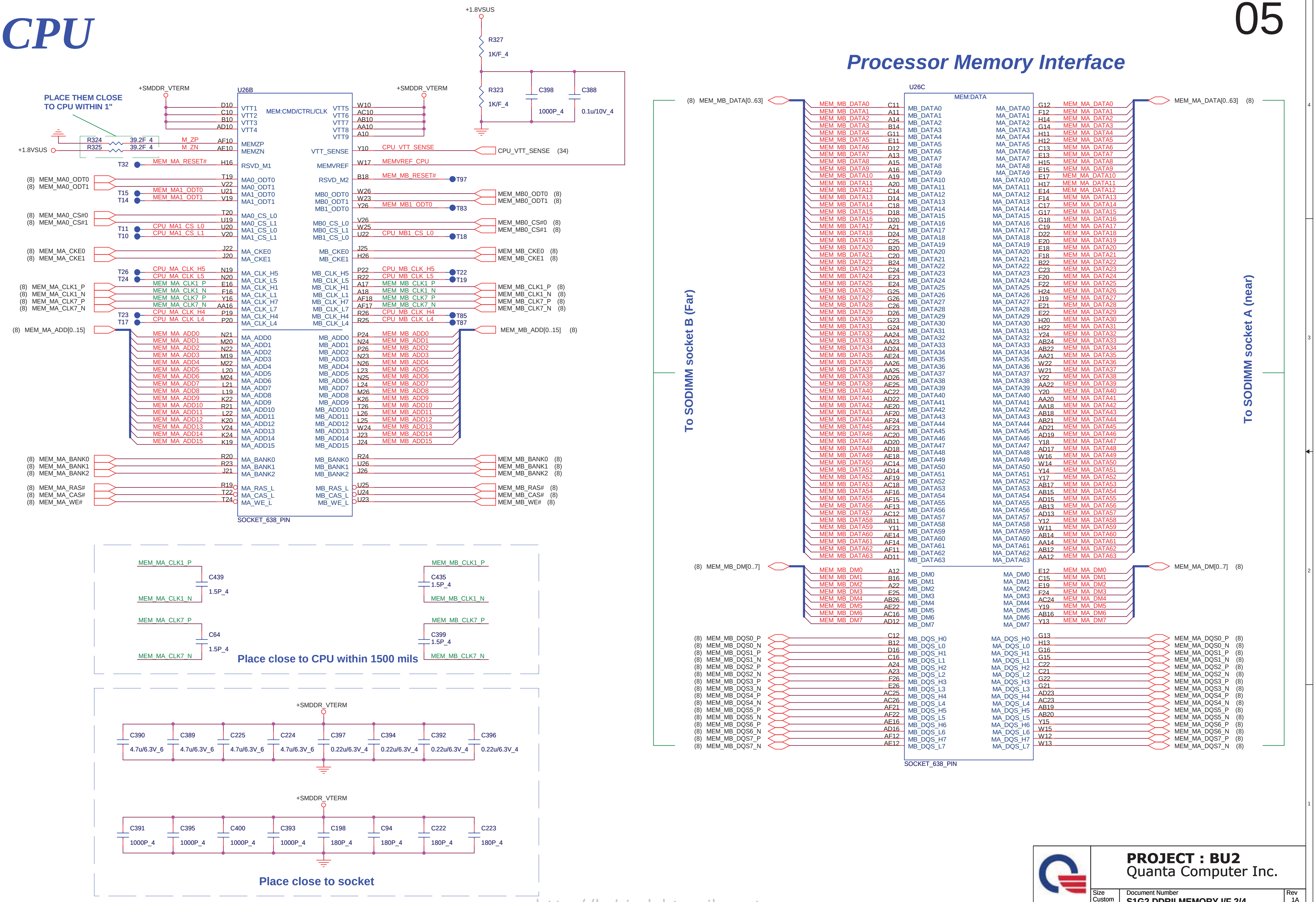


CPU

NB4	PROJECT : BU2 Quanta Computer Inc.	
Size B	Document Number S1G2 HT I/F 1/4	Rev 1A
Date: Thursday, July 24, 2008	Sheet 4 of 35	

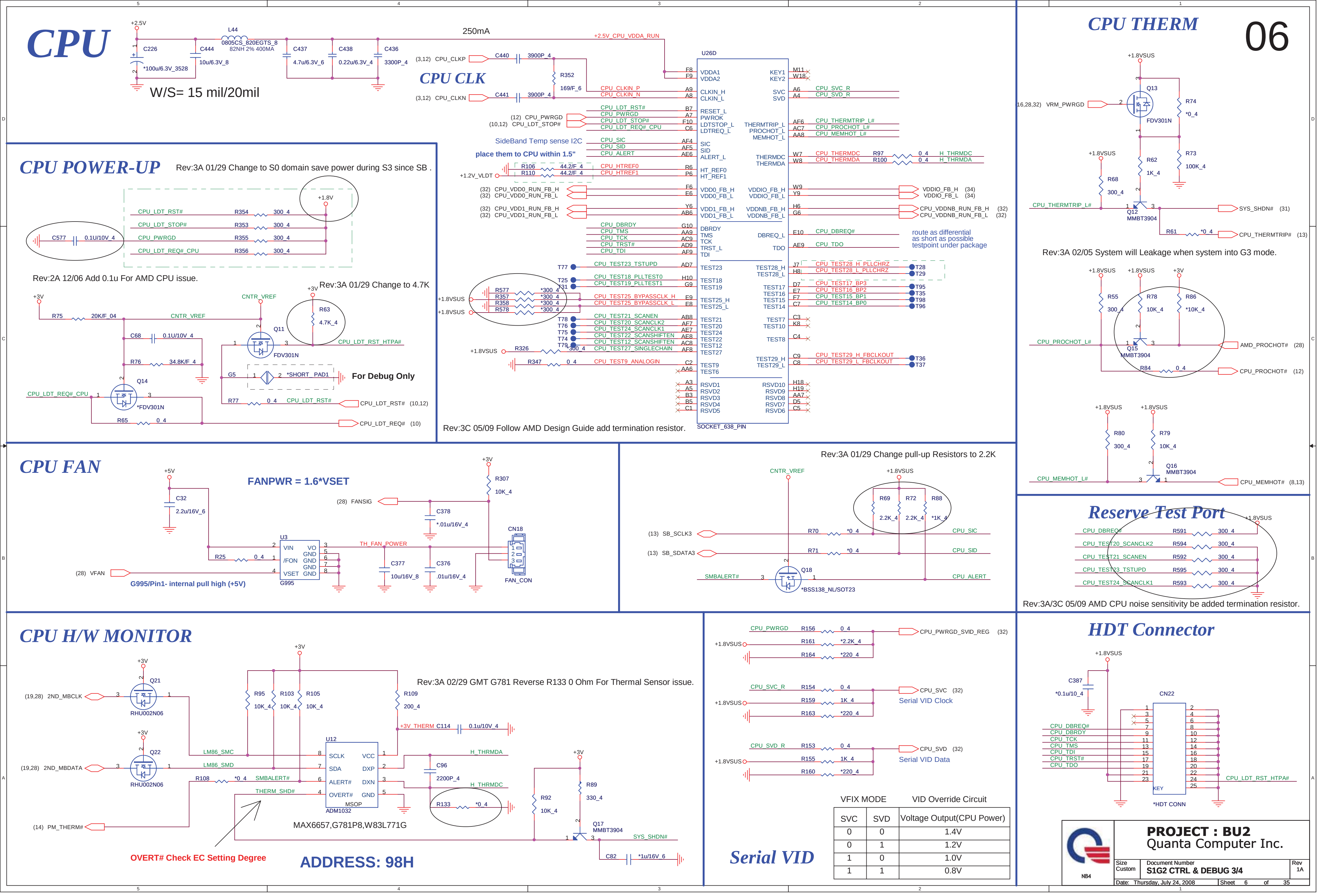
CPU

Processor Memory Interface



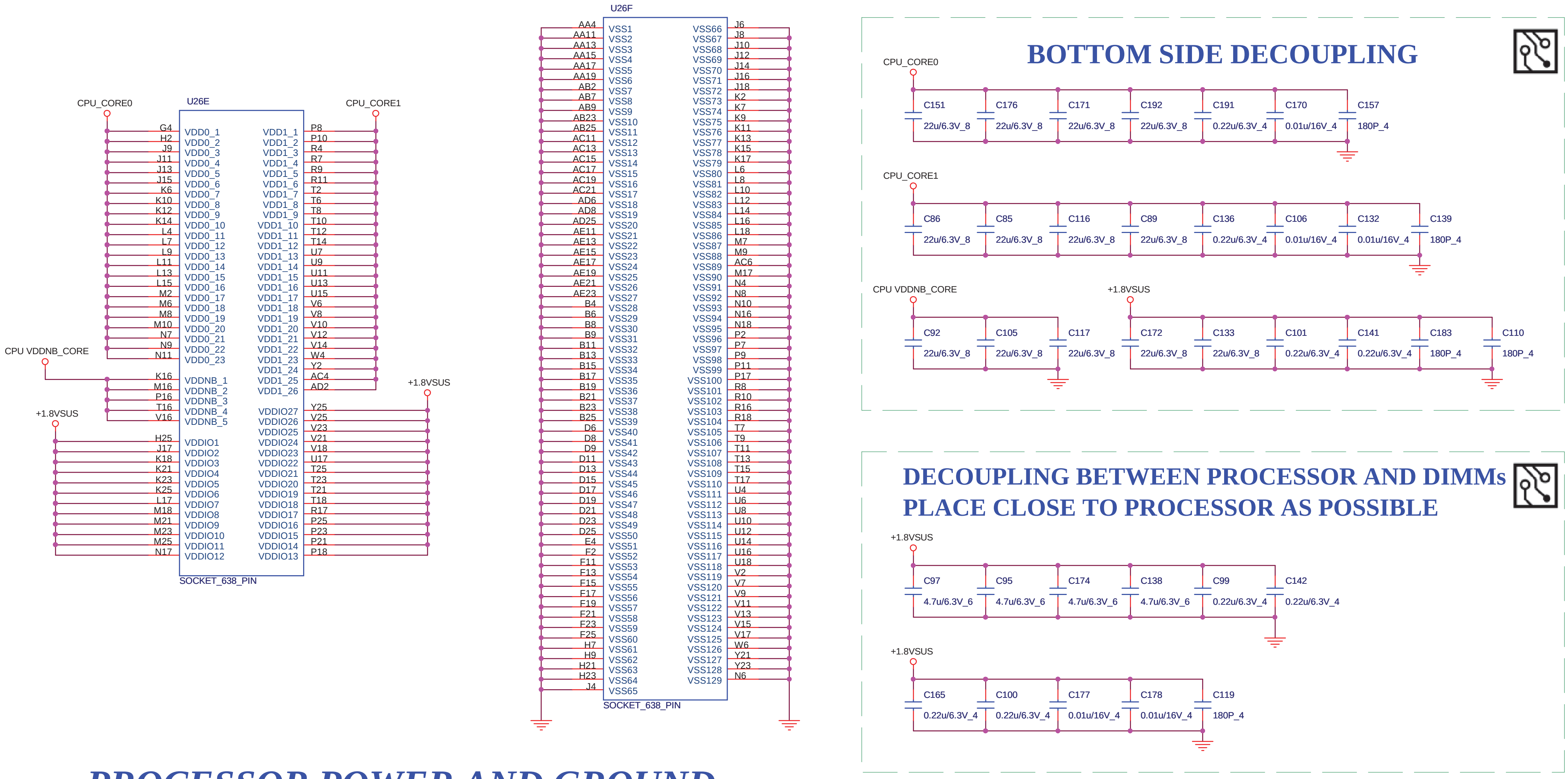
PROJECT : BU2	Quanta Computer Inc.
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/4
Rev: 1A	
Date: Thursday, July 24, 2008	Sheet 5 of 35

NB4



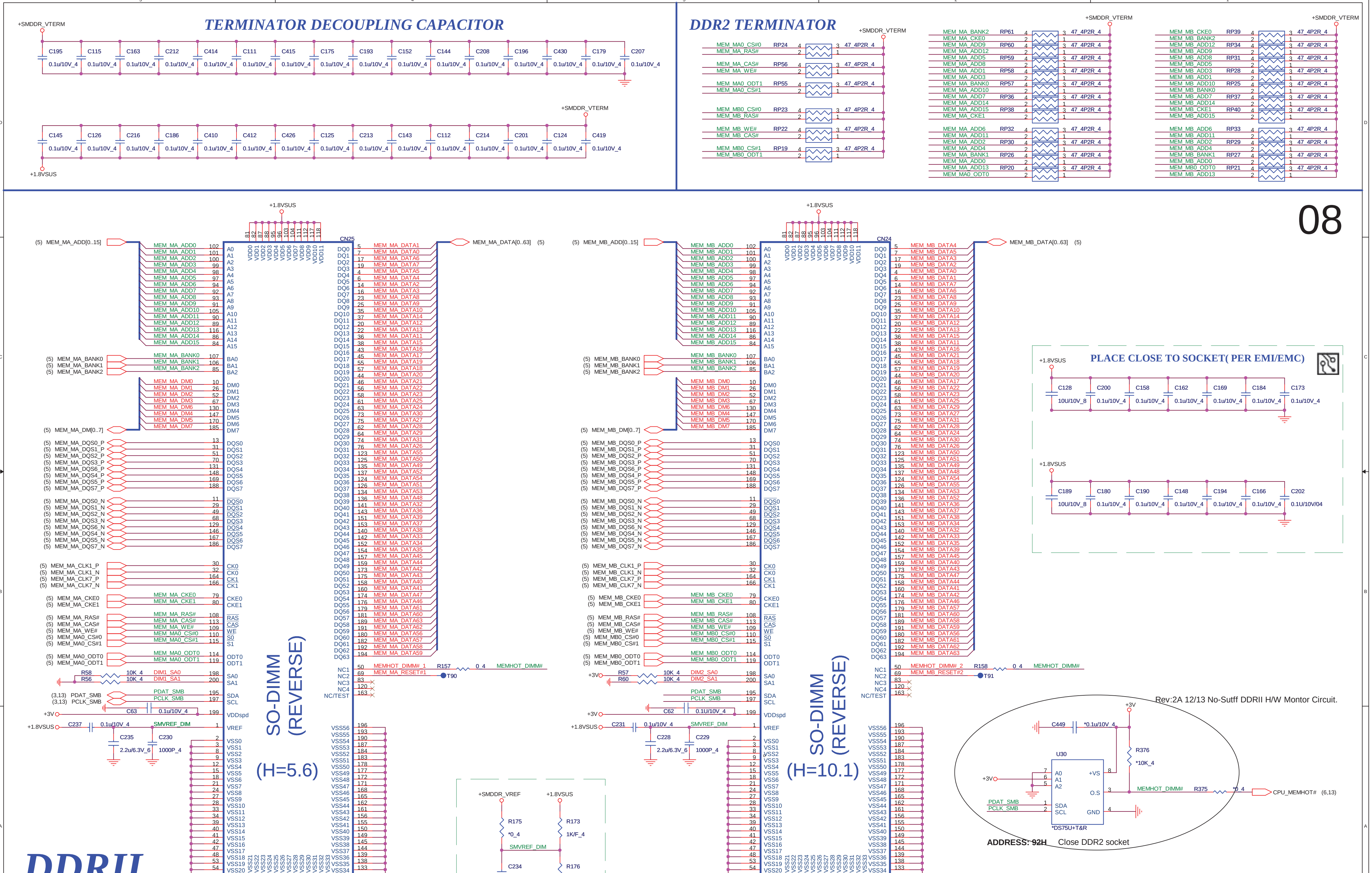
VFIX MODE		VID Override Circuit
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

CPU



PROCESSOR POWER AND GROUND

NB4	**PROJECT : BU2** Quanta Computer Inc.	
Size: Custom	Document Number: S1G2 PWR & GND 4/4	Rev: 1A
Date: Wednesday, December 19, 2007	Sheet 7 of 35	



PROJECT : BU2

Quanta Computer Inc.

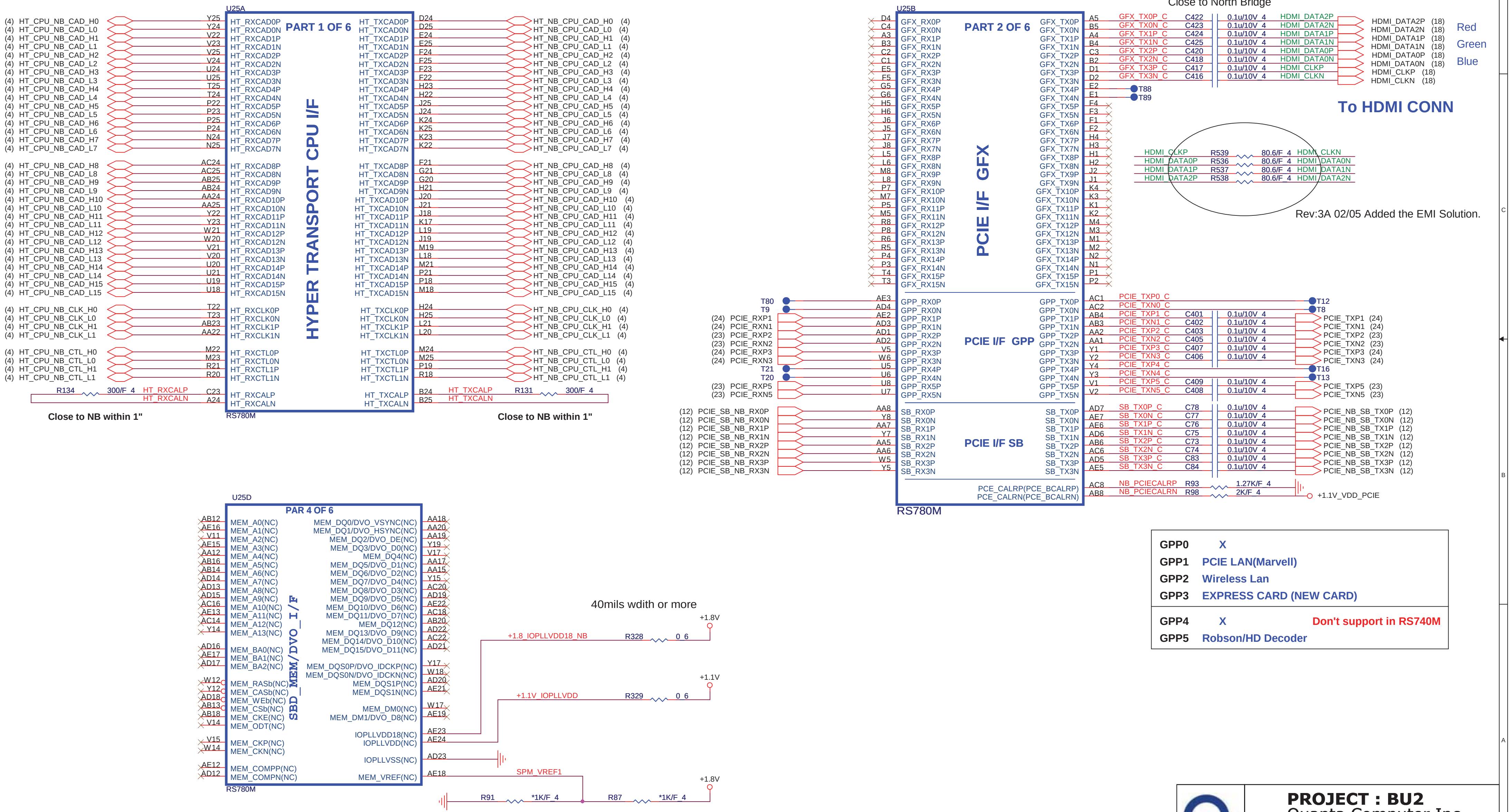
Size	Document Number	Rev
Custom	DDR2 SODIMMS: A/B CHANNEL	1A

Date: Thursday, July 24, 2008 Sheet 8 of 35

RS780

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



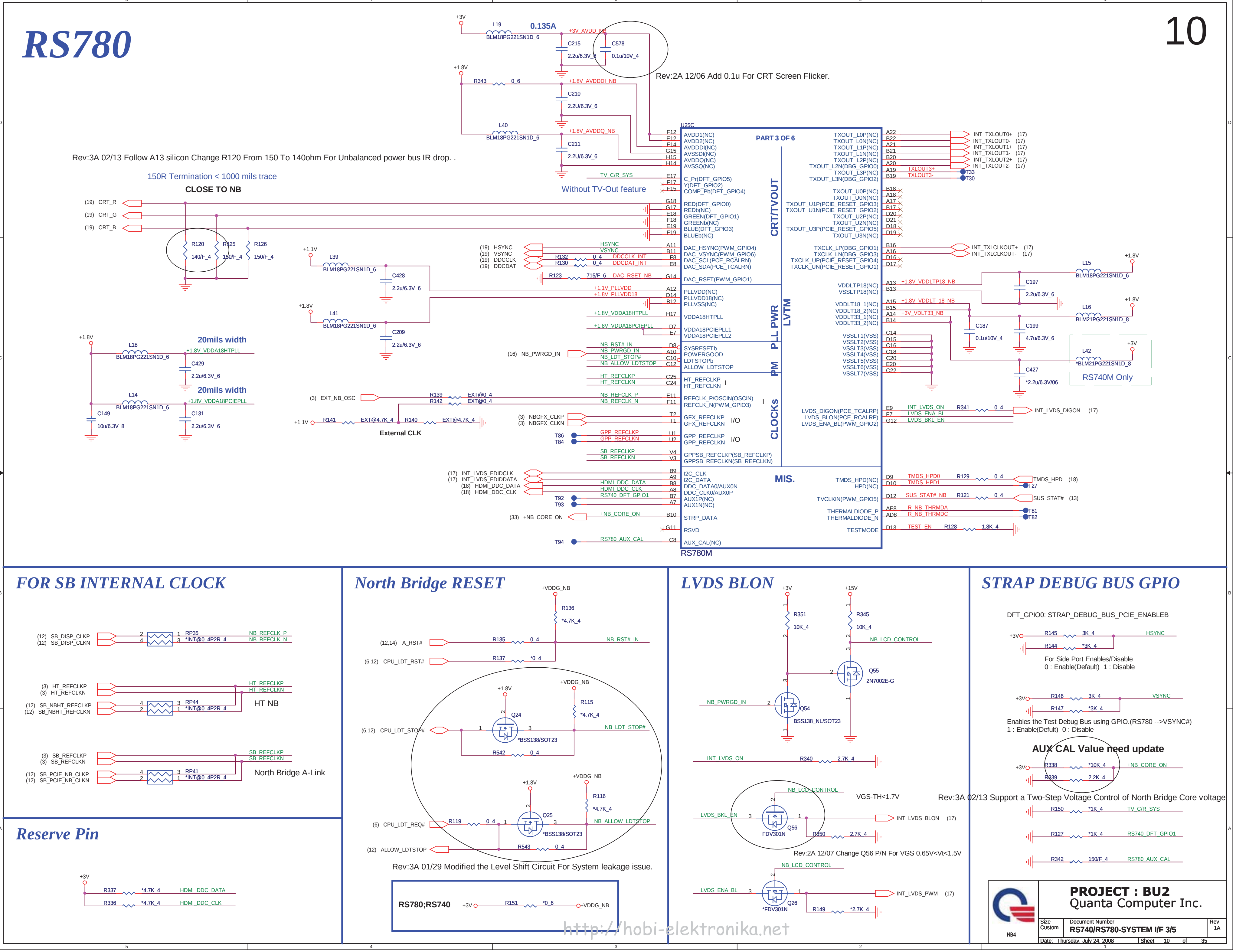
GPP0	X	
GPP1	PCIE LAN(Marvell)	
GPP2	Wireless Lan	
GPP3	EXPRESS CARD (NEW CARD)	
GPP4	X	Don't support in RS740M
GPP5	Robson/HD Decoder	

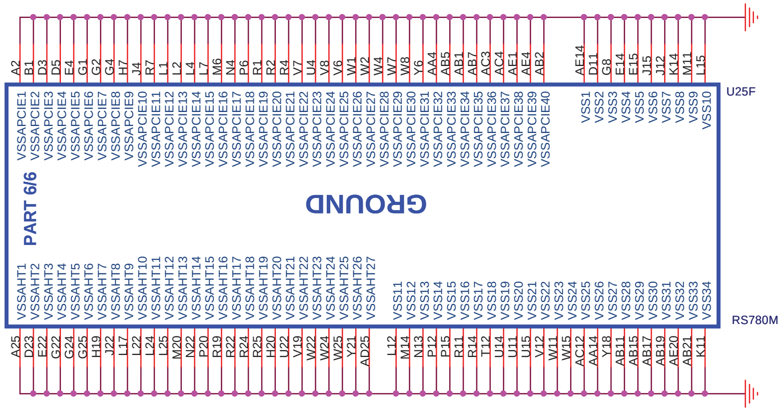
PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	RS740/RS780-HT LINK/PCIE I/F 1/4	1A

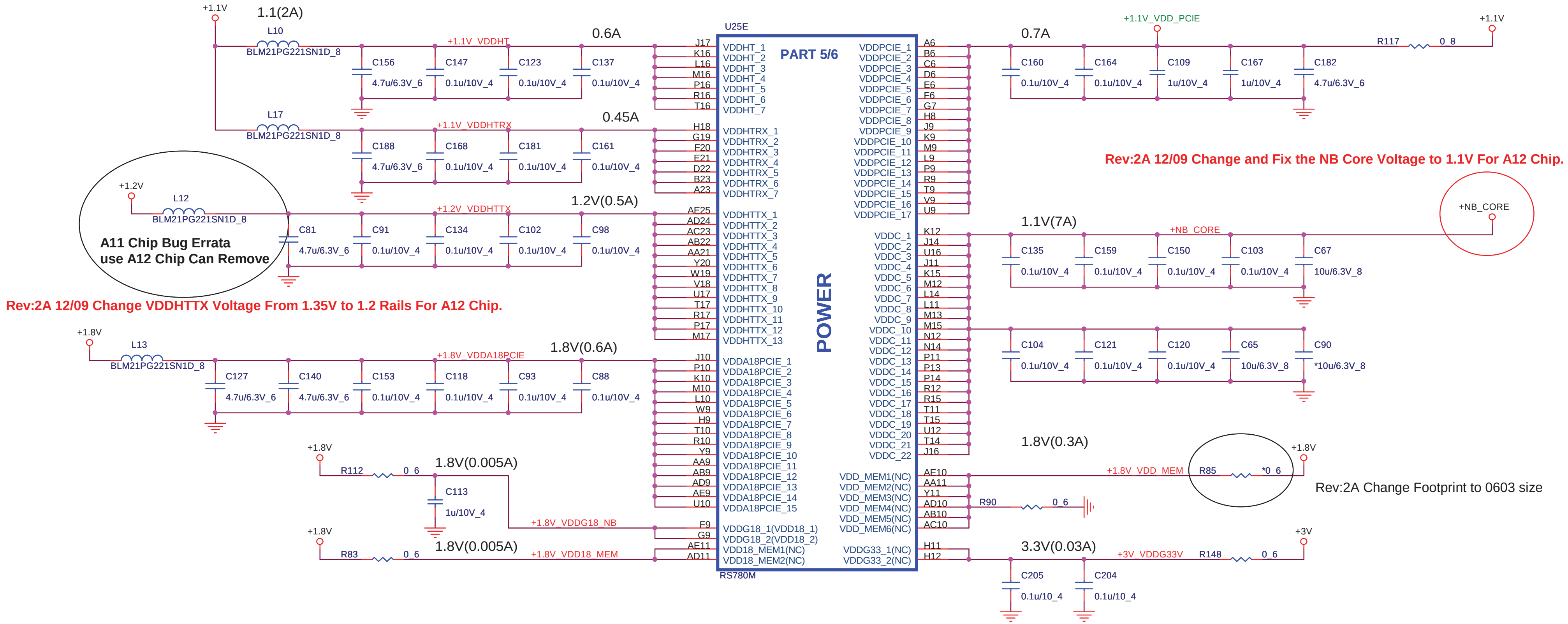
Date: Thursday, July 24, 2008 Sheet 9 of 35


RS780
10
0.135A
Rev:2A 12/06 Add 0.1u For CRT Screen Flicker.
Rev:3A 02/13 Follow A13 silicon Change R120 From 150 To 140ohm For Unbalanced power bus IR drop. .
150R Termination < 1000 mils trace
CLOSE TO NB
Without TV-Out feature
PART 3 OF 6
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKS
MIS.
20mils width
20mils width
External CLK
RS740M Only
RS780M
FOR SB INTERNAL CLOCK
HT NB
North Bridge A-Link
North Bridge RESET
Rev:3A 01/29 Modified the Level Shift Circuit For System leakage issue.
RS780;RS740
LVDS BLON
VGS-TH<1.7V
Rev:2A 12/07 Change Q56 P/N For VGS 0.65V<Vt<1.5V
STRAP DEBUG BUS GPIO
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEB
For Side Port Enables/Disable
0 : Enable(Default) 1 : Disable
Enables the Test Debug Bus using GPIO.(RS780 -->VSYNC#)
1 : Enable(Deflult) 0 : Disable
AUX CAL Value need update
Rev:3A 02/13 Support a Two-Step Voltage Control of North Bridge Core voltage
Reserve Pin
PROJECT : BU2
Quanta Computer Inc.
Document Number
RS740/RS780-SYSTEM I/F 3/5
Rev 1A
Date: Thursday, July 24, 2008
Sheet 10 of 35
http://hobi-elektronika.net



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

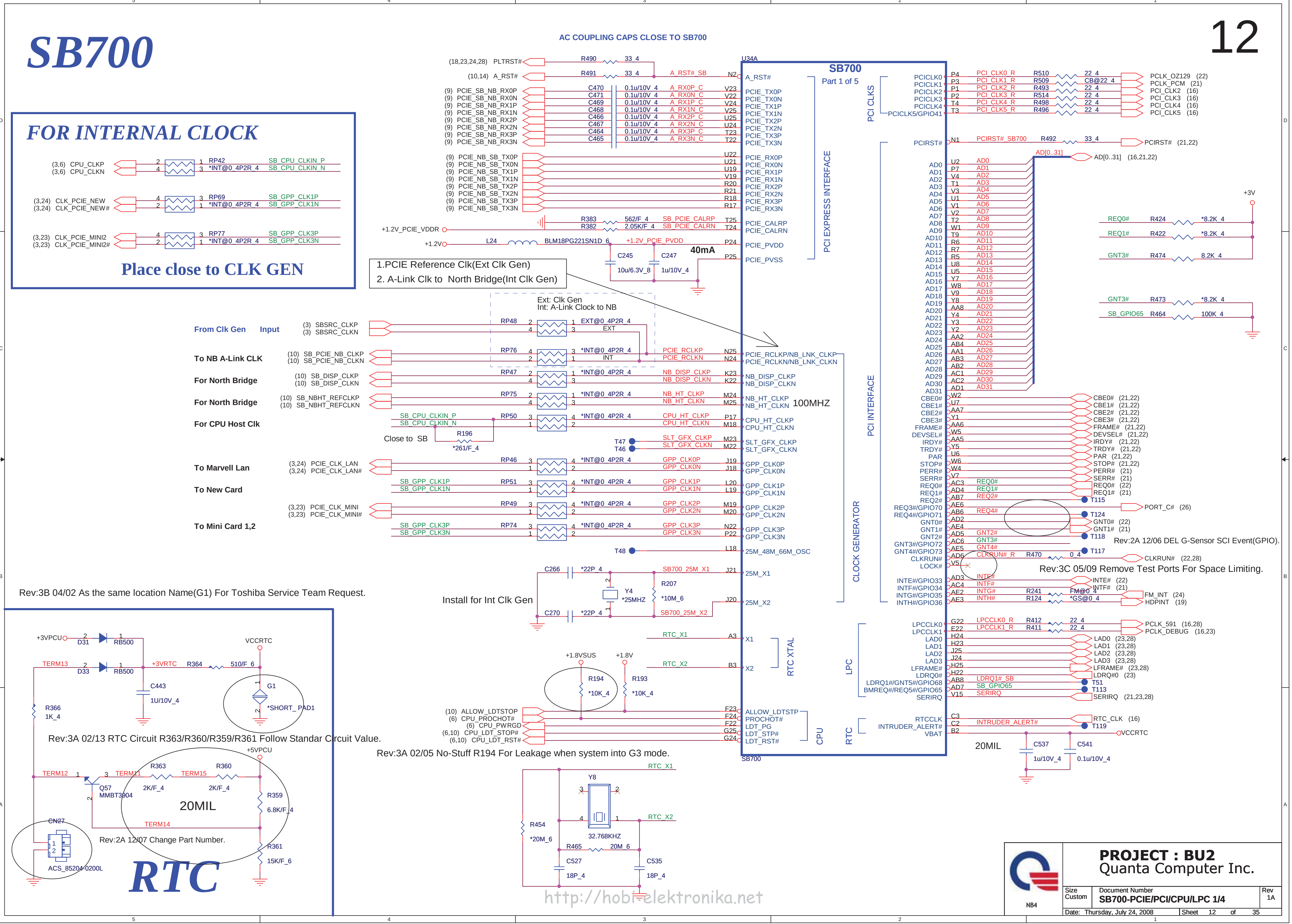


RS780

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

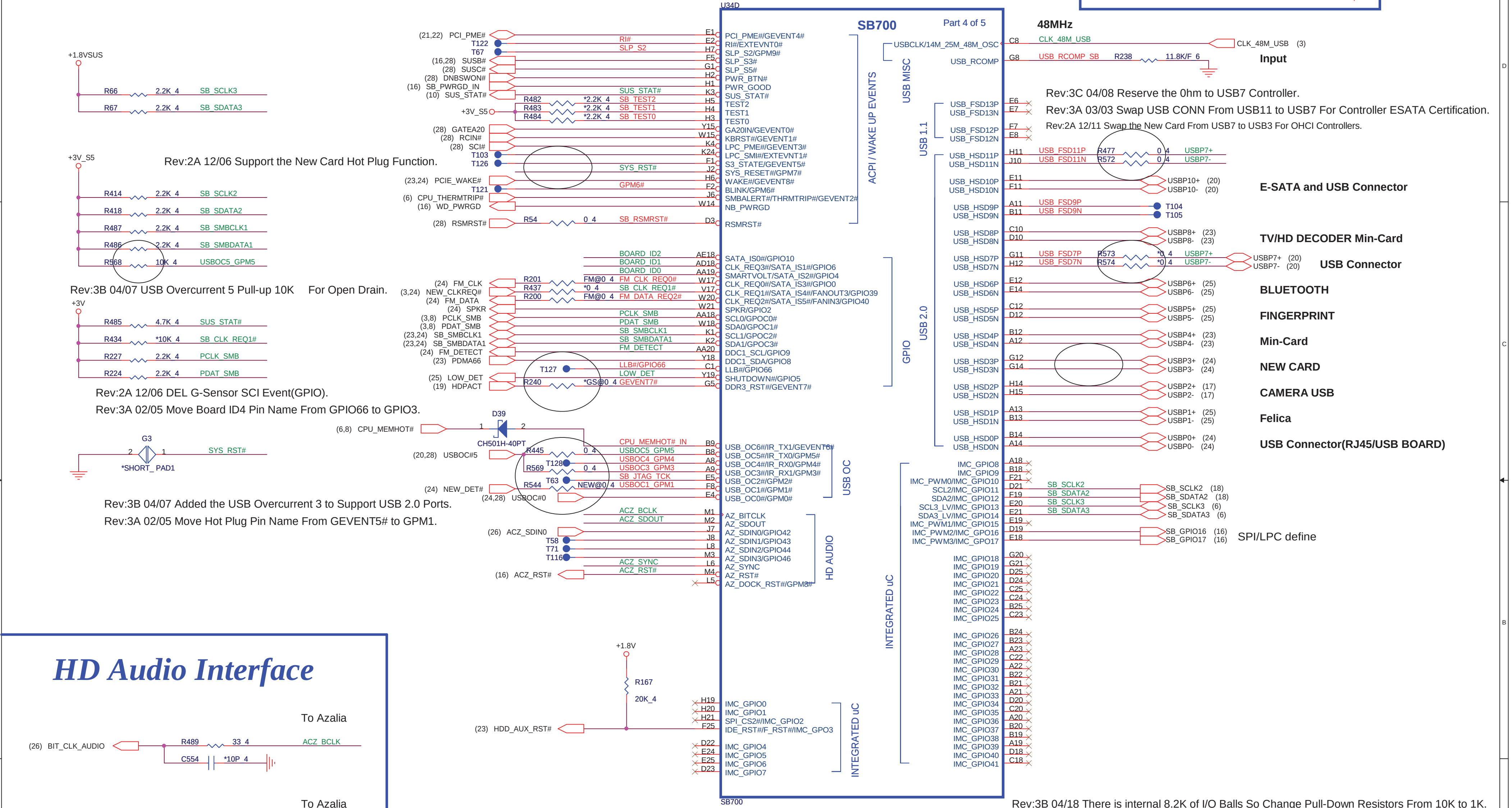
Date: Thursday, April 10, 2008 Sheet 11 of 35



SB700
12
AC COUPLING CAPS CLOSE TO SB700
FOR INTERNAL CLOCK
Place close to CLK GEN
(3,6) CPU_CLKP
(3,6) CPU_CLKN
RP42 *INT@0_4P2R_4 SB_CPU_CLKIN_P SB_CPU_CLKIN_N
(3,24) CLK_PCIE_NEW
(3,24) CLK_PCIE_NEW#
RP69 *INT@0_4P2R_4 SB_GPP_CLK1P SB_GPP_CLK1N
(3,23) CLK_PCIE_MINI2
(3,23) CLK_PCIE_MINI2#
RP77 *INT@0_4P2R_4 SB_GPP_CLK3P SB_GPP_CLK3N
(18,23,24,28) PLTRST#
(10,14) A_RST#
R490 33_4
R491 33_4 A_RST#_SB
U34A
SB700
Part 1 of 5
PCIE_SB_NB_RX0P PCIE_SB_NB_RX0N PCIE_SB_NB_RX1P PCIE_SB_NB_RX1N PCIE_SB_NB_RX2P PCIE_SB_NB_RX2N PCIE_SB_NB_RX3P PCIE_SB_NB_RX3N
C470 C471 C469 C468 C466 C467 C464 C465 0.1u/10V_4
PCIE_NB_SB_TX0P PCIE_NB_SB_TX0N PCIE_NB_SB_TX1P PCIE_NB_SB_TX1N PCIE_NB_SB_TX2P PCIE_NB_SB_TX2N PCIE_NB_SB_TX3P PCIE_NB_SB_TX3N
+1.2V_PCIE_VDDR
R383 562/F_4 SB_PCIE_CALRP
R382 2.05K/F_4 SB_PCIE_CALRN
+1.2V L24 BLM18PG221SN1D_6 +1.2V_PCIE_PVDD
40mA
C245 10u/6.3V_8
C247 1u/10V_4
PCIE_CALRP PCIE_CALRN PCIE_PVDD PCIE_PVSS
PCI EXPRESS INTERFACE
1.PCIE Reference Clk(Ext Clk Gen)
2. A-Link Clk to North Bridge(Int Clk Gen)
Ext: Clk Gen
Int: A-Link Clock to NB
From Clk Gen Input
(3) SBSRC_CLKP
(3) SBSRC_CLKN
RP48 EXT@0_4P2R_4 EXT
To NB A-Link CLK
(10) SB_PCIE_NB_CLKP
(10) SB_PCIE_NB_CLKN
RP76 *INT@0_4P2R_4 INT PCIE_RCLKP PCIE_RCLKN
For North Bridge
(10) SB_DISP_CLKP
(10) SB_DISP_CLKN
RP47 *INT@0_4P2R_4 NB_DISP_CLKP NB_DISP_CLKN
For North Bridge
(10) SB_NBHT_REFCLKP
(10) SB_NBHT_REFCLKN
RP75 *INT@0_4P2R_4 NB_HT_CLKP NB_HT_CLKN
100MHZ
For CPU Host Clk
SB_CPU_CLKIN_P SB_CPU_CLKIN_N
RP50 *INT@0_4P2R_4 CPU_HT_CLKP CPU_HT_CLKN
Close to SB
R196 *261/F_4
T47 T46 SLT_GFX_CLKP SLT_GFX_CLKN
To Marvell Lan
(3,24) PCIE_CLK_LAN
(3,24) PCIE_CLK_LAN#
RP46 *INT@0_4P2R_4 GPP_CLK0P GPP_CLK0N
To New Card
SB_GPP_CLK1P SB_GPP_CLK1N
RP51 *INT@0_4P2R_4 GPP_CLK1P GPP_CLK1N
(3,23) PCIE_CLK_MINI
(3,23) PCIE_CLK_MINI#
RP49 *INT@0_4P2R_4 GPP_CLK2P GPP_CLK2N
To Mini Card 1,2
SB_GPP_CLK3P SB_GPP_CLK3N
RP74 *INT@0_4P2R_4 GPP_CLK3P GPP_CLK3N
T48 25M_48M_66M_OSC
C266 *22P_4 SB700_25M_X1
Y4 *25MHZ
R207 *10M_6
C270 *22P_4 SB700_25M_X2
Install for Int Clk Gen
25M_X1 25M_X2
CLOCK GENERATOR
Rev:3B 04/02 As the same location Name(G1) For Toshiba Service Team Request.
RTC_X1 RTC_X2 X1 X2 RTC XTAL
+1.8VSUS +1.8V
R194 *10K_4
R193 *10K_4
(10) ALLOW_LDTSTOP
(6) CPU_PROCHOT#
(6) CPU_PWRGD
(6,10) CPU_LDT_STOP#
(6,10) CPU_LDT_RST#
ALLOW_LDTSTP PROCHOT# LDT_PG LDT_STP# LDT_RST#
CPU
Rev:3A 02/05 No-Stuff R194 For Leakage when system into G3 mode.
RTC_X1
Y8 32.768KHZ
RTC_X2
R454 *20M_6
R465 20M_6
C527 18P_4
C535 18P_4
+3VPCU D31 RB500
TERM13 D33 RB500
+3VRTC R364 510/F_6
VCCRTC
C443 1U/10V_4
G1 *SHORT_PAD1
R366 1K_4
Rev:3A 02/13 RTC Circuit R363/R360/R359/R361 Follow Standar Circuit Value.
+5VPCU
TERM12 TERM11 TERM15
R363 2K/F_4
R360 2K/F_4
Q57 MMBT3904
R359 6.8K/F_4
20MIL
TERM14
CN27
Rev:2A 12/07 Change Part Number.
R361 15K/F_6
ACS_85204-0200L
RTC
PCI CLKS
PCICLK0 PCICLK1 PCICLK2 PCICLK3 PCICLK4 PCICLK5/GPIO41
PCI_CLK0_R PCI_CLK1_R PCI_CLK2_R PCI_CLK3_R PCI_CLK4_R PCI_CLK5_R
R510 22_4 R509 CB@22_4 R493 22_4 R514 22_4 R498 22_4 R496 22_4
PCLK_OZ129 (22)
PCLK_PCM (21)
PCI_CLK2 (16)
PCI_CLK3 (16)
PCI_CLK4 (16)
PCI_CLK5 (16)
PCIRST# PCIRST#_SB700 R492 33_4 PCIRST# (21,22)
AD[0..31] AD[0..31] (16,21,22)
AD0 … AD31
+3V
REQ0# R424 *8.2K_4
REQ1# R422 *8.2K_4
GNT3# R474 8.2K_4
GNT3# R473 *8.2K_4
SB_GPIO65 R464 100K_4
PCI INTERFACE
CBE0# (21,22)
CBE1# (21,22)
CBE2# (21,22)
CBE3# (21,22)
FRAME# (21,22)
DEVSEL# (21,22)
IRDY# (21,22)
TRDY# (21,22)
PAR (21,22)
STOP# (21,22)
PERR# (21)
SERR# (21)
REQ0# (22)
REQ1# (21)
T115
PORT_C# (26)
T124
GNT0# (22)
GNT1# (21)
T118
Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).
T117
CLKRUN#_R R470 0_4 CLKRUN# (22,28)
Rev:3C 05/09 Remove Test Ports For Space Limiting.
INTE# (22)
INTF# (21)
R241 FM@0_4 FM_INT (24)
R124 *GS@0_4 HDPINT (19)
LPCCLK0 LPCCLK1 R412 22_4 R411 22_4
PCLK_591 (16,28)
PCLK_DEBUG (16,23)
LAD0 (23,28)
LAD1 (23,28)
LAD2 (23,28)
LAD3 (23,28)
LFRAME# (23,28)
LDRQ#0 (23)
LDRQ1#_SB T51
SB_GPIO65 T113
SERIRQ SERIRQ (21,23,28)
LPC
RTCCLK RTC_CLK (16)
INTRUDER_ALERT# T119
VBAT VCCRTC
20MIL
C537 1u/10V_4
C541 0.1u/10V_4
SB700
PROJECT : BU2
Quanta Computer Inc.
NB4
Size Custom
Document Number SB700-PCIE/PCI/CPU/LPC 1/4
Rev 1A
Date: Thursday, July 24, 2008 Sheet 12 of 35

SB700

EMI



Rev:3C 04/08 Reserve the 0hm to USB7 Controller.

Rev:3A 03/03 Swap USB CONN From USB11 to USB7 For Controller ESATA Certification.

Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers.

Rev:2A 12/06 Support the New Card Hot Plug Function.

Rev:3B 04/07 USB Overcurrent 5 Pull-up 10K For Open Drain.

Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).

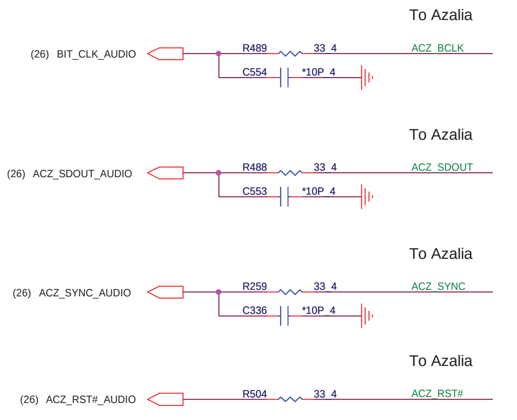
Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.

Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.

Rev:3A 02/05 Move Hot Plug Pin Name From GEVENT5# to GPM1.

Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K.

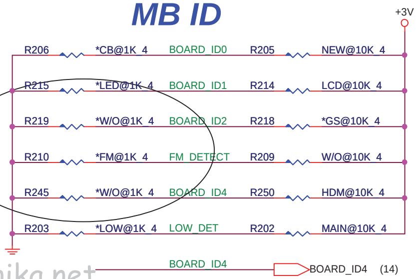
HD Audio Interface



MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H L					
W/ CCFL Panel W/ LED Panel		H L				
W/ G-Sensor W/O G-Sensor			H L			
W/O FM W/FM				H L		
W/ HDMI W/O HDMI					H L	
Main Strem Low Cost						H L

MB ID



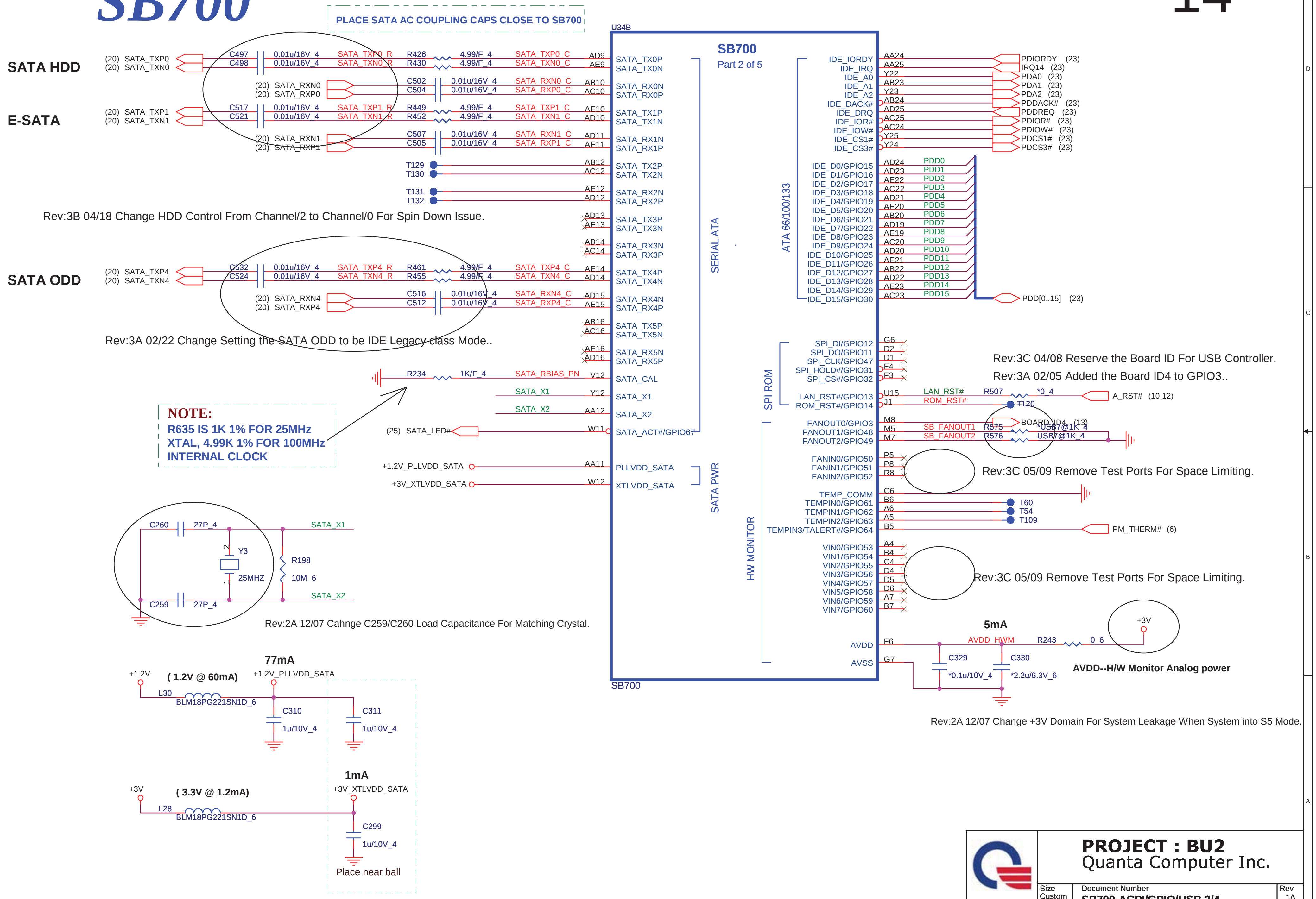
PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

Date: Thursday, July 24, 2008 Sheet 13 of 35

SB700



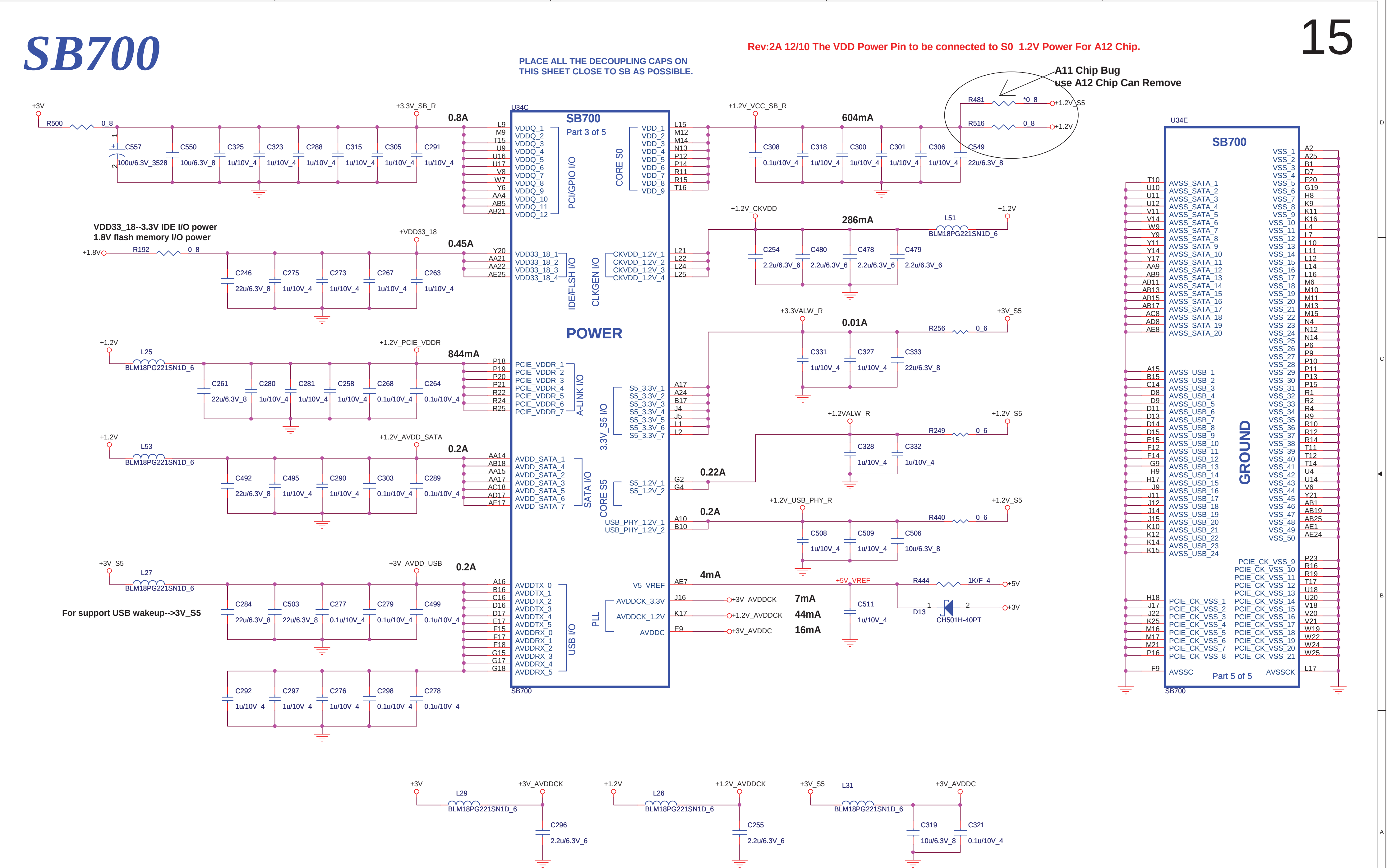
PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	1A

Date: Thursday, July 24, 2008 | Sheet 14 of 35

SB700



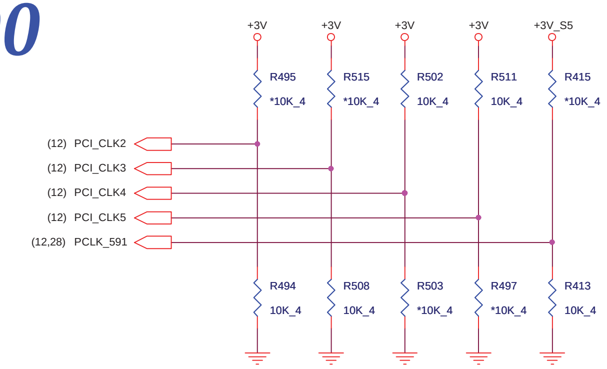
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-PWR/DECOUPLING 4/4	1A

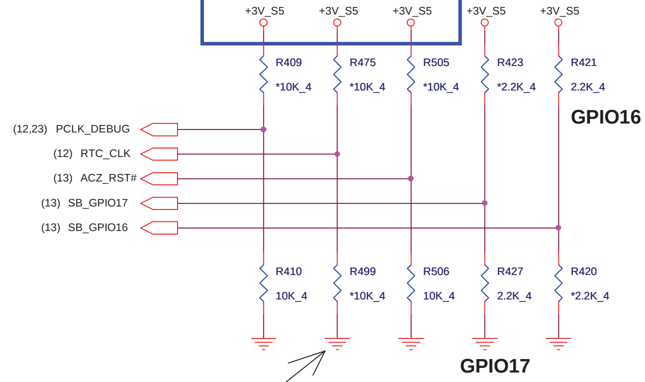
NB4

Date: Friday, May 09, 2008 Sheet 15 of 35

SB700



It must ready refore RSMRST#



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

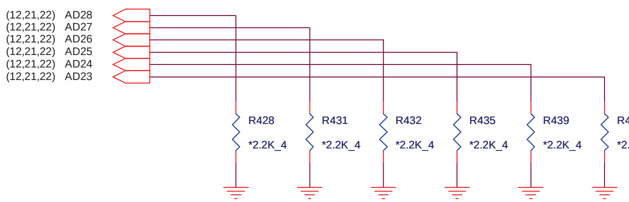
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT

	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



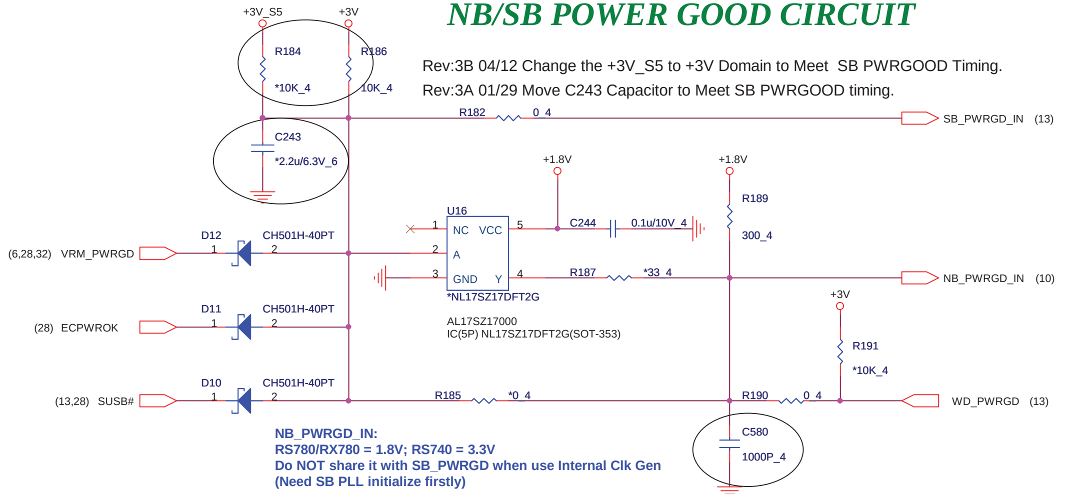
Use 2.2K PD.

REQUIRED STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB/SB POWER GOOD CIRCUIT

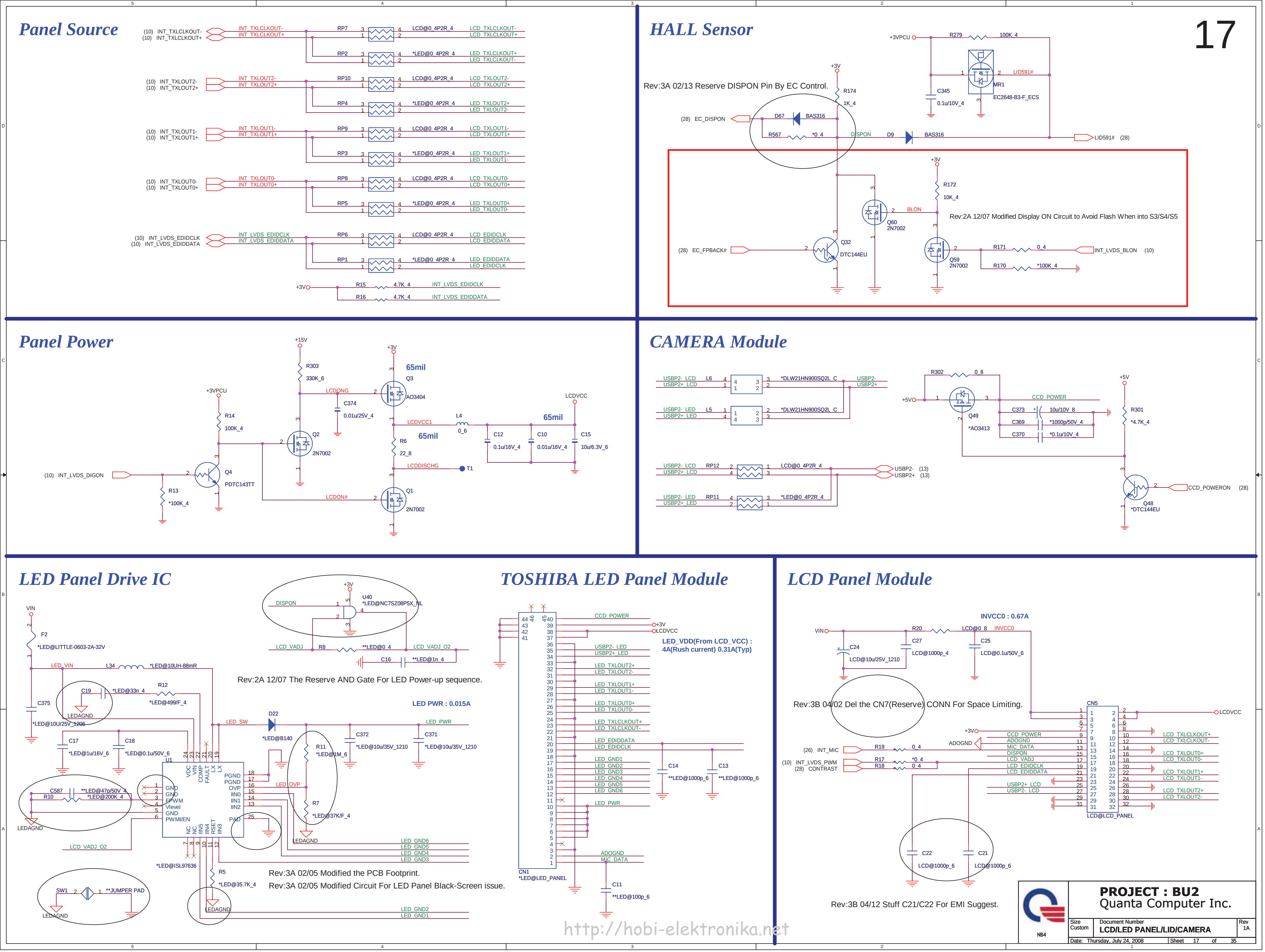
Rev:3B 04/12 Change the +3V_S5 to +3V Domain to Meet SB PWRGOOD Timing.
Rev:3A 01/29 Move C243 Capacitor to Meet SB PWRGOOD timing.

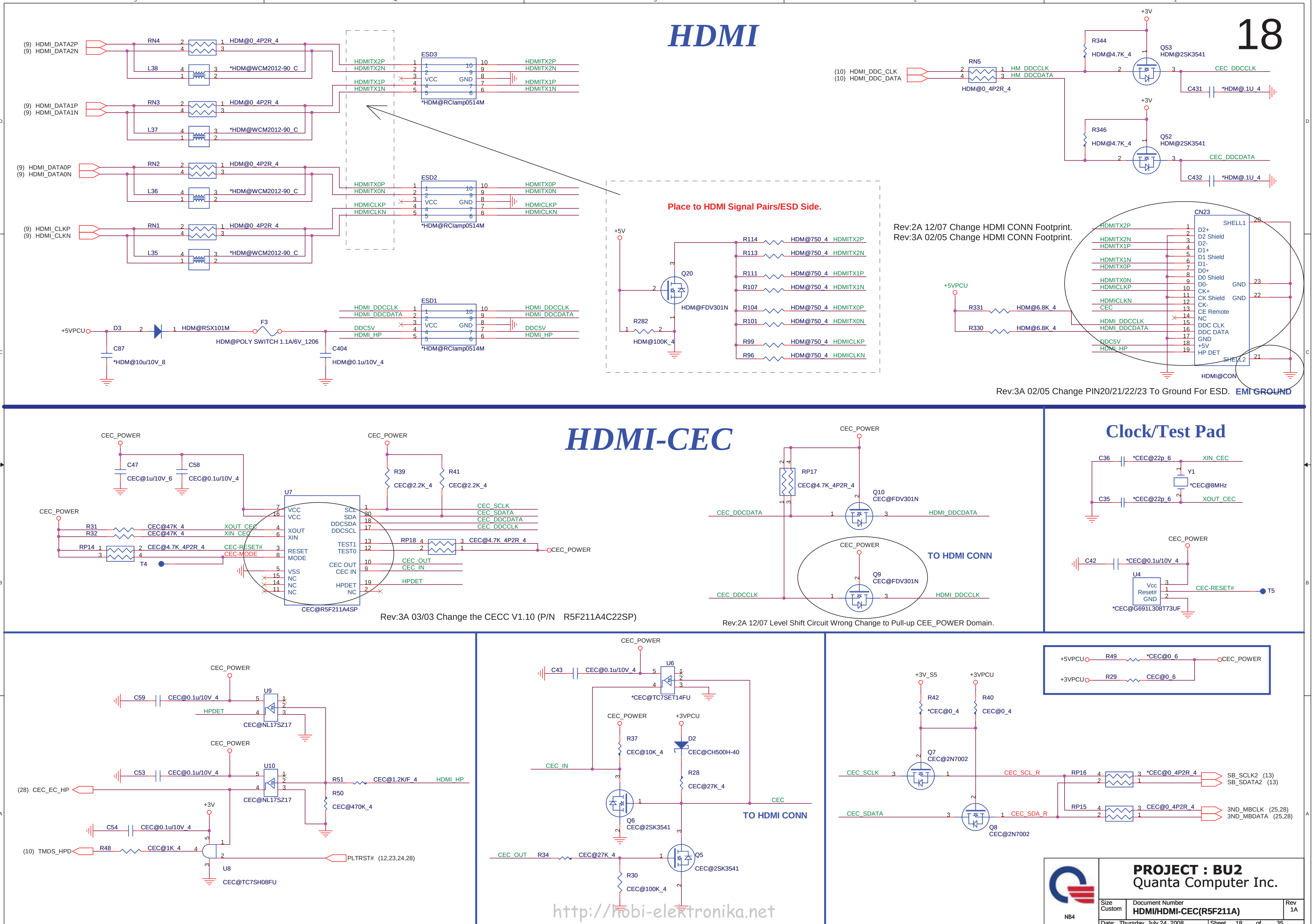


NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

Rev:2A 12/07 Add 1N Capacitor to Smoothing NB_PWRGD_IN.

PROJECT : BU2	Quanta Computer Inc.
Size: Custom	Document Number: SB700-STRAPS & PWRGD
Rev: 1A	Date: Thursday, July 24, 2008
Sheet 16 of 35	NB4


Panel Source
HALL Sensor
Rev:3A 02/13 Reserve DISPON Pin By EC Control.
Rev:2A 12/07 Modified Display ON Circuit to Avoid Flash When into S3/S4/S5
Panel Power
65mil
CAMERA Module
LED Panel Drive IC
Rev:2A 12/07 The Reserve AND Gate For LED Power-up sequence.
LED PWR : 0.015A
Rev:3A 02/05 Modified the PCB Footprint.
Rev:3A 02/05 Modified Circuit For LED Panel Black-Screen issue.
TOSHIBA LED Panel Module
LED_VDD(From LCD_VCC) :
4A(Rush current) 0.31A(Typ)
LCD Panel Module
INVCC0 : 0.67A
Rev:3B 04/02 Del the CN7(Reserve) CONN For Space Limiting.
Rev:3B 04/12 Stuff C21/C22 For EMI Suggest.
PROJECT : BU2
Quanta Computer Inc.
Size Custom
Document Number
LCD/LED PANEL/LID/CAMERA
Rev 1A
Date: Thursday, July 24, 2008
Sheet 17 of 35
NB4
http://hobi-elektronika.net



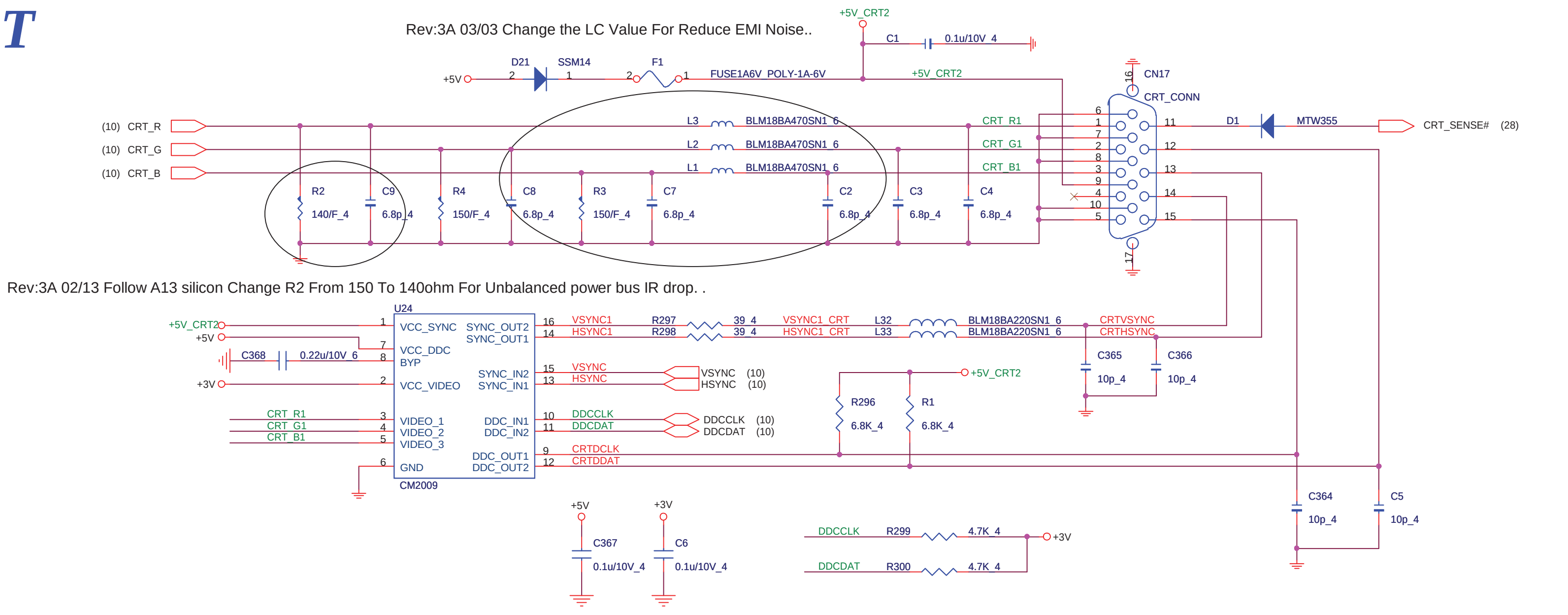
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI/HDMI-CEC(R5F211A)	1A

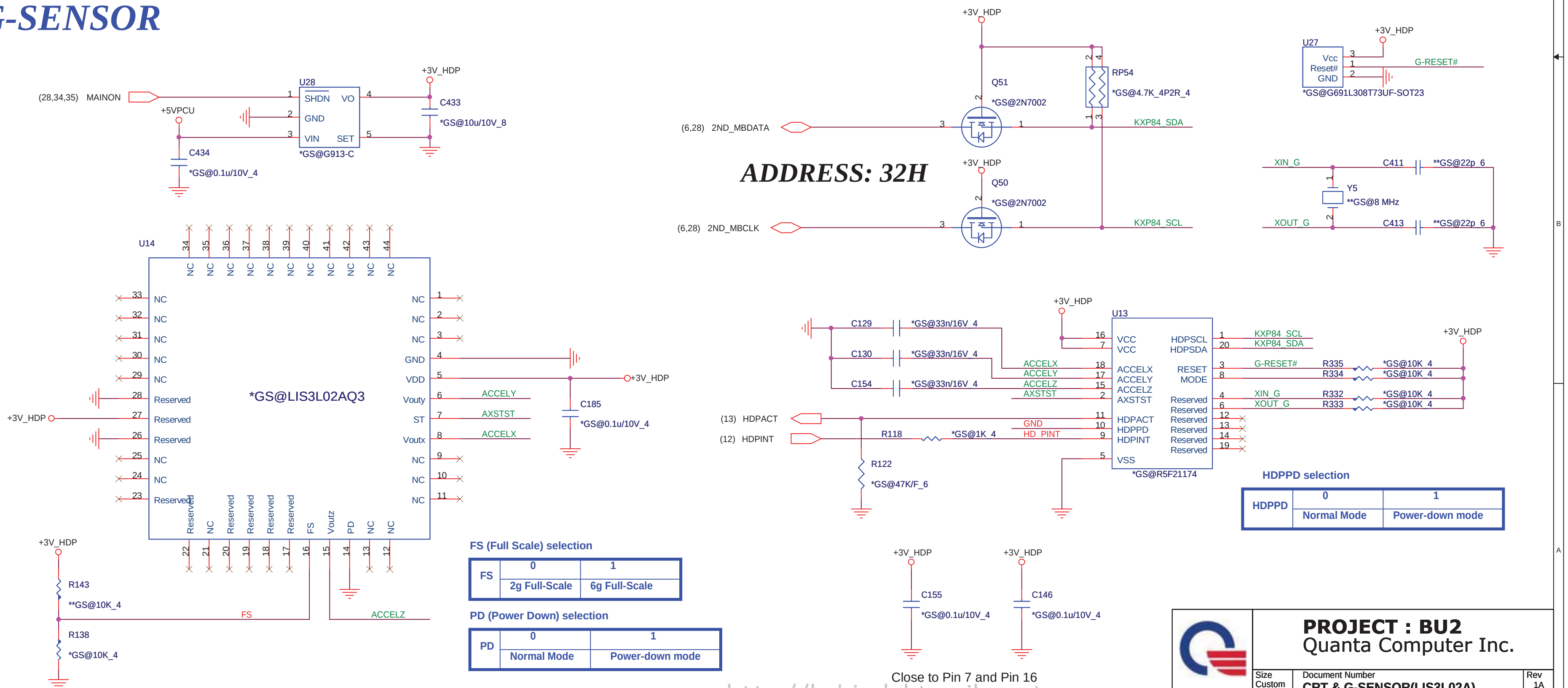
Date: Thursday, July 24, 2008 Sheet 18 of 35

NB4

CRT



G-SENSOR



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

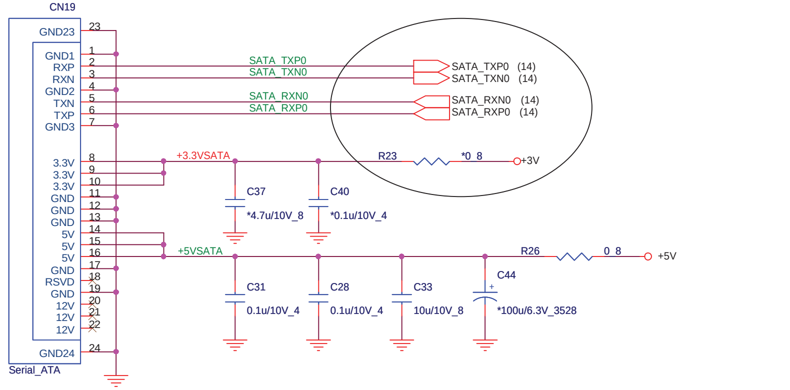
NB4

PROJECT : BU2
Quanta Computer Inc.

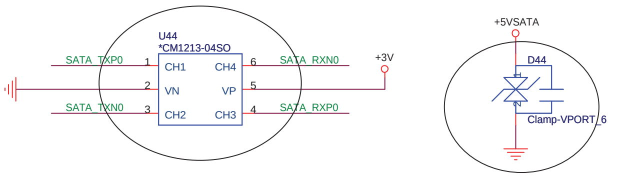
Size	Document Number	Rev
Custom	CRT & G-SENSOR(LIS3L02A)	1A

Date: Thursday, July 24, 2008 | Sheet 19 of 35

SATA HDD



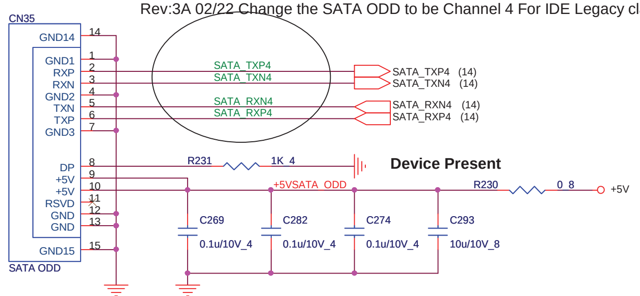
Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

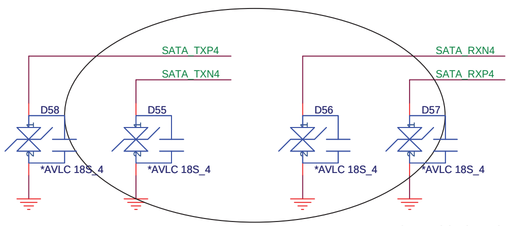


Rev:3B 04/18 Remove D51/D52/D53/D54 Varistor And Change to U44 CM1213-04SO ESD Protection Arrays.

SATA ODD

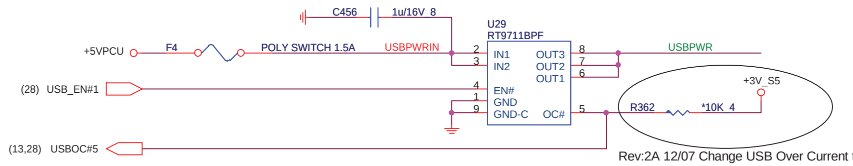
Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode..





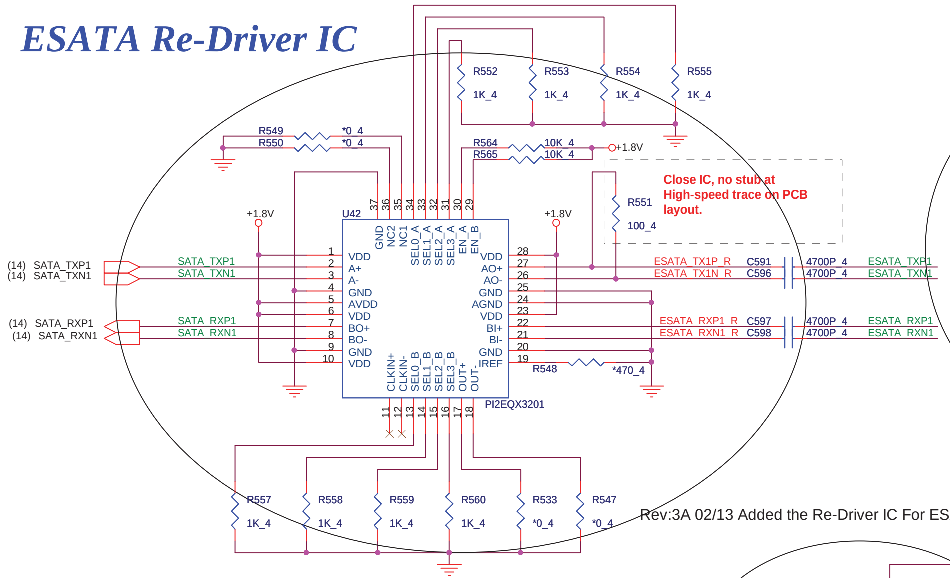
Rev:3A 01/29 Added Varistor ESD Solution.

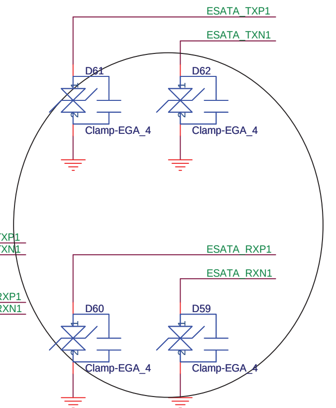
USB & ESATA



Rev:2A 12/07 Change USB Over Current to +3V_S5 Domain.

ESATA Re-Driver IC

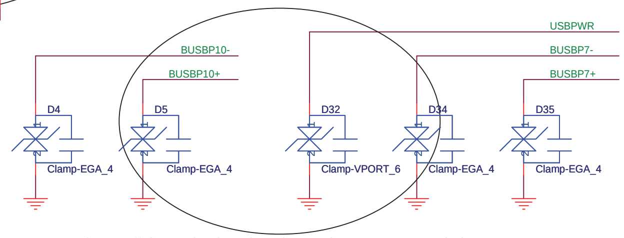




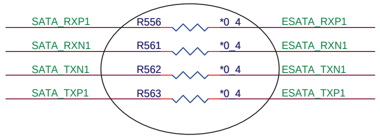
Rev:3A 01/29 Added Varistor ESD Solution.

Rev:3A 02/13 Added the Re-Driver IC For ESATA.

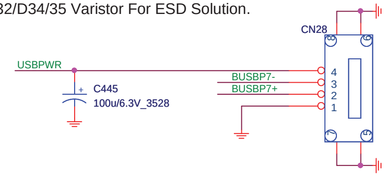
SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				



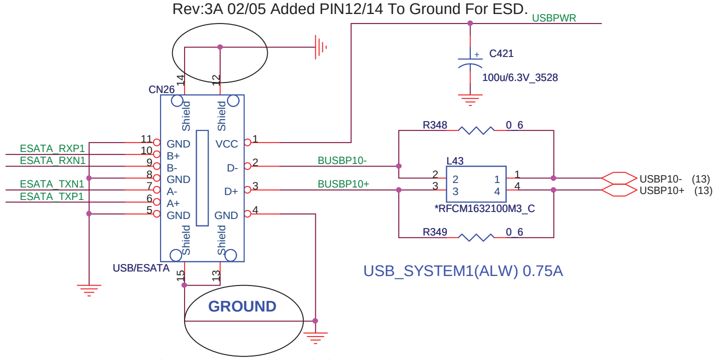
Rev:3A 03/03 Stuff the D4/D5/D32/D34/35 Varistor For ESD Solution.



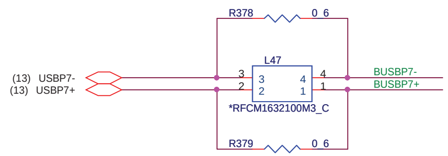
Rev:3A 02/05 Added PIN12/14 To Ground For ESD.



USB_SYSTEM2(ALW) 0.75A



USB_SYSTEM1(ALW) 0.75A



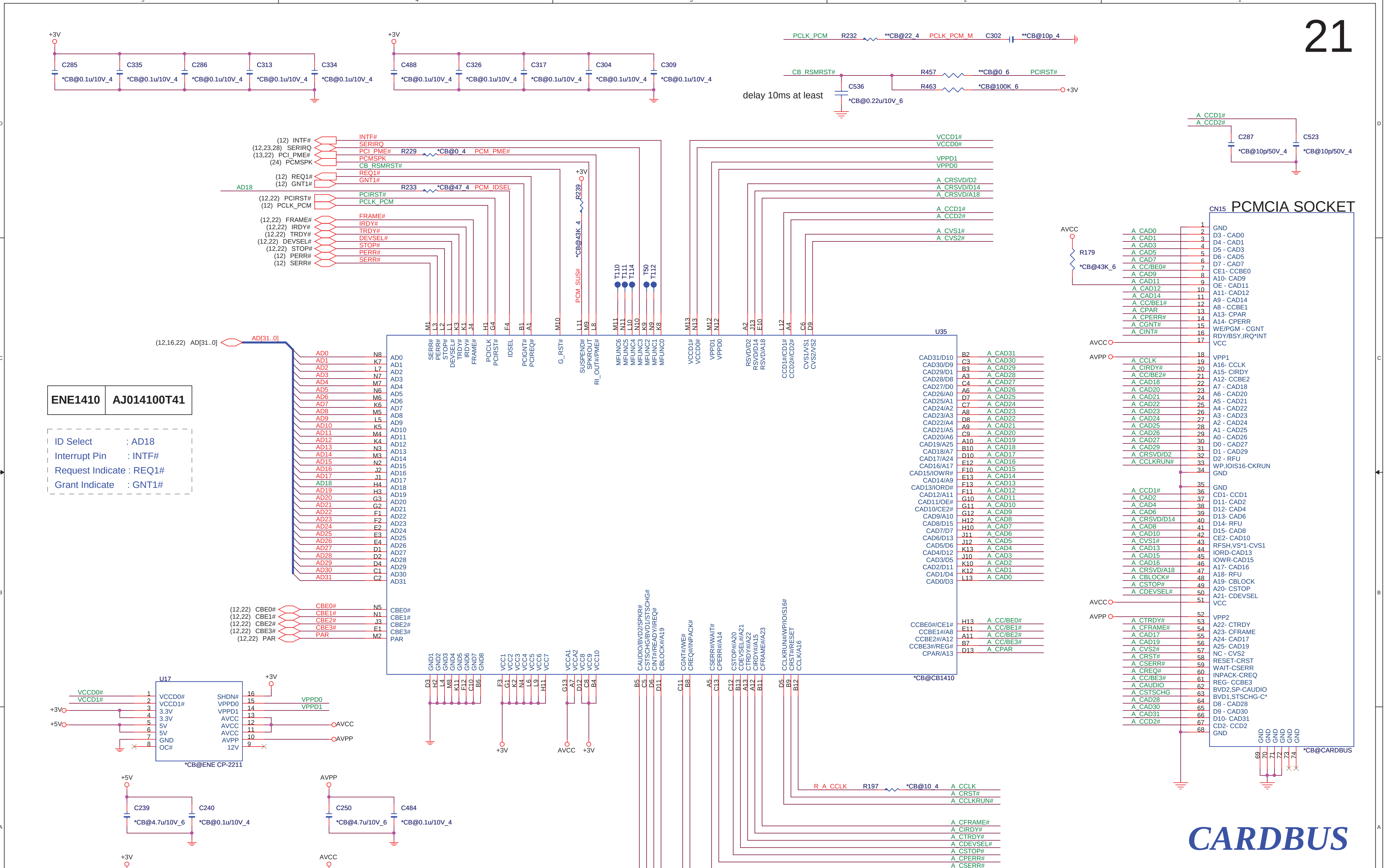
Rev:3A 01/29 Delete R133 For ESD Solution.

PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	SATA HDD/ODD & ESATA/USB	1A

Date: Tuesday, August 19, 2008 Sheet 20 of 35



ENE1410	AJ014100T41

ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ1#
Grant Indicate : GNT1#

PROJECT : BU2
Quanta Computer Inc.

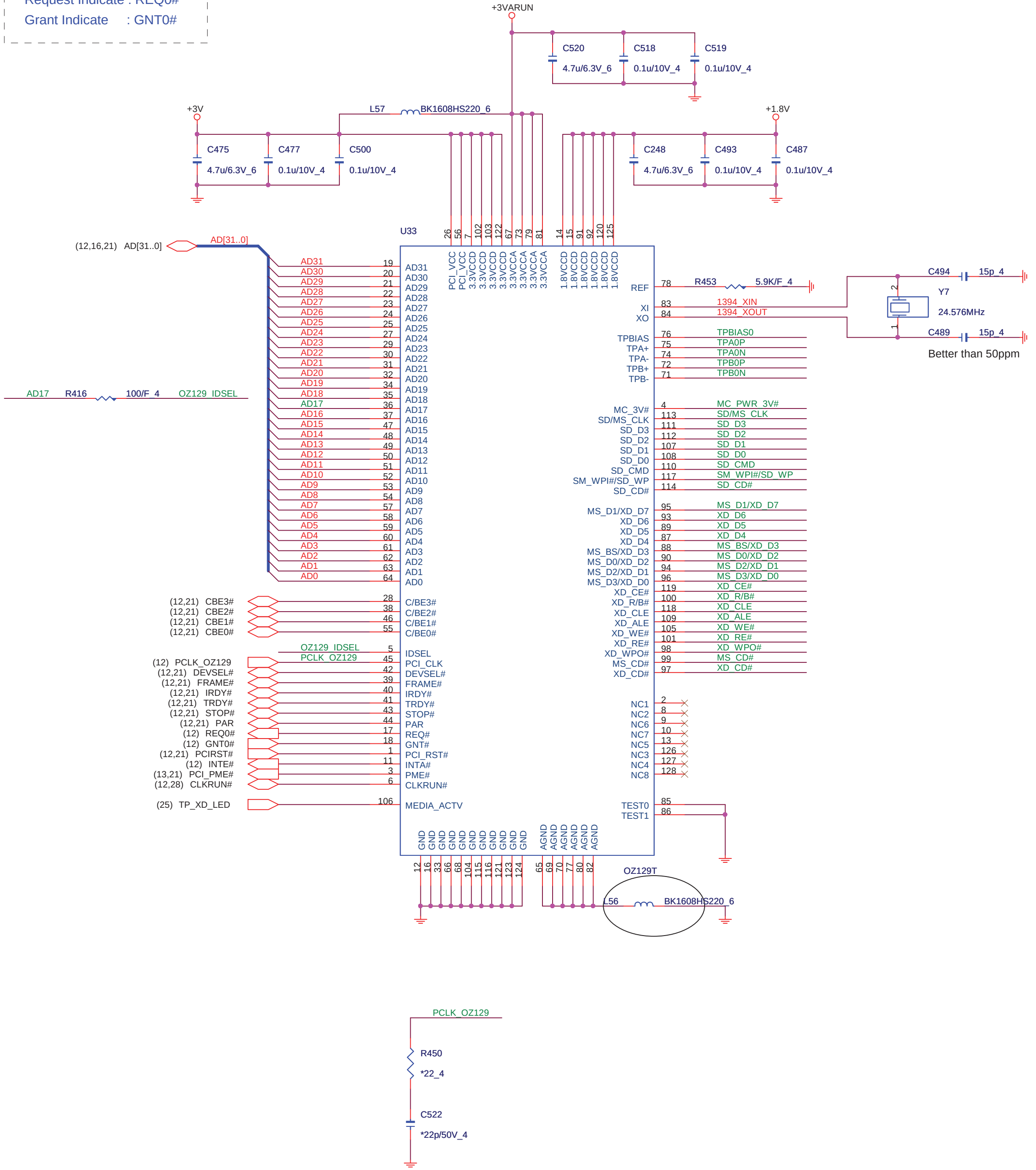
NB4

Size	Document Number	Rev
Custom	PCMCIA(CB1410) -OPTION	1A

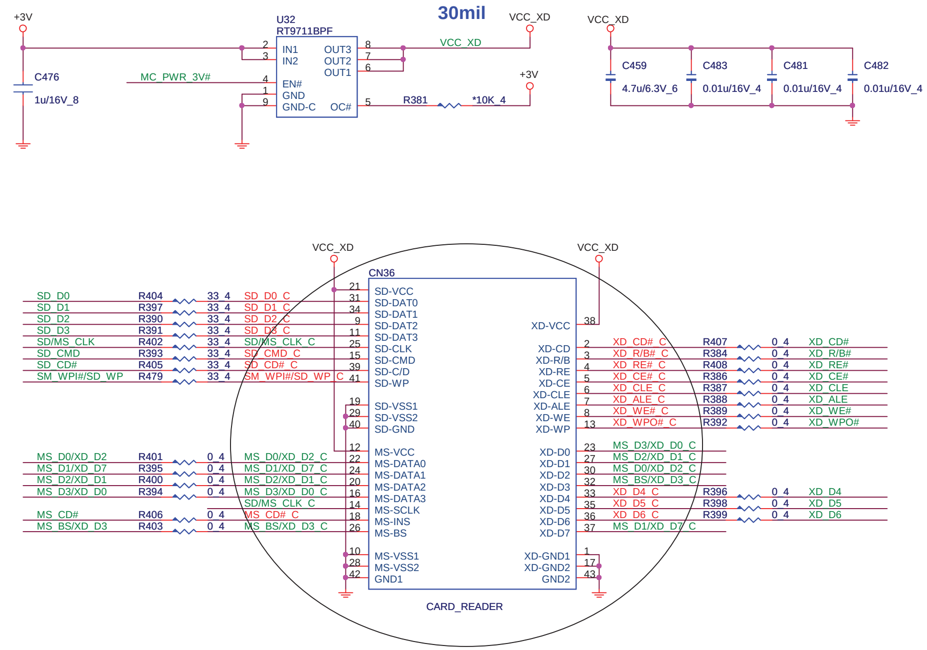
Date: Thursday, July 24, 2008 Sheet 21 of 35

OZ129 CardReader/1394

ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ0#
Grant Indicate : GNT0#

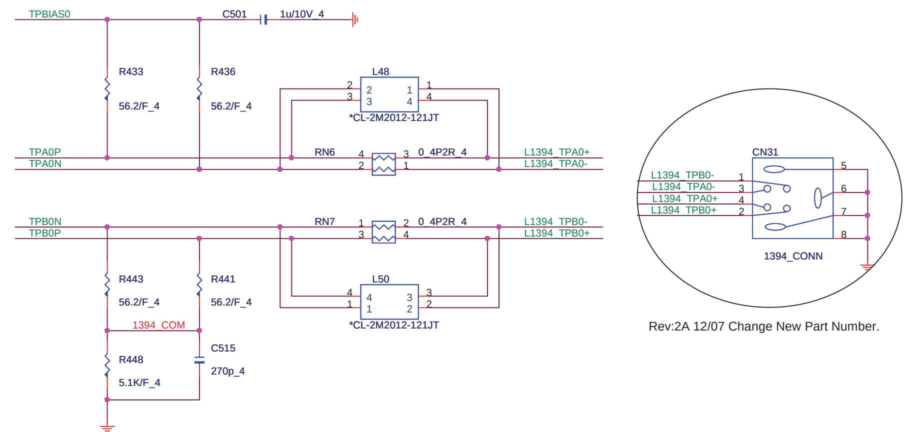


5 IN 1 Card Reader



Rev:2A 12/07 Modified the CN36 Footprint For Open Issue.

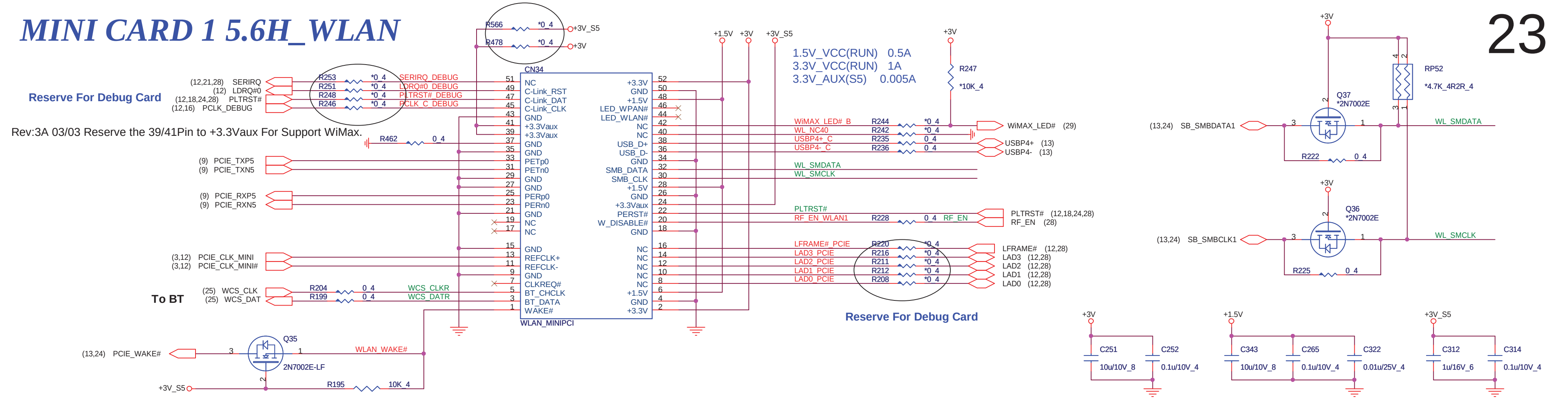
1394



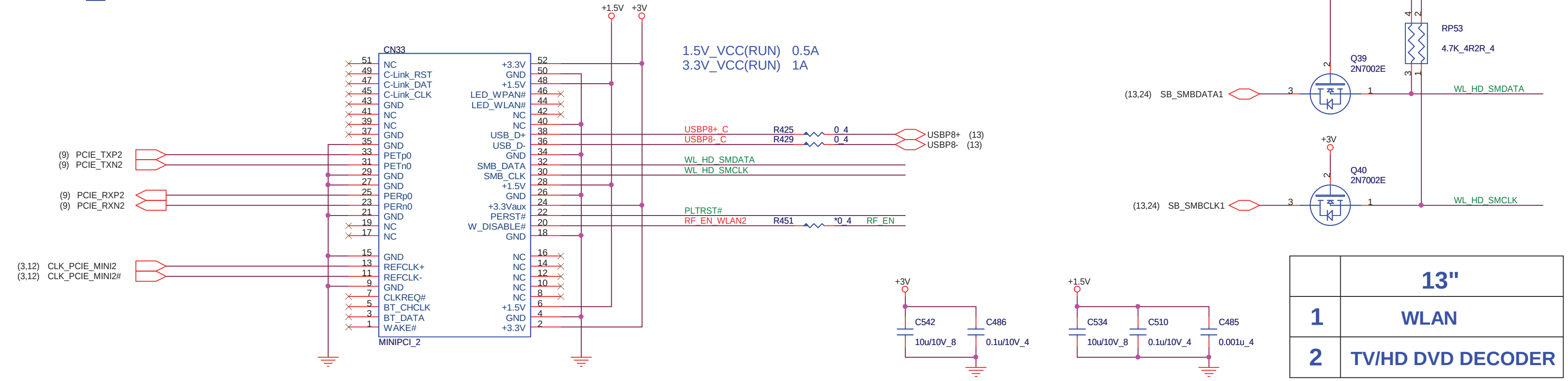
Rev:2A 12/07 Change New Part Number.

PROJECT : BU2
Quanta Computer Inc.
NB4
Size: Custom
Document Number: OZ129T(5IN1/1394)
Rev: 1A
Date: Thursday, July 24, 2008
Sheet 22 of 35

MINI CARD 1 5.6H_WLAN

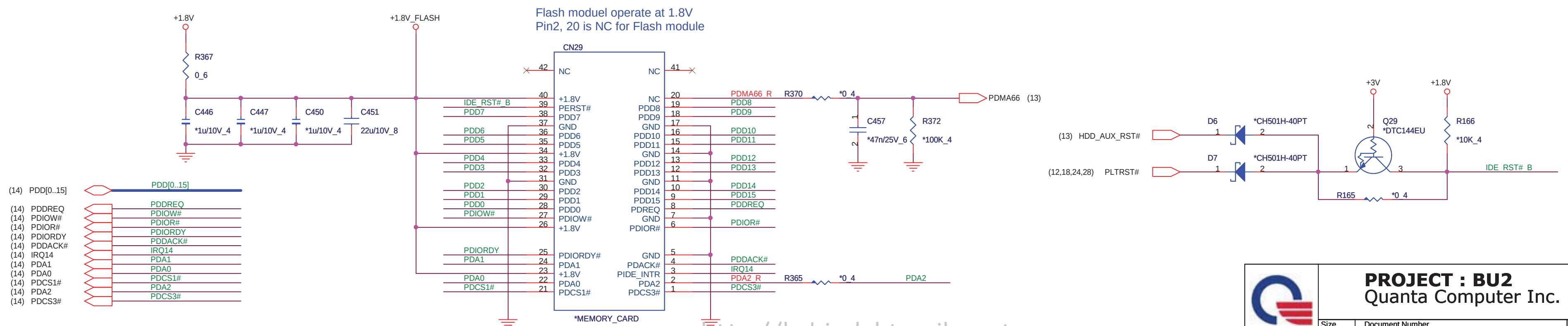


MINI Card 2 5.6H_TV/HD DVD DECODER



	13"
1	WLAN
2	TV/HD DVD DECODER

NAND FLASH MEMORY CARD



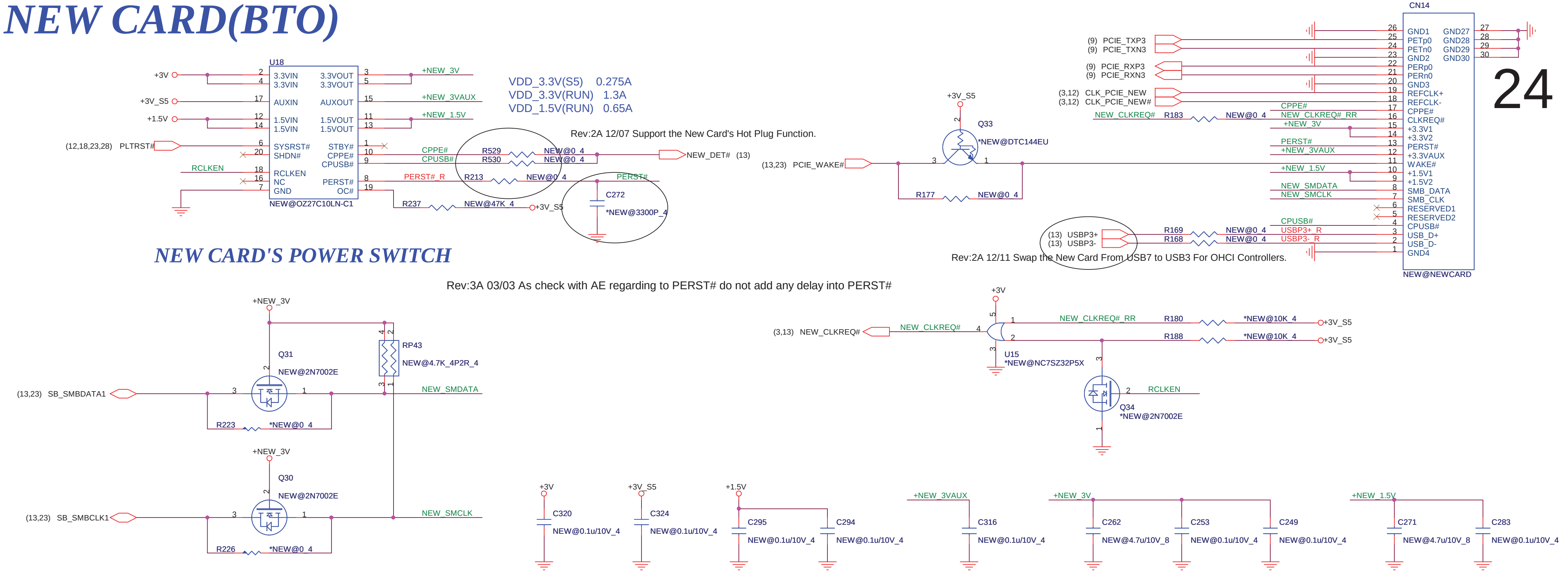
PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	MINI CARD & NAND FLASH CARD	1A

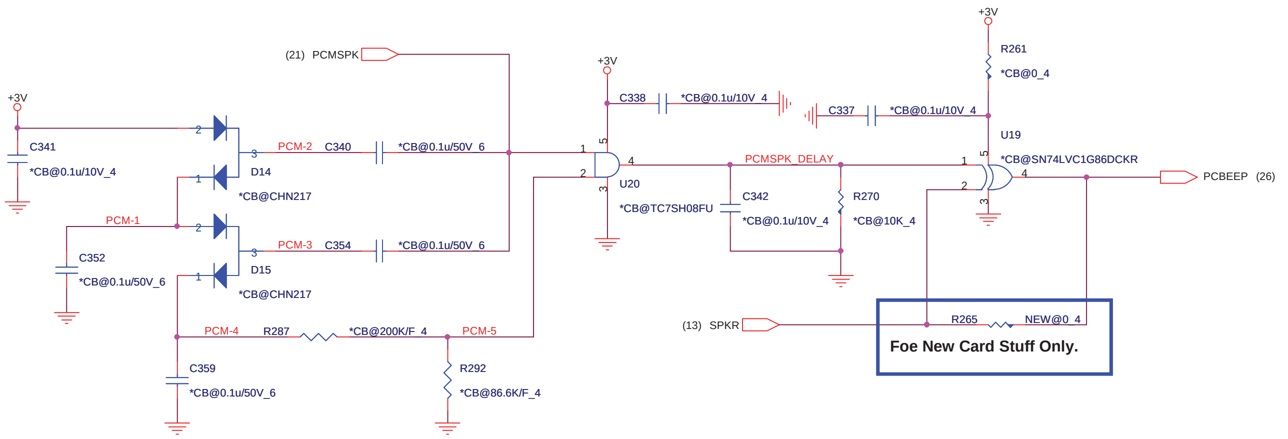
Date: Thursday, July 24, 2008 Sheet 23 of 35

NEW CARD(BTO)



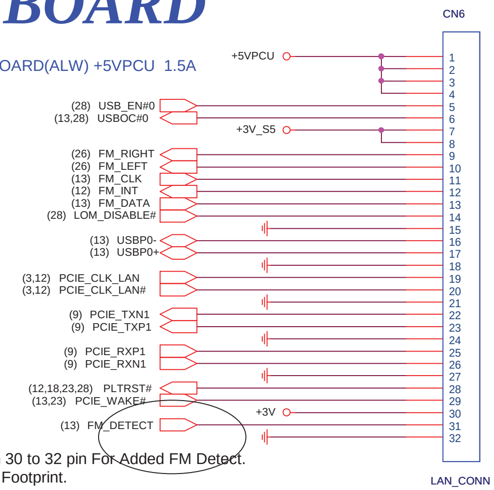
NEW CARD'S POWER SWITCH

PC-BEEP



RJ45/USB BOARD

USB & LAN BOARD(ALW) +5VPCU 1.5A



Rev:2A 12/07 Change Connector From 30 to 32 pin For Added FM Detect.
Rev:3A 02/05 Change Connector PCB Footprint.

PROJECT : BU2
Quanta Computer Inc.

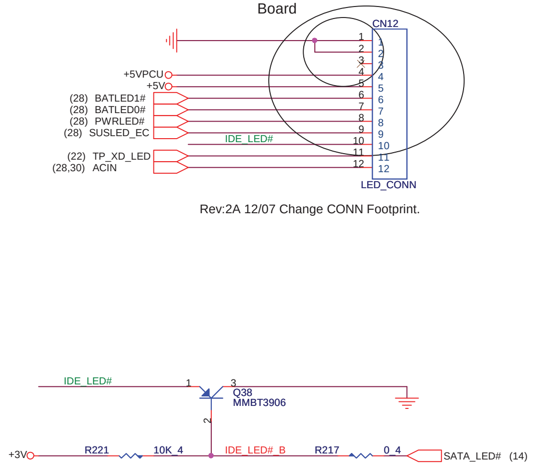
NB4

Size	Document Number	Rev
Custom	NEW CARD & RJ45 BOARD/BEEP	1A

Date: Thursday, July 24, 2008 Sheet 24 of 35

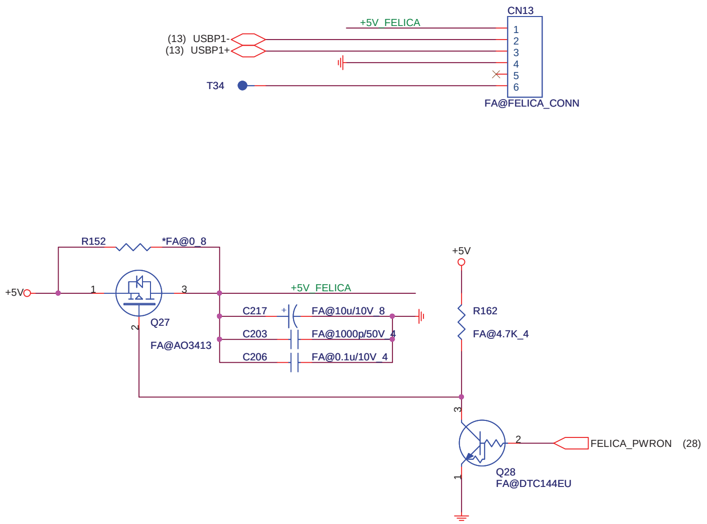
LED BOARD

Rev:3A 02/05 NC PIN3 To Follow LED Board



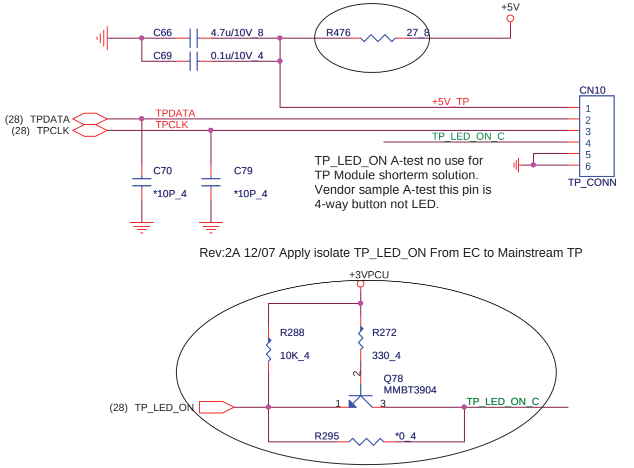
Rev:2A 12/07 Change CONN Footprint.

Felica



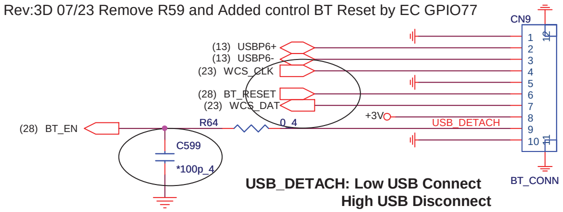
TP BOARD

Rev:3C 12/07 Change R476 Resistor PCB Footprint From 0605 to 0805.



Bluetooth Module

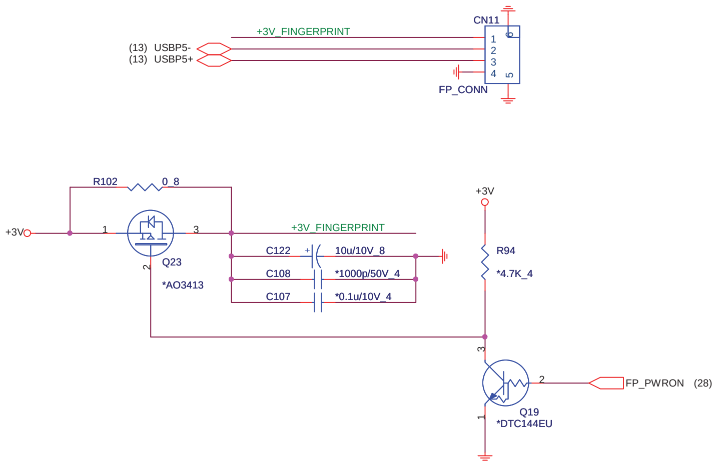
Rev:3D 07/23 Remove R59 and Added control BT Reset by EC GPIO77



USB_DETACH: Low USB Connect
High USB Disconnect

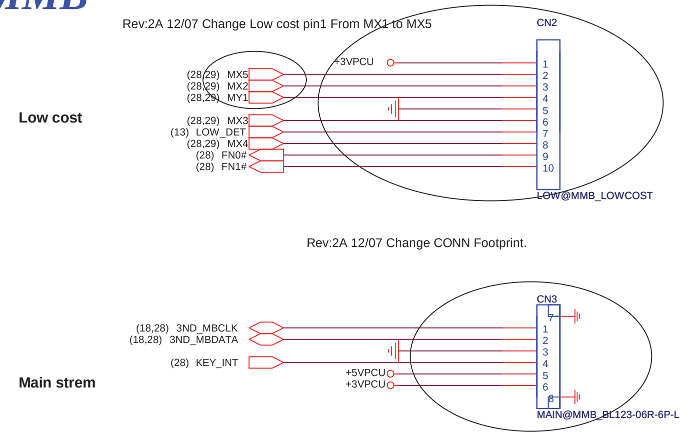
Rev:3A 03/03 Reserve C599 Capacitors to Bluetooth Enable For EMI..

FINGER-PRINT

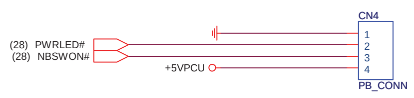


MMB

Rev:2A 12/07 Change Low cost pin1 From MX1 to MX5



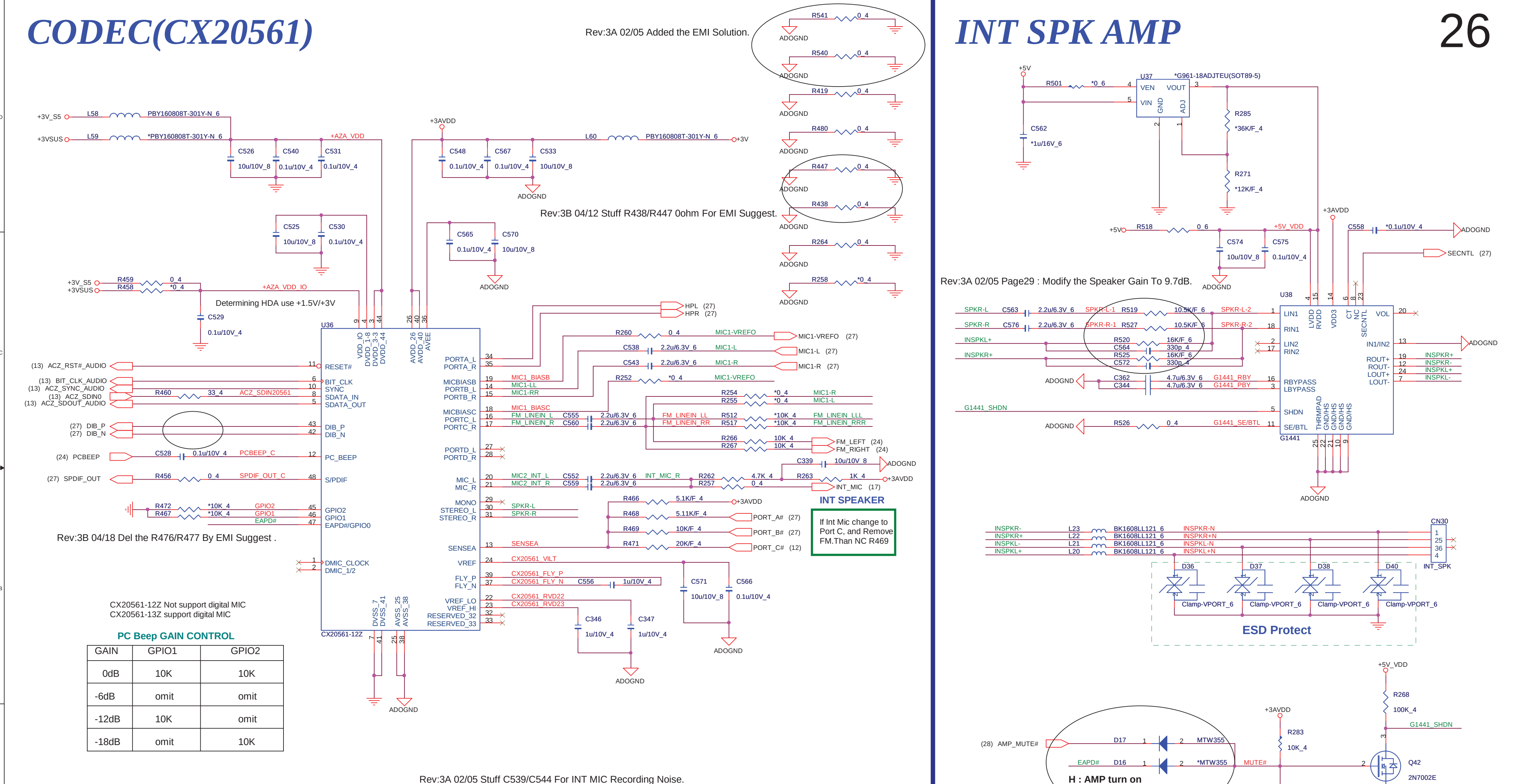
POWER BOARD



NB4	**PROJECT : BU2** Quanta Computer Inc.	
Size: Custom	Document Number: TP/FP/BT/PB/FELICA/MMB CONN	Rev: 1A
Date: Tuesday, August 19, 2008	Sheet 25 of 35	

CODEC(CX20561)

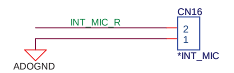
INT SPK AMP



PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

Reserve INTMIC

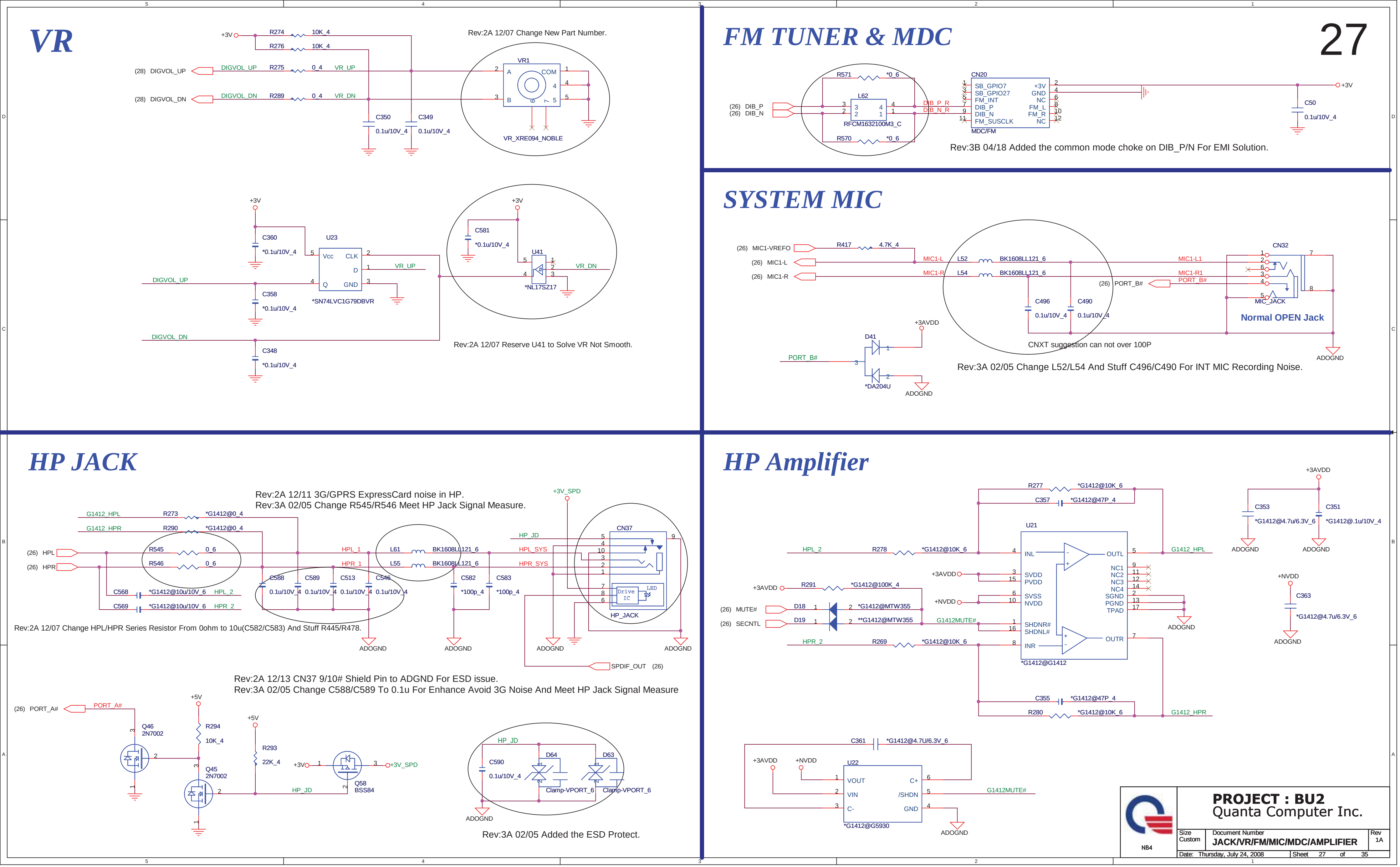


Reserve FM

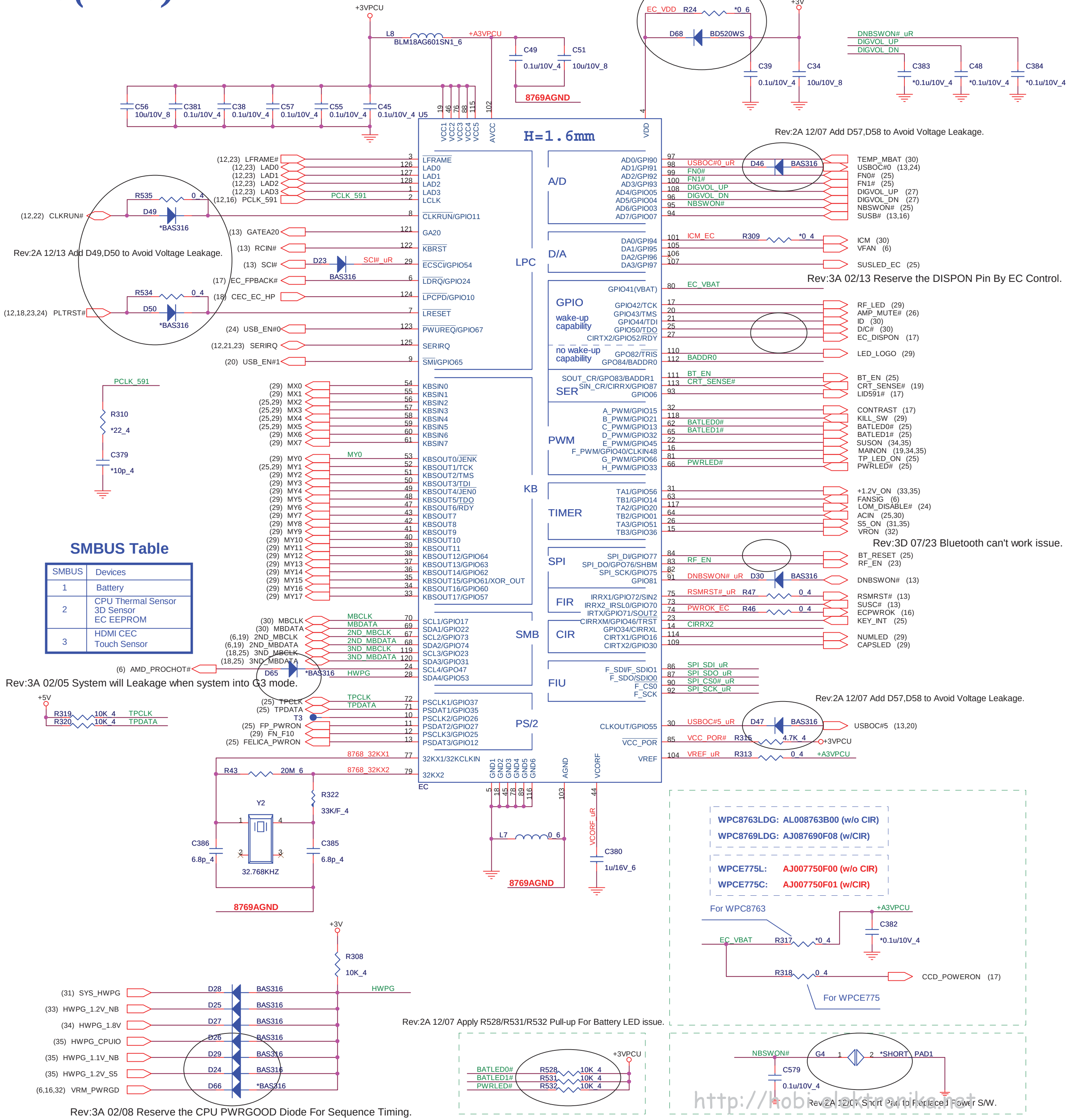
PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CONEXANT(CX205601)/SPK/AMP	1A

Date: Thursday, July 24, 2008 Sheet 26 of 35


27
VR
Rev:2A 12/07 Change New Part Number.
+3V
R274 10K_4
R276 10K_4
(28) DIGVOL_UP
DIGVOL_UP
R275 0_4 VR_UP
(28) DIGVOL_DN
DIGVOL_DN
R289 0_4 VR_DN
C350 0.1u/10V_4
C349 0.1u/10V_4
VR1
COM
VR_XRE094_NOBLE
C360 *0.1u/10V_4
U23
Vcc CLK D Q GND
*SN74LVC1G79DBVR
C358 *0.1u/10V_4
C348 *0.1u/10V_4
C581 *0.1u/10V_4
U41
*NL17SZ17
Rev:2A 12/07 Reserve U41 to Solve VR Not Smooth.
FM TUNER & MDC
R571 *0_6
L62
RFCM1632100M3_C
R570 *0_6
(26) DIB_P
(26) DIB_N
DIB_P_R
DIB_N_R
CN20
SB_GPIO7 SB_GPIO27 FM_INT DIB_P DIB_N FM_SUSCLK
+3V GND NC NC FM_L FM_R NC
MDC/FM
C50 0.1u/10V_4
Rev:3B 04/18 Added the common mode choke on DIB_P/N For EMI Solution.
SYSTEM MIC
(26) MIC1-VREFO
R417 4.7K_4
(26) MIC1-L
(26) MIC1-R
L52 BK1608LL121_6
L54 BK1608LL121_6
MIC1-L1
MIC1-R1
(26) PORT_B#
CN32
MIC_JACK
Normal OPEN Jack
C496 0.1u/10V_4
C490 0.1u/10V_4
CNXT suggestion can not over 100P
+3AVDD
D41
*DA204U
PORT_B#
ADOGND
Rev:3A 02/05 Change L52/L54 And Stuff C496/C490 For INT MIC Recording Noise.
HP JACK
Rev:2A 12/11 3G/GPRS ExpressCard noise in HP.
Rev:3A 02/05 Change R545/R546 Meet HP Jack Signal Measure.
G1412_HPL R273 *G1412@0_4
G1412_HPR R290 *G1412@0_4
(26) HPL
(26) HPR
R545 0_6
R546 0_6
HPL_1 L61 BK1608LL121_6 HPL_SYS
HPR_1 L55 BK1608LL121_6 HPR_SYS
C568 *G1412@10u/10V_6 HPL_2
C569 *G1412@10u/10V_6 HPR_2
C588 C589 C513 C546
0.1u/10V_4
C582 *100p_4
C583 *100p_4
+3V_SPD
HP_JD
CN37
Drive IC
LED
HP_JACK
ADOGND
SPDIF_OUT (26)
Rev:2A 12/07 Change HPL/HPR Series Resistor From 0ohm to 10u(C582/C583) And Stuff R445/R478.
Rev:2A 12/13 CN37 9/10# Shield Pin to ADGND For ESD issue.
Rev:3A 02/05 Change C588/C589 To 0.1u For Enhance Avoid 3G Noise And Meet HP Jack Signal Measure
(26) PORT_A# PORT_A#
Q46 2N7002
+5V
R294 10K_4
Q45 2N7002
R293 22K_4
+3V
Q58 BSS84
+3V_SPD
HP_JD
C590 0.1u/10V_4
D64 Clamp-VPORT_6
D63 Clamp-VPORT_6
Rev:3A 02/05 Added the ESD Protect.
HP Amplifier
R277 *G1412@10K_6
C357 *G1412@47P_4
U21
HPL_2 R278 *G1412@10K_6
INL OUTL
G1412_HPL
+3AVDD
SVDD PVDD
NC1 NC2 NC3 NC4 SGND PGND TPAD
R291 *G1412@100K_4
+NVDD
SVSS NVDD
(26) MUTE# D18 *G1412@MTW355
(26) SECNTL D19 **G1412@MTW355
G1412MUTE#
SHDNR# SHDNL#
HPR_2 R269 *G1412@10K_6
INR OUTR
*G1412@G1412
C355 *G1412@47P_4
R280 *G1412@10K_6
G1412_HPR
C353 *G1412@4.7u/6.3V_6
C351 *G1412@.1u/10V_4
C363 *G1412@4.7u/6.3V_6
C361 *G1412@4.7U/6.3V_6
U22
VOUT VIN C- C+ /SHDN GND
*G1412@G5930
G1412MUTE#
PROJECT : BU2
Quanta Computer Inc.
NB4
Size Custom
Document Number JACK/VR/FM/MIC/MDC/AMPLIFIER
Rev 1A
Date: Thursday, July 24, 2008 Sheet 27 of 35

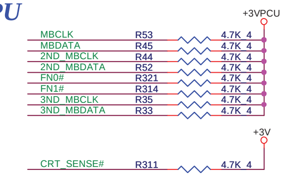
EC(KBC)



SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	HDMI CEC Touch Sensor

SM BUS PU

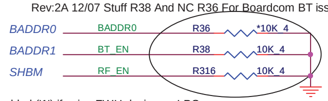


I/O Base Address

BADDR1-0	I/O Address: Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

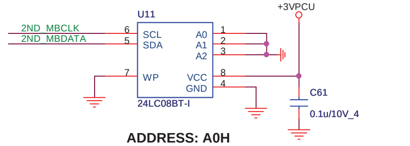
SHBM=0: Enable shared memory with host BIOS

Rev:2A 12/07 Stuff R38 And NC R36 For Boardcom BT issue.



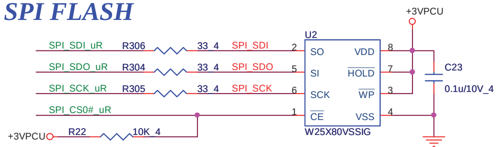
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID



ADDRESS: A0H

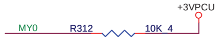
SPI FLASH



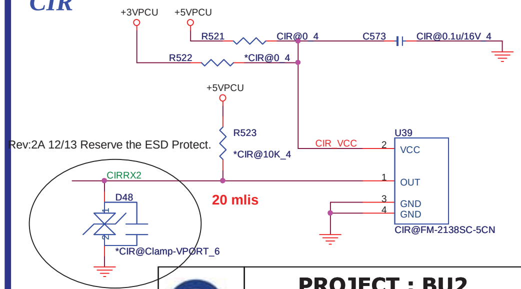
2nd sorce

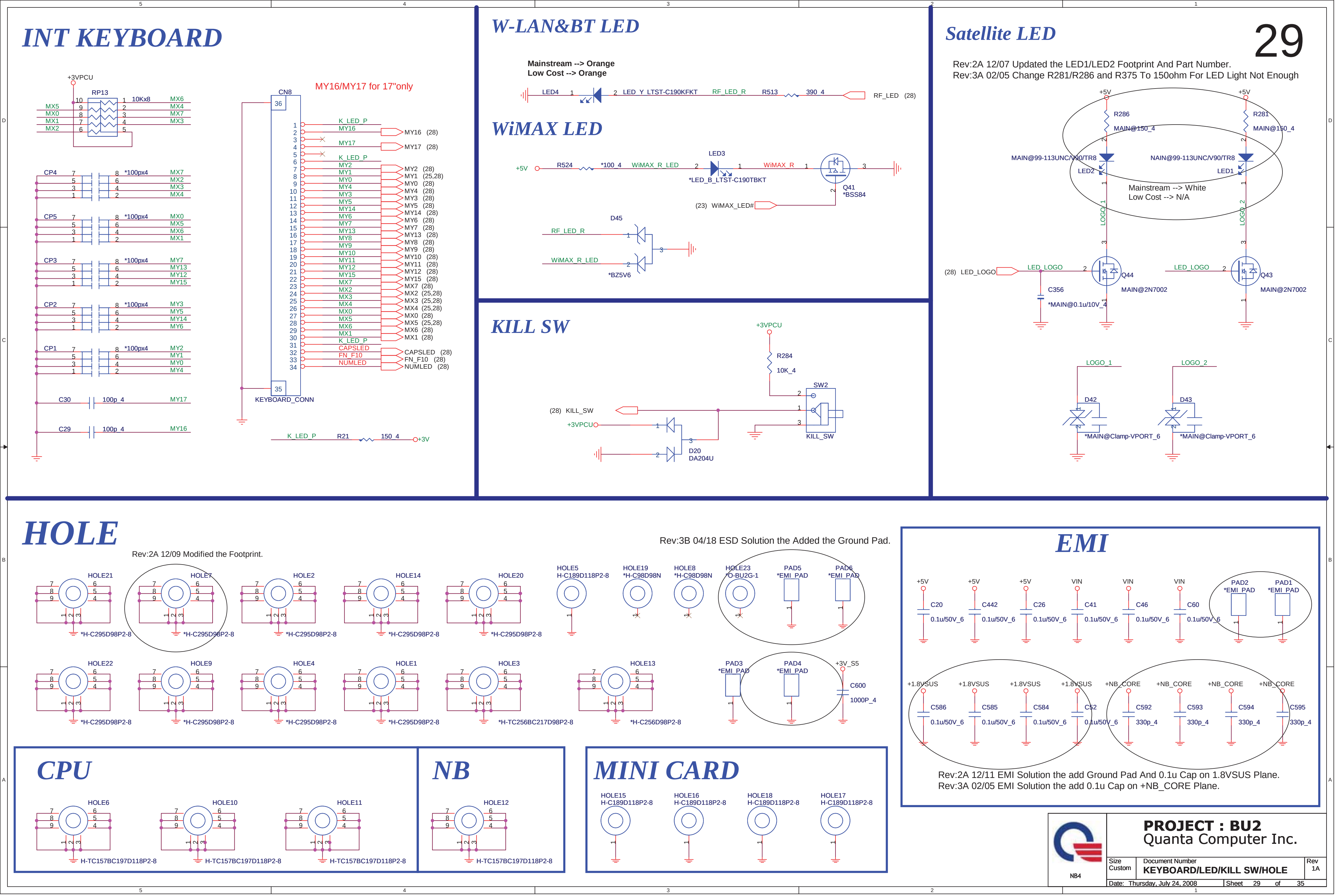
MXIC	MX25L8005M2C-15G	AKE5GFK0Z09
Winbond	W25X80VSSIG	AKE3GFP0N08
EON	EN25F80-75HCP	AKE3GZP0Q00

INTERNAL KEYBOARD STRIP SET



CIR





29
INT KEYBOARD
MY16/MY17 for 17"only
KEYBOARD_CONN
W-LAN&BT LED
Mainstream --> Orange
Low Cost --> Orange
WiMAX LED
KILL SW
Satellite LED
Rev:2A 12/07 Updated the LED1/LED2 Footprint And Part Number.
Rev:3A 02/05 Change R281/R286 and R375 To 150ohm For LED Light Not Enough
Mainstream --> White
Low Cost --> N/A
HOLE
Rev:2A 12/09 Modified the Footprint.
Rev:3B 04/18 ESD Solution the Added the Ground Pad.
EMI
Rev:2A 12/11 EMI Solution the add Ground Pad And 0.1u Cap on 1.8VSUS Plane.
Rev:3A 02/05 EMI Solution the add 0.1u Cap on +NB_CORE Plane.
CPU
NB
MINI CARD
PROJECT : BU2
Quanta Computer Inc.
NB4
Size Custom
Document Number KEYBOARD/LED/KILL SW/HOLE
Rev 1A
Date: Thursday, July 24, 2008
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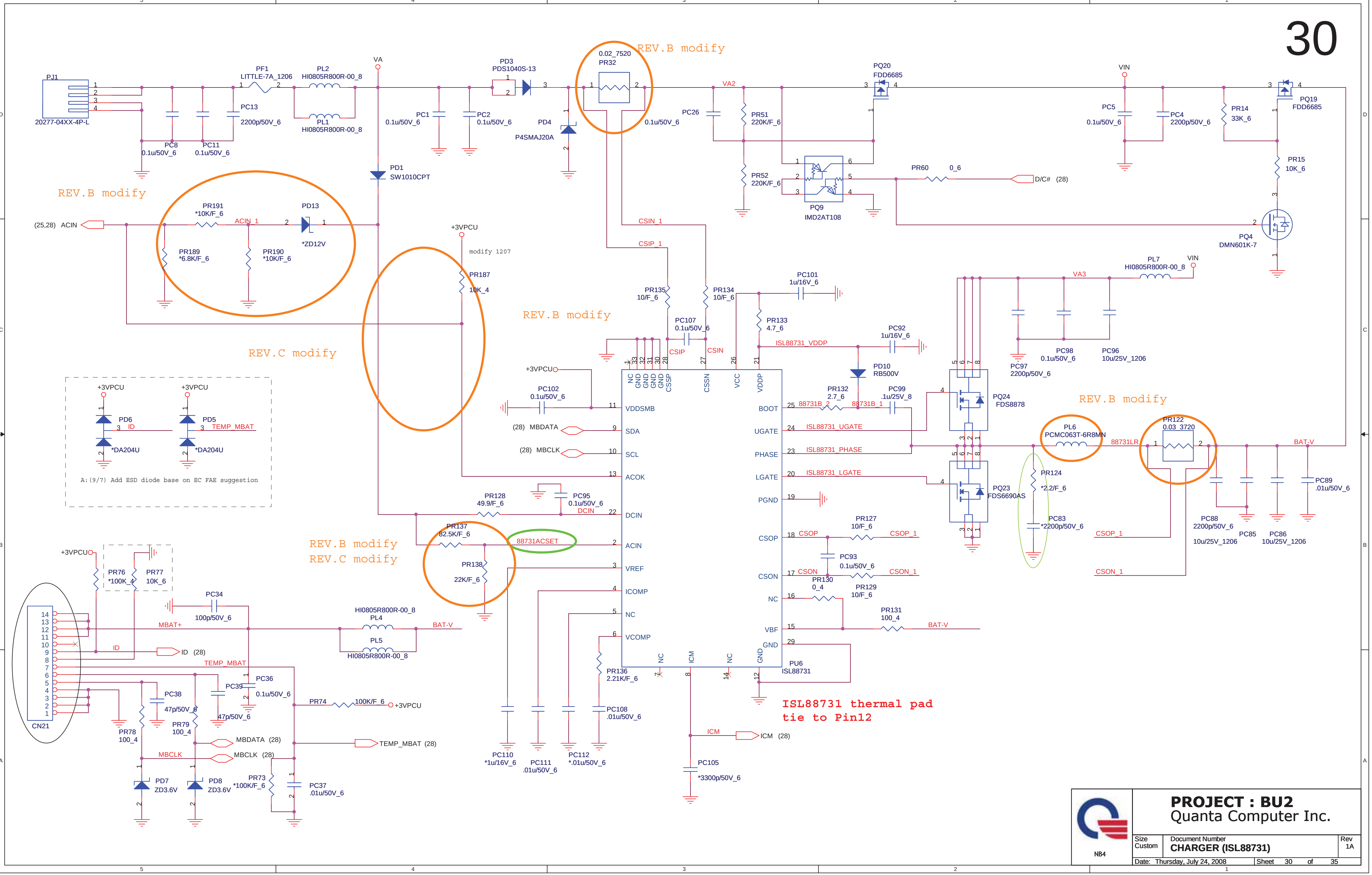

REV.B modify
REV.C modify
REV.B modify
REV.C modify
modify 1207
A:(9/7) Add ESD diode base on EC FAE suggestion
ISL88731 thermal pad
tie to Pin12
PJ1
20277-04XX-4P-L
PF1
LITTLE-7A_1206
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA
PD3
PDS1040S-13
0.02_7520
PR32
VA2
PQ20
FDD6685
VIN
PQ19
FDD6685
PC13
2200p/50V_6
PC8
0.1u/50V_6
PC11
0.1u/50V_6
PC1
0.1u/50V_6
PC2
0.1u/50V_6
PD4
P4SMAJ20A
PC26
0.1u/50V_6
PR51
220K/F_6
PC5
0.1u/50V_6
PC4
2200p/50V_6
PR14
33K_6
PD1
SW1010CPT
PR52
220K/F_6
PQ9
IMD2AT108
PR60
0_6
D/C# (28)
PR15
10K_6
PQ4
DMN601K-7
(25,28) ACIN
PR191
*10K/F_6
ACIN_1
PD13
*ZD12V
PR189
*6.8K/F_6
PR190
*10K/F_6
+3VPCU
PR187
10K_4
CSIN_1
CSIP_1
PR135
10/F_6
PR134
10/F_6
PC101
1u/16V_6
PR133
4.7_6
PL7
HI0805R800R-00_8
VA3
PC107
0.1u/50V_6
CSIP
CSIN
PC92
1u/16V_6
ISL88731_VDDP
PD10
RB500V
PC97
2200p/50V_6
PC98
0.1u/50V_6
PC96
10u/25V_1206
PC102
0.1u/50V_6
VDDSMB
(28) MBDATA
SDA
(28) MBCLK
SCL
ACOK
PR128
49.9/F_6
PC95
0.1u/50V_6
DCIN
PR137
82.5K/F_6
88731ACSET
ACIN
PR138
22K/F_6
VREF
ICOMP
NC
VCOMP
PR136
2.21K/F_6
PC110
*1u/16V_6
PC111
.01u/50V_6
PC112
*.01u/50V_6
PC108
.01u/50V_6
ICM
ICM (28)
PC105
*3300p/50V_6
PU6
ISL88731
BOOT
PR132
2.7_6
88731B_2
88731B_1
PC99
.1u/25V_8
UGATE
ISL88731_UGATE
PHASE
ISL88731_PHASE
LGATE
ISL88731_LGATE
PGND
CSOP
CSOP_1
PR127
10/F_6
PC93
0.1u/50V_6
CSON
CSON_1
PR130
0_4
PR129
10/F_6
PR131
100_4
VBF
BAT-V
GND
VDDP
VCC
CSSN
PQ24
FDS8878
PQ23
FDS6690AS
PL6
PCMC063T-6R8MN
88731LR
PR122
0.03_3720
PR124
*2.2/F_6
PC83
*2200p/50V_6
PC88
2200p/50V_6
PC85
10u/25V_1206
PC86
10u/25V_1206
PC89
.01u/50V_6
PD6
*DA204U
PD5
TEMP_MBAT
*DA204U
ID
PR76
*100K_4
PR77
10K_6
PC34
100p/50V_6
CN21
MBAT+
HI0805R800R-00_8
PL4
PL5
HI0805R800R-00_8
ID (28)
TEMP_MBAT
PC36
0.1u/50V_6
PC38
47p/50V_6
PC39
47p/50V_6
PR74
100K/F_6
PR78
100_4
PR79
100_4
MBDATA (28)
MBCLK (28)
TEMP_MBAT (28)
PD7
ZD3.6V
PD8
ZD3.6V
PR73
*100K/F_6
PC37
.01u/50V_6
PROJECT : BU2
Quanta Computer Inc.
NB4
Size
Custom
Document Number
CHARGER (ISL88731)
Rev
1A
Date: Thursday, July 24, 2008
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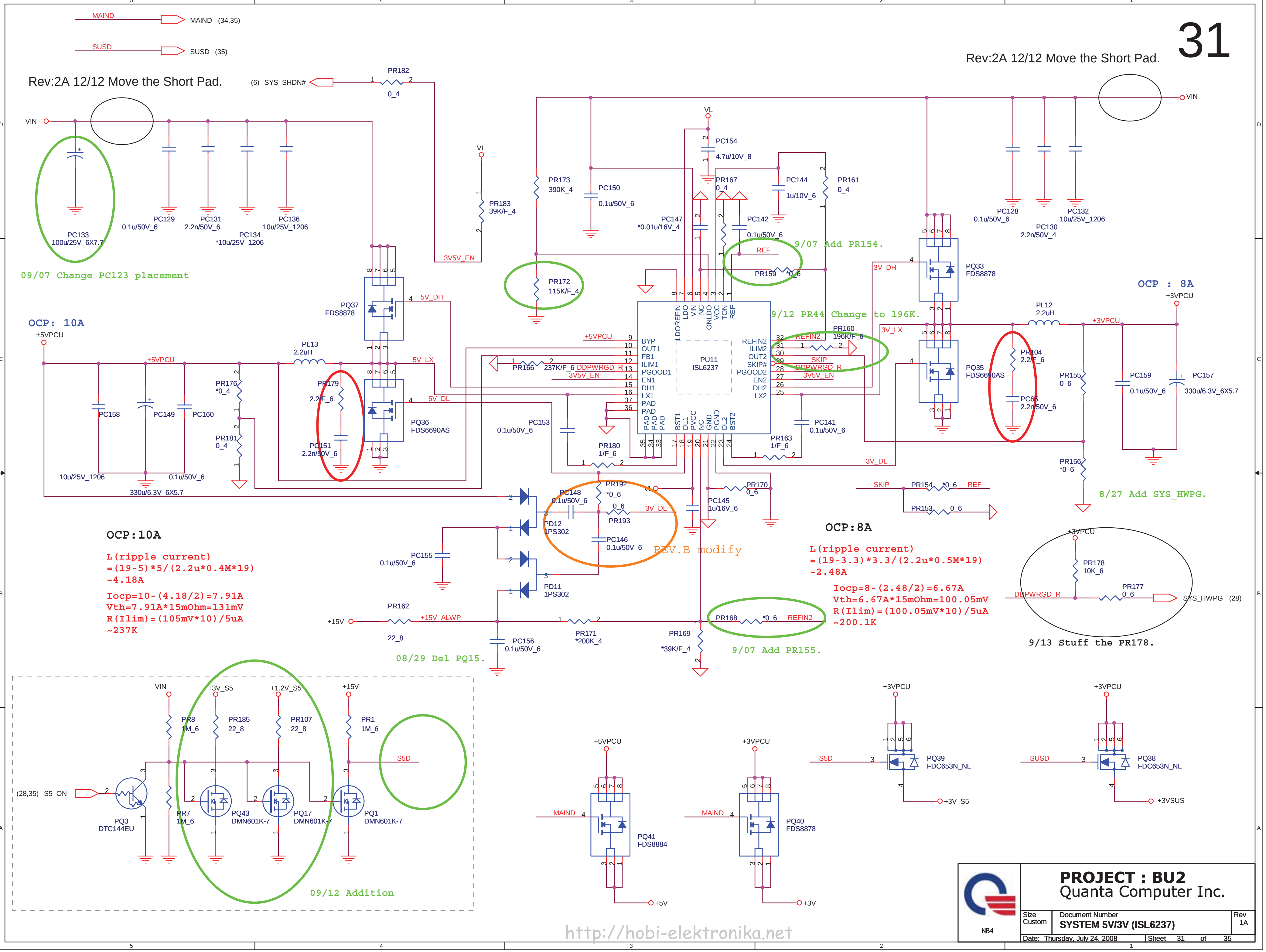
Rev:2A 12/12 Move the Short Pad.
Rev:2A 12/12 Move the Short Pad.
MAIND (34,35)
SUSD (35)
(6) SYS_SHDN#
VIN
09/07 Change PC123 placement
OCP: 10A
OCP : 8A
9/07 Add PR154.
9/12 PR44 Change to 196K.
PU11
ISL6237
8/27 Add SYS_HWPG.
REV.B modify
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*15mOhm=131mV
R(Ilim)=(105mV*10)/5uA
~237K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
08/29 Del PQ15.
9/07 Add PR155.
9/13 Stuff the PR178.
SYS_HWPG (28)
(28,35) S5_ON
09/12 Addition
PROJECT : BU2
Quanta Computer Inc.
NB4
Size Custom
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Thursday, July 24, 2008
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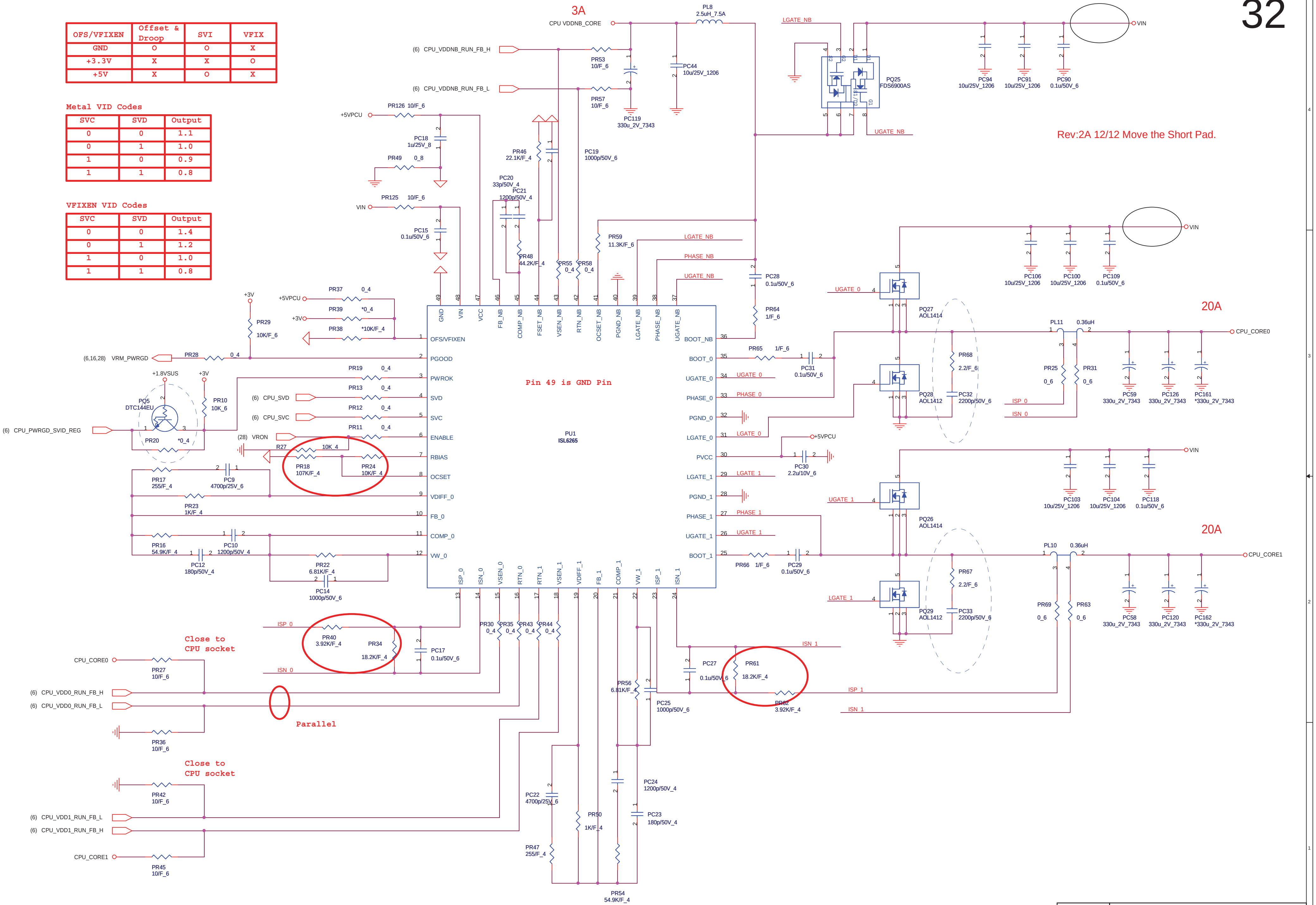
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
C	AMD GRIFFIN CPU (ISL6265)	1A

NB4

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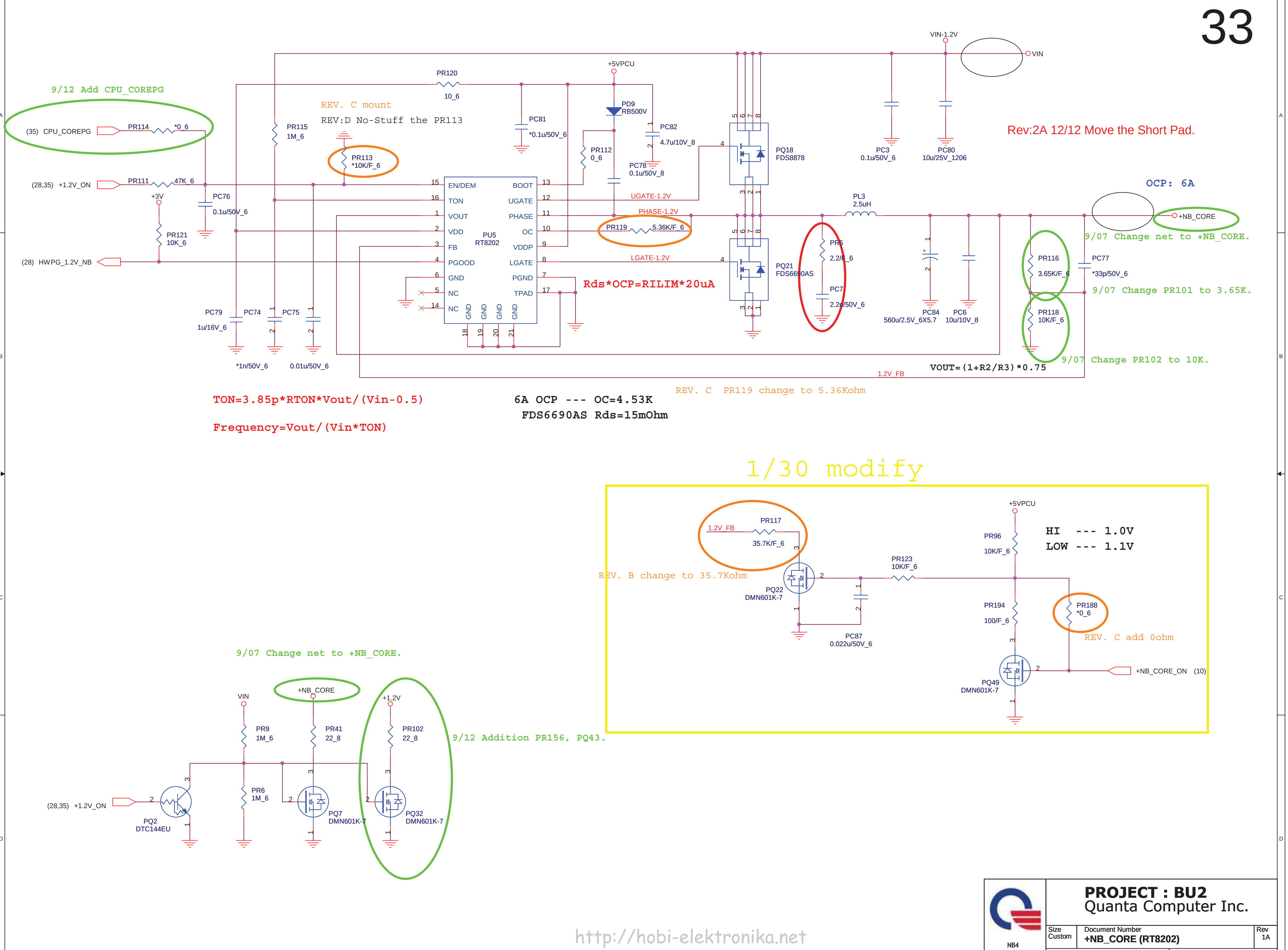

PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	+NB_CORE (RT8202)	1A

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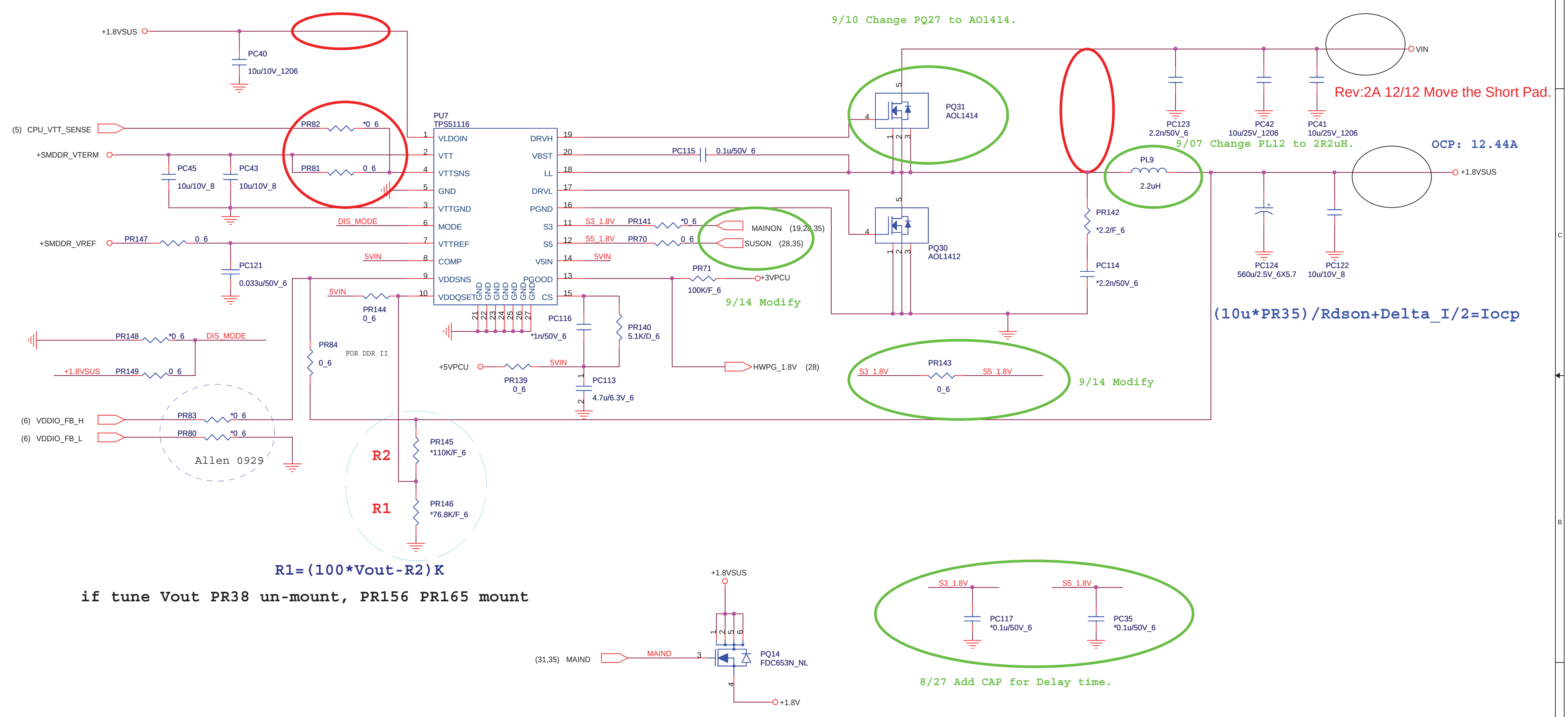

PROJECT : BU2
Quanta Computer Inc.

NB4

Size	Document Number	Rev
Custom	DDR 1.8V(TPS51116)	1A

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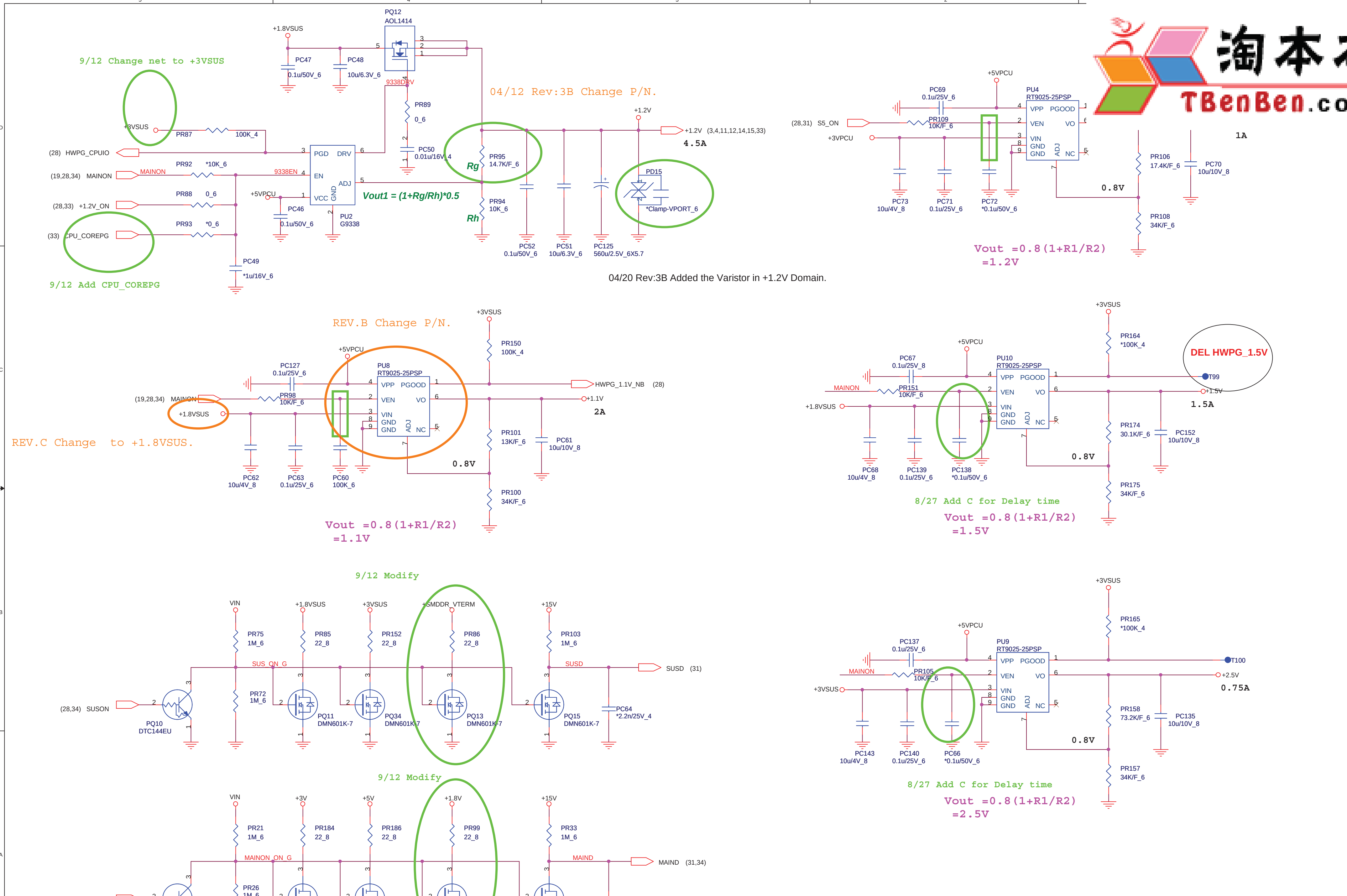

PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE (1.25V/1.5V/1.2V)	1A

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NB4