

Compal Confidential

HBL51 Schematics Document

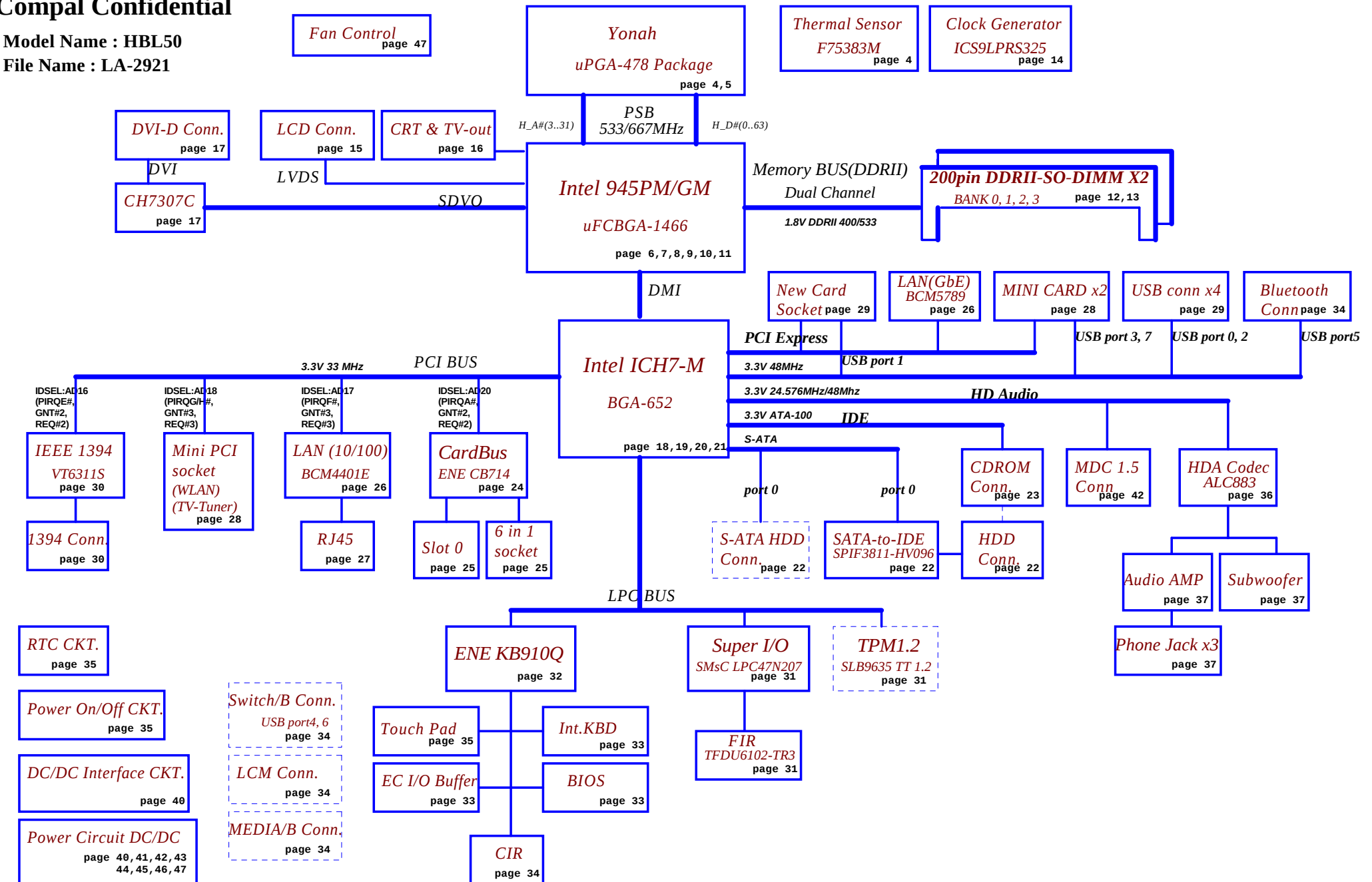
Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M

2005-11-03

REV: 0.2

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Model Name : HBL50
File Name : LA-2921



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

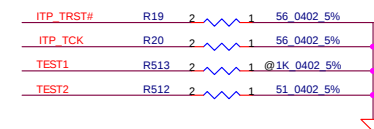
BTO Option Table

BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@

SKU ID Table

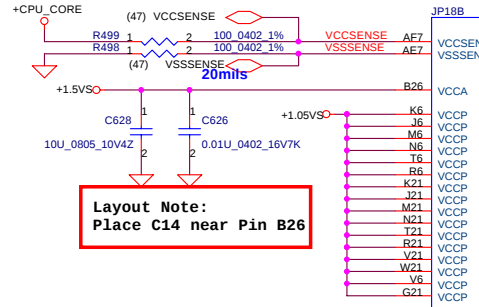
SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	

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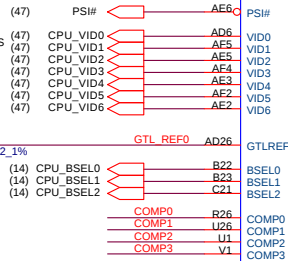


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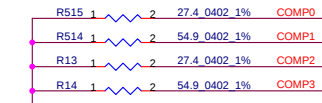
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms
with 50 mil spacing.
Place PU and PD within 1 inch of CPU.



Layout Note:
Place C14 near Pin B26



BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166



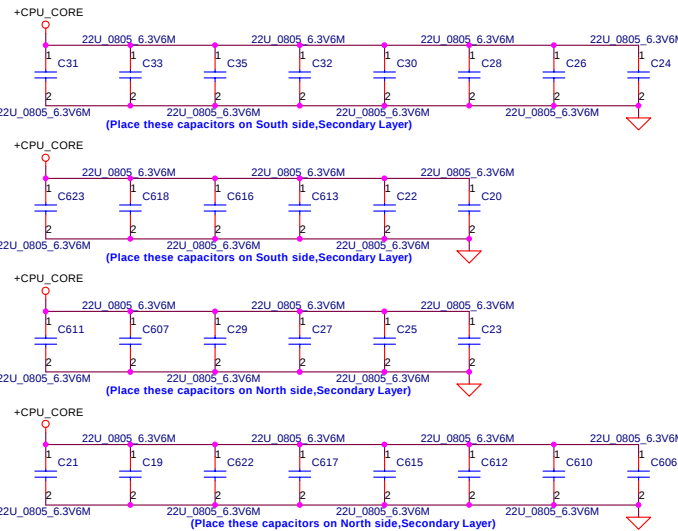
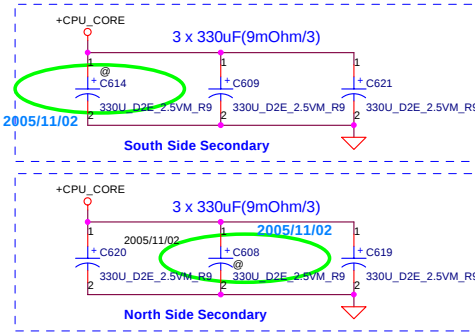
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)
COMP1, COMP3 layout : Space 25mils (550hms)

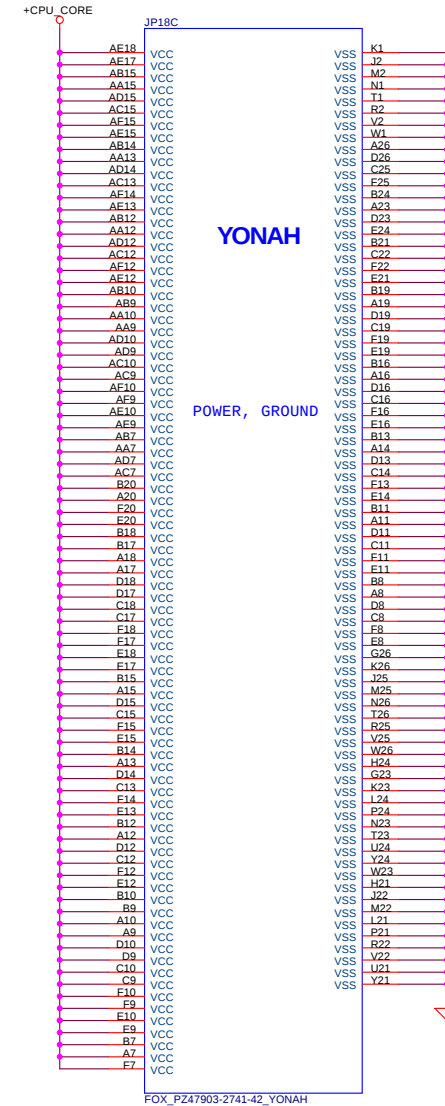
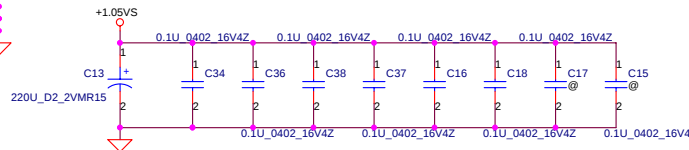
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

FOX_PZ47903-2741-42_YONAH



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32

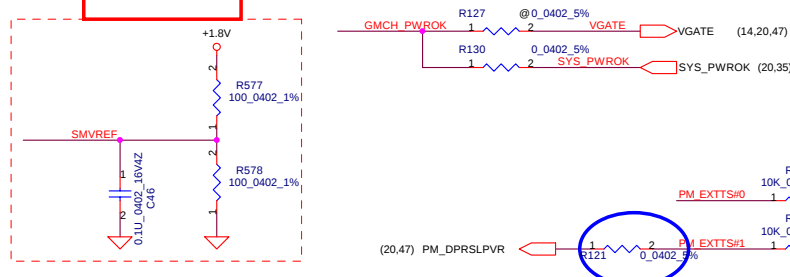
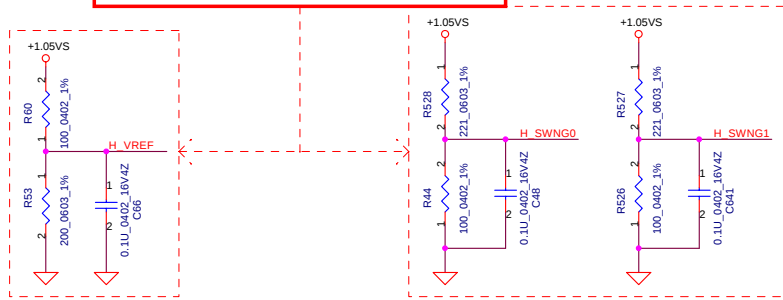


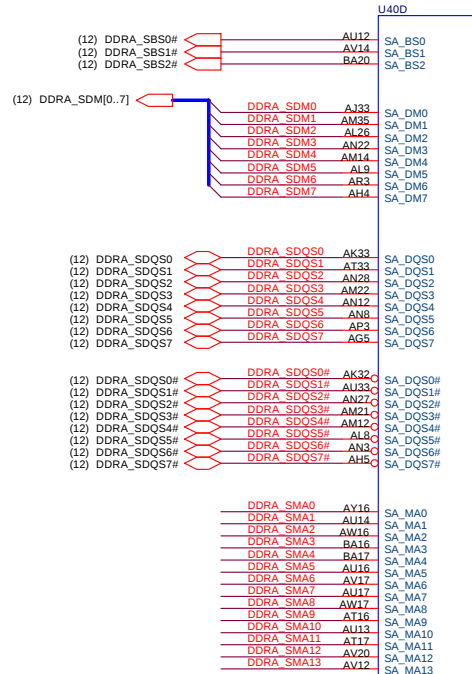
YONAH

POWER, GROUND

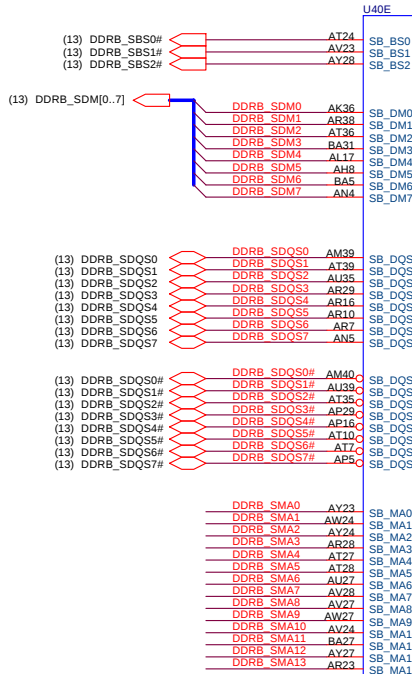
FOX_PZ47903-2741-42_YONAH

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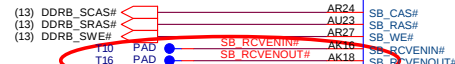




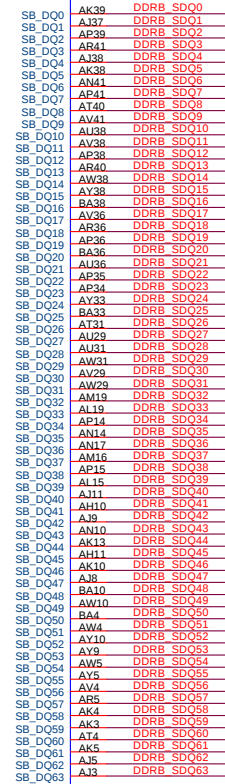
DDR SYS MEMORY A



DDR SYS MEMORY B



check layout

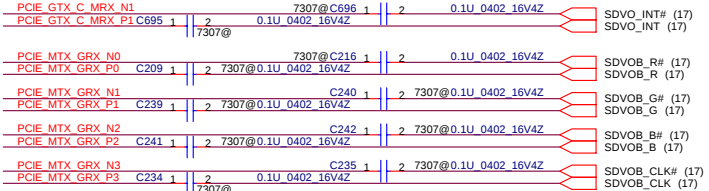
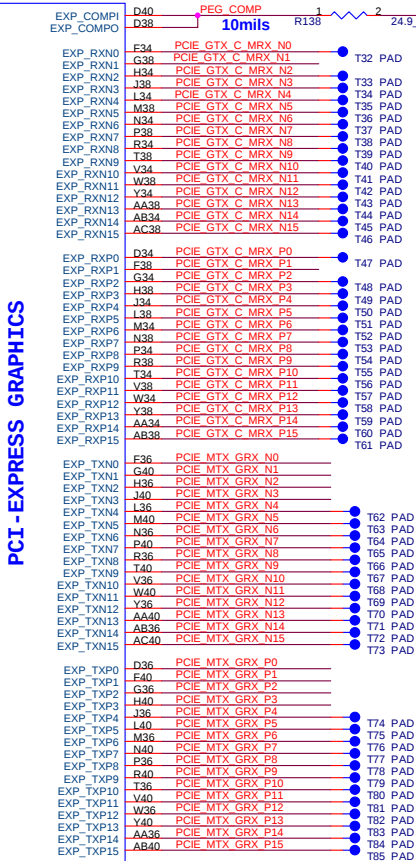
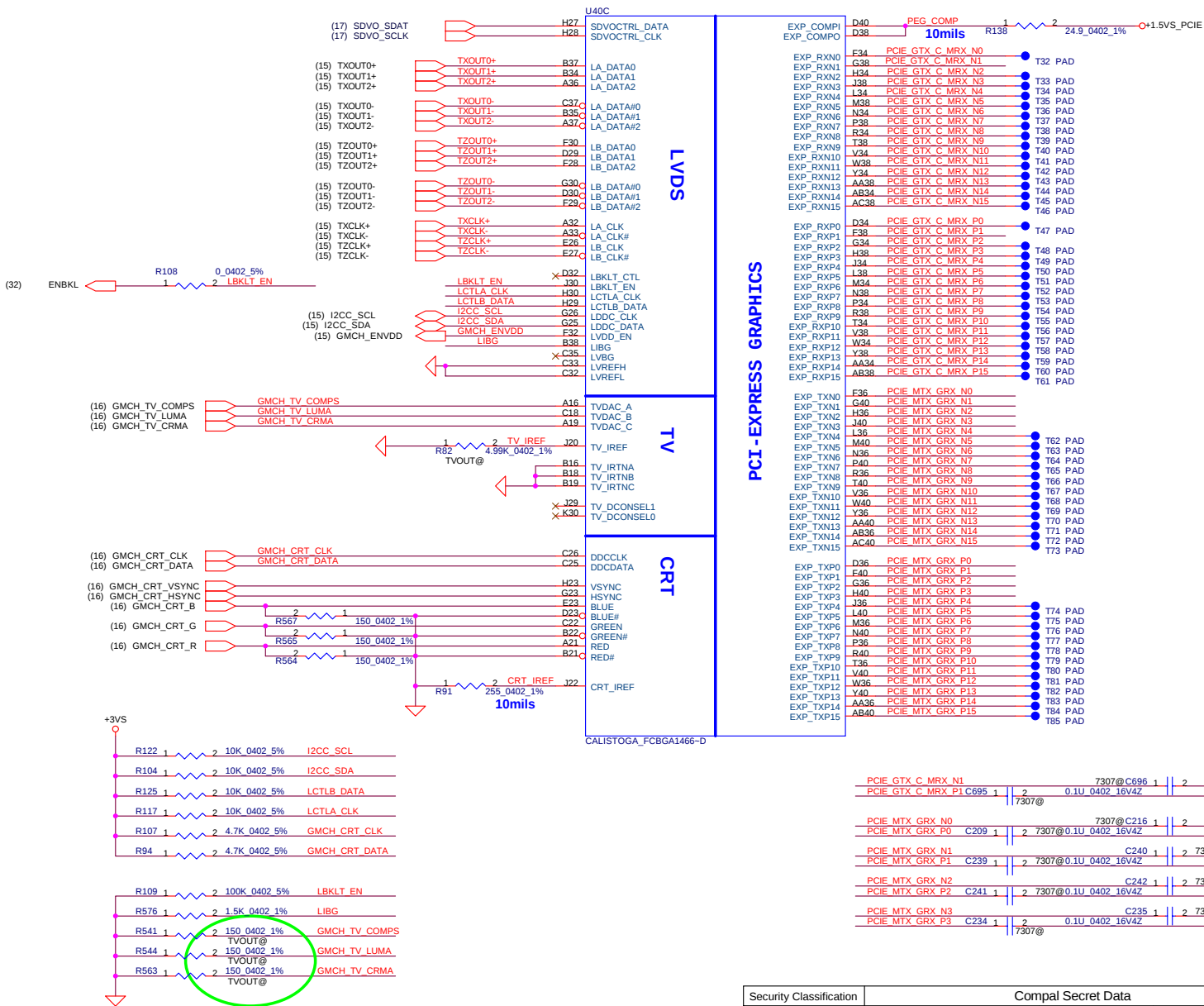


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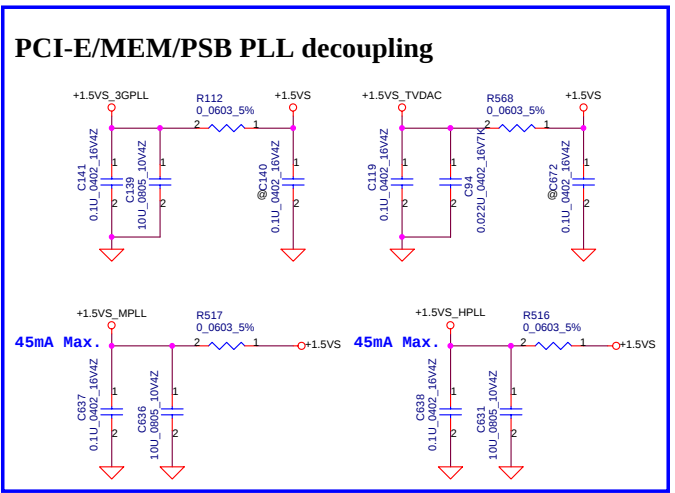
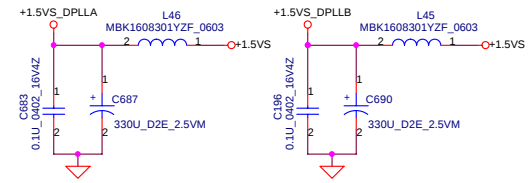
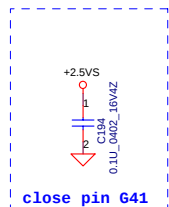
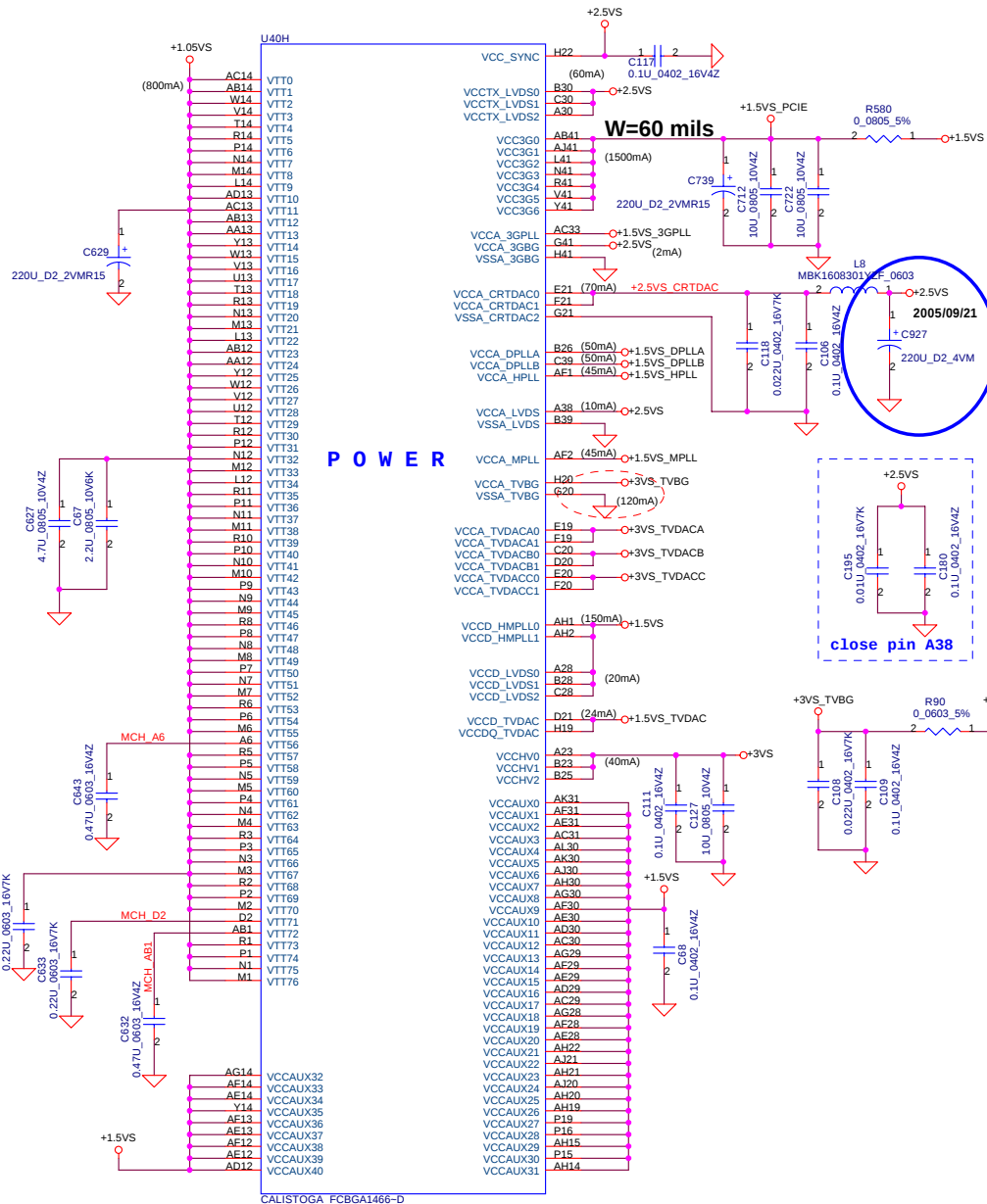
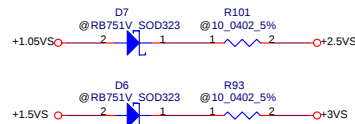
CALISTOGA_FCBGA1466-D

CALISTOGA_FCBGA1466-D

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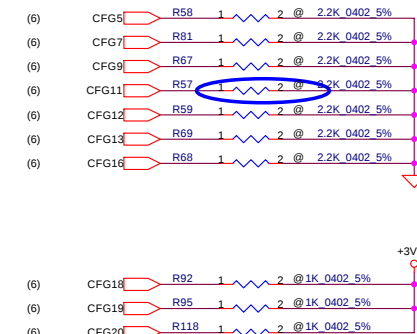
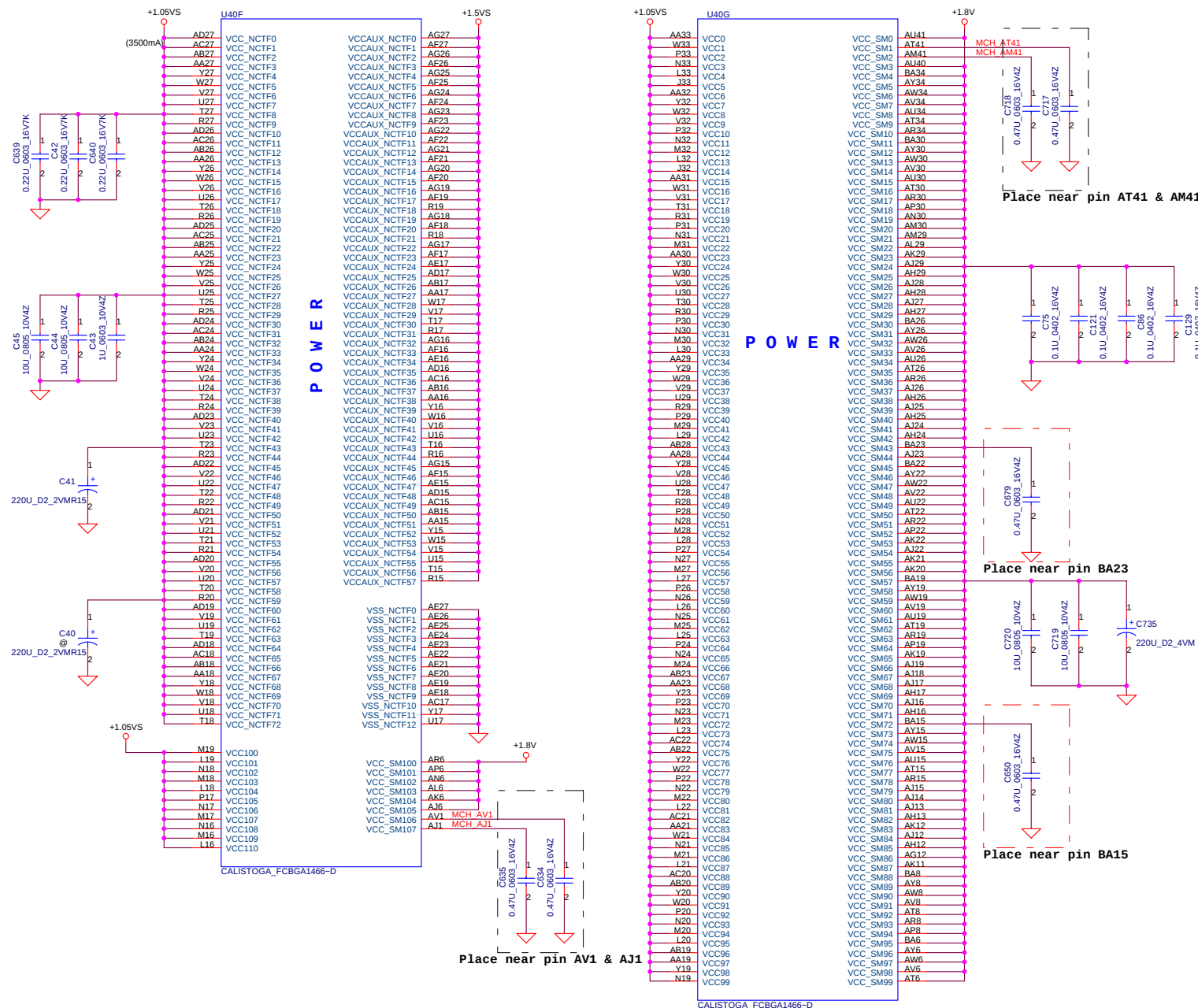


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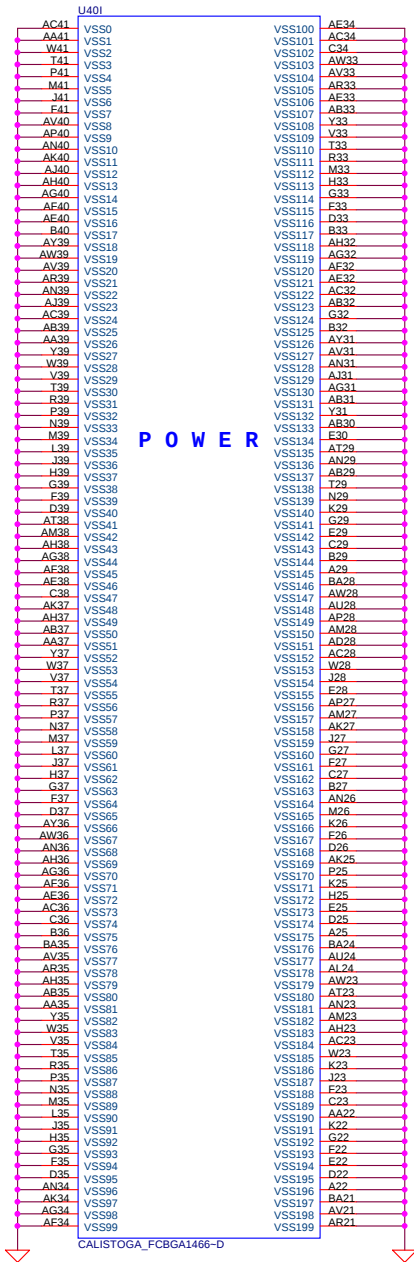
Strap Pin Table

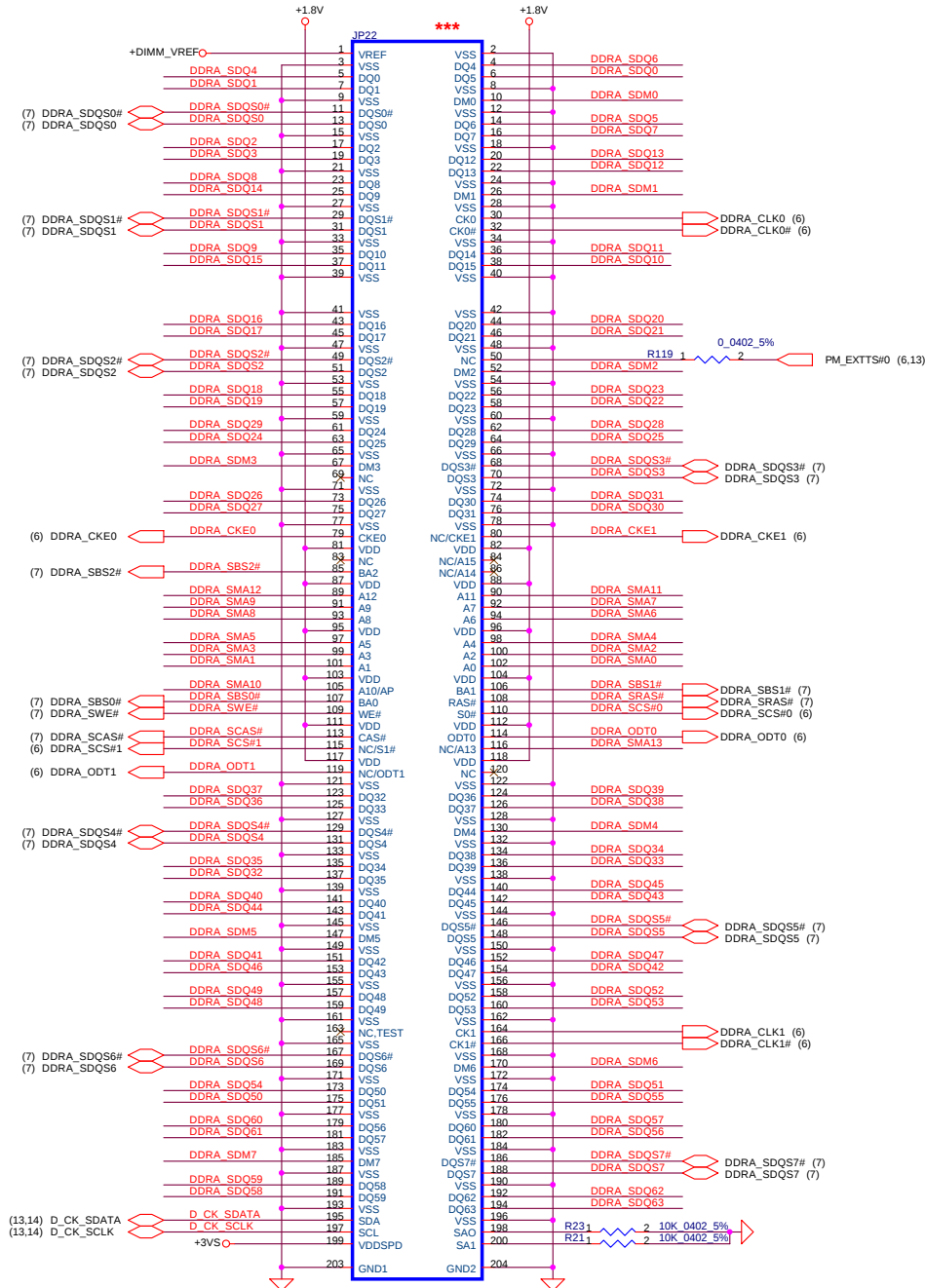
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.95V *(Default) 1 = 1.5V
CFG19	0 = No SDVO Device Present *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

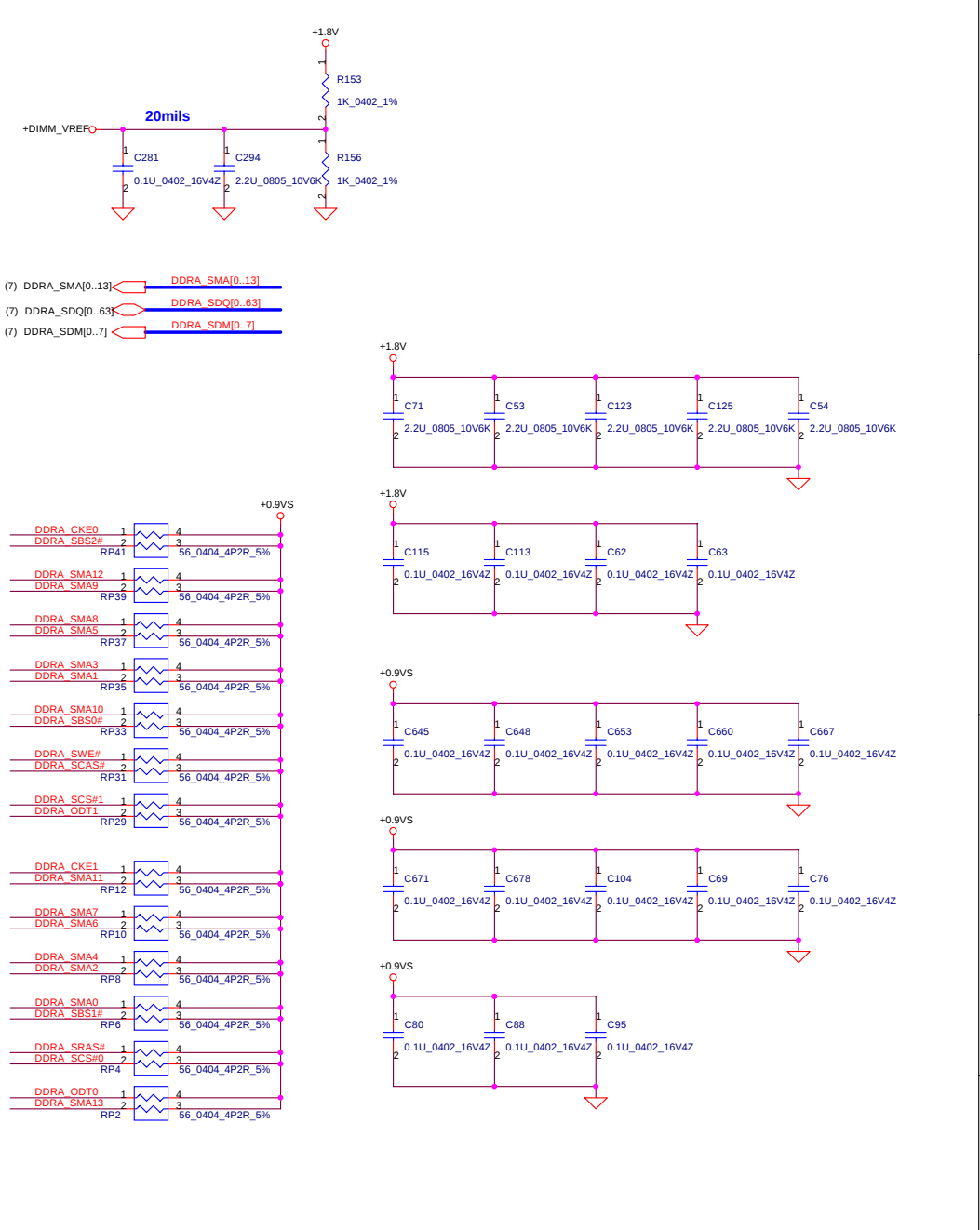


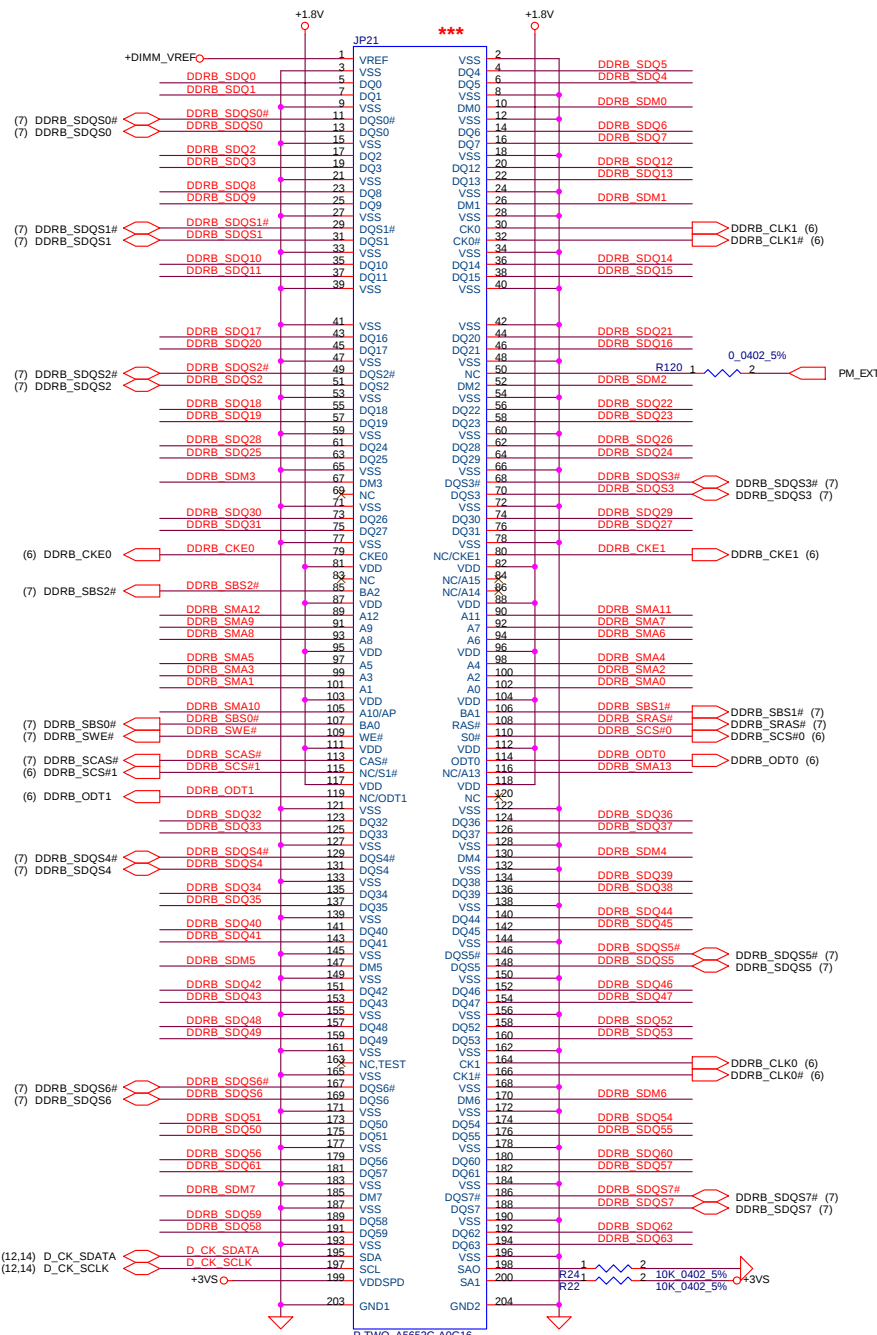
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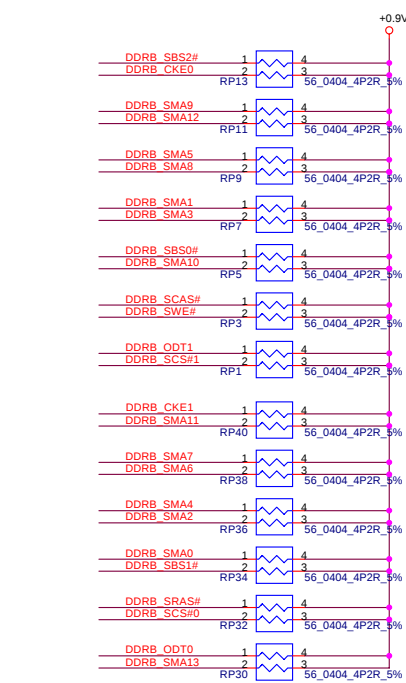
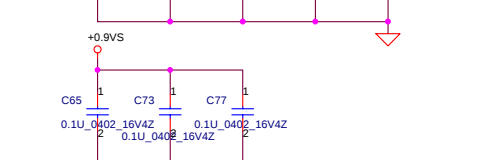
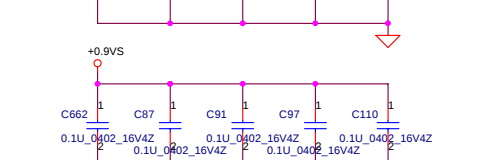
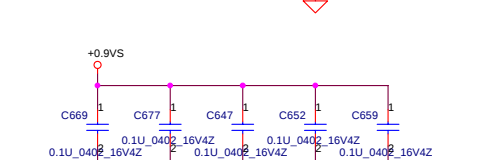
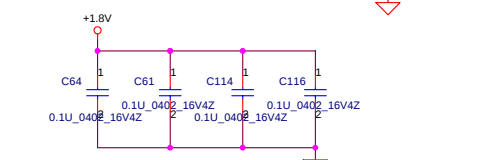
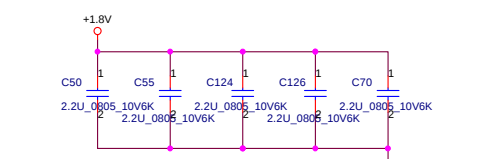
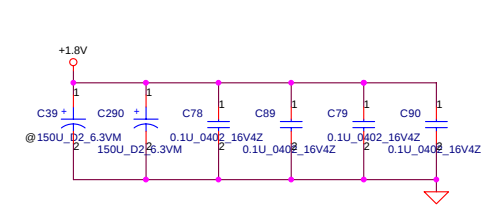
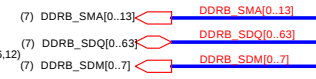
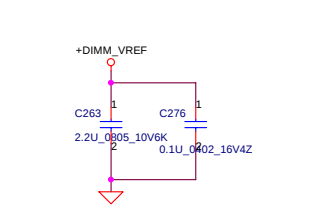


DIMM0 STD H:9.2mm (BOT)

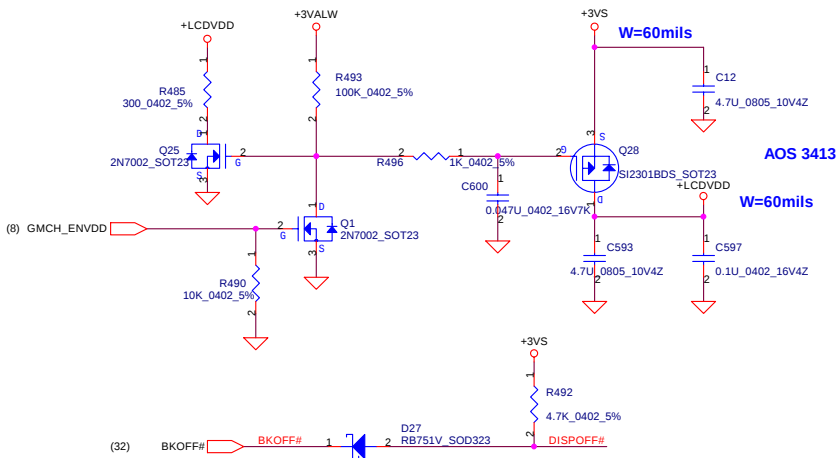




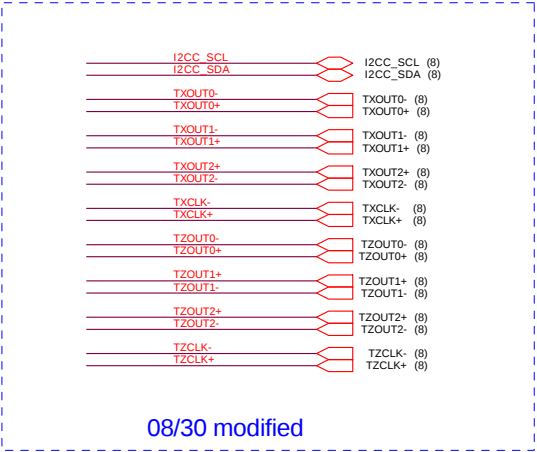
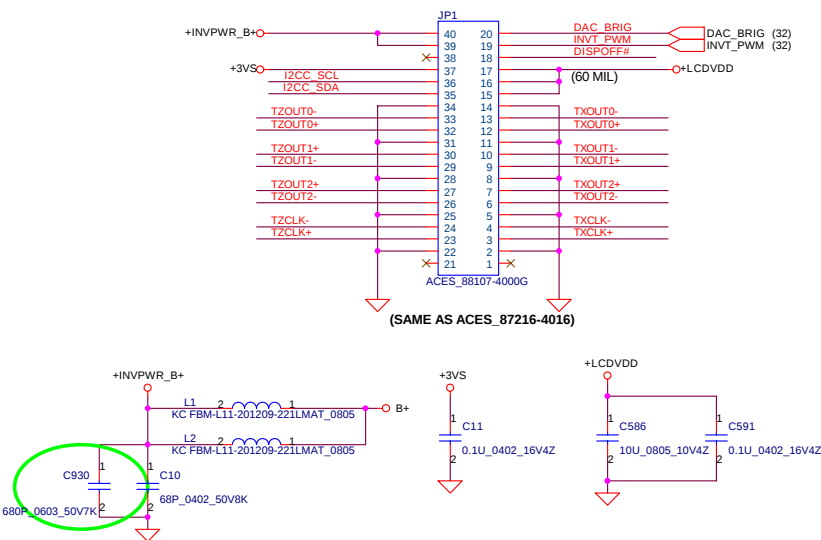
DIMM1 STD H:5.2mm (BOT)



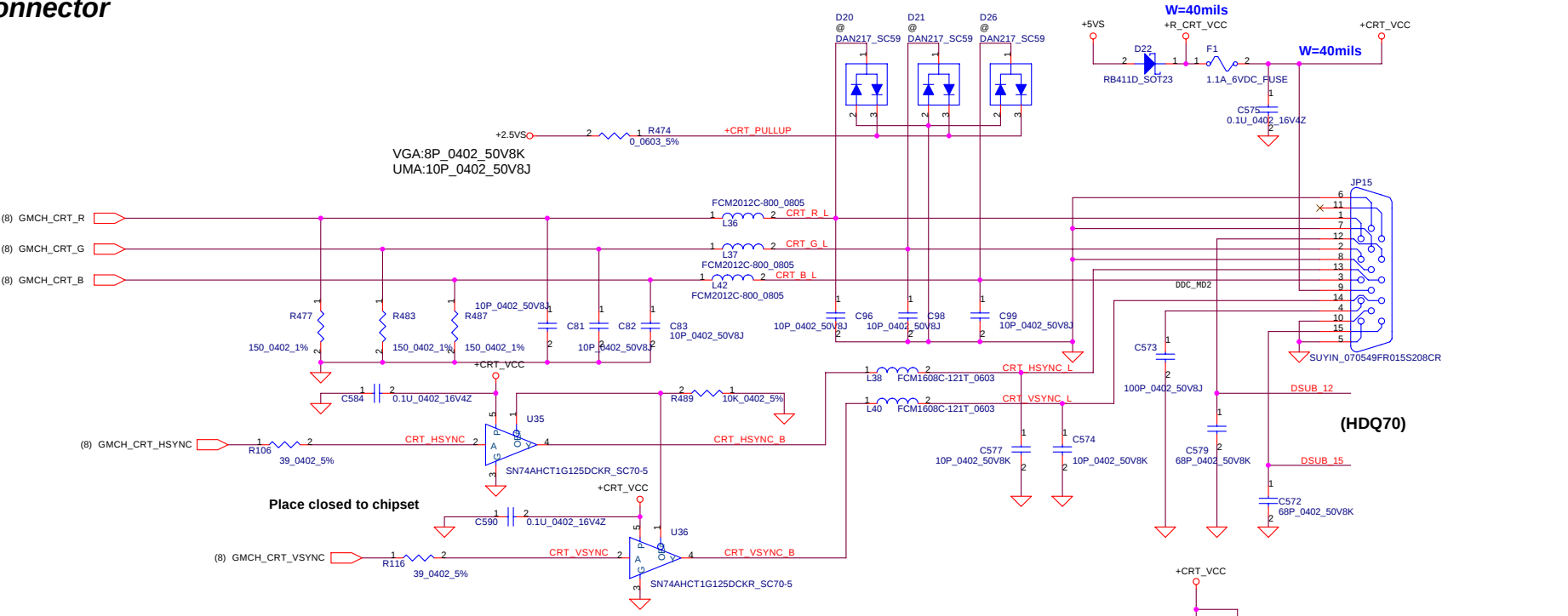
LCD POWER CIRCUIT



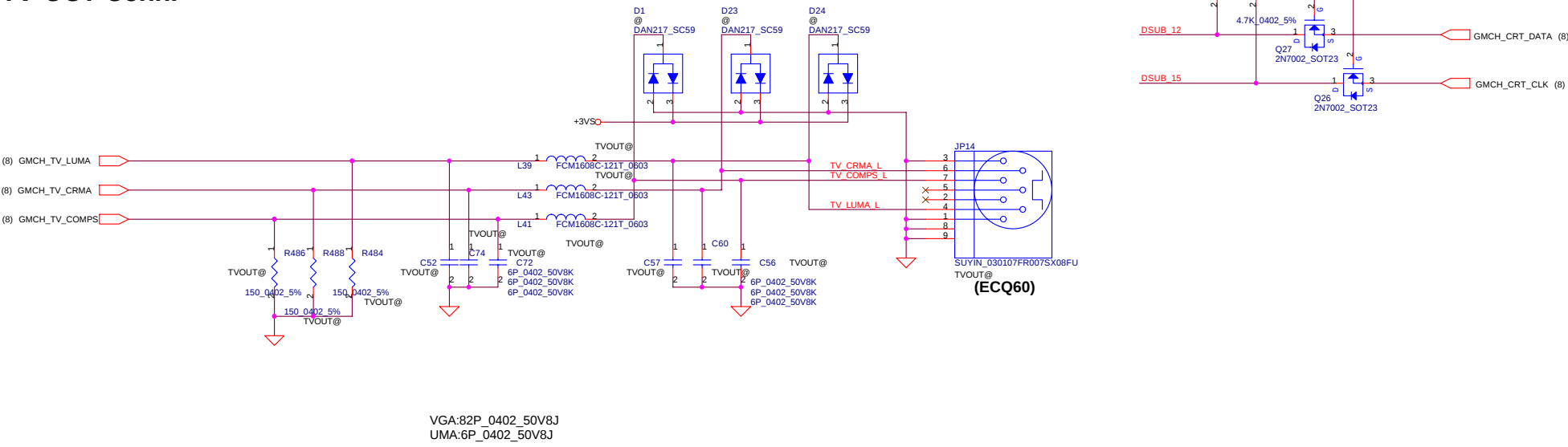
LCD/PANEL BD. Conn.



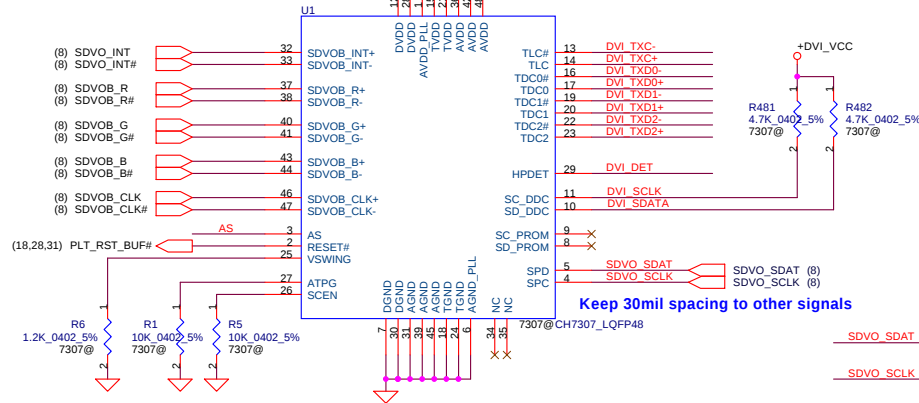
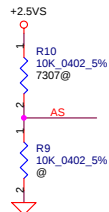
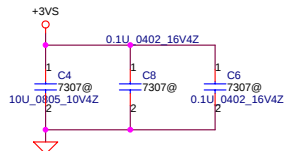
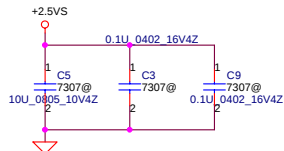
CRT Connector



TV-OUT Conn.



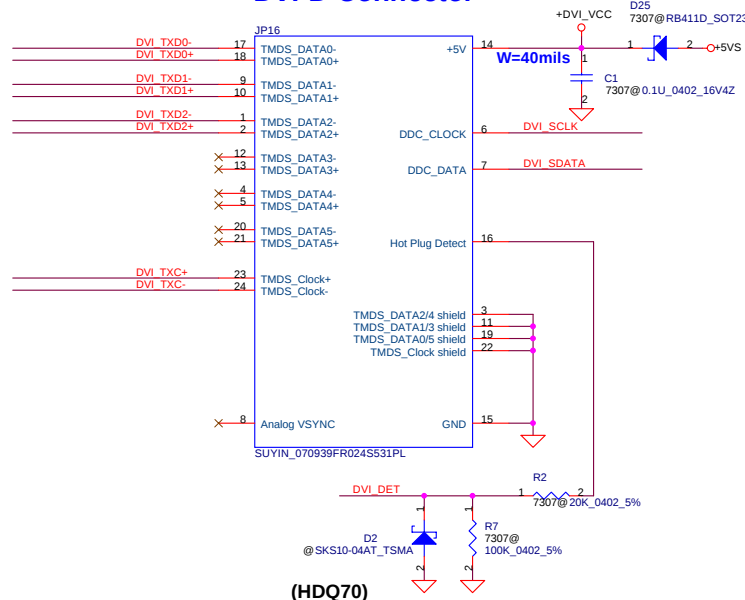
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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BOM structure	DVI from SDVO
7307@	Stuff
@	No_Stuff

Keep 30mil spacing to other signals

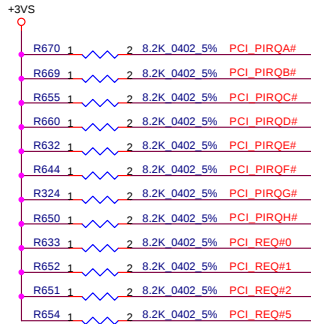
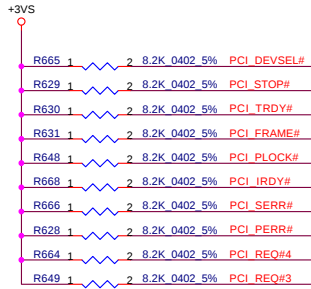
DVI-D Connector



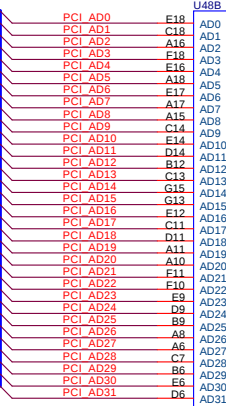
(HDQ70)

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				Size	Document Number	Rev
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				Sheet 17 of 47		

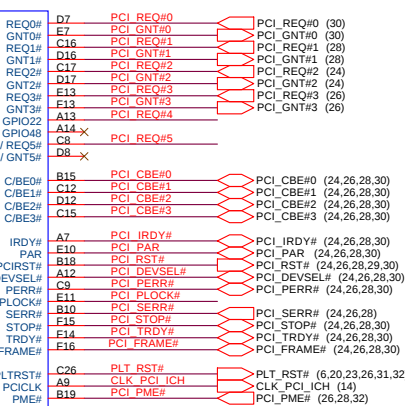
ICH7M(B-0) (QK17) [ES3] : SA00000JK30



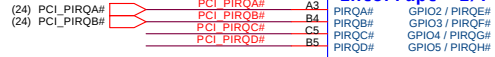
(24,26,28,30) PCI_AD[0..31]



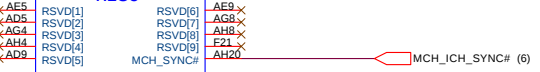
PCI



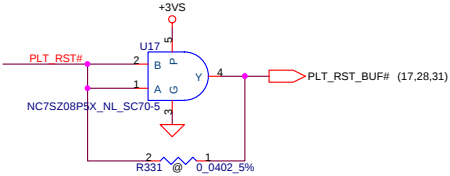
Interrupt I/F



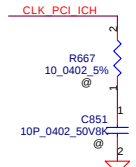
MISC



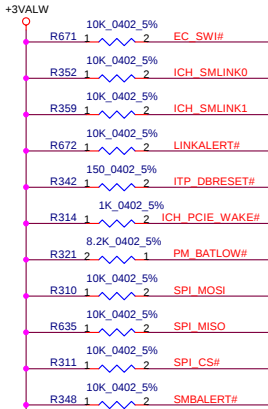
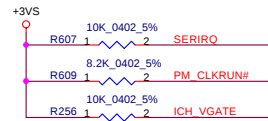
ICH7_BGA652-D



Place closely pin A9



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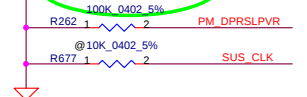


2005/10/27

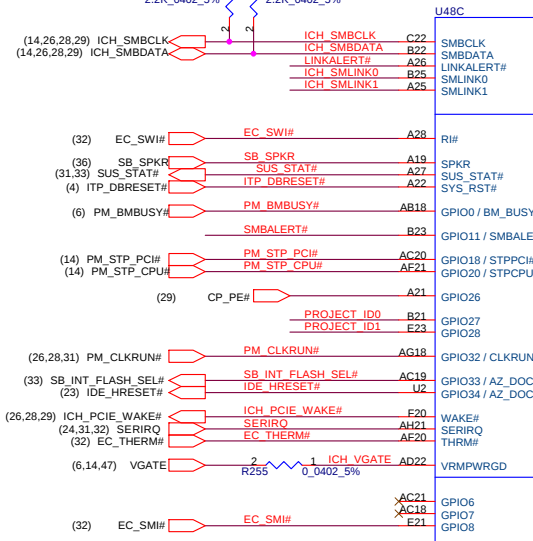
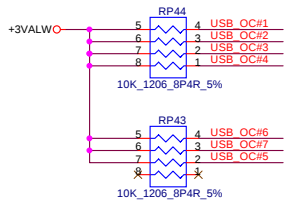
2005/11/02

PROJECT_ID0

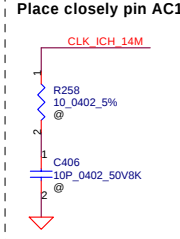
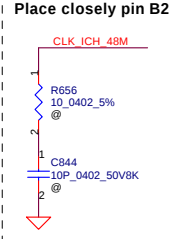
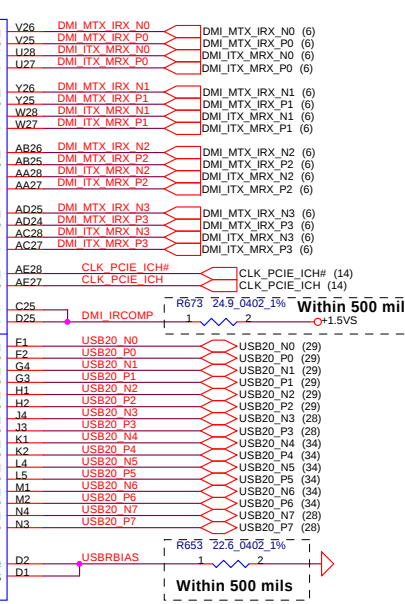
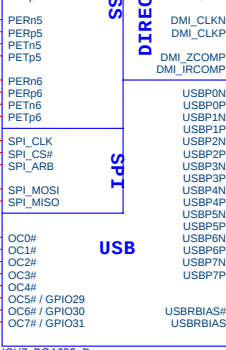
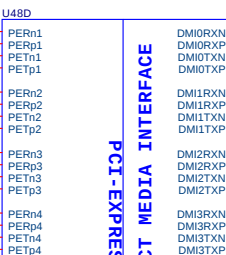
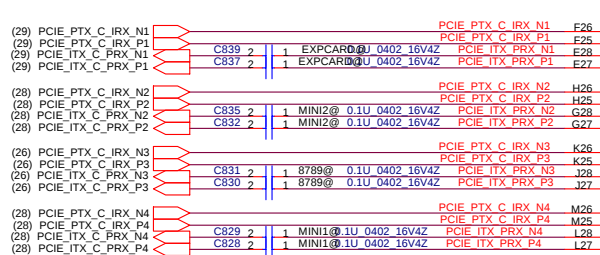
PROJECT_ID1



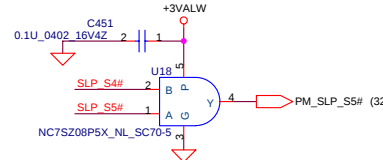
PROJECT_ID[1:0]	
00	Grapevine
01	Geneva
10	HBL51_PATA



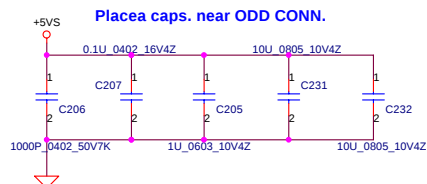
Need update symbol



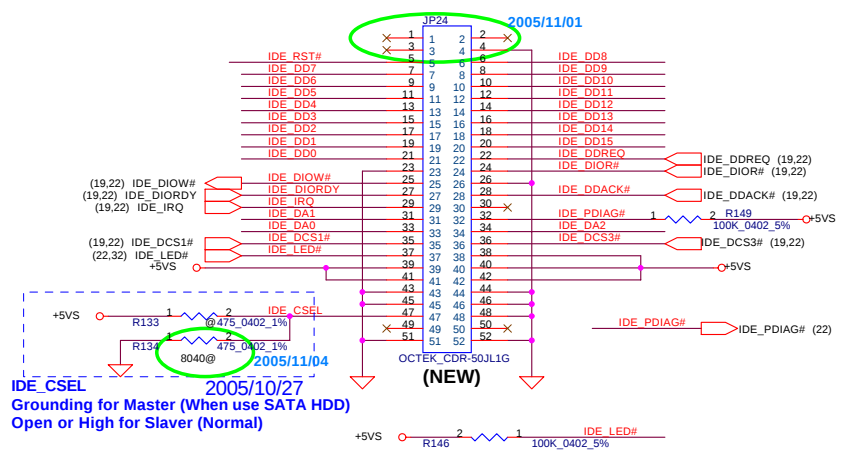
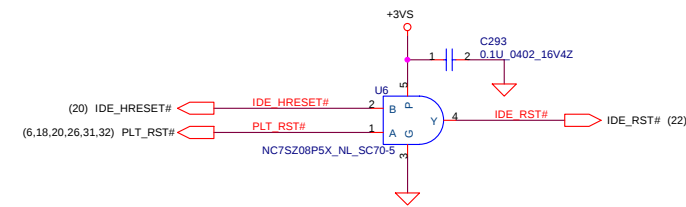
PM_DPRSPLVR : Need to series a 500ohm resistor to IMVP6



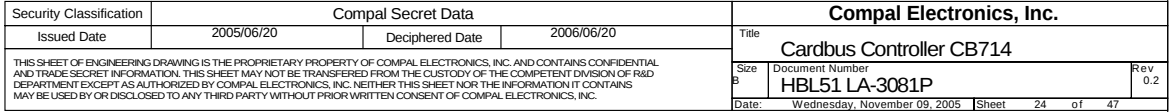
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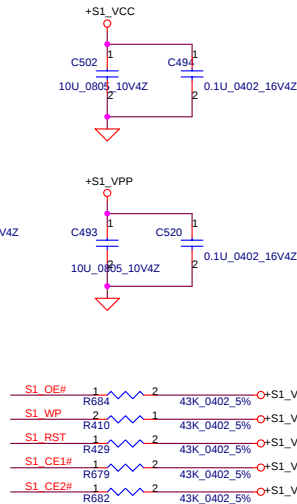
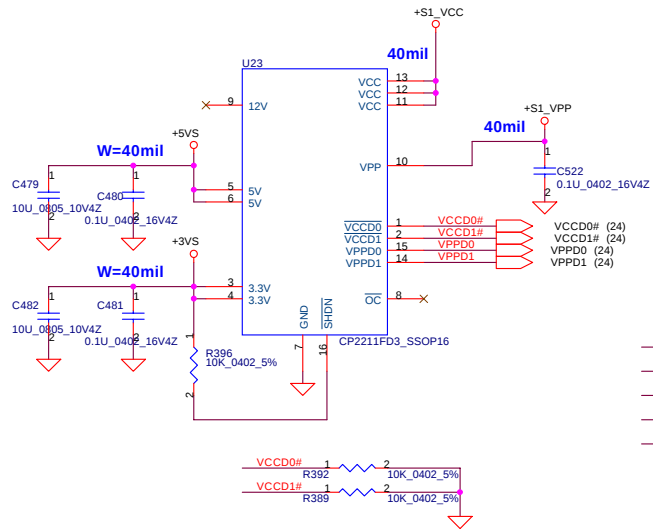
(19,22) IDE_DD[0..15] $\rightarrow$ IDE_DD[0..15]
 (19,22) IDE_DA[0..2] $\rightarrow$ IDE_DA[0..2]



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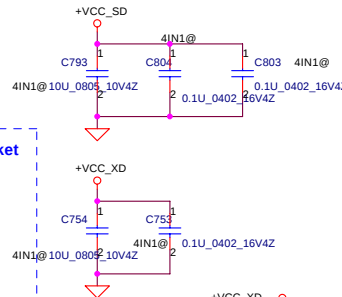
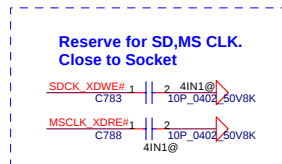
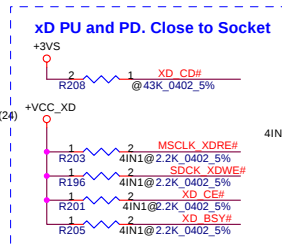
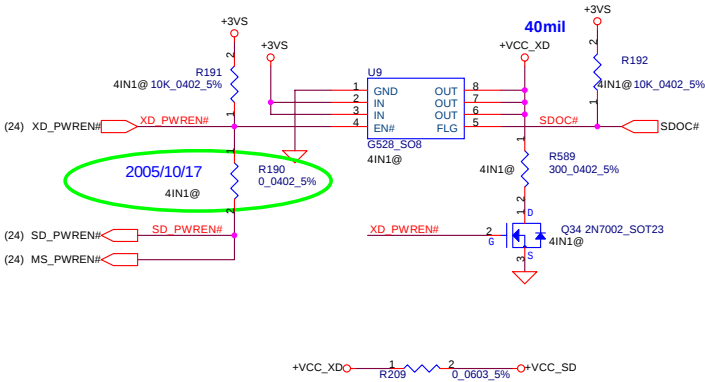


PCMCIA Power Control



(24) S1_A[0..25] S1_A[0..25]
(24) S1_D[0..15] S1_D[0..15]

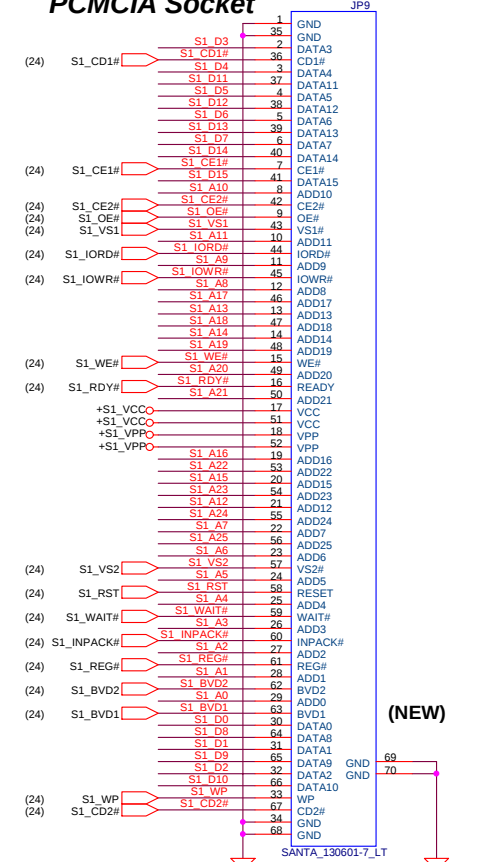
SD/MS Power Control XD Power Control



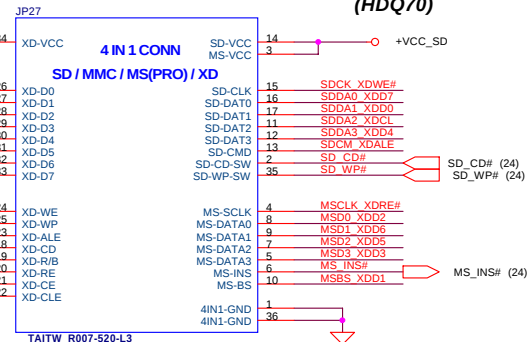
(24) SDDA1_XDD0 SDDA1_XDD0
(24) MSBS_XDD1 MSBS_XDD1
(24) MSD0_XDD2 MSD0_XDD2
(24) MSD3_XDD3 MSD3_XDD3
(24) SDDA3_XDD4 SDDA3_XDD4
(24) MSD2_XDD5 MSD2_XDD5
(24) MSD1_XDD6 MSD1_XDD6
(24) SDDA0_XDD7 SDDA0_XDD7

(24) SDCK_XDWE# SDCK_XDWE#
(24) XD_WP# XD_WP#
(24) SDCM_XDALE SDCM_XDALE
(24) XD_CD# XD_CD#
(24) XD_BSY# XD_BSY#
(24) MSLCK_XDRE# MSLCK_XDRE#
(24) XD_CE# XD_CE#
(24) SDDA2_XDCL SDDA2_XDCL

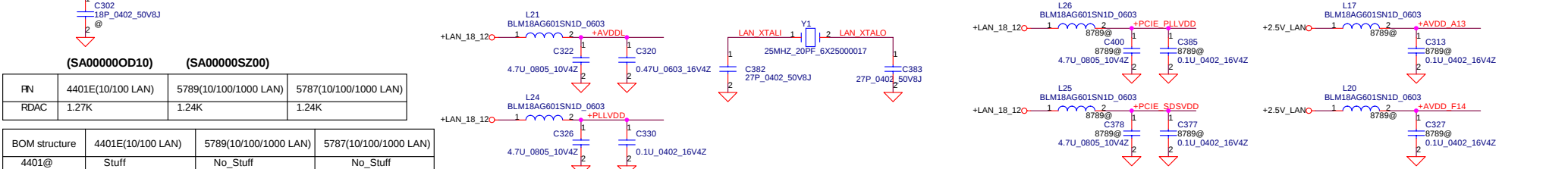
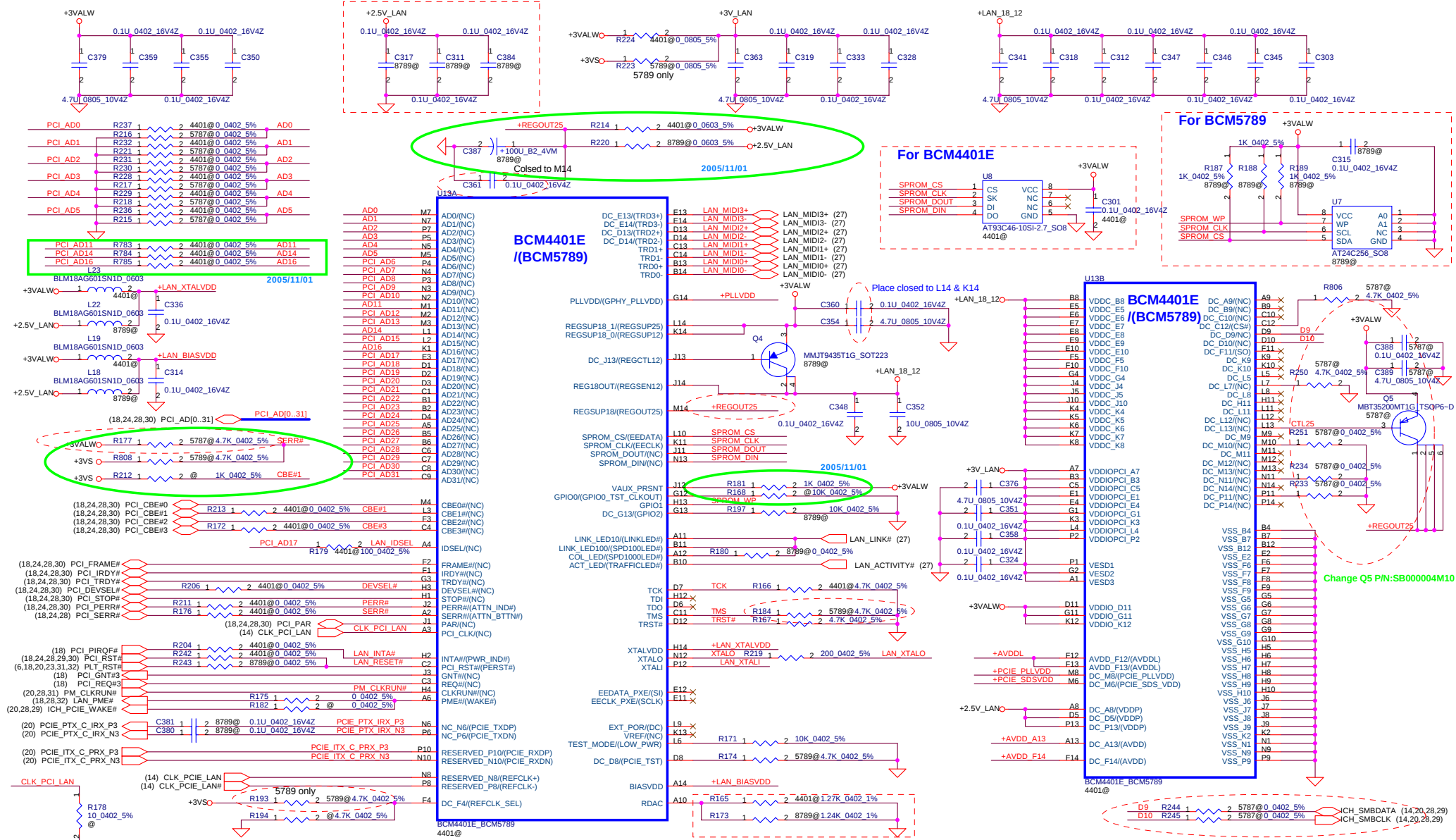
PCMCIA Socket



4 IN 1 Socket (HDQ70)



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(SA000000D10)		(SA000000S200)	
FN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

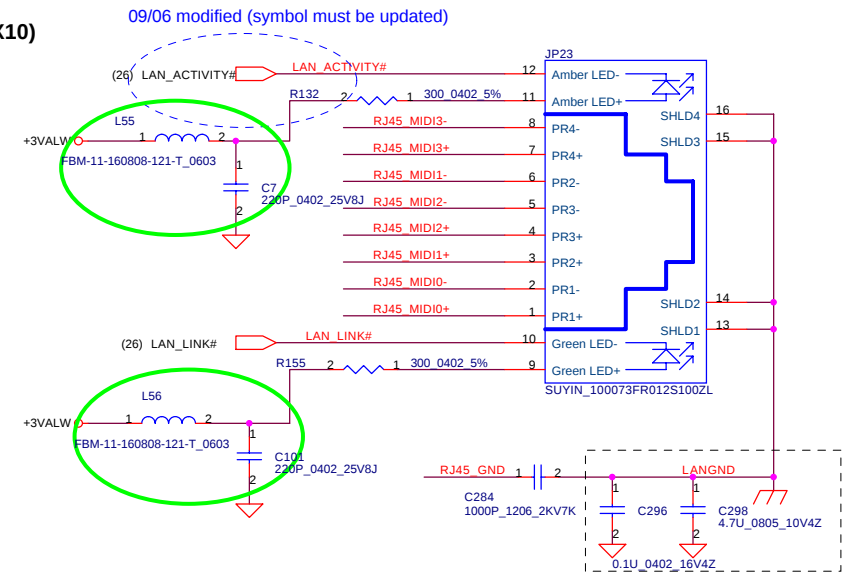
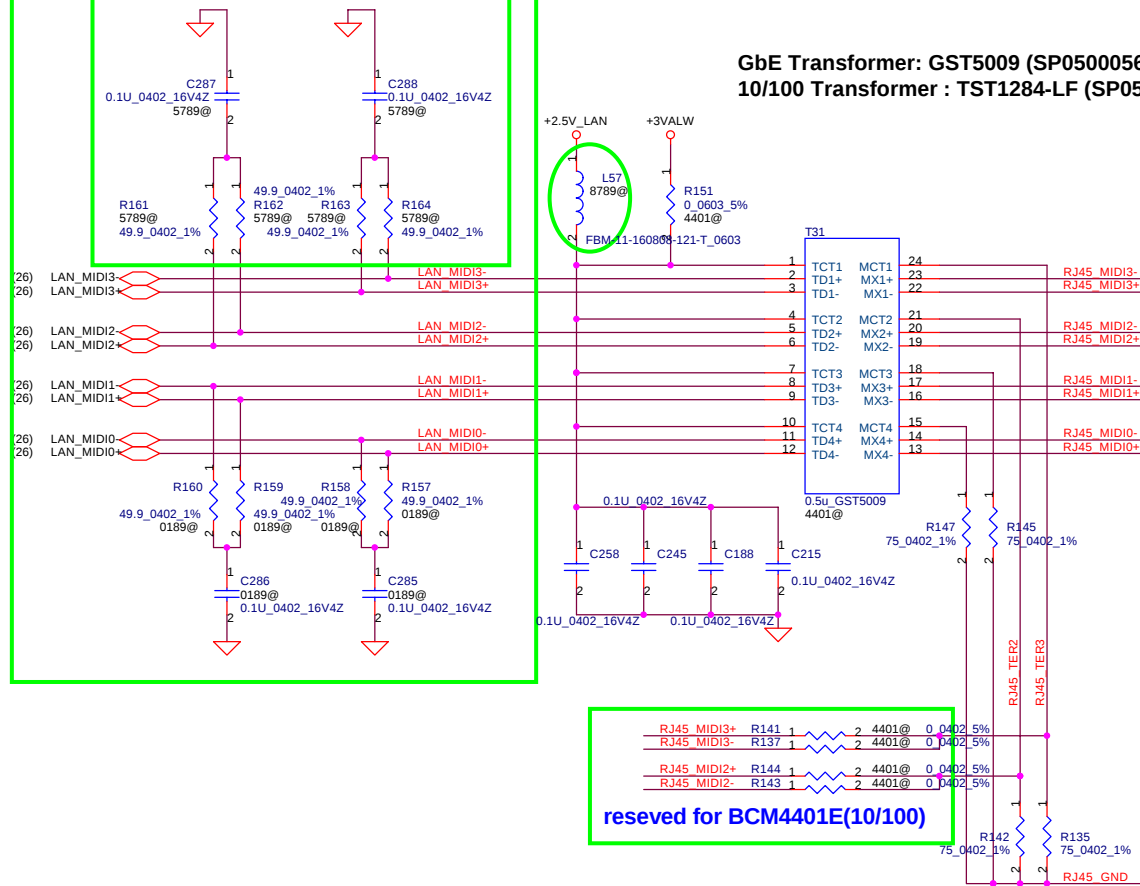
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Date: Wednesday, November 09, 2005			

Compal Electronics, Inc.			
LAN BCM4401E/Jade15			
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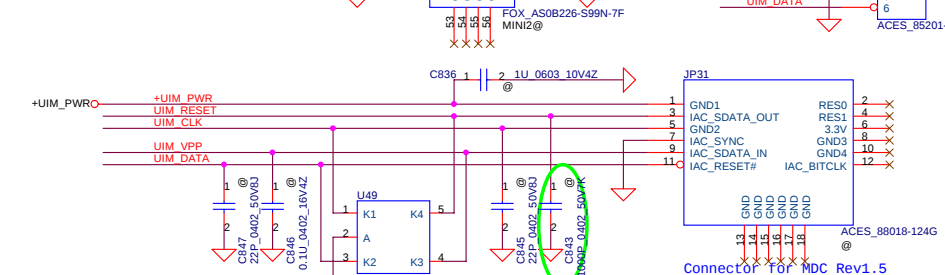
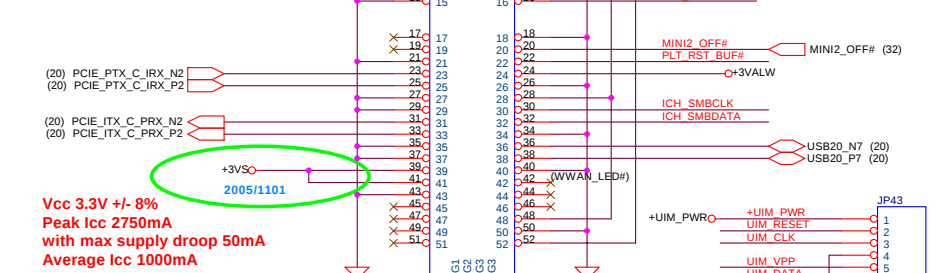
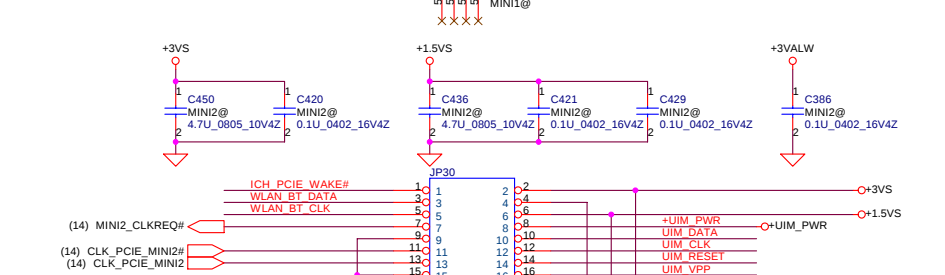
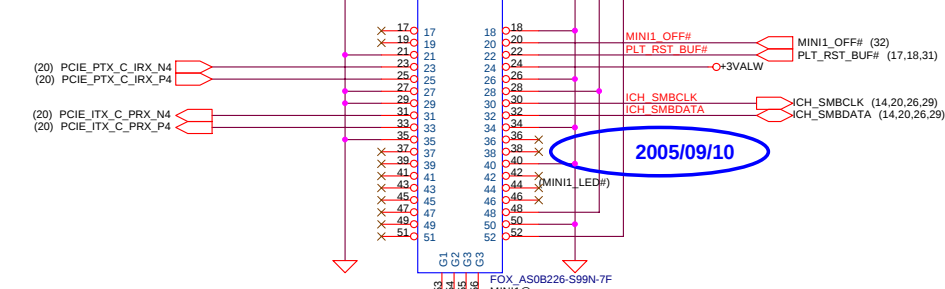
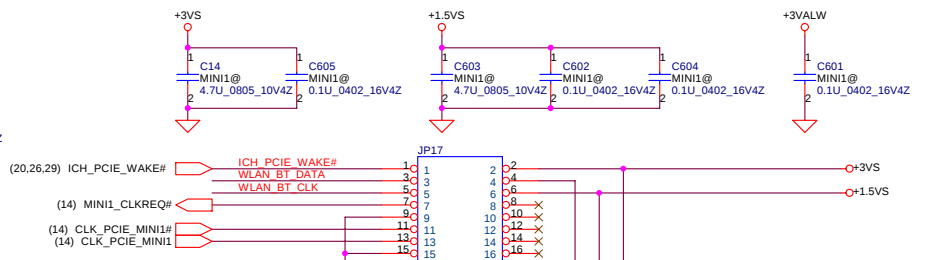
LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)



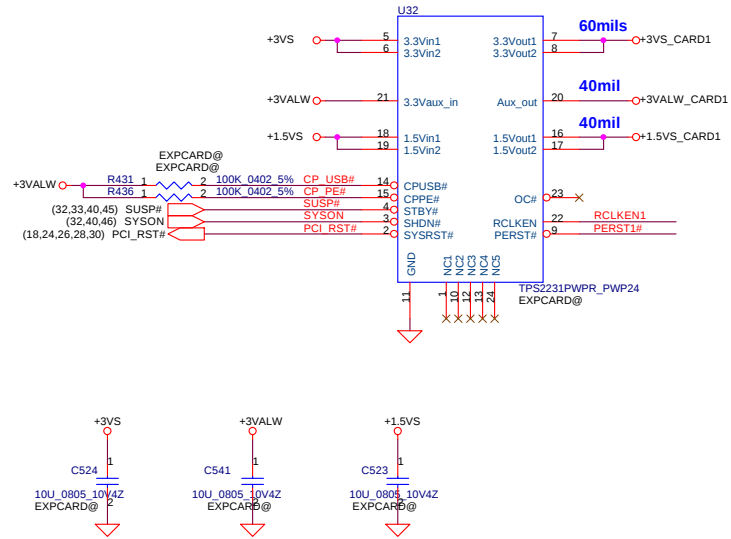
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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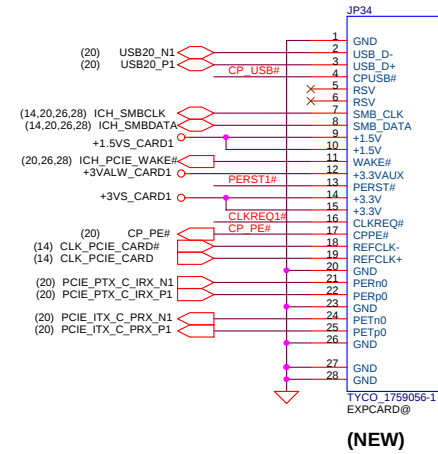
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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								Size B	Document Number						Rev 0.2
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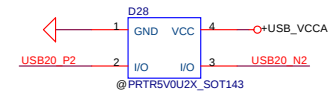
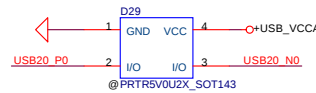
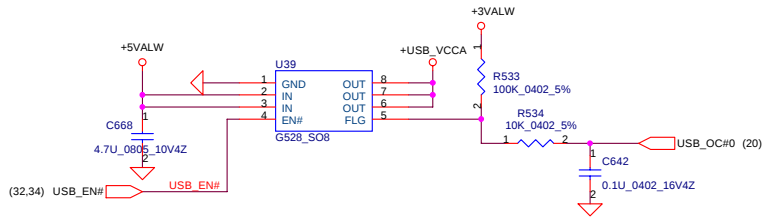
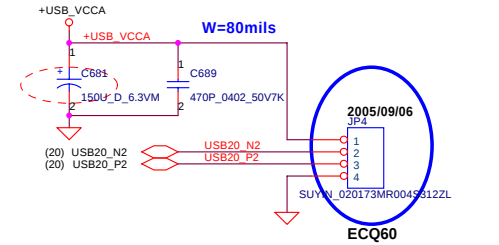
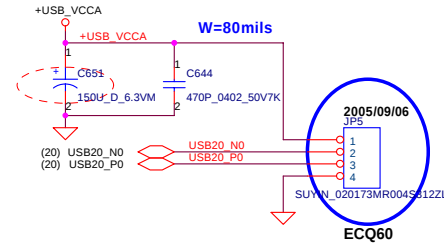
New Card Power Switch



New Card Socket (Left)



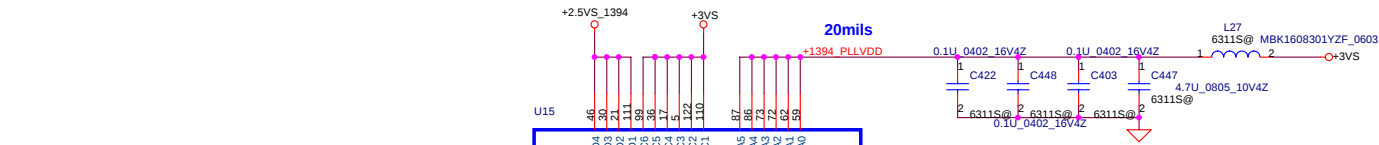
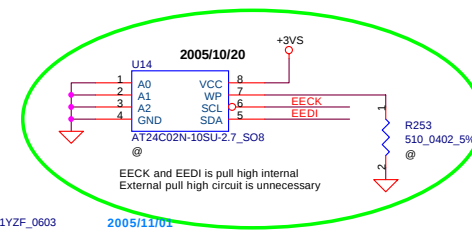
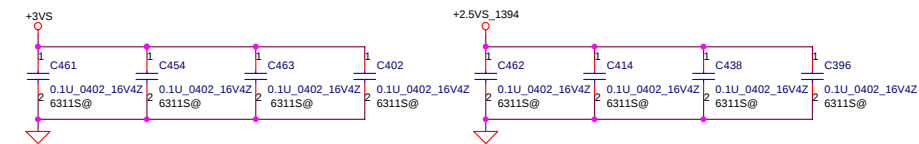
USB CONN. 1 & 2



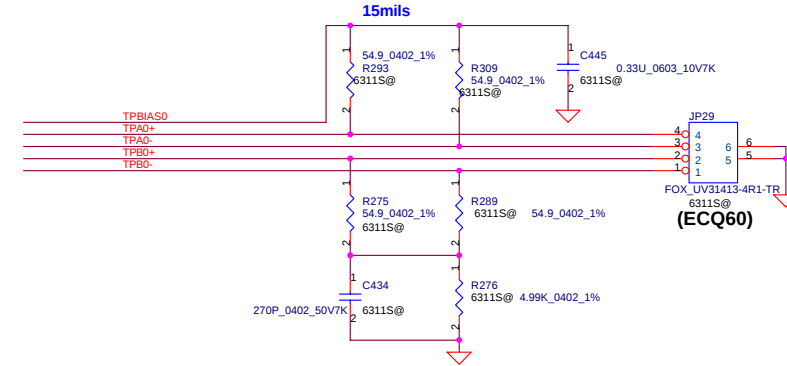
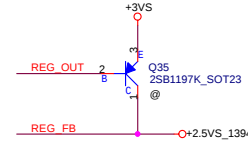
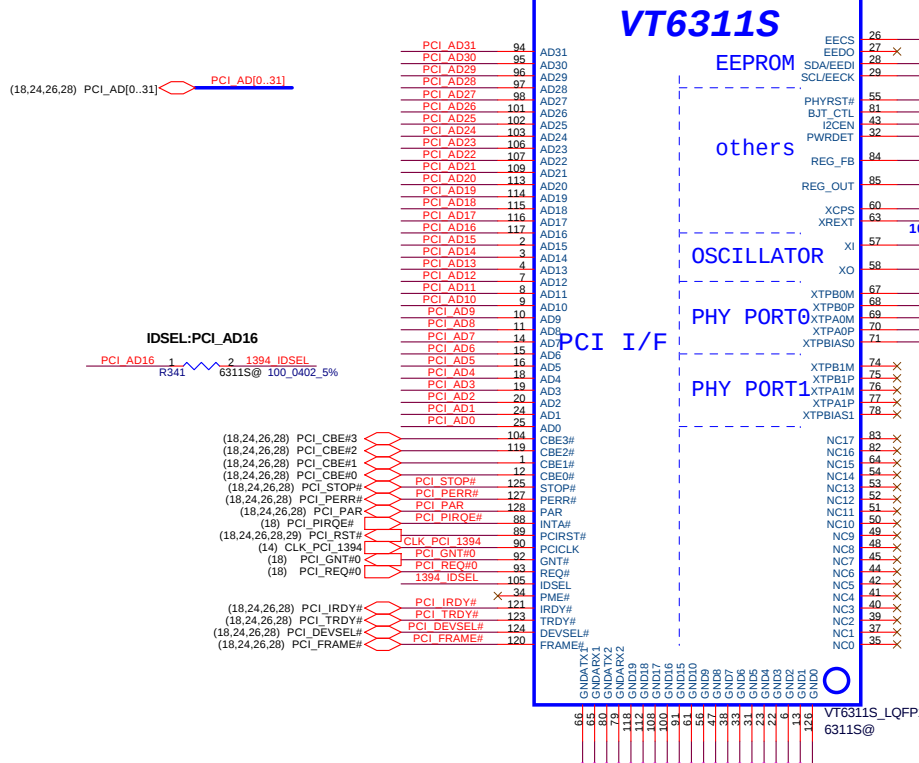
SUYIN_020173MR004G533ZR_4P

SUYIN_020173MR004G533ZR_4P

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				Size B	Document Number
				HBL51 LA-3081P	
Date: Thursday, November 10, 2005				Sheet 29	of 47



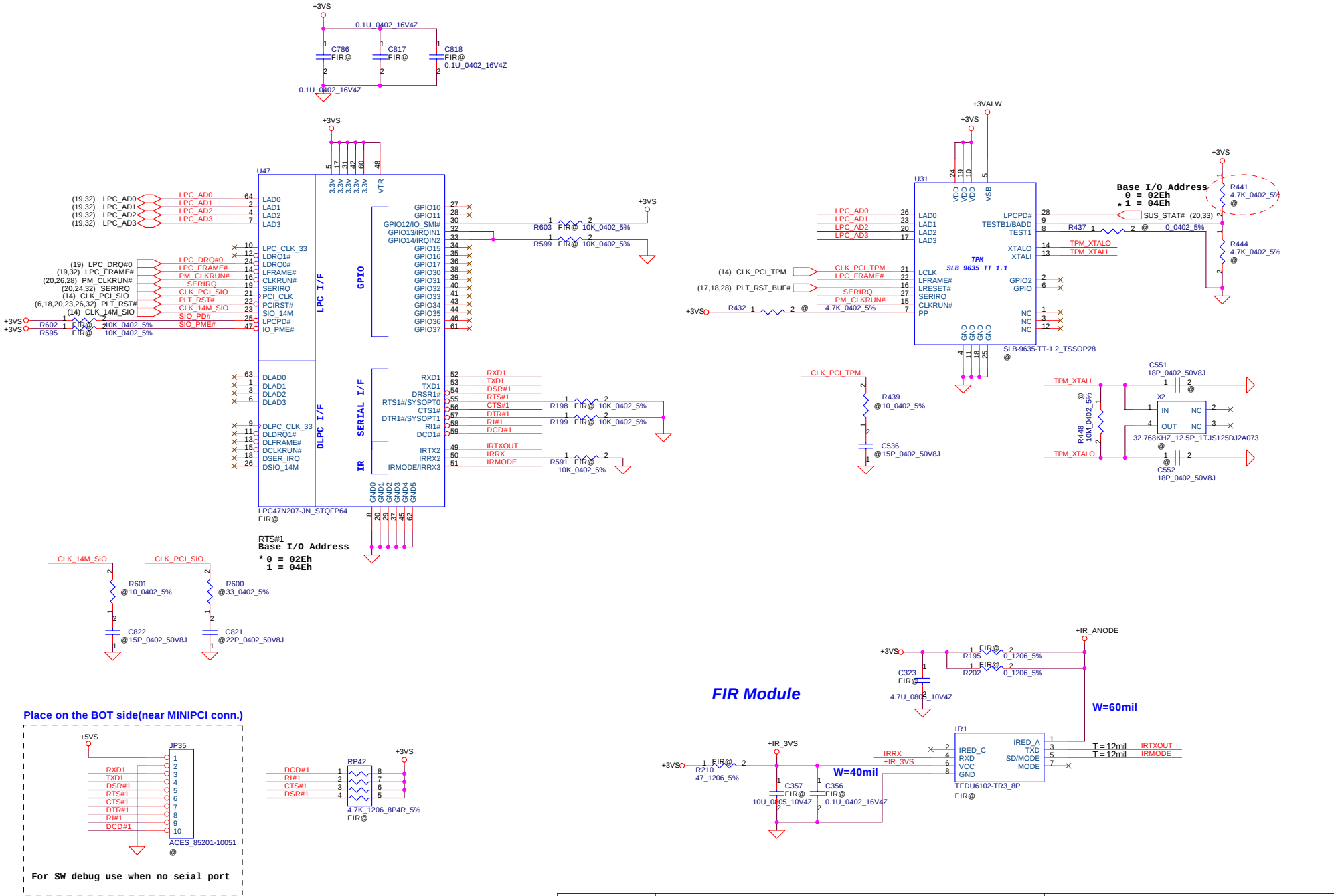
When use external EEPROM
Populate U14, R246, R253
Un-populate R261



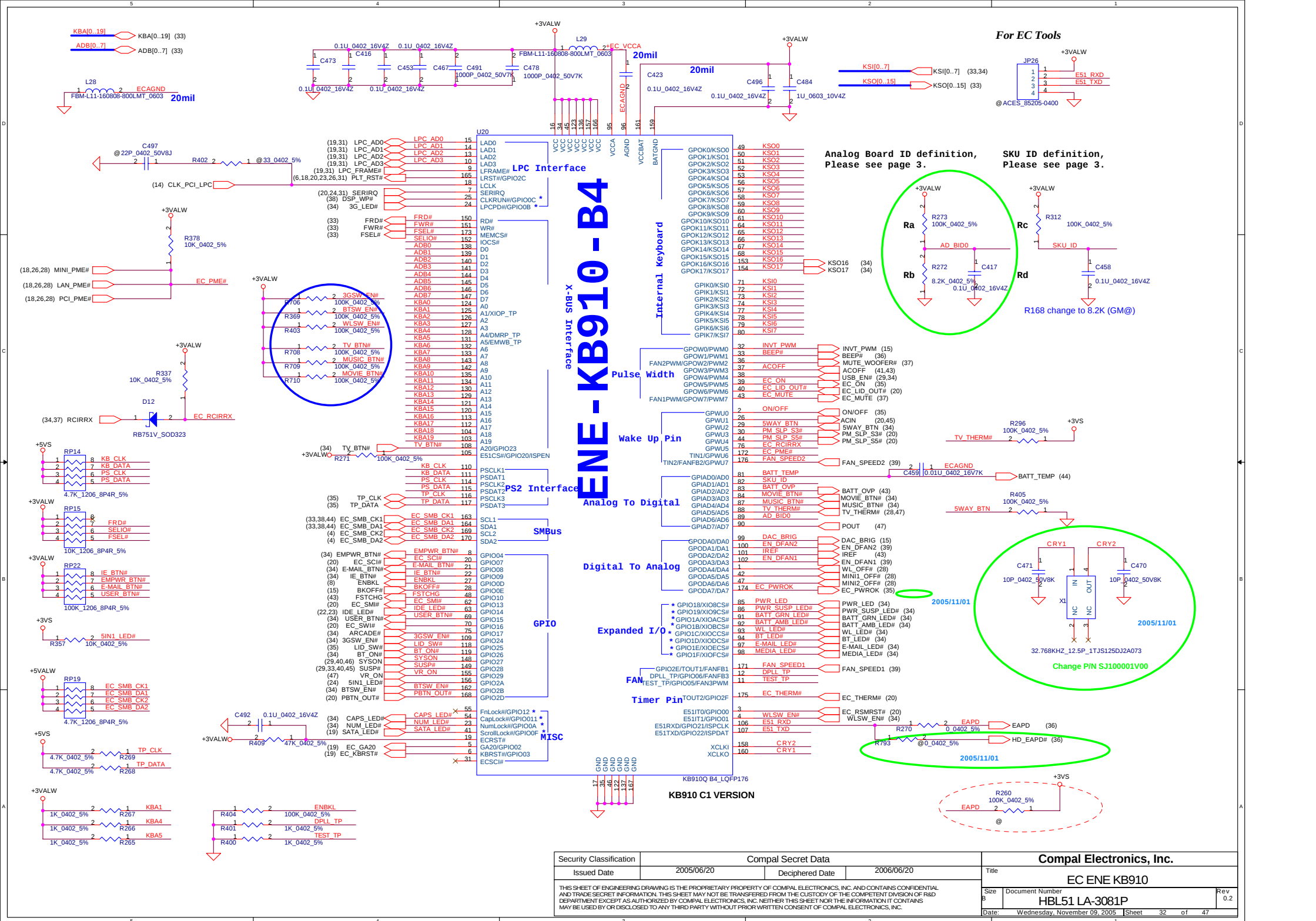
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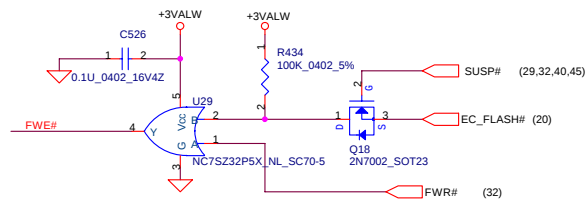
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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Size B	Document Number	HBL51 LA-3081P		Date:	Wednesday, November 09, 2005
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SUPER I/O SMsC LPC47N207

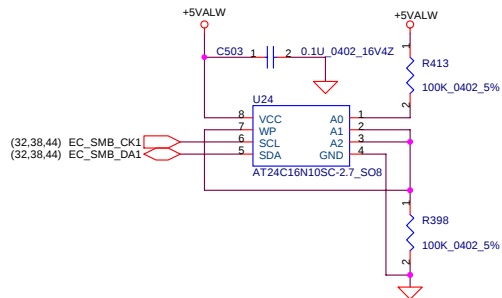


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Size B	Document Number	HBL51 LA-3081P			Rev 0.2	
Date:	Wednesday, November 09, 2005	Sheet	31	of	47	

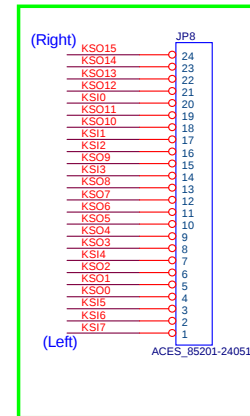
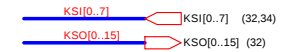




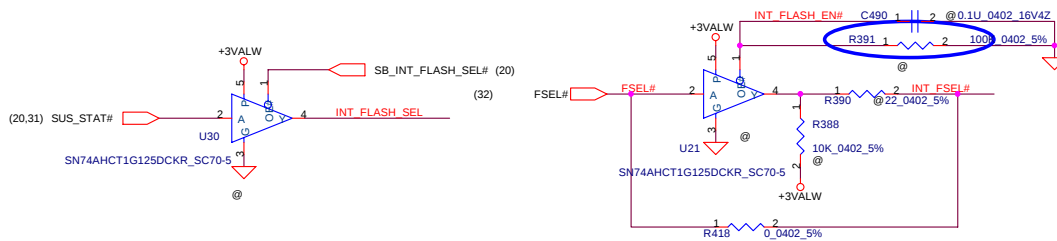
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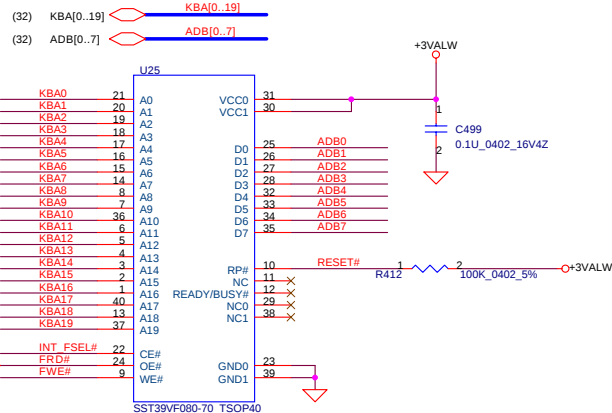
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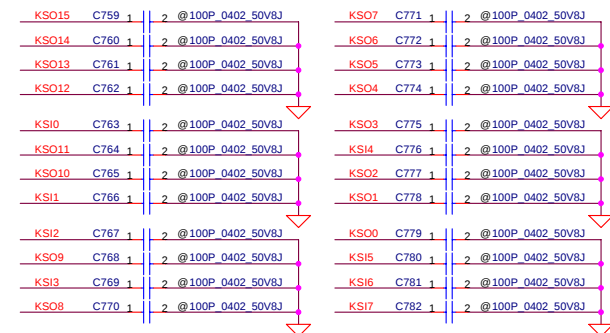
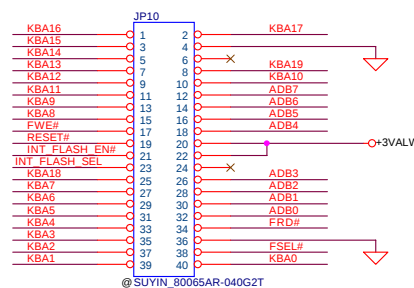
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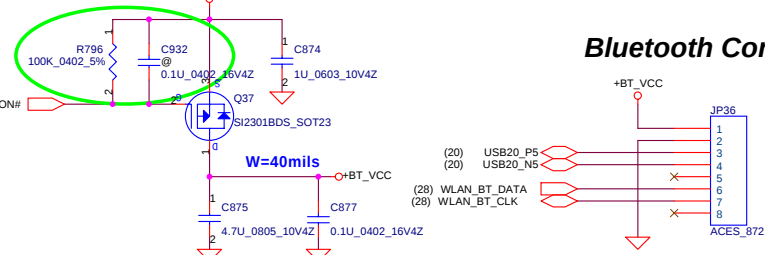
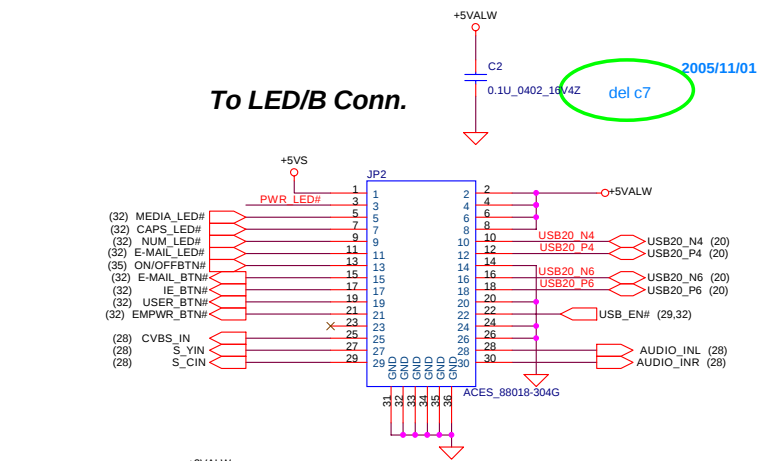
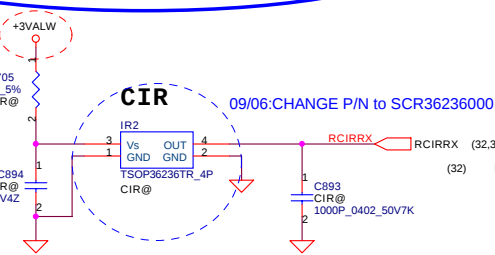
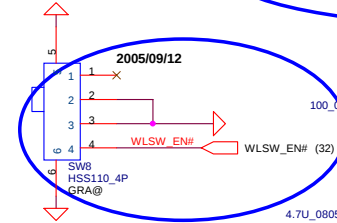
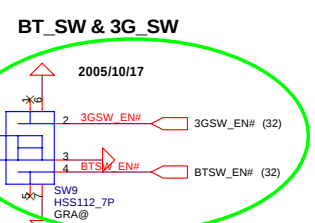
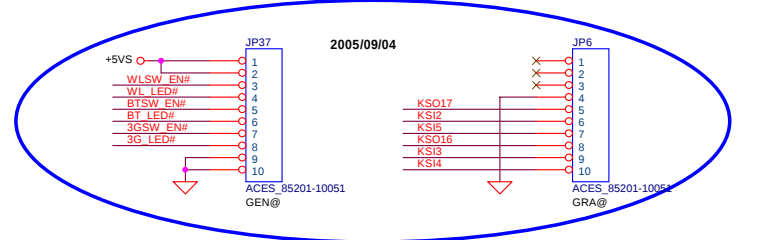
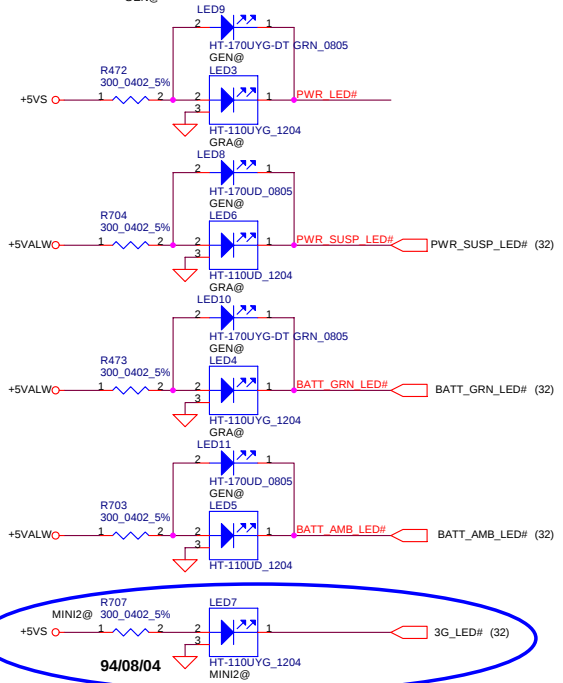
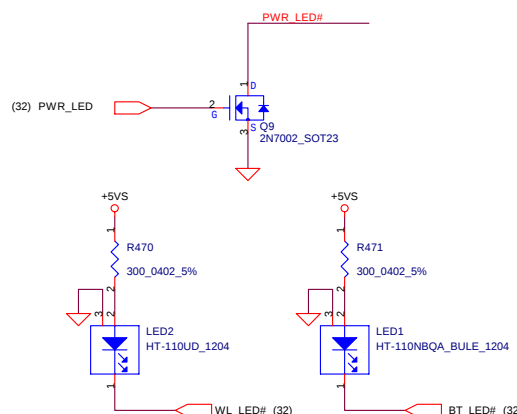
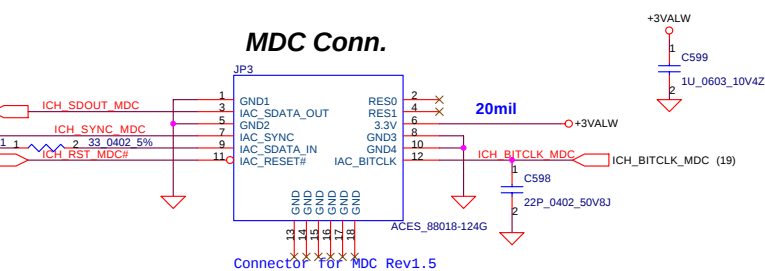
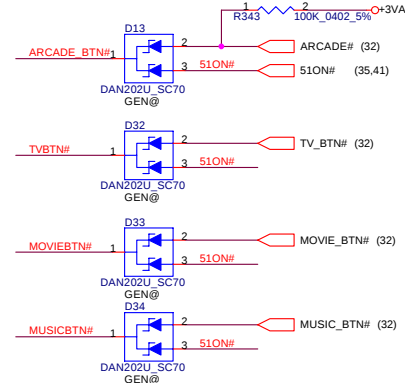
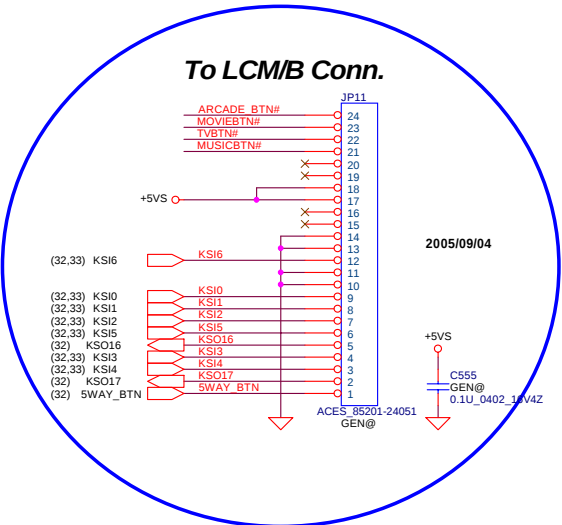
1MB Flash ROM



1MB ROM Socket

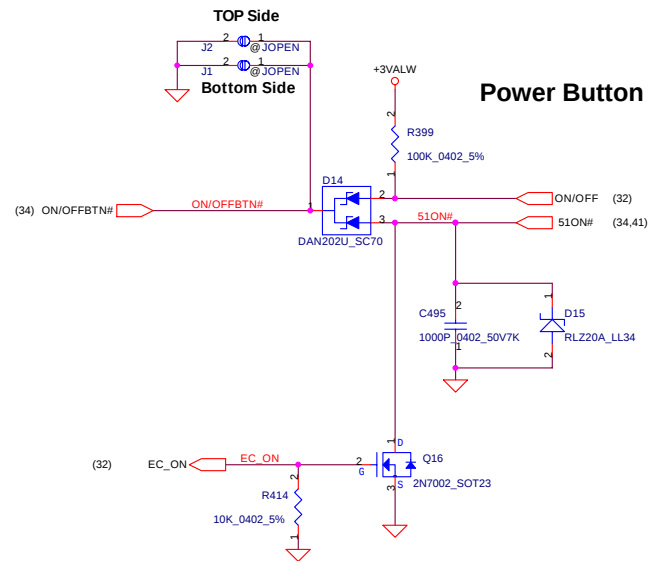


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								Document Number			
								HBL51 LA-3081P			
								Rev			
								0.2			
								Date			
								Wednesday, November 09, 2005			
								Sheet			
								33			
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								47			

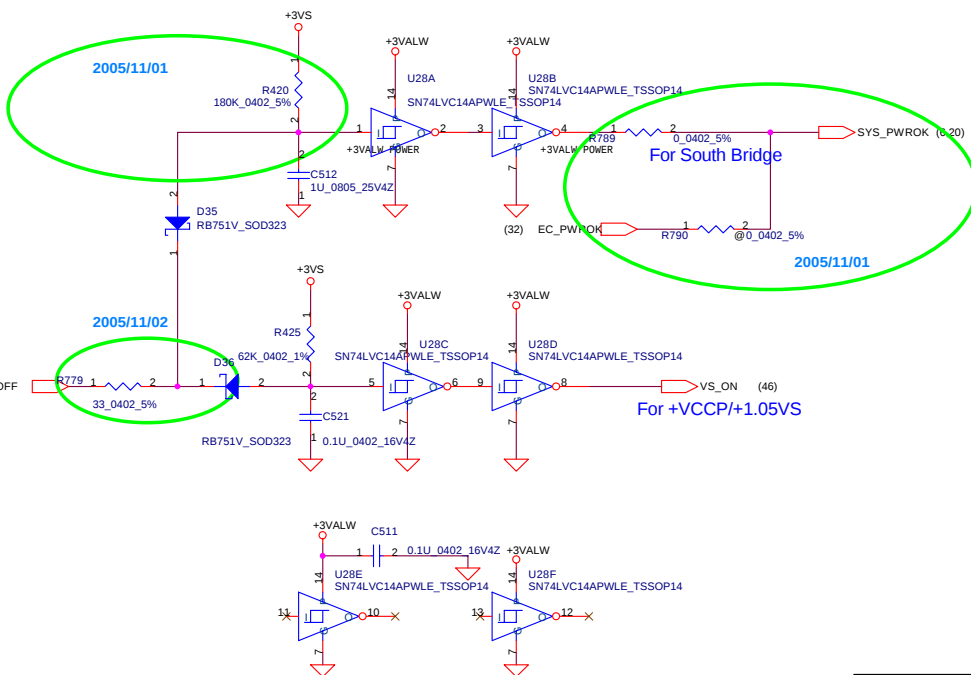


Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER			
KSI3	STOP				
KSI4	NEXT				
KSI5	REV				
KSI6		RECORD			

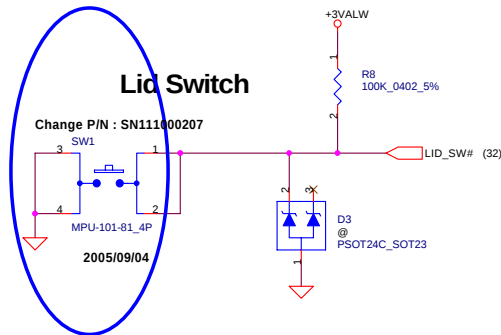
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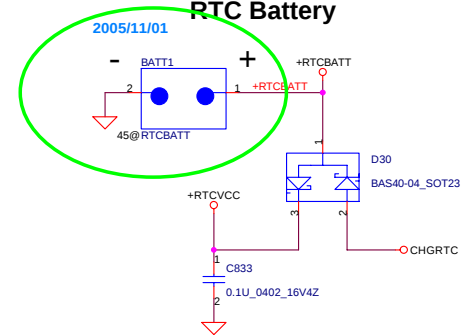
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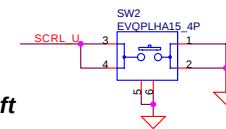
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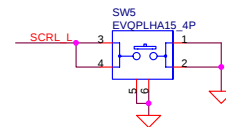
~~RTC Battery~~



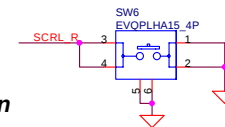
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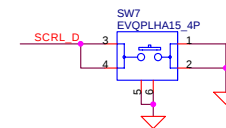
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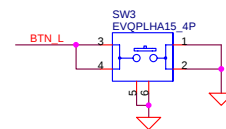
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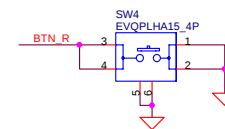
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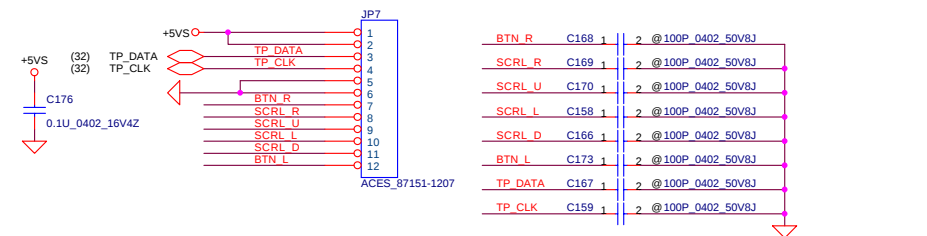
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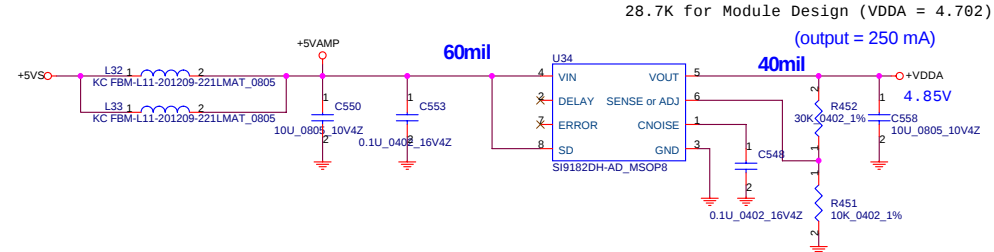
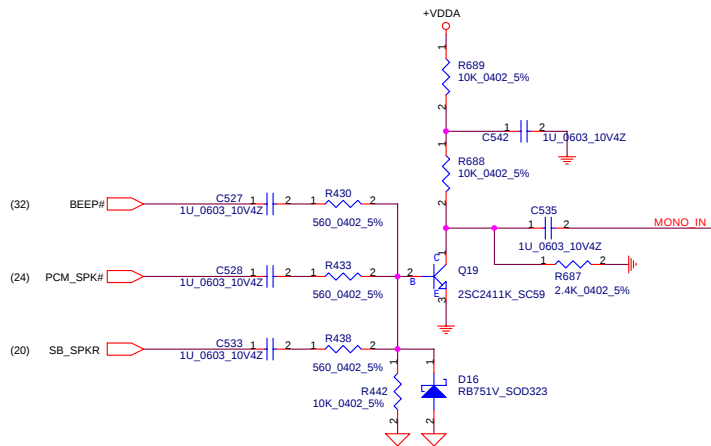
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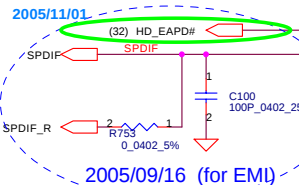
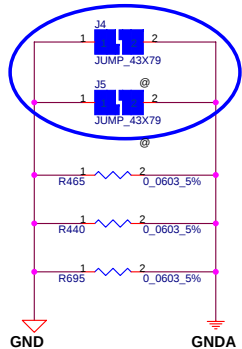
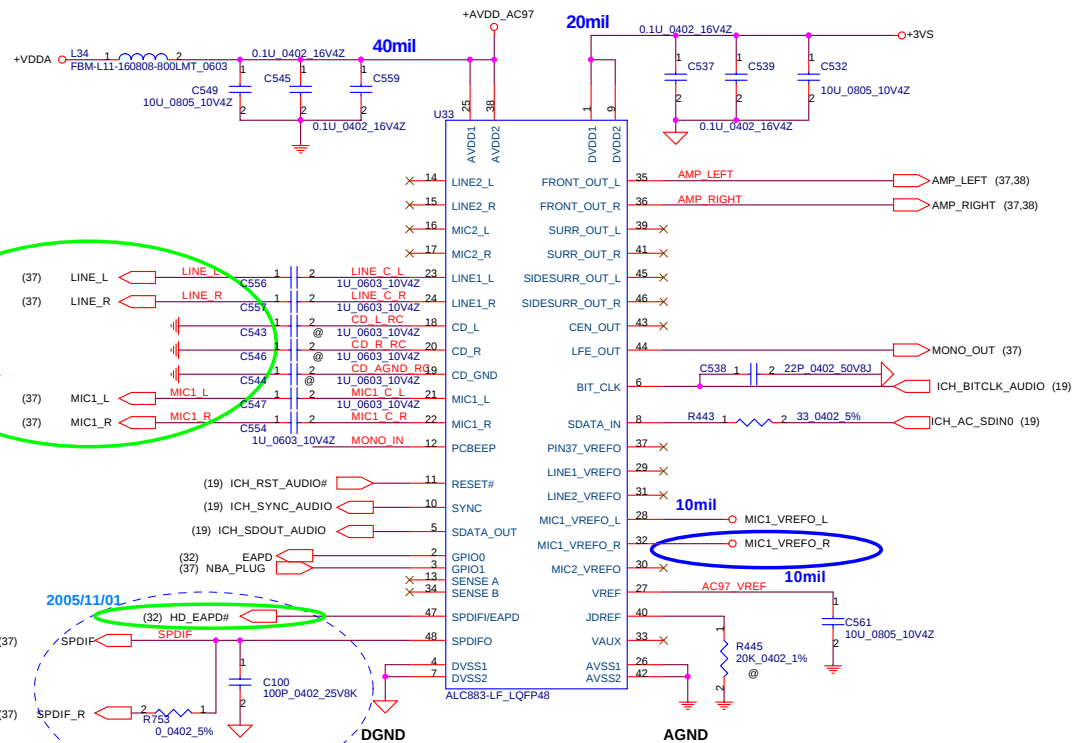
To TP/B Conn.



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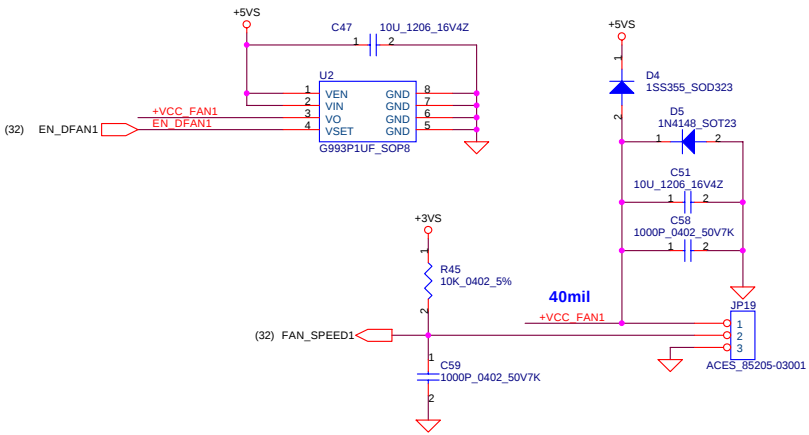


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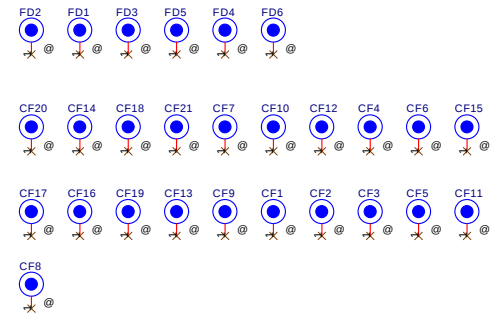
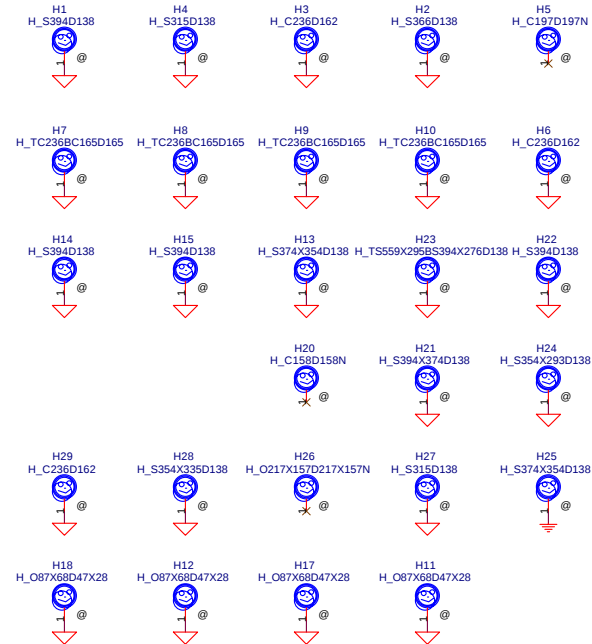
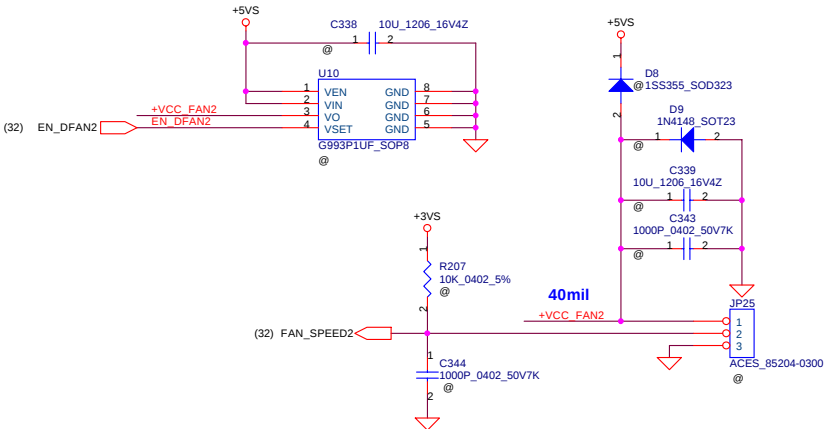


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FAN1 Conn

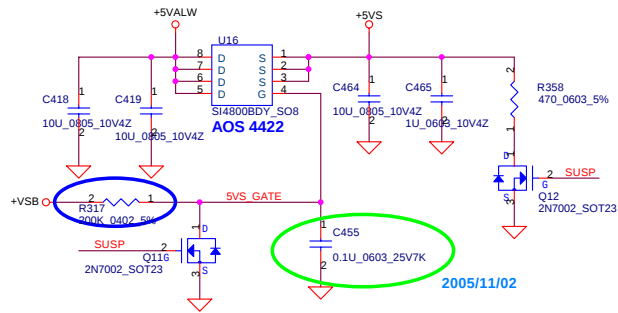


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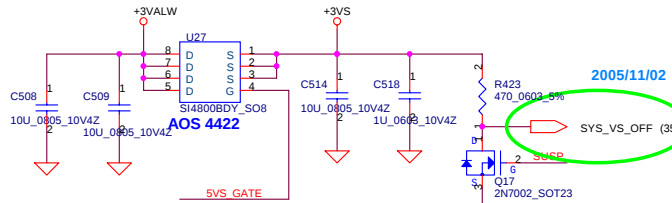


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Size	B	Document Number	HBL51 LA-3081P	Rev	0.2	
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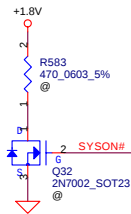
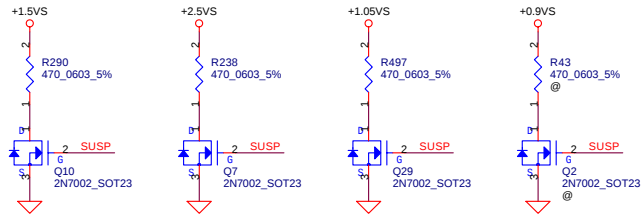
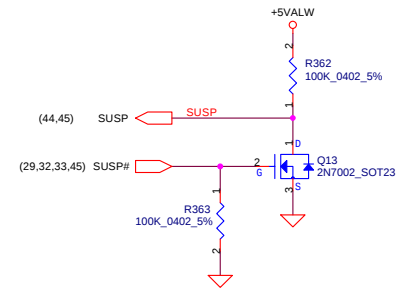
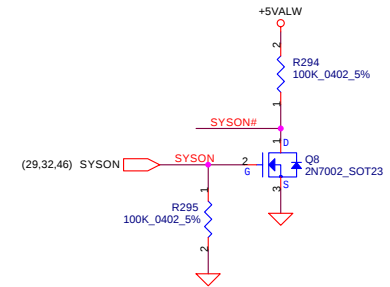
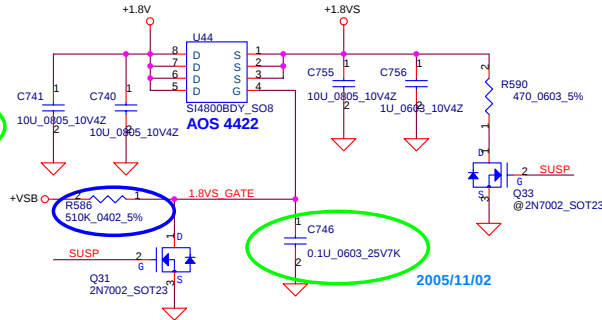
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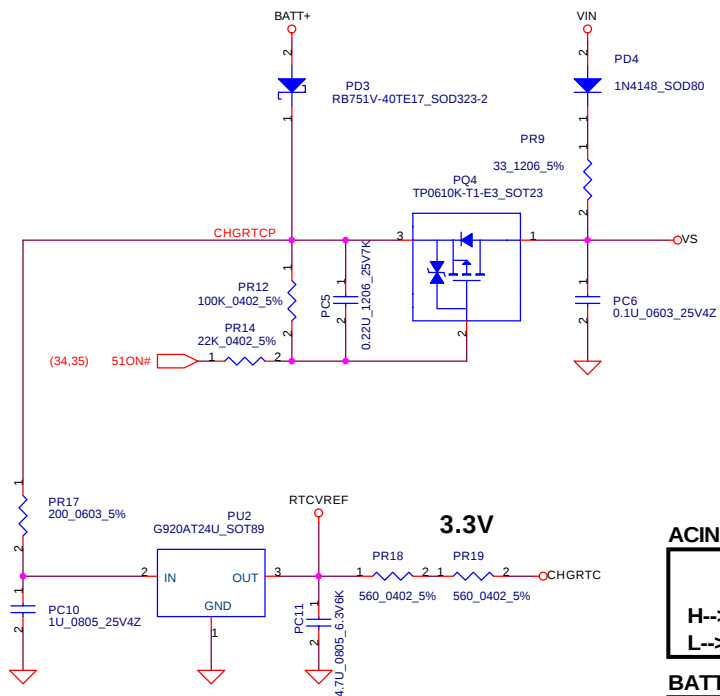
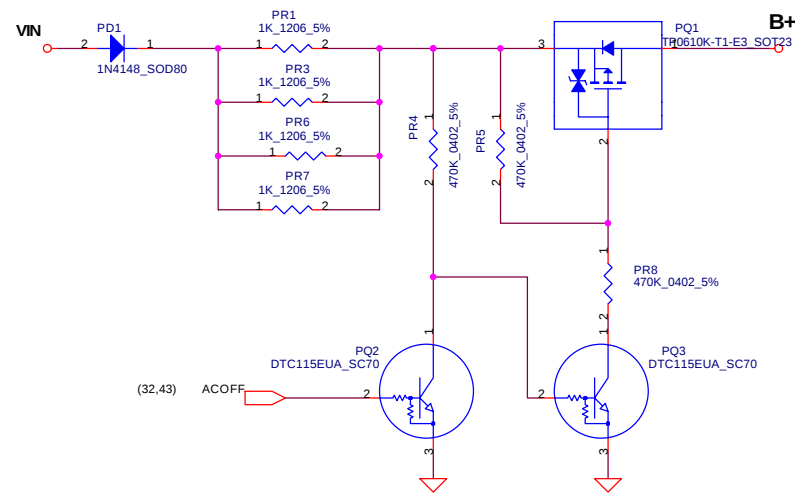
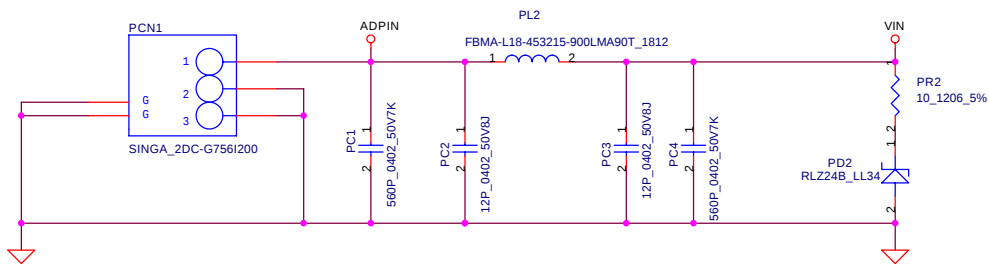
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+1.8V to +1.8VS

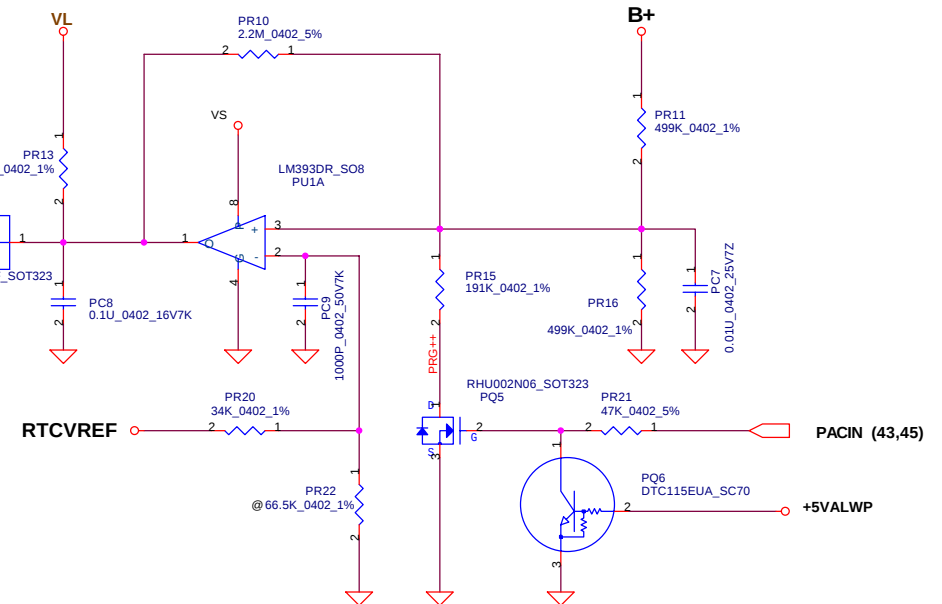


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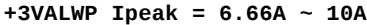


ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

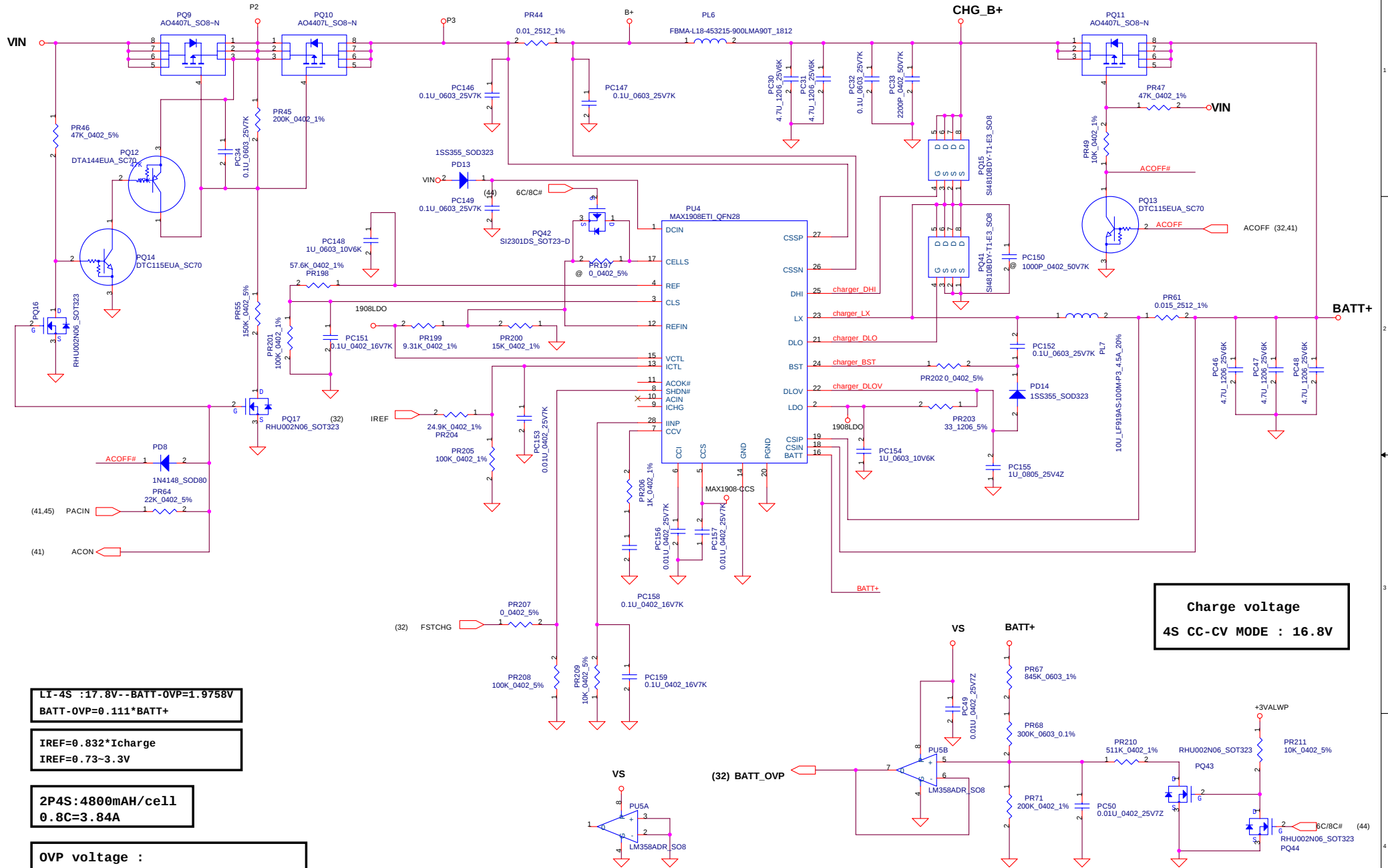
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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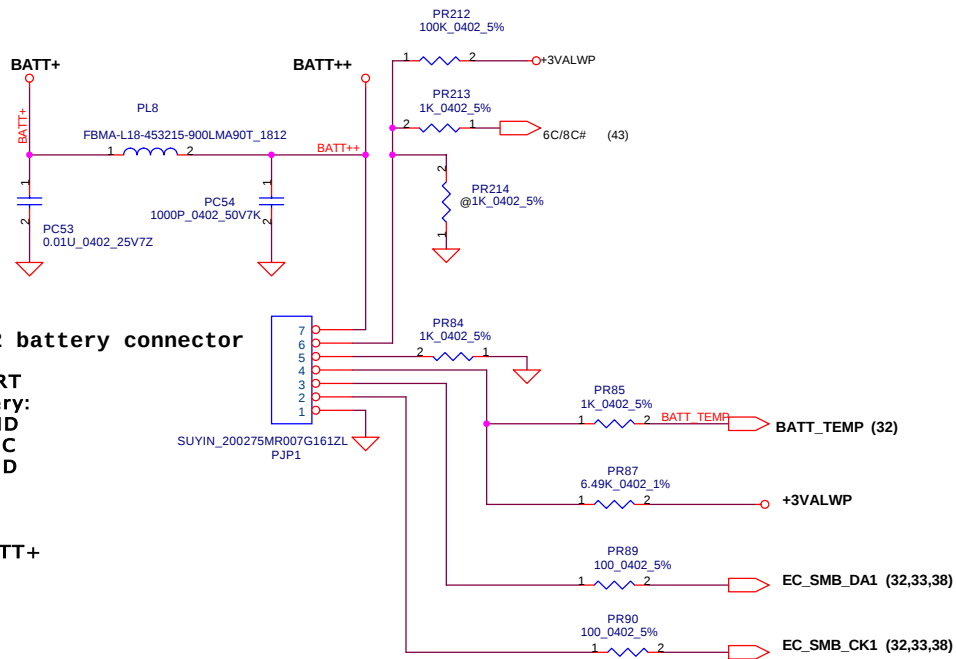
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I_{adp}=0~4.74A(90W)

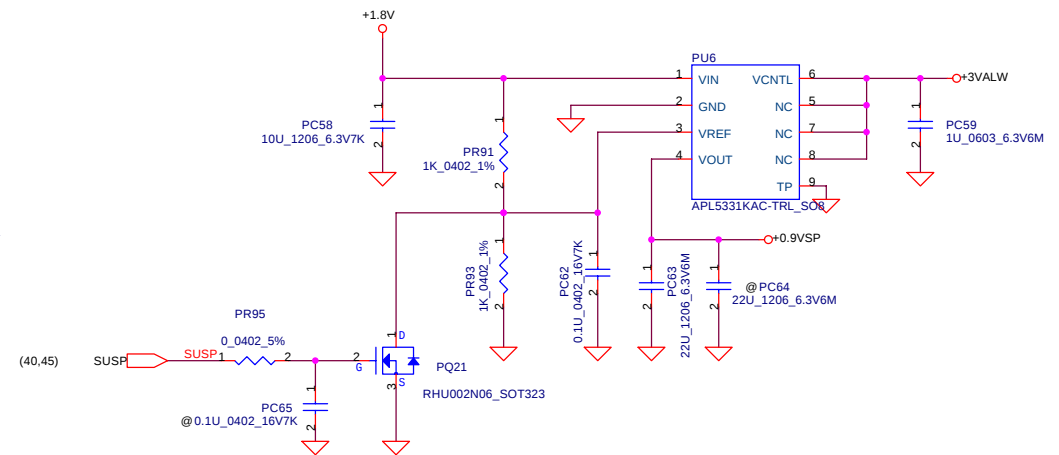
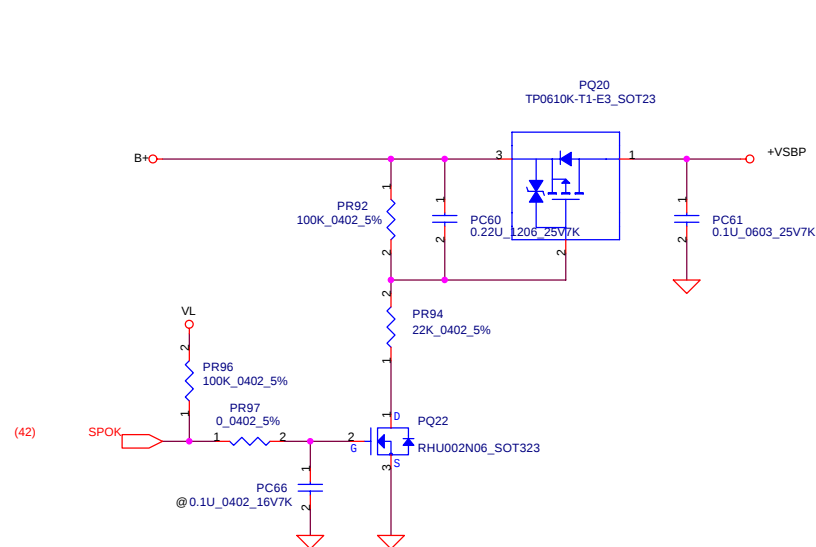
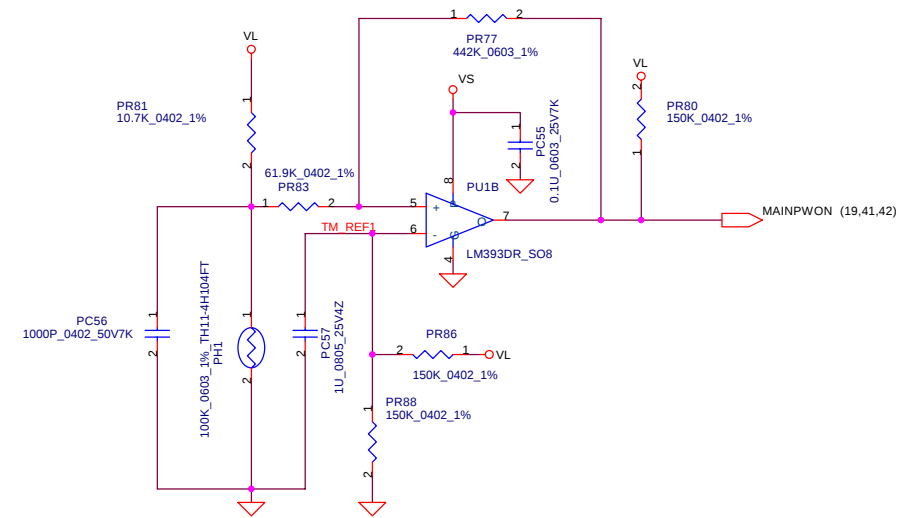
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	Charger
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PJP2 battery connector

SMART Battery:
 1.GND
 2.SMC
 3.SMD
 4.TS
 5.B/I
 6.ID
 7.BATT+

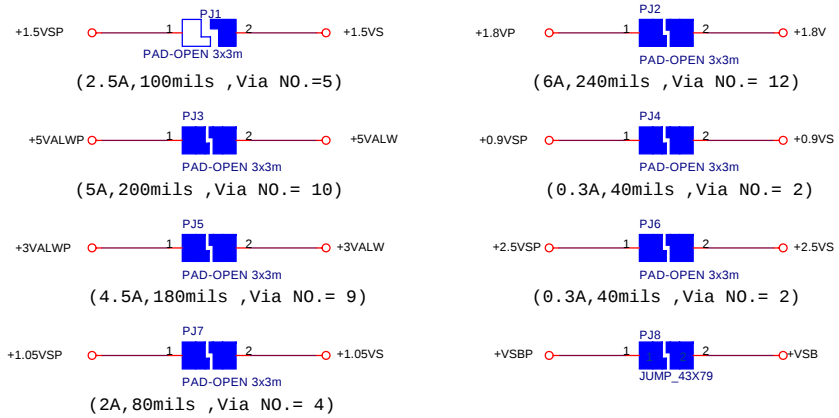


PH1 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

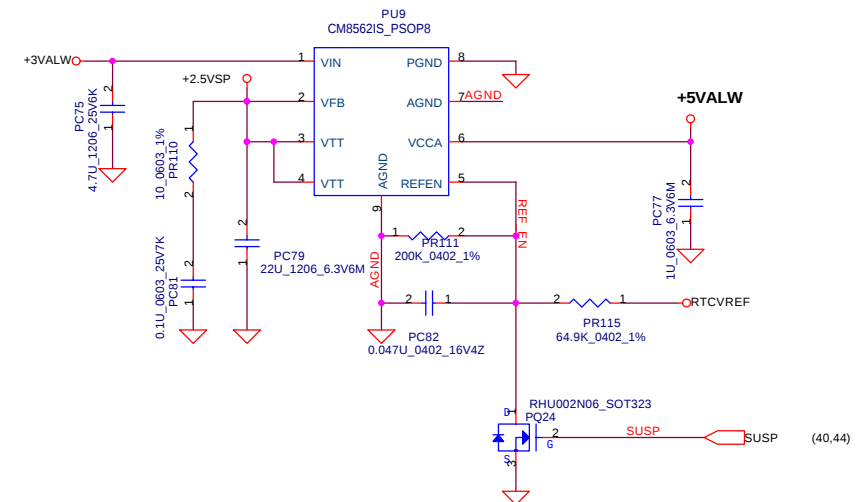
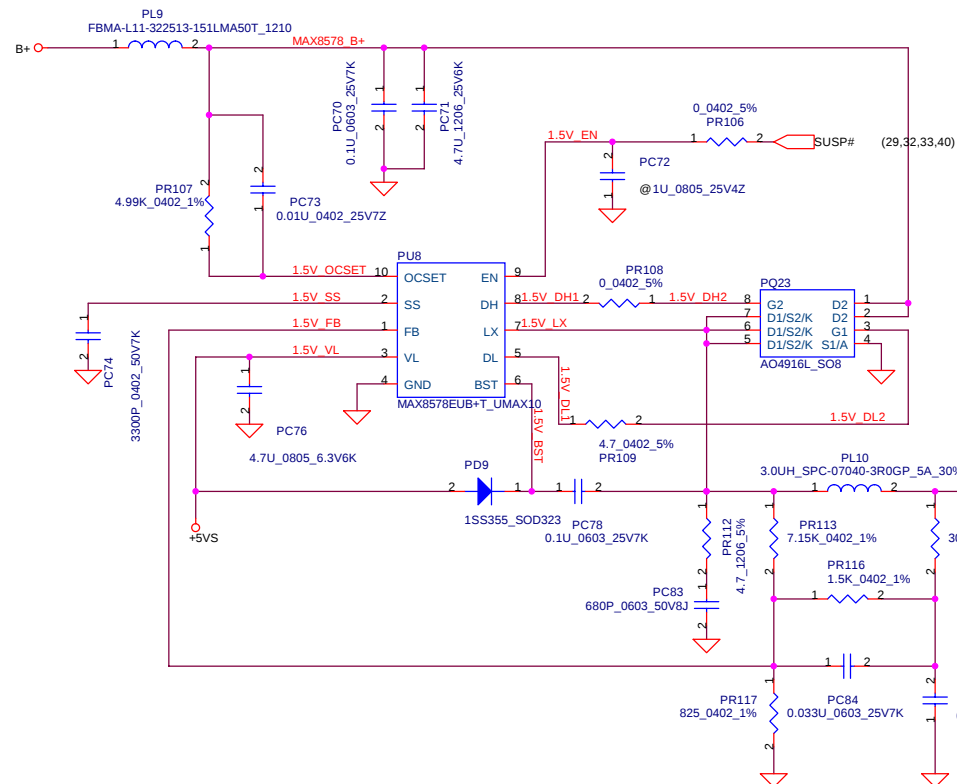
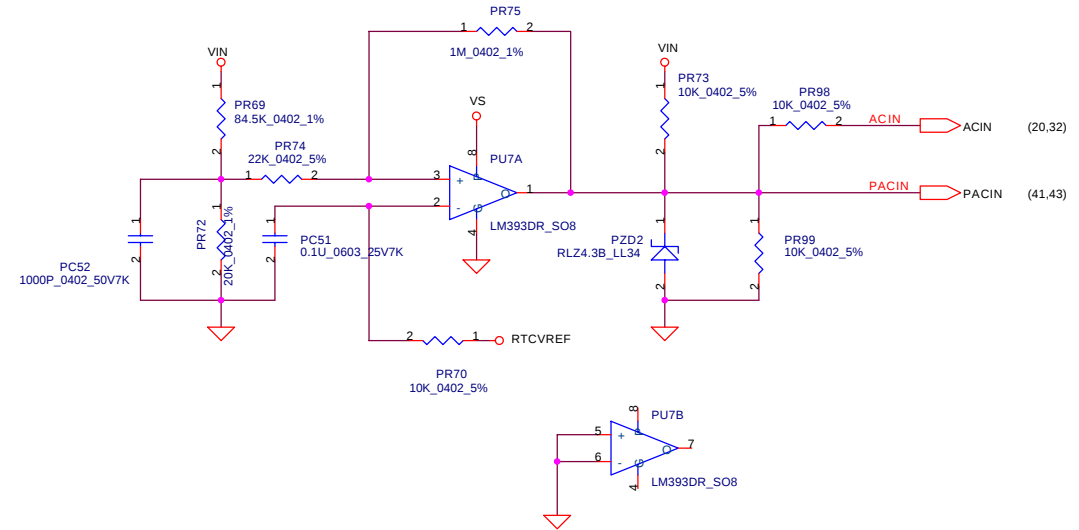


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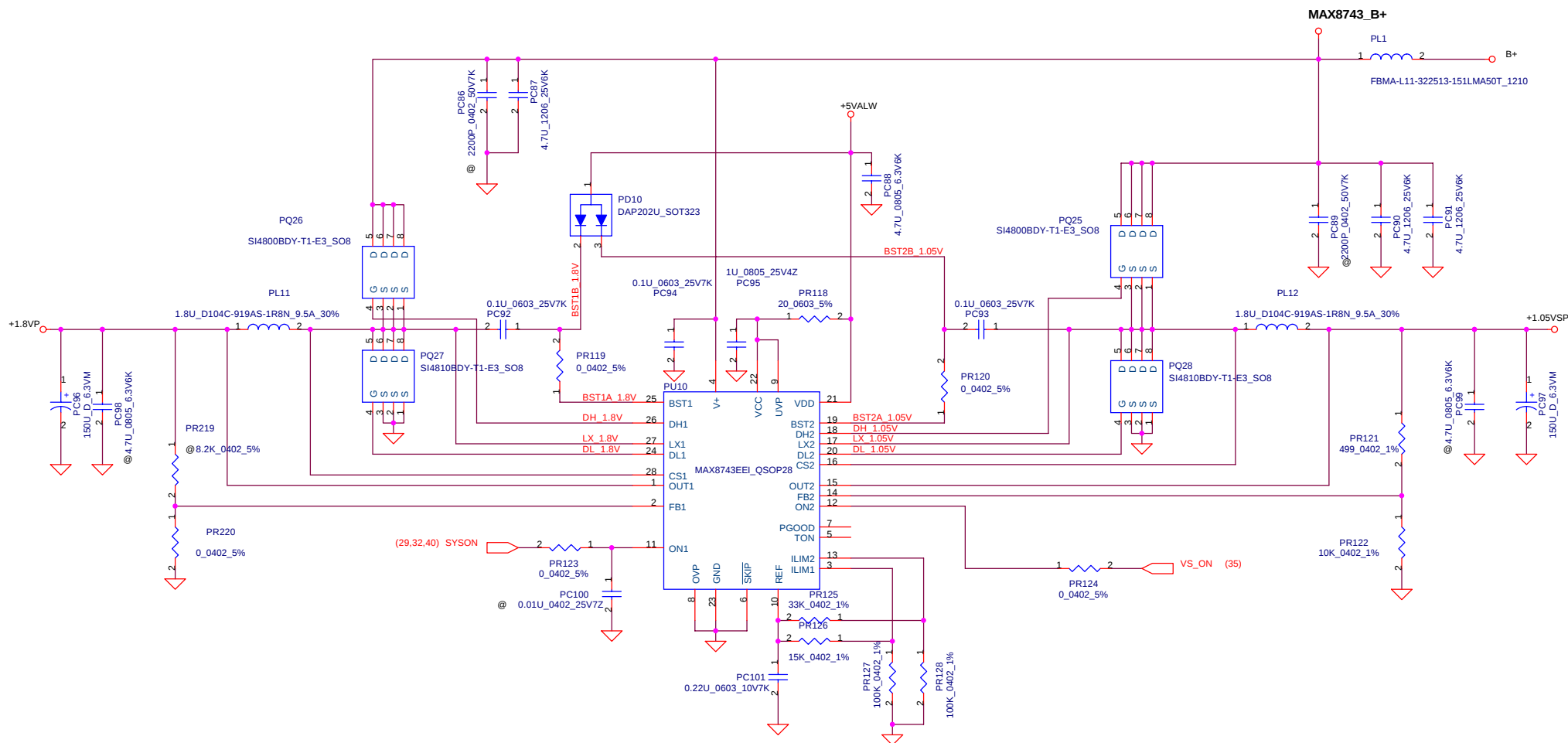
AC Adapter Detector



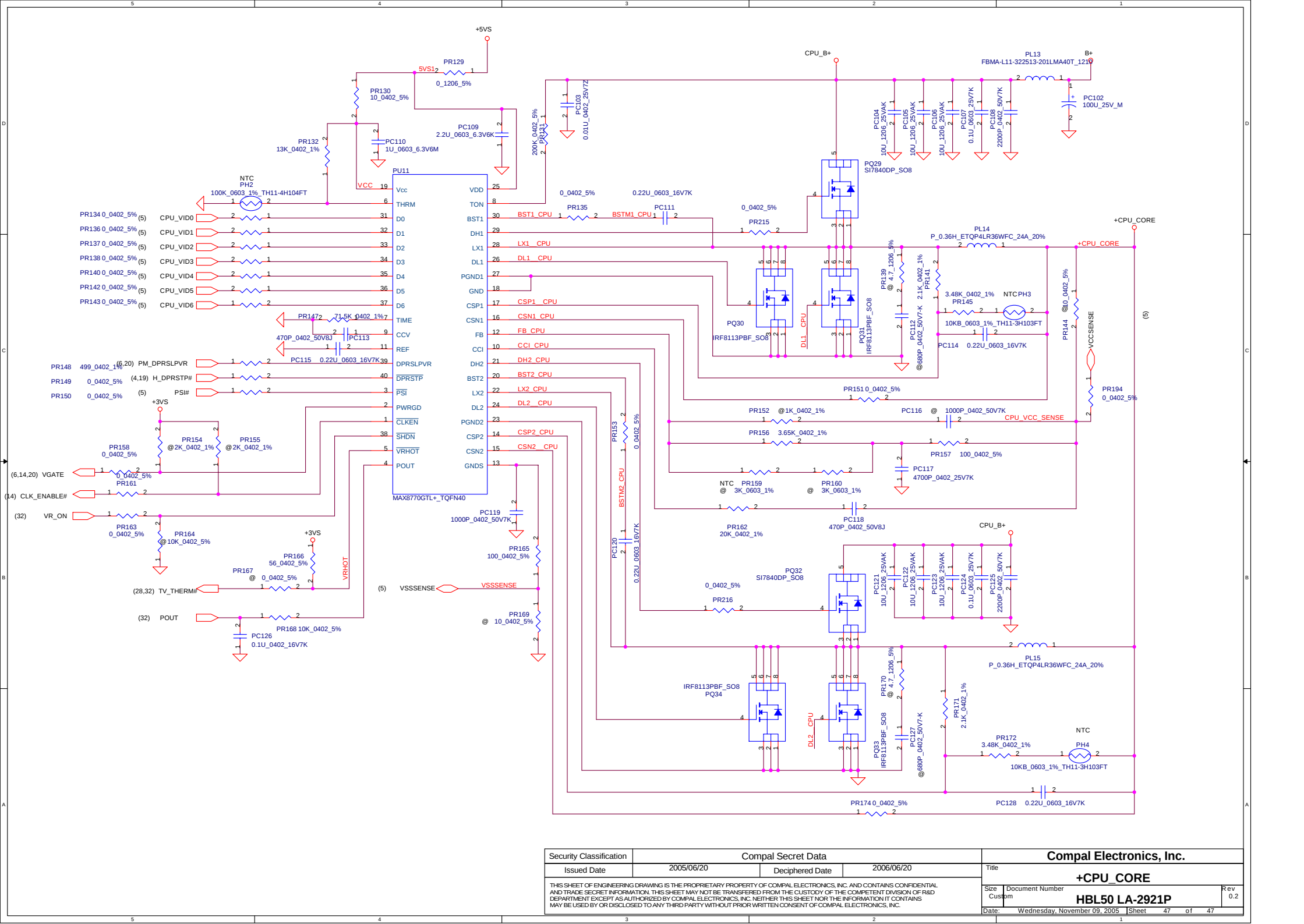
Vin Detector
17.90V/17.24V



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