NDU00/NDU10

Streamline-S 11.6"

Streamline-M 13.3"

LA-6031P REV 1.0 Schematic

Intel Arrandale SFF/IBEX PEAK

2010-04-12 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

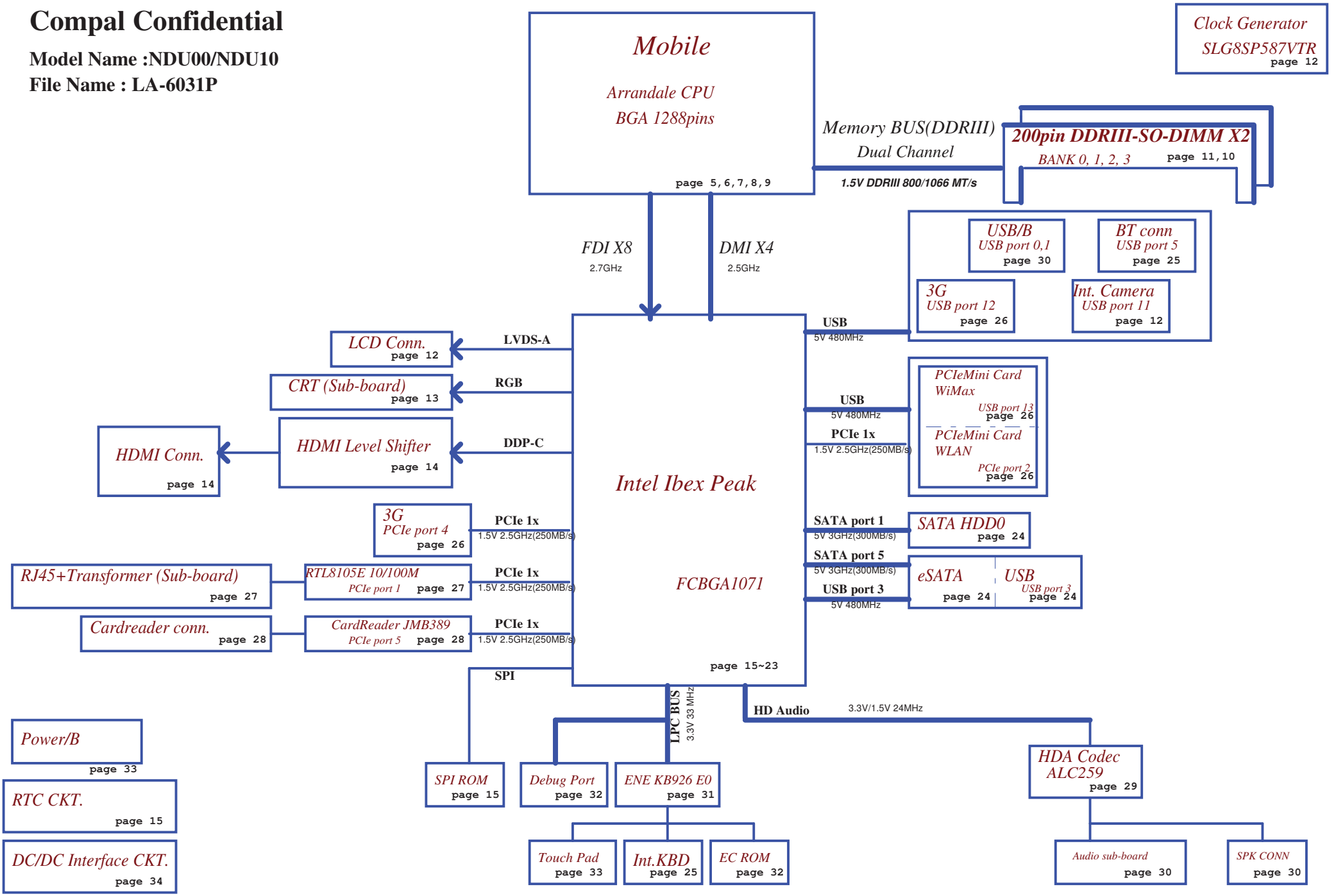
Title: **Cover Page**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 1 of 45

Compal Confidential

Model Name :NDU00/NDU10
File Name : LA-6031P



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

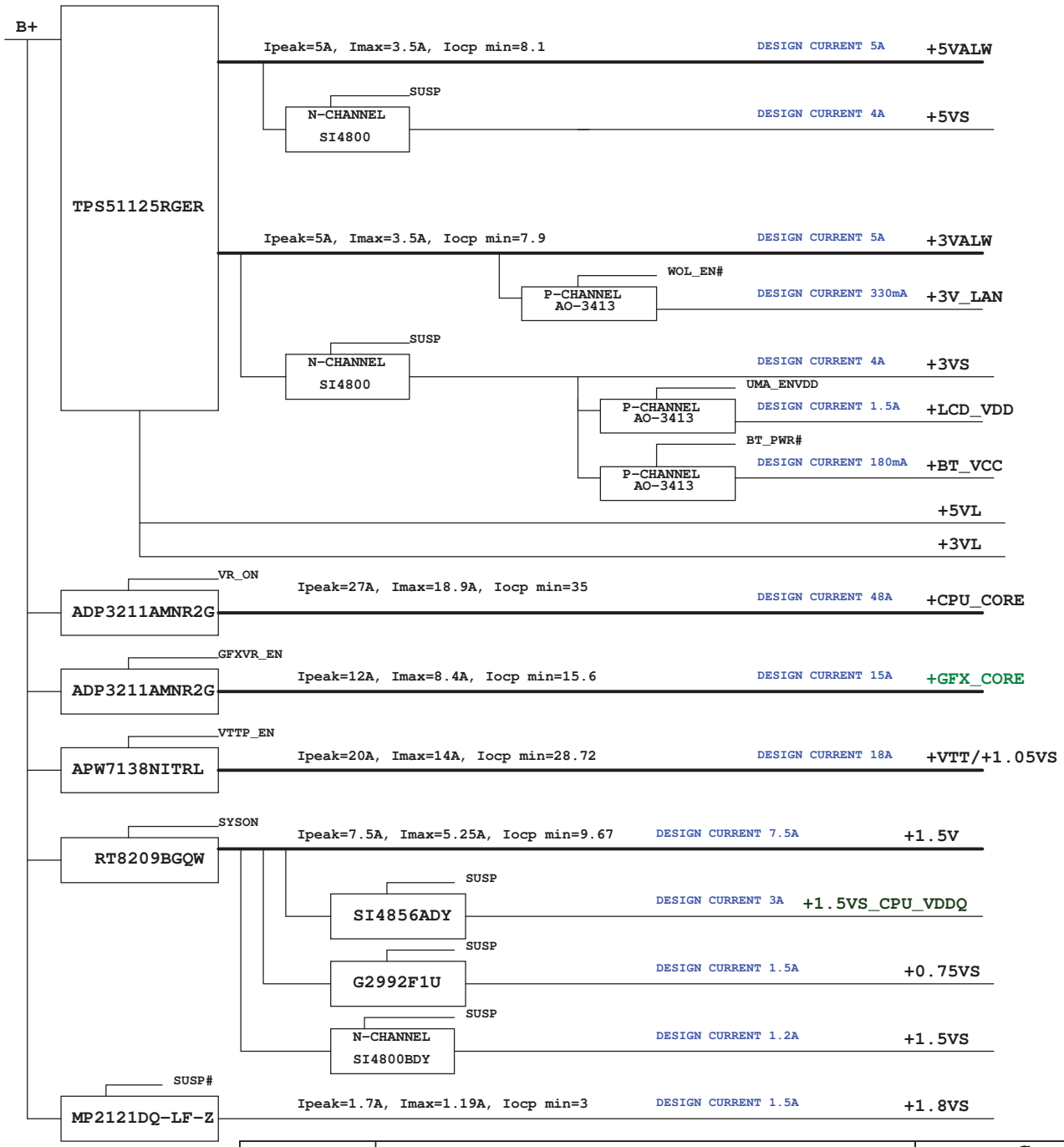
Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 2 of 45

NSWAA Liverpool Intel Arrandale
NTWAA Sunderland Intel Arrandale



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **Power Tree**

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 3 of 45

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B +5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +GFX_CORE +CPU_CORE +VTT +0.75VS +1.8VS +1.5VS_CPU_VDDQ
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	HDMI	3G	Mini Card	Mini Card	Gensor	
						main	2nd
explain	Bluetooth	HDMI	3G	WIRELESS	WIMAX	R5F211B4D31SP	R5F211B4D34SP
BTO	BT@	IHDMI@	3G@	WLAN@	WIMAX@	GSENSOR@ 1STGSENSOR@ 1ST@	GSENSOR@ 2NDGSENSOR@ 2ND@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D3	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	Gensor	
+3VS	PCH	0100 110x b

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN/Wimax/3G	

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

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Layout rule : 10mil width
trace length < 0.5",
spacing 20mil

U1B

Misc
Clocks
Thermal
DDR3 Misc
Power Management
JTAG & MBP

COMP3 COMP2 COMP1 COMP0 PROC_DETECT CATERR# PECI PROCHOT# THERMTRIP# RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK VTTPWRGOOD TAPPWRGOOD RSTIN#

INTEL_ARRANDALE_1288

Design guide
1.11update,PLTRST series
resittor 1.5K, PL
resistor 750 ohm

12/22 follow NWQAA

DDR3 Compensation Signals
Layout Note:Please these
resistors near Processor

Routed as a single daisy chain

EMI reverse, close to CPU

For S3 CPU power saving

JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

For S3 CPU power saving

PMEG2010AEH_SOD123
SN74AHC1G08DCKR_SC70-5

12/22 follow NWQAA

XDP Connector

JXDP1
SAMTE_BSH-030-01-L-D-A

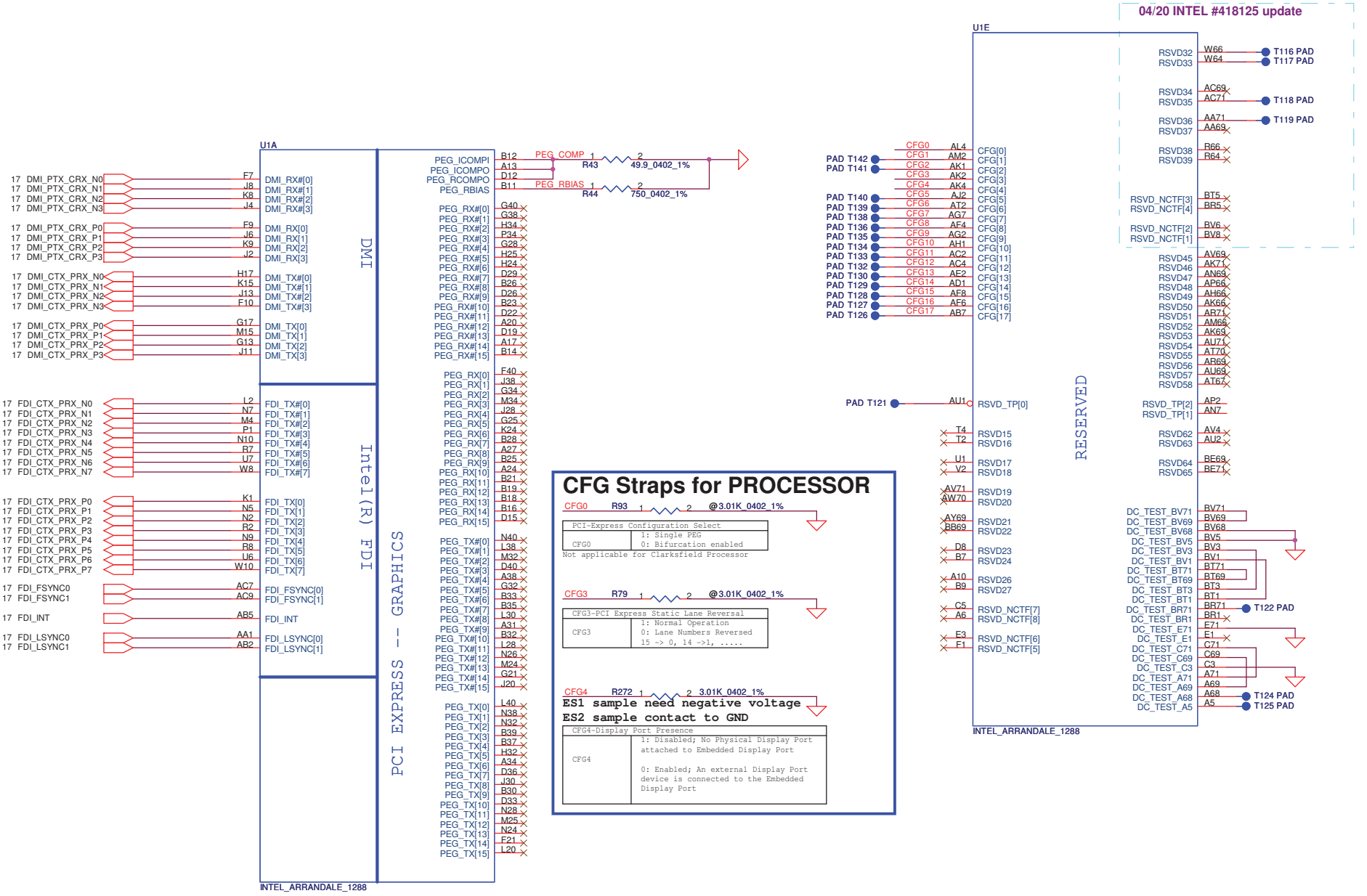
Security Classification	Compal Secret Data	
Issued Date	2010/04/12	Deciphered Date: 2010/01/23

Compal Electronics, Inc.

Title: CPU CLK/MISC/JTAG

Size: Custom | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 5 of 45



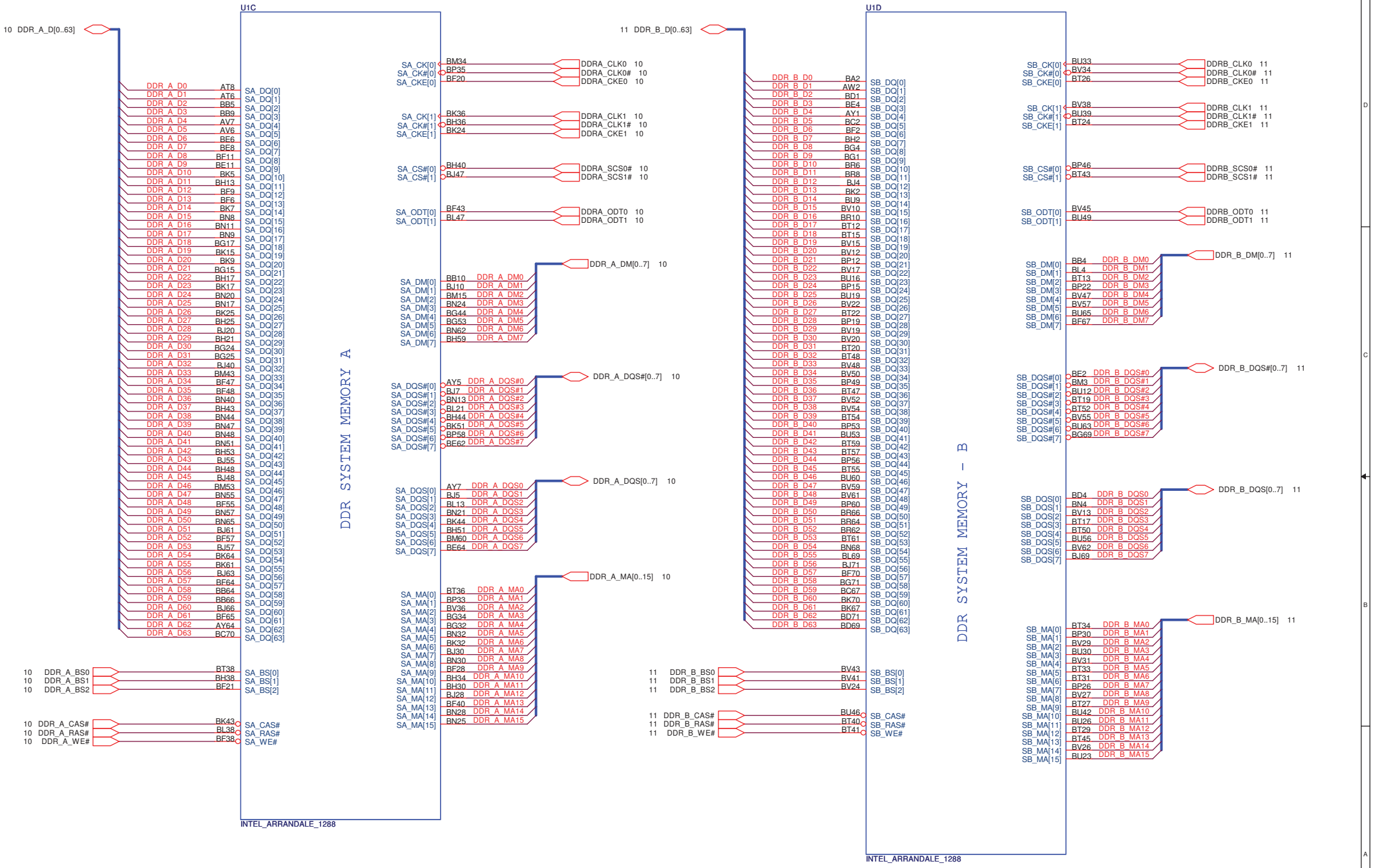
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CPU DMI/FDI/PEG**

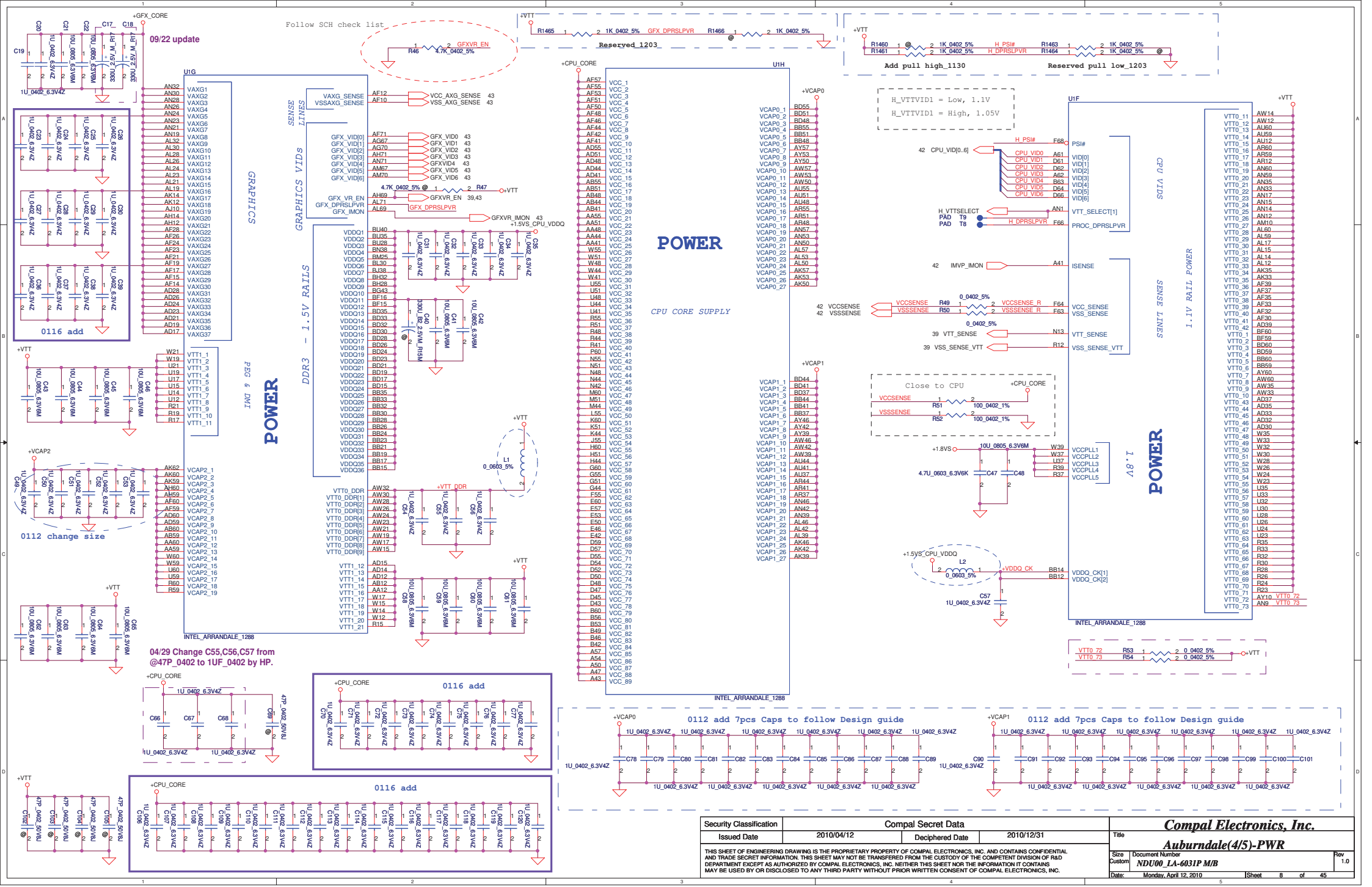
Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 6 of 45



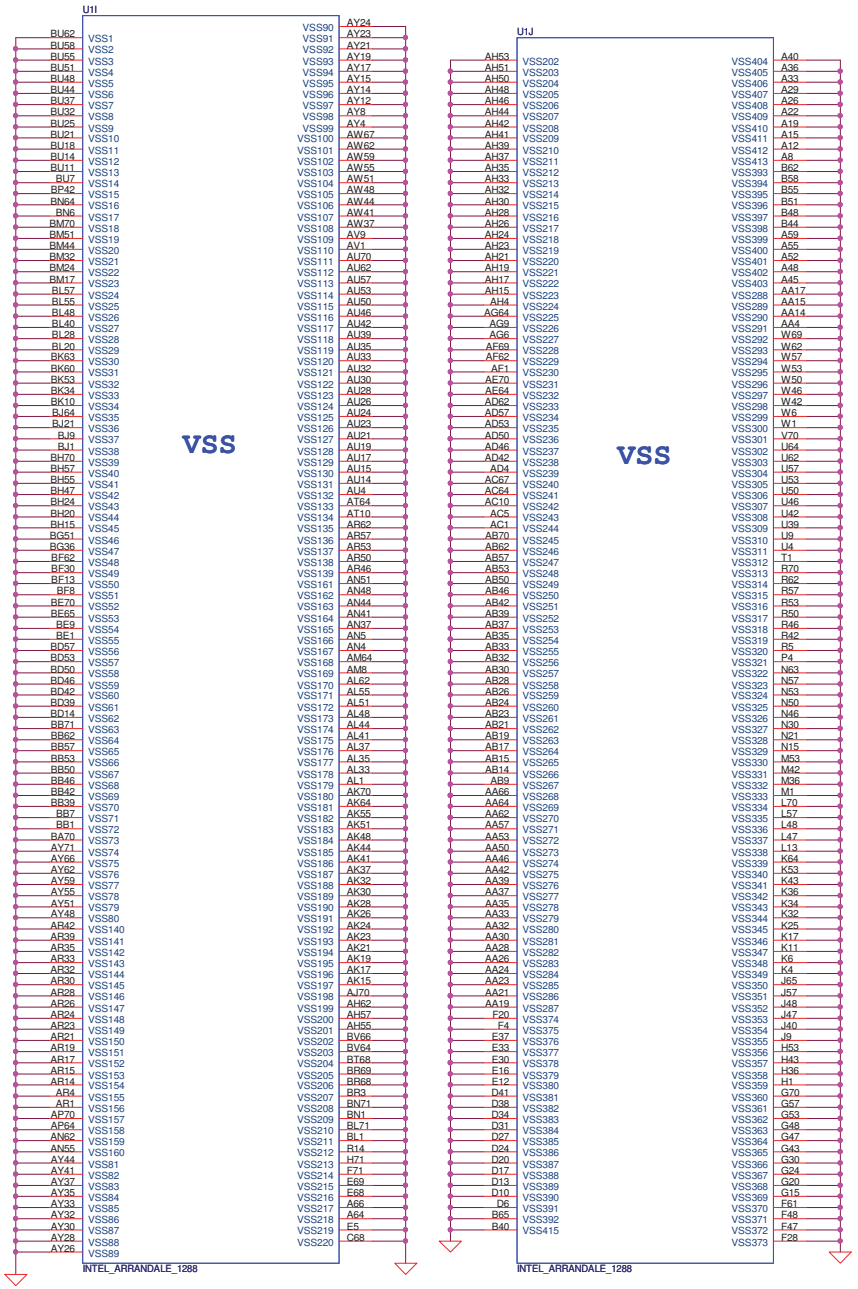
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

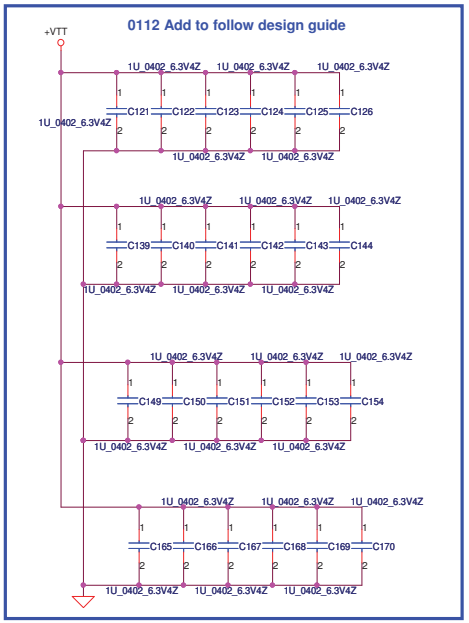
Compal Electronics, Inc.		
Title: CPU DDRIII		
Size: B	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 7 of 45	

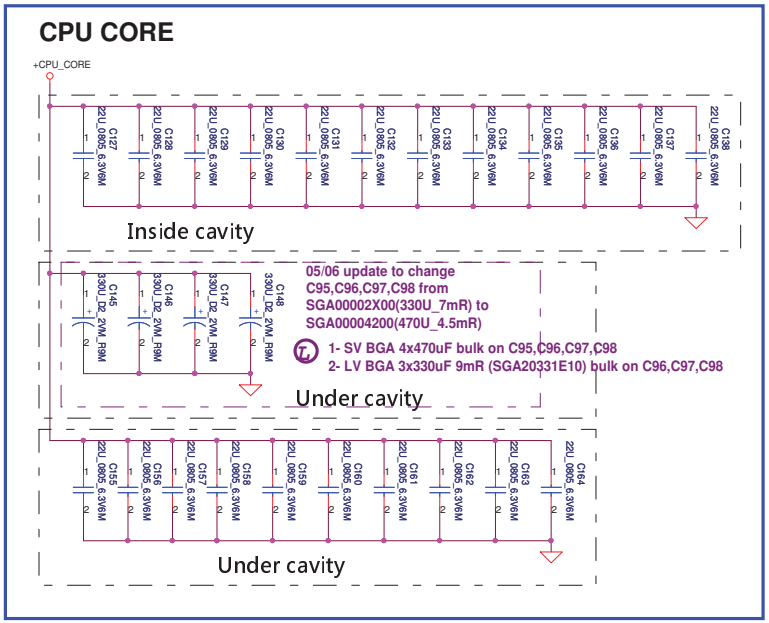


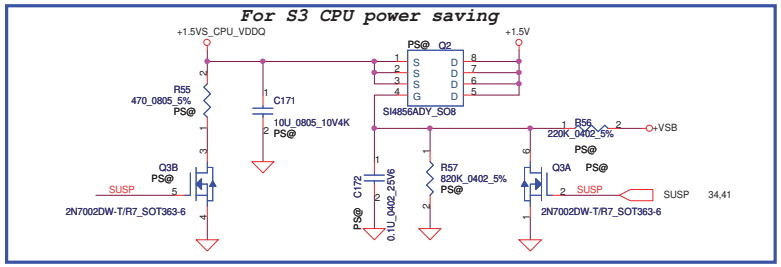
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/12/31

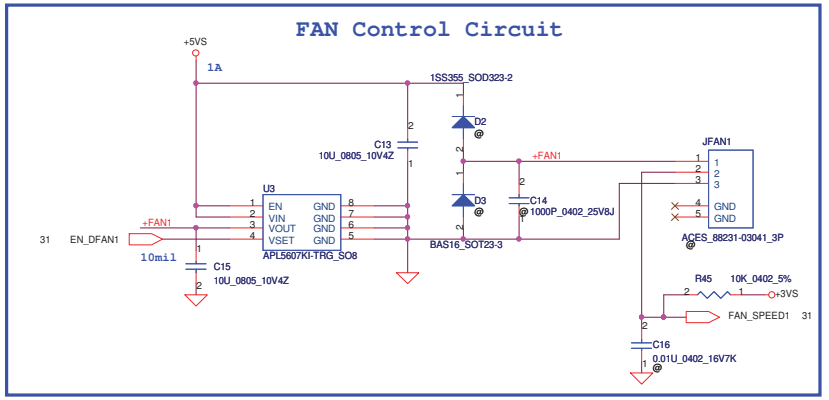
Compal Electronics, Inc.		
Title: Auburndale(4/5)-PWR		
Size: Custom	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 8 of 45	











Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: Auburndale(5/5)-GND/Bypass

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 9 of 45

DDR3 SO-DIMM A
Standard Type

JDDRL1

+VREF_DQA

C173 0.1U_0402_16V4Z
C174 2.2U_0603_6.3V4Z

close to JDDRL.1

+1.5V

R60 1K_0402_1% PS@

For S3 CPU power saving

SM_DRAMRST# 5,11

7 DDR_A_DQS[0..7]
7 DDR_A_DQS#[0..7]
7 DDR_A_D[0..63]
7 DDR_A_DM[0..7]
7 DDR_A_MA[0..15]

M1 Circuit

+1.5V
R59 1K_0402_1%
R62 1K_0402_1%
+V_DDR3_DIMM_REF
R58 0_0402_5%
R61 0_0402_5%
+VREF_DQB
+VREF_DQA

	VREF_DQ	1	2	VSS1			
DDR_A_D0	VSS2	3	4	DQ4	DDR_A_D4		
DDR_A_D1	DQ0	5	6	DQ5	DDR_A_D5		
	DQ1	7	8	VSS3			
DDR_A_DM0	VSS4	9	10	DQS#0	DDR_A_DQS#0		
	DM0	11	12	DQS0	DDR_A_DQS0		
DDR_A_D2	VSS5	13	14	VSS6			
DDR_A_D3	DQ2	15	16	DQ6	DDR_A_D6		
	DQ3	17	18	DQ7	DDR_A_D7		
DDR_A_D8	VSS7	19	20	VSS8			
DDR_A_D9	DQ8	21	22	DQ12	DDR_A_D12		
	DQ9	23	24	DQ13	DDR_A_D13		
DDR_A_DQS#1	VSS9	25	26	VSS10			
DDR_A_DQS1	DQS#1	27	28	DM1	DDR_A_DM1		
	DQS1	29	30	RESET#	SM_DRAMRST# 5,11		
DDR_A_D10	VSS11	31	32	VSS12			
DDR_A_D11	DQ10	33	34	DQ14	DDR_A_D14		
	DQ11	35	36	DQ15	DDR_A_D15		
DDR_A_D16	VSS13	37	38	VSS14			
DDR_A_D17	DQ16	39	40	DQ20	DDR_A_D20		
	DQ17	41	42	DQ21	DDR_A_D21		
DDR_A_DQS#2	VSS15	43	44	VSS16			
DDR_A_DQS2	DQS#2	45	46	DM2	DDR_A_DM2		
	DQS2	47	48	VSS17			
DDR_A_D18	VSS18	49	50	DQ22	DDR_A_D22		
DDR_A_D19	DQ18	51	52	DQ23	DDR_A_D23		
	DQ19	53	54	VSS19			
DDR_A_D24	VSS20	55	56	DQ28	DDR_A_D28		
DDR_A_D25	DQ24	57	58	DQ29	DDR_A_D29		
	DQ25	59	60	VSS21			
DDR_A_DM3	VSS22	61	62	DQS#3	DDR_A_DQS#3		
	DM3	63	64	DQS3	DDR_A_DQS3		
DDR_A_D26	VSS23	65	66	VSS24			
DDR_A_D27	DQ26	67	68	DQ30	DDR_A_D30		
	DQ27	69	70	DQ31	DDR_A_D31		
	VSS25	71	72	VSS26			
7 DDRA_CKE0	CKE0	73	74	CKE1		DDRA_CKE1 7	
	VDD1	75	76	VDD2			
	NC1	77	78	A15	DDR_A_MA15		
7 DDR_A_BS2	BA2	79	80	A14	DDR_A_MA14		
	VDD3	81	82	VDD4			
DDR_A_MA12	A12/BC#	83	84	A11	DDR_A_MA11		
DDR_A_MA9	A9	85	86	A7	DDR_A_MA7		
	VDD5	87	88	VDD6			
DDR_A_MA8	A8	89	90	A6	DDR_A_MA6		
DDR_A_MA5	A5	91	92	A4	DDR_A_MA4		
	VDD7	93	94	VDD8			
DDR_A_MA3	A3	95	96	A2	DDR_A_MA2		
DDR_A_MA1	A1	97	98	A0	DDR_A_MA0		
	VDD9	99	100	VDD10			
7 DDRA_CLK0	CK0	101	102	CK1		DDRA_CLK1 7	
7 DDRA_CLK0#	CK0#	103	104	CK1#		DDRA_CLK1# 7	
	VDD11	105	106	VDD12			
DDR_A_MA10	A10/AP	107	108	BA1		DDR_A_BS1 7	
7 DDR_A_BS0	BA0	109	110	RAS#		DDR_A_RAS# 7	
	VDD13	111	112	VDD14			
7 DDR_A_WE#	WE#	113	114	S0#		DDRA_SCS0# 7	
7 DDR_A_CAS#	CAS#	115	116	ODT0		DDRA_ODT0 7	
	VDD15	117	118	VDD16			
DDR_A_MA13	A13	119	120	ODT1		DDRA_ODT1 7	
7 DDRA_SCS1#	S1#	121	122	NC2			
	VDD17	123	124	VDD18			
	NCTEST	125	126	VREF_CA	+DDR_VREF_CA_DIMMA		
	VSS27	127	128	VSS28			
DDR_A_D32	DQ32	129	130	DQ36	DDR_A_D36		
DDR_A_D33	DQ33	131	132	DQ37	DDR_A_D37		
	VSS29	133	134	VSS30			
DDR_A_DQS#4	DQS#4	135	136	DM4	DDR_A_DM4		
DDR_A_DQS4	DQS4	137	138	VSS31			
	VSS32	139	140	DQ38	DDR_A_D38		
DDR_A_D34	DQ34	141	142	DQ39	DDR_A_D39		
DDR_A_D35	DQ35	143	144	VSS33			
	VSS34	145	146	DQ44	DDR_A_D44		
DDR_A_D40	DQ40	147	148	DQ45	DDR_A_D45		
DDR_A_D41	DQ41	149	150	VSS35			
	VSS36	151	152	DQS#5	DDR_A_DQS#5		
DDR_A_DM5	DM5	153	154	DQS5	DDR_A_DQS5		
	VSS37	155	156	VSS38			
DDR_A_D42	DQ42	157	158	DQ46	DDR_A_D46		
DDR_A_D43	DQ43	159	160	DQ47	DDR_A_D47		
	VSS39	161	162	VSS40			
DDR_A_D48	DQ48	163	164	DQ52	DDR_A_D52		
DDR_A_D49	DQ49	165	166	DQ53	DDR_A_D53		
	VSS41	167	168	VSS42			
DDR_A_DQS#6	DQS#6	169	170	DM6	DDR_A_DM6		
DDR_A_DQS6	DQS6	171	172	VSS43			
	VSS44	173	174	DQ54	DDR_A_D54		
DDR_A_D50	DQ50	175	176	DQ55	DDR_A_D55		
DDR_A_D51	DQ51	177	178	VSS45			
	VSS46	179	180	DQ60	DDR_A_D60		
DDR_A_D56	DQ56	181	182	DQ61	DDR_A_D61		
DDR_A_D57	DQ57	183	184	VSS47			
	VSS48	185	186	DQS#7	DDR_A_DQS#7		
DDR_A_DM7	DM7	187	188	DQS7	DDR_A_DQS7		
	VSS49	189	190	VSS50			
DDR_A_D58	DQ58	191	192	DQ62	DDR_A_D62		
DDR_A_D59	DQ59	193	194	DQ63	DDR_A_D63		
	VSS51	195	196	VSS52			
	SA0	197	198	EVENT#		PM_EXTTS# 5,11	
	VDDSPD	199	200	SDA		PM_SMBDATA 11,12,16,26	
	SA1	201	202	SCL		PM_SMBCLK 11,12,16,26	
	VTT1	203	204	VTT2			
	G1	205	206	G2			

@FOX_AS0A626-U4SG-7H

+1.5V
+0.75VS
+3VS
+V_DDR3_DIMM_REF

R63 0_0402_5%
C175 2.2U_0603_6.3V4Z
C176 0.1U_0402_16V4Z

close to JDDRL.126

Reserve for cost down

C192 330U_2.5V_M_R17

R64 10K_0402_5%
C194 2.2U_0603_6.3V4Z
C195 0.1U_0402_16V4Z
R65 10K_0402_5%

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

C177 330U_B2_2.5VM_R15M
C180 10U_0805_6.3V6M
C182 10U_0805_6.3V6M
C185 10U_0805_6.3V6M
C188 10U_0805_6.3V6M
C190 10U_0805_6.3V6M
C193 10U_0805_6.3V6M

C178 0.1U_0402_16V4Z
C181 0.1U_0402_16V4Z
C184 0.1U_0402_16V4Z
C187 0.1U_0402_16V4Z

Layout Note:
Place near JDDRL1.203 and 204

C179 10U_0805_6.3V6M
C183 1U_0402_6.3V4Z
C186 1U_0402_6.3V4Z
C189 1U_0402_6.3V4Z
C191 1U_0402_6.3V4Z

Compal Electronics, Inc.

Title: **DDRIII-SODIMM0**

Size: Custom | Document Number: **NDU00_LA-6031P M/B** | Rev: 1.0

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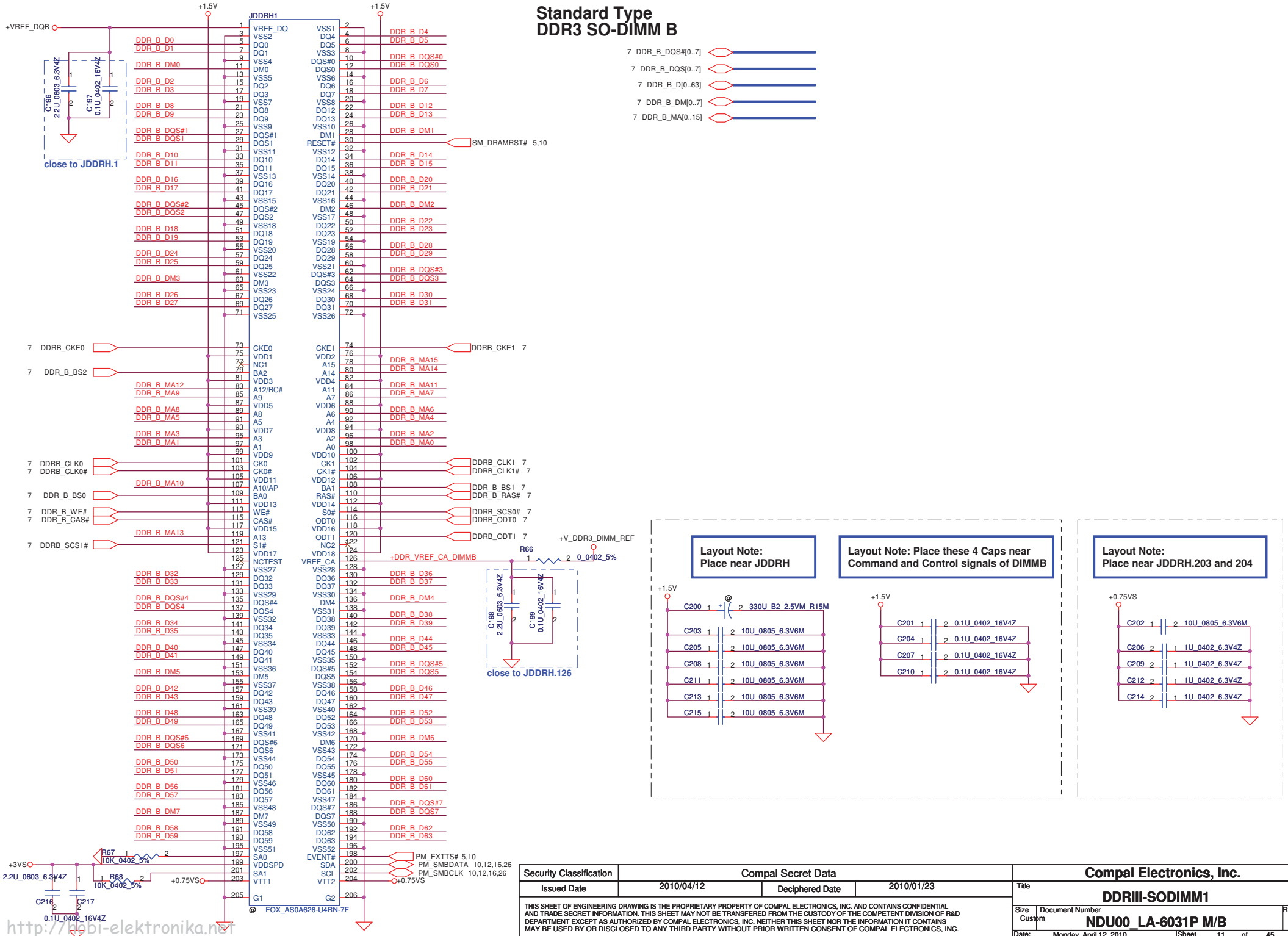
Standard Type
DDR3 SO-DIMM B



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

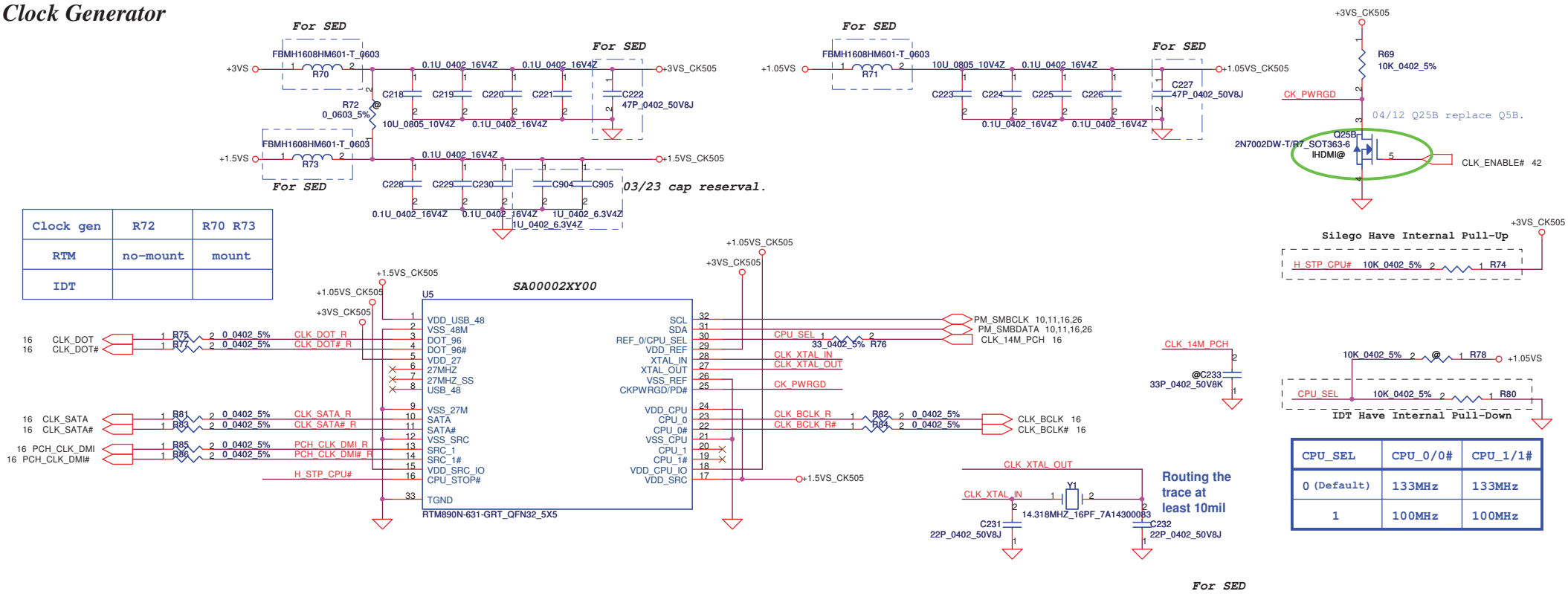
Compal Electronics, Inc.

Title: **DDRIII-SODIMM1**

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 11 of 45

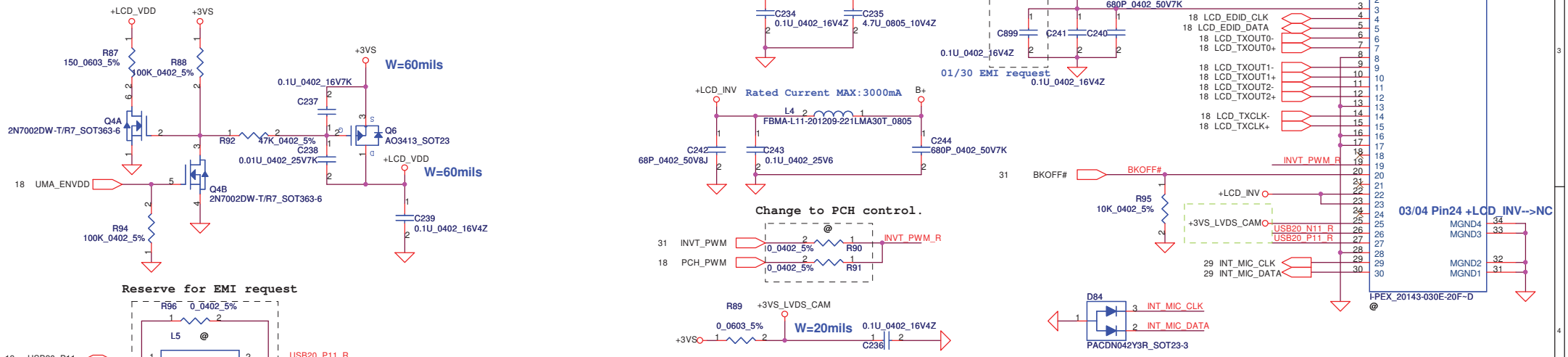
Clock Generator



Clock gen	R72	R70 R73
RTM	no-mount	mount
IDT		

CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **Clock Generator (CK505)/ LVDS CONN**

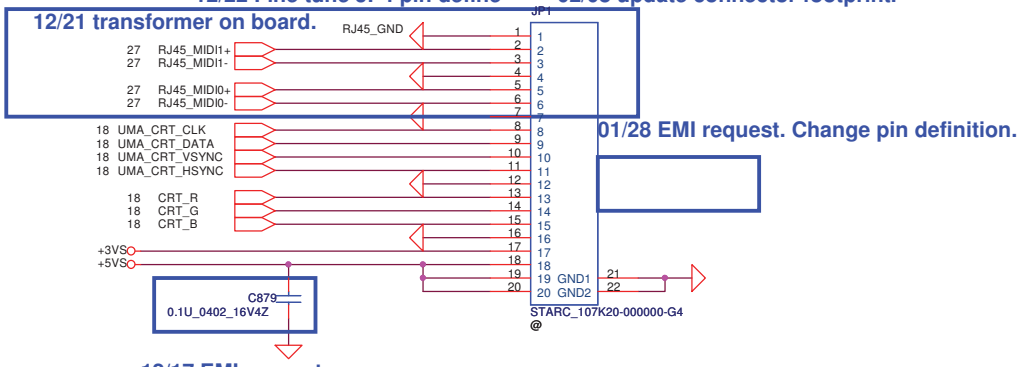
Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 | Sheet 12 of 45

CRT CONNECTOR

12/14 Fine tune pin define JP1 Pin1 Pin2 Pin8-->GND
12/21 pin 2,3 to RJ45_GND
12/22 Fine tune JP4 pin define
02/08 update connector footprint.

12/21 transformer on board.



01/28 EMI request. Change pin definition.

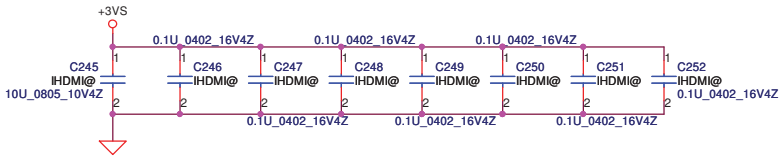
12/17 EMI request.

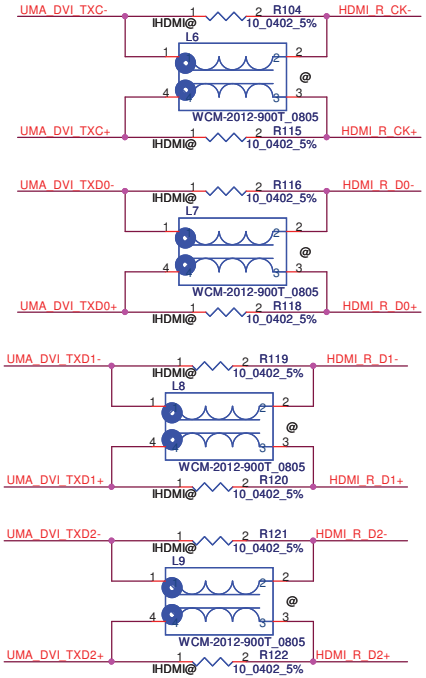
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

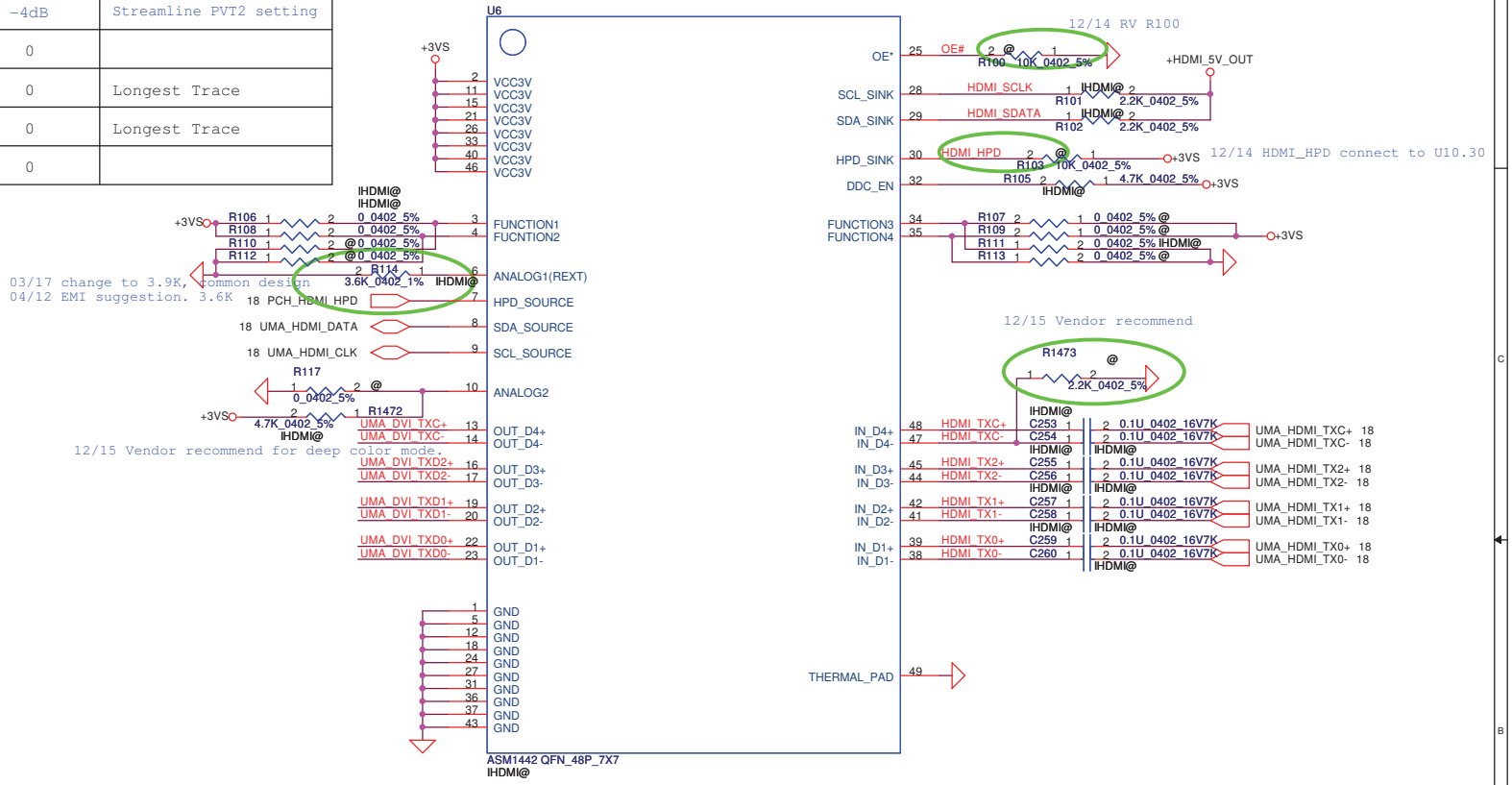
Compal Electronics, Inc.

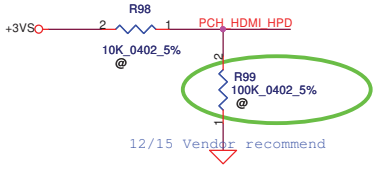
Title	CRT\TV\LVDS	
Size	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 13 of 45	

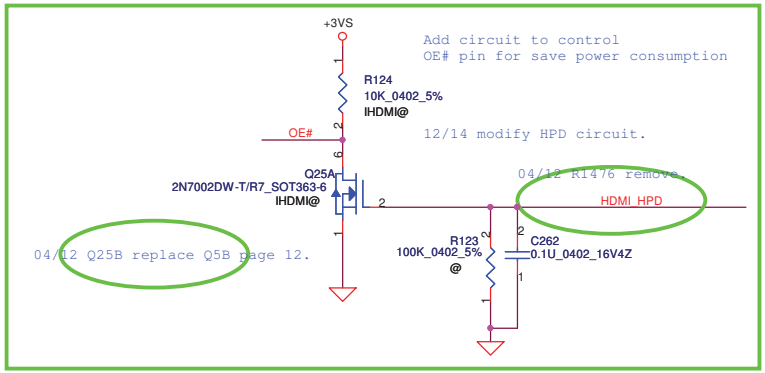
ANALOG2	Function2	Function1	Swing	Pre-Amp	Slew-rate	Note
Low	Low	Low	450	0	0	
Low	Low	High	420	0	-3dB	Shortest trace
Low	High	Low	450	0	-3dB	Shortest trace
Low	High	High	460	0	-4dB	Streamline PVT2 setting
High	Low	Low	340	0	0	
High	Low	High	400	2dB	0	Longest Trace
High	High	Low	400	2dB	0	Longest Trace
High	High	High	420	0	0	

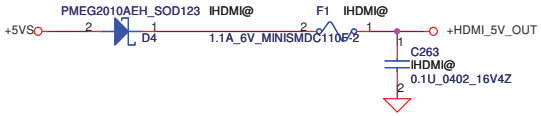






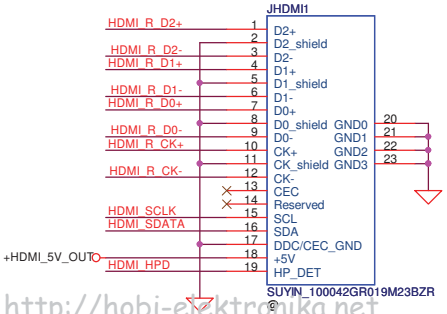






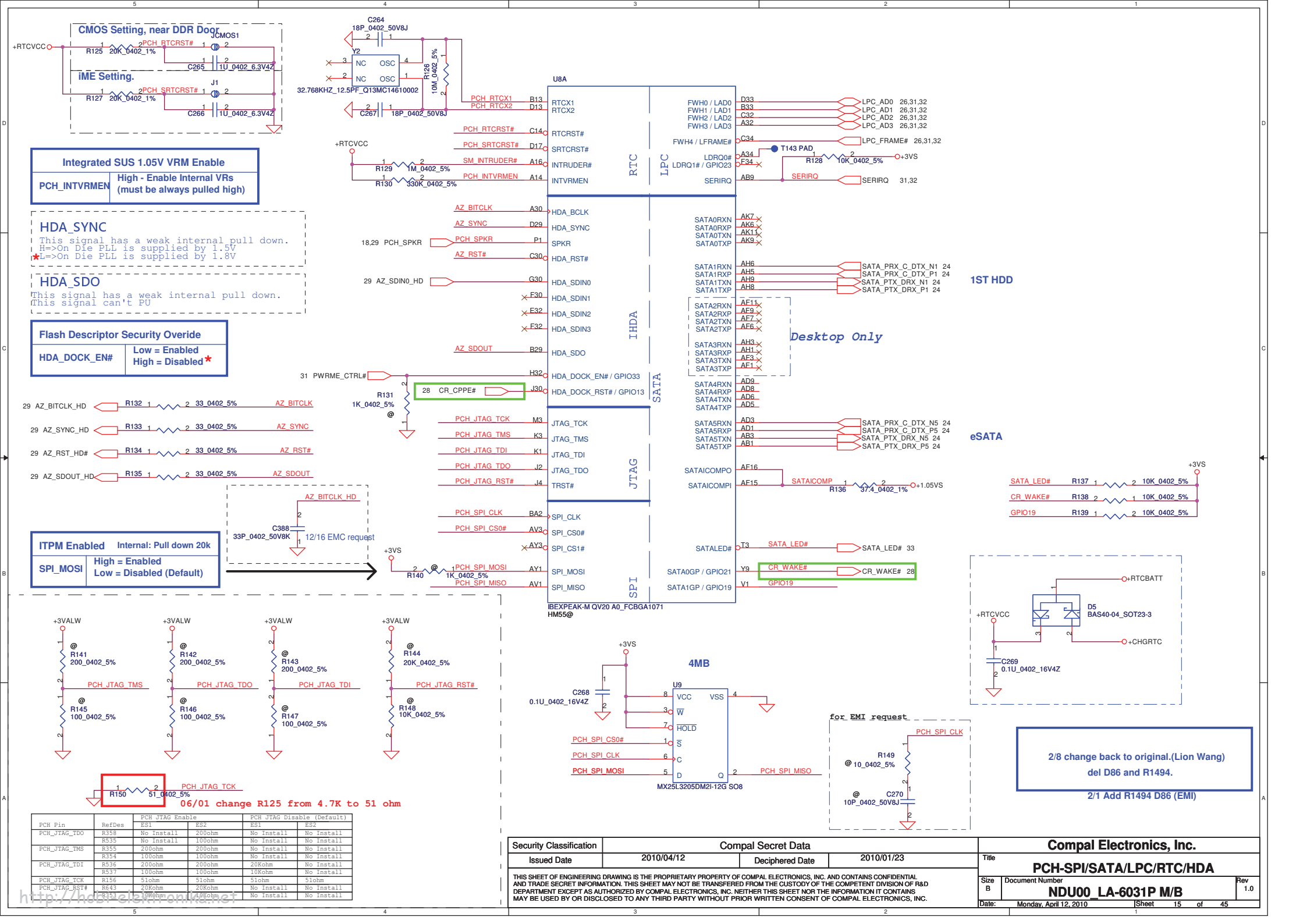
HDMI Connector

<01/27 update HDMI Connector >



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

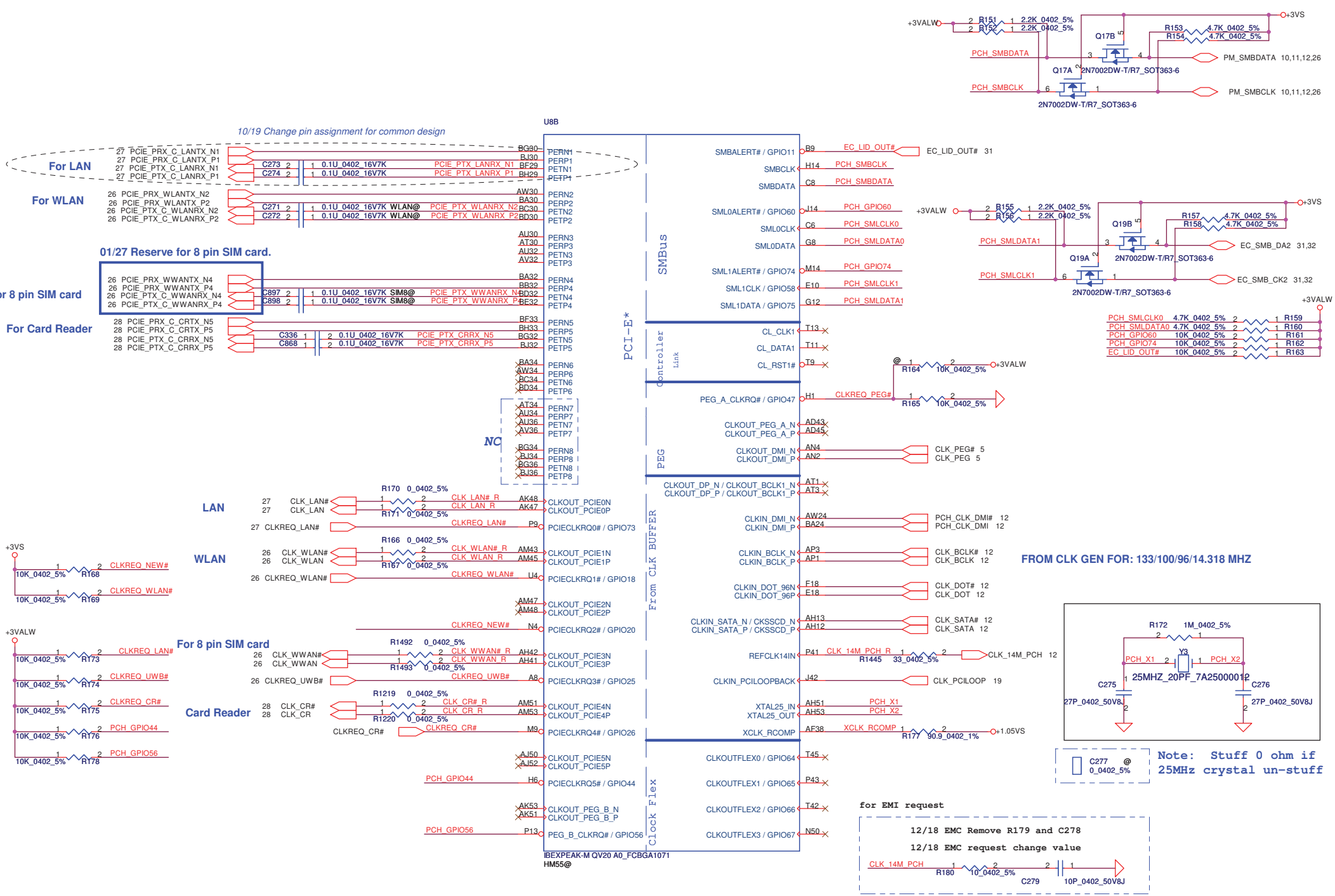
Compal Electronics, Inc.			
Title: HDMI Connector			
Size	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 14 of 45		



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	PCH-SPI/SATA/LPC/RTC/HDA
Size B	Document Number NDU00_LA-6031P M/B
Rev	1.0
Date: Monday, April 12, 2010	Sheet 15 of 45



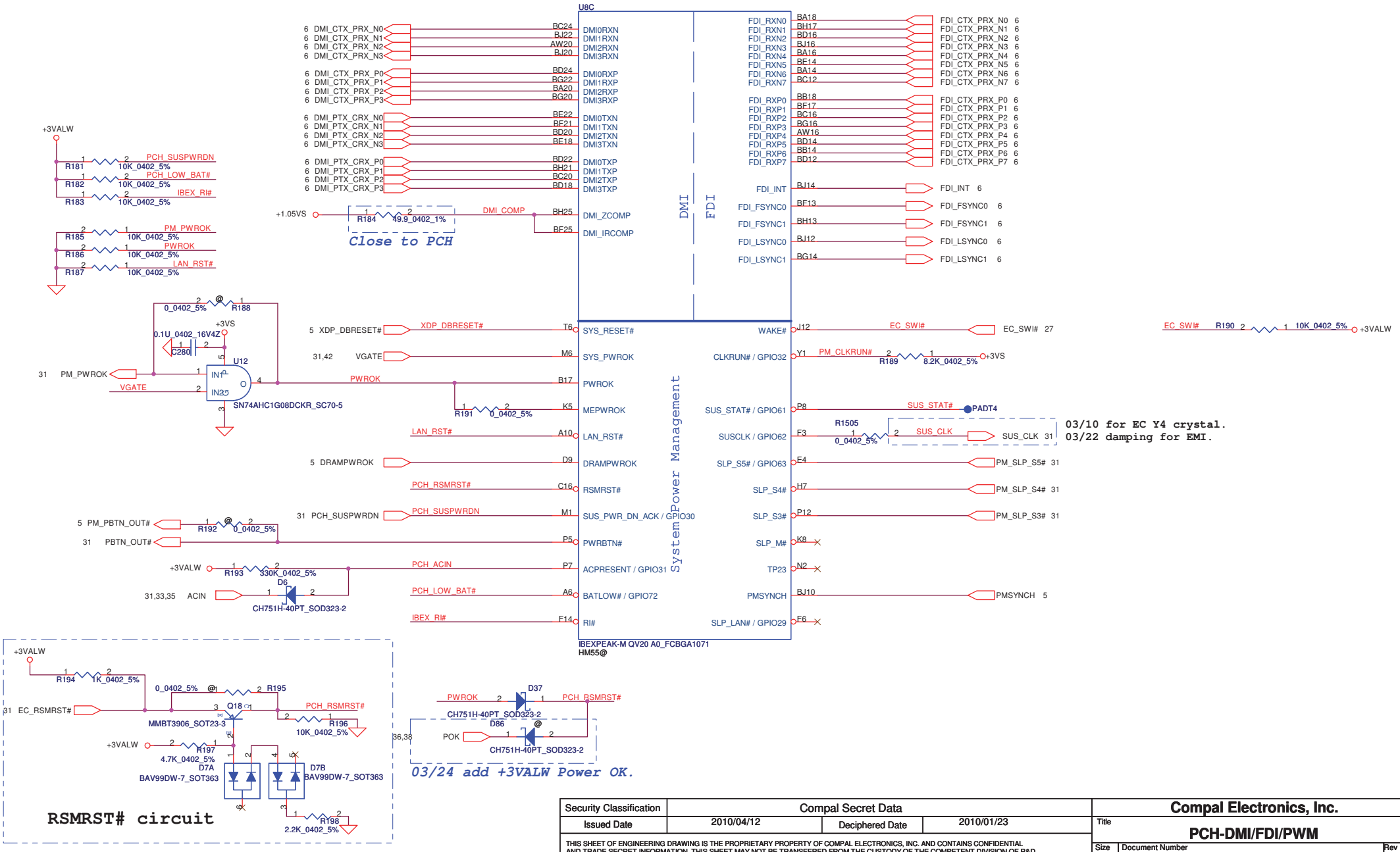
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: CLK/PCIE/SMBUS

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 16 of 45



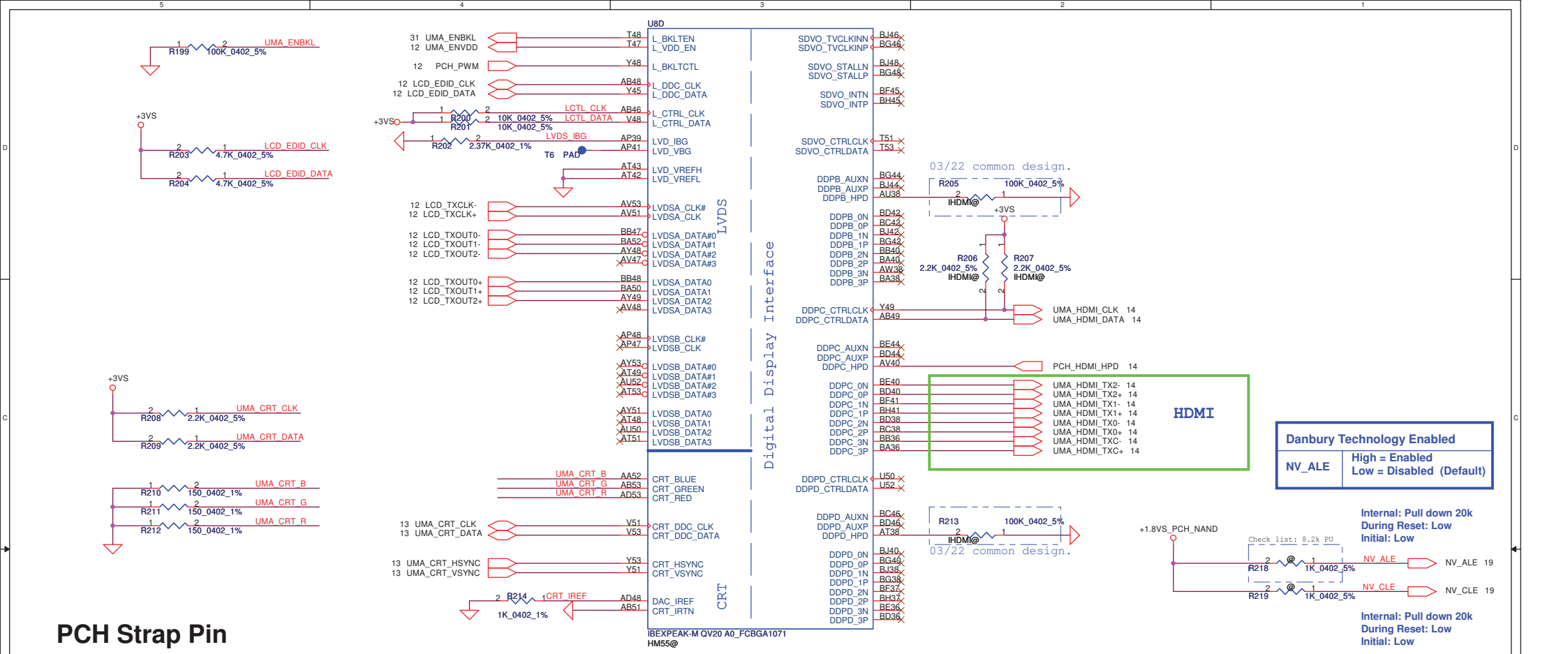
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH-DMI/FDI/PWM**

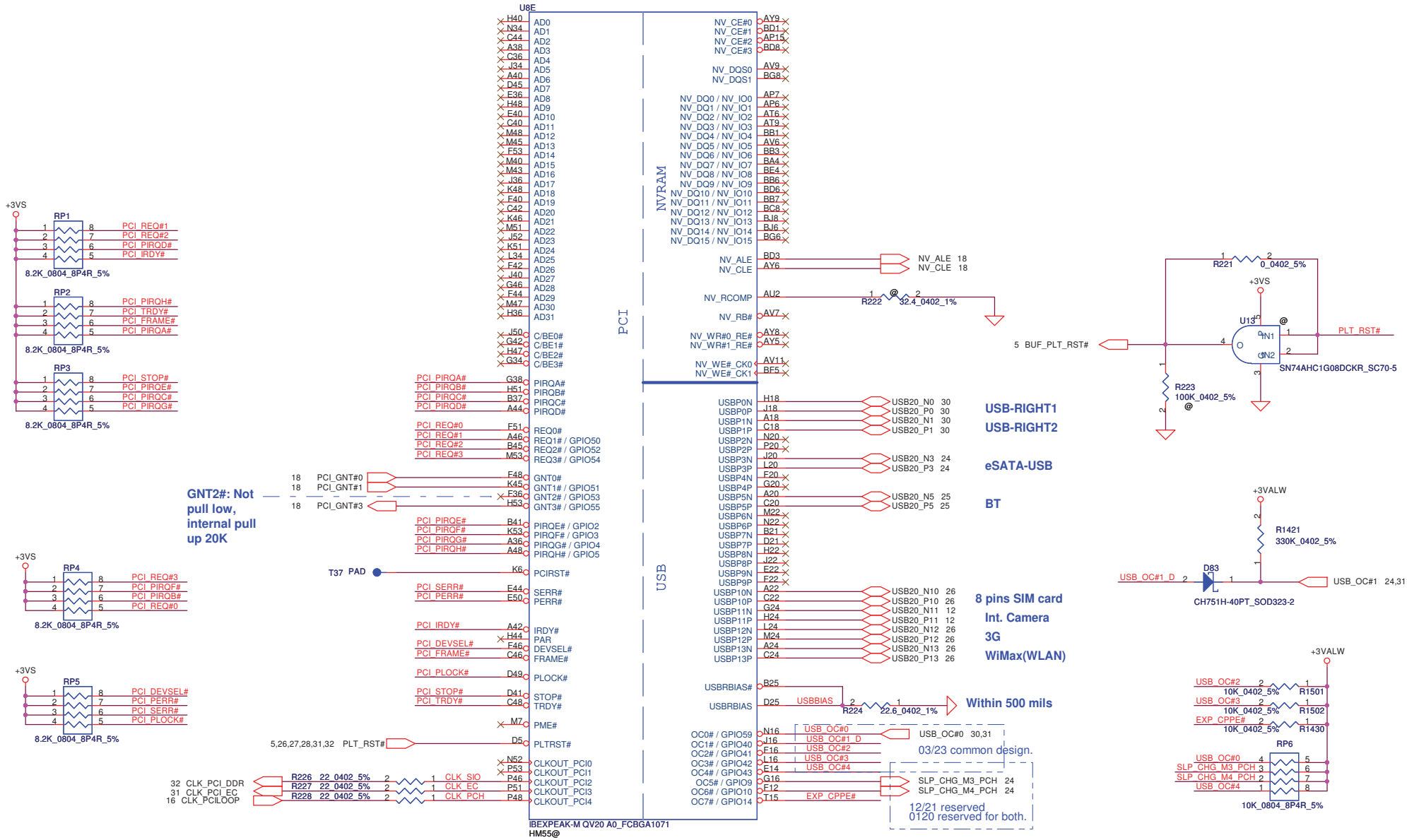
Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 17 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	PCH-CRT/LVDS/HDMI		
Size: Custom	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 18 of 45		



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH USB/PCI/NAND**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 19 of 45

GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR	
PCH_GPIO27	High = Enabled (Default) Low = Disabled

1019 change net name to follow common design

U8F

BMBUSY# / GPIO0 — PCH_GPIO0 — Y3
TACH1 / GPIO1 — PCH_GPIO1 — C38
TACH2 / GPIO6 — PCH_GPIO6 — D37
TACH3 / GPIO7 — EC_SCI# — J32 — 31 EC_SCI#
GPIO8 — EC_SMI# — F10 — 31 EC_SMI#
LAN_PHY_PWR_CTRL / GPIO12 — PCH_GPIO12 — K9
GPIO15 — PCH_GPIO15 — T7
SATA4GP / GPIO16 — PCH_GPIO16 — AA2
TACH0 / GPIO17 — 3G_OFF# — F38 — 26 3G_OFF#
SCLOCK / GPIO22 — BT_DET# — Y7 — 25 BT_DET#
GPIO24 — H10
GPIO27 — PCH_GPIO27 — AB12 — R232 2 @ 1 1K_0402_5%
GPIO28 — PCH_GPIO28 — V13
STP_PCI# / GPIO34 — M11 — 25,26 BT_PWR#
SATACLKREQ# / GPIO35 — V6 — 25 BT_RST#
SATA2GP / GPIO36 — PCH_GPIO36 — AB7
SATA3GP / GPIO37 — PCH_GPIO37 — AB13
SLOAD / GPIO38 — PCH_GPIO38 — V3
SDATAOUT0 / GPIO39 — PCH_GPIO39 — P3
PCIECLKRQ6# / GPIO45 — PCH_GPIO45 — H3
PCIECLKRQ7# / GPIO46 — RST_GATE — F1 — 5 RST_GATE
SDATAOUT1 / GPIO48 — ISDBT_DET — AB6
SATA5GP / GPIO49 — THM_ALT# — AA4 — 31 THM_ALT#
GPIO57 — PCH_GPIO57 — F8

MISC
GPIO
CPU

CLKOUT_PCIE6N — AH45
CLKOUT_PCIE6P — AH46
CLKOUT_PCIE7N — AF48
CLKOUT_PCIE7P — AF47
A20GATE — U2 — GATEA20 — GATEA20 31
CLKOUT_BCLK0_N / CLKOUT_PCIE8N — AM3 — CLK_CPU_BCLK# 5
CLKOUT_BCLK0_P / CLKOUT_PCIE8P — AM1 — CLK_CPU_BCLK 5
PECI — BG10 — PCH_PECI — R231 1 2 0_0402_5% — PECI 5
RCIN# — T1 — KB_RST# — KB_RST# 31
PROCPWRGD — BE10 — H_PWRGOOD 5
THRMTRIP# — BD10 — THRMTRIP_PCH# — R233 1 2 56_0402_1% — H_THERMTRIP# 5
R234 1 2 56_0402_1% +VTT

+3VS
R230 10K_0402_5%
KB_RST# — R229 2 1 10K_0402_5% — +3VS

TP1 — BA22
TP2 — AW22
TP3 — BB22
TP4 — AY45
TP5 — AY46
TP6 — AV43
TP7 — AV45
TP8 — AF13
TP9 — M18
TP10 — N18
TP11 — AJ24
TP12 — AK41
TP13 — AK42
TP14 — M32
TP15 — N32
TP16 — M30
TP17 — N30
TP18 — H12
TP19 — AA23
NC_1 — AB45
NC_2 — AB38
NC_3 — AB42
NC_4 — AB41
NC_5 — T39
INIT3_3V# — P6
TP24 — C10

NCTF
RSVD

VSS_NCTF_1 — A4
VSS_NCTF_2 — A49
VSS_NCTF_3 — A5
VSS_NCTF_4 — A50
VSS_NCTF_5 — A52
VSS_NCTF_6 — A53
VSS_NCTF_7 — B2
VSS_NCTF_8 — B4
VSS_NCTF_9 — B52
VSS_NCTF_10 — B53
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE53
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF53
VSS_NCTF_15 — BH1
VSS_NCTF_16 — BH2
VSS_NCTF_17 — BH52
VSS_NCTF_18 — BH53
VSS_NCTF_19 — BJ1
VSS_NCTF_20 — BJ2
VSS_NCTF_21 — BJ4
VSS_NCTF_22 — BJ49
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ50
VSS_NCTF_25 — BJ52
VSS_NCTF_26 — BJ53
VSS_NCTF_27 — D1
VSS_NCTF_28 — D2
VSS_NCTF_29 — D53
VSS_NCTF_30 — E1
VSS_NCTF_31 — E53

IBEXPEAK-M QV20 A0_FCBGA1071
HM55@

Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

+3VS
R235 PCH_GPIO0 10K_0402_5%
R236 PCH_GPIO1 10K_0402_5%
R237 PCH_GPIO6 8.2K_0402_5%
R238 EC_SCI# 10K_0402_5%
R239 PCH_GPIO16 10K_0402_5%
R240 3G_OFF# 10K_0402_5%
R241 BT_DET# 10K_0402_5%
R242 @ PCH_GPIO36 10K_0402_5%
R243 @ PCH_GPIO37 10K_0402_5%
R244 PCH_GPIO38 10K_0402_5%
R245 PCH_GPIO39 10K_0402_5%
R246 ISDBT_DET 10K_0402_5%
R247 THM_ALT# 10K_0402_5%

+3VALW
R248 EC_SMI# 10K_0402_5%
R249 PCH_GPIO57 10K_0402_5%
R250 PCH_GPIO15 1K_0402_5%
R251 PCH_GPIO28 10K_0402_5%
R252 PCH_GPIO45 10K_0402_5%
R253 RST_GATE 10K_0402_5%
R254 PCH_GPIO12 10K_0402_5%
R1495 PCH_GPIO36 10K_0402_5%
R1496 PCH_GPIO37 10K_0402_5%
02/08 reserved for porject ID.
R255 @ BT_RST# 10K_0402_5%
R256 @ EC_SMI# 1K_0402_5%

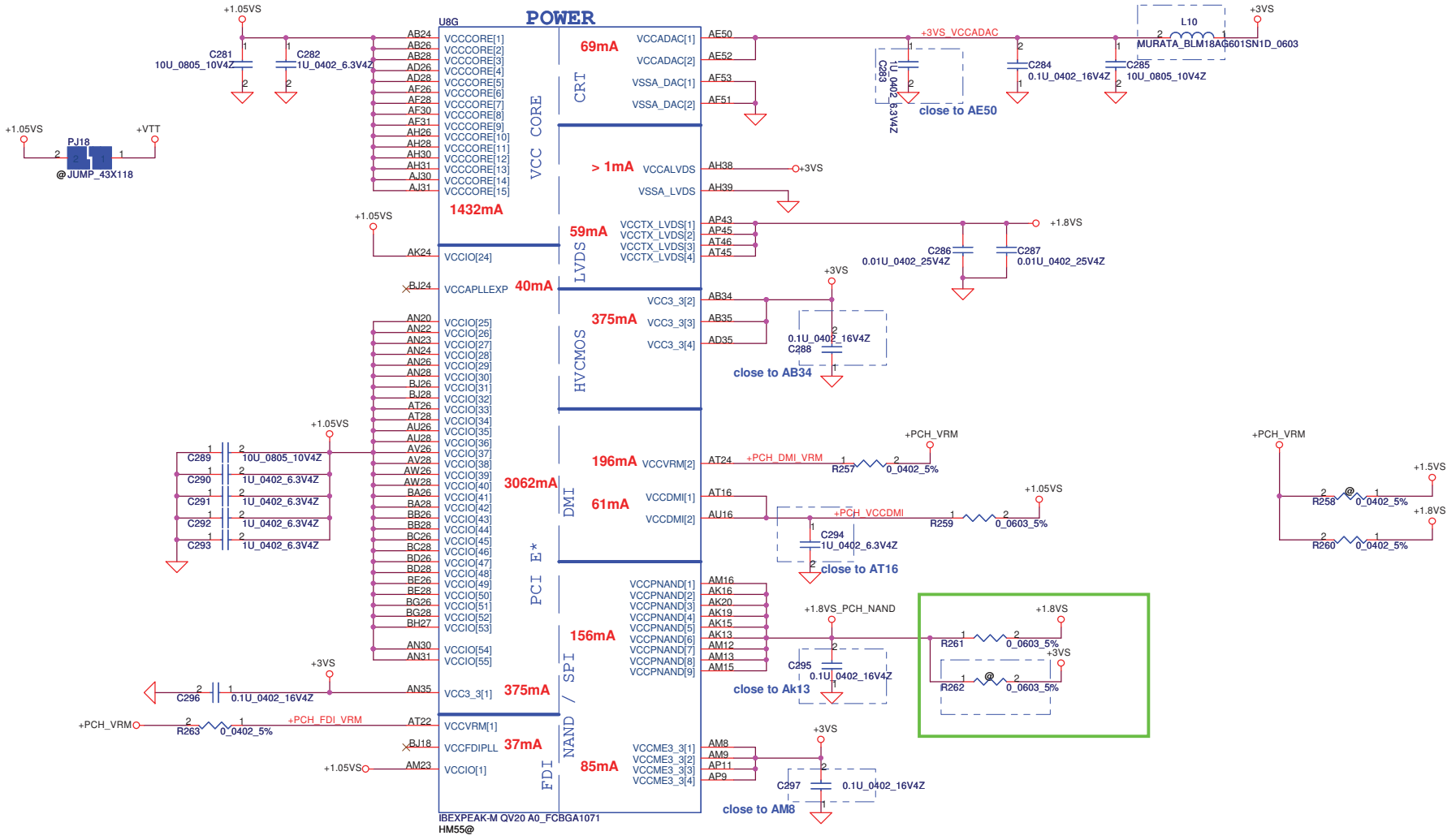
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PCH CPU/GPIO

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 Sheet 20 of 45



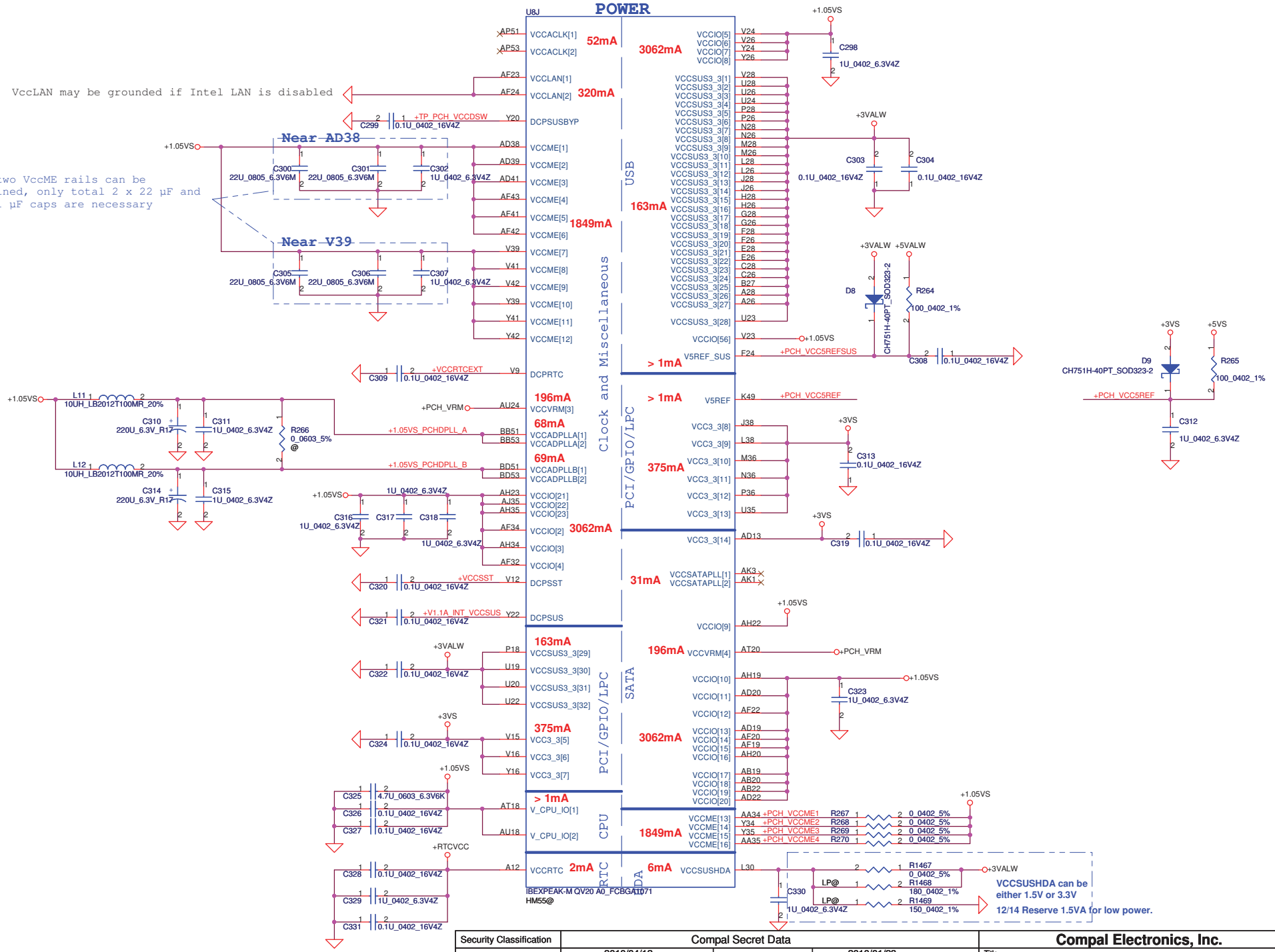
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH POWER-1**

Size	Document Number	Rev
B	NDU00_LA-6031P M/B	1.0

Date: Monday, April 12, 2010 | Sheet 21 of 45



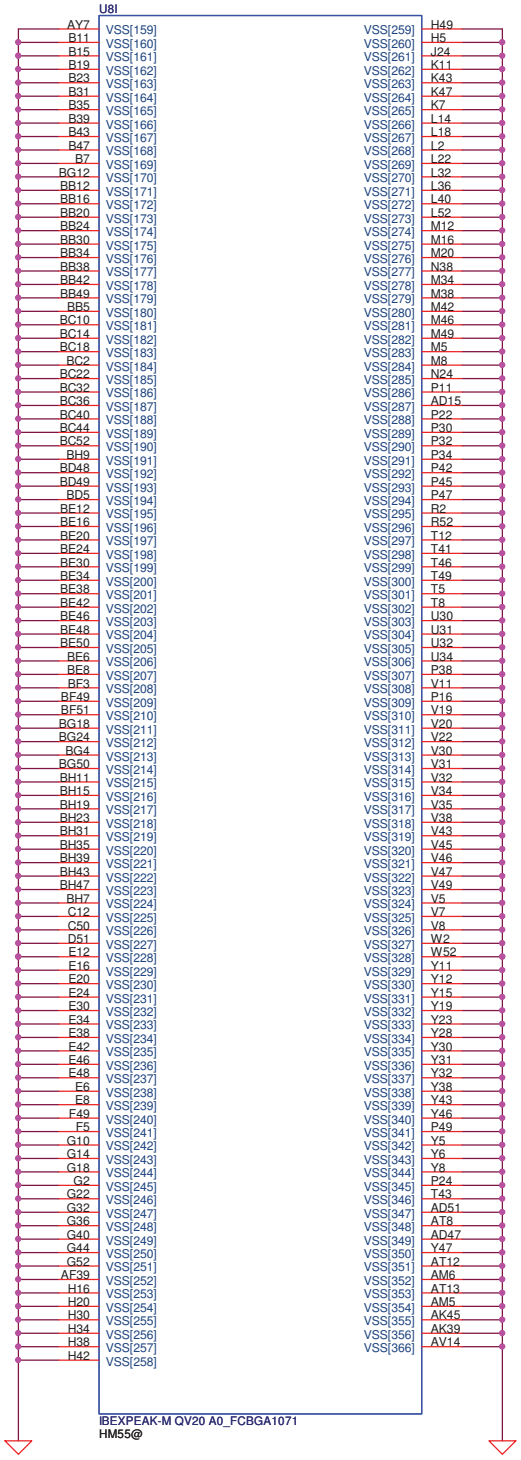
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

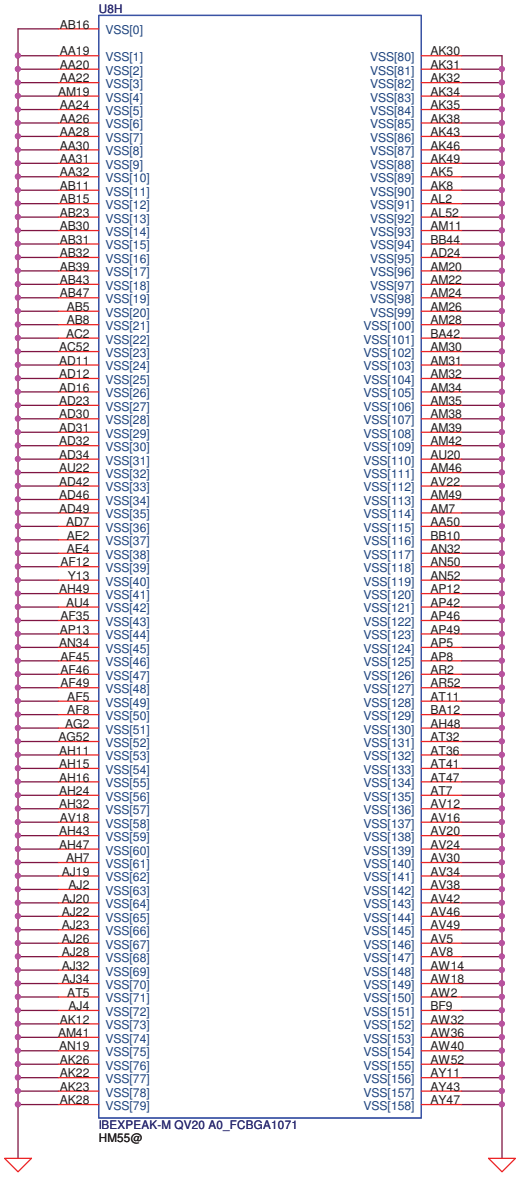
Compal Electronics, Inc.

Title: PCH POWER-2

Size: Custom | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 22 of 45





Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **PCH-GND**

Size	Document Number	Rev
Custom	NDU00_LA-6031P M/B	1.0

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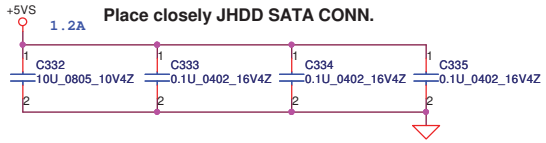
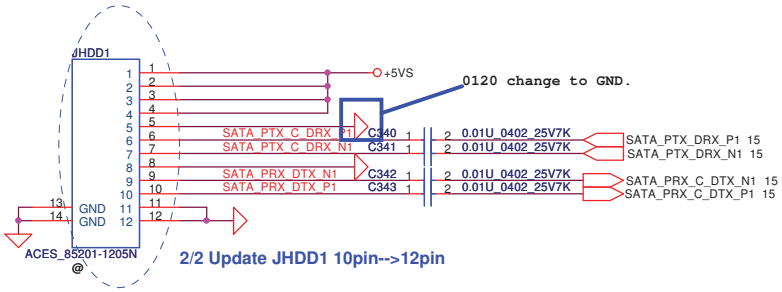
SATA HDD Conn.

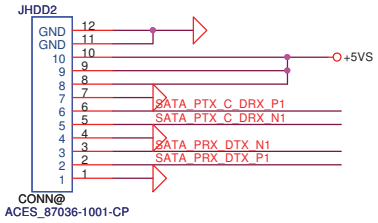


1/28 Add JHDD2

JHDD2 Layout symbol reverse JHDD1, recerse the pin define



2/2 Update JHDD1 10pin-->12pin

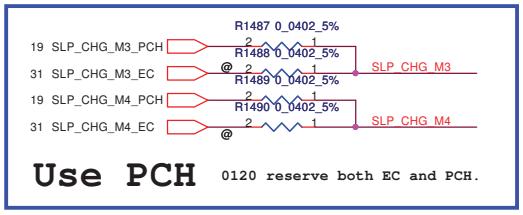


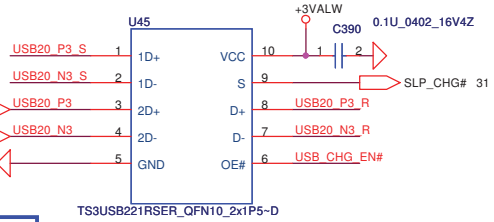
Add wire connector for H/W SATA verify

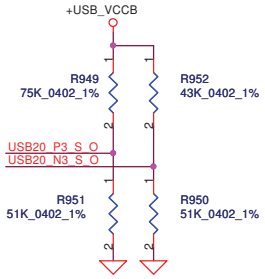
eSATA/USB Combo

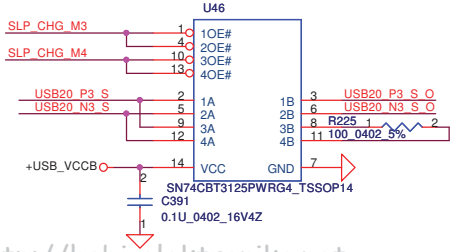
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

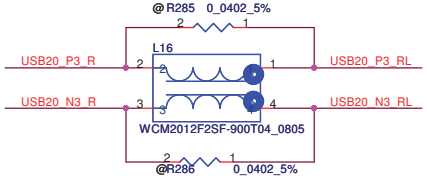
SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

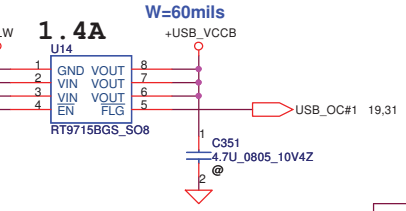


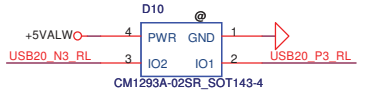


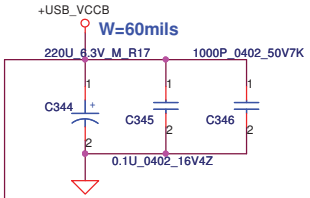






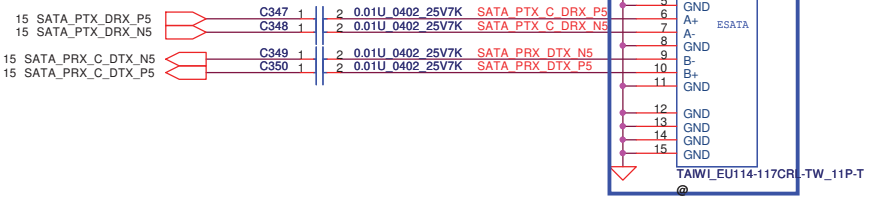






eSATA/USB Conn

1/26 update JSATA1 footprint

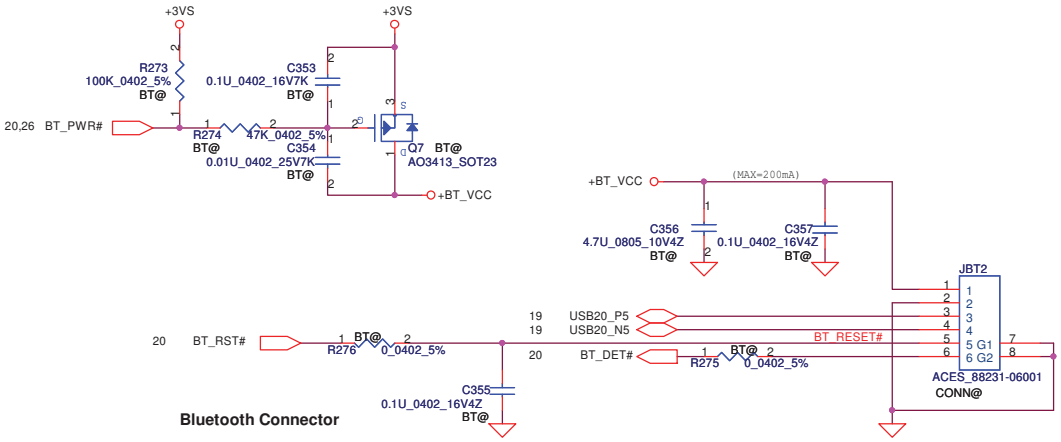


Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

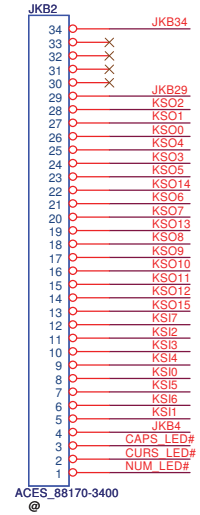
Compal Electronics, Inc.

Title	SATA-HDD/ODD/USB	
Size	Document Number NDU00_LA-6031P M/B	Rev 1.0
Date: Monday, April 12, 2010	Sheet 24 of 45	

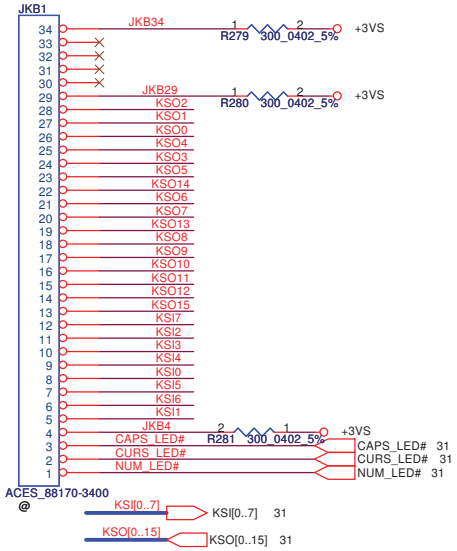
BlueTooth Interface

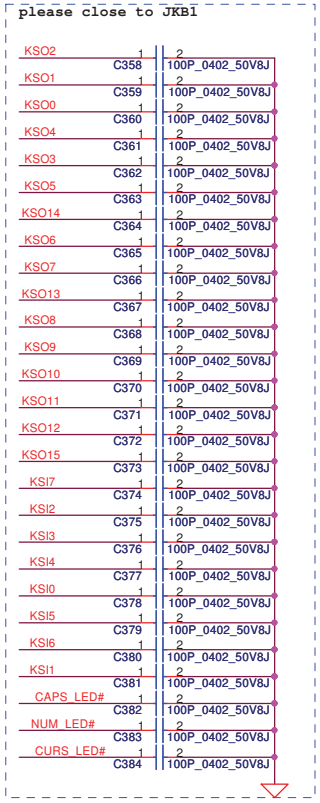


KEYBOARD CONN. for 11.6"



KEYBOARD CONN. for 13.3"





Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

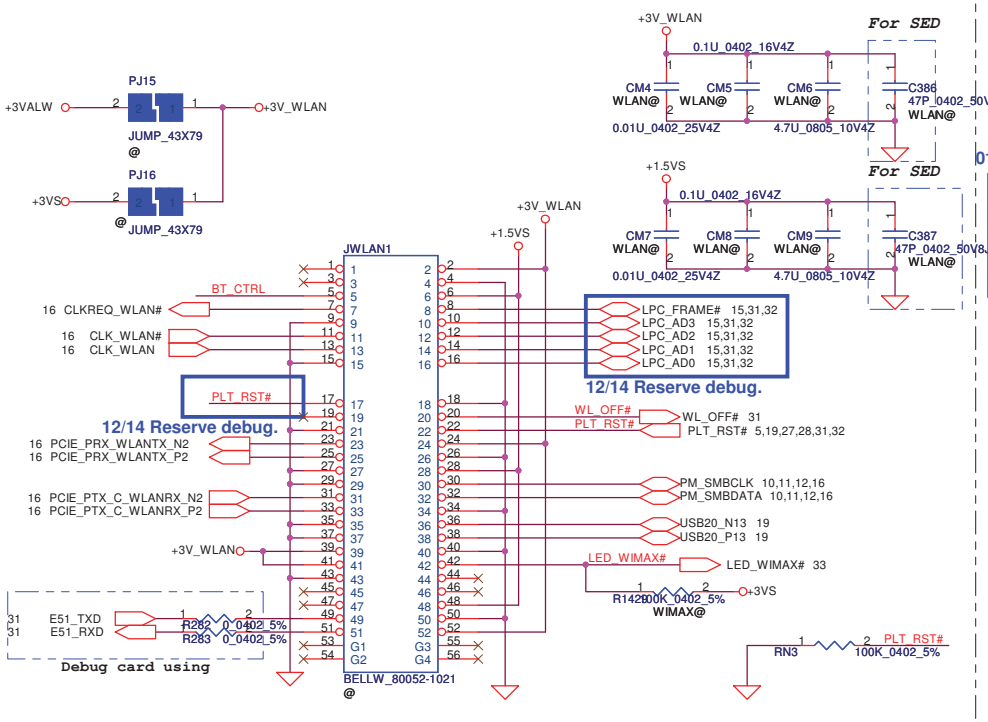
Compal Electronics, Inc.

Title: USB/BT/FP/Int. Cam

Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 25 of 45

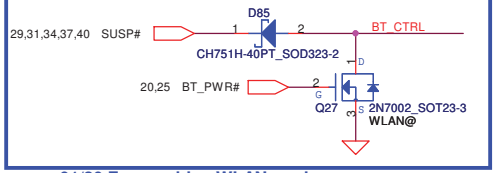
PCIe Mini Card-WLAN/WiMax



WLAN&BT Combo module circuits

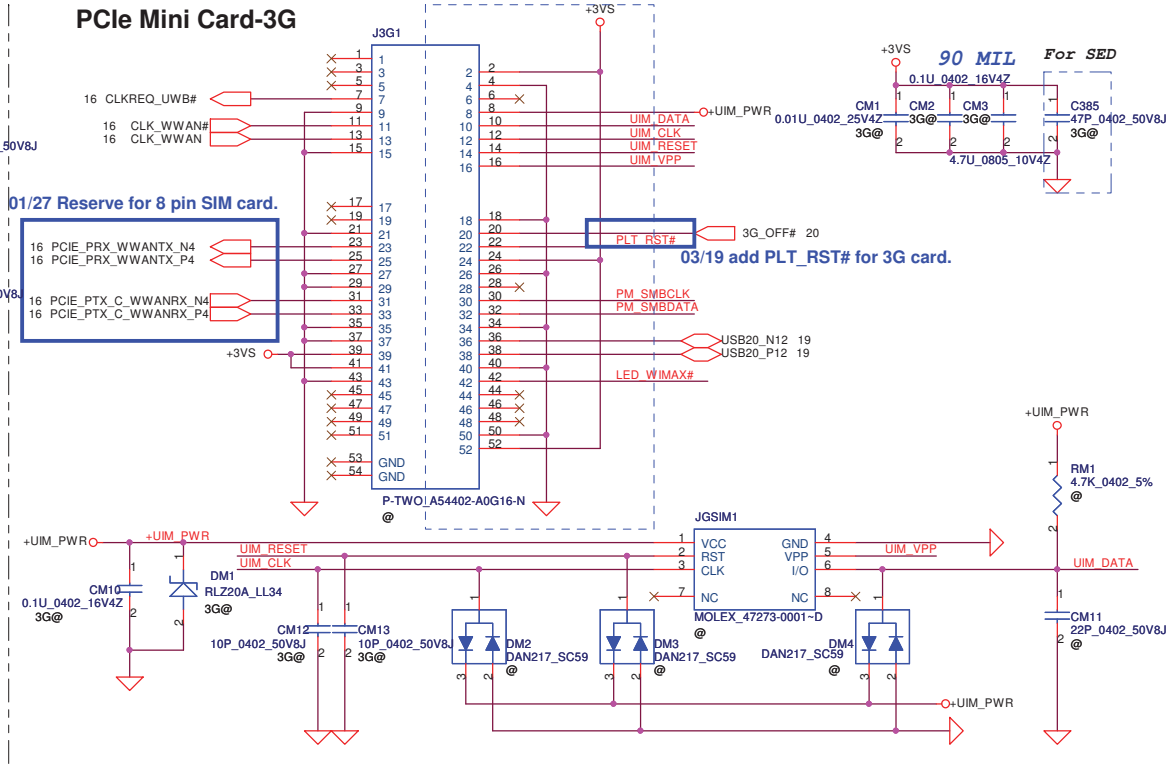
	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

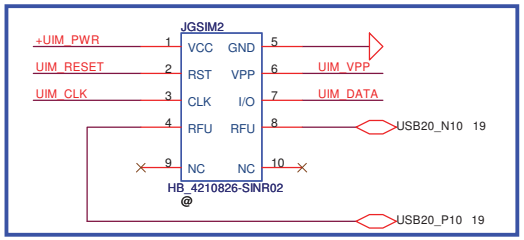
**If +3V_WLAN is +3VS, please remove D21.



01/20 For combine WLAN card.

PCIe Mini Card-3G





01/26 Co-lay with JGSIM1.

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

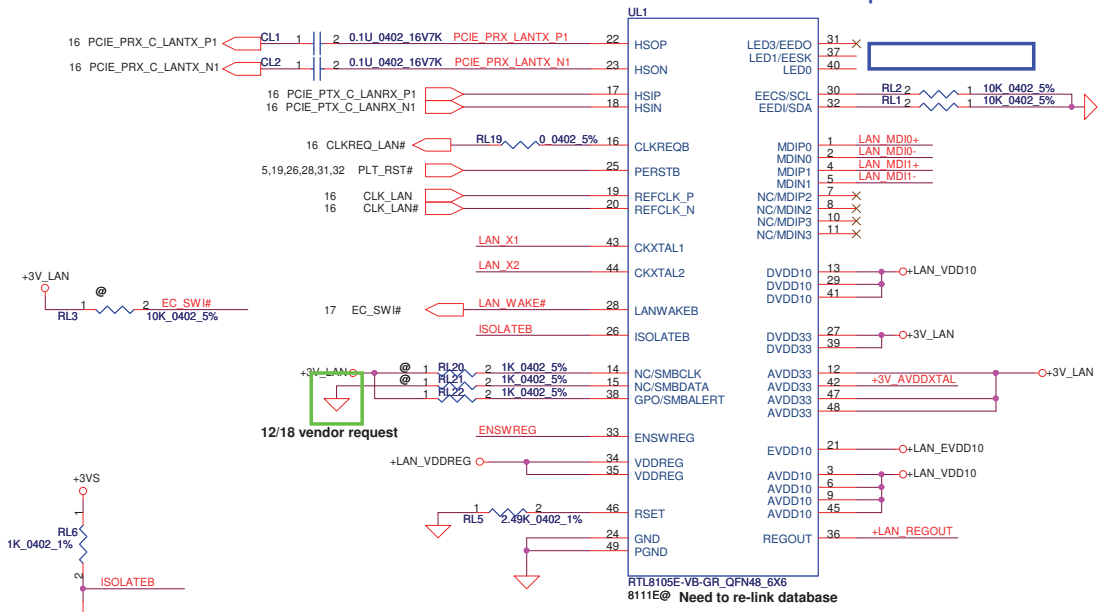
Compal Electronics, Inc.

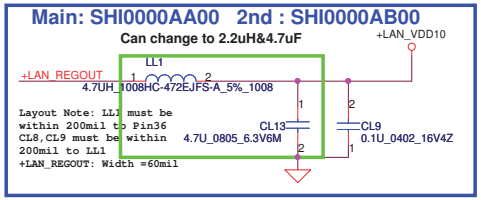
Title: PCIe-WLAN/HDDVD/NAND/NEW

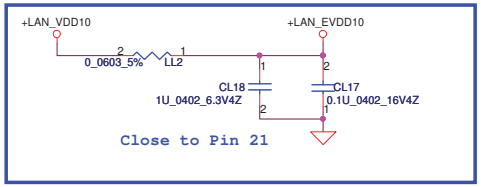
Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

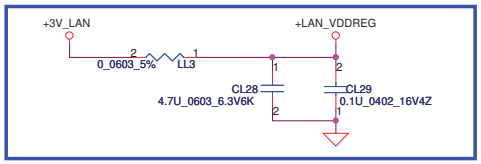
Date: Monday, April 12, 2010 Sheet 26 of 45

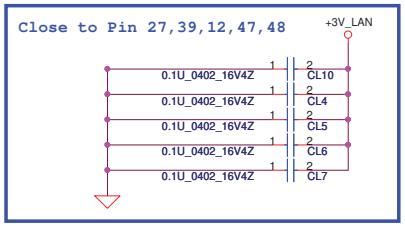
12/14 Fine tune pin define UL1 Pin37 Pin40 -->Dummy

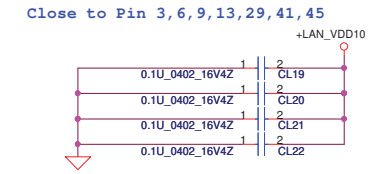


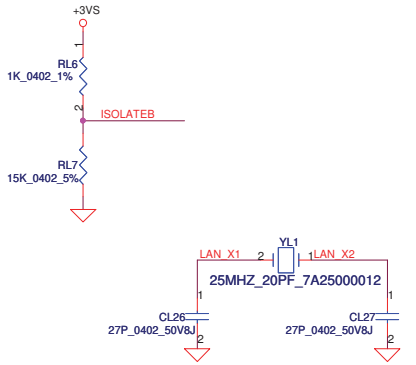


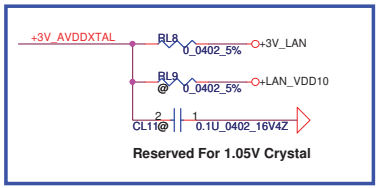


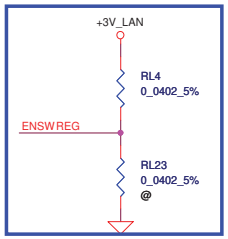


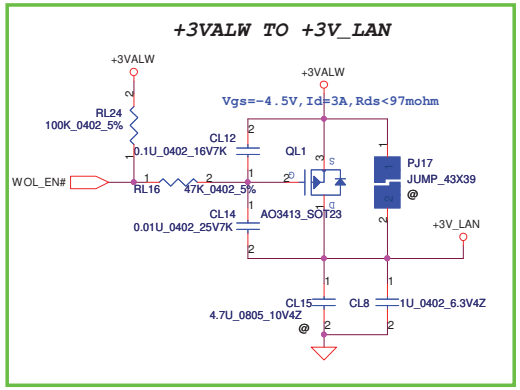


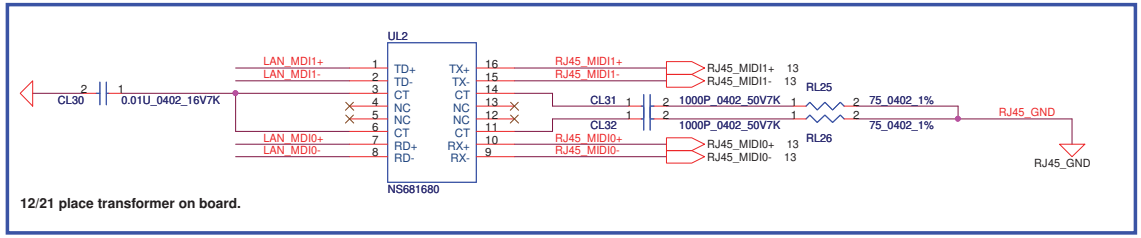












Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/02/02

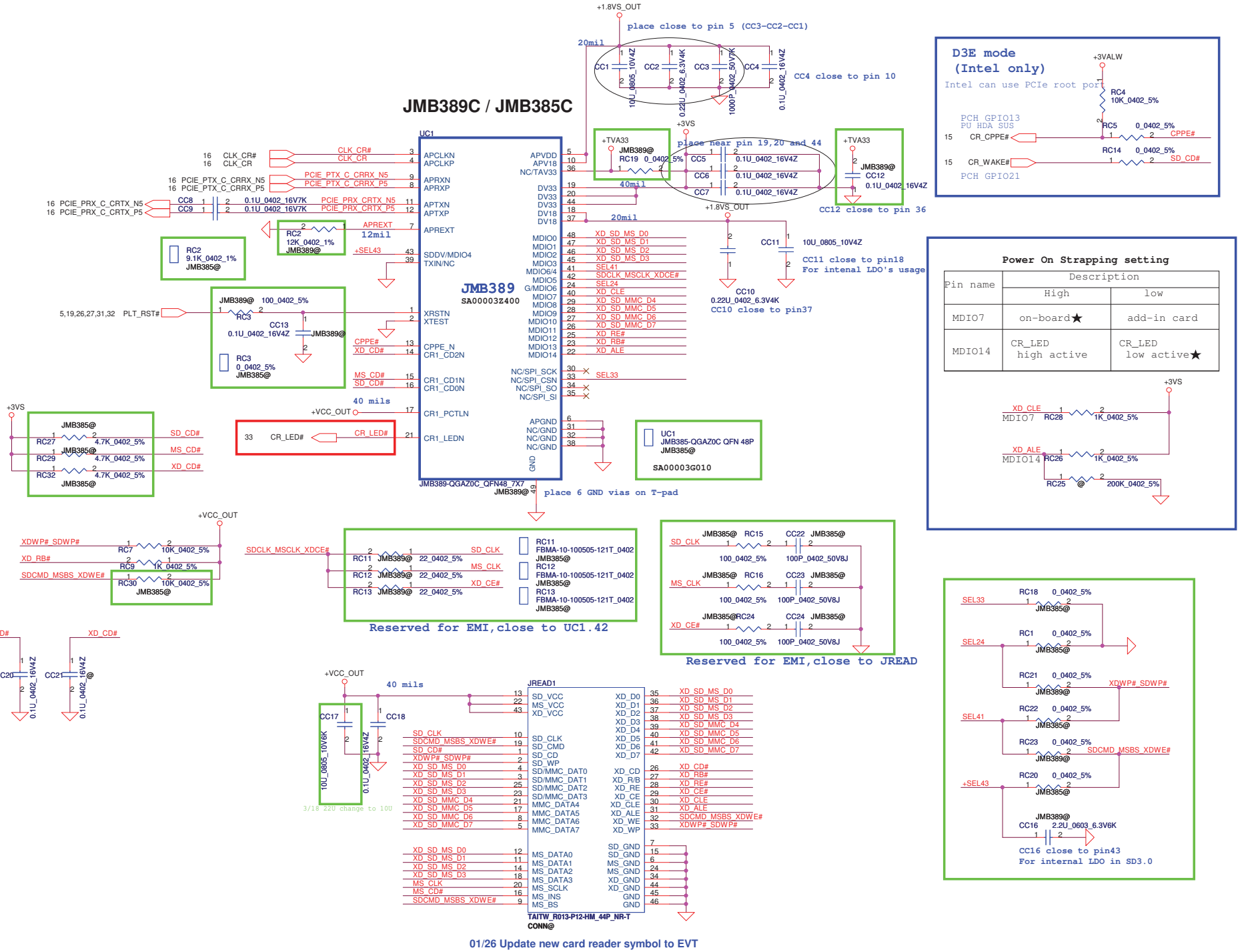
Compal Electronics, Inc.

Title: RTL8105E/RTL8111E

Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 27 of 45

JMB389C / JMB385C



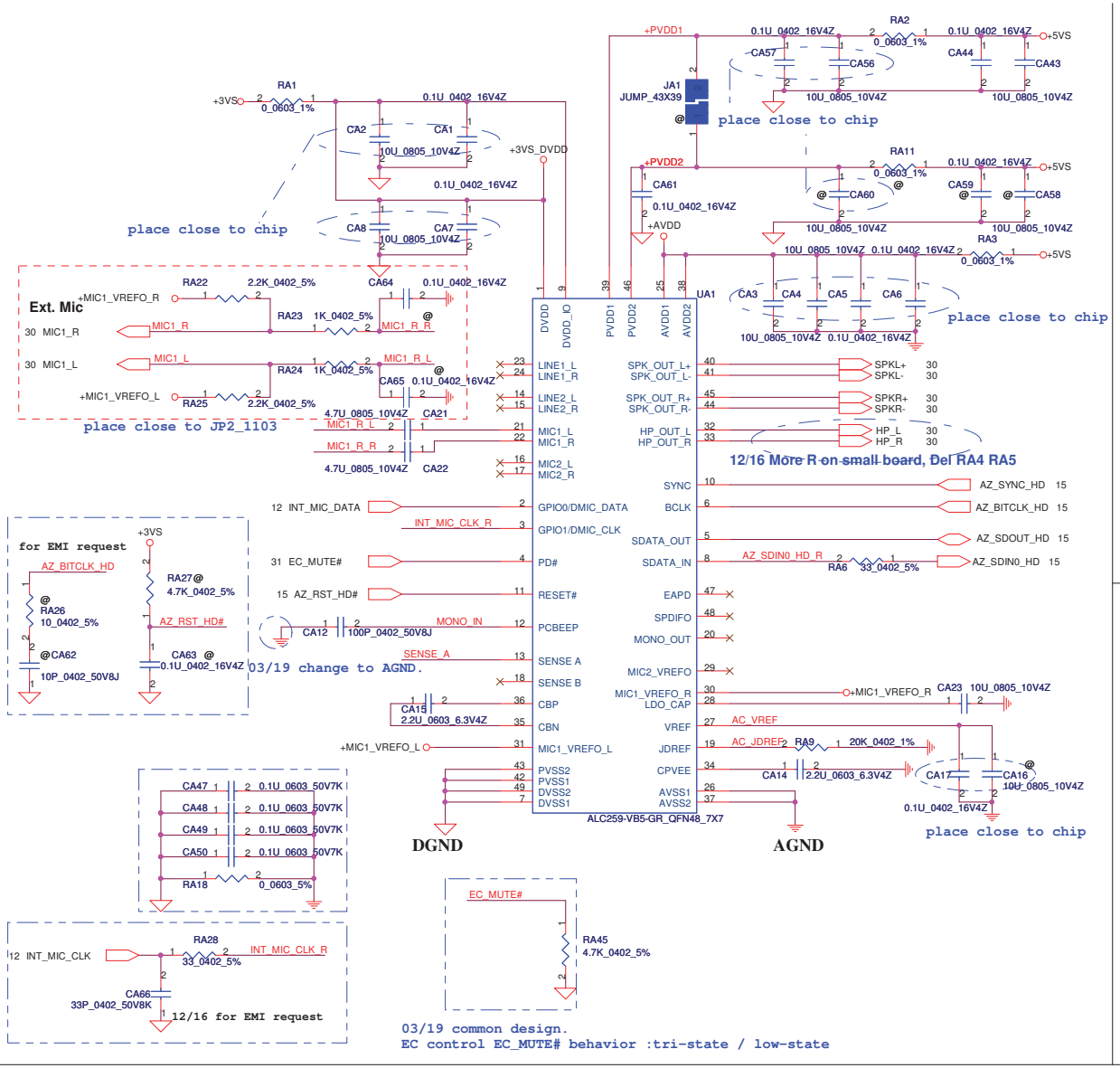
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/08

Compal Electronics, Inc.

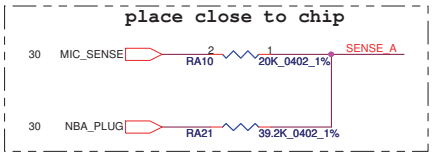
Title: **Card Reader-JMB389C/385C**

Size	Document Number	Rev
Custom	NBQAA LA6071P M/B	1.0

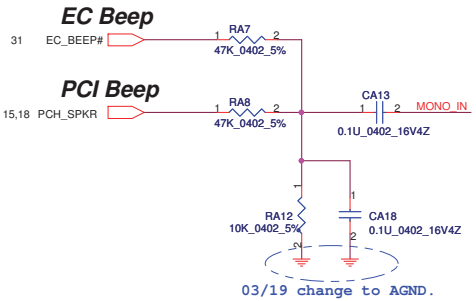
Date: Monday, April 12, 2010 Sheet 28 of 45

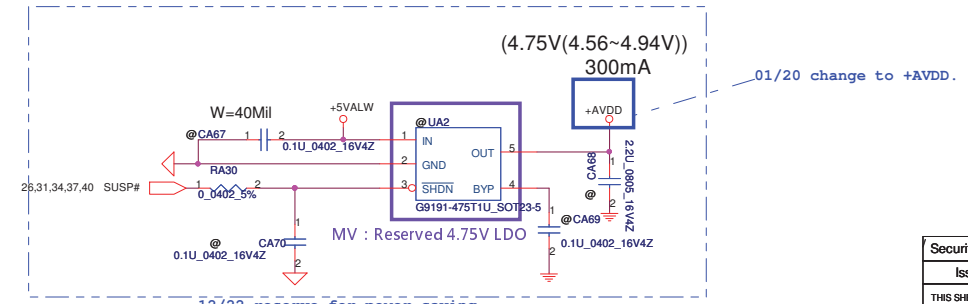


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



Beep sound



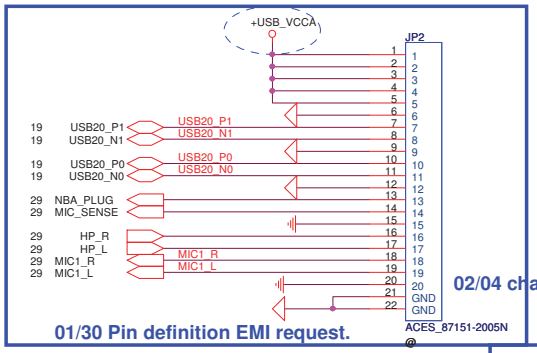


Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title: HD Audio ALC272 Codec			
Size: Custom	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 29 of 45		

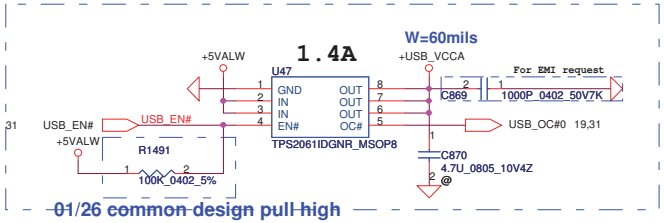
USB+Audio FFC conn
Pin=20pin, pitch=0.5

01/30 New JP2 Layout symbol reverse old conn, reserse the pin define

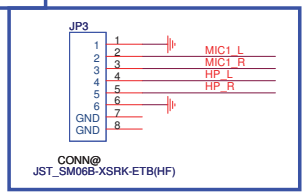


01/30 Pin definition EMI request.

02/04 change back to 20 pins.

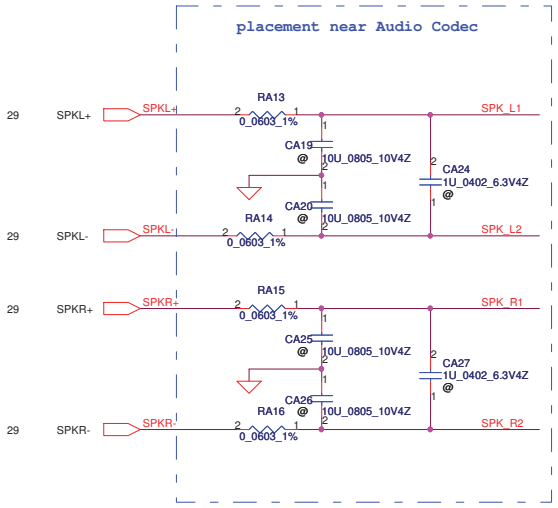


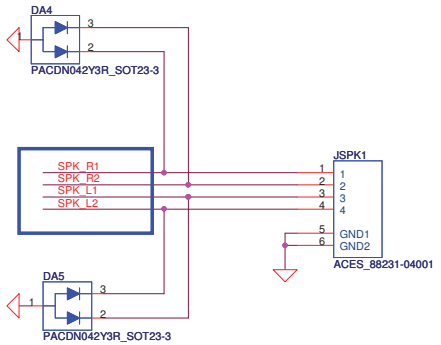
~~01/26 common design pull high~~



12/19 Reserved JP6 for audio test

Speaker Connector





12/16 Fine tune SPK_L1,SPK_L2,SPK_R1 and SPK_R2 for SPK

Compal Electronics, Inc.	
Title	AMP/Audio Jack/HP/SPEAKER/VR
Size: Custom	Document Number: NDU00_LA-6031P M/B
Rev: 1.0	
Date: Monday, April 12, 2010	Sheet 30 of 45

Use E0

U15 — KB926QFE0_LQFP128_14X14

LPC & MISC: GA20/GPIO00, KBRST#/GPIO01, SERIRQ#, LFRAME#, LAD3, LAD2, LAD1, LAD0, PCICLK, PCIRST#/GPIO05, ECRST#, SCI#/GPIO0E, CLKRUN#/GPIO1D

PWM Output: INVT_PWM/PWM1/GPIO0F, BEEP#/PWM2/GPIO10, FANPWM1/GPIO12, ACOFF/FANPWM2/GPIO13

AD Input: BATT_TEMP/AD0/GPIO38, BATT_OVP/AD1/GPIO39, ADP_I/AD2/GPIO3A, AD3/GPIO3B, AD4/GPIO42, SELIO2#/AD5/GPIO43

DA Output: DAC_BRIG/DA0/GPIO3C, EN_DFAN1/DA1/GPIO3D, IREF/DA2/GPIO3E, DA3/GPIO3F

PS2 Interface: PSCLK1/GPIO4A, PSDAT1/GPIO4B, PSCLK2/GPIO4C, PSDAT2/GPIO4D, TP_CLK/PSCLK3/GPIO4E, TP_DATA/PSDAT3/GPIO4F

SPI Device Interface: SDICS#/GPXOA00, SDICLK/GPXOA01, SDIDO/GPXOA02, SDIDI/GPXID0

SPI Flash ROM: SPIDI/RD#, SPIDO/WR#, SPICLK/GPIO58, SPICS#

Int. K/B Matrix: KSI0/GPIO30 … KSI7/GPIO37, KSO0/GPIO20 … KSO17/GPIO49

GPIO: CIR_RX/GPIO40, CIR_RLC_TX/GPIO41, FSTCHG/SELIO#/GPIO50, BATT_CHGI_LED#/GPIO52, CAPS_LED#/GPIO53, BATT_LOW_LED#/GPIO54, SUSP_LED#/GPIO55, SYSON/GPIO56, VR_ON/XCLK32K/GPIO57, AC_IN/GPIO59

SM Bus: SCL1/GPIO44, SDA1/GPIO45, SCL2/GPIO46, SDA2/GPIO47

GPIO: PM_SLP_S3#/GPIO04, PM_SLP_S5#/GPIO07, EC_SMI#/GPIO08, LID_SW#/GPIO0A, SUSP#/GPIO0B, PBTN_OUT#/GPIO0C, EC_PME#/GPIO0D, EC_THERM#/GPIO11, FAN_SPEED1/FANFB1/GPIO14, FANFB2/GPIO15, EC_TX/GPIO16, EC_RX/GPIO17, ON_OFF/GPIO18, PWR_LED#/GPIO19, NUMLED#/GPIO1A

GPO: EC_RSMRST#/GPXO03, EC_LID_OUT#/GPXO04, EC_ON/GPXO05, EC_SWI#/GPXO06, ICH_PWROK/GPXO06, BKOFF#/GPXO08, WL_OFF#/GPXO09, GPXO10, GPXO11

GPI: PM_SLP_S4#/GPXID1, ENBKL/GPXID2, GPXID3, GPXID4, GPXID5, GPXID6, GPXID7

XCLK1, XCLK0, V18R, +EC_V18R

for EMI request

1013 EMC request

to avoid EC entry ENE test mode

Add pull high_1130

03/10 for Y4 remove.

01/27 toshiba request

03/23 add current resistance.

12/17 EC recommend

12/16 EMI request

EC_SEL	EC Version
High	KB926D3
Low	KB926E0

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: ENE-KB926 RevD2

Size: | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

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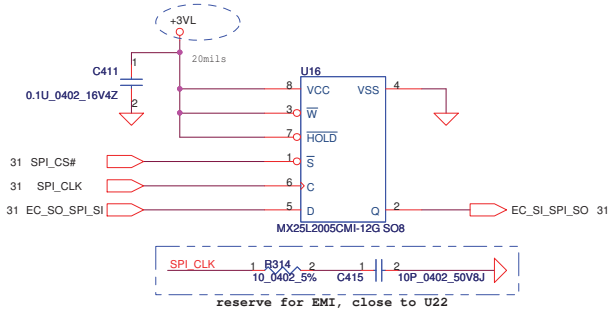
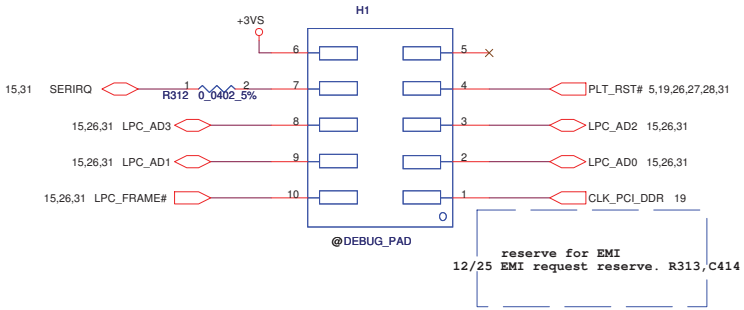
SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

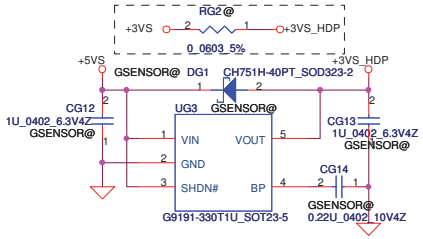


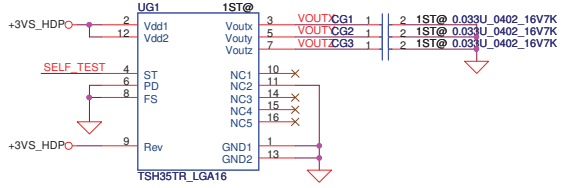
LPC Debug Port

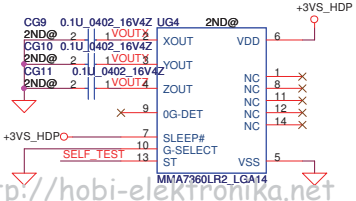
Please place the PAD under DDR DIMM.

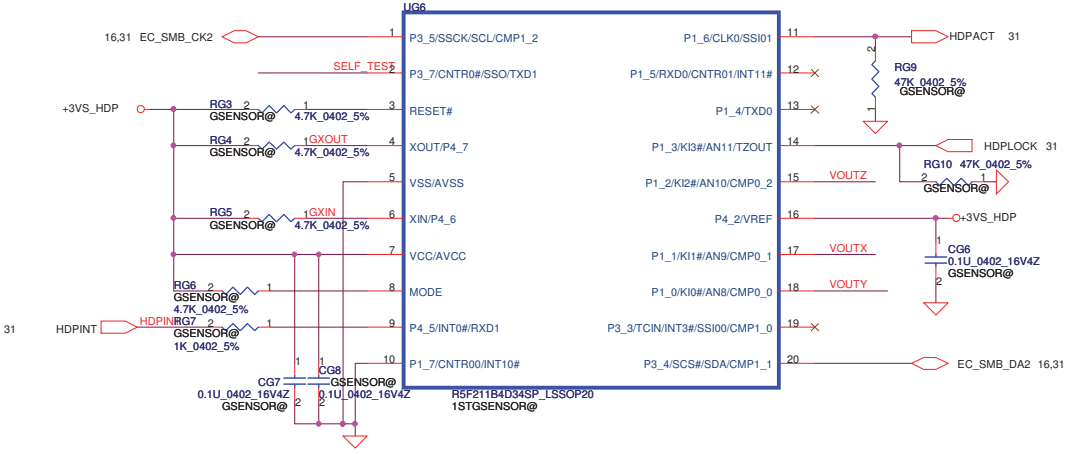


G-Sensor





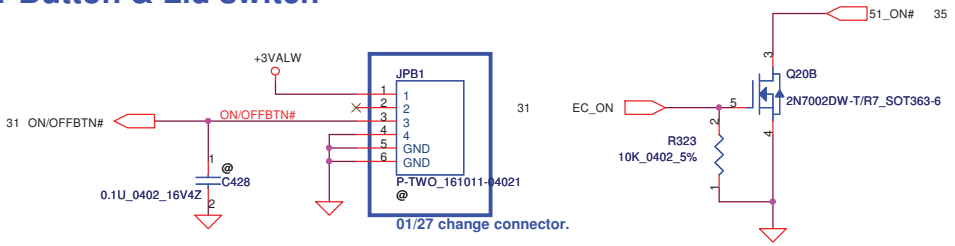




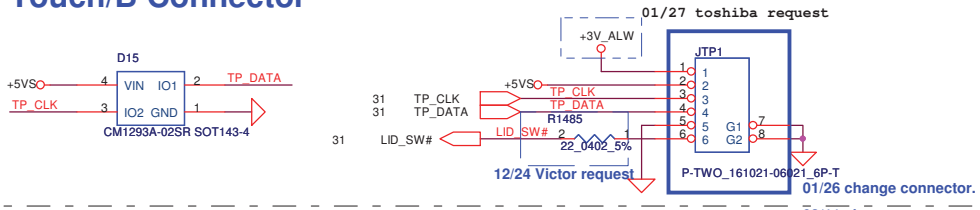
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title: SPI/LPC/PS2/MDC/FM/CIR			
Size: Custom	Document Number: NDU00_LA-6031P M/B		Rev: 1.0
Date: Monday, April 12, 2010	Sheet 32 of 45		

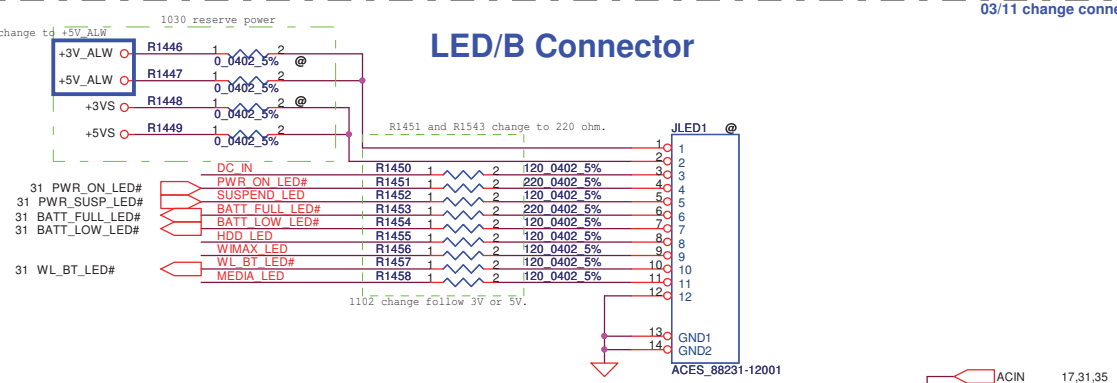
Power Button & Lid switch

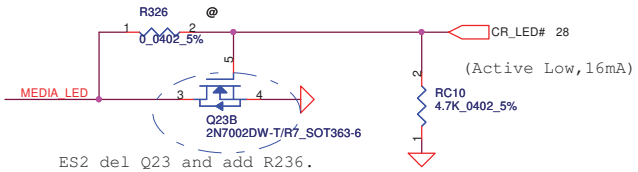


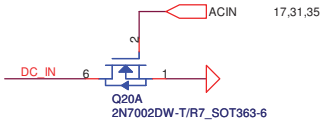
Touch/B Connector

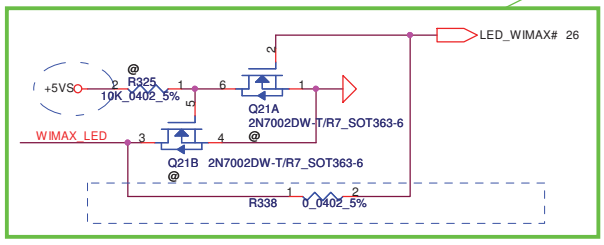


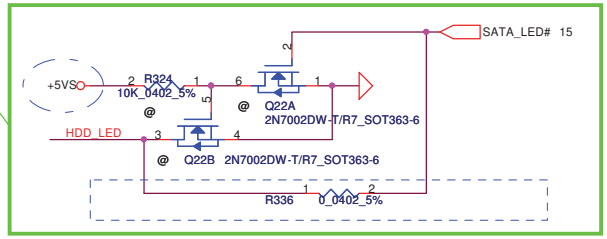
LED/B Connector





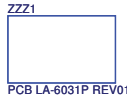




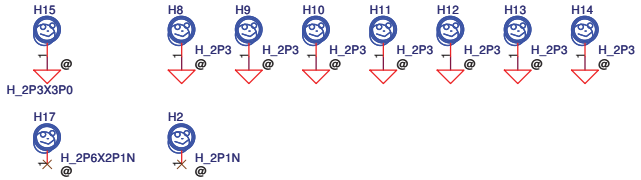


ISPD

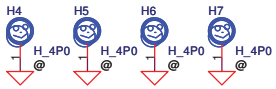
PCB



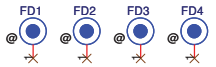
Screw Hole

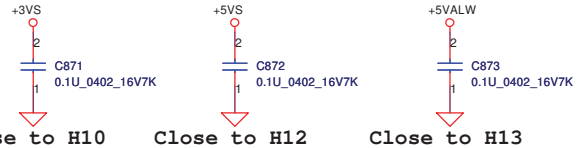


CPU



PCB Fedical Mark PAD





Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

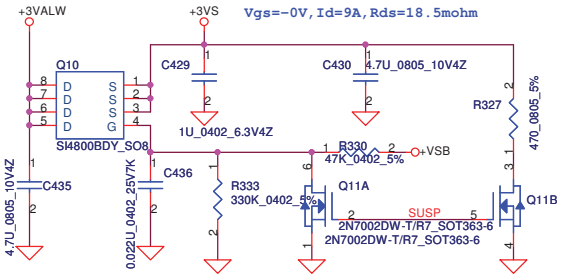
Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS

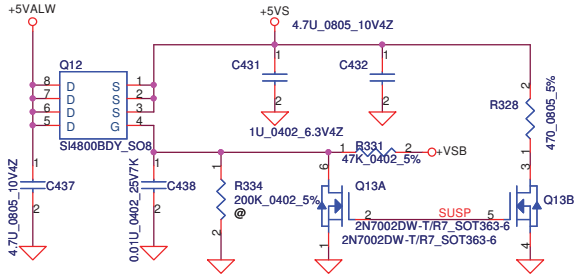
Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

Date: Monday, April 12, 2010 | Sheet 33 of 45

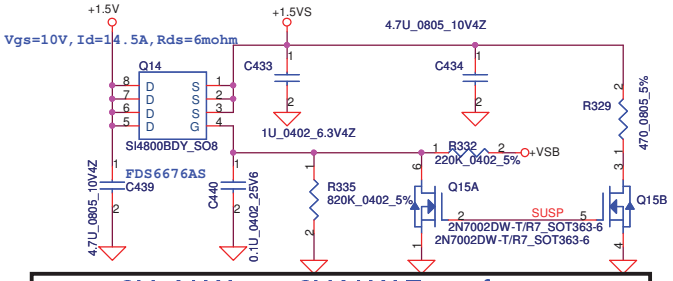
+3VALW TO +3VS



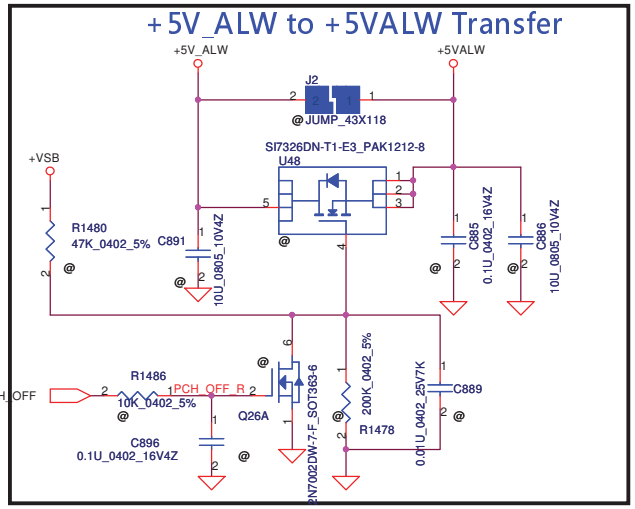
+5VALW TO +5VS



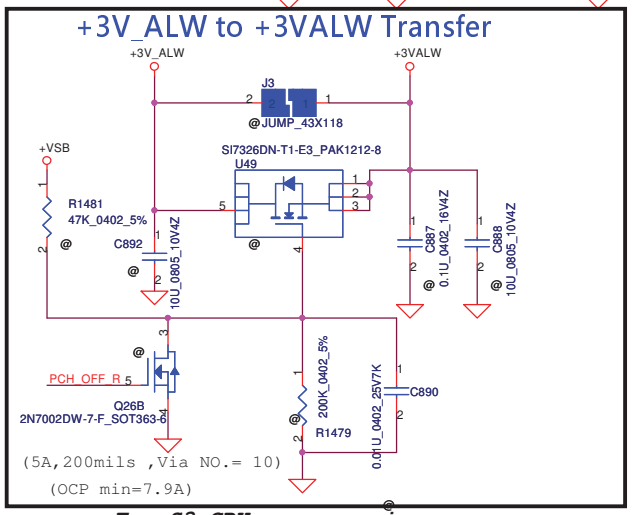
+1.5V to +1.5VS



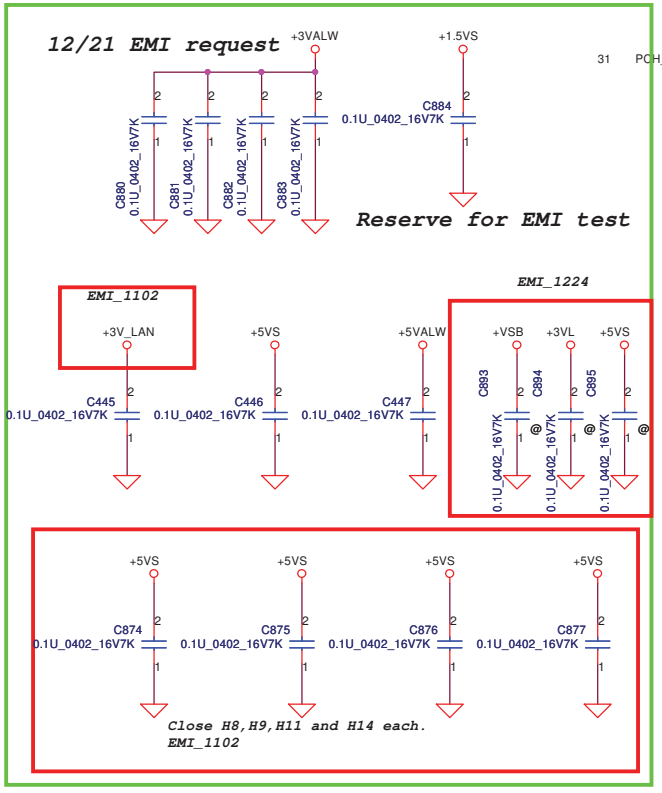
+5V_ALW to +5VALW Transfer



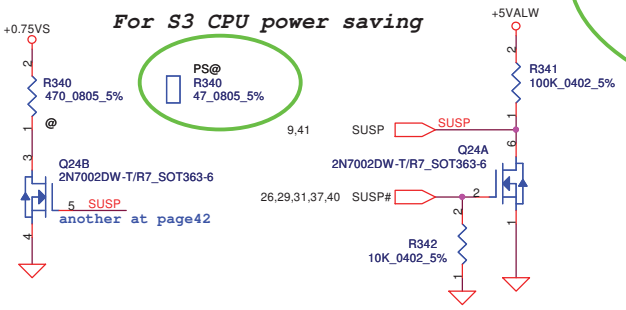
+3V_ALW to +3VALW Transfer



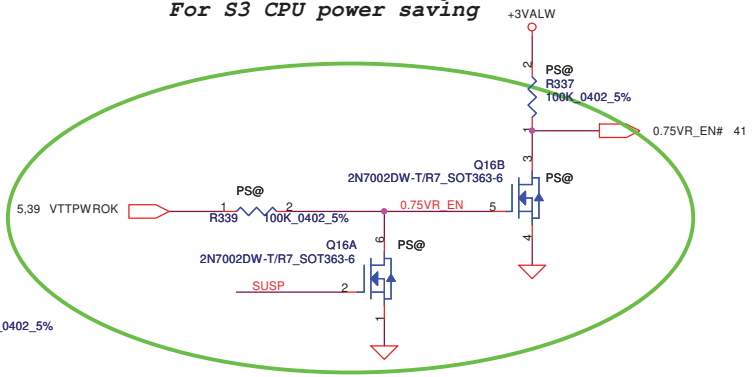
12/21 EMI request



For S3 CPU power saving



For S3 CPU power saving



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0

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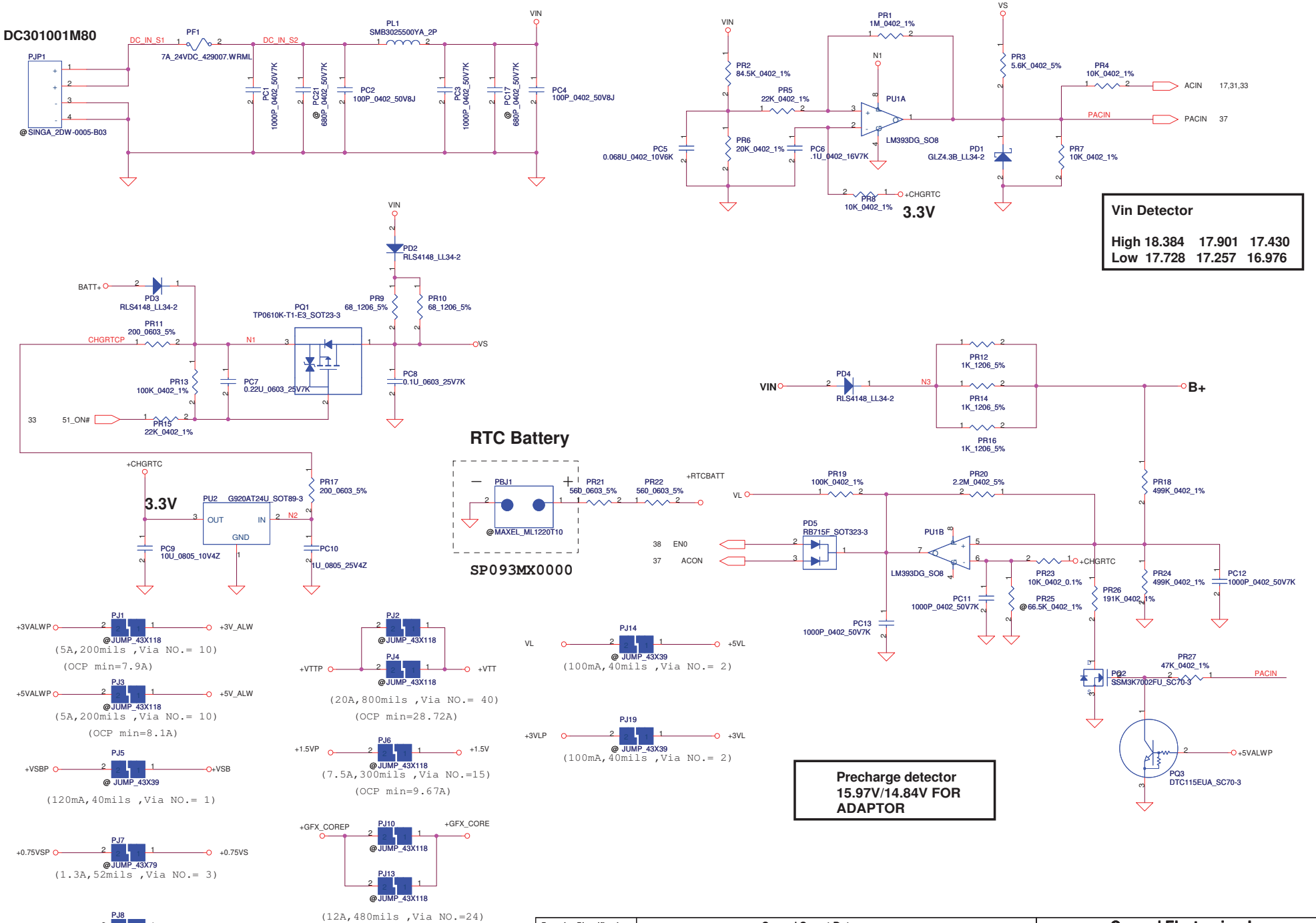

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: DCIN / DETECTOR

Size	Document Number	Rev
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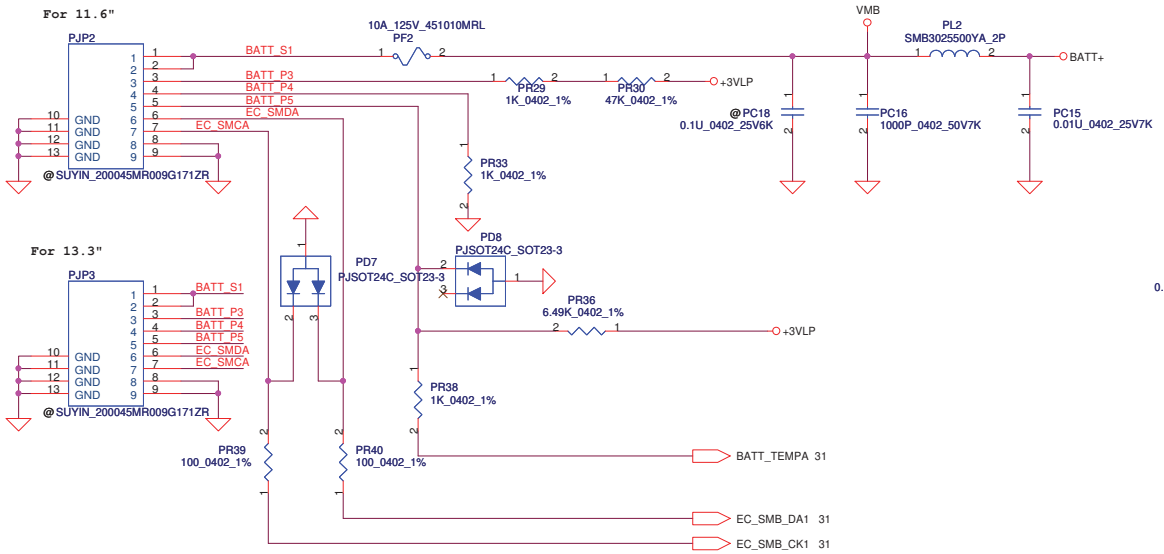
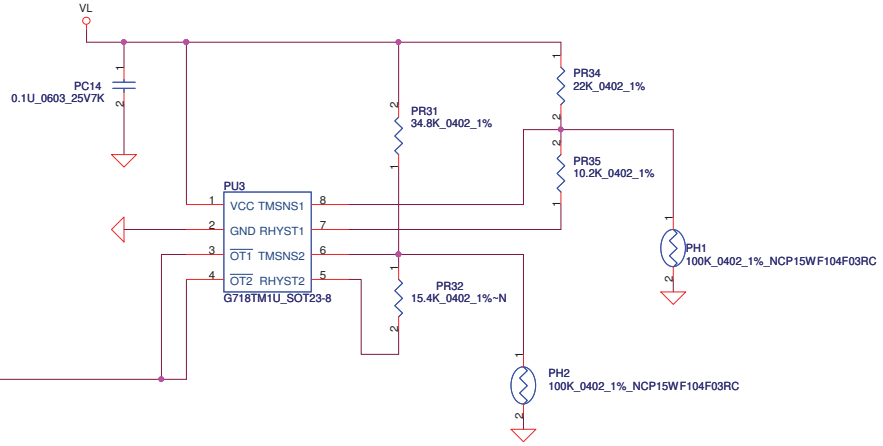
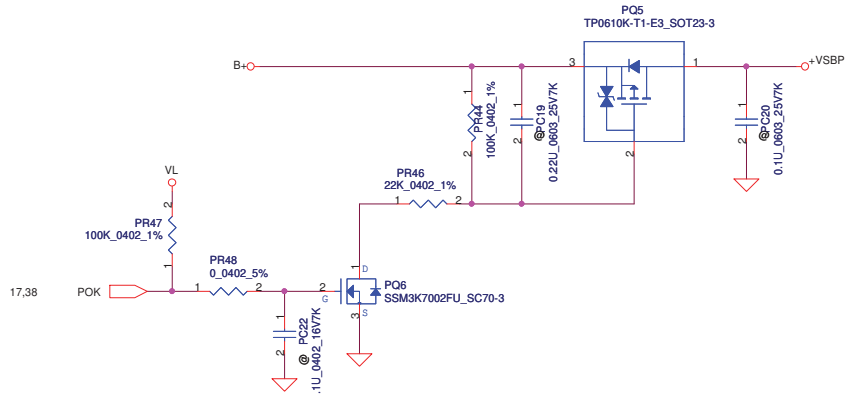
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

PH2 near main battery CONN:
BAT.thermal protection at 78 degree C
Recovery at 42 degree C

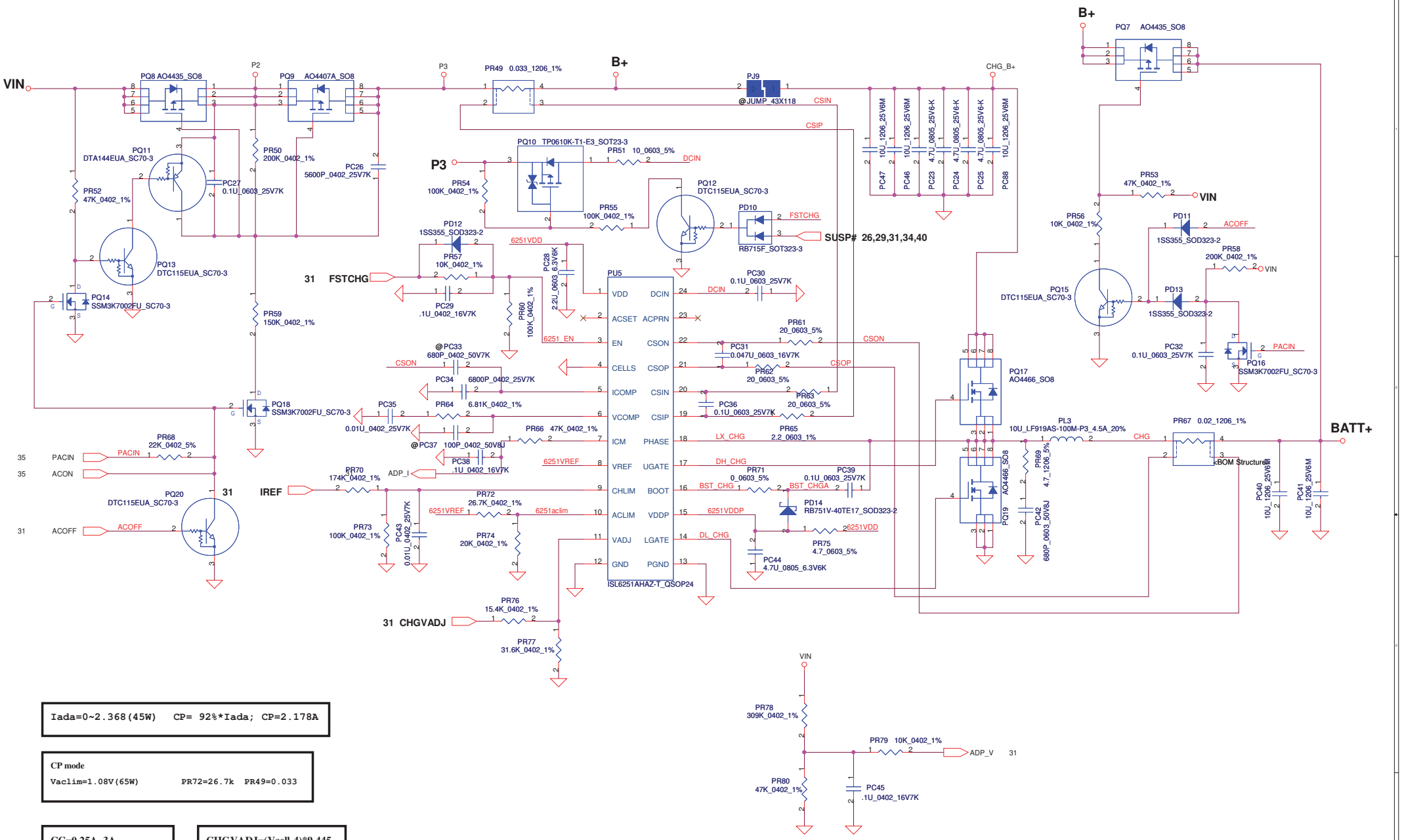






Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title	BATTERY CONN / OTP		
Size	Document Number LA-6031P		Rev 1.0
Date: Monday, April 12, 2010		Sheet 36 of 45	



Iada=0~2.368(45W) CP= 92%*Iada; CP=2.178A

CP mode

Vaclim=1.08V(65W) PR72=26.7k PR49=0.033

CC=0.25A~3A
IREF=1.096*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: LA-6031P | Rev: 1.0

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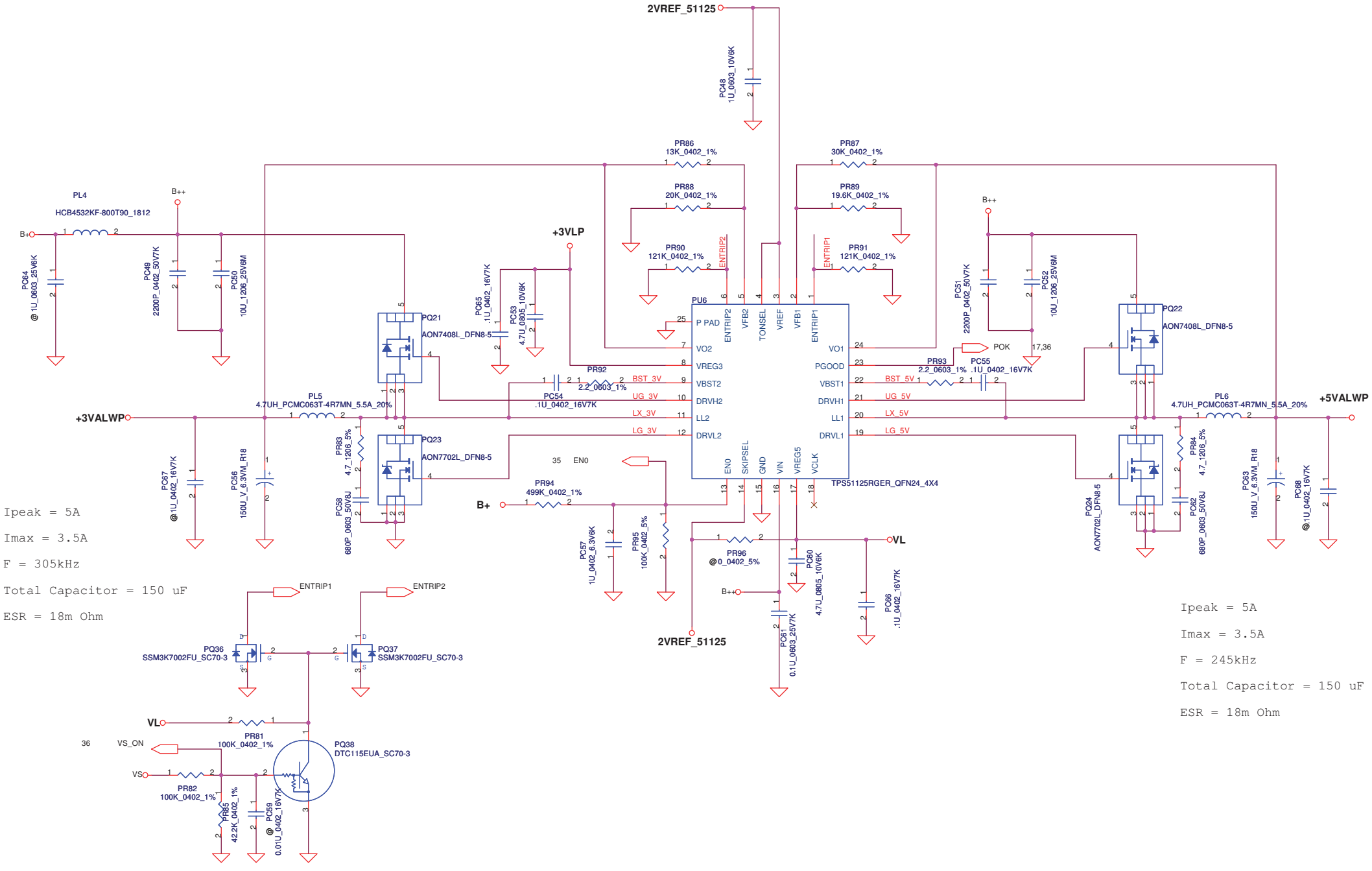
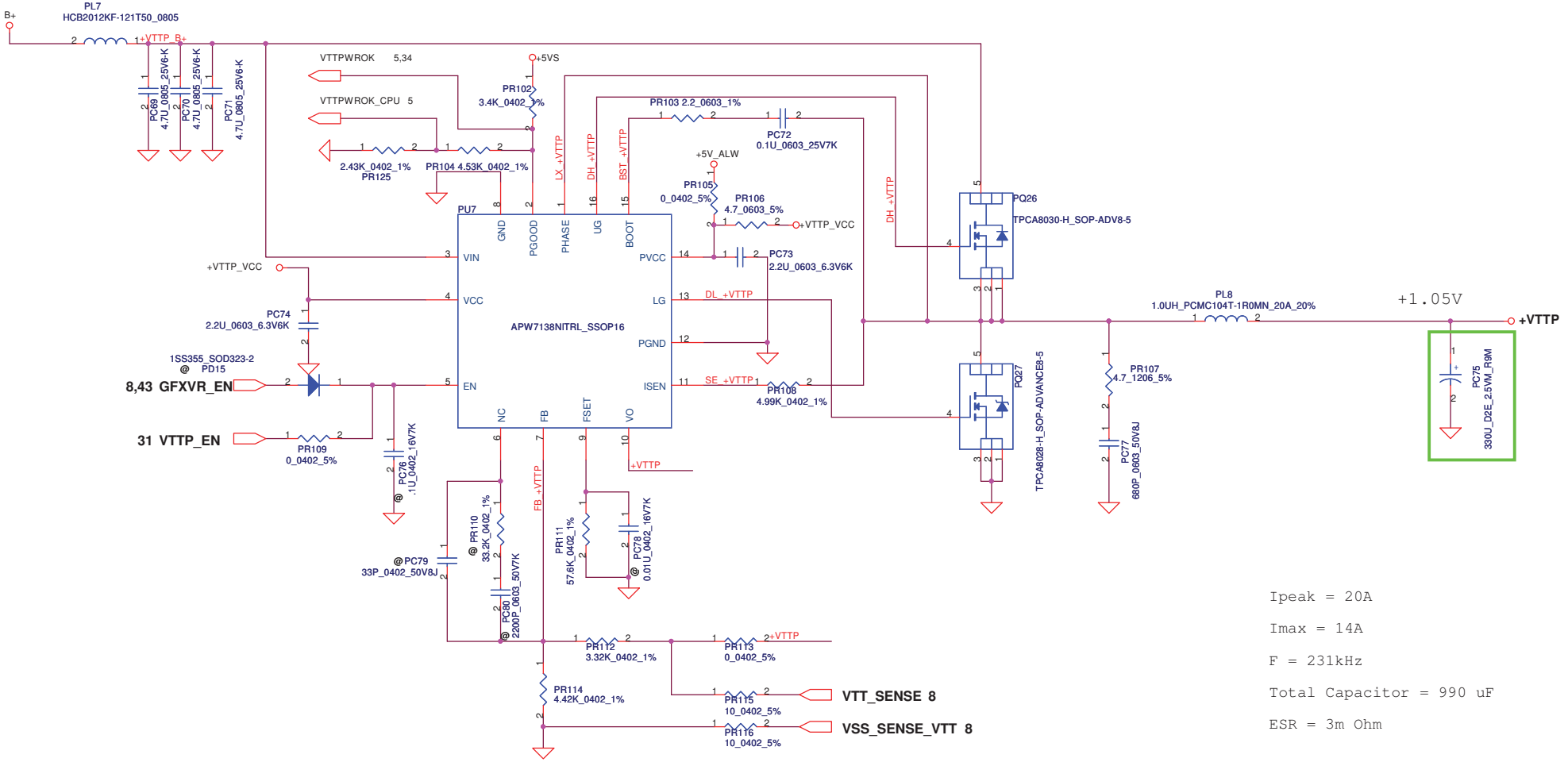


Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

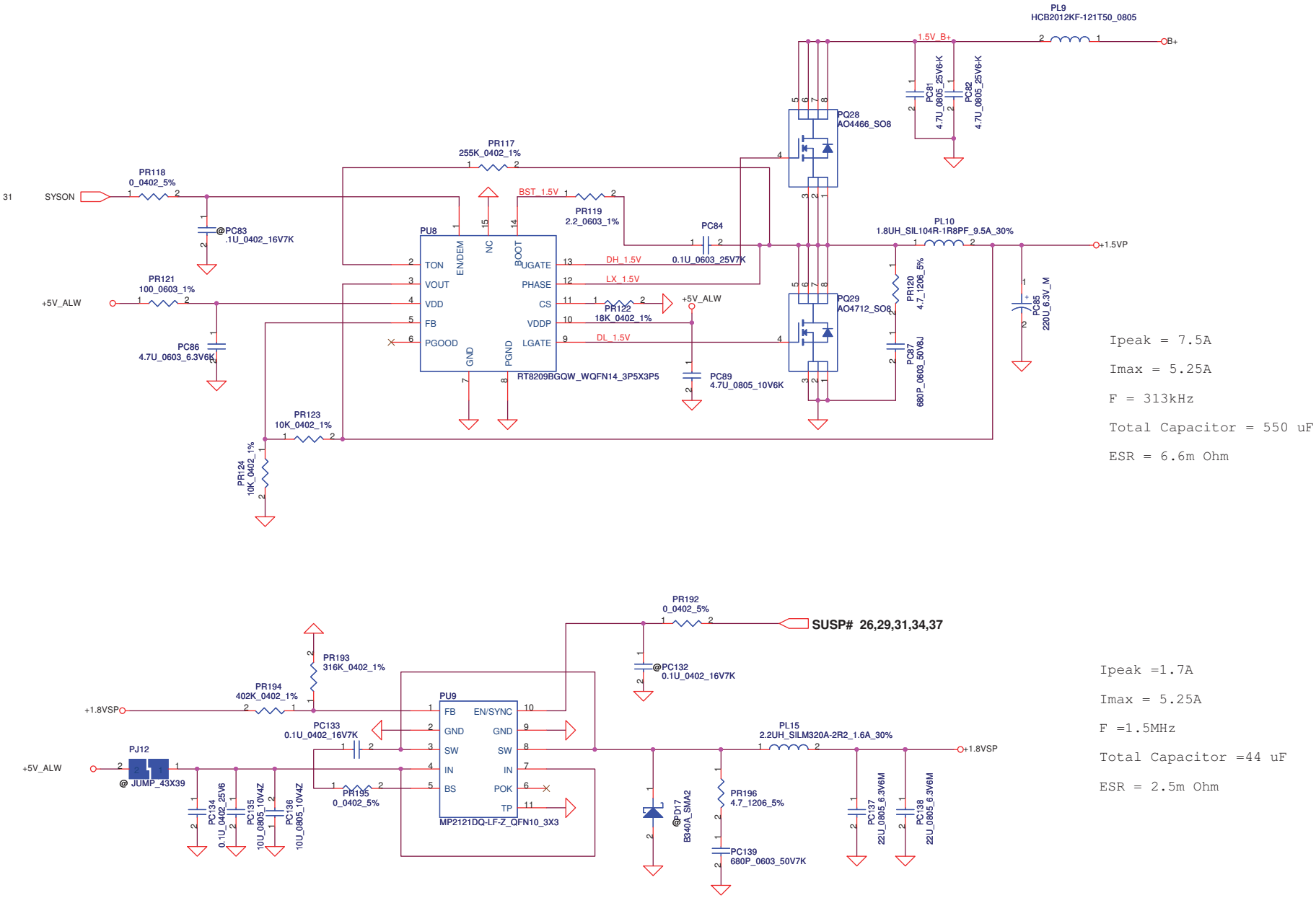
Title	+5VALWP/+3VALWP	
Size	Document Number: LA-6032P	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 38 of 45	



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/01/23

Compal Electronics, Inc.

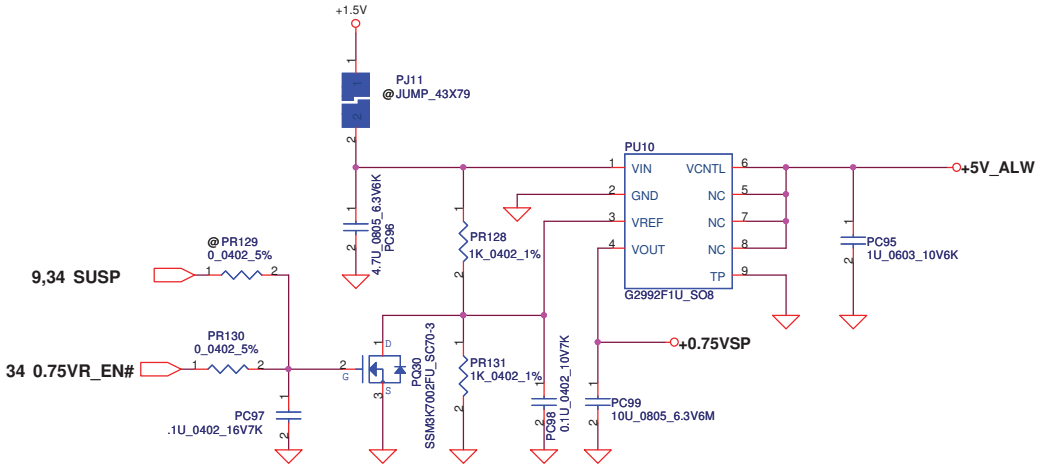
Title	+VTTP	
Size	Document Number	Rev
	NDU00_LA-6031P M/B	1.0
Date: Monday, April 12, 2010	Sheet 39 of 45	



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

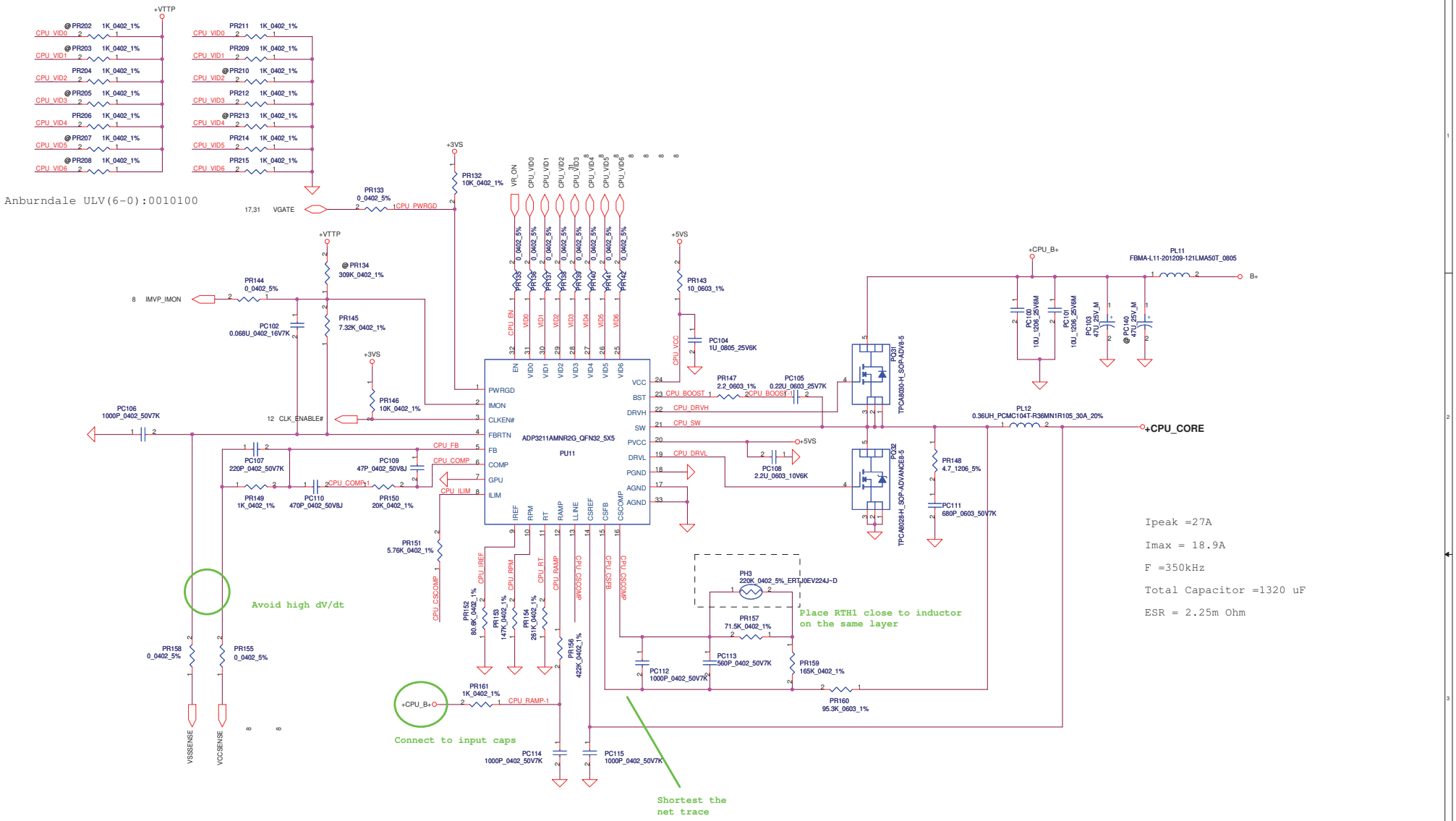
Title	+1.5VP/+1.8VSP	
Size: Custom	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 40 of 45	



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title	0.75VSP	
Size	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
Date: Monday, April 12, 2010	Sheet 41 of 45	



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

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Compal Electronics, Inc.

Title: +CPU_CORE

Size | Document Number: NDU00_LA-6031P M/B | Rev: 1.0

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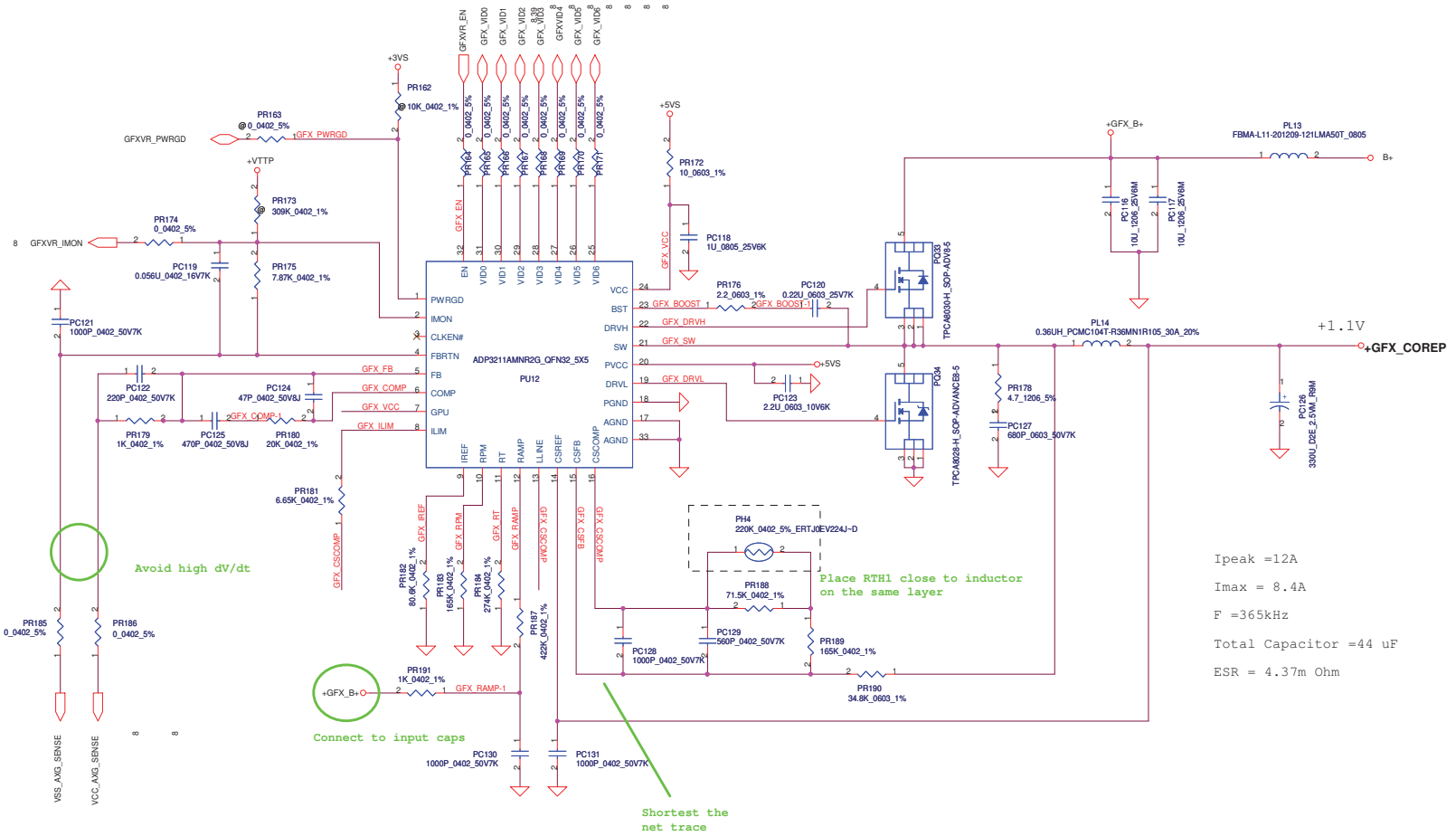

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/02
Title	+GFX		
Size	Document Number		Rev
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2009/11/9(EVT)	P38 +5VALWP/+3VALWP	PC54,PC55,PC65,PC66 change SE076104KM8 to SE076104K80	change to A51 material
	2009/11/9(EVT)	P39 +VTTP	Resever PD15	Design change
	2009/11/9(EVT)	P41 +0.75VSP	Change PQ30 to SB000009610	Design change
	2009/11/9(EVT)	P42 CPU_CORE	Change PU11 change to ADP3211	Design change
	2009/11/9(EVT)	P42 CPU_CORE	Change PH3 &PH4	change to A51 material
	2009/11/9(EVT)	P37 CHARGE	Change PR49 change to 33m	Design change
	2009/11/9(EVT)	P38 +5VALWP/+3VALWP	PR90 & PR91 change to 121K	Design change
	2009/12/1(DVT)	P39 +CPU-CORE	Add PR202~PR215 pull-up & pull-down	Design change
	2009/12/17(DVT)	P36 Battery	Change PR31,PR32,PR34,PR35	Design change
	2009/12/17(DVT)	P37 CHARGE	Change PC23,PC24,PC25,PC81,PC82 1206 to 0805	Design change
	2009/12/22(DVT)	P42 CPU_CORE	Change PR147 0 ohm change to 2.2 ohm	EMI commond
	2009/12/22(DVT)	P43 GFX	Change PR176 0 ohm change to 2.2 ohm	EMI commond
	2009/12/22(DVT)	P39 +VTTP	ADD material PR125 & PR104 & PR102 and add net VTTPWORK_CPU	Design change
	2010/01/25(PVT)	P36 Battery	Add PD7,PD8	EMI require
	2010/01/27(PVT)	P37 CHARGE	Add 10u x3 PC46,PC47,PC88	EMC require
	2010/02/04(PVT)	P41 +0.75VSP	Resever PR129 Add PR130 and PC97	Design change
	2009/02/04(PVT)	P38 +5VALWP/+3VALWP	Change PQ38	Design change
	2010/02/04(PVT)	P42 CPU_CORE	Change PR160 to 95.3K and PR145 to 7.32K	Design change
	2010/02/08(PVT-2)	P36 Battery	Change PR21&PR22 and +CHGRTC	Design change

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/02

Compal Electronics, Inc.		
Title: Power PIR		
Size	Document Number: NDU00_LA-6031P M/B	Rev: 1.0
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Intel S3 power saving	05	Install Q1, R1484, C878, R8, R40 and Remove R2, R42	12/25	DVT
2	HDMI Detection function	14	modify HDMI_HPD circuit (Remove U7)	12/25	DVT
3	Sleep charge control method change	19 & 31	SLP_CHG_M3_R & SLP_CHG_M4_R change from PCH to Pin103 & 74 of EC	12/25	DVT
4	Implement Low power HDA	22	Reserve R1468 & R1469 for 1.5VALW (Low Power HDA)	12/25	DVT
5	Debug usage	26	Reserve LPC bus at WLAN solt	12/14	DVT
6	LAN circuit change for Vendore request	27	RL21 contact to GND	12/18	DVT
7	Avoid power leakage & reduce double pull up	27	Remove RL3	12/25	DVT
8	Transformer change	27	Move Transformer from Sub-board to M/B	12/21	DVT
9	Prevent Card Reader IC damagewhen insert dummy card	28	Add F2	12/24	DVT
10	Audio PD# issue (Could not work)	29	Add RA29 pull up	12/19	DVT
11	Avoid Audio noise	29	reserve and unistall CA70, CA68, CA69, UA2, RA30, CA67	12/22	DVT
12	Enhance Right side USB ability	30	modify JP2 pin assignment and reserve JP3 pad for test	12/19	DVT
13	Sleep charge control method change	31	add pin 21 of EC for control ALW power MOS	12/21	DVT
14	Sleep charge control method change	34	add two V_ALW power transfer circuits (3V_ALW to 3VALW & 5V_ALW to 5VALW)	12/21	DVT
15	system idle hang up issue	8	CPU_PSI# Pull down 1k ohm & H_DPRSLPVR pull up 1k ohm to Vtt	12/19	DVT
16	Sleep charge control method change	24	change U14 power from 5VALW to 5V_ALW	12/21	DVT
17					
18	EC_SWI# pull up twice. R190	27	RL3 reserved.	01/20	PVT
19	Audio LDO reserved for AVDD.	29	UA2 pin 5 for +AVDD	01/20	PVT
20	For S3 power saving.	05	Reserve R2 and change R1484 to 0 ohm.	01/20	PVT
21	For 3G LED flash when resume from S3.	33	Reserve Q21 and Q22 circuit. Add R338 and R336.	01/20	PVT
22	Don't need discharge circuit.	34	Modify Q26 and Q27 circuit.	01/20	PVT
23	Reserve for PCH and EC both.	19,24,31	Add R1487,R1488,R1489 and R1490.	01/20	PVT
24	Change JHDD1 pin 4 to GND.	24		01/20	PVT
25	Add BT power control circuit.	26	Add D85 and Q27.	01/20	PVT
26	change cardreader connector.	28	ME request	01/26	PVT
27	change LED always power	33	3G LED flash issue.	01/26	PVT
28	change TP connector.	33	ME request	01/26	PVT
29	JGSIM2 connector.	26		01/26	PVT
30	add R1491 in USB_EN#	30		01/26	PVT
31	Lid switch change to +3V_ALW	31,33	Toshiba request.	01/26	PVT
32	add USB port 9 and PCIe port 4 for 8 pin SIM card.	16,19,26		01/27	PVT
33	add R1494 and D84 near D5 and add L,C near U8	15,18	EMI request	02/03	PVT
34	change MIC1_R and MIC1_L pull high.	29	MIC issue.	02/03	PVT
35	JLVDS1 pin24 change to NC.	12	Common design.	03/04	PVT2
36	CRT trace modify.	18	wrong trace.	03/04	PVT2
37	D5 layout close to PCH (U8)		layout change.	03/04	PVT2
38	Change O2 to JMicron card reader.	28		03/22	PVT2
39	USB OC# change.	19	Common design.	03/22	PVT2
40	Add R1505.	17	EMI request	03/22	PVT2

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: PIR

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