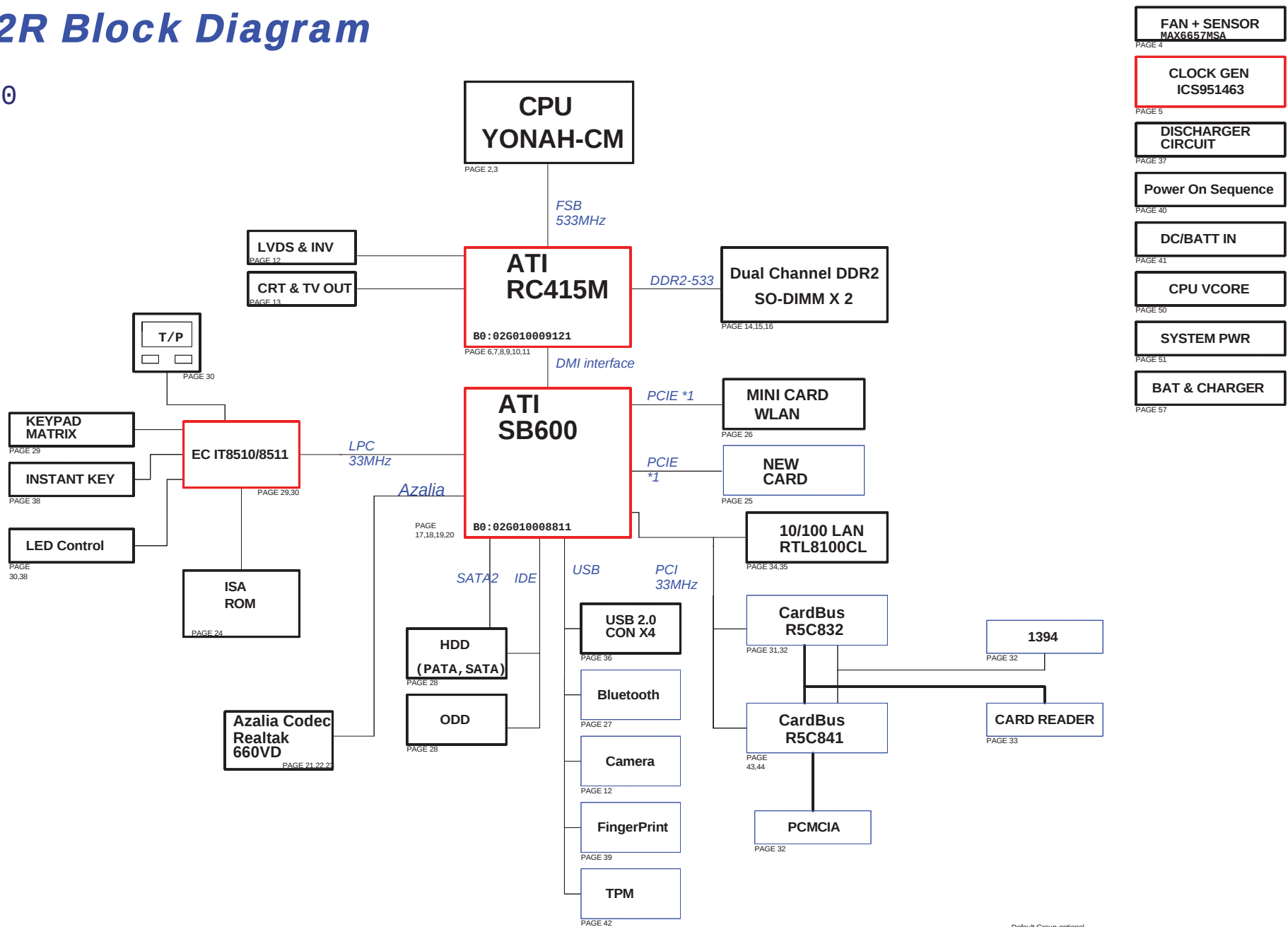


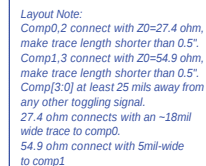
T12R Block Diagram

V2.0





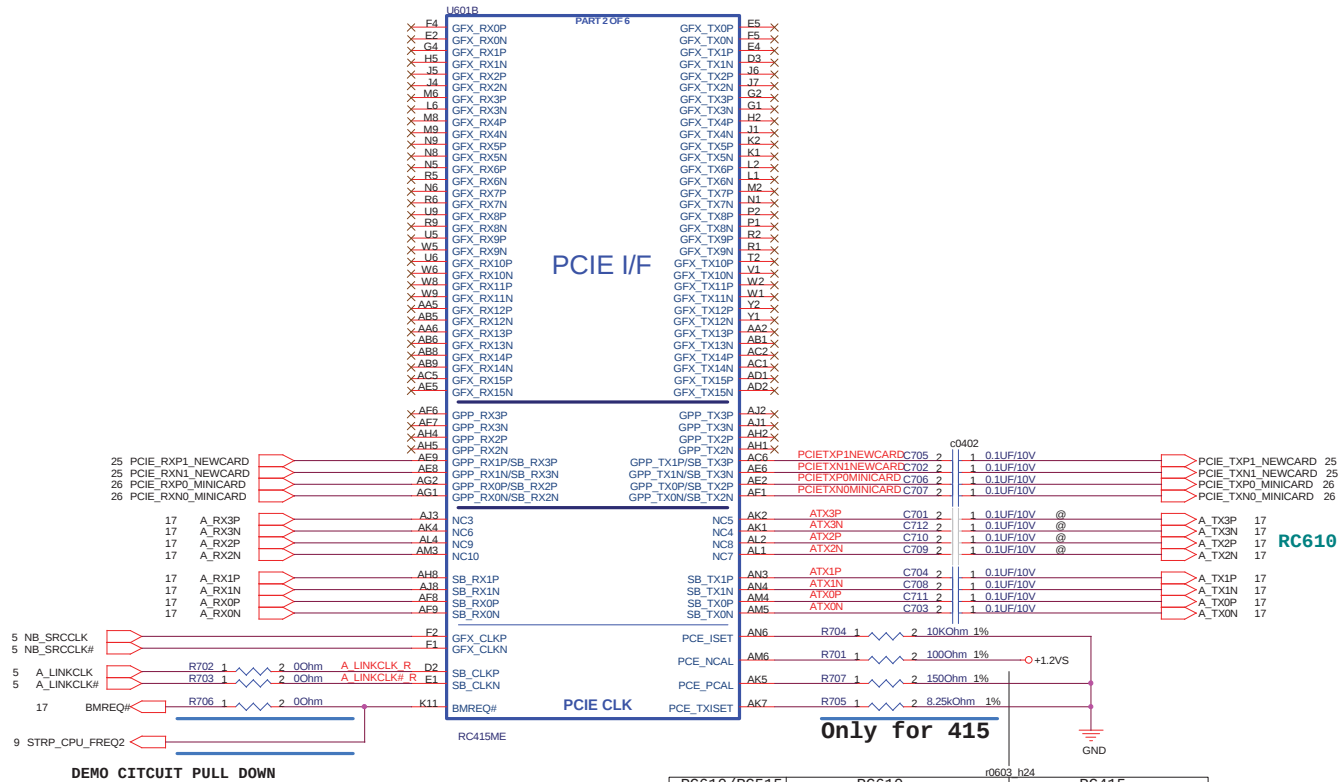
V1.1 ME



68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

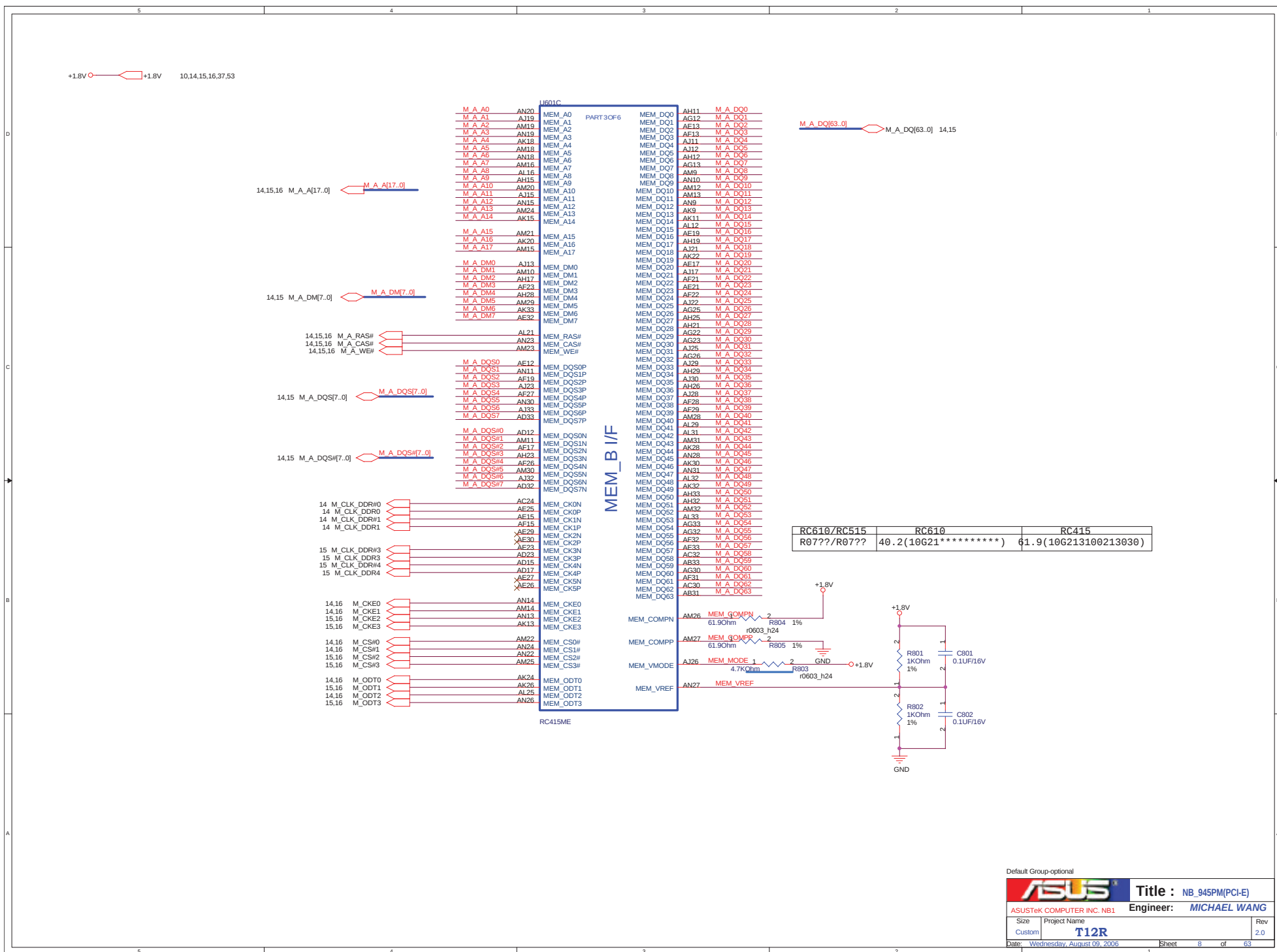


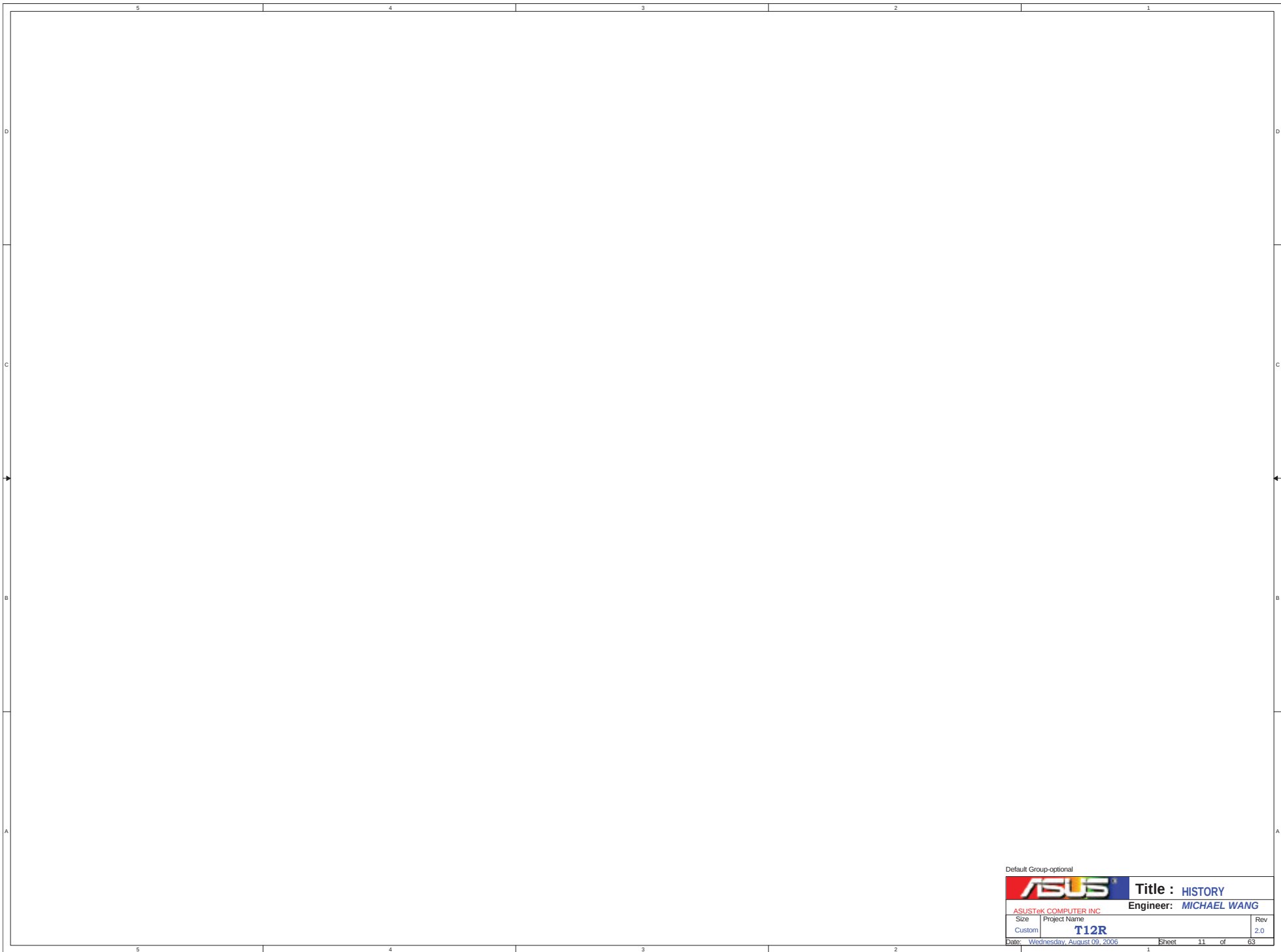
+1.2VS  +1.2VS 6,9,10,20,37,61

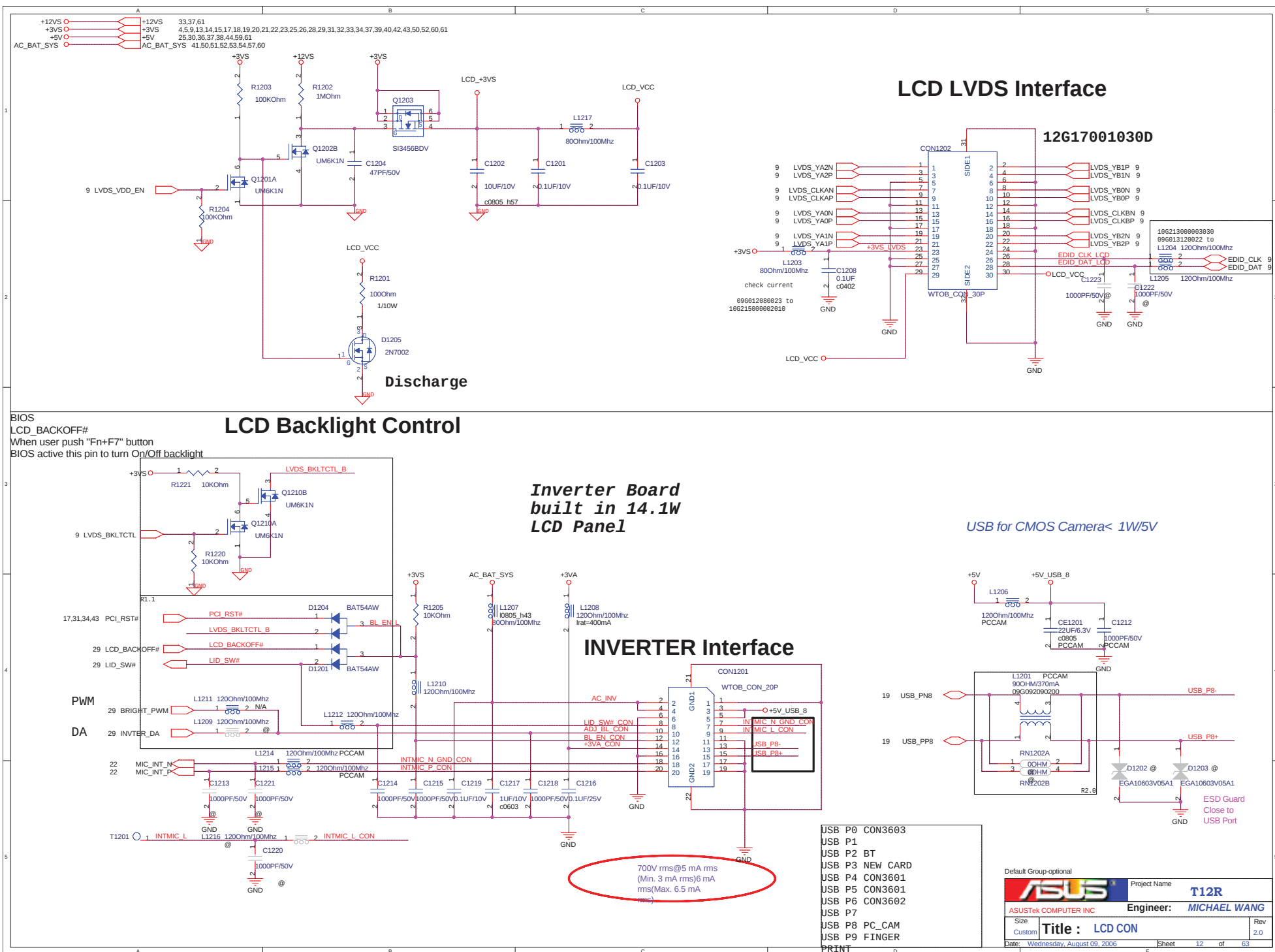


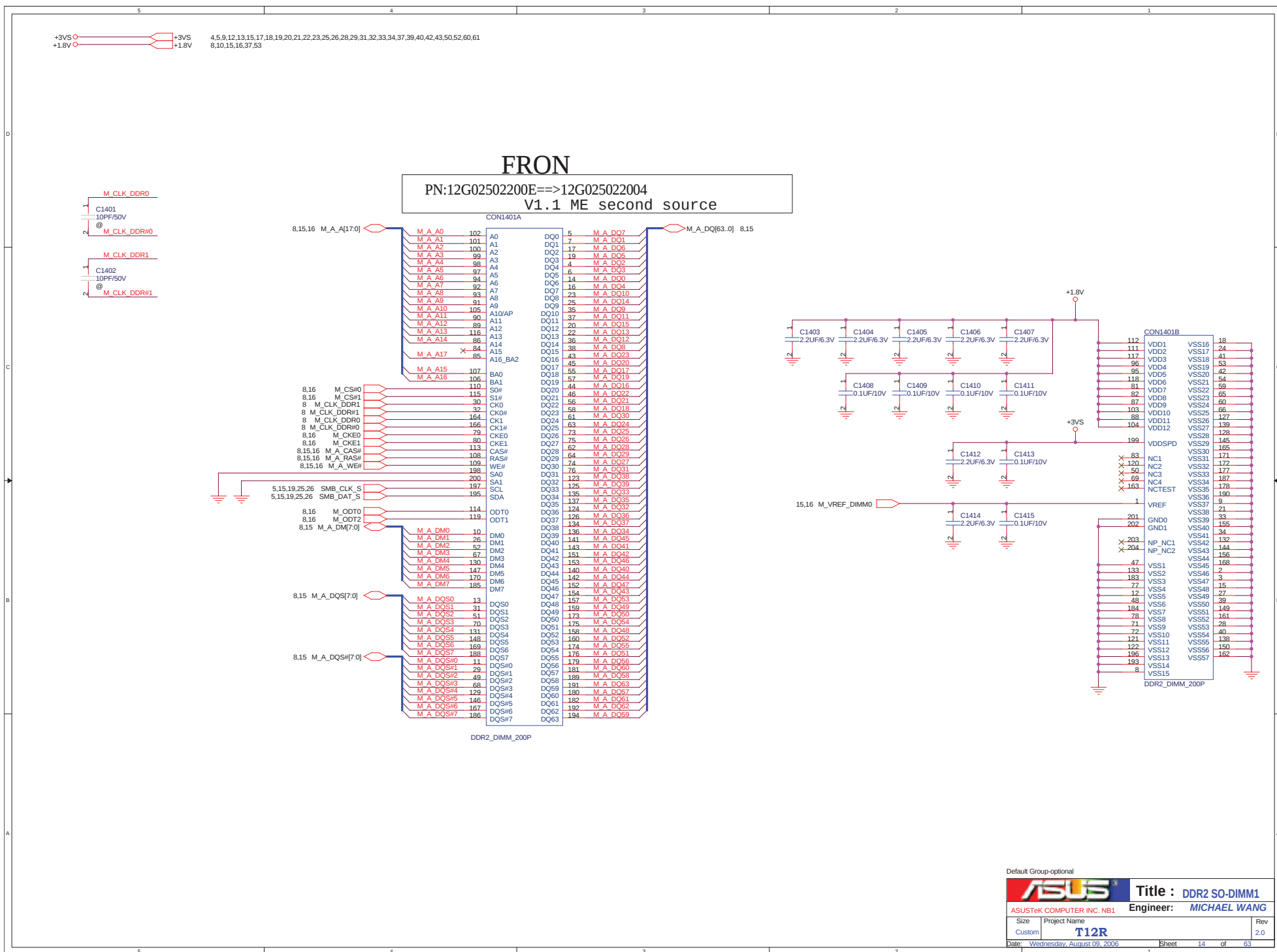
Default Group-optional

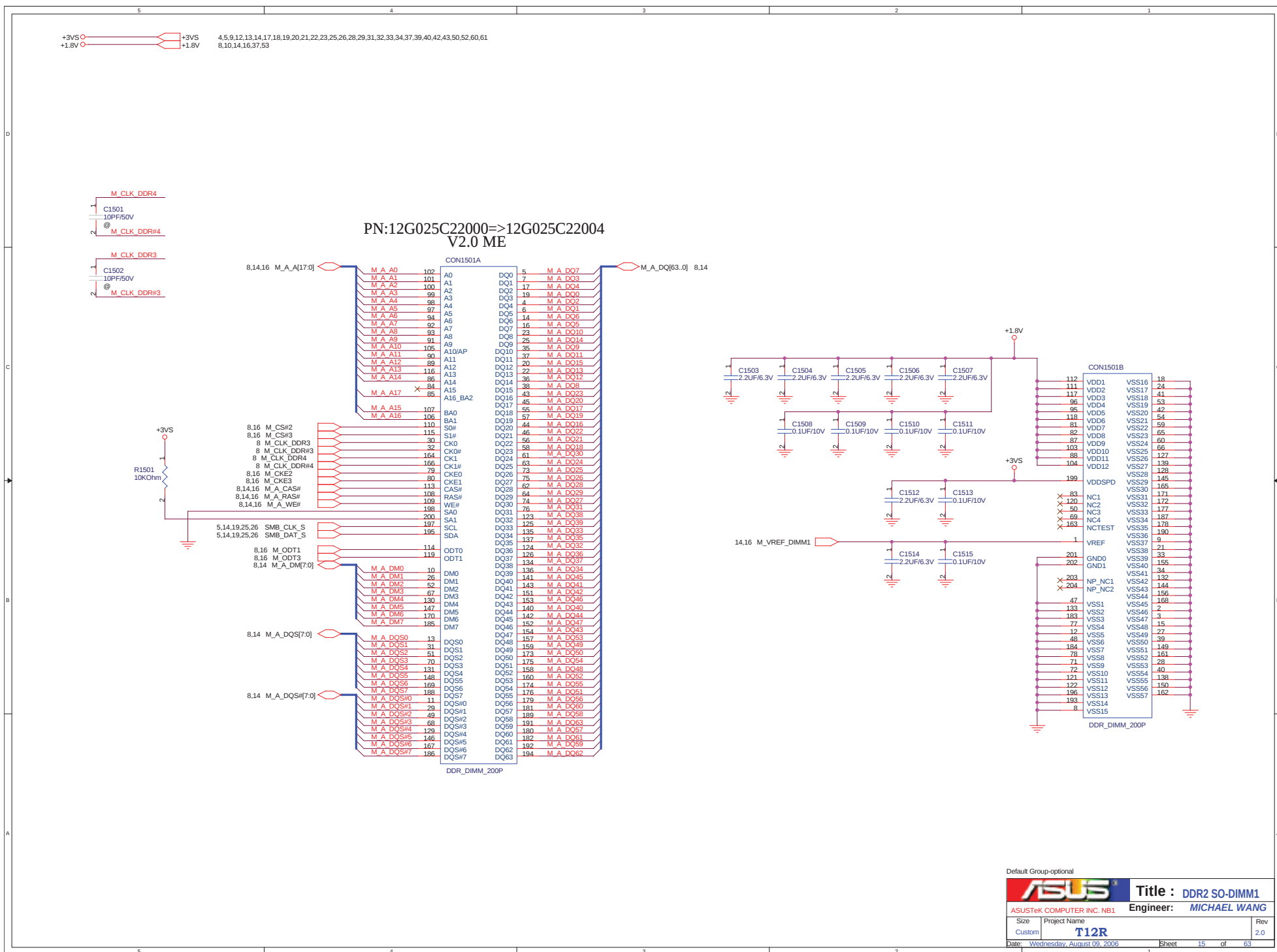
		Title : NB-945PM(DMI & CFG)	
ASUSTek COMPUTER INC. NB1		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	T12R		
Date: Wednesday, August 09, 2006		Sheet	7 of 63

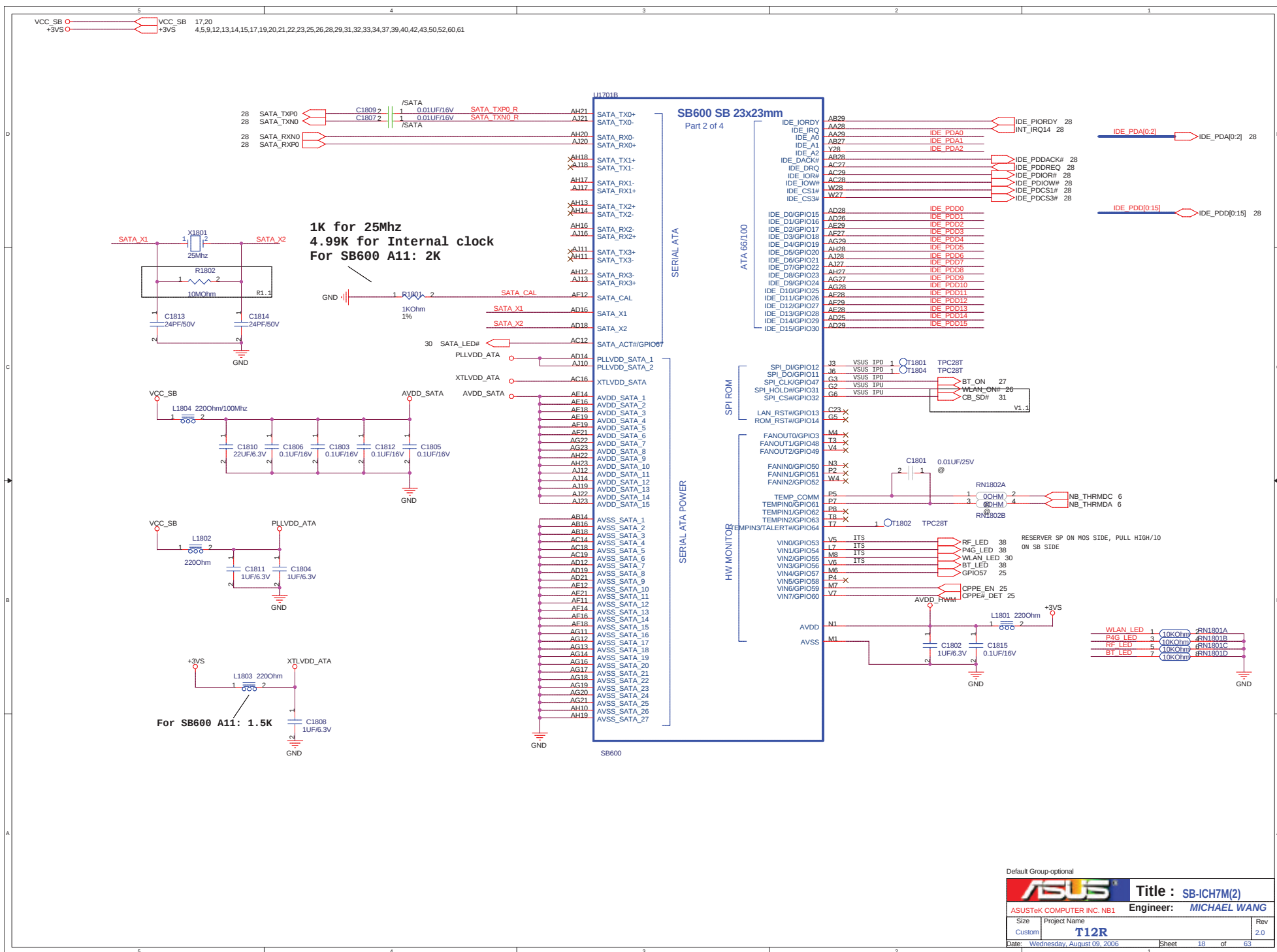


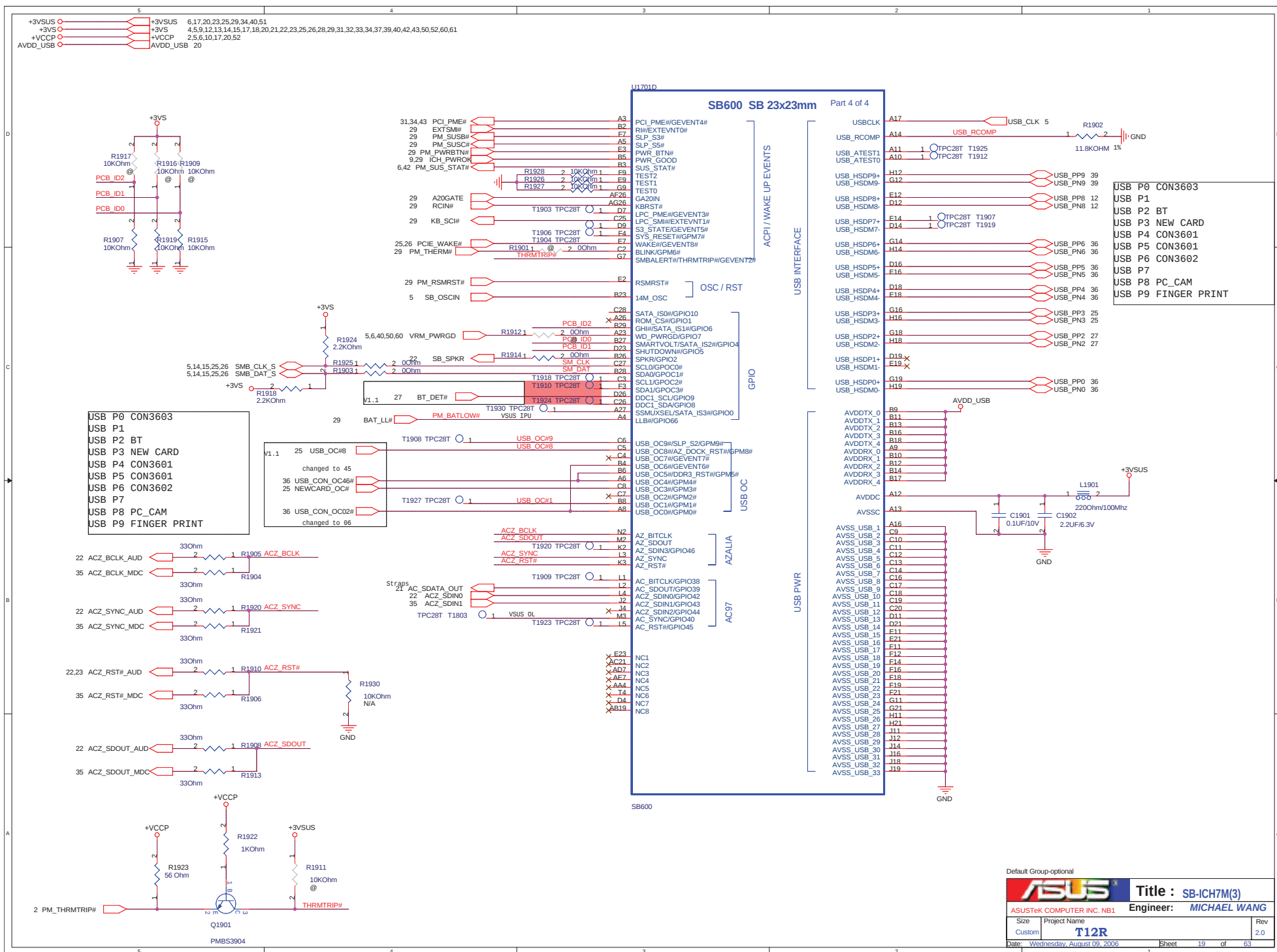






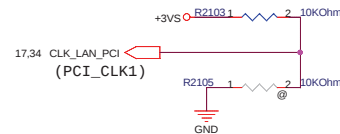
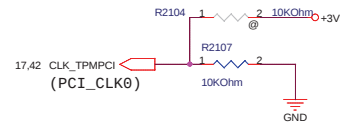
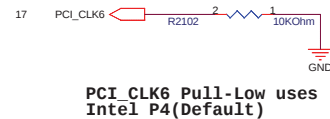
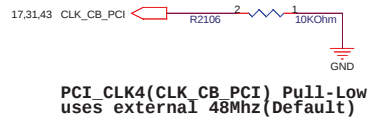
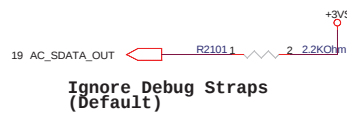
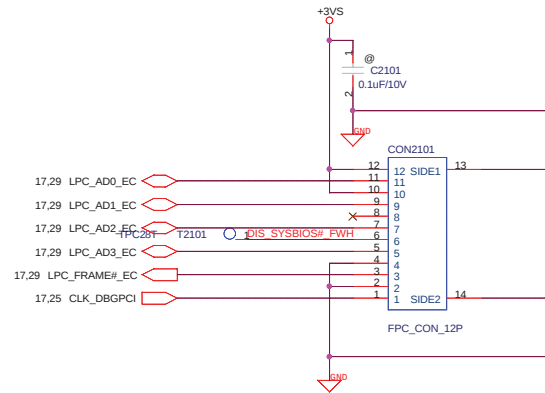








Amino Acid	Relative Abundance (%)
D27	~95
D28	~90
D29	~85
F26	~80
G23	~75
G24	~70
G25	~65
H27	~60
J23	~55
J26	~50
J28	~45
K27	~40
L22	~35
L23	~30
L24	~25
L27	~20
L28	~15
M21	~10
M24	~5
M27	~2
N27	~1
N28	~0.5
P22	~0.2
P23	~0.1
P24	~0.05
P25	~0.02
P26	~0.01

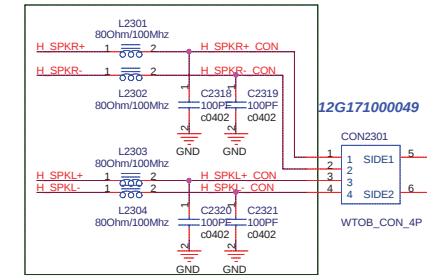
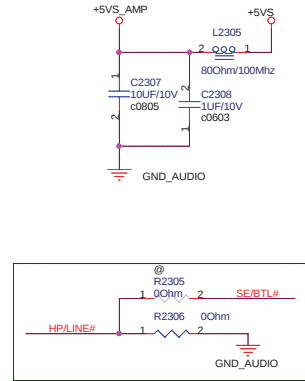
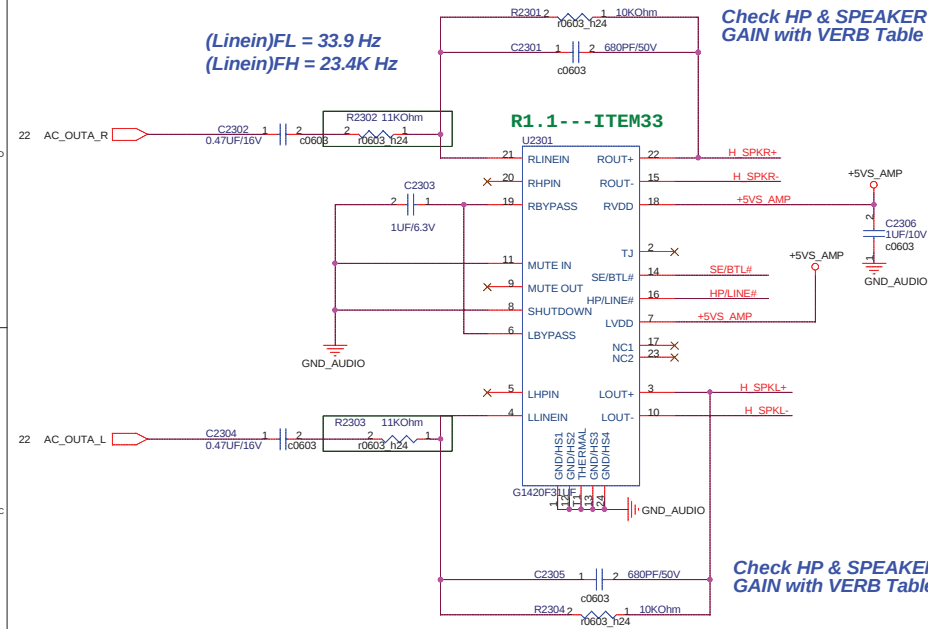


PCI_CLK0	PCI_CLK1	(ROM Type)	
H	H	PCI ROM	
H	L	SPI ROM	
L	H	LPC ROM	(Default)
L	L	FWH ROM	

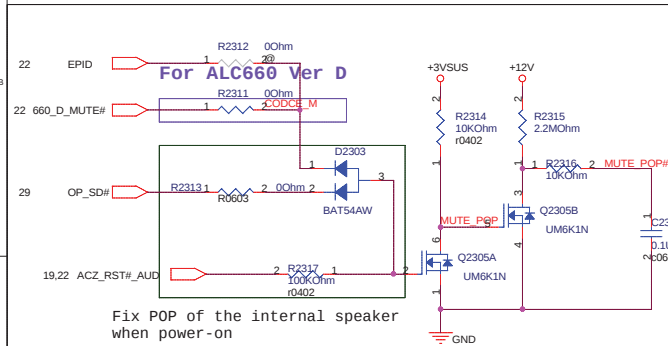
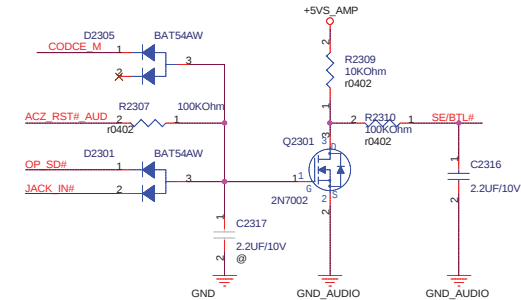
Default Group-optional

ASUS		Title : BLOCK DIAGRAM	
<OrigName>		Engineer:	
Size	Project Name	Rev	
Custom	T12R	2.0	
Date:	Wednesday, August 09, 2006	Sheet	21 of 63

(Linein)FL = 33.9 Hz
(Linein)FH = 23.4K Hz



Fix POP of the internal speaker when power-off

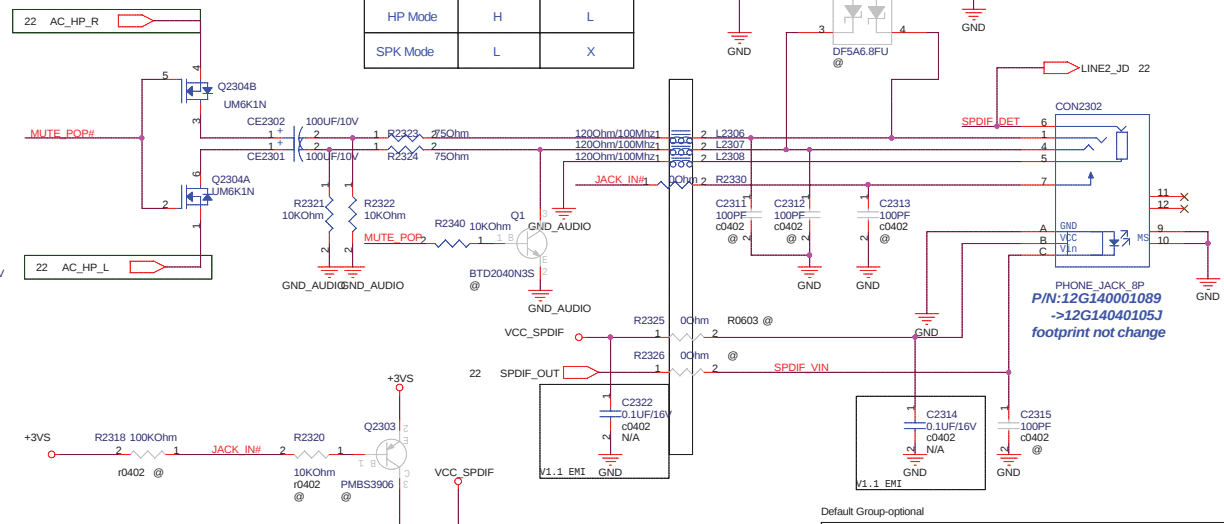


DIGITAL AREA

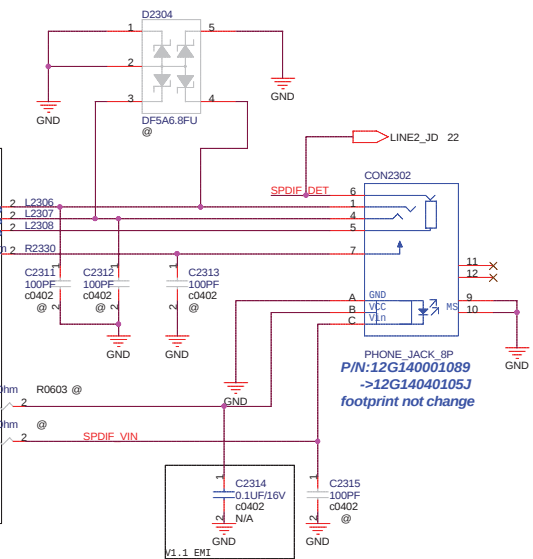
+3VS	4,5,9,12,13,14,15,17,18,19,20,21,22,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+5VS	4,13,20,22,28,29,30,37,38,50,61
+5V_AUDIO	+5V_AUDIO 22
+3VSUS	6,17,19,20,25,29,34,40,51
+12V	37,54,61

JACK_IN

	SE/BTL#	SPDIF_DET
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X



Headphone & SPDIF JACK



Default Group-optional

ASUSTek COMPUTER INC.

MICHAEL WANG/Eric Rd. Peitou, Taipei, Taiwan, ROC

Title

Audio AMP

Size

Document Number

Custom

T12R

Date:

Wednesday, August 09, 2006

Sheet

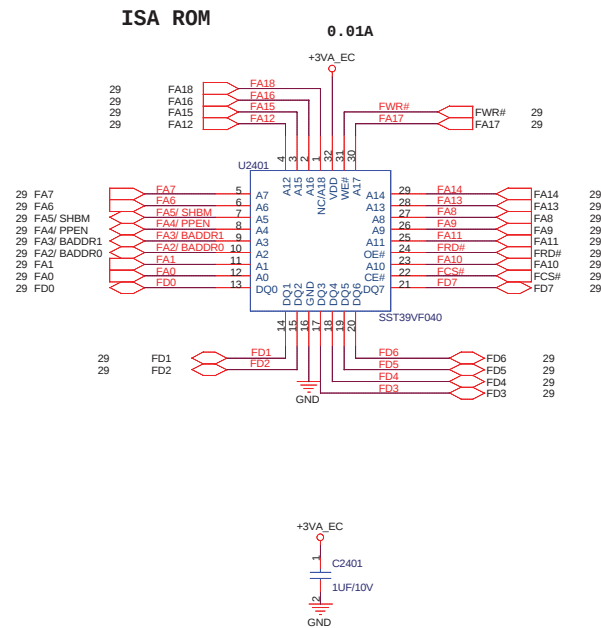
23

of

63

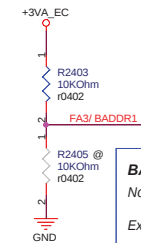
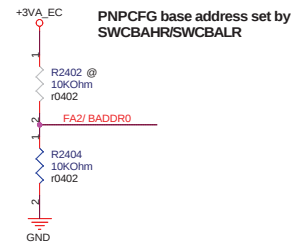
Rev

2.0



EC Hardware Strap

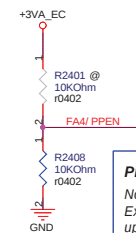
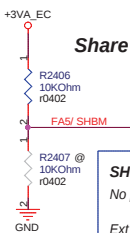
*Strap value sampled after
VSTBY power up reset*



Share Memory

SHBM

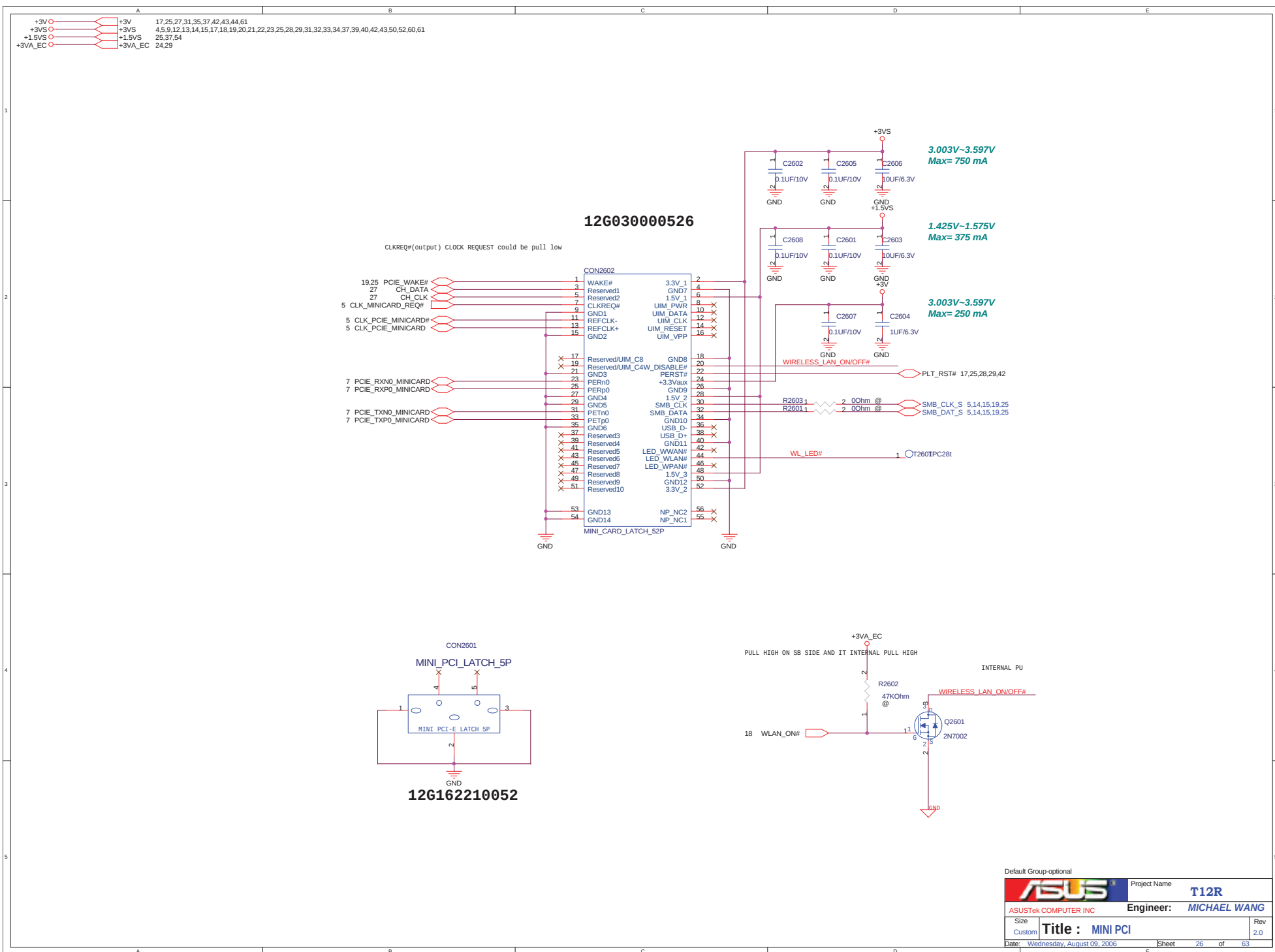
No pull up: Disable shared memory with host BIOS
Ext 10K up: Enable shared memory with host BIOS



PPEN

No pull up: Normal
Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.

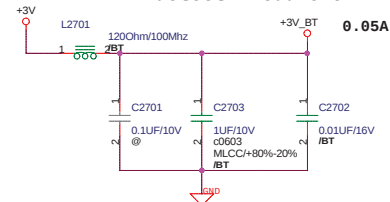
Default Group-optional		Title : ISA ROM	
ASUSTek COMPUTER INC		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	T12R	2.0	
Date: Wednesday, August 09, 2006	Sheet	24	of 63



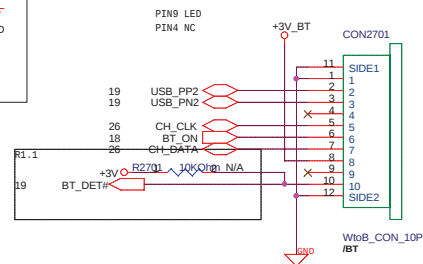
+3V  +3V 17,25,26,31,35,37,42,43,44,61

For Bluetooth

Bluetooth Module CN



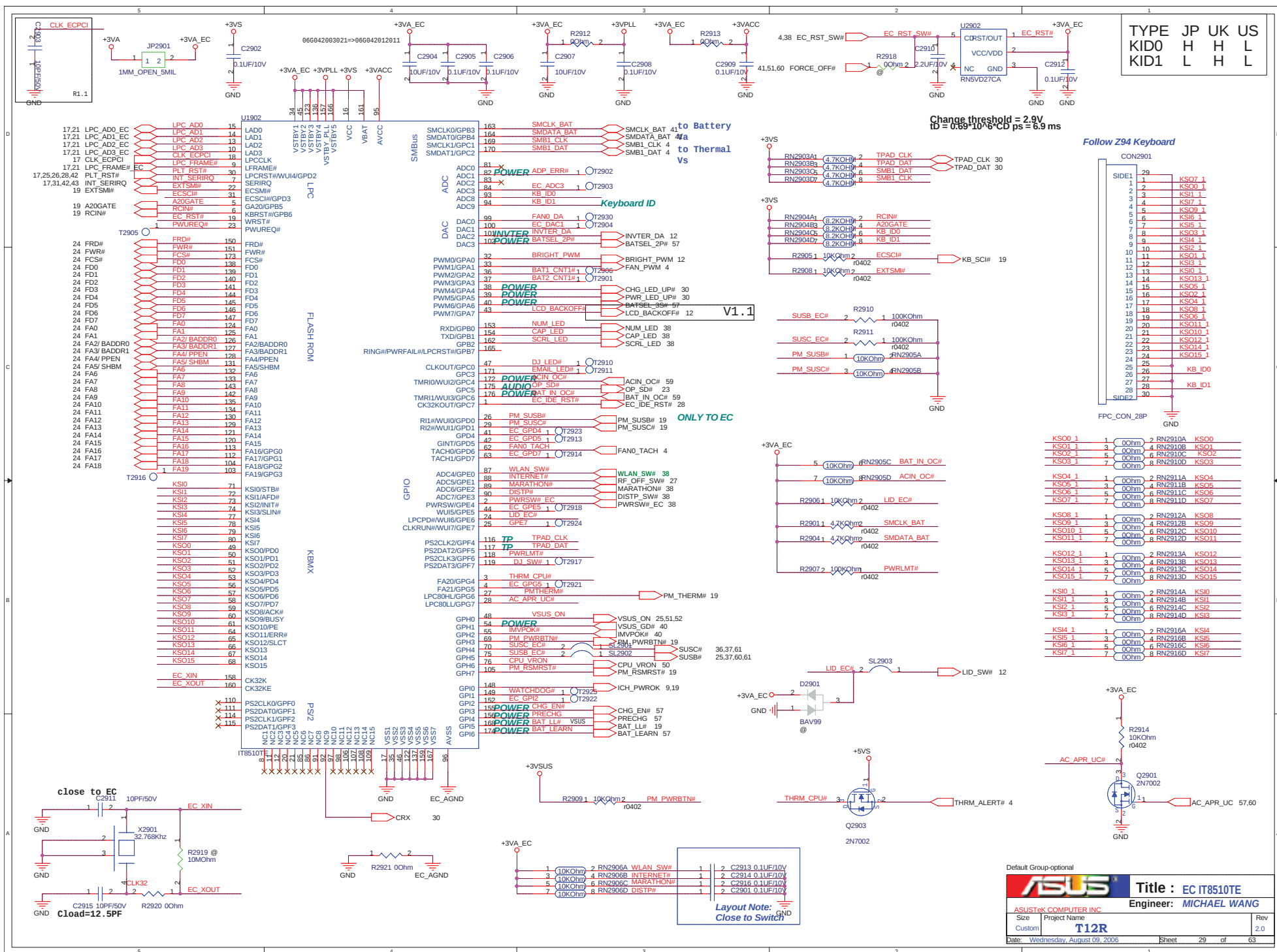
12G17101010L

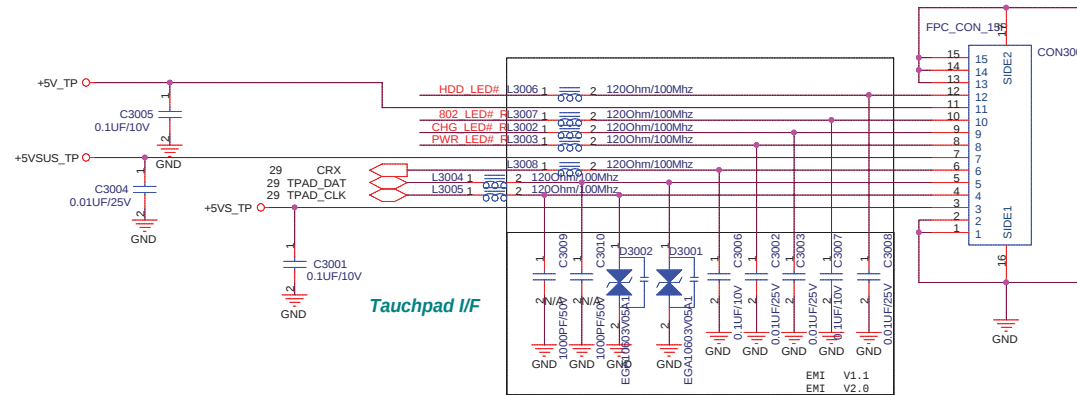
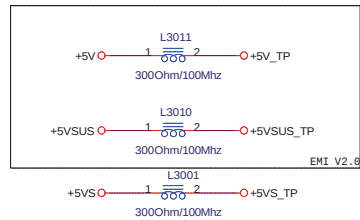


USB P0 CON3603
 USB P1
 USB P2 BT
 USB P3 NEW CARD
 USB P4 CON3601
 USB P5 CON3601
 USB P6 CON3602
 USB P7
 USB P8 PC_CAM
 USB P9 FINGER
 PRINT

Default Group-optional

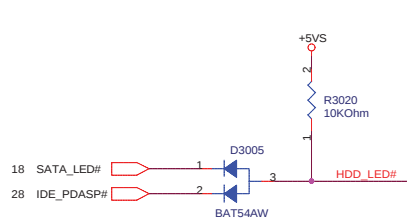
		Title : Blue Tooth	
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG	
Size Custom	Project Name T12R	Rev 2.0	
Date: Wednesday, August 09, 2006	Sheet 27	of 63	



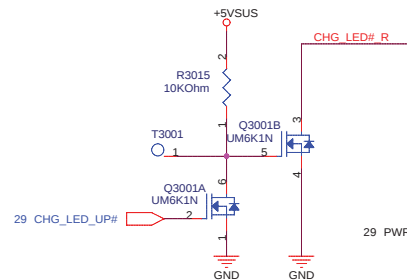


Touchpad

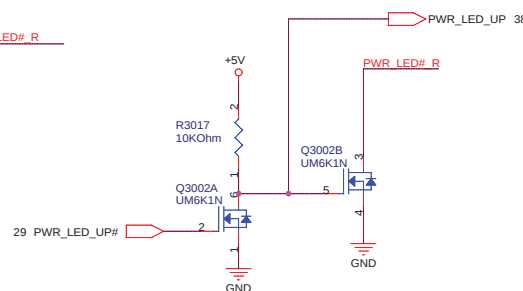
HDD LED



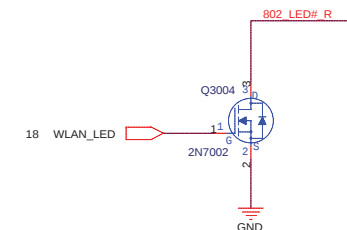
CHARGE LED



POWER LED

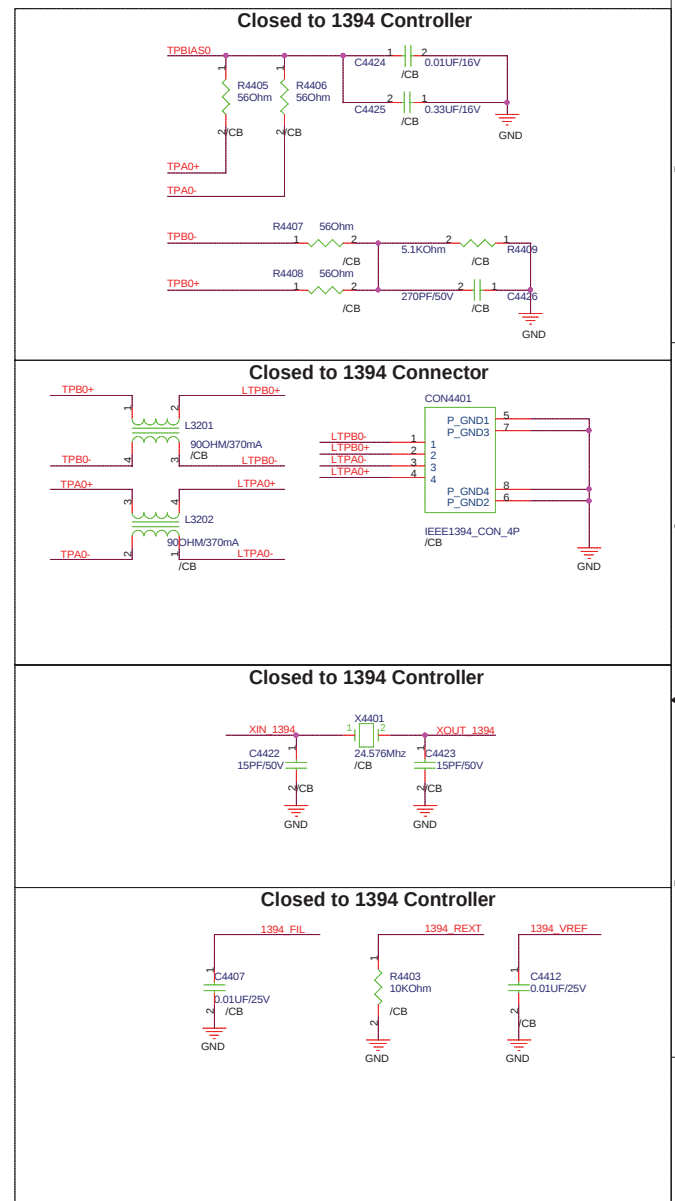
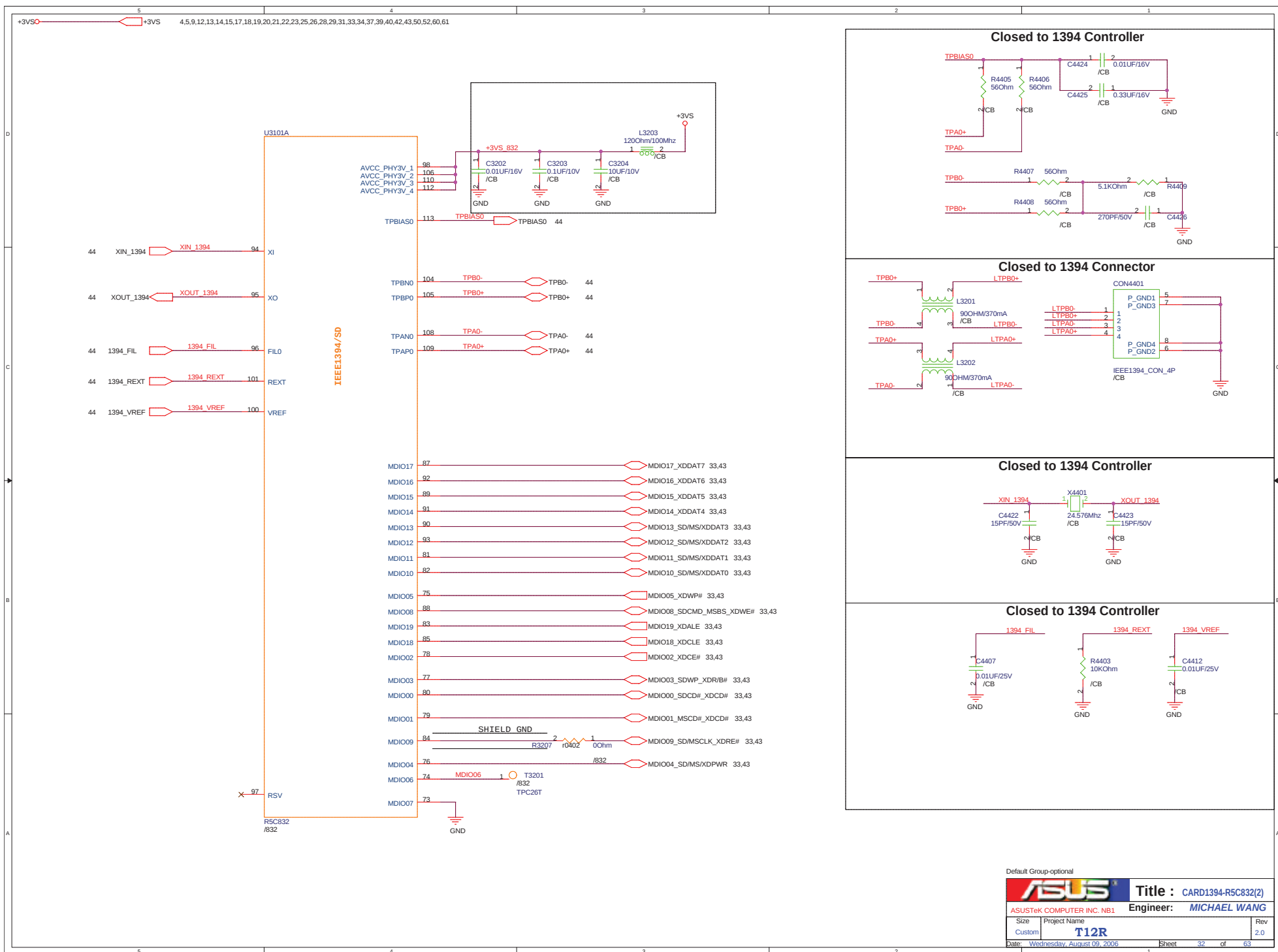


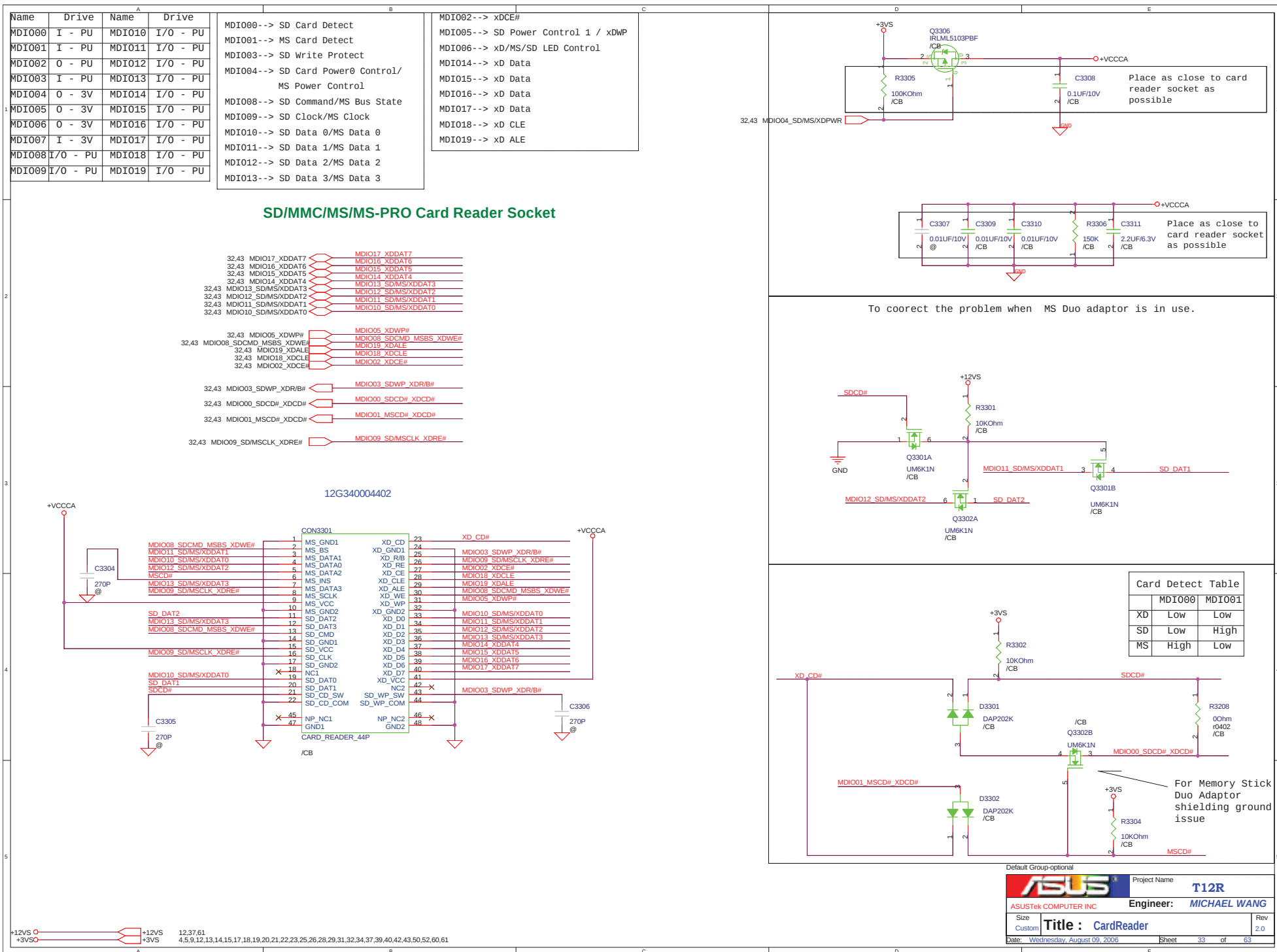
WLAN LED



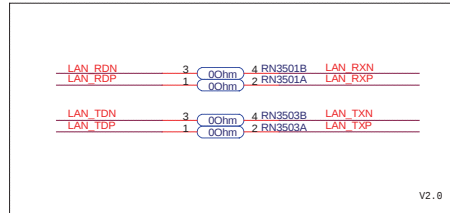
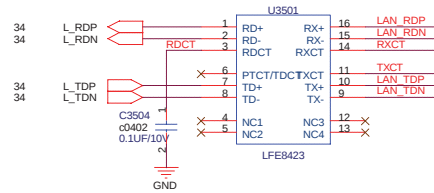
Default Group-optional

ASUS		Title : EC IT8510TE(2/2)	
ASUSTek COMPUTER INC.		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
A3	T12R	2.0	
Date: Wednesday, August 09, 2006	Sheet	30	of 63

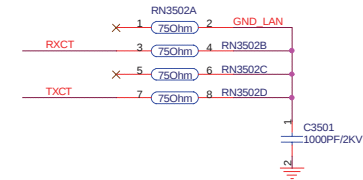
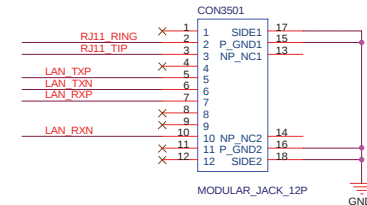




LAN PORT

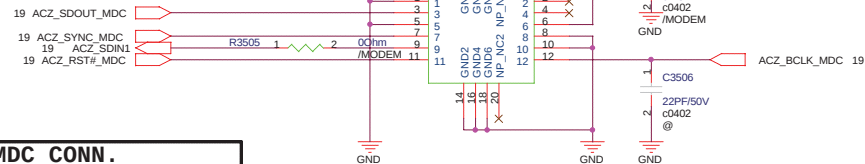
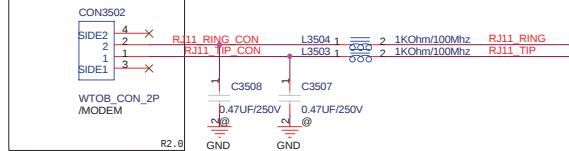


12G142111120



MDC CONNECTOR

12G17000002B=>12G17100002C



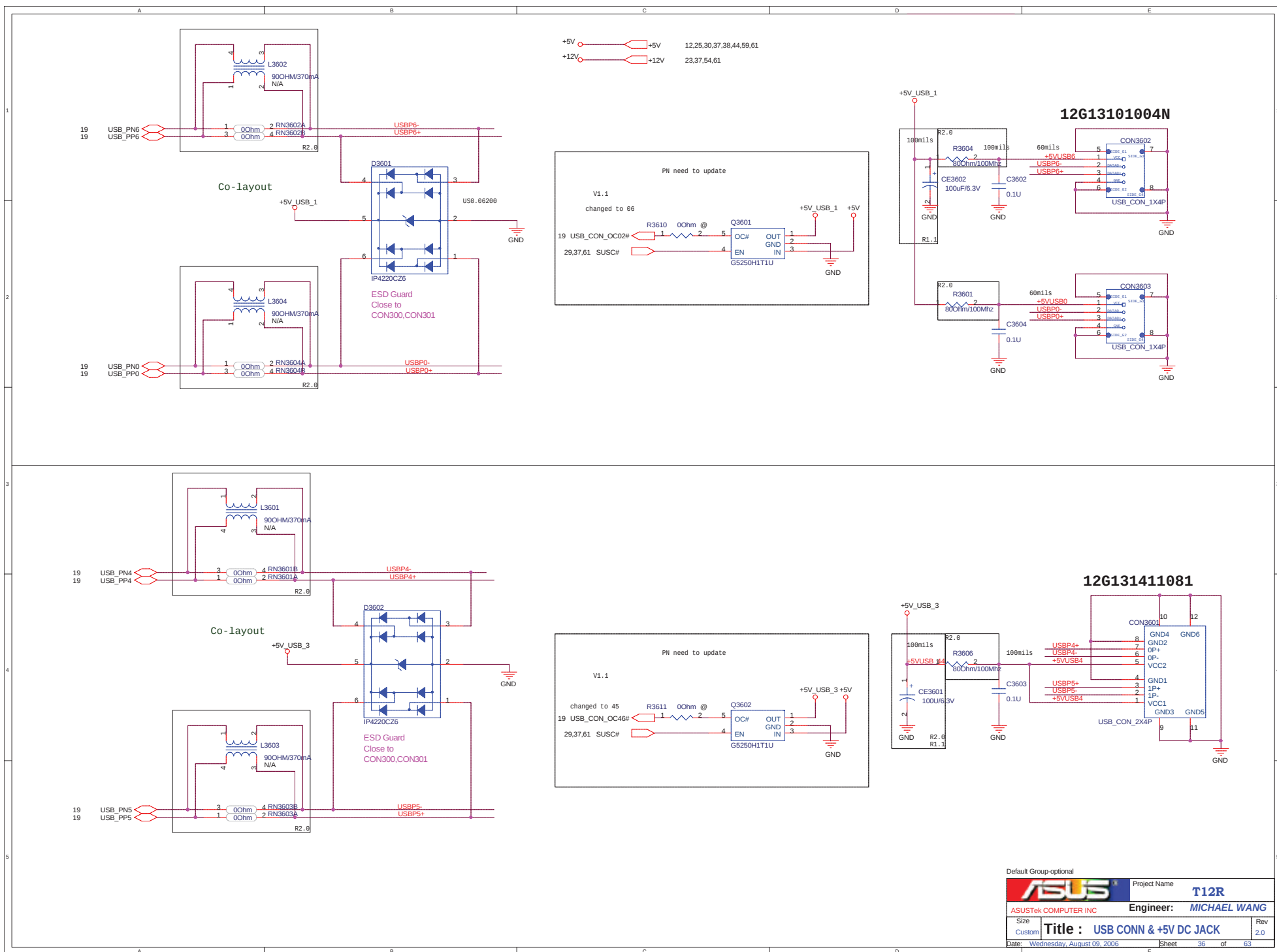
For MDC CONN.

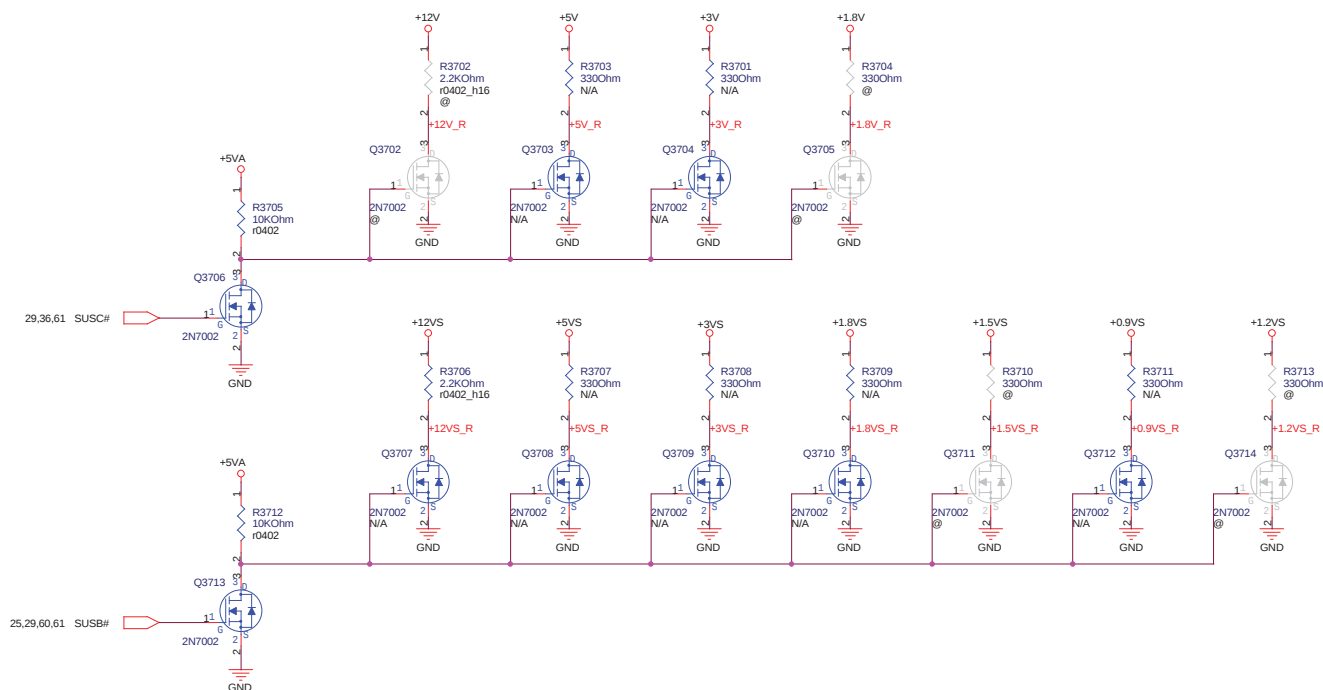


Must change to
13GN7510M270

Default Group-optional

ASUS		Title : RJ11/45 & MDC	
ASUSTeK COMPUTER INC.		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	T12R	2.0	
Date: Wednesday, August 09, 2006		Sheet	35 of 63



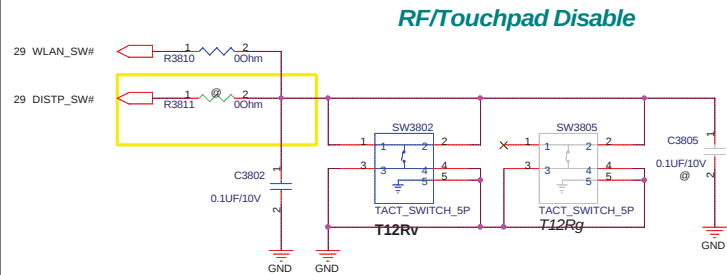


Check all power plan

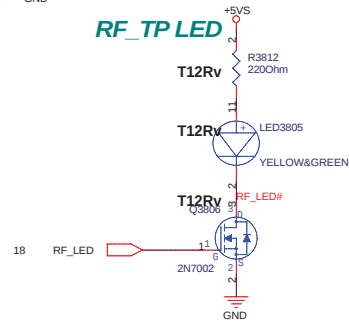
Default Group-optional				
		Title : Discharge Circuit		
ASUSTek COMPUTER INC		Engineer: MICHAEL WANG		
Size	Project Name			Rev
Custom	T12R			2.0
Date:	Wednesday, August 09, 2006		Sheet	37 of 63

Main Board SW & LED

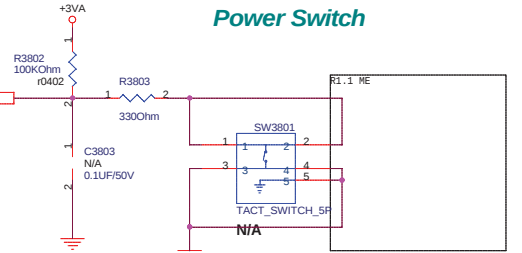
RF/Touchpad Disable



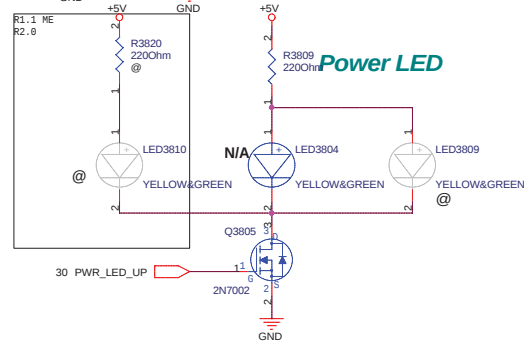
RF_TP LED



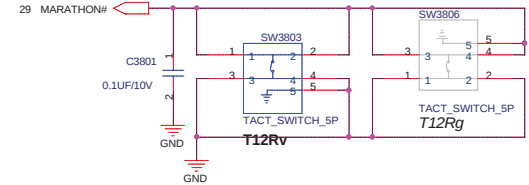
Power Switch



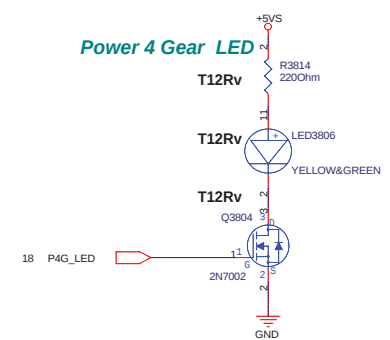
Power LED



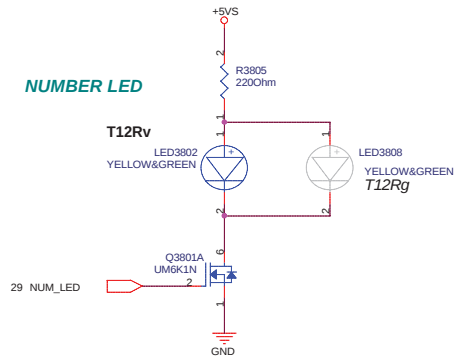
Power4 Gear



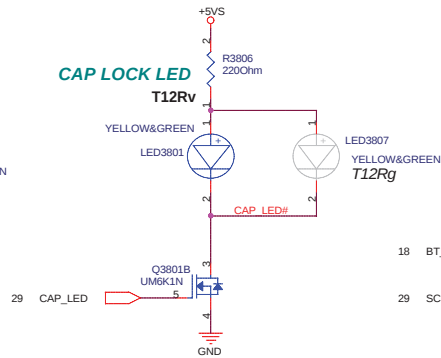
Power 4 Gear LED



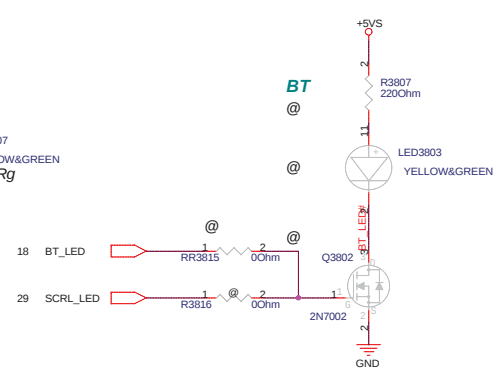
NUMBER LED



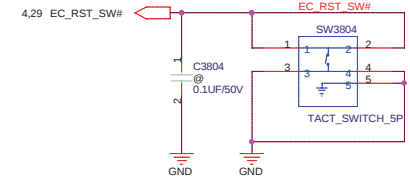
CAP LOCK LED



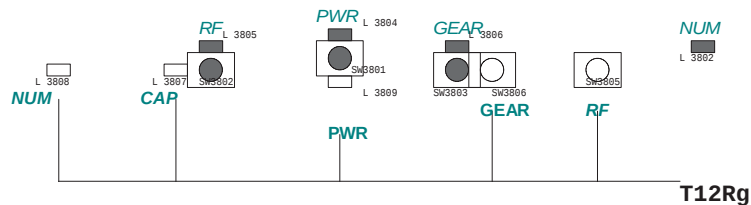
BT



Reset Switch



Pleacmant LED&SW



Default Group-optional

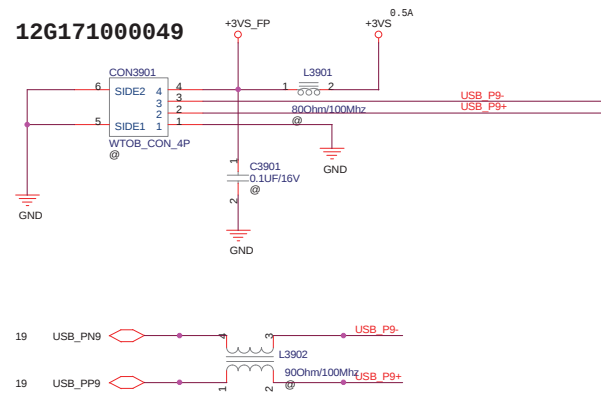
ASUS		Title : SW/LED	
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	T12R	2.0	
Date: Wednesday, August 09, 2006	Sheet	38	of 63

+3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT Reserved

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT

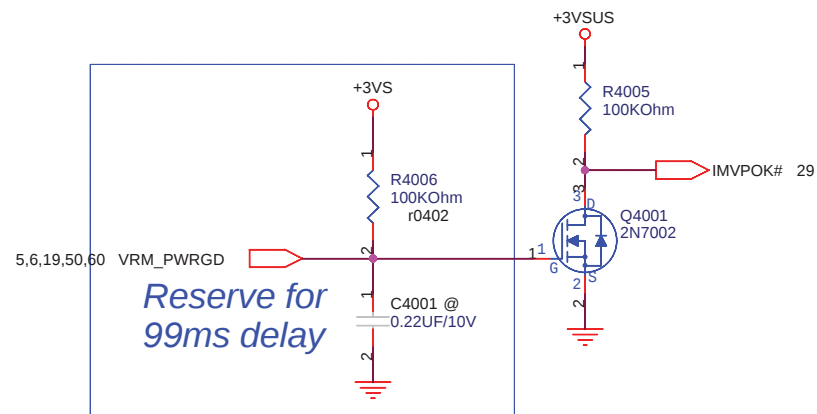
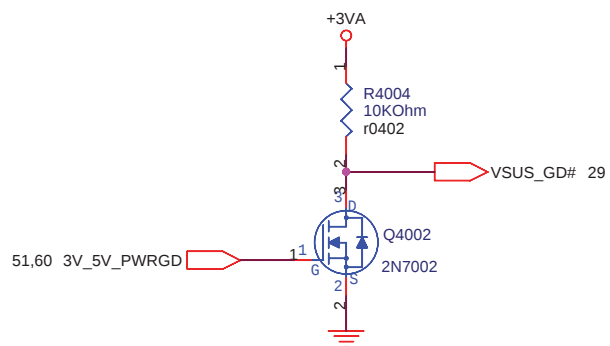
12G171000049



Default Group-optional

ASUS		Title :FINGER PRINT	
ASUSTek COMPUTER INC		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	T12R	2.0	
Date: Wednesday, August 09, 2006	Sheet	39	of 63

+3VA	12,29,38,54,57,59,63
+3VS	4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,42,43,50,52,60,61
+3VSUS	6,17,19,20,23,25,29,34,51



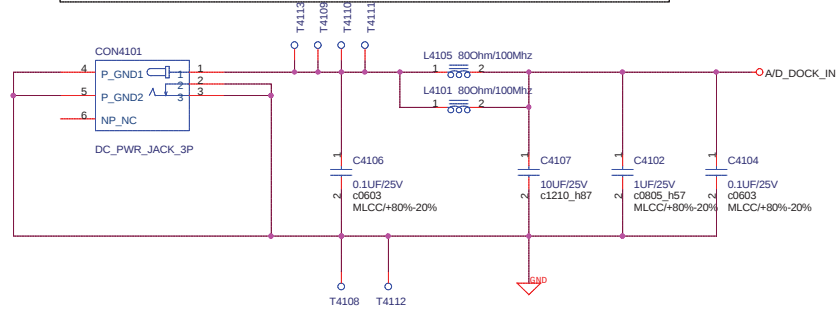
Default Group-optional

ASUS		Title : POWER-ON SEQ.	
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG	
Size A4	Project Name T12R	Rev 2.0	
Date: Wednesday, August 09, 2006		Sheet	40 of 63

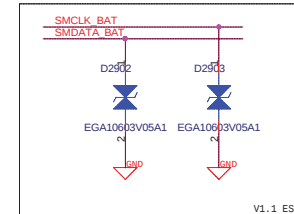
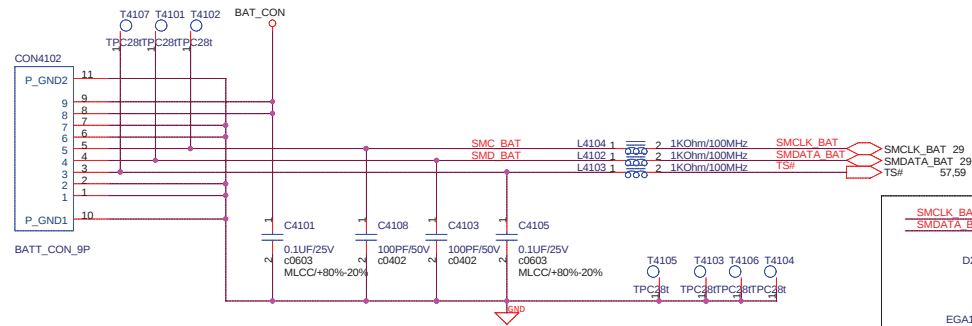
A/D_DOCK_IN 57.59
 BAT_CON 57
 AC_BAT_SYS 12.50,51.52,53,54,57,60

12G145002034=>12G14530103E

V2.8 ME

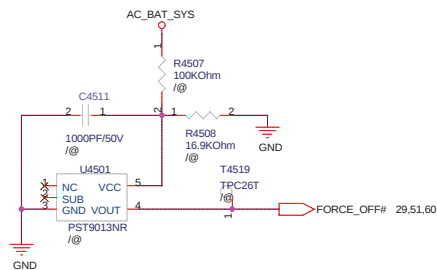


12G20001090G



V1.1 ESD

**Without Battery & Pull out Adapter
 RESERVED**

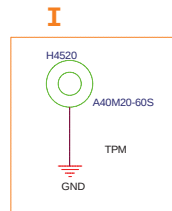
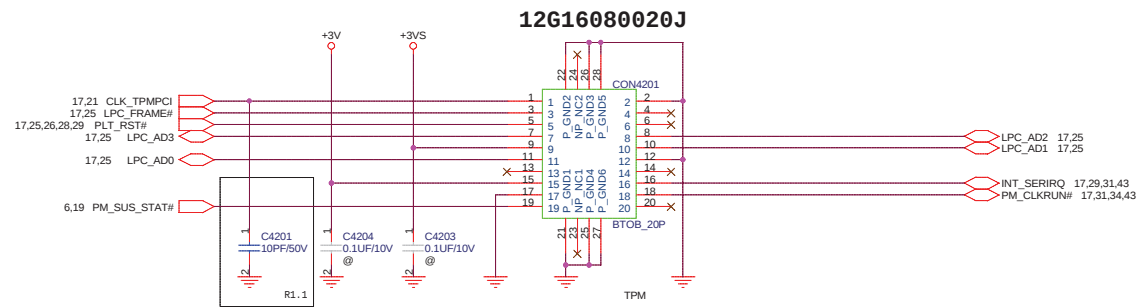


Default Group-optional		Project Name	T12R
ASUSTek COMPUTER INC		Engineer:	MICHAEL WANG
Size	Custom	Title : DC IN	Rev 2.0
Date: Wednesday, August 09, 2006	Sheet 41	of 63	

+3VS  +3VS
 +3V  +3V

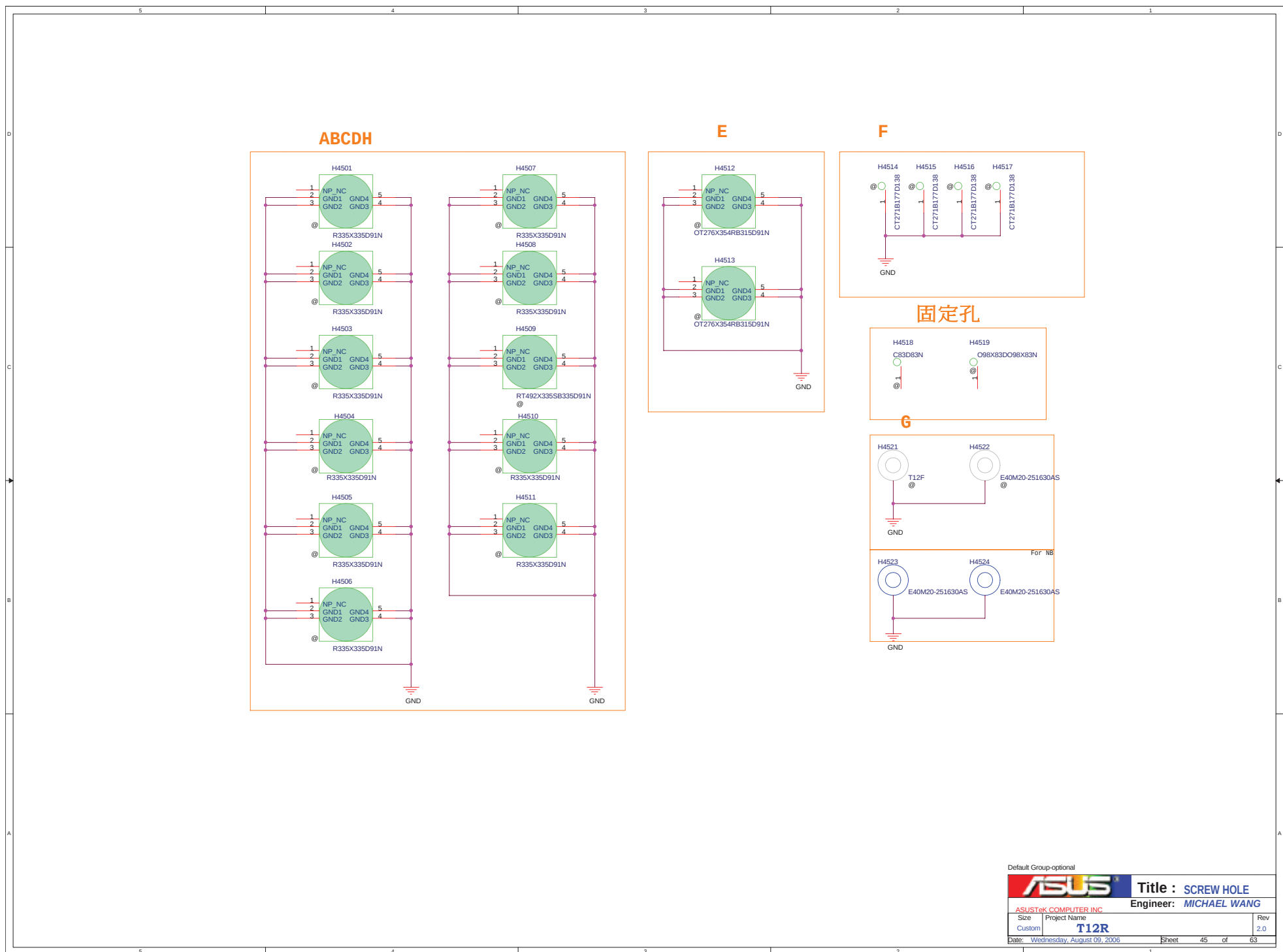
4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61
 17,25,26,27,31,35,37,43,44,61

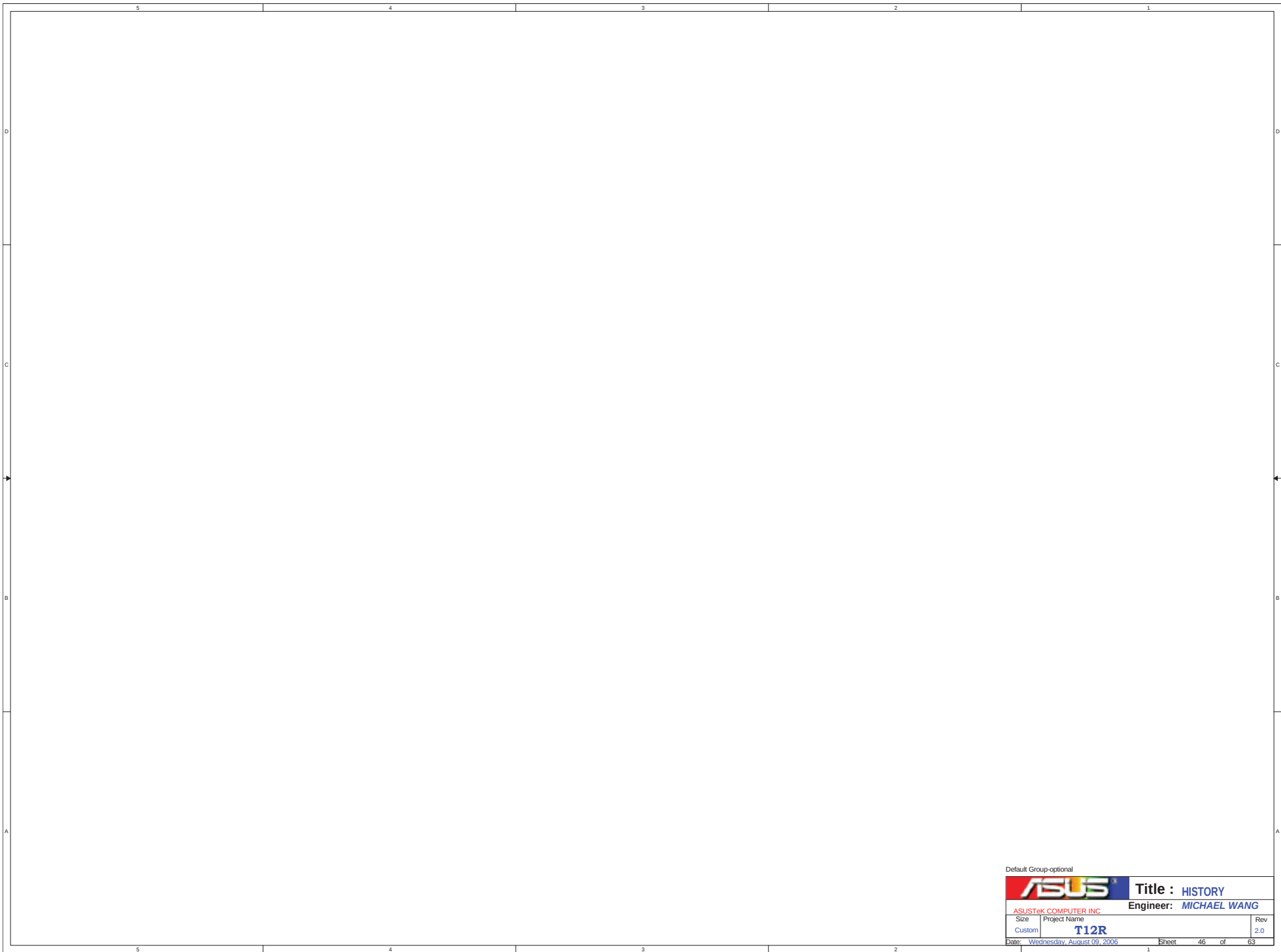
TPM Module CON RESERVED

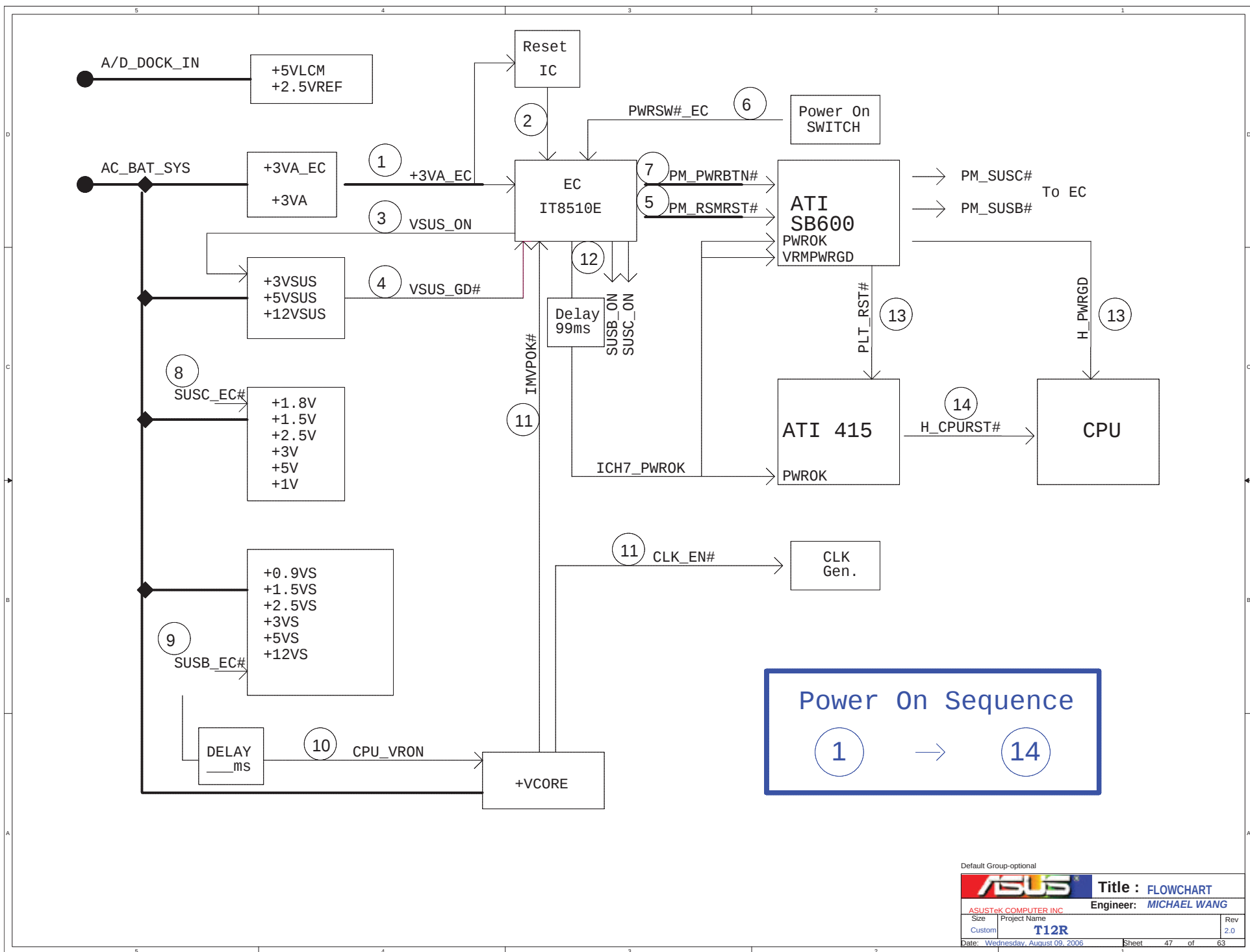


For TPM CONN.

Default Group-optional		Project Name		T12R	
ASUS		ASUSTek COMPUTER INC		Engineer: MICHAEL WANG	
Size	Custom	Title : TPM 1.2			Rev 2.0
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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM		48	GPH0	VSUS_ON	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/		55	GPH2	IMVPOK#	I
37	PWM3/GPA3	/		69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH7_PWROK	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCH_DOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/O	155	GPI3	CHG_EN#	O
164	SMDAT0/GPB4	SMDATA_BAT	I/O	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RC_IN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	8	GPI0	WLAN_ON#	O
169	SMCLK1/GPC1	SMB1_CLK	I/O	11	GPI1	BT_ON#	O
170	SMDAT1/GPC2	SMB1_DAT	I/O	12	GPI2	RF_OFF_SW#	I
171	GPC3	/		20	GPI3	RF_LED	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I	92	CRX	CRX	I/O
175	GPC5	OP_SD#	O				
176	TMR11/WUI3/GPC6	BAT_INV_OC#	O				
1	CK32KOUT/GPC7	/	I				
26	RI1#WUI0/GPD0	PM_SUSB#	I				
29	RI2#WUI1/GPD1	PM_SUSC#	I				
30	LPCRST#WUI4/GPD2	PLT_RST#	I				
31	ECSCI#GPD3	EXT_SCI#	O				
41	GPD4	/	I				
42	GINT/GPD5	/	I				
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#	I				
88	ADC5/GPE1	/	I				
89	ADC6/GPE2	MARATHON#	I				
90	ADC7/GPE3	DISTP_SW#	I				
2	PWRSW/GPE4	PWRSW#_EC	I				
44	WUI5/GPE5	/	I				
24	LPCPD#WUI6/GPE6	LID_EC#	I				
25	CLKRUN#WUI7/GPE7	/	O				
110	PS2CLK0/GPF0	/					
111	PS2DAT0/GPF1	/					
114	PS2CLK1/GPF2	/	I/O				
115	PS2DAT1/GPF3	/	I/O				
116	PS2CLK2/GPF4	TP_CLK					
117	PS2DAT2/GPF5	TP_DAT					
118	PS2CLK3/GPF6	PWRLMT#					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSM#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCH#	STP_PCH#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIe Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

Default Group-optional

		Title : GPIO Setting	
ASUSTek COMPUTER INC.		Engineer: MICHAEL WANG	
Size	Project Name		Rev
Custom	T12R		2.0
Date: Wednesday, August 09, 2006		Sheet	48 of 63

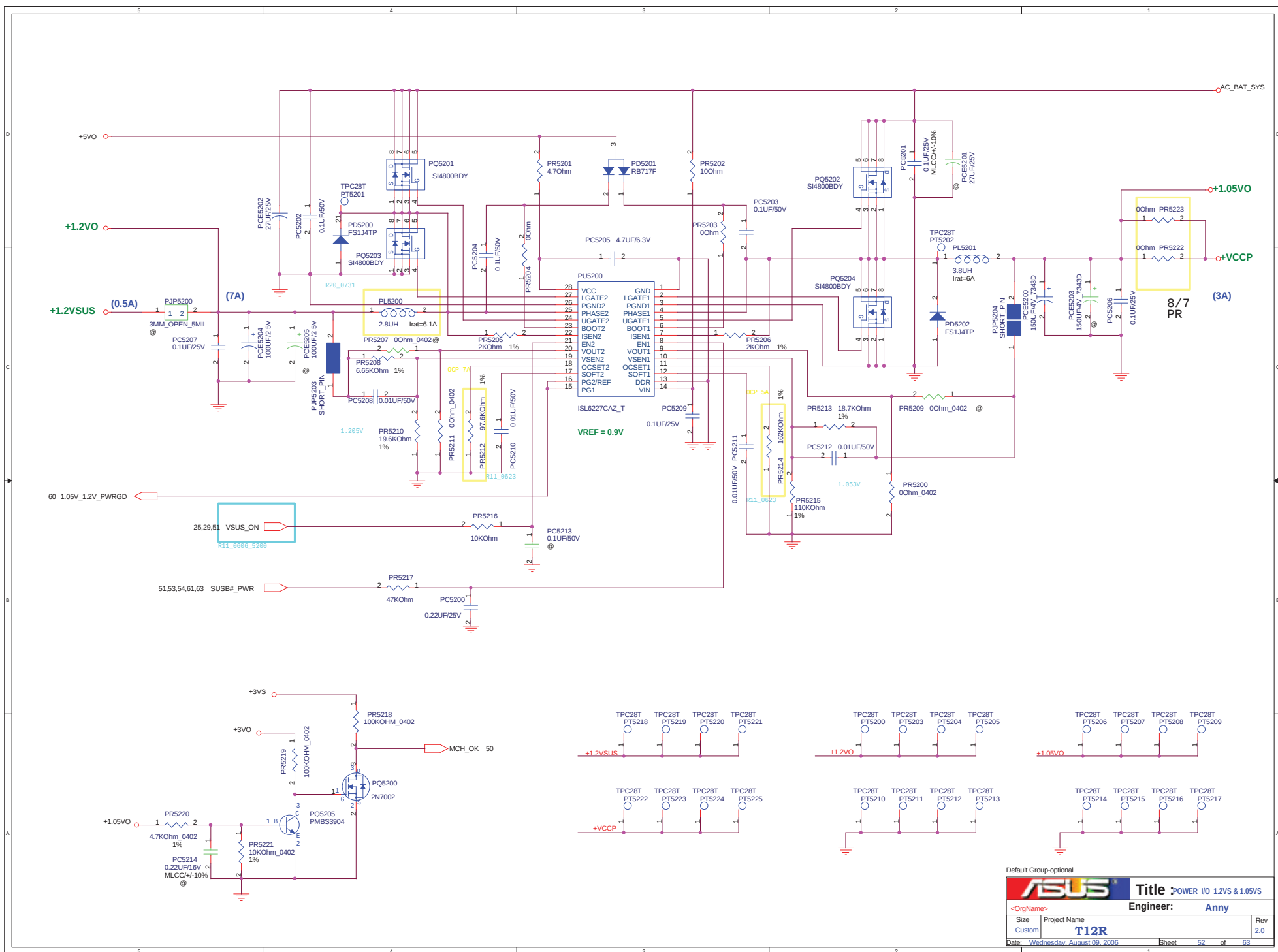
T12R V1.1 History

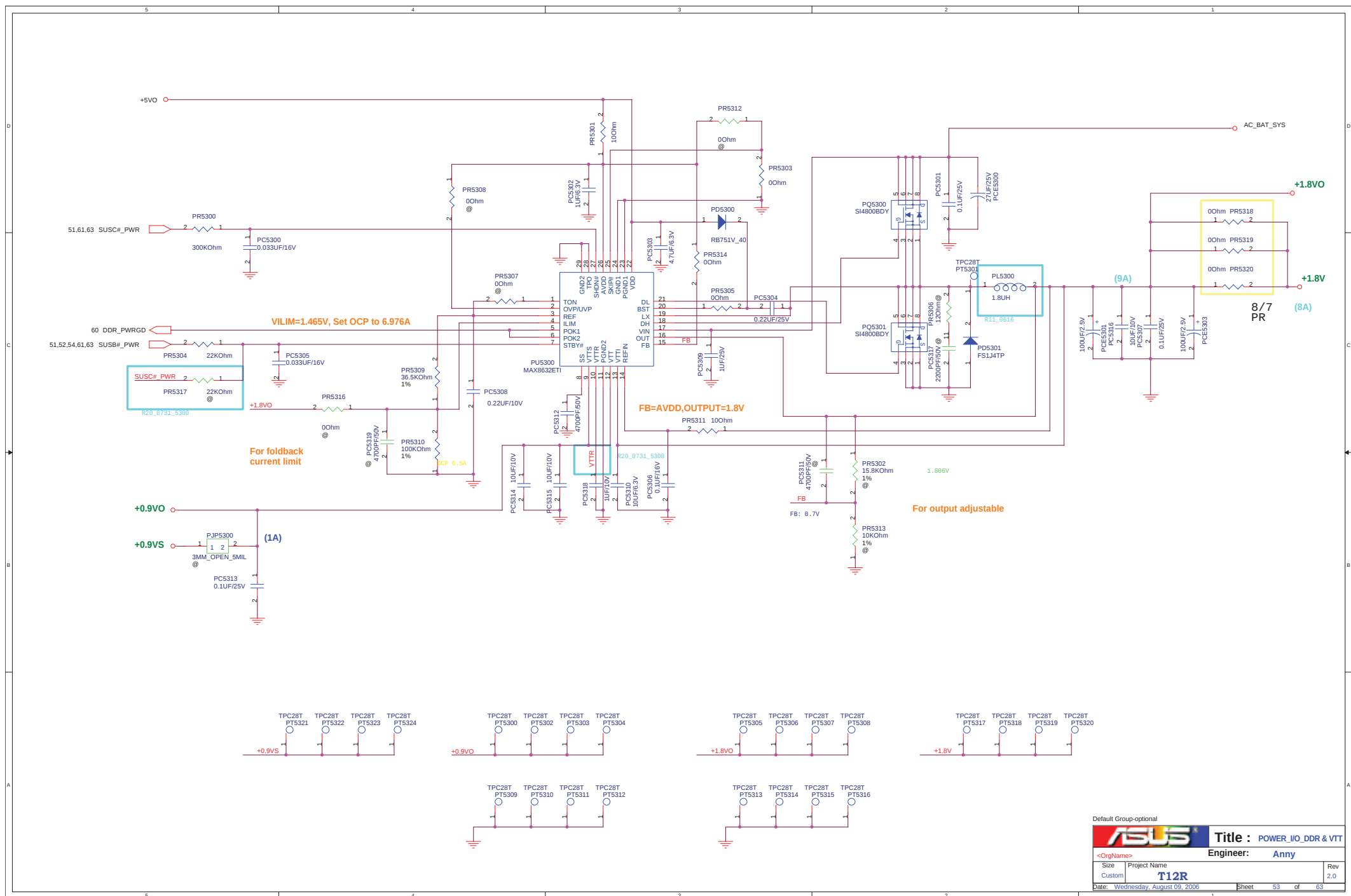
1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
 3. Page 18, added R1802
 4. Page 43&12, D4301 and L1201改footprint
 5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
 6. Page 17, Mount R1708, U1703 option changed reset path
 7. Page 43, Mount R4302 for R5C841 internal LDO input
 8. Page 9, un-mount L906 C914 , these for 610 only
 - 9.All PCI clock added 6.8 pF to decrease skew.
 - 10.PWM connected to EC and back-light connected to NB
 - 11.D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
 - 12.page 19, added BT_DET# to detect BT.
 - 13.Page 19, adjust USB OC ping to correspond USB port
 - 14.Page 25, modification NEW CARD debug circuit to correspond new debug card
 - 15.page 28, we used correctly capacity for customer request.
 - 16.page 36, we used LDO with over current protect IC
 - 17.page 41, DC in connector add 2nd source.
- ME modify
- 1.ODD往板外移0.4mm
 - 2
 - 3.BATT 往板內移0.23mm
 - 4.增加螺絲鎖付記號
 - 6.DDR2 added 2nd source
P/N :12G025022004
DDR2 DIMM 200P,1.8V,H:4mm,STD
FOXCONN/AS0A426-N4SN-1
 - 7.add led 1 pcs LED3810 and del. SW3807(option)
 - 8.連版圖修改

T12R V2.0 Modify History

1. Page 6, R609 replacement 220K by 10K
2. Page 12, RN1203 replacement C.M chock by 00hm for EMI.
3. For DDRII connector(H=4mm) replacement 12G025022004 by original.
4. For DDRII connector(H=9mm) replacement 12G025C22004 by original.
5. For DC IN jack replacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 10U with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006-3010
- 10 Page 35, for EMI requestion, we added 00hm before LAN jack for option CM chock.

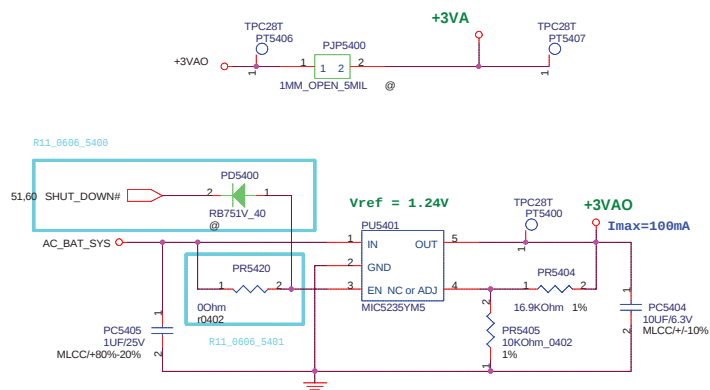
Default Group-optional		ASUS		Title : HISTORY	
<OrgName>		Engineer:			
Size	Project Name			Rev	
Custom	T12R			2.0	
Date: Wednesday, August 09, 2006		Sheet 49 of 63			



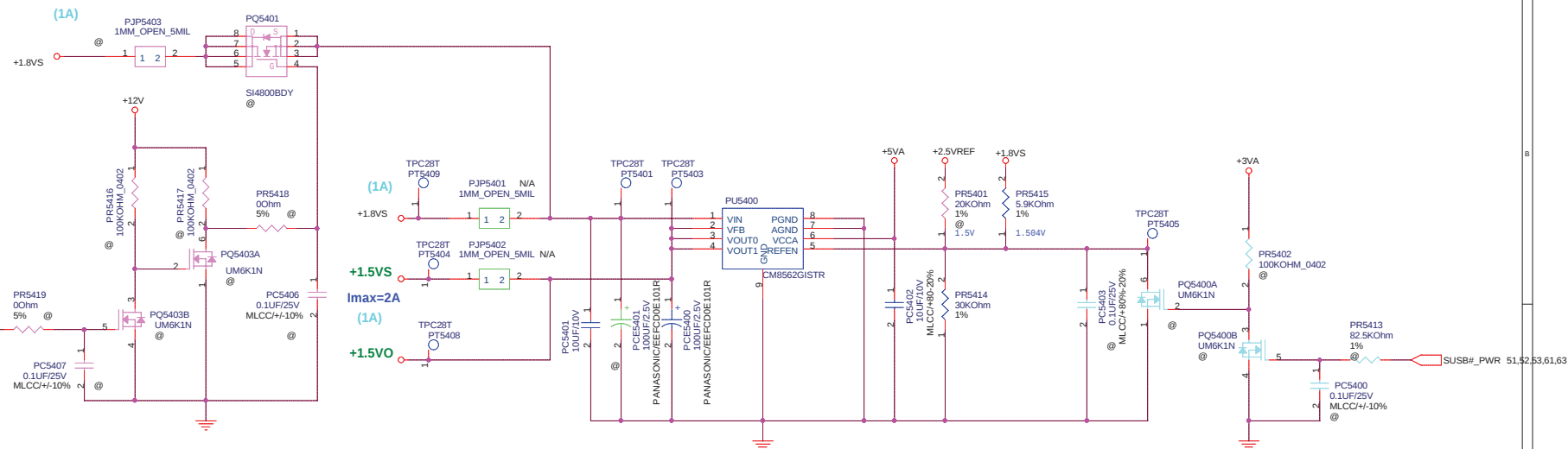


Default Group-optional		Title : POWER_I/O_DDR & VTT	
ASUS		Engineer: Anny	
Size	Project Name	Rev	
Custom	T12R	2.0	
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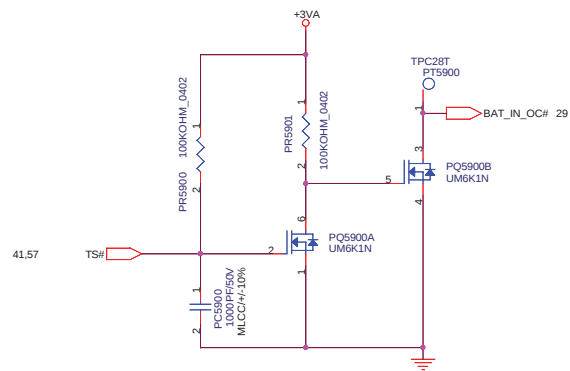
+3VA0



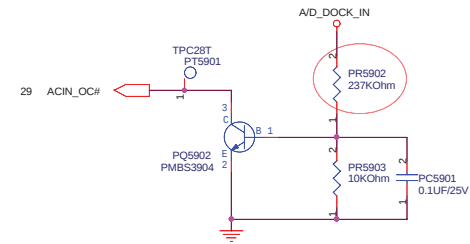
+2.5VS



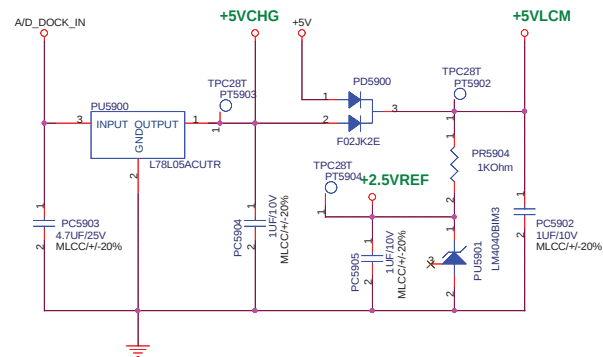
BATTERY IN DETECT



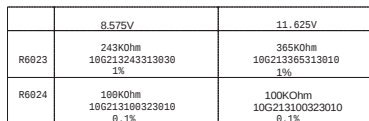
ADAPTER IN DETECT



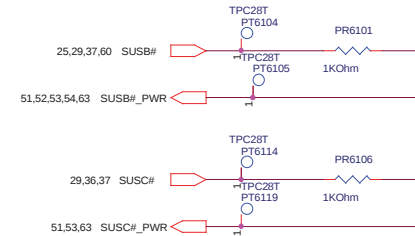
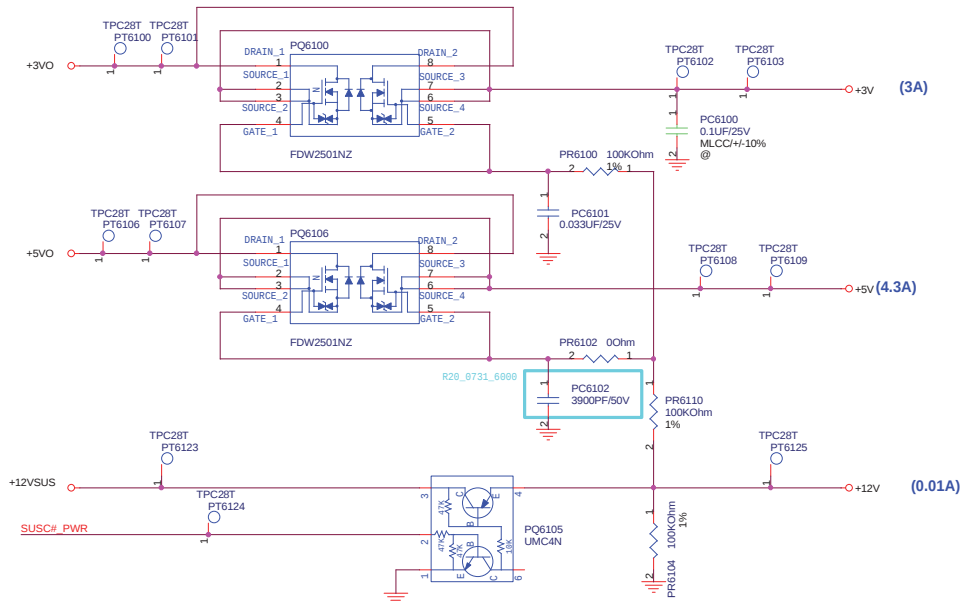
+5VLCM, +5VCHG & +2.5VREF



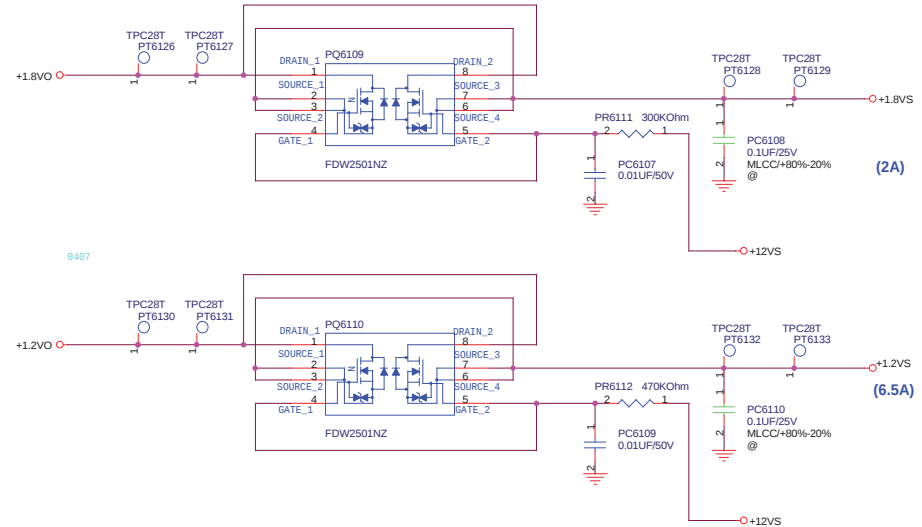
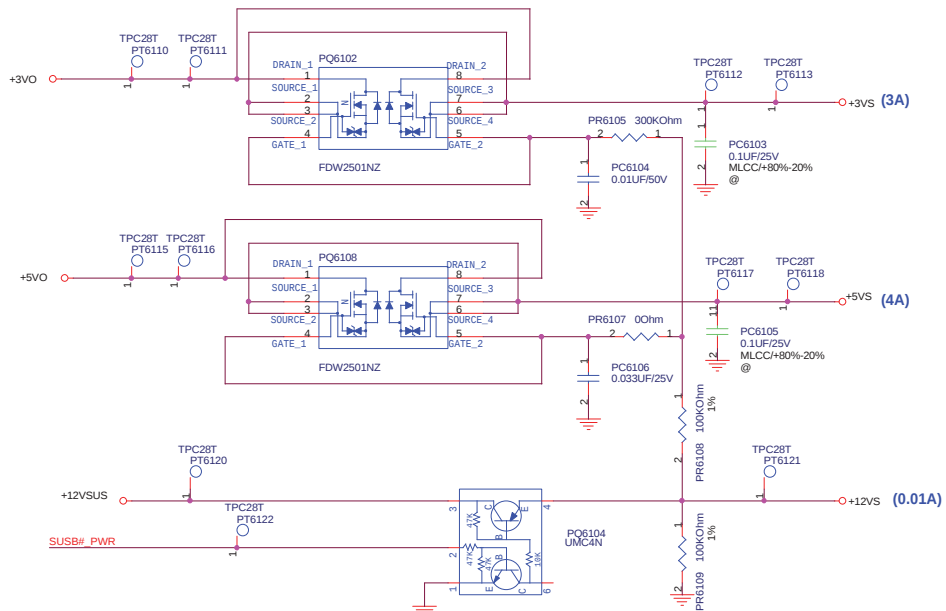
Default Group-optional		
ASUS		
Title : POWER_DETECT		
Engineer: Anny		
Size	Project Name	Rev
Custom	T12R	2.0
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SUSC#_PWR POWER



SUSB#_PWR POWER

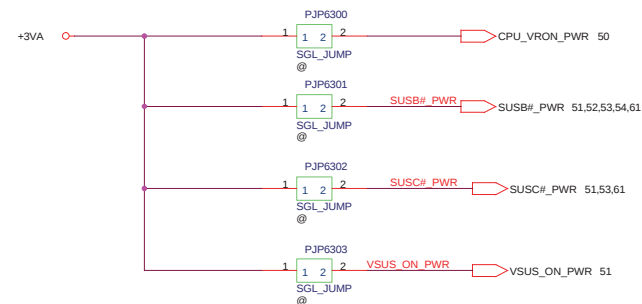


Default Group-optional

ASUS		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer: Anny	
Size	Project Name	Rev	
Custom	T12R	2.0	
Date: Wednesday, August 09, 2006	Sheet	61	of 63



FOR POWER TEST



Default Group-optional

ASUS		Title : POWER_SIGNAL	
<OrgName>		Engineer: Anny	
Size	Project Name	Rev	
Custom	T12R	2.0	
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R1.1

Item	Before	After	Reason	Owner	Date
R11_0606_5100		Add PD5104	for shutdown application		2006.06.06
R11_0606	PC5100: 0.01uF	PC5100 change to 0.047uF	for EE timing request		2006.06.06
R20_0606_5101		add PR5124	Pull ground to avoid vsus_on is float.		2006.06.06
R11_0606_5200	VSUS_ON_PWR	VSUS_ON			2006.06.06
R11_0609_5700		Add PR5735 to +3VA on CHG_EN# pin	To avoid CHG_EN# pin floating in initial		2006.06.06

R2.0

Item	Before	After	Reason	Owner	Date
R20_0731_6000	0.047uF	3900pF	for EE timing request		2006.07.31
R20_0731_5300	None	VTTR	For DDR Vref		2006.07.31

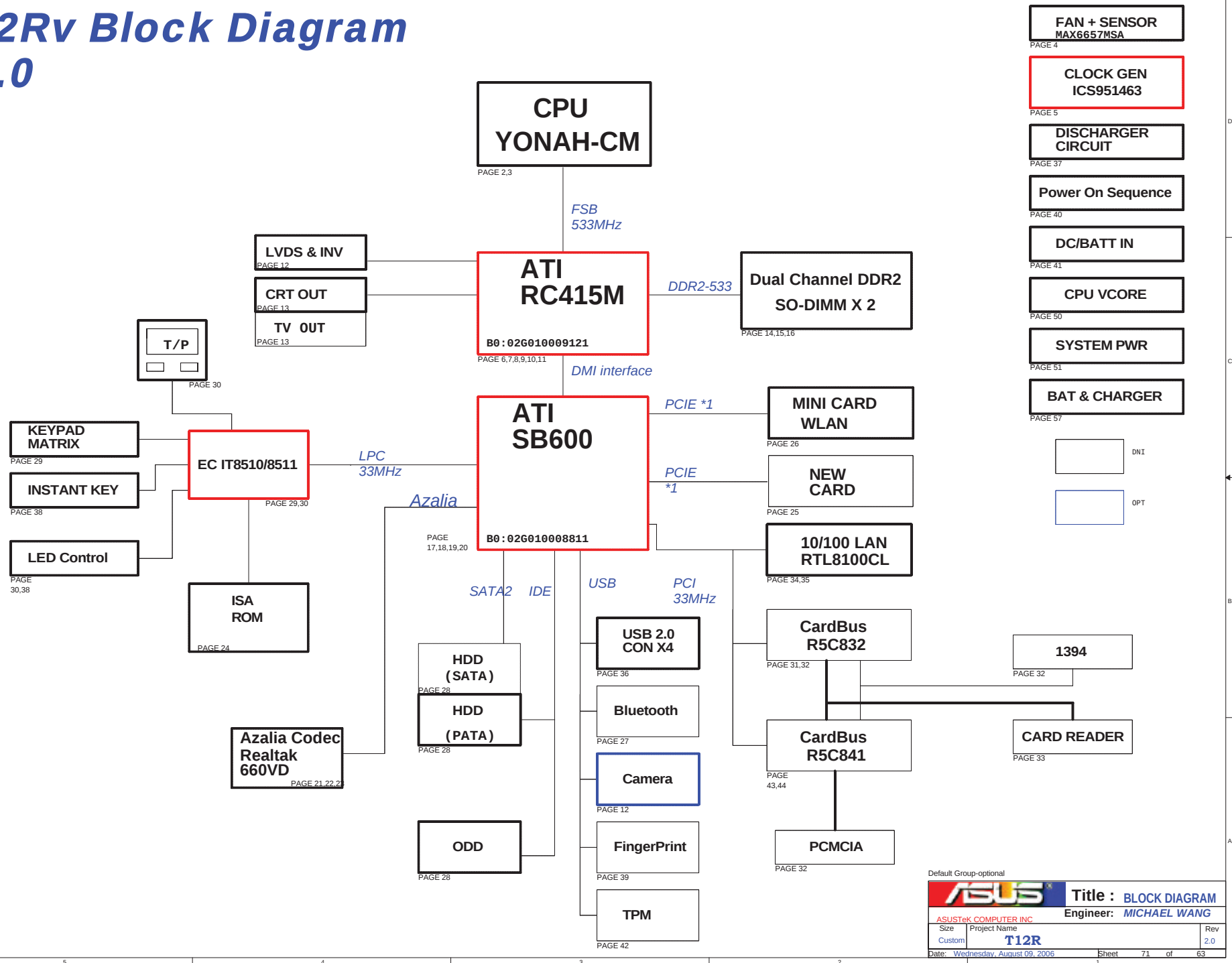
R2.0

Item	Before	After	Reason	Owner	Date

Default Group-optional

		Title : POWER_PIC	
<OrgName>		Engineer:	
Size Custom	Project Name NAPA	Rev 2.0	
Date: Wednesday, August 09, 2006		Sheet 64 of 63	

T12Rv Block Diagram V2.0



T12Rg Block Diagram V1.1

