

Compal confidential

Low Cost Los Angeles 10AL+

NBWAE LA-5831P Schematics Document

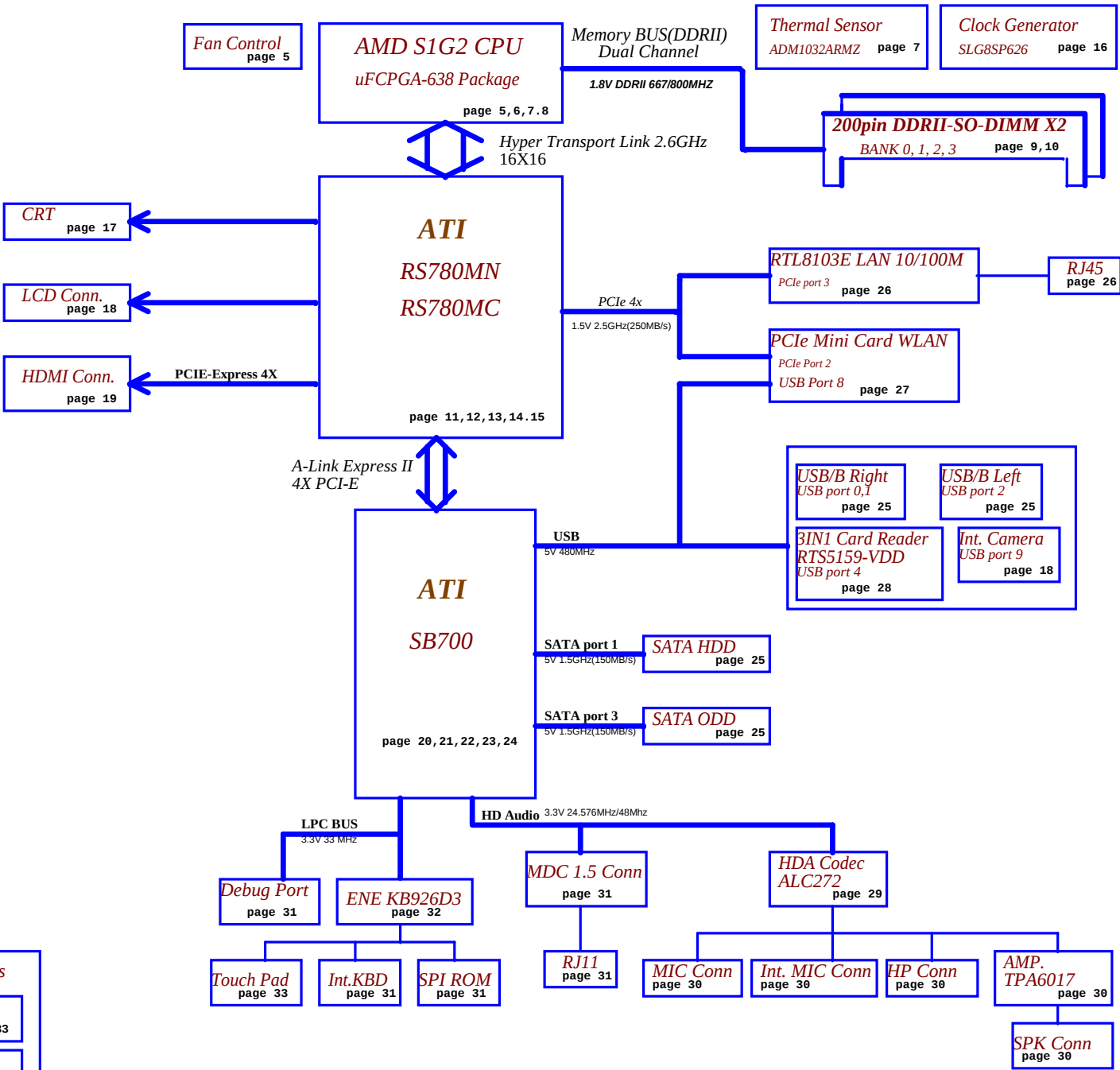
**Mobile AMD S1G2
RS780MN & RS780MC / SB700
2009-08-12 Rev. 1.0**

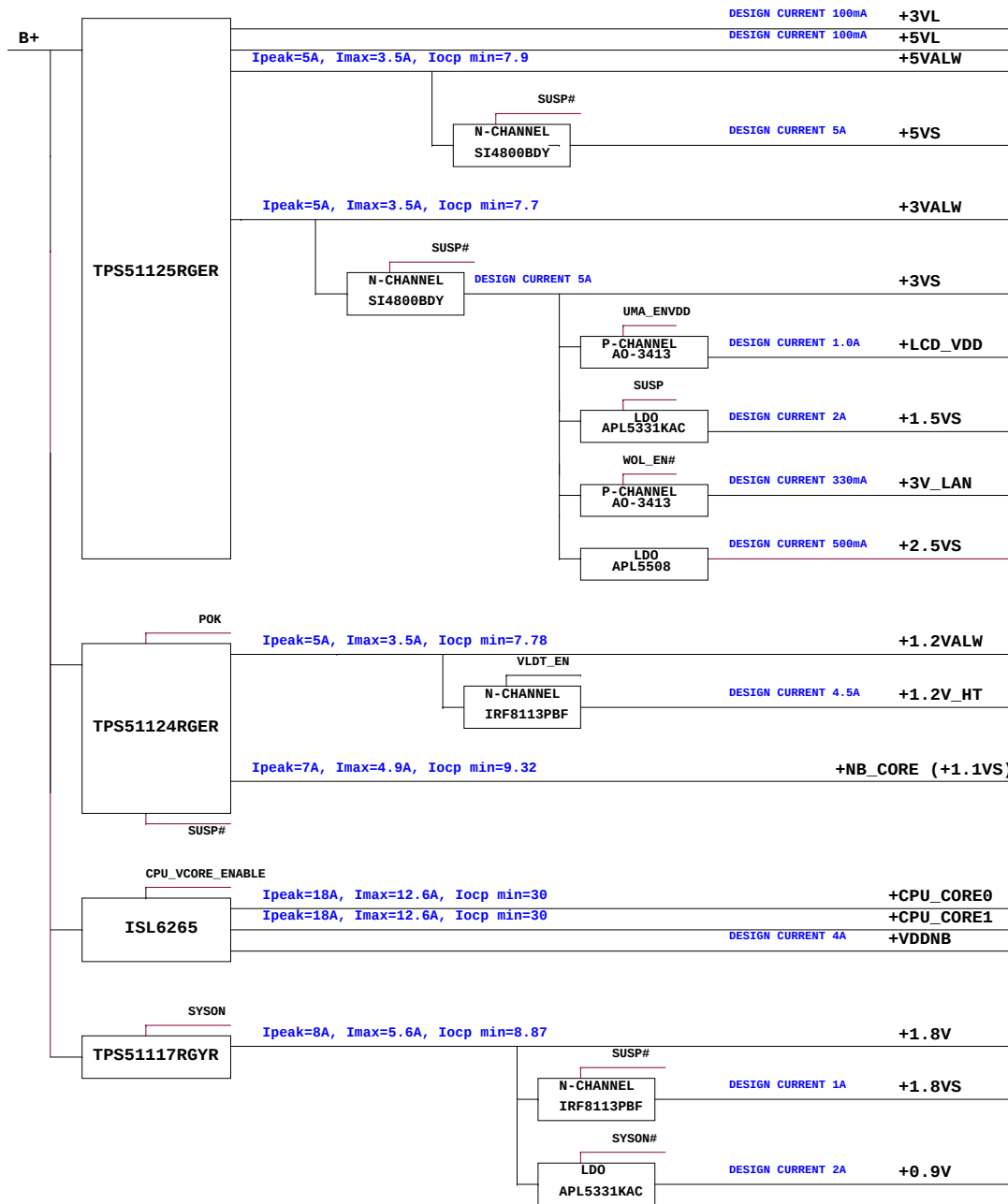
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Cover Sheet	
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Compal Confidential

Model Name : NBWAE

File Name : LA-5831P





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	Power Map
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Voltage Rails

O : ON
X : OFF

State	power plane			
	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.2V_HT +VDDNB +CPU_CORE_0 +CPU_CORE_1
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SB700 SM Bus0 Address				SB700 SM Bus1 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

KB926 SM Bus1 Address				KB926 SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
KB926 ESB Address							
	Power	Device	HEX	Address			
	+3VL	Cap. Sensor		Virtual I2C			

Platform	CPU	NB	SB
PUMA@	S1G2	RS780MC	SB700
	S1G2	RS780MN	SB700
TIGRIS@	S1G3	RS880MC	SB710
	S1G3	RS880M	SB710

@ : just reserve , no build

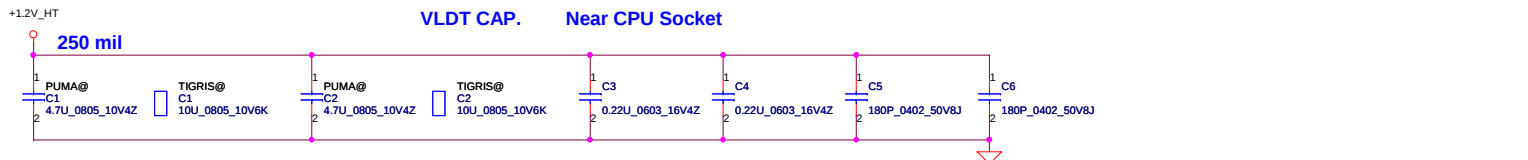
BTO (Build-To-Order) Option Table

Function	Modem	HDMI	CAMERA & MIC	
Description	(R)	(Y)	(X)	
Explain			CAMERA	MIC
BTO	MDC@	HDMI@	CAM@	MIC@

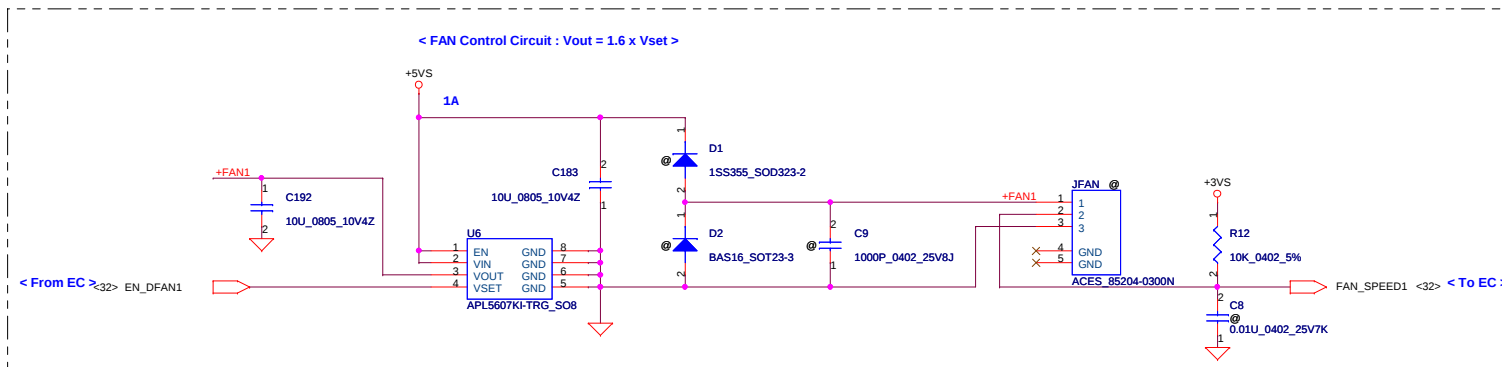
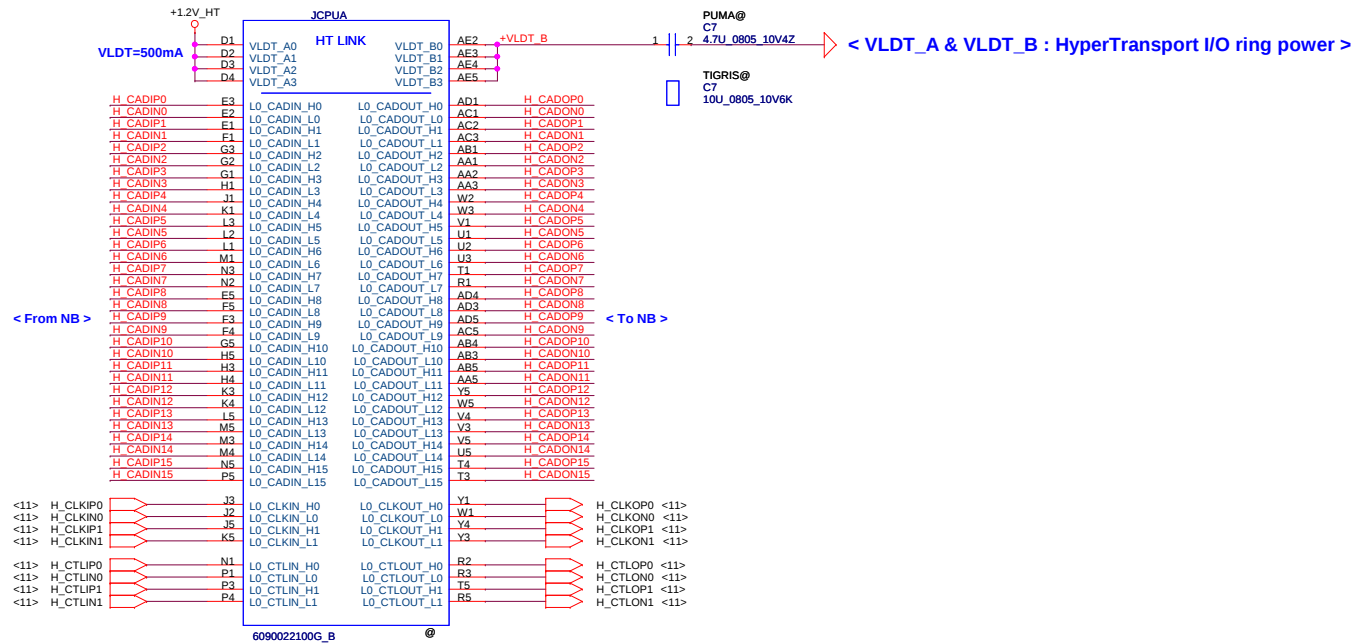
SMBUS Control Table

	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD
EC_SMB_CK1 EC_SMB_DA1	KB926		V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V						
I2C_CLK I2C_DATA	RS780MN RS780MC								V		
DDC_CLK0 DDC_DATA0	RS780MN RS780MC									V	
DDC_CLK1 DDC_DATA1	RS780MN RS780MC										
SCL0 SDA0	SB700					V	V				
SCL1 SDA1	SB700							V			
SCL2 SDA2	SB700										
SCL3 SDA3	SB700										

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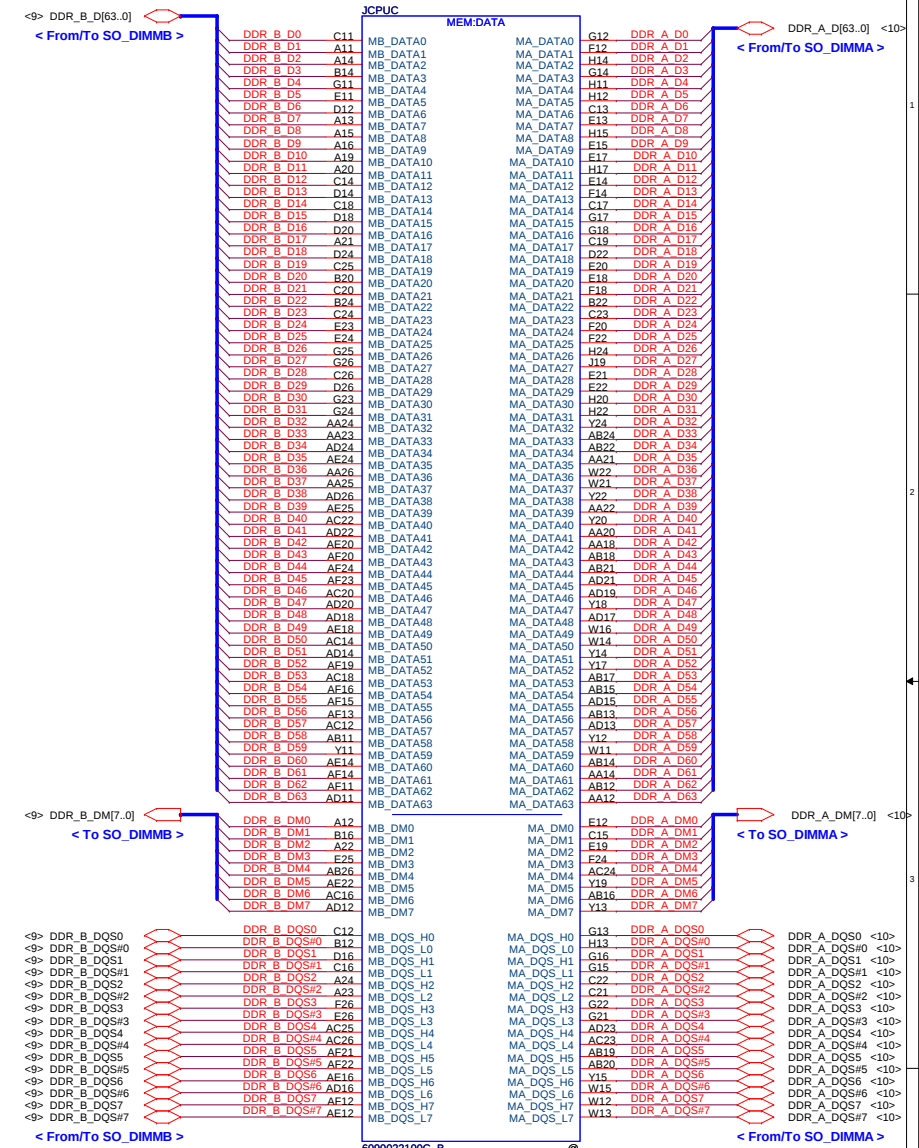
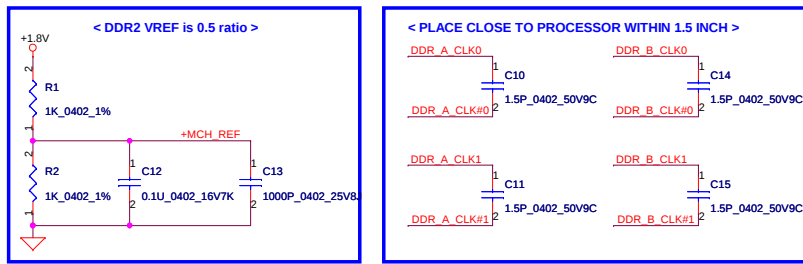


<11> H_CADIP[0..15] → H_CADIP[0..15] → H_CADOP[0..15] <11>
 <11> H_CADIN[0..15] → H_CADIN[0..15] → H_CADON[0..15] <11>

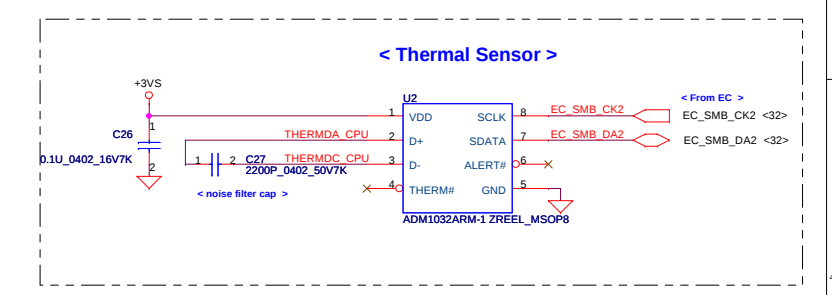
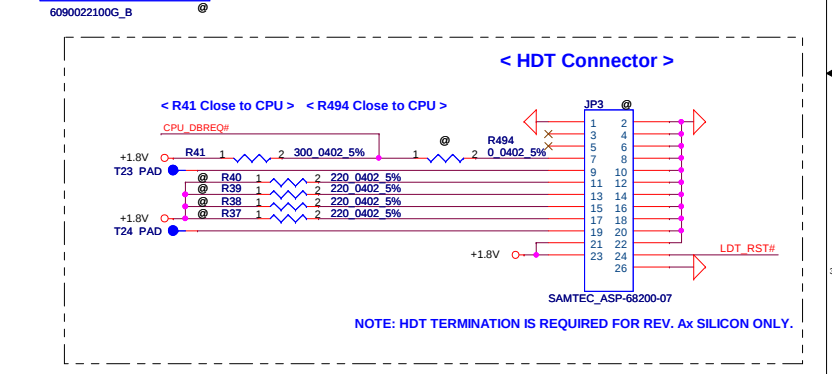
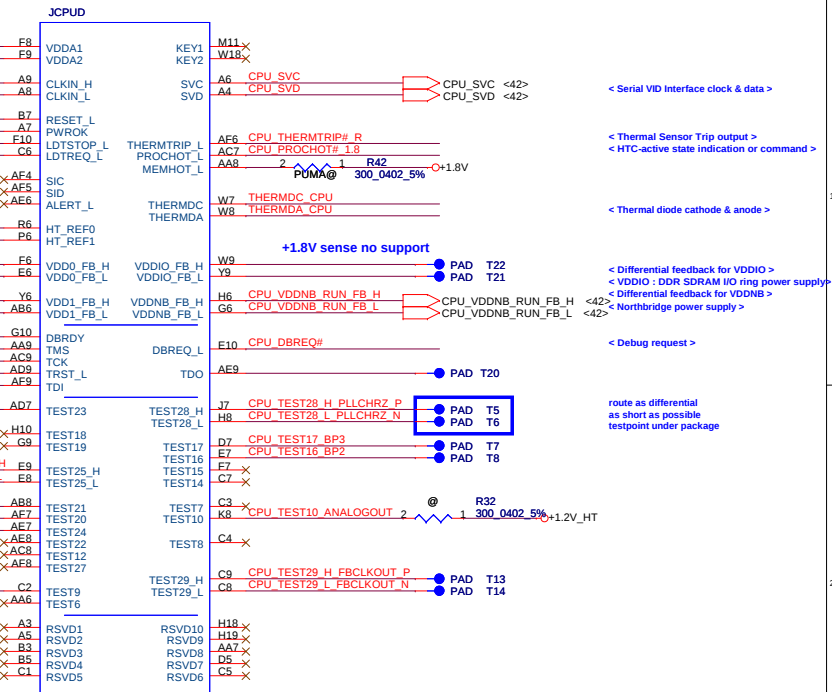
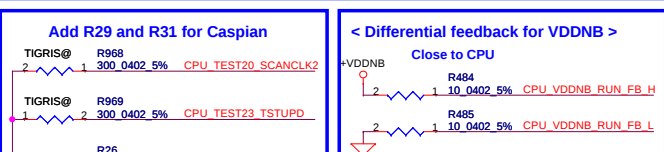
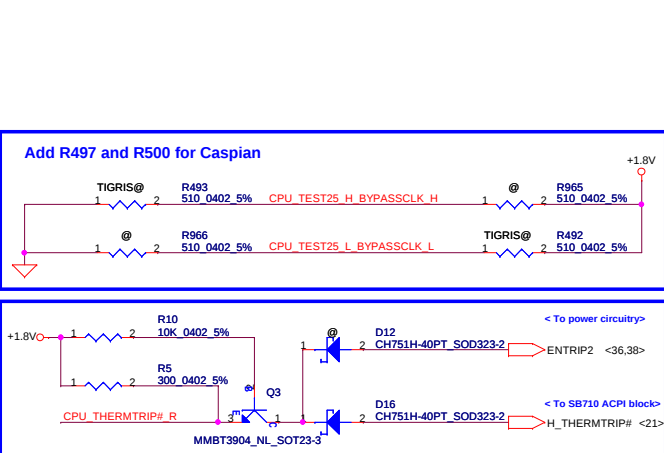
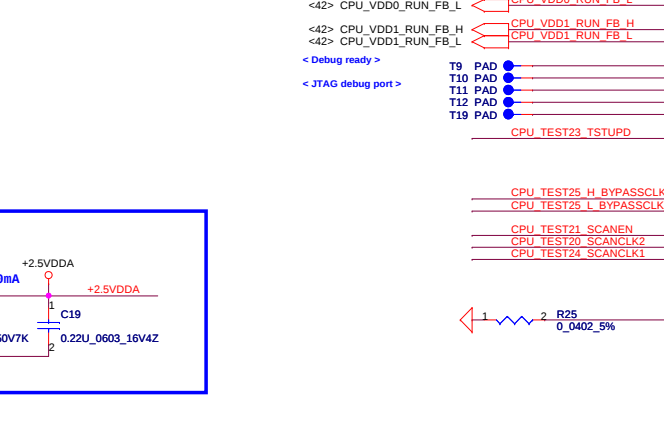
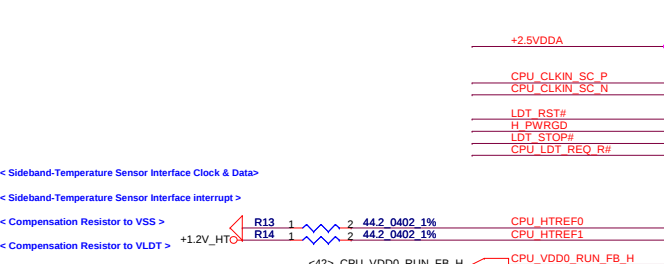
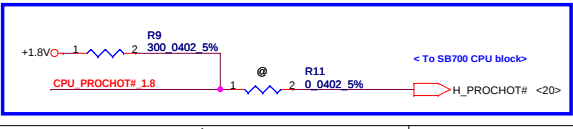
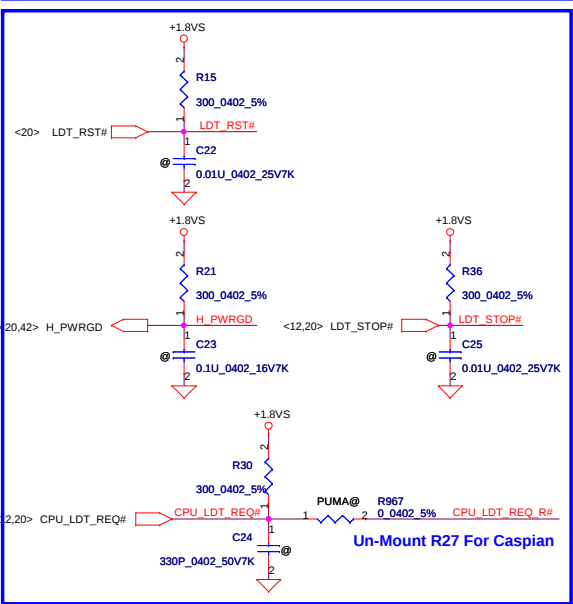
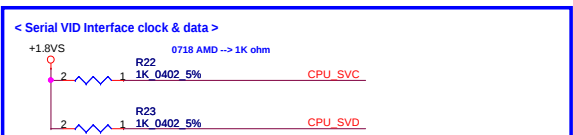
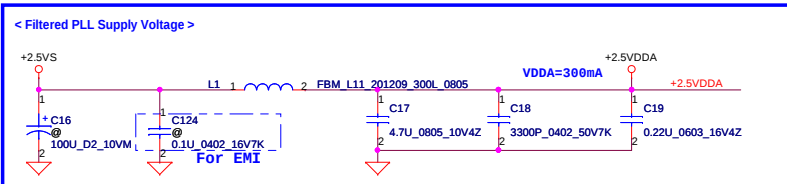
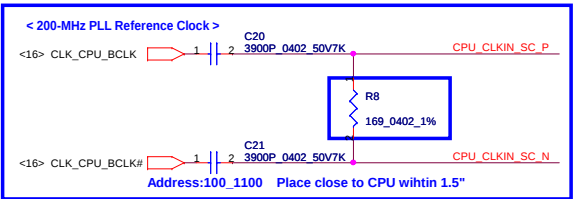
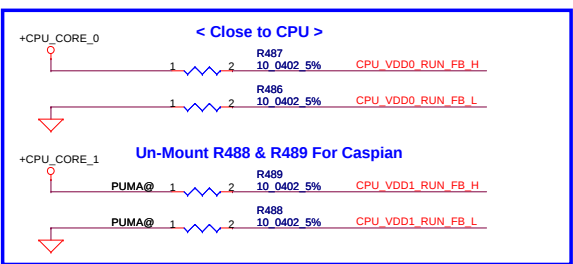


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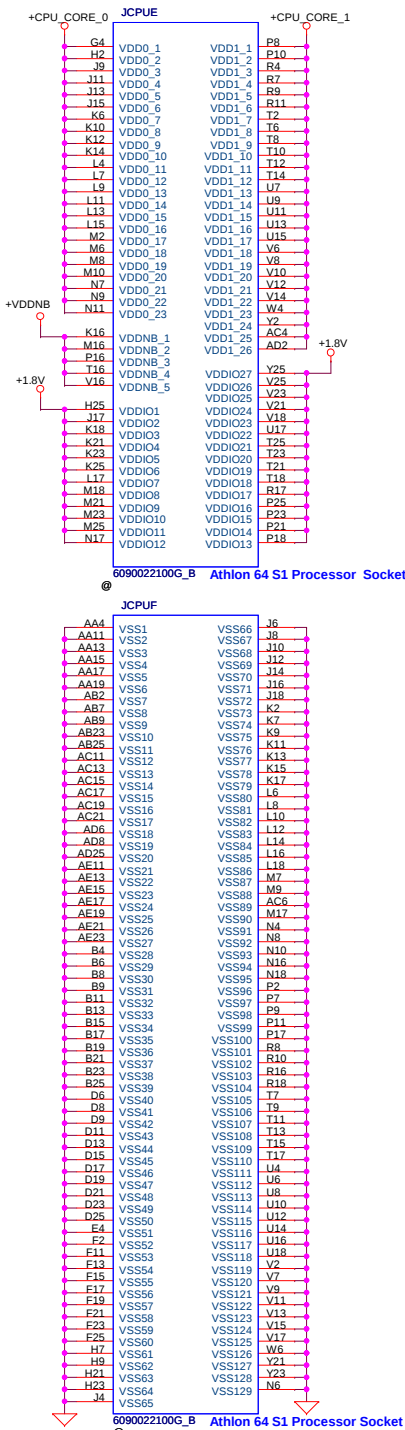
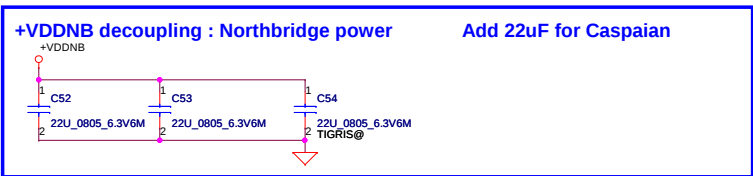
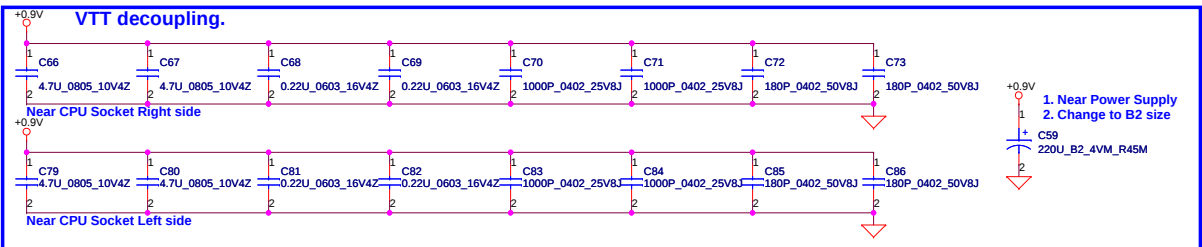
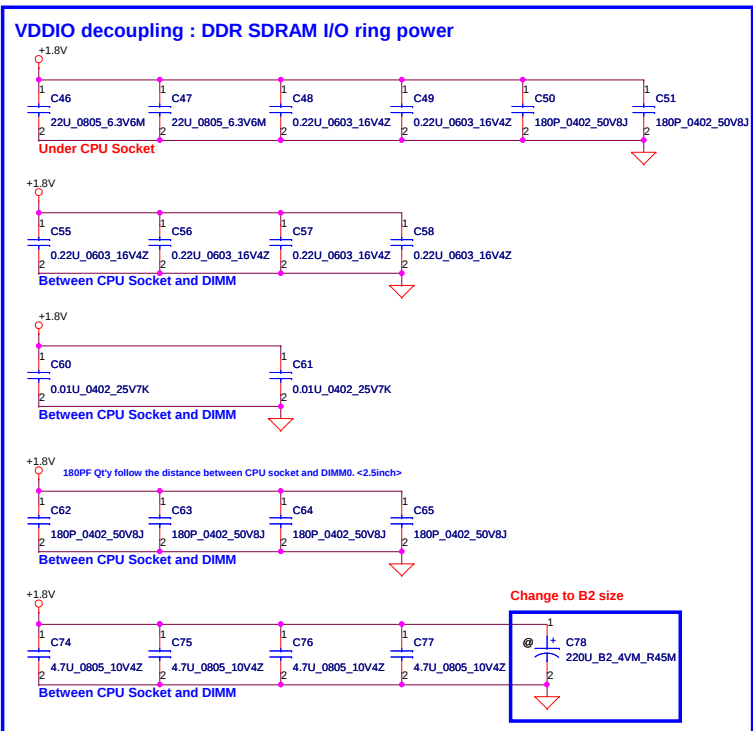
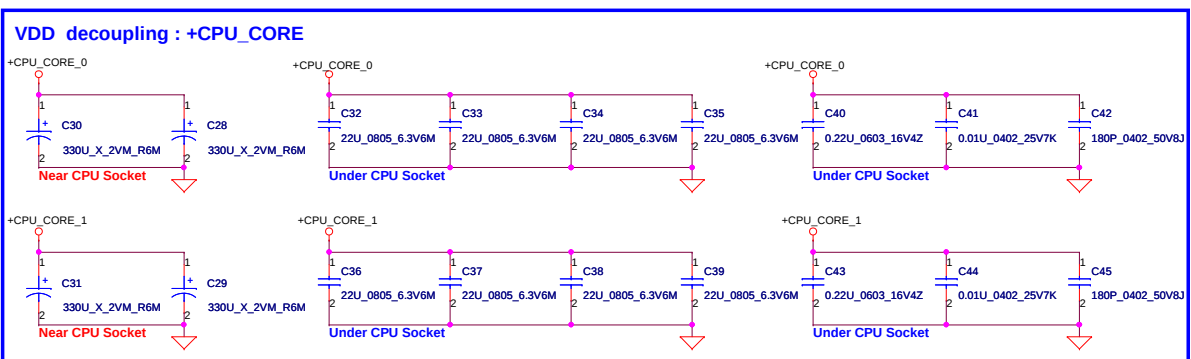
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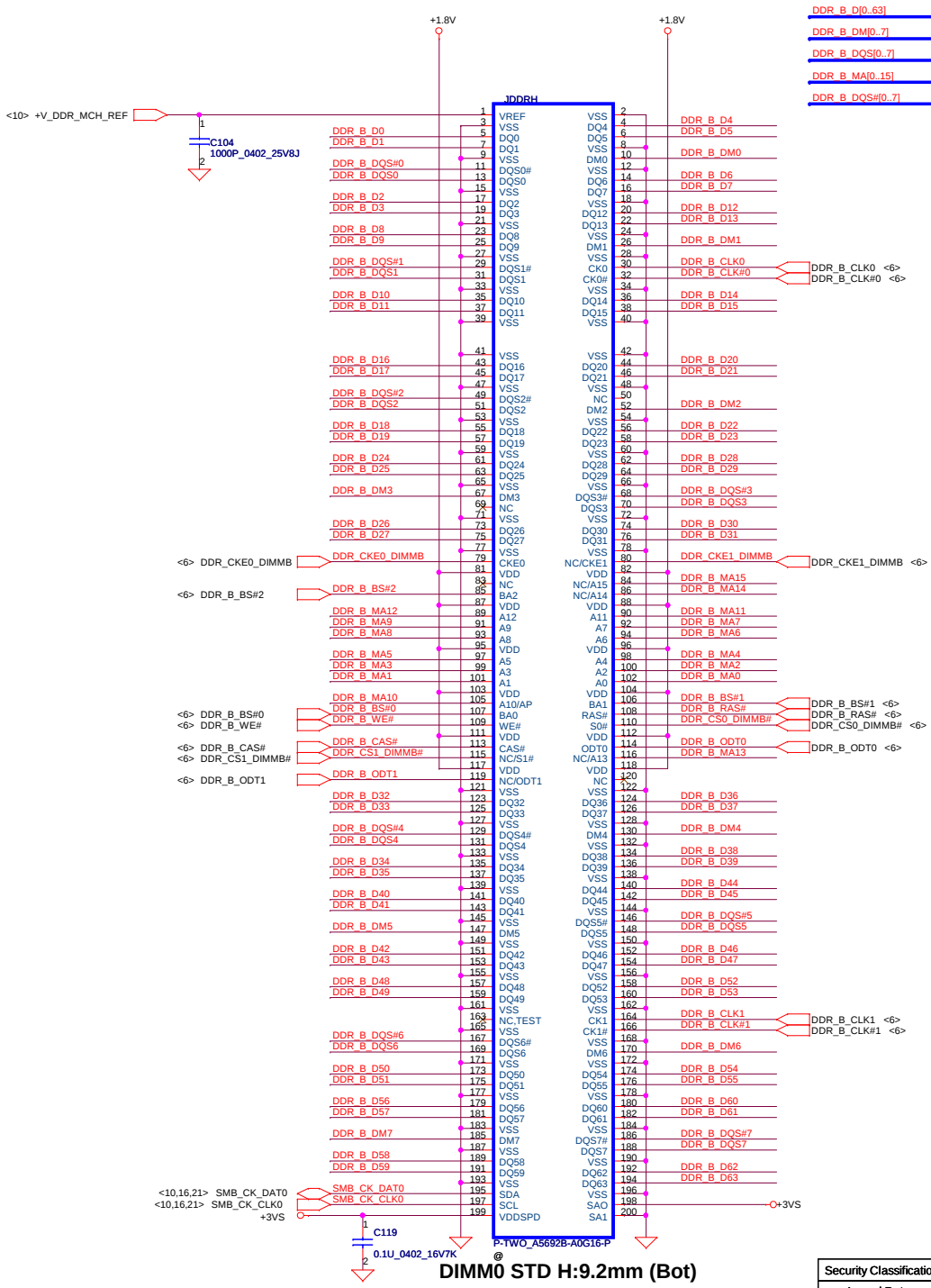


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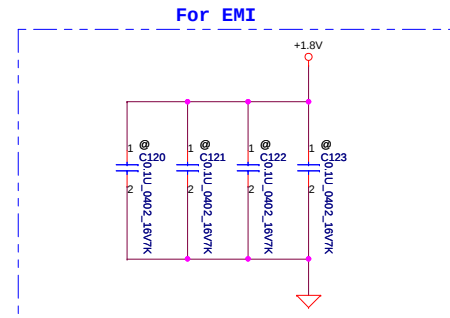
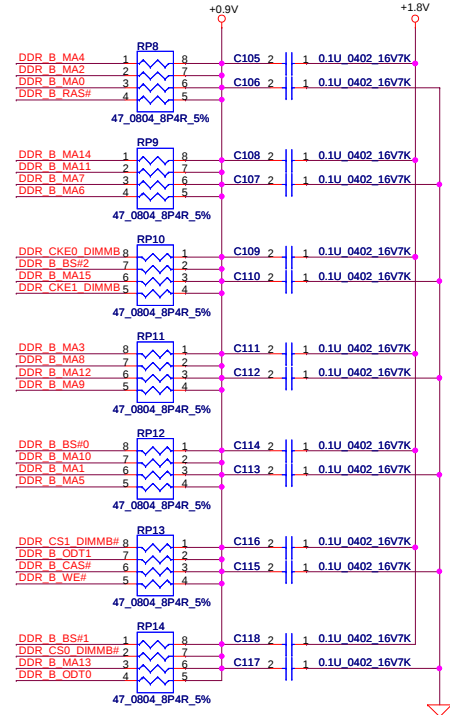


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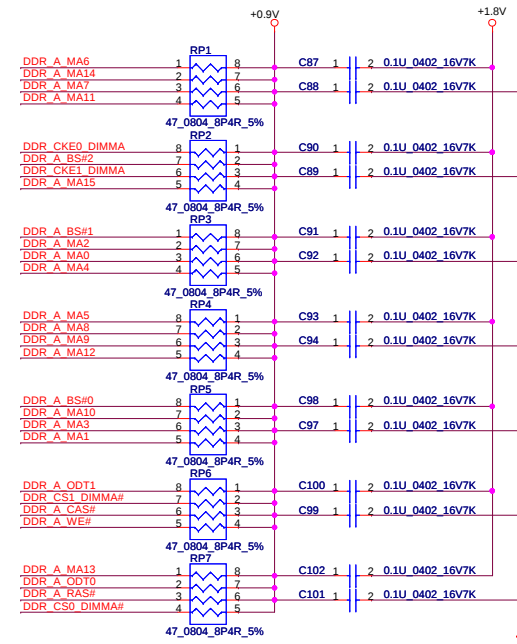
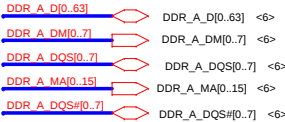




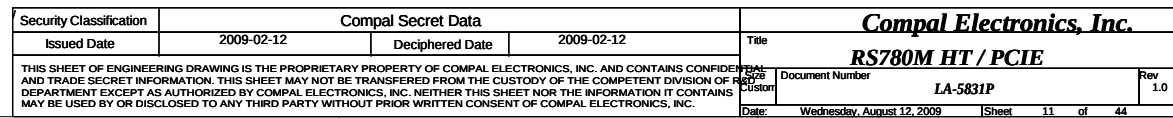
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- DDR_B_DM[0..7] <6>
- DDR_B_DQS[0..7] <6>
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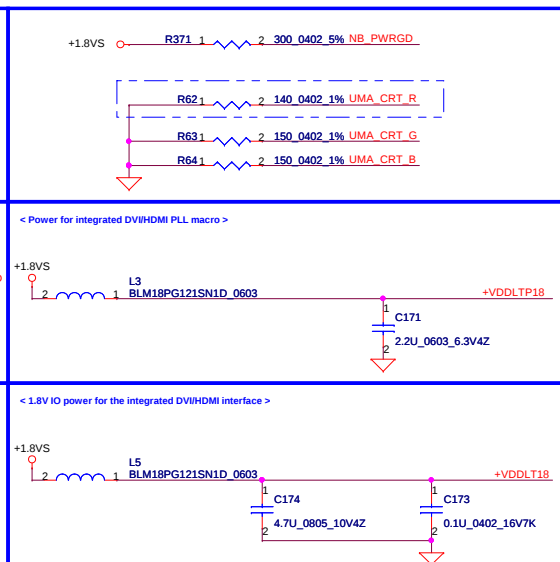
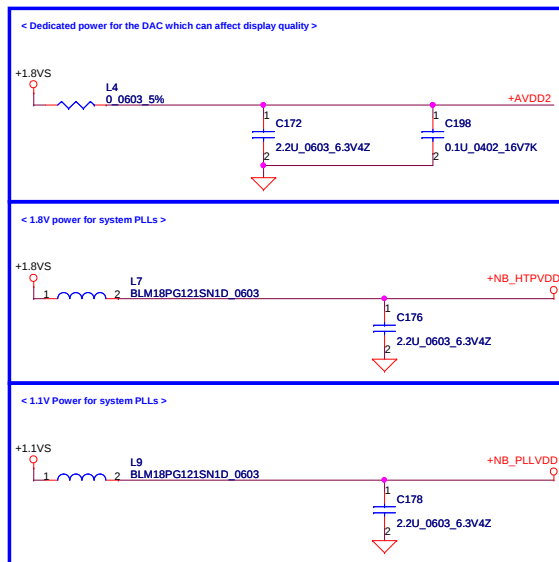
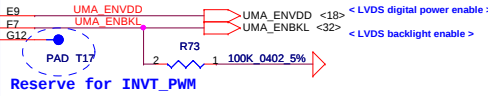


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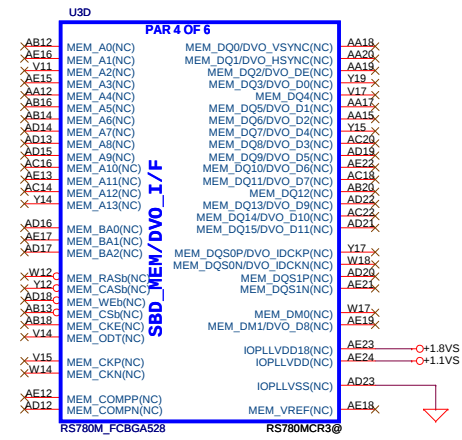


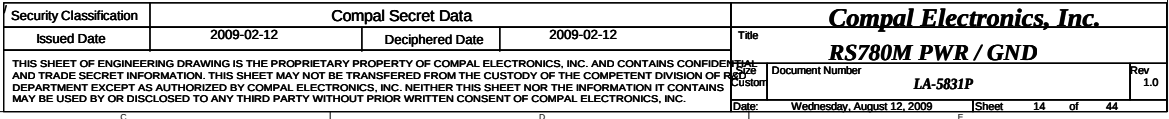
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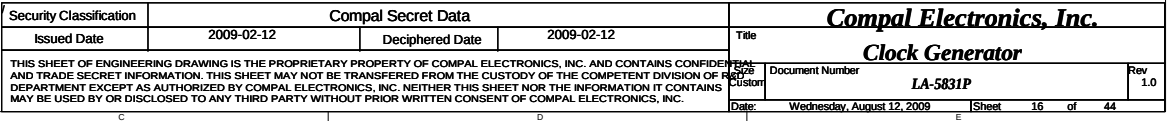
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	RS780M VEDIO/CLK GEN
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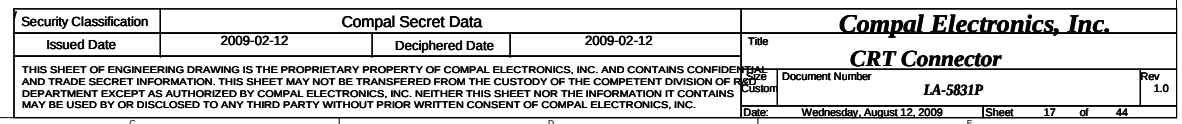
< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K > SI2: Change to 3K pull high <12.17> UMA_CRT_VSYNC R101 3K_0402_5% +3VS R102 3K_0402_5%	< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb > Enables the Test Debug Bus using GPIO. 1 : Enable (RX780, RS780) 0 : Disable (RX780, RS780) PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#
< RS780 use register to control PCI-E configure >	< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] > These pin straps are used to configure PCI-E GPP mode. 000 : 00001 001 : 00010 010 : 01011 011 : 00100 100 : 01010 101 : 01100 111 : 01011
< RS780 DFT_GPIO1 > <12> AUX_CAL R104 150_0402_1% +3VS <12.21> SUS_STAT# D4 CH751H-40PT_SOD323-2 PLT_RST# <12.20,26,27,31,32>	< DFT_GPIO1 : LOAD_EEPROM_STRAPS > Selects Loading of STRAPS from EPROM 1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected RS740/RX780: DFT_GPIO1 RS780:SUS_STAT
< RS780 use HSYNC to enable SIDE PORT (internal pull high) > <12.17> UMA_CRT_HSYNC R125 3K_0402_5% +3VS	< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb > RX780: Enables the Test Debug Bus using PCIE bus 1 : Disable (Can still be enabled using nbcfg register access) 0 : Enable RS780: Enables Side port memory (RS780 use HSYNC#) 1. Disable (RS780) 0 : Enable (RS780)

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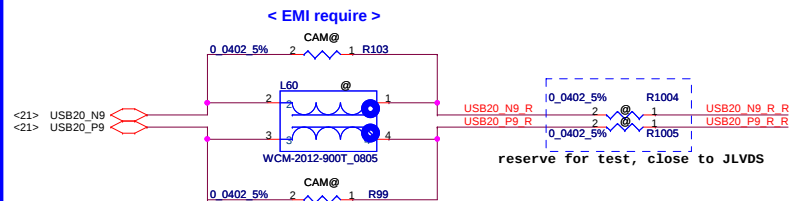


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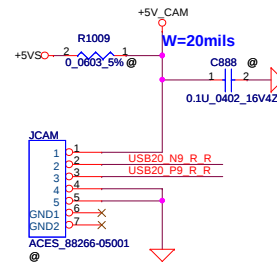
RS780 DAC_SCL & SDA is 5V tolerance



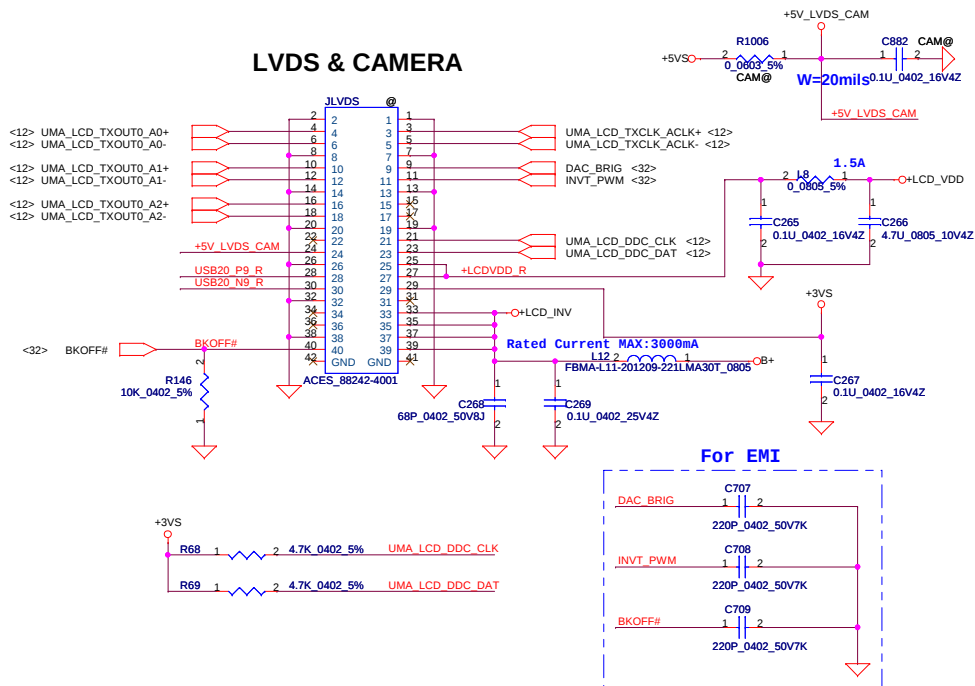
< Int. Camera, USB port 9 >



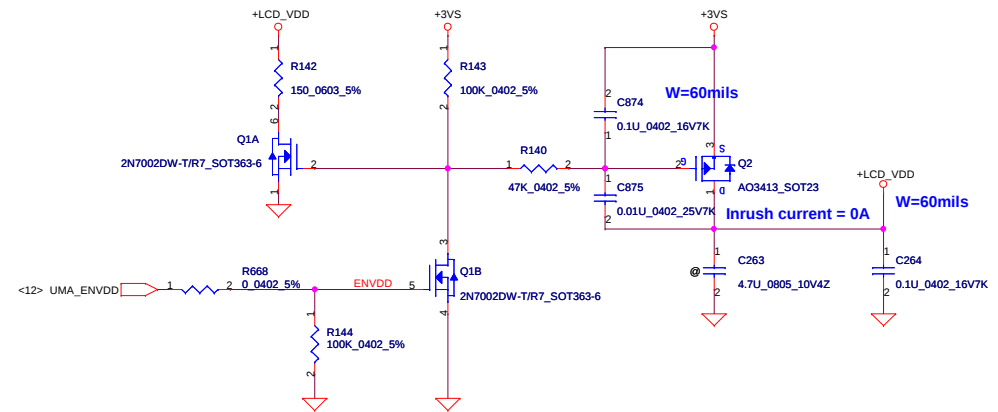
Int. Camera



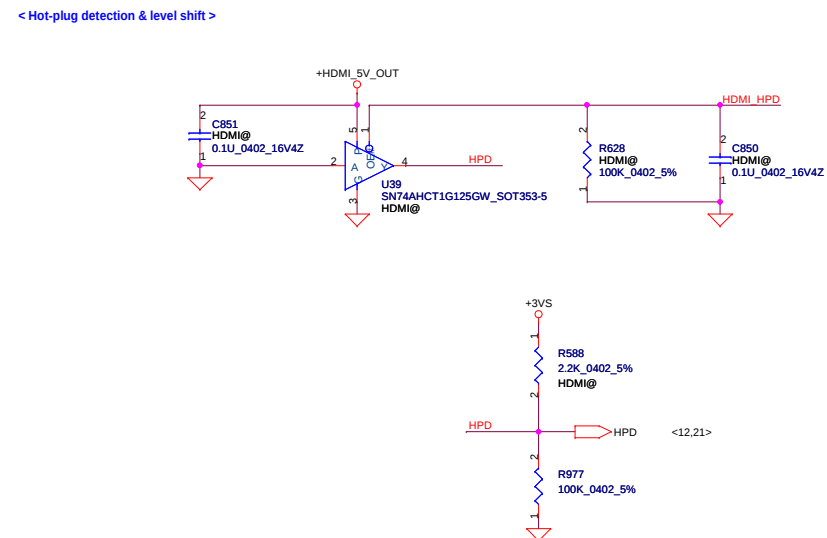
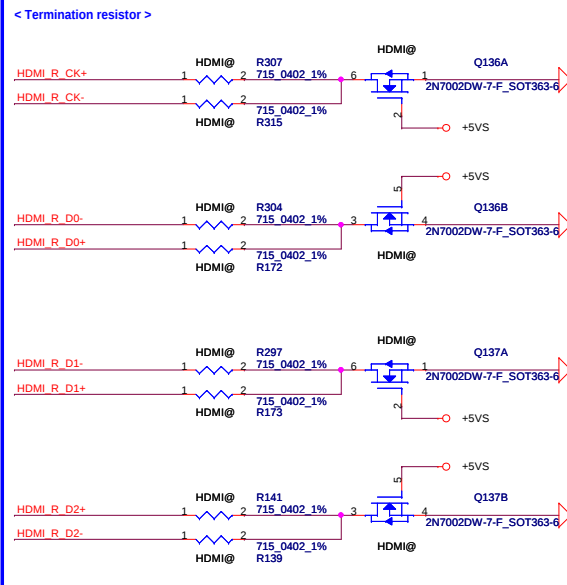
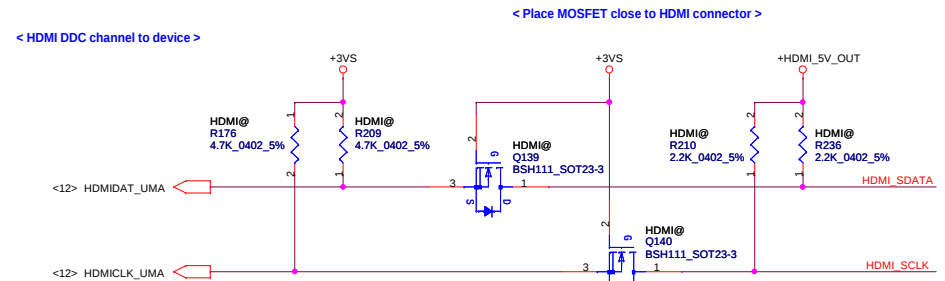
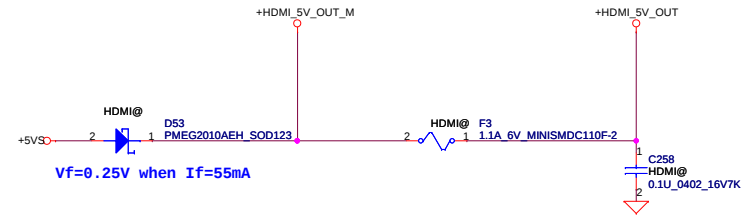
LVDS & CAMERA



LCD/PANEL BD. Conn.



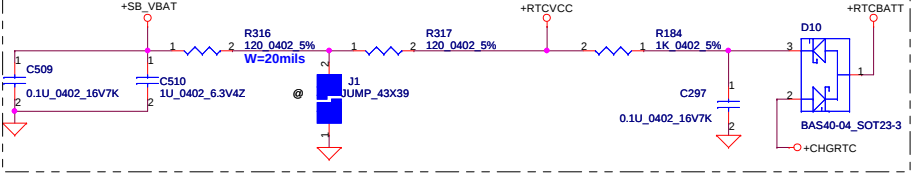
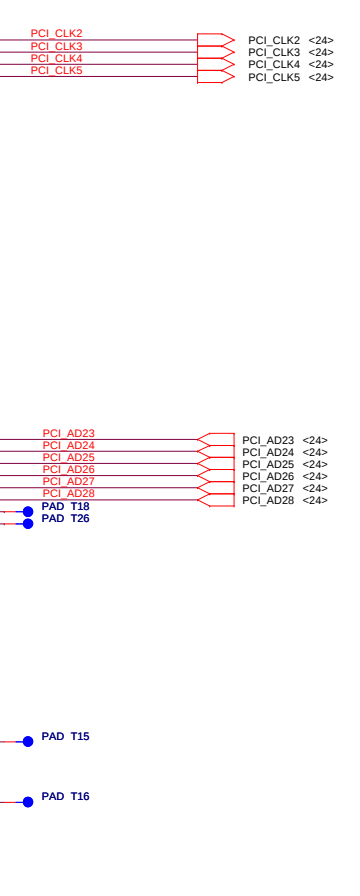
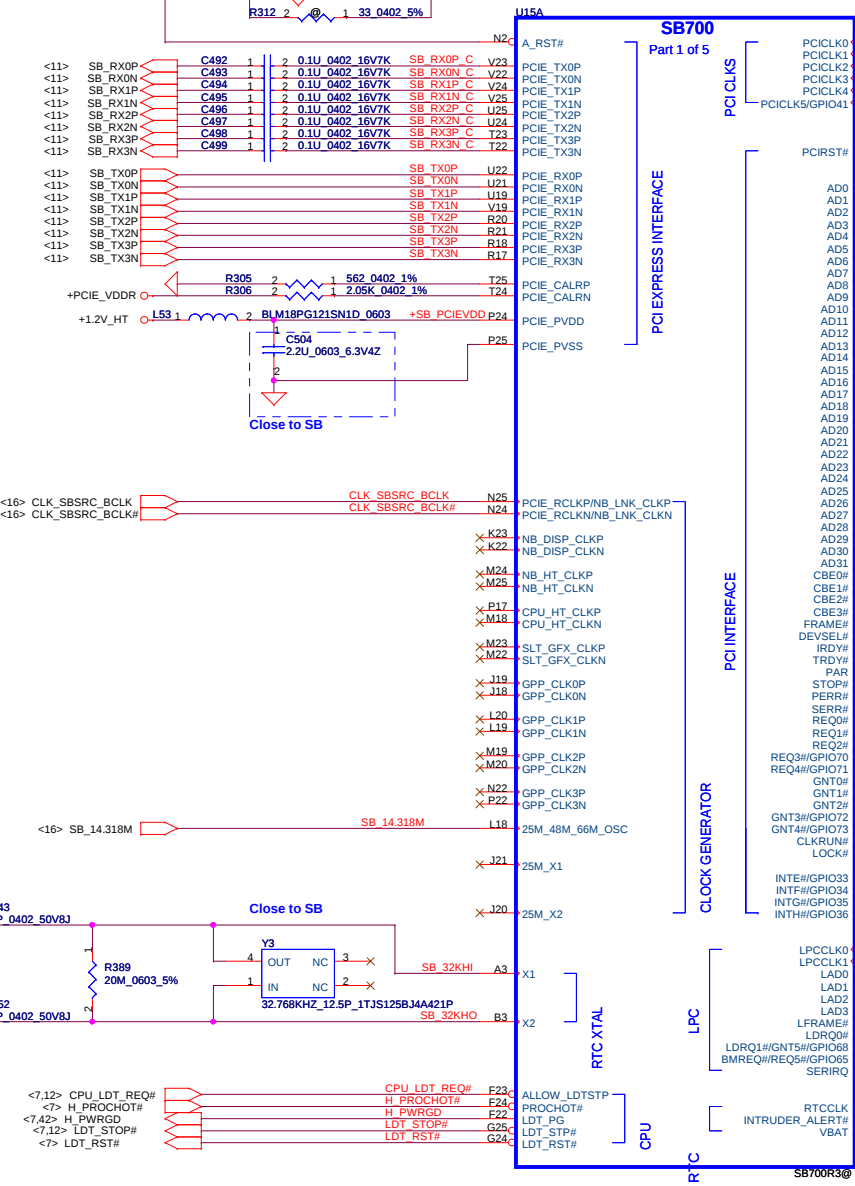
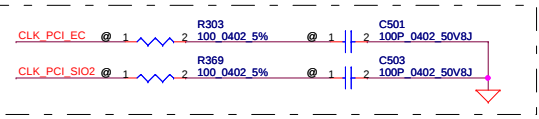
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						Document Number		LA-5831P		Rev	
										1.0	
						Date:		Wednesday, August 12, 2009		Sheet	



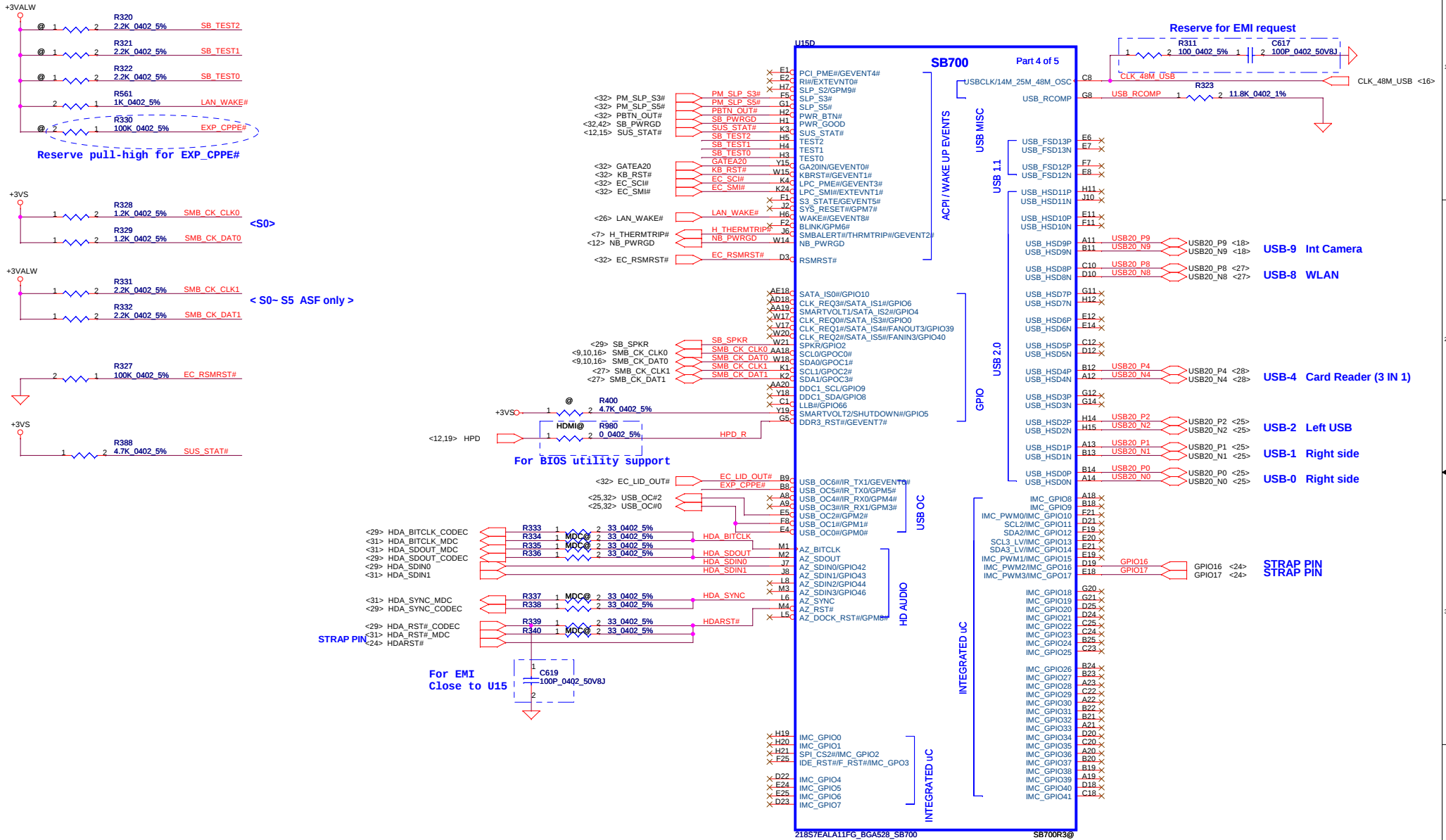
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date	2009-02-12	Deciphered Date	2009-02-12	HDMI					
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				Doc Number	LA-5831P			Rev	1.0
				Date	Wednesday, August 12, 2009			Sheet	19 of 44

< x4 PCIe A-link To NB >

< x4 PCIe A-link from NB >



Security Classification		Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 - PCIE / PCI / ACPI / LPC / RTC	Document Number
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				Wednesday, August 12, 2009	Sheet 20 of 44



Security Classification	Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 USB / AC97
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Date: Wednesday, August 12, 2009				Sheet 21 of 44

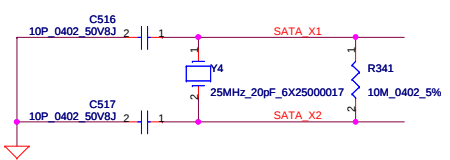
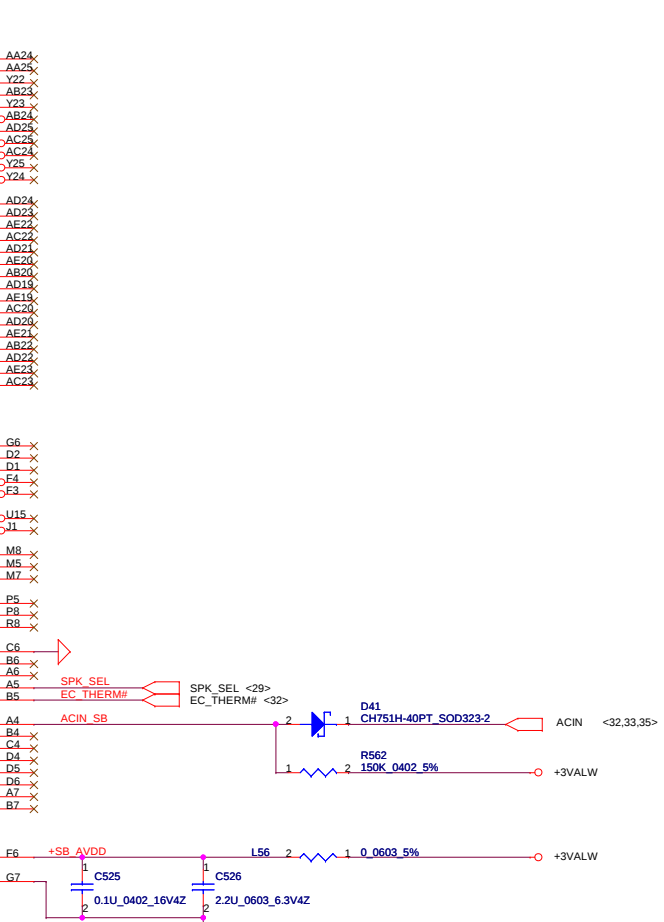
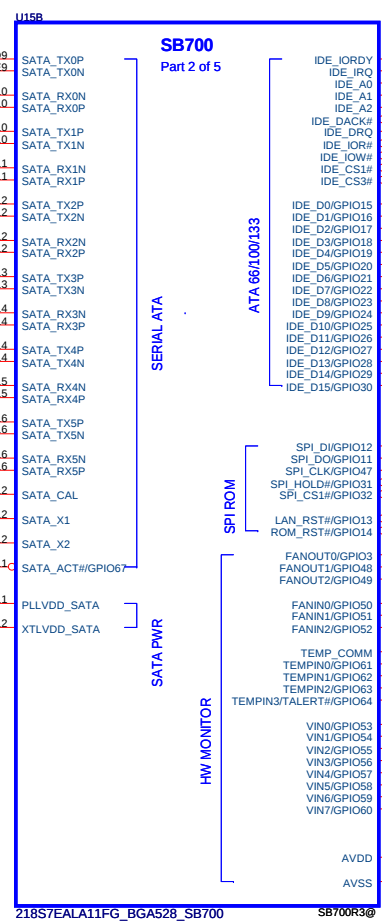
HDD

ODD

2

3

4

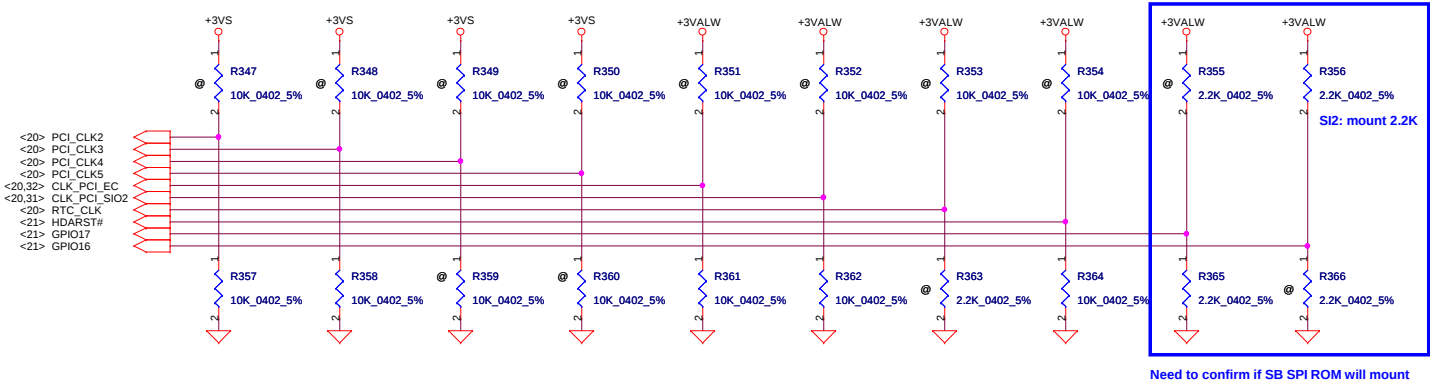


Security Classification	Compal Secret Data			Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 SATA / IDE / SPI	
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

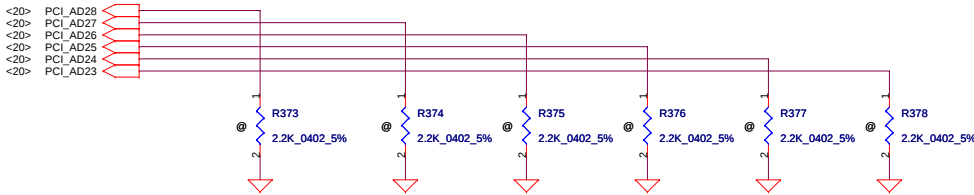
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM



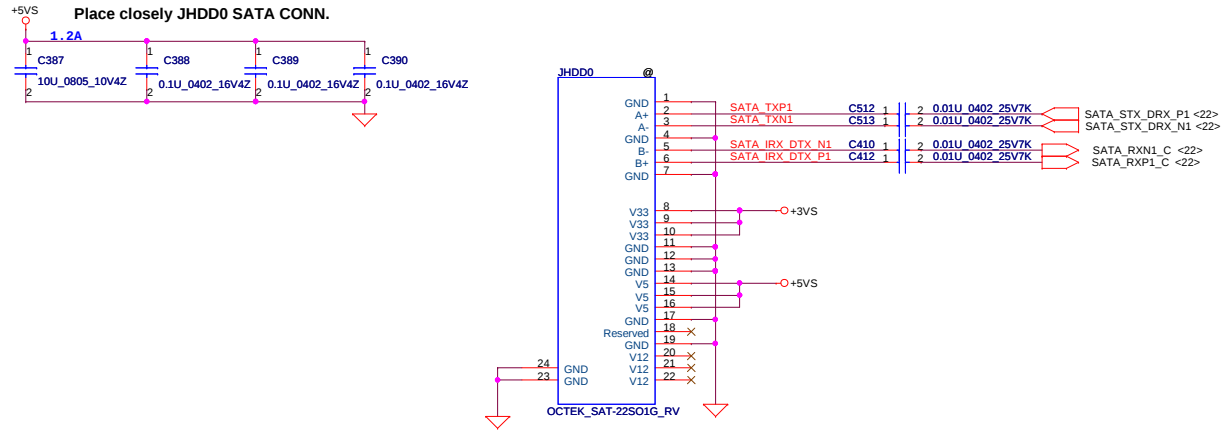
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

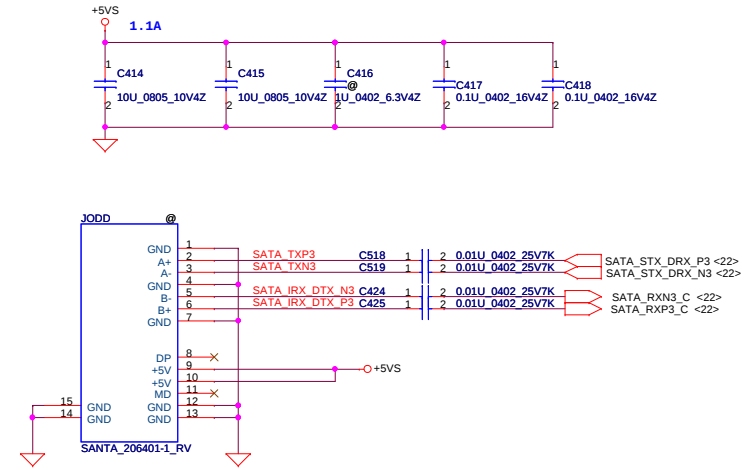
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



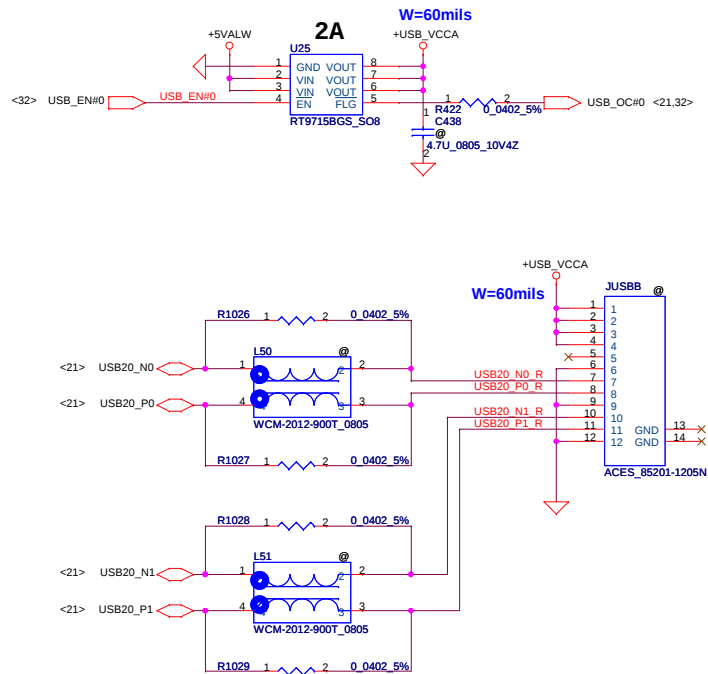
SATA HDD Conn.



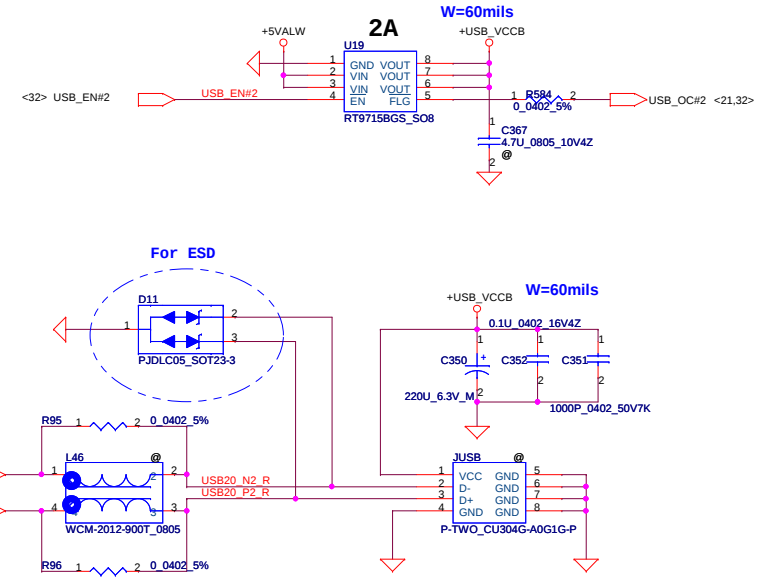
SATA ODD Conn



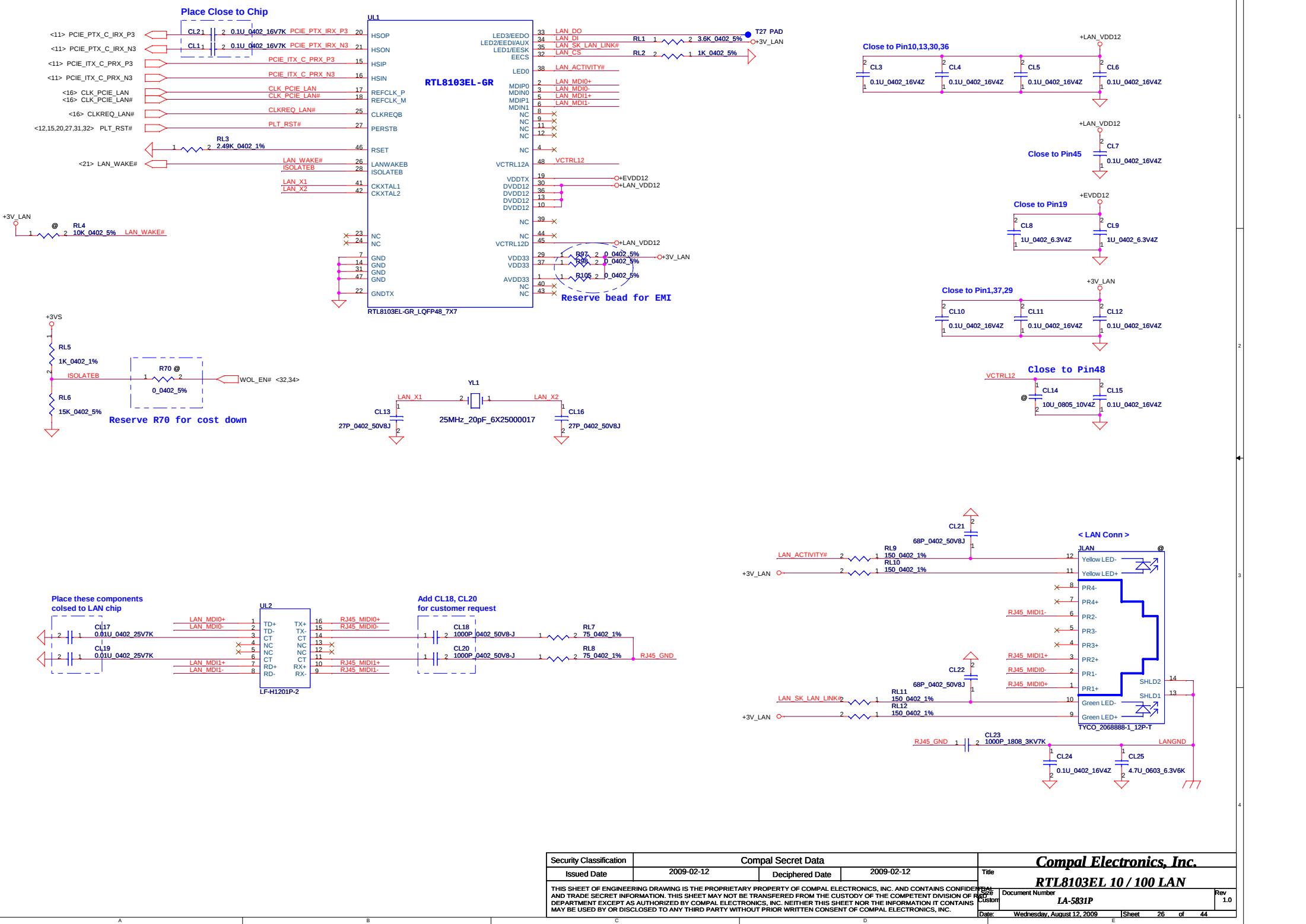
USB Right Board



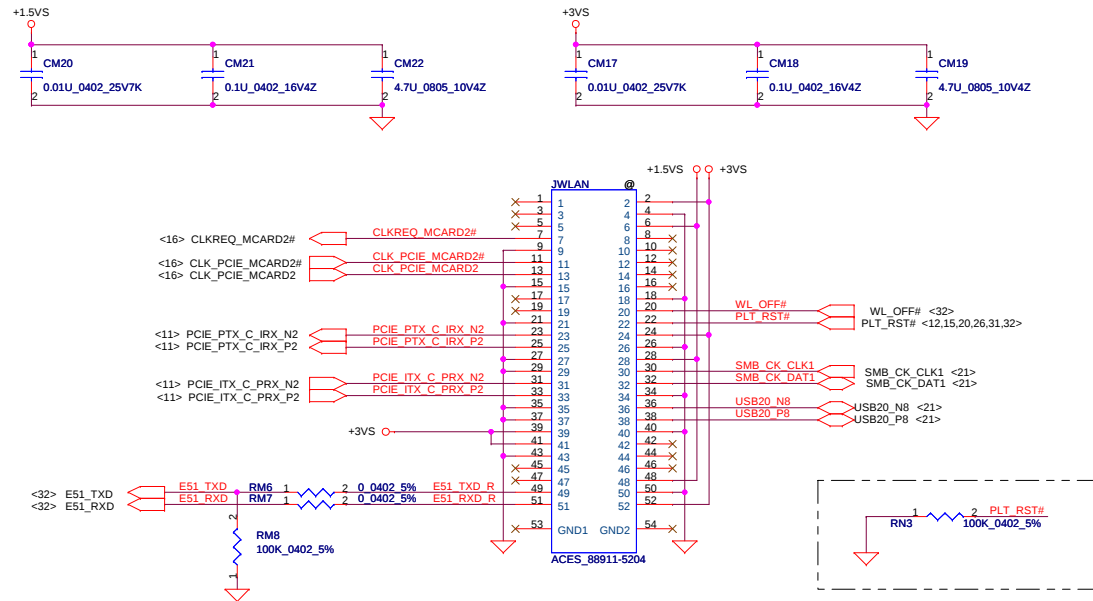
USB Left Conn



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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	SATA HDD/ODD
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< PCIe Mini Card for WLAN/ WiMAX >

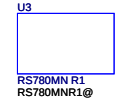


<NB & SB >

< R1 for customer BOM STRUCTURE >

< R3 for mass production BOM STRUCTURE >

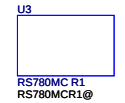
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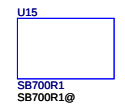
RS780MN



RS780MC



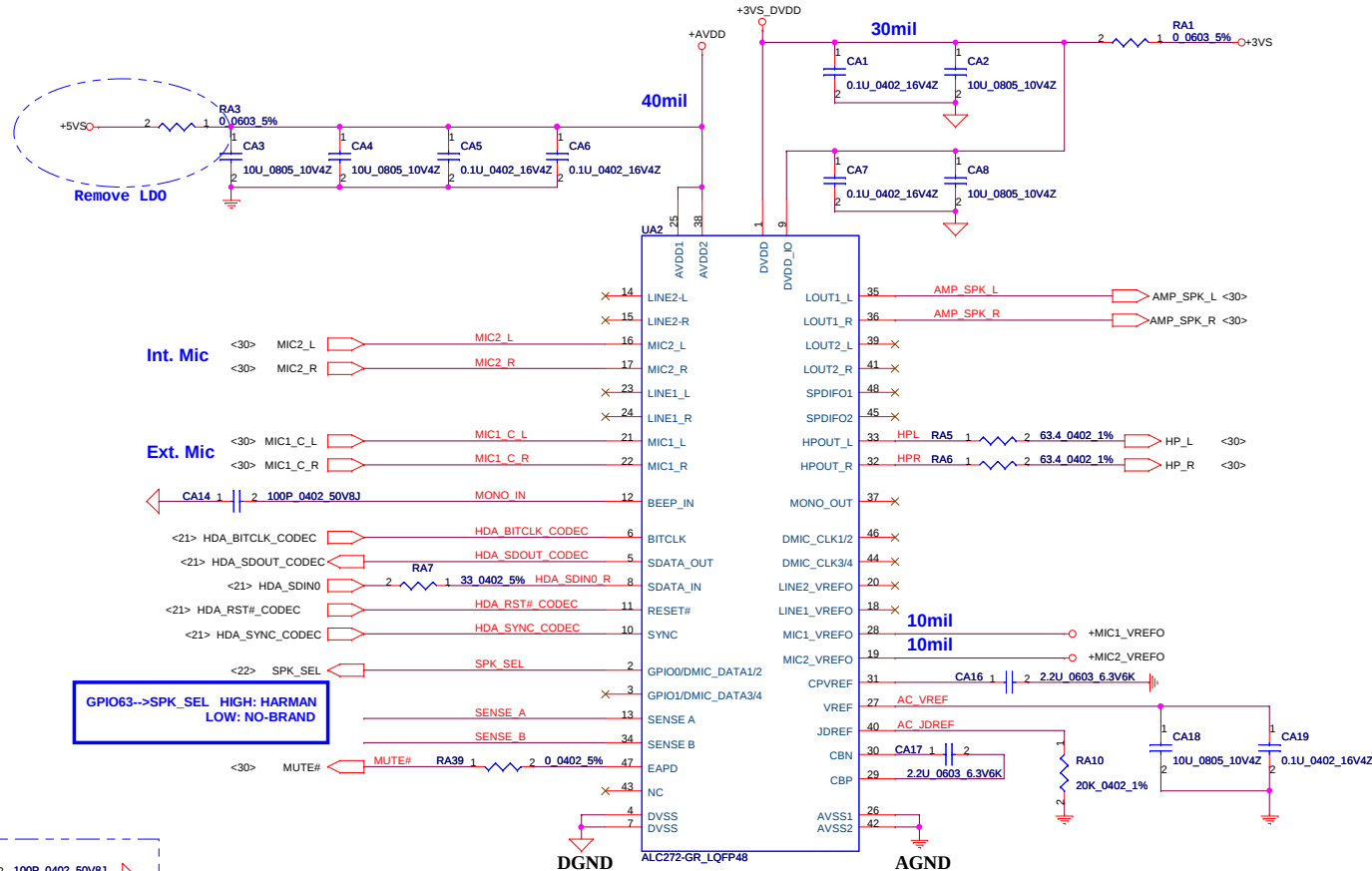
SB700



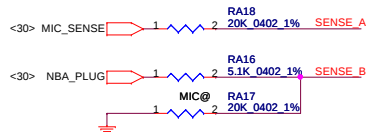
< PCB >

PCB



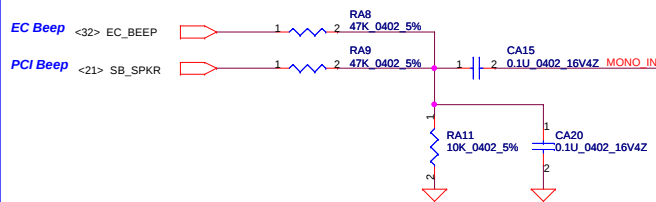


< SENSE_A & SENSE_B, place close to chip >

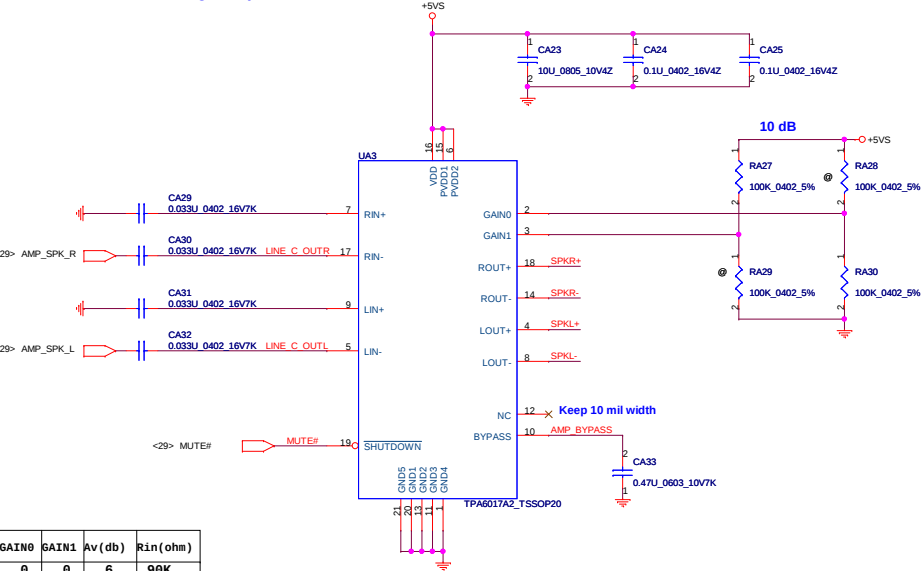


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

< MONO_IN SOURCE >

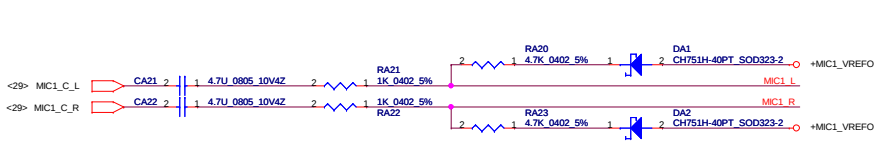


< TPA6017 Medium Range Amplifier >

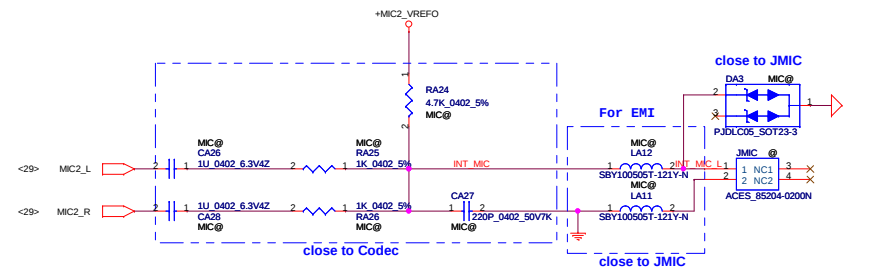


GAIN0	GAIN1	Av (db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

< Ext. Mic >

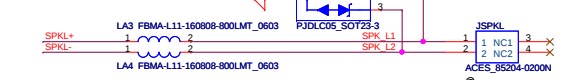


< Int. Mic >

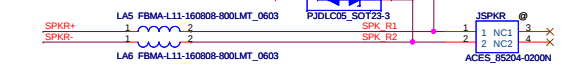


< Speaker Connector >

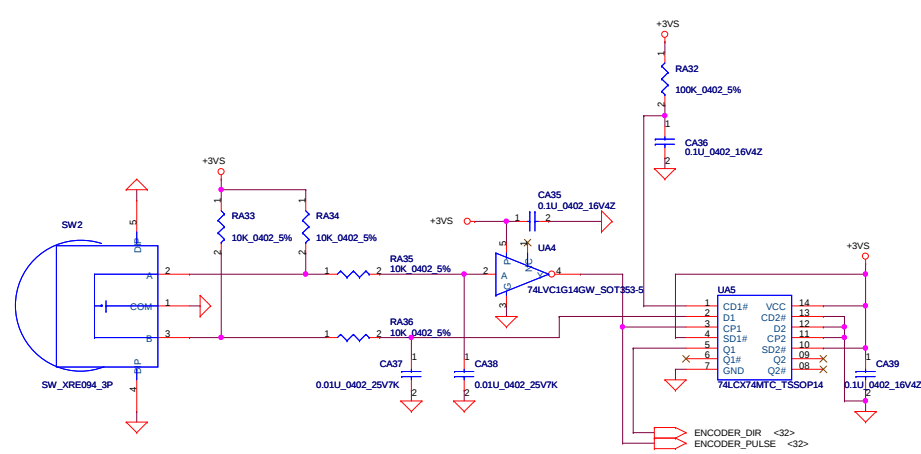
Left Connector



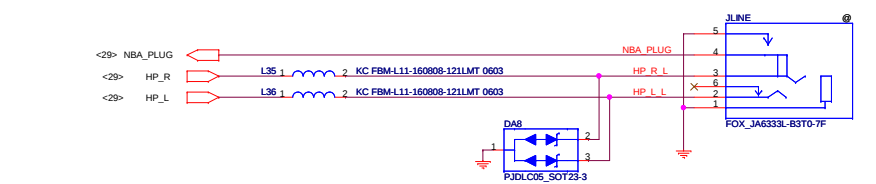
Right Connector



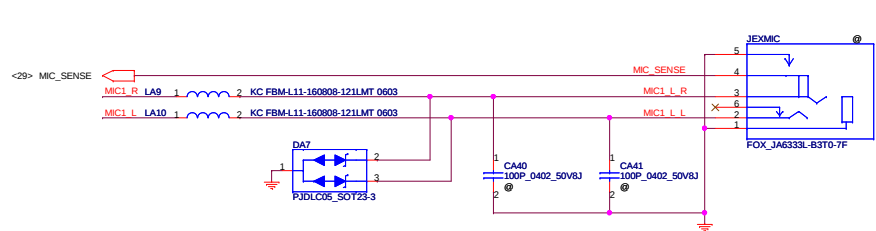
< Volume Control >



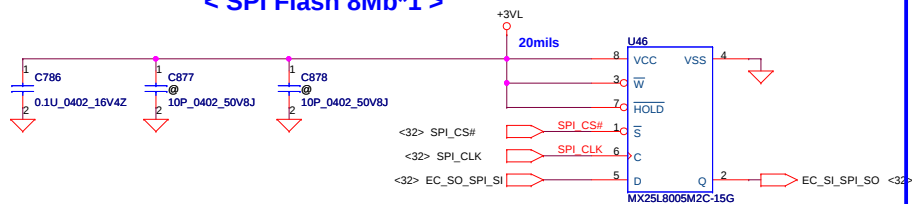
< HeadPhone JACK >



< Ext.MIC/LINE IN JACK >

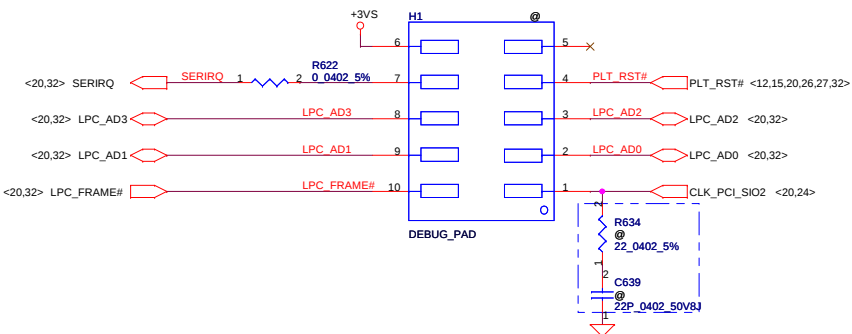


< SPI Flash 8Mb*1 >

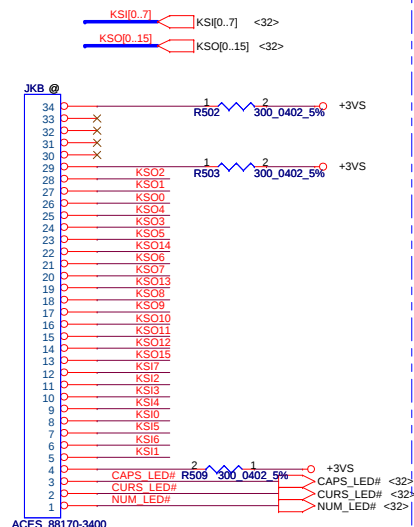


< LPC Debug Port >

Please place the PAD under DDR DIMM.



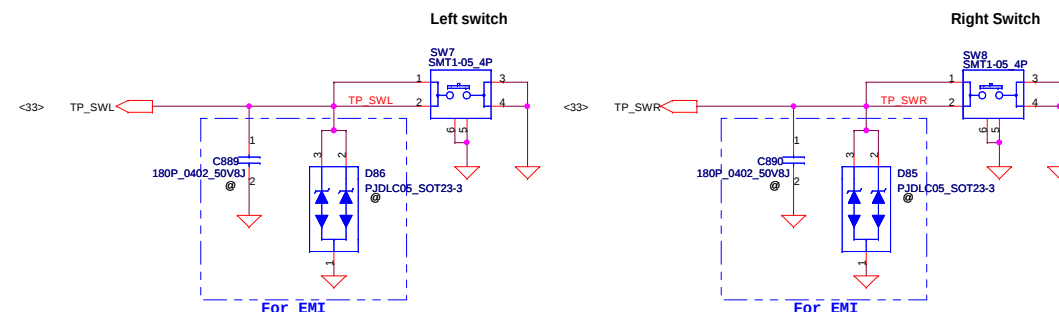
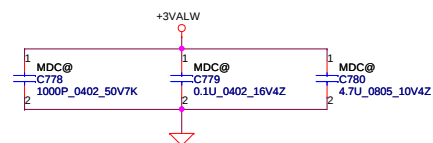
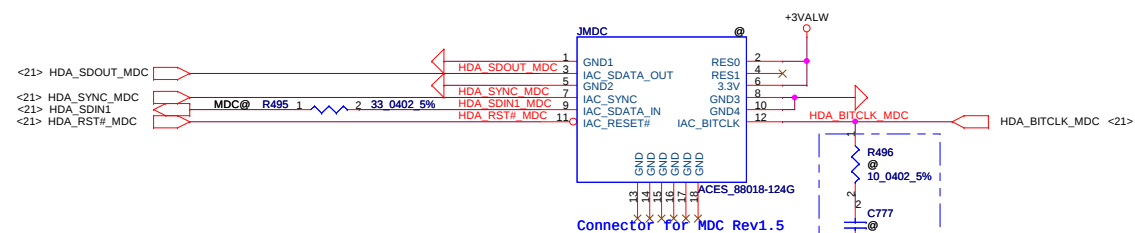
KEYBOARD CONN.



For EMI

<u>KS02</u>	1	2
<u>KS01</u>	C725	100P_0402_50VB3
<u>KS00</u>	C717	100P_0402_50VB3
<u>KS04</u>	C721	2
		100P_0402_50VB3
<u>KS03</u>	C609	2
		100P_0402_50VB3
<u>KS05</u>	C724	2
		100P_0402_50VB3
<u>KS014</u>	C728	2
		100P_0402_50VB3
<u>KS06</u>	C730	2
		100P_0402_50VB3
<u>KS07</u>	C715	2
		100P_0402_50VB3
<u>KS013</u>	C732	2
		100P_0402_50VB3
<u>KS08</u>	C733	2
		100P_0402_50VB3
<u>KS09</u>	C740	2
		100P_0402_50VB3
<u>KS010</u>	C737	2
		100P_0402_50VB3
<u>KS011</u>	C729	2
		100P_0402_50VB3
<u>KS012</u>	C738	2
		100P_0402_50VB3
<u>KS015</u>	C718	2
		100P_0402_50VB3
<u>KS17</u>	C736	2
		100P_0402_50VB3
<u>KS12</u>	C716	2
		100P_0402_50VB3
<u>KS13</u>	C741	2
		100P_0402_50VB3
<u>KS14</u>	C726	2
		100P_0402_50VB3
<u>KS10</u>	C723	2
		100P_0402_50VB3
<u>KS15</u>	C731	2
		100P_0402_50VB3
<u>KS16</u>	C739	2
		100P_0402_50VB3
<u>KS11</u>	C735	2
		100P_0402_50VB3
<u>CAPS_LED#</u>	C734	2
		100P_0402_50VB3
<u>CURS_LED#</u>	C722	2
		100P_0402_50VB3
<u>NUM_LED#</u>	C727	2
		100P_0402_50VB3
	C714	2
		100P_0402_50VB3

< MDC 1.5 Conn >



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Date:				Wednesday, August 12, 2009	Sheet 31 of 44

20 mil width

ACES_85201-06051

For EMI

Diagram illustrating the connection of the HT-210UD/YUG_AMBI/GRN LED. The LED is connected to a +3VALVIO input through a resistor R549 (120_0402_5%). The LED is labeled "Ultra Bright Yellow Green". The output is connected to BATT_FULL_LED# <32> and BATT_CHG_LOW_LED# <32>.

HT-210UD/YUG_AMBI/GRN

< Ultra Bright Yellow Green >

3 — BATT_FULL_LED# <32>

2 — BATT_CHG_LOW_LED# <32>

Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

WLAN LED Vf=1.9V(typ), 2.4V(max)

+3VS 1 2 R550 120_0402 5% 2 1 D50 HT-110UD 1204 AMBER WL_LED# <32>

HDD LED

HDD LED

+3V5

R548 120_0402_5%

D46 HT-110UYG-CT_YEL/GRN

+3V5

R546 10K_0402_5%

Q18A 2N7002DW-T/R7_SOT363-6

Q18B 2N7002DW-T/R7_SOT363-6

SATA_LED# <22>

Vf=1.9V (typ) , 2.4V (max)

< Ultra Bright Yellow Green >

D49

+3VALW — 1 — R521 120_0402_5% — 2 —

1 — 3 — PWR_ON_LED# <32>

2 — PWR_SUSP_LED# <32>

HT-2100D/UYG_AMB/GRN

< Ultra Bright Amber >

$V_f = 1.9V(\text{typ}), 2.4V(\text{max})$ for amber
 $V_f = 2.0V(\text{typ}), 2.4V(\text{max})$ for green
 $I_f = 30\text{mA}(\text{max})$

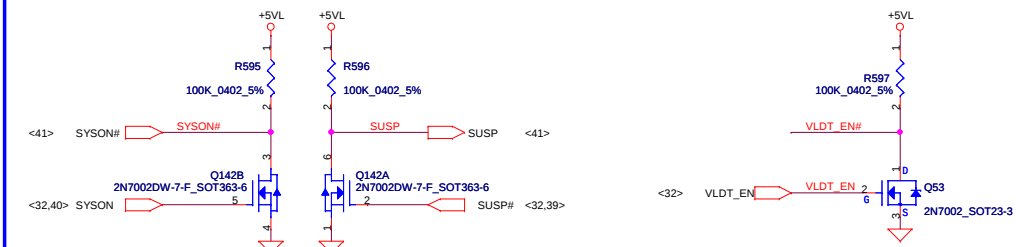
For EMI

Diagram illustrating EMI mitigation for a 5V power rail. The signal path is shown with a 5VSWO input connected to a common ground plane. The output path is connected to a 2.2uF capacitor and a 0.063uF capacitor, both connected to ground. The diagram shows five parallel traces (C199, C200, C201, C202, C203) connecting the 5VSWO signal to the capacitors, indicating a multi-layer PCB design for EMI reduction.

1. **CPU** INS87990490422 H19 H21

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				LA-5831P	1.0
				Date: Wednesday, August 12, 2009	Sheet 33 of 44

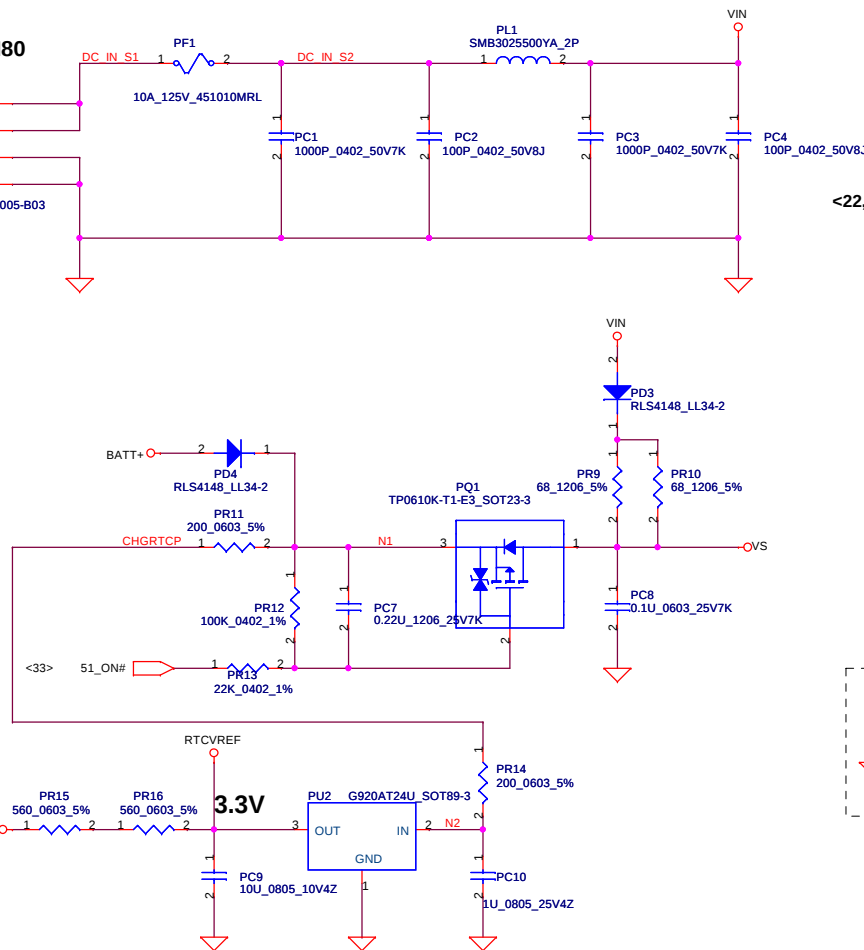
< close to PQ20, must EMI confirm > < +1.8V TO +1.8VS >



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DC / DC Circuits						
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						Document Number
				1.0		
		Date:		Wednesday, August 12, 2009		
		Sheet		34 of 44		

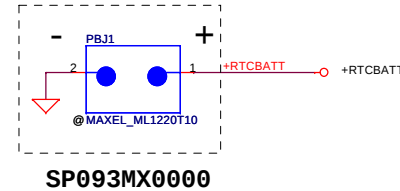
DC301001M80

@ SINGA_2DW-0005-B03



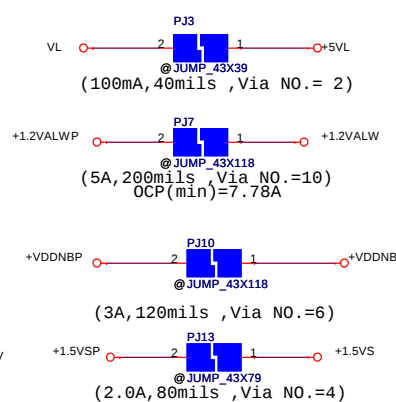
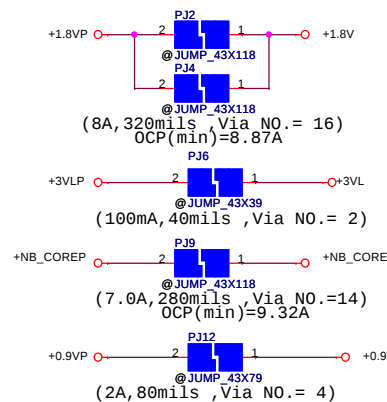
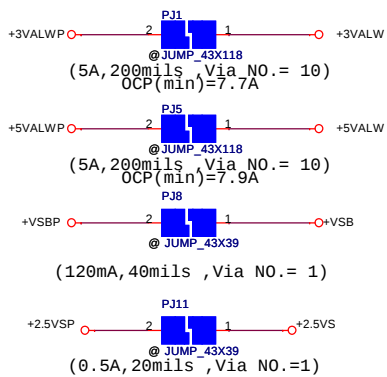
<22,32,33> ACIN

RTC Battery

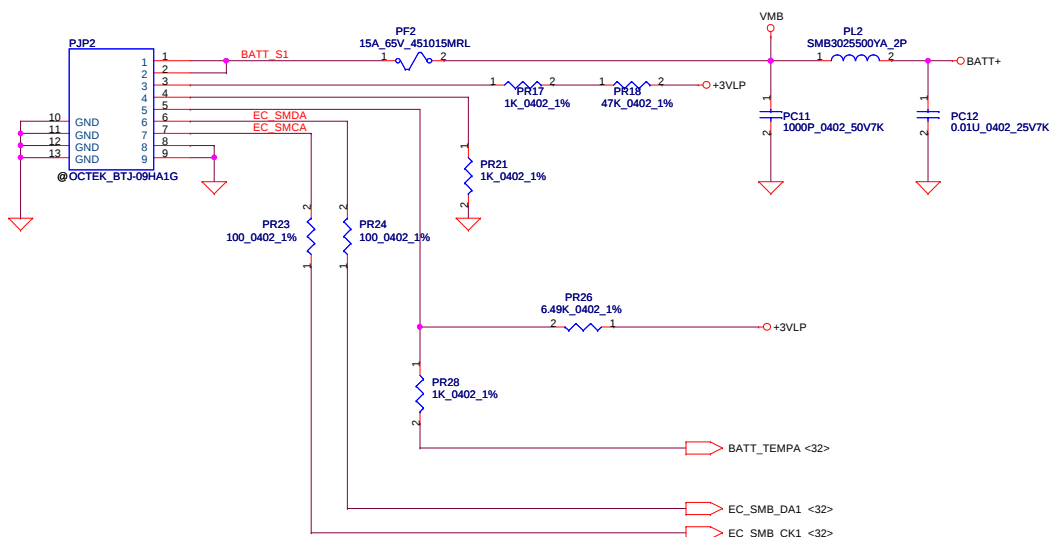


Vin Detector

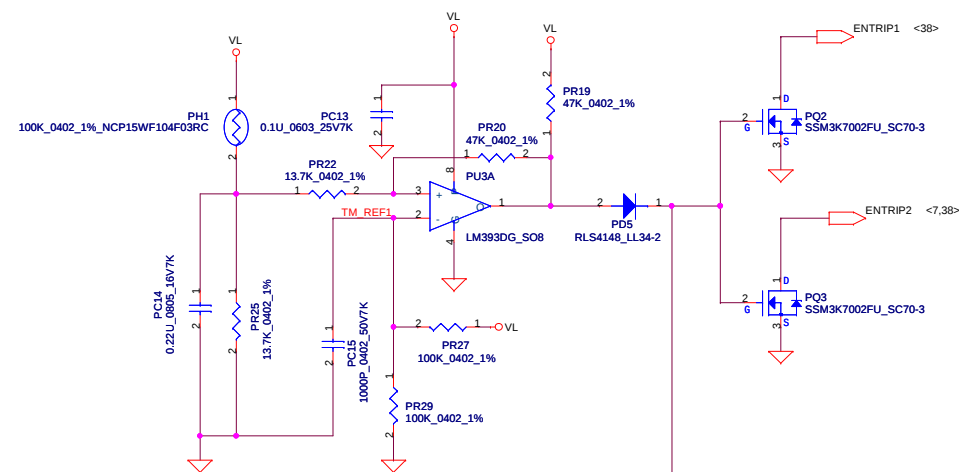
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



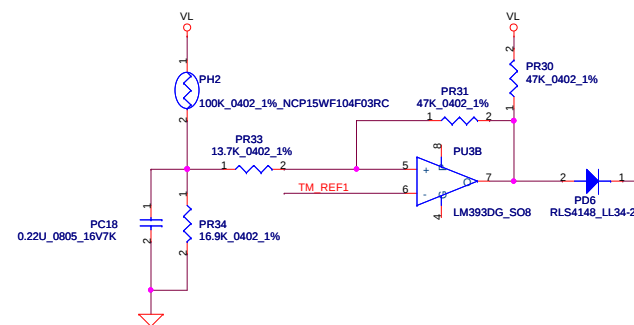
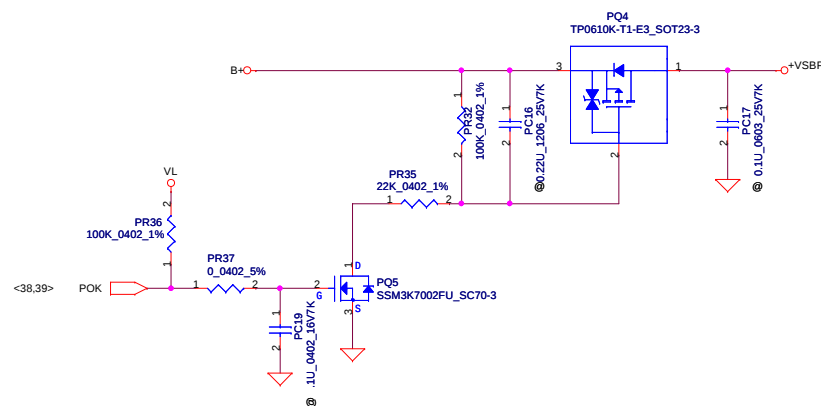
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				Date:	Wednesday, August 12, 2009	Sheet 35 of 44



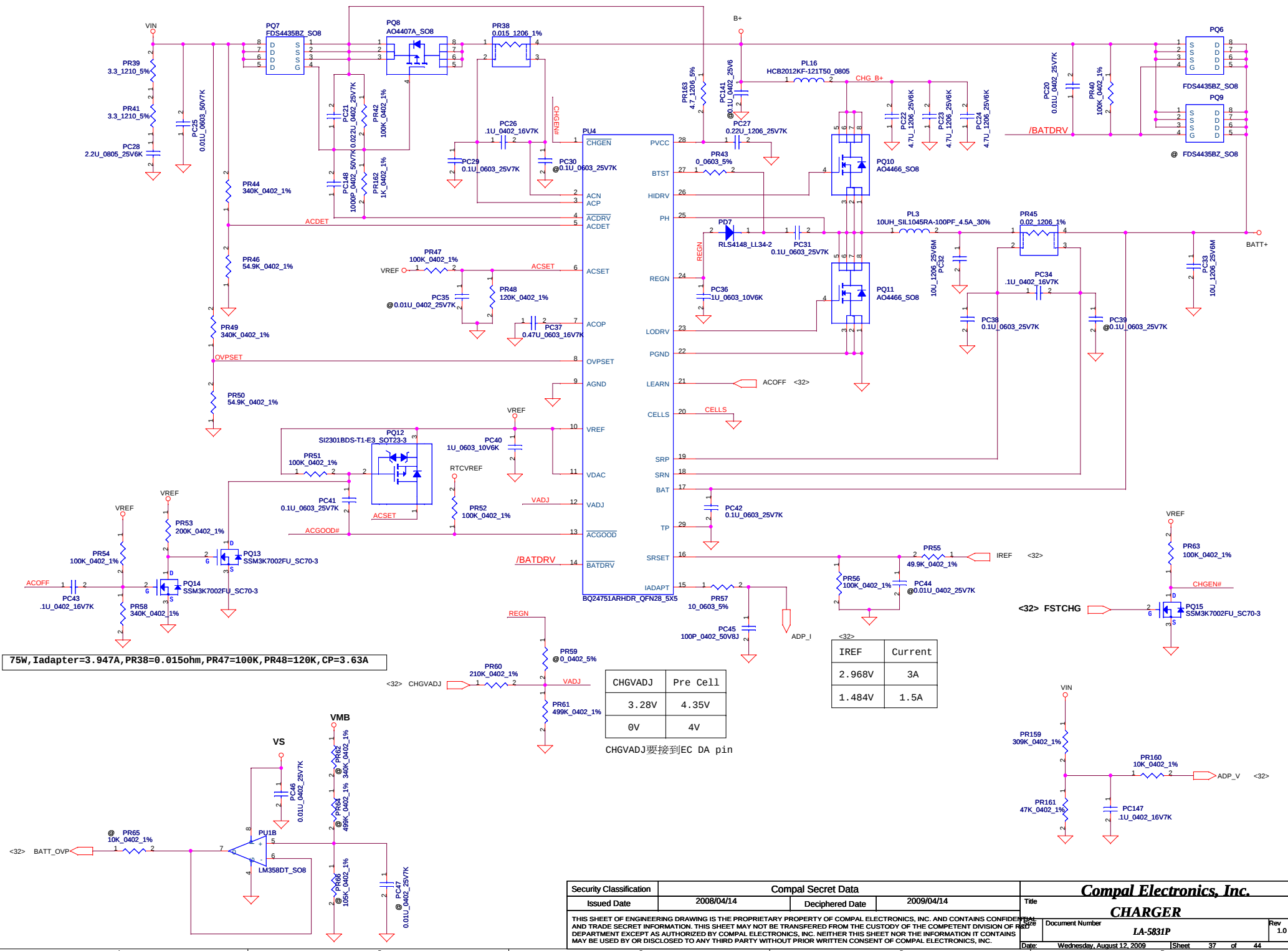
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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			Date: Wednesday, August 12, 2009	Sheet 36 of 44



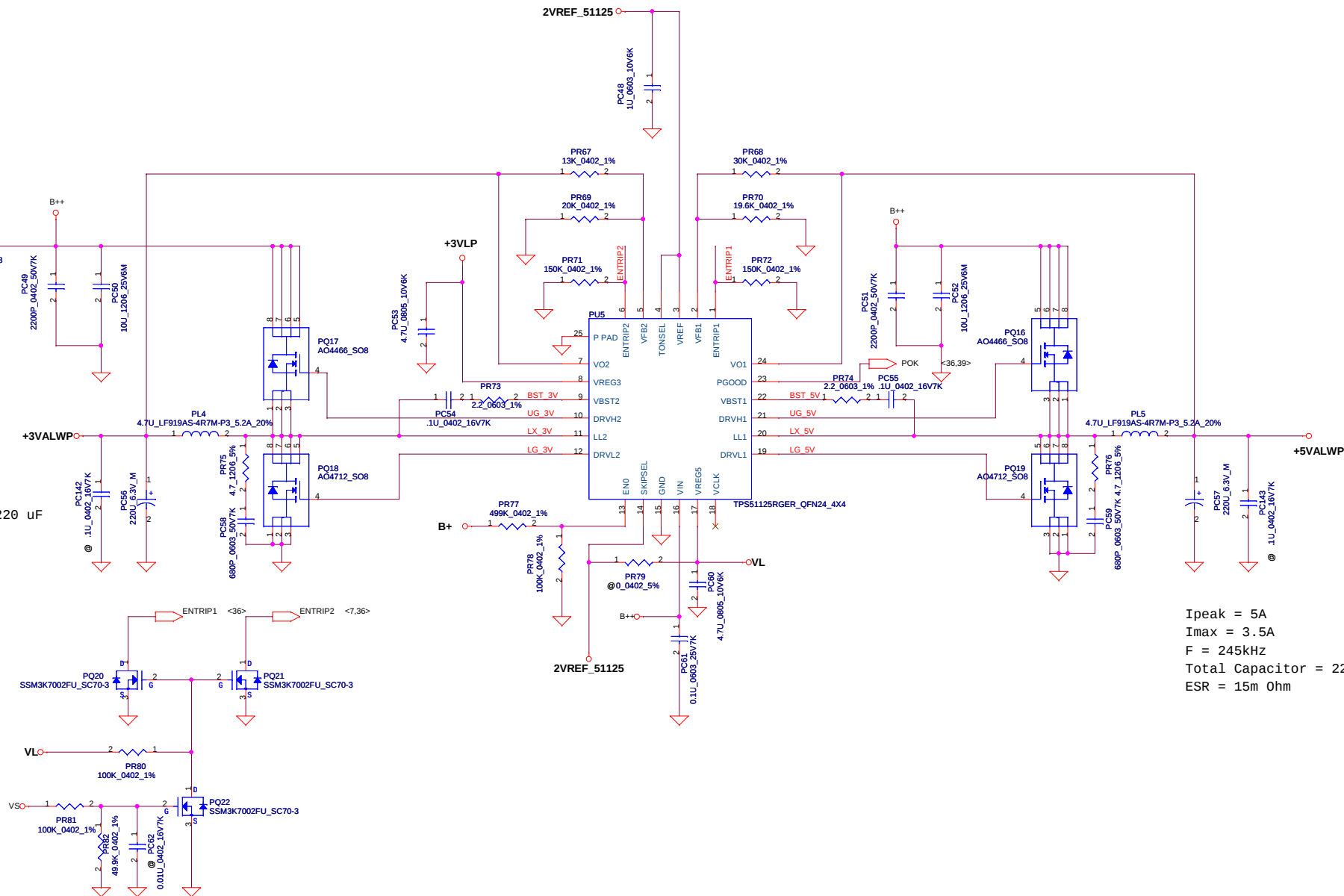
75W, Iadapter=3.947A, PR38=0.015ohm, PR47=100K, PR48=120K, CP=3.63A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

CHGVADJ要接到EC DA pin

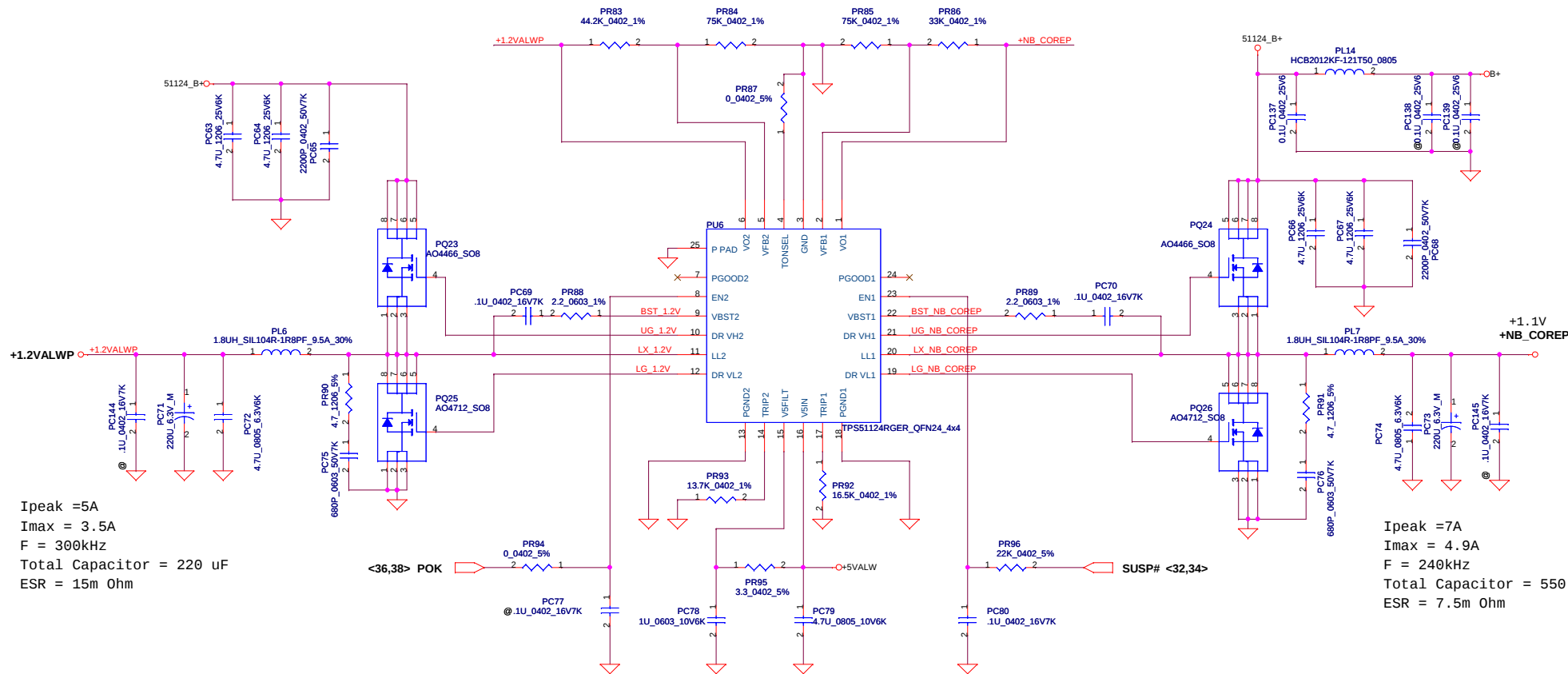
IREF	Current
2.968V	3A
1.484V	1.5A

Ipeak = 5A
Imax = 3.5A
F = 305kHz
Total Capacitor = 220 uF
ESR = 15m Ohm



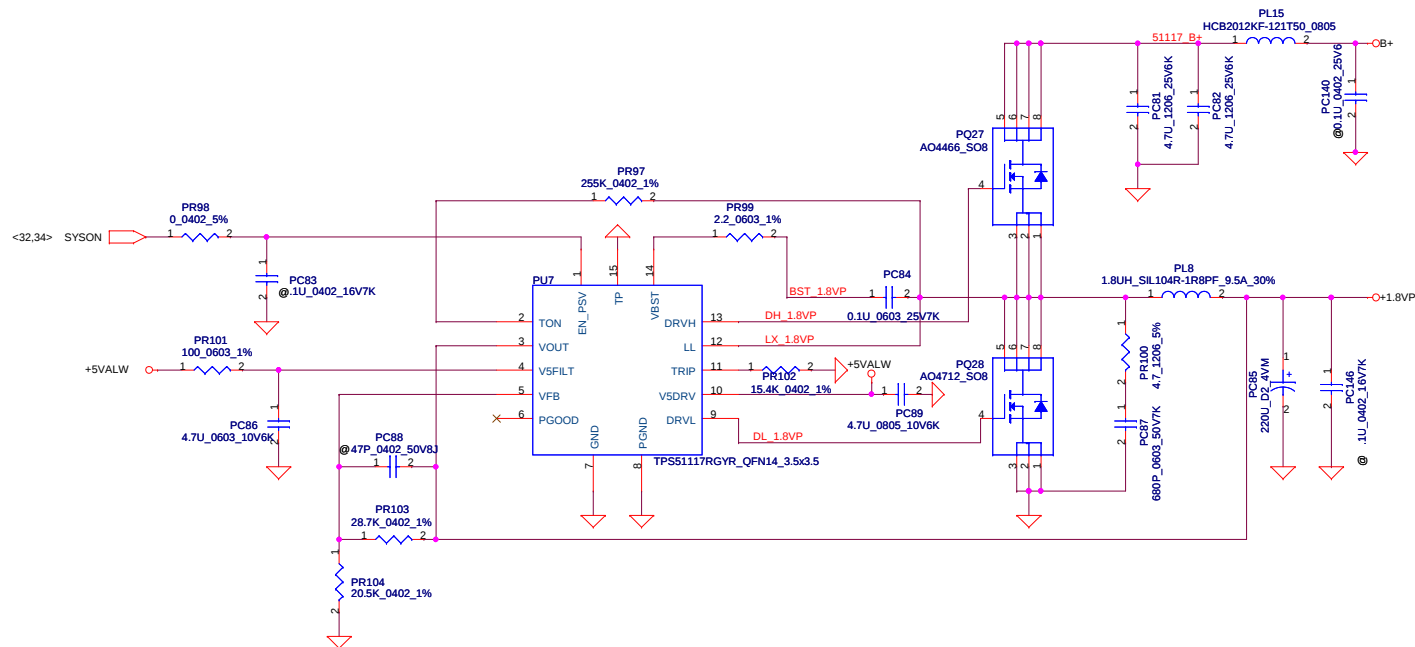
Ipeak = 5A
Imax = 3.5A
F = 245kHz
Total Capacitor = 220 uF
ESR = 15m Ohm

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			Date: Wednesday, August 12, 2009	Sheet 38 of 44

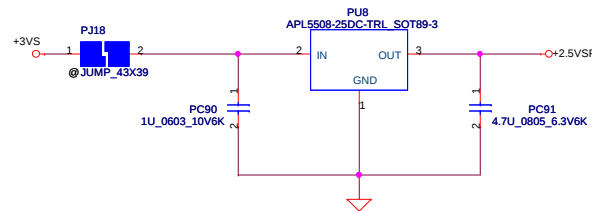


Ipeak = 7A
 Imax = 4.9A
 F = 240kHz
 Total Capacitor = 550 uF
 ESR = 7.5m Ohm

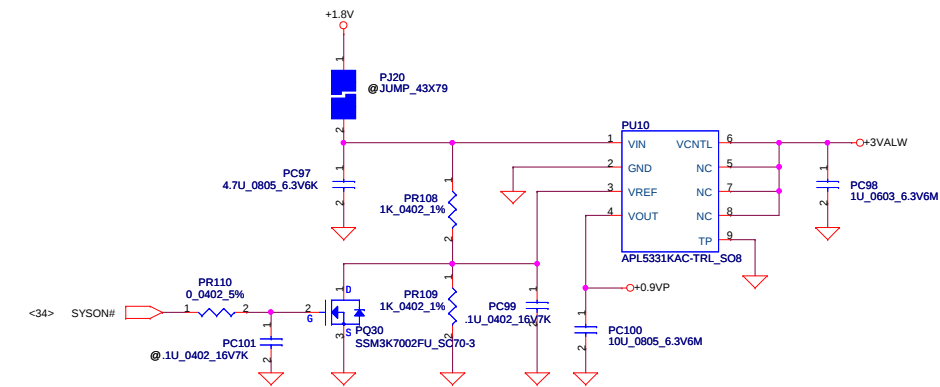
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Date: Wednesday, August 12, 2009				Sheet	39 of 44



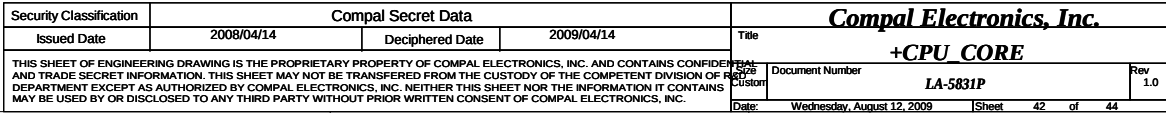
$I_{peak} = 8A$
 $I_{max} = 5.6A$
 $F = 312kHz$
 Total Capacitor = 220 μF
 ESR = 15m Ohm



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Version Change List (P. I. R, List) for Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
35-43	PVT		2009/07/20	Release			
39-40	Pre-MP	Change PL6,PL7,PL8	2009/07/30	POWER		Change PL6,PL7,PL8 footprint	
38	Pre-MP	Change PC56	2009/07/30	POWER		change to common circuit.	
36	Pre-MP	Change PH1,PH2	2009/08/4	POWER		change to common circuit.	
37	Pre-MP	Change PR38,PR45	2009/08/4	POWER		change to common circuit.	

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HW4 Product Improvement Record (P.I.R.)

NBWA E LA-5831P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0
GERBER-OUT DATE: 2009/08/07

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/21	25	Change JUSBB footprint back to E-T_6905-E12N-00R_12P	USB/B pin define reverse
2	7/27	25	Add D11	For ESD
3	7/27	9	Add C120-C123	For EMI
4	7/27	32	Add R344 and R345	For EC pin damage issue
5	7/30	26	Add R97, R98 and R105	Reserve bead for EMI
6	8/6	18	Add C707, C708 and C709	For EMI
7	8/6	30	Add LA11 and LA12	For EMI
8	8/6	32	Add R74 and C607	For EMI
9	8/6	31	Delete R518 and C606	For EMI
10	8/6	7	Add C124	For EMI

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