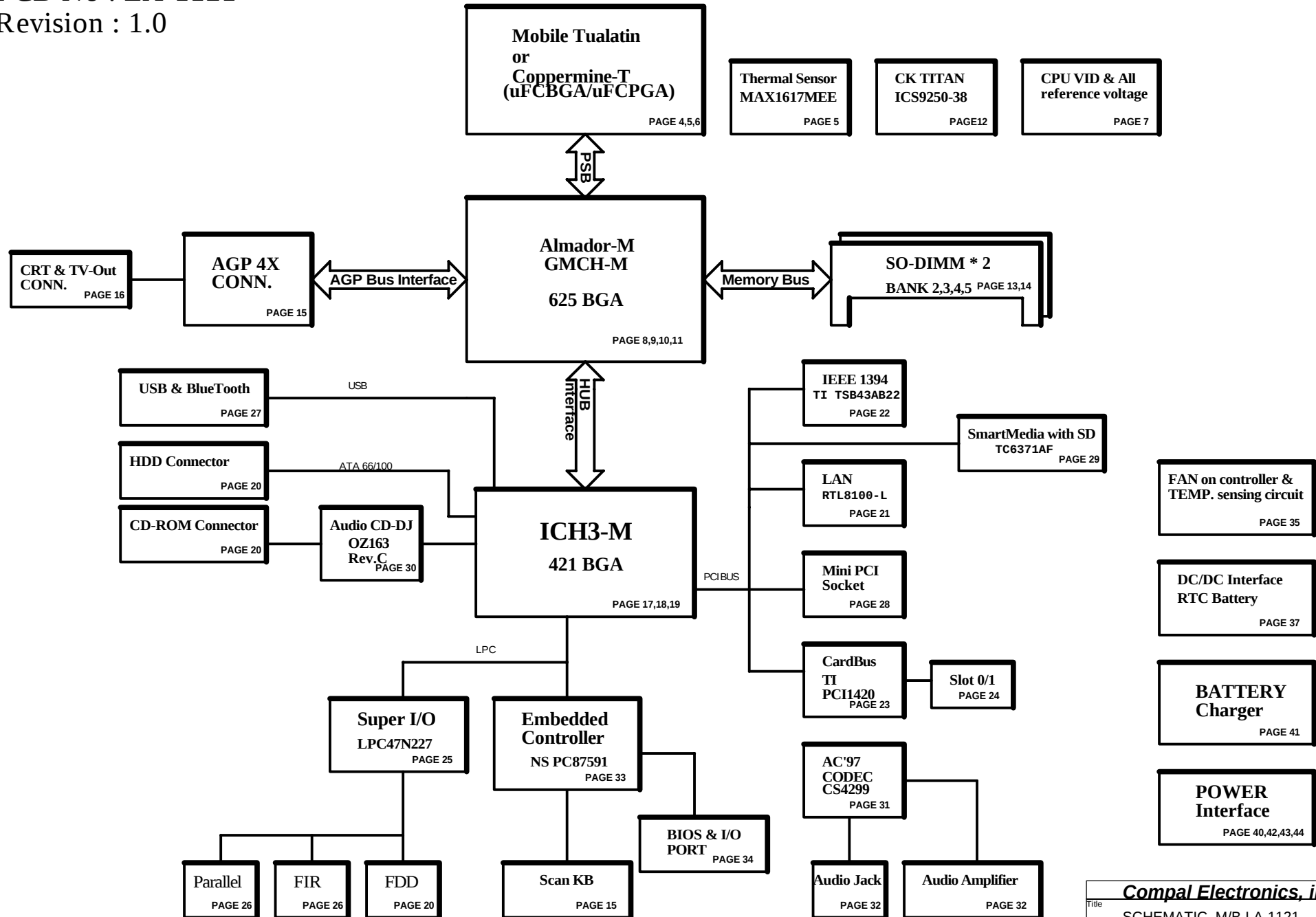


Model Name : 888M3
PCB No : LA-1121
Revision : 1.0

BLOCK DIAGRAM

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
AGP 4X CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM	AD22		PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ163	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

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PIR

REV 0.2

Date	Page	Description
5/8	29	Modification toshiba SM+SD function
5/8	32	Modification audio volume control function
5/8	42	ADD system thermal protection
5/14	33	DEL R244 ,Add D44

REV 0.3

Date	Page	Description
5/23	5	U8 Vcc plane modify to +5VALW
5/23	18	DEL R90,R89,R281
5/23	32	R448 change gnd to +5VCD, R479 change +5VCD to gnd.
5/23	37	U2.4 link to U20.8
5/23	30	Add R519.
5/23	5	U9.AF19 add R517 link to +1.5VS
5/23	25	Modify LPC_RST# timing. Add U55,D45,R518.
5/31	27	JP15.8 connector to U29.57
5/31	25	ADD R520, Add net name BT_DET# to U29.57
5/31	34	Modify net name ANT_SW to WL_OFF#, ADD R221
5/31	28	Modify net name RFOFF# to WL_OFF#
5/31	35	DEL R19

REV 0.4

Date	Page	Description
7/3	16	Del L23,R14,R12,R10,R6,R8
7/3	27	ADD C720,C721,C722,C723,C724,C725
7/3	29	IDSEL0 change to PCI_AD26, INTA#/INTB# change to PIRQC#/PIRQD#
7/10	24	Add U58,U59,R531,R532,R533,R534,C718,C719
7/17	29	Del SD function
7/18	29	Change IDSEL to PCI_AD22
7/23	21	DEL C15

REV 0.5

Date	Page	Description
8/13	15	Add R544 reserve for sus_stat# and stp_agg#
8/13	29	Add R545 pull-up signal SM_LED to SMC_VCC,Add@ in U62,C729,R486
8/13	35	Change R543 pull-up form SMC_VCC to +5VS
8/13	29	Add R546,R547 signal PCIRST#,CBRST#
8/13	37	Del U2,Q4,R330
8/16	10	Add Signal TV_out_DDC2CCLK,TV_out_DDC2DATA ,VCH_I2CCLK,VCH_I2CDATA,AGP_DDCCLK,AGP_DDCDATA
8/16	10	Add R551,R552. DEL R225,R235
8/16	15	Add RP38,RP39
8/16	16	Add R553,R554,R555
8/17	34	Del R29, Add R557, R558
8/17	20	Add R556

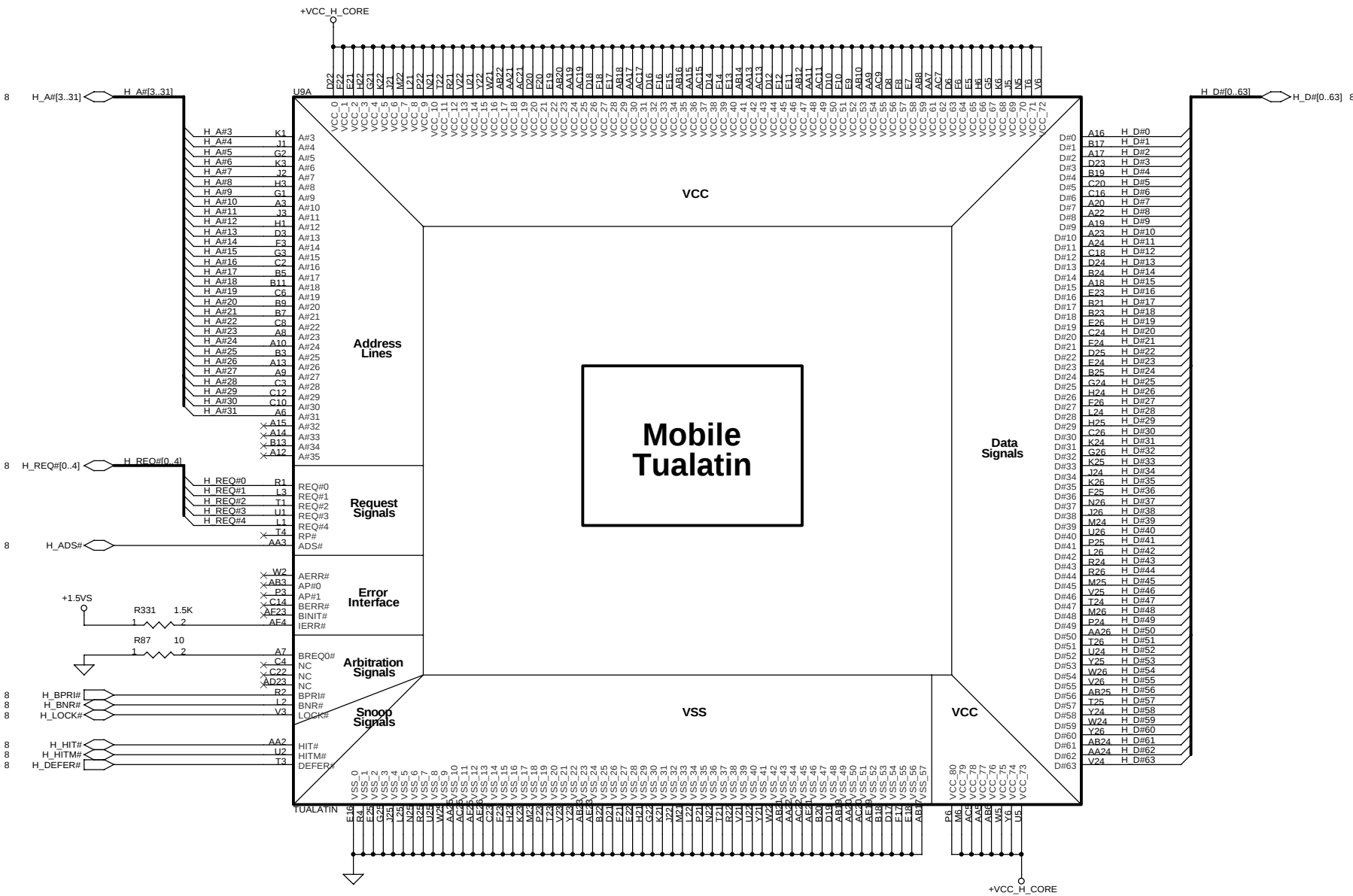
REV 1.0

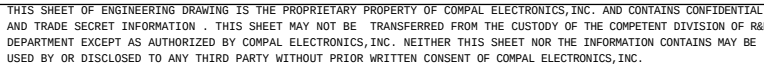
Date	Page	Description
8/31	5	Q6 RESERVE

REV 1.A

Date	Page	Description
9/6	12	Add D47 and R562

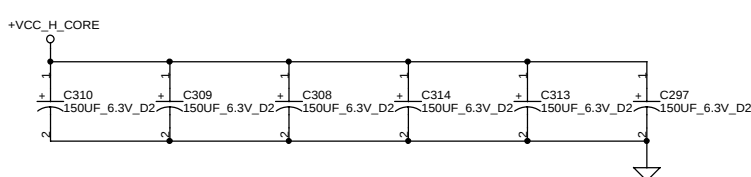
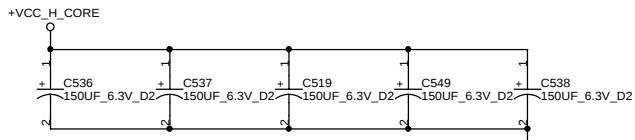
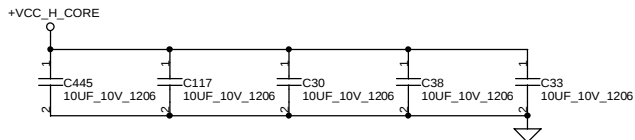
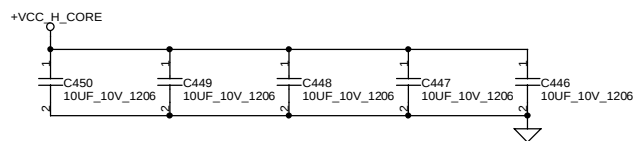
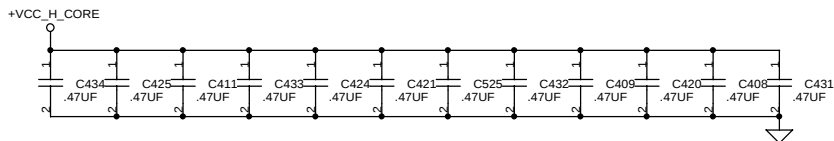
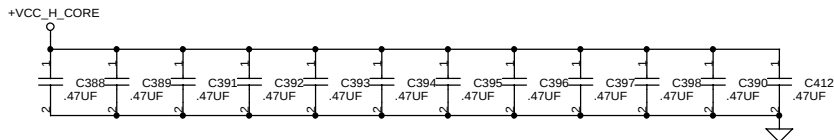
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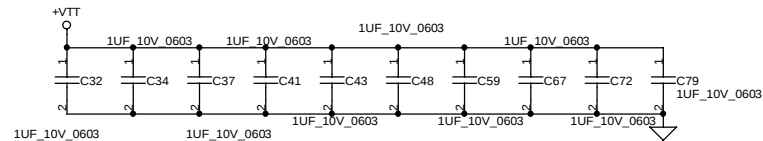
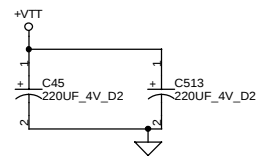
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.



Layout note :

Place close to CPU,
Use 2 vias per PAD.

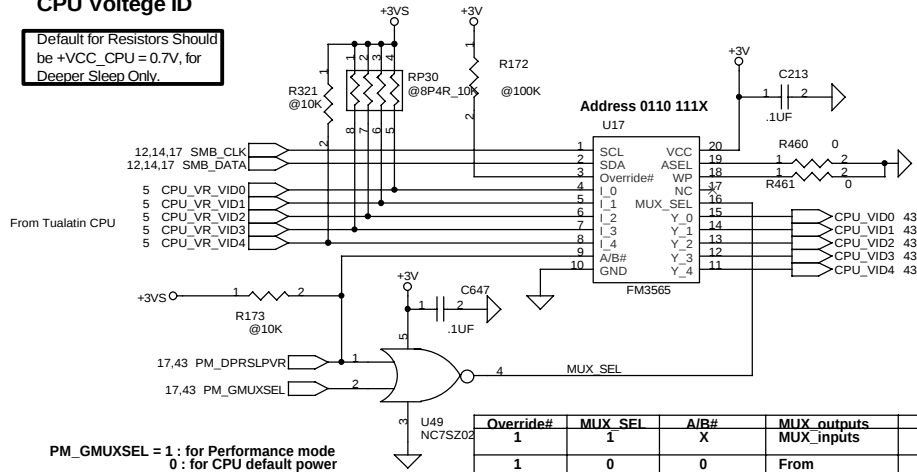


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CPU Voltage ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1 : for Deeper Sleep mode
0 : for Performance mode

Override#	MUX_SEL	A/B#	MUX_outputs MUX_inputs	Mode
1	1	X		Battery
1	0	0	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

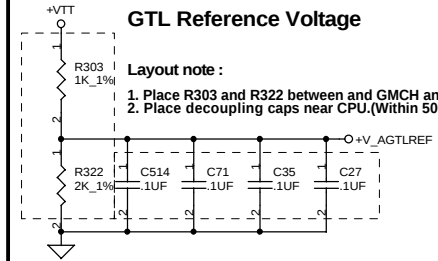
D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

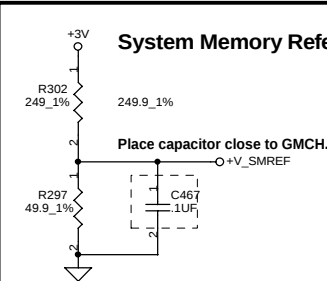
GTL Reference Voltage

Layout note :

1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)



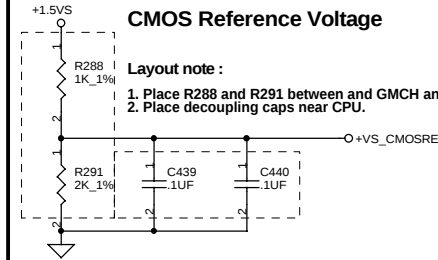
System Memory Reference



CMOS Reference Voltage

Layout note :

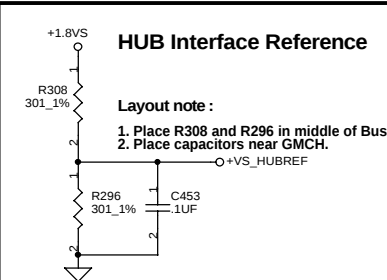
1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.



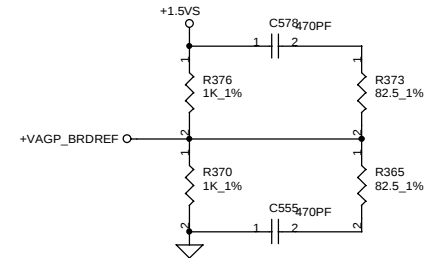
HUB Interface Reference

Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

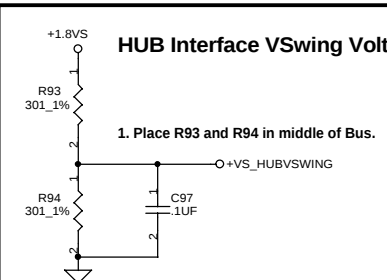


Place Reference Circuit near GMCH

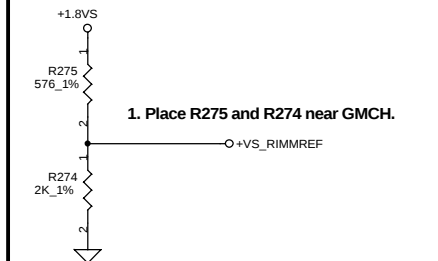


HUB Interface VSwing Voltage

1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.

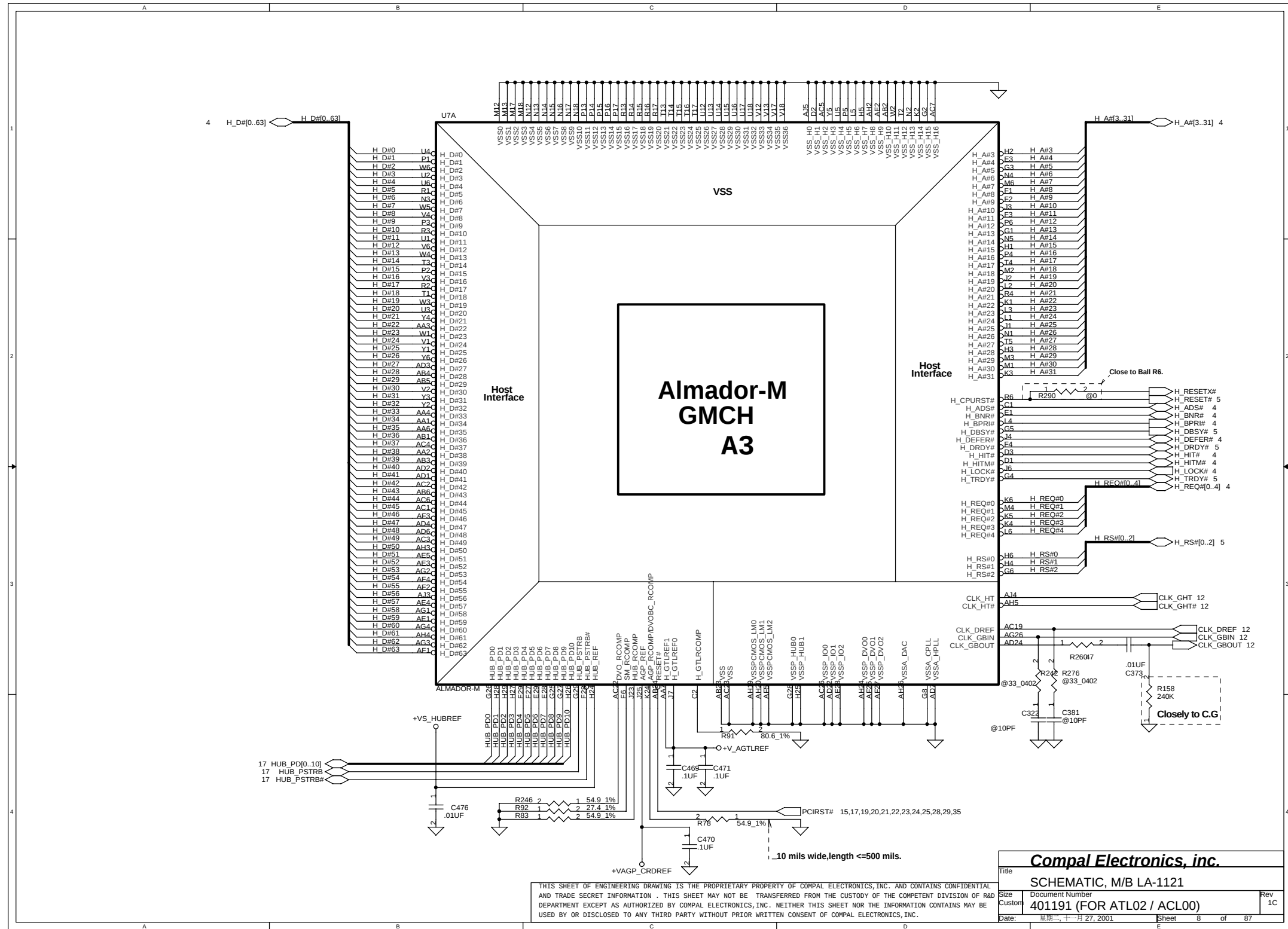


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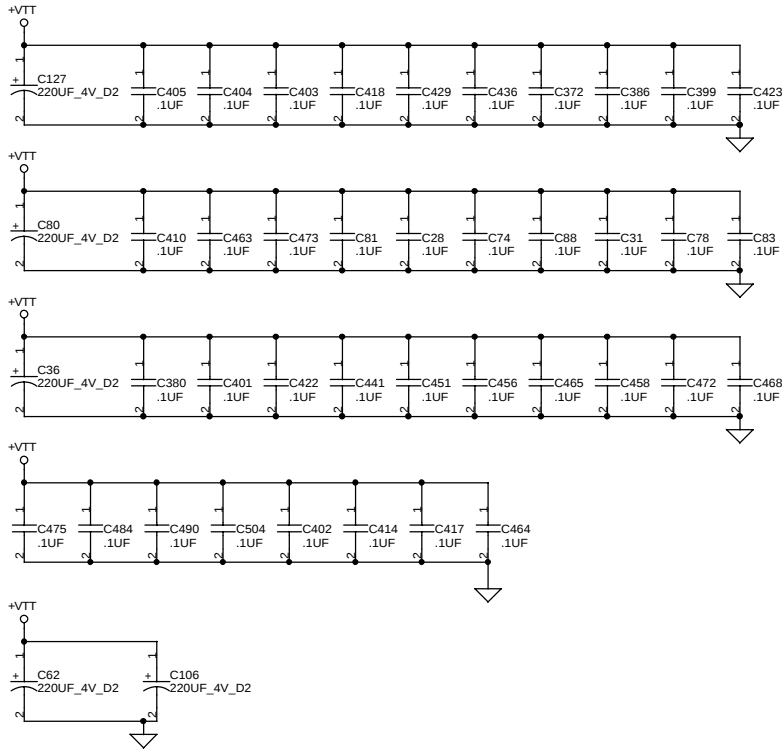
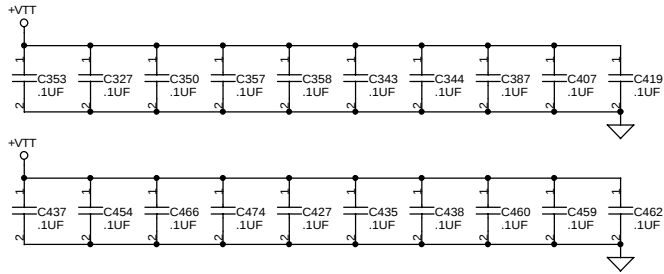
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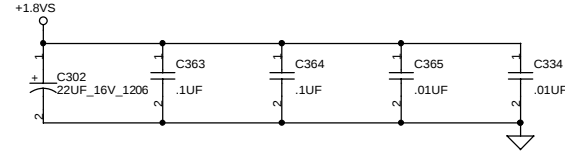
Layout note :

Distribute as close as possible
to GMCH Processor Quadrant .



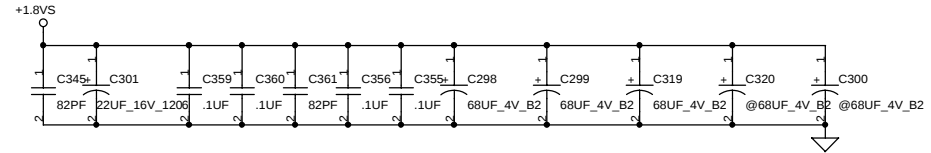
Layout note :

Distribute as close as possible
to VCCPCMOS_LM .



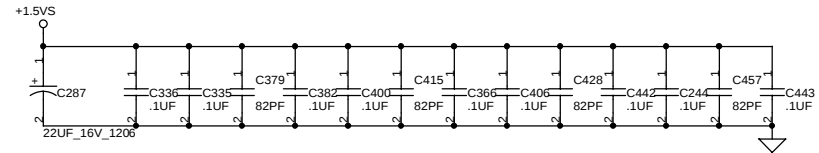
Layout note :

Distribute as close as possible
to GMCH Local Memory Quadrant .



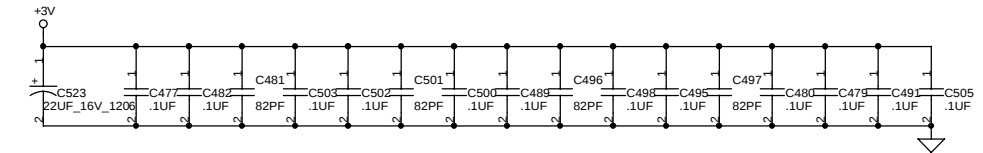
Layout note :

Distribute as close as possible
to GMCH AGP/DVO Quadrant .



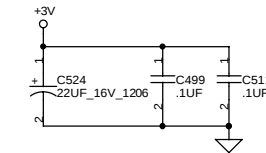
Layout note :

Distribute as close as possible
to GMCH System Memory Quadrant .



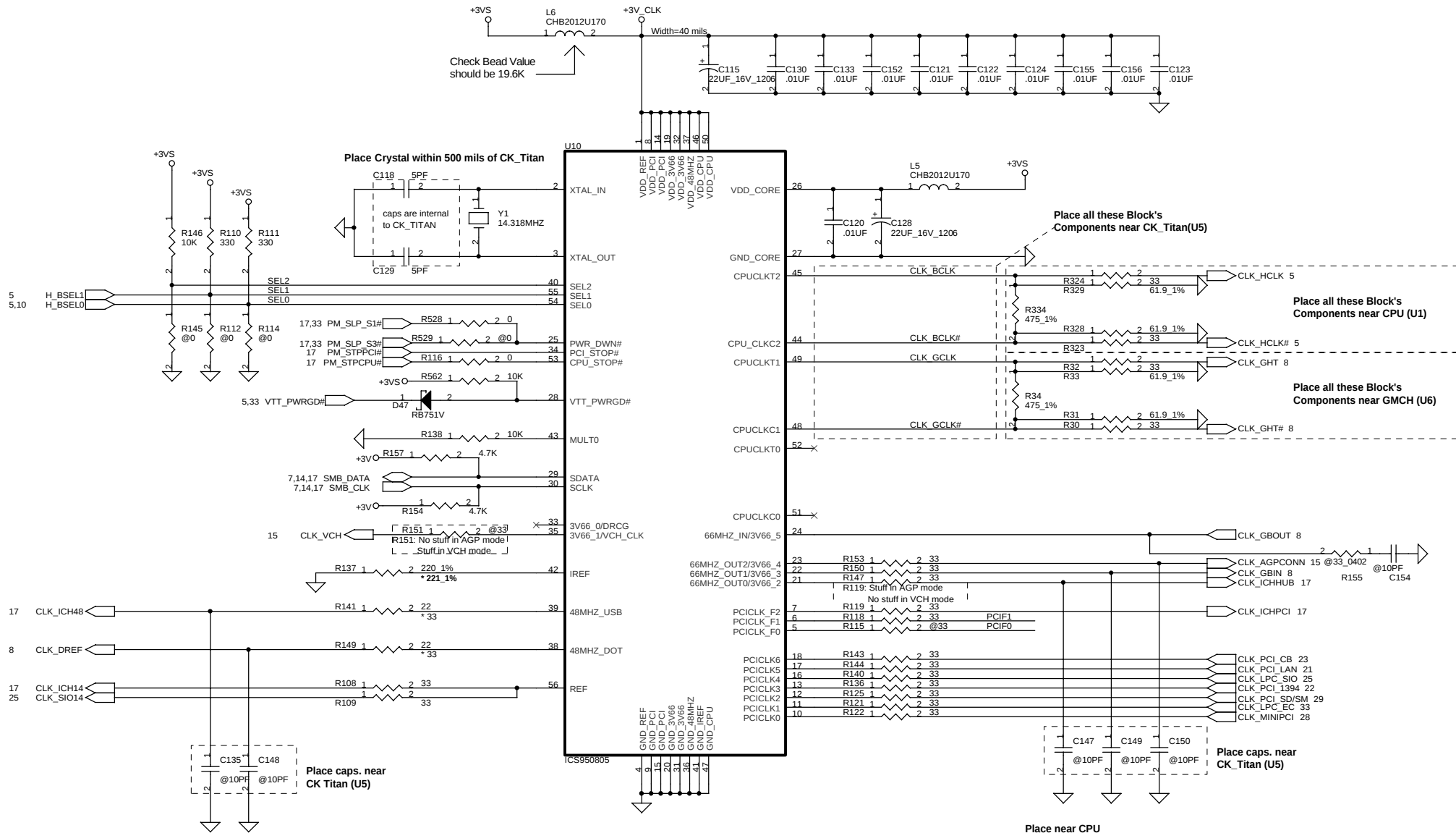
Layout note :

Distribute as close as possible
to IO Quadrant .



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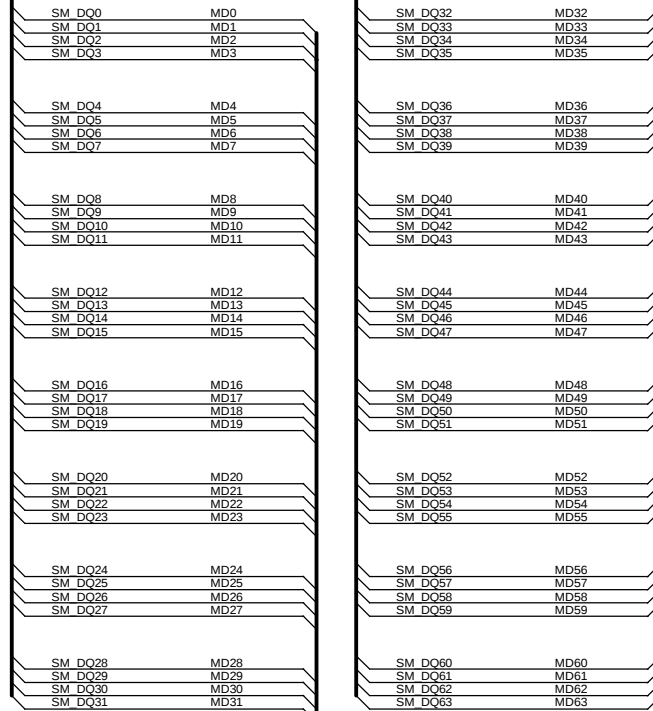


SEL2	SEL1	SEL0	CPUCLKC0[0..2]	CPUCLKT0[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

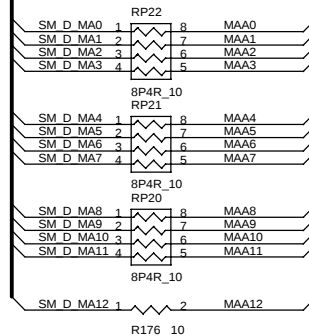
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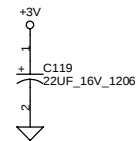
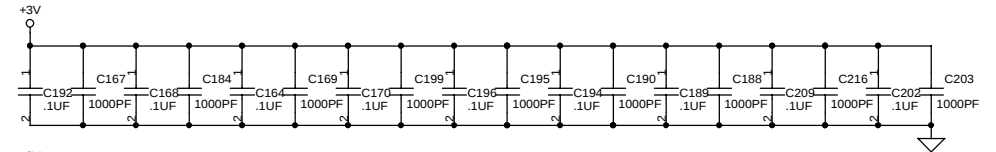
9,14 SM_DQ[0..63] MD[0..63] 9,14



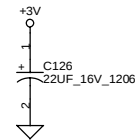
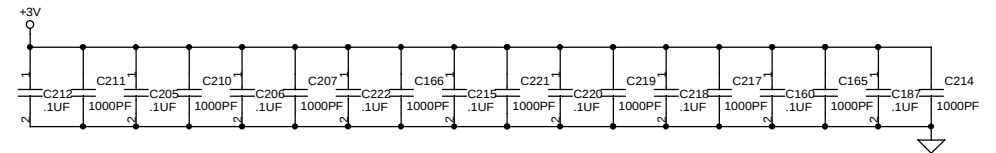
9 SM_D_MA[0..12] MAA[0..12] 14



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .



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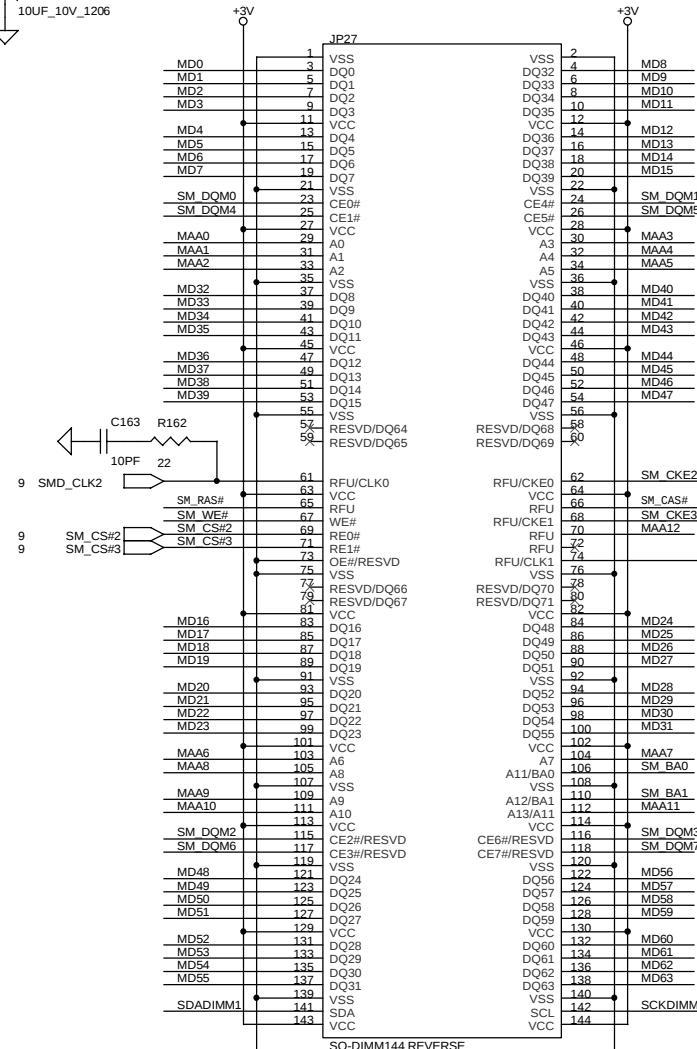
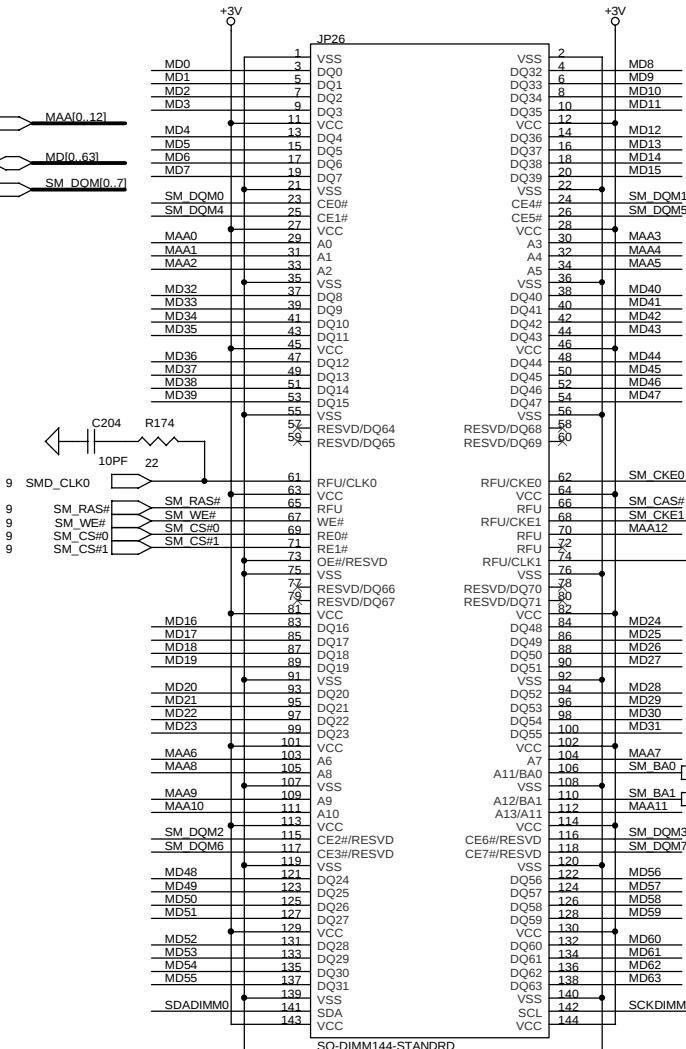
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SO-DIMM 144 PINS RAM MODULE CONN.

BANK 0/1

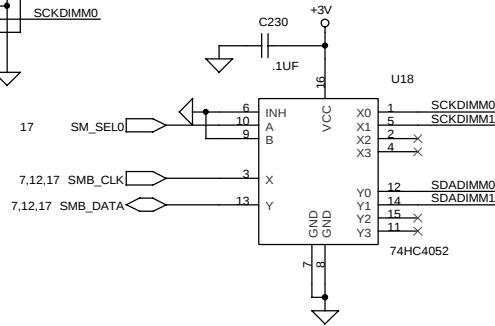
BANK 2/3

13 MAA[0..12] MAA[0..12]
9 MD[0..63] MD[0..63]
9 SM_DQM[0..7] SM_DQM[0..7]



DIMM0

DIMM1



SM_SEL0	X/Y
0	SCKDIMM0
1	SCKDIMM1

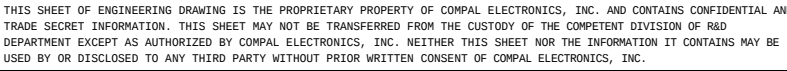
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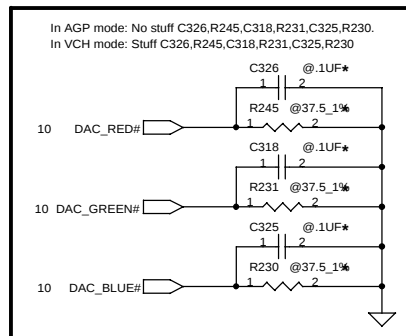
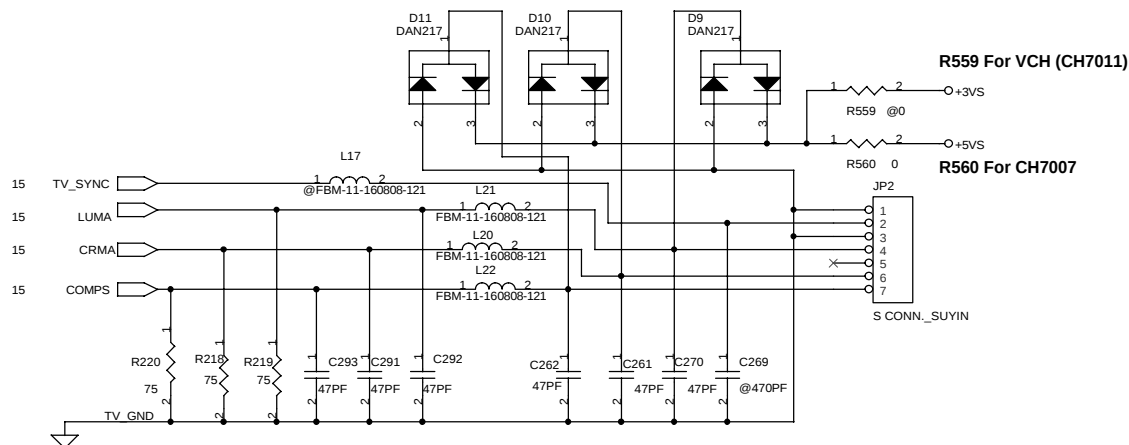
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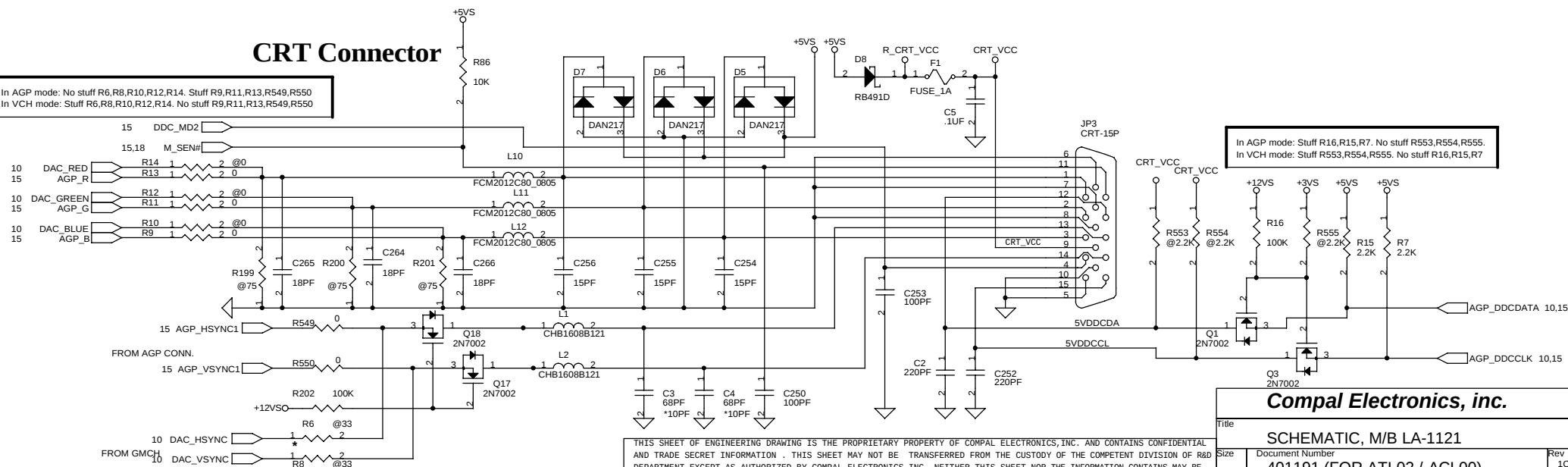


TV_OUT CONN.



CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550



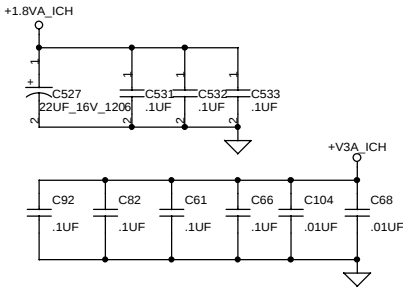
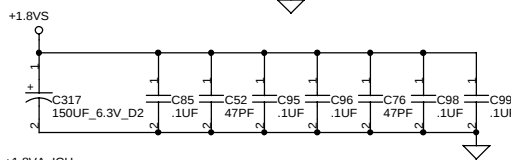
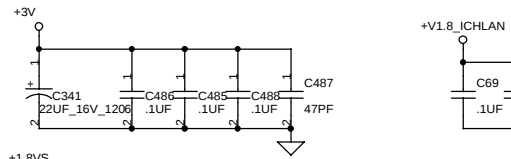
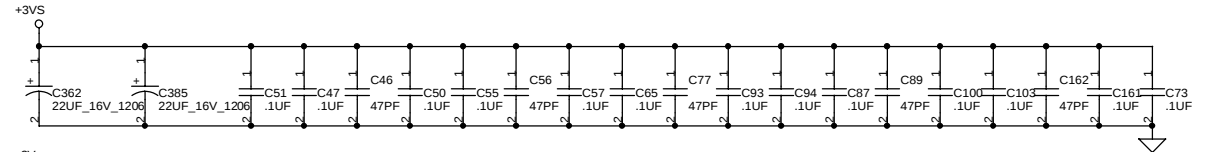
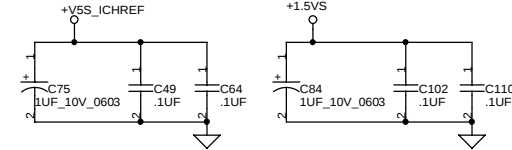
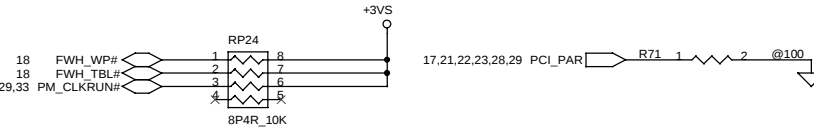
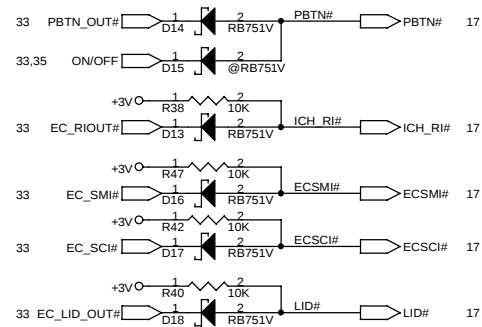
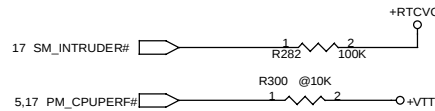
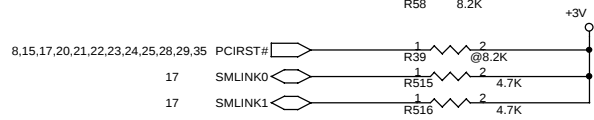
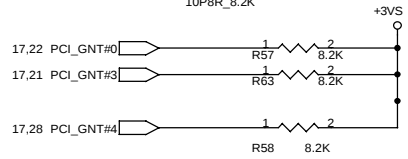
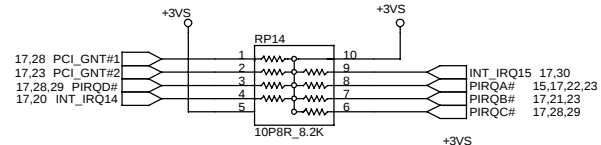
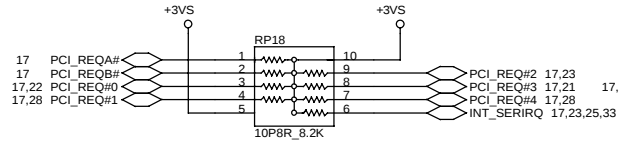
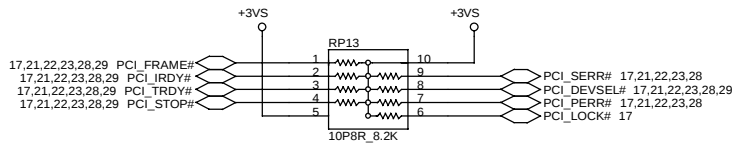
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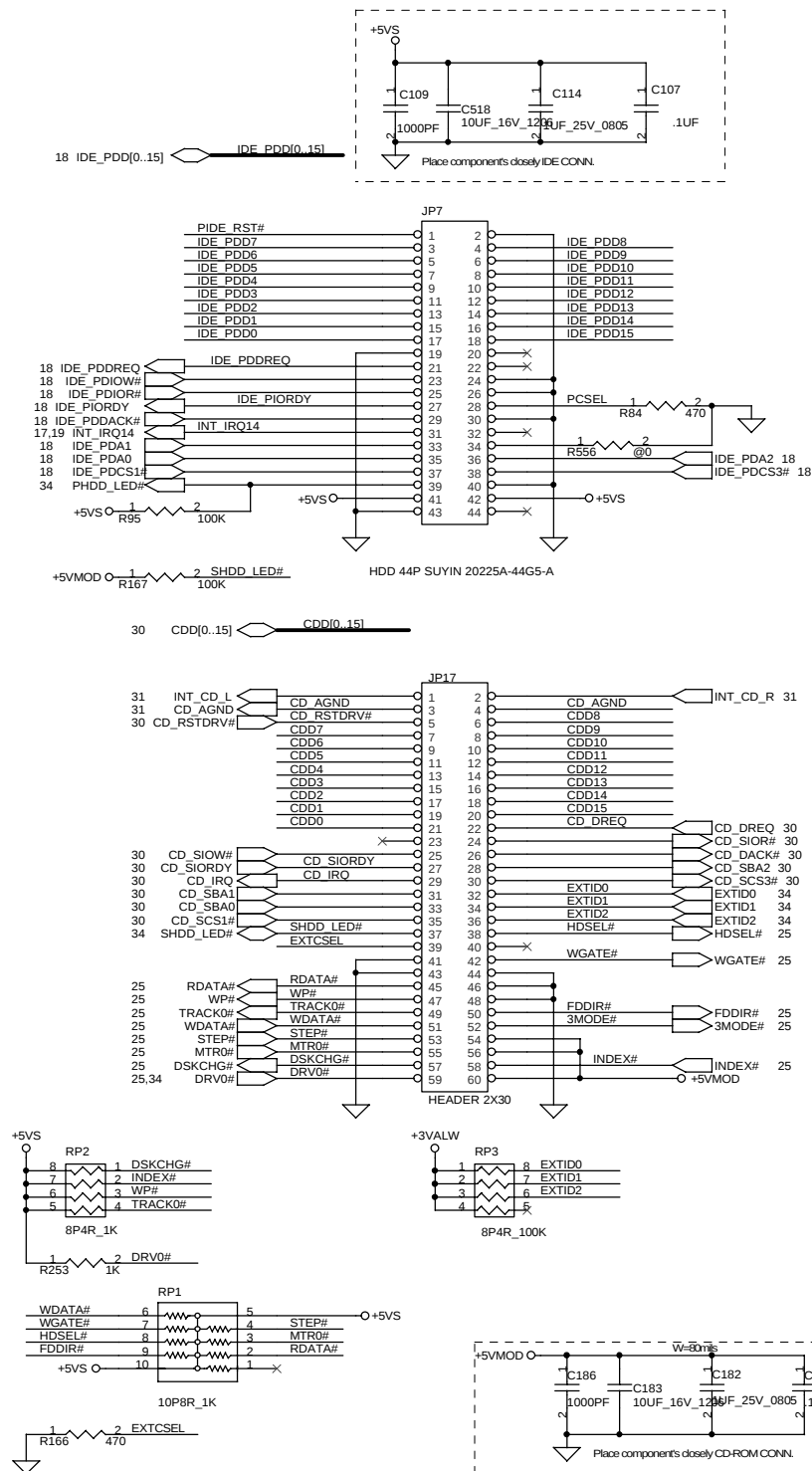
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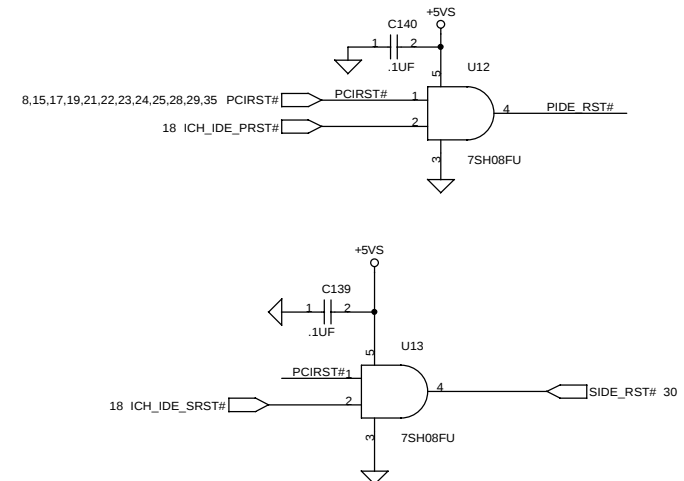
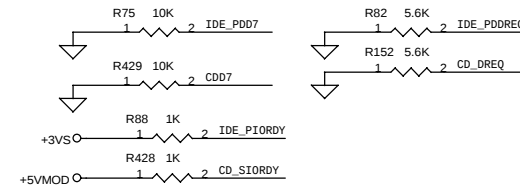
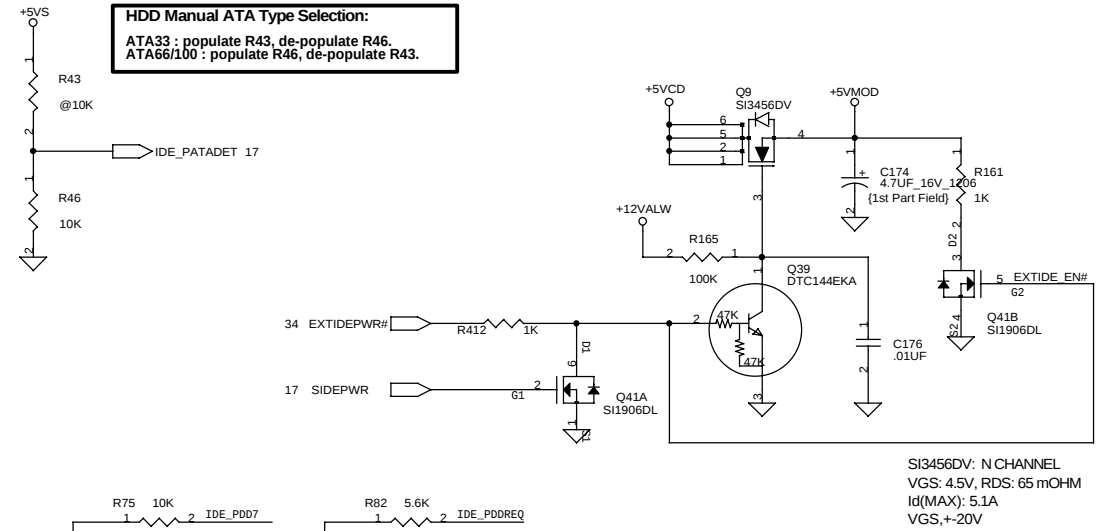
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IDE,CD-ROM Module CONN.



HDD Manual ATA Type Selection:

ATA33 : populate R43, de-populate R46.
ATA66/100 : populate R46, de-populate R43.



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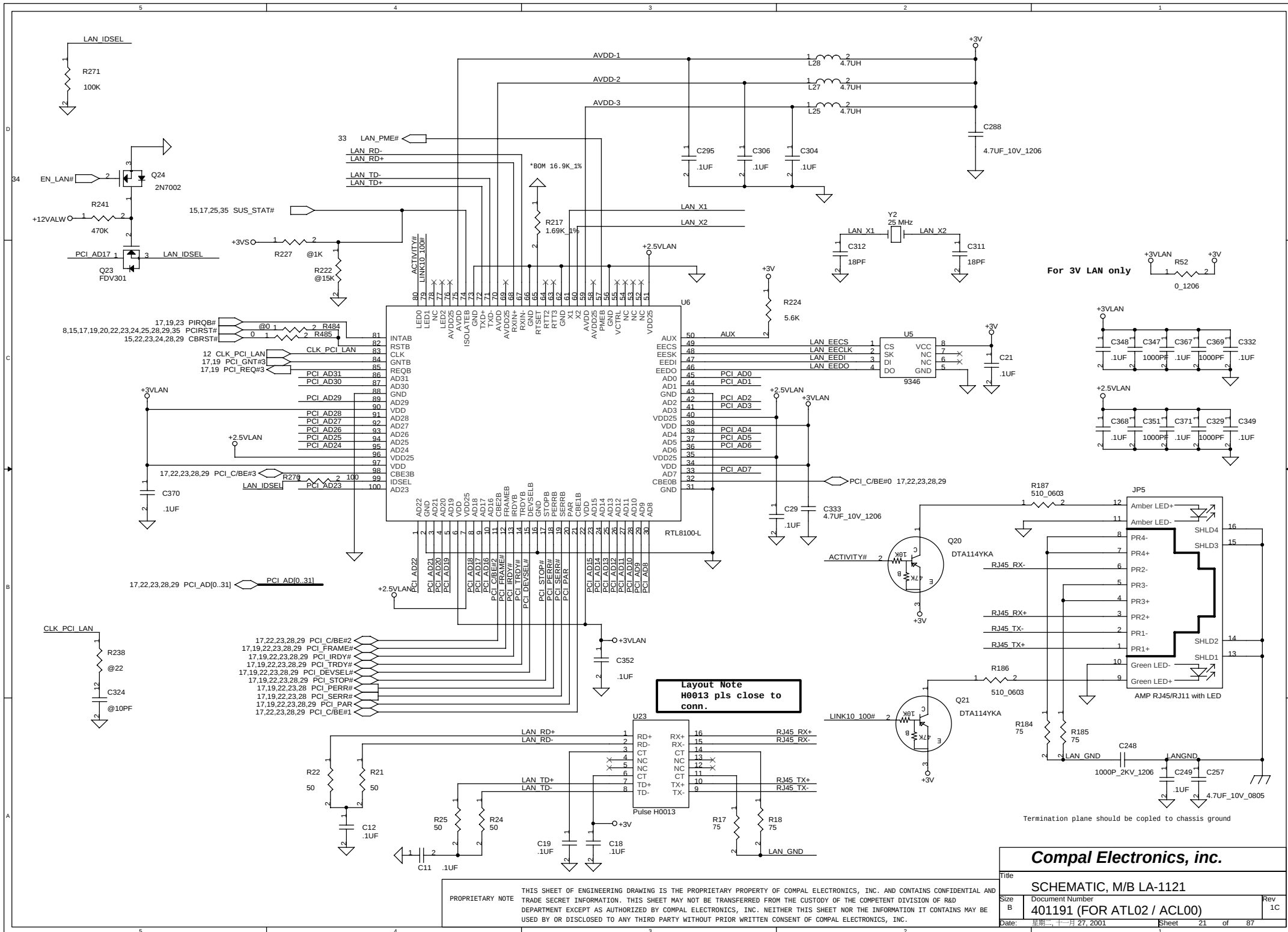
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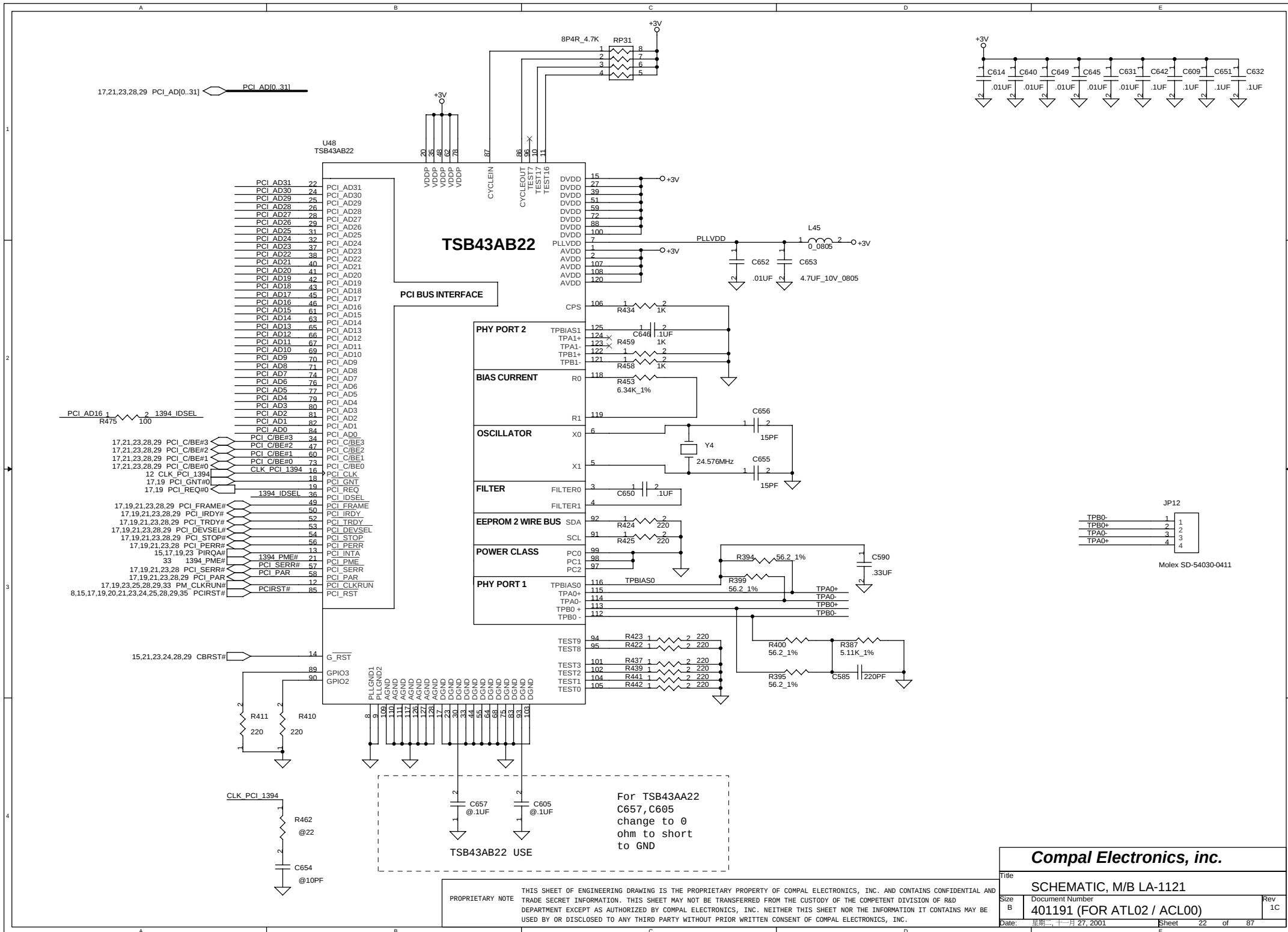
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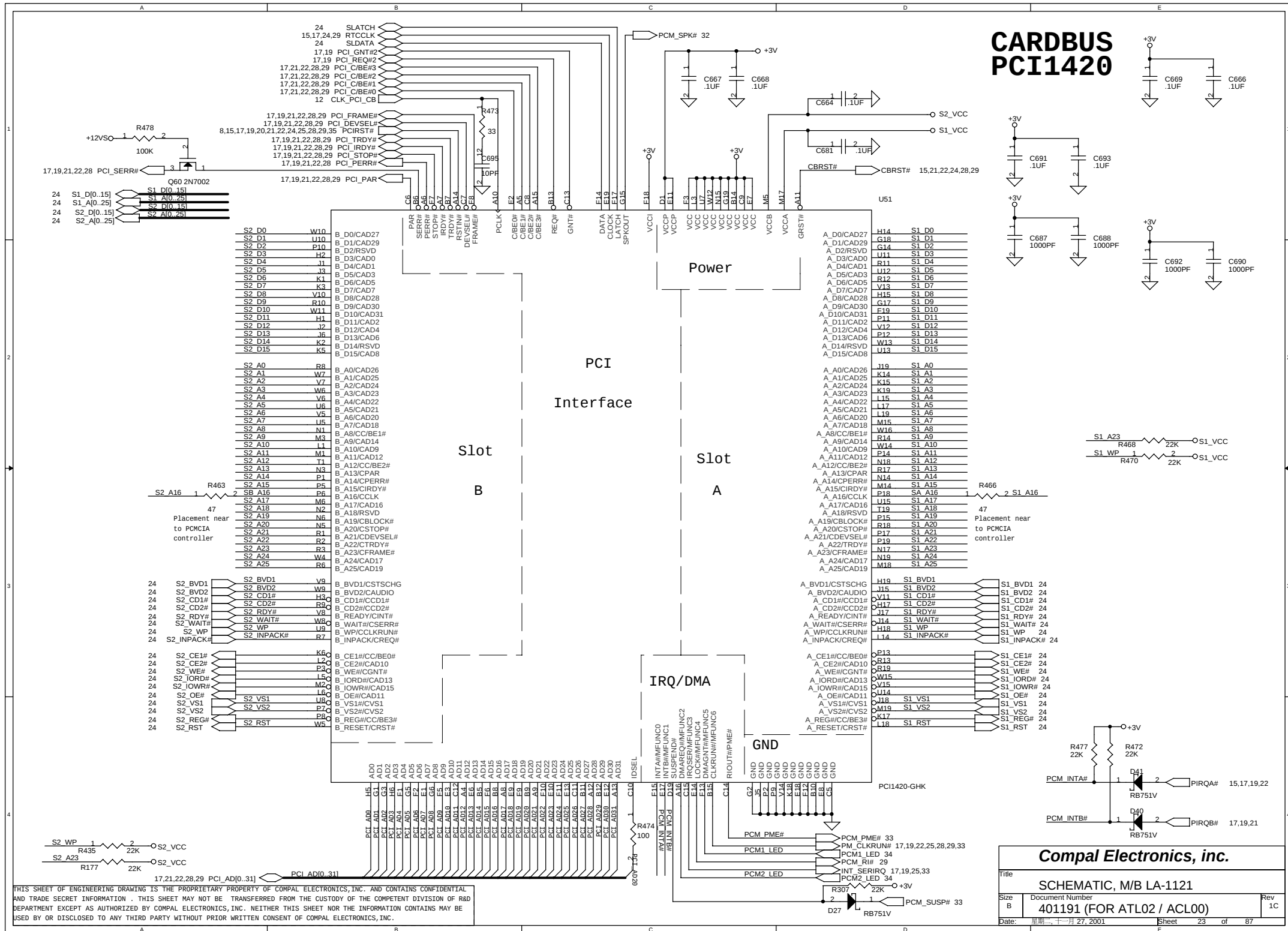
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CARDBUS PCI1420

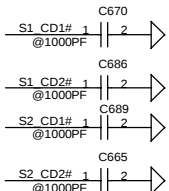
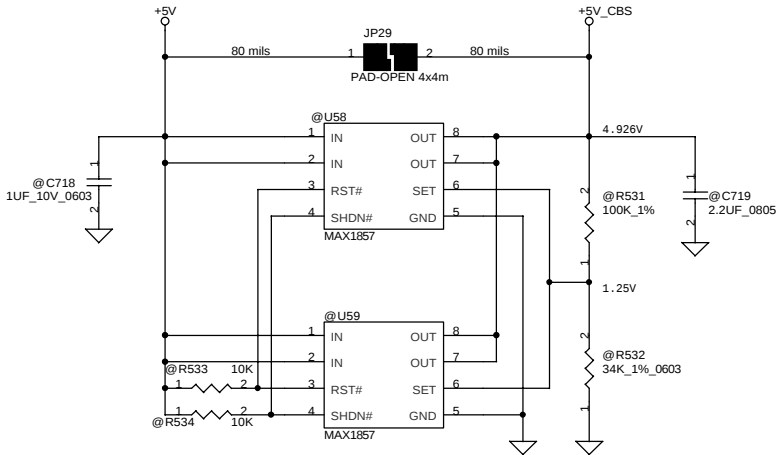
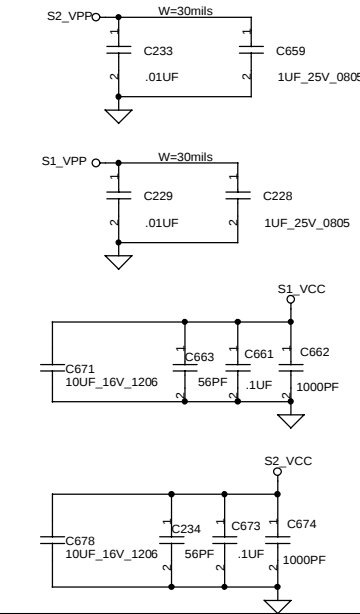
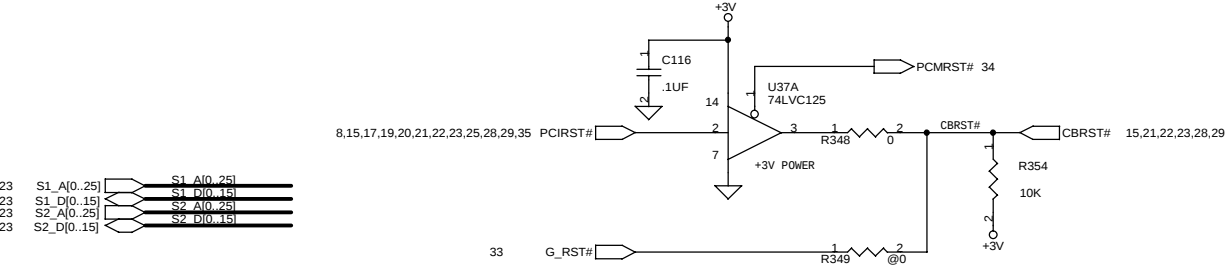
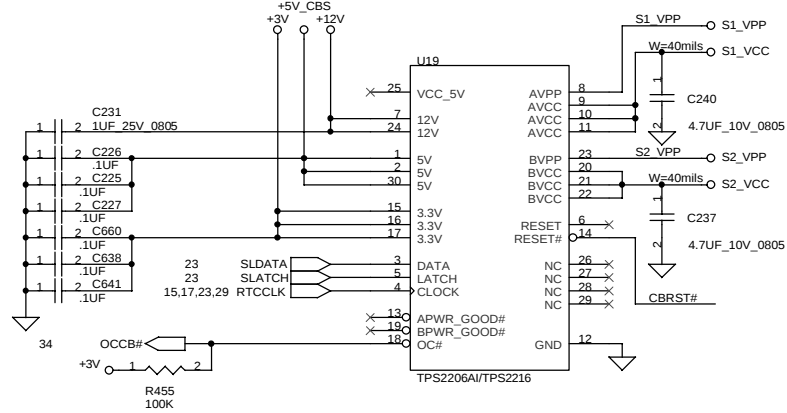
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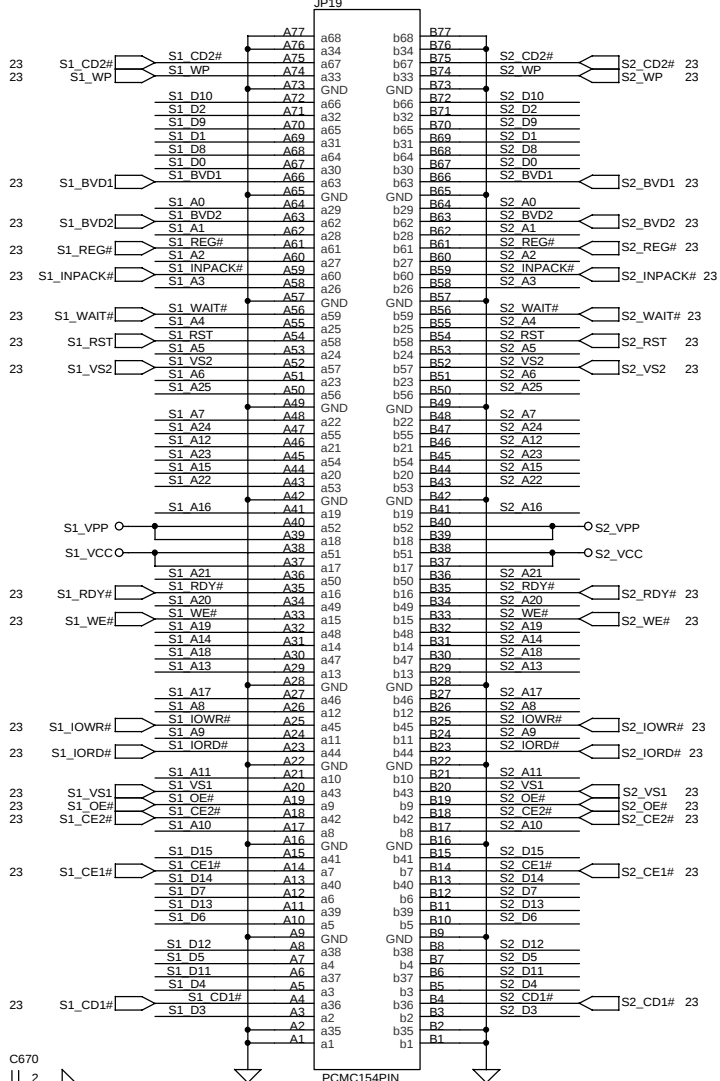
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PCMCIA POWER CTRL.

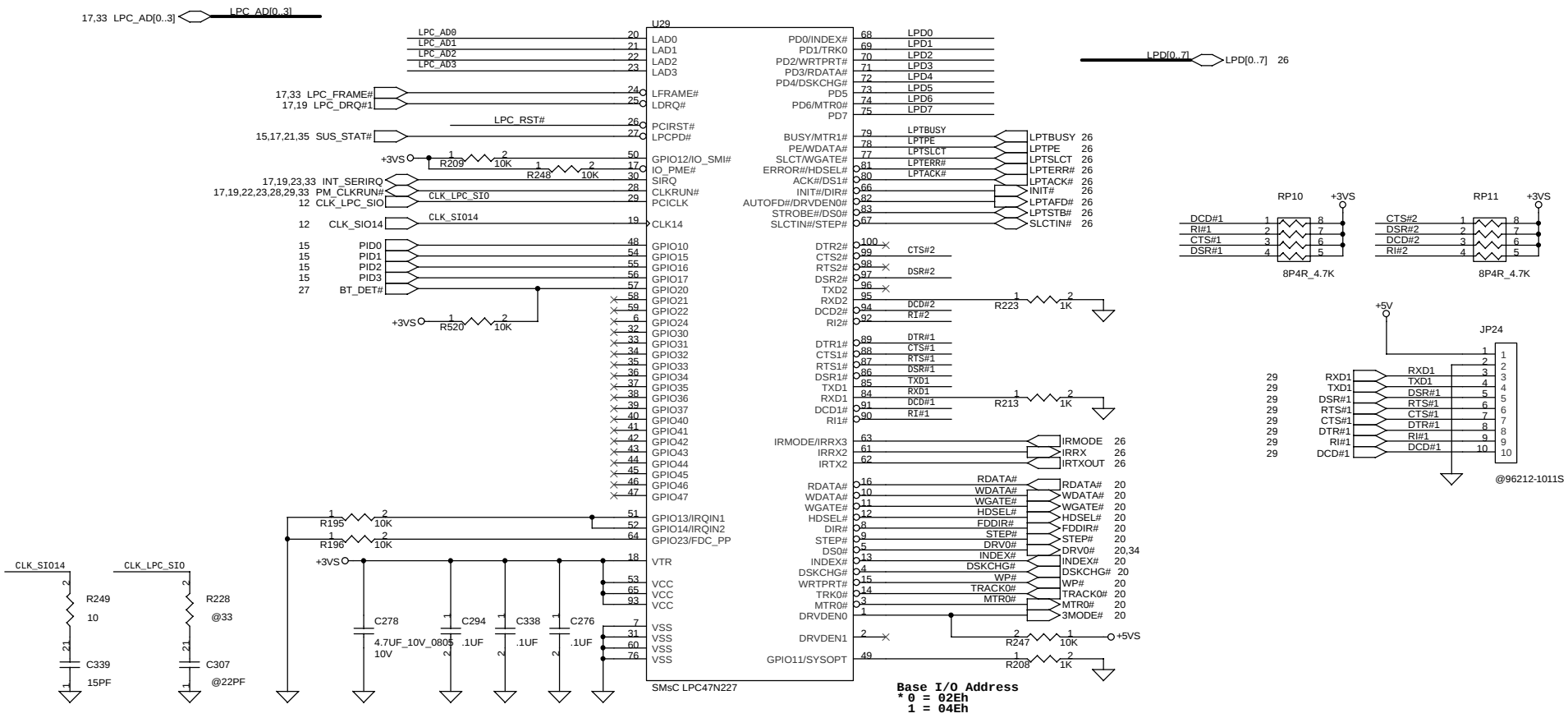


CARDBUS
SOCKET



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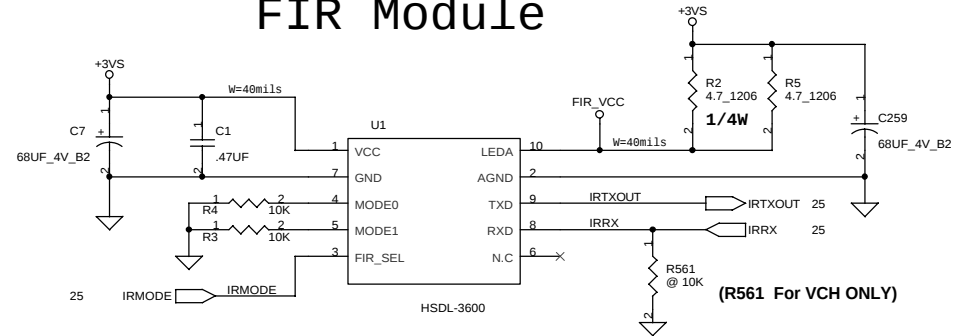
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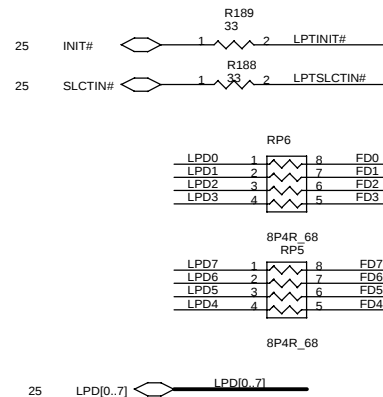
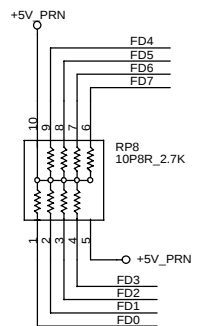
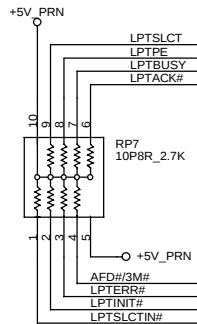
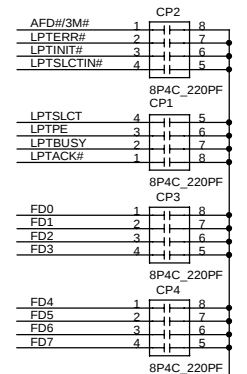
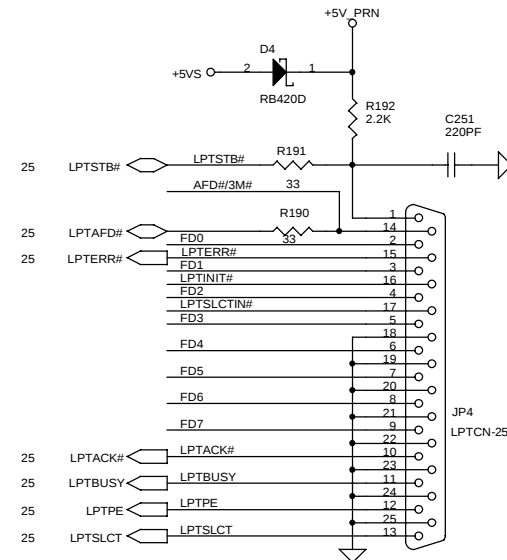
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FIR Module



The component's most place
cloely IRDA MODULE.

PARALLEL PORT



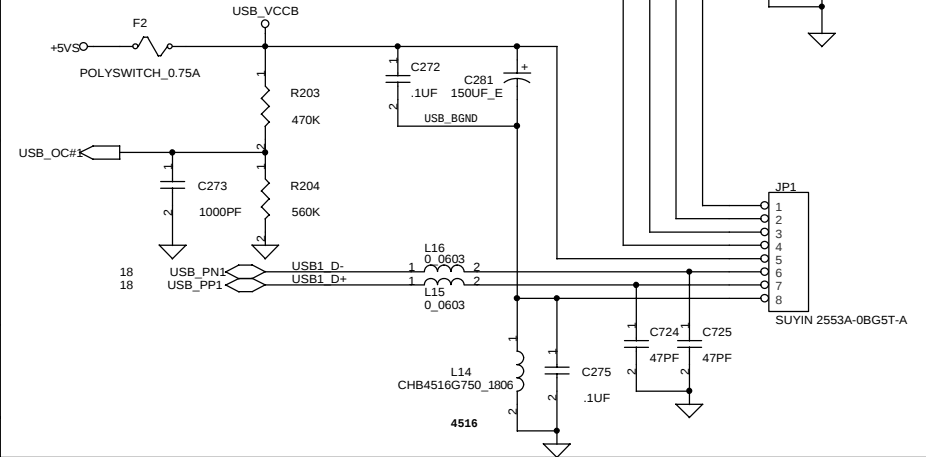
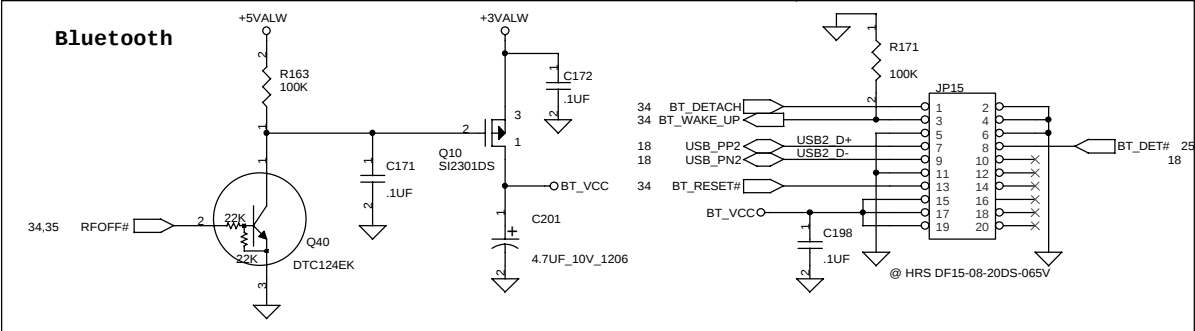
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The schematic diagram illustrates the USB interface circuit for the SUIYIN USB Connector 2569A-04G3T-B. Key components and connections include:

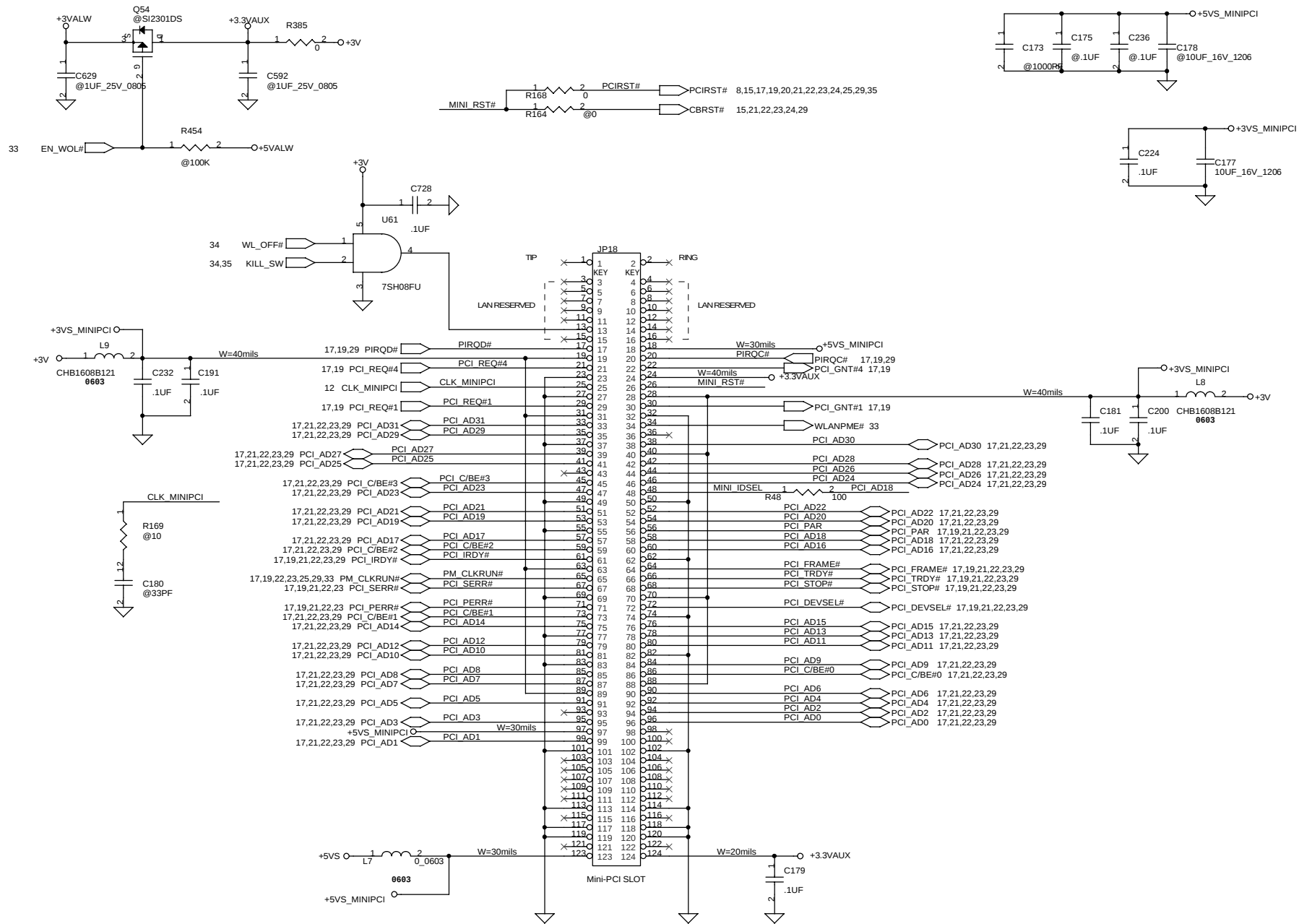
- Power Supply:** A +5V supply is connected to the circuit via a polyswitch (POLYSWITCH_0.75A) and a fuse (F4).
- USB_VCCA:** The USB_VCCA pin is connected to the +5V supply through a 470K resistor (R353) and a 560K resistor (R355).
- USB_OC#:** The USB_OC# pin is connected to the USB_VCCA line through a 1000PF capacitor (C560).
- USB_PN0 and USB_PP0:** These pins are connected to the USB_D- and USB_D+ lines, respectively, through a 0.0603 inductor (L36) and a 0.0603 inductor (L34).
- USB_D- and USB_D+:** These lines are connected to the USB connector pins 1 and 2, respectively, through a 47PF capacitor (C720) and a 47PF capacitor (C721).
- USB_GND:** The USB_GND pin is connected to the ground plane through a 150UF capacitor (C153).
- USB_VCCA:** The USB_VCCA pin is connected to the +5V supply through a 150UF capacitor (C153).
- USB_VCCA:** The USB_VCCA pin is connected to the +5V supply through a 150UF capacitor (C153).
- USB_VCCA:** The USB_VCCA pin is connected to the +5V supply through a 150UF capacitor (C153).

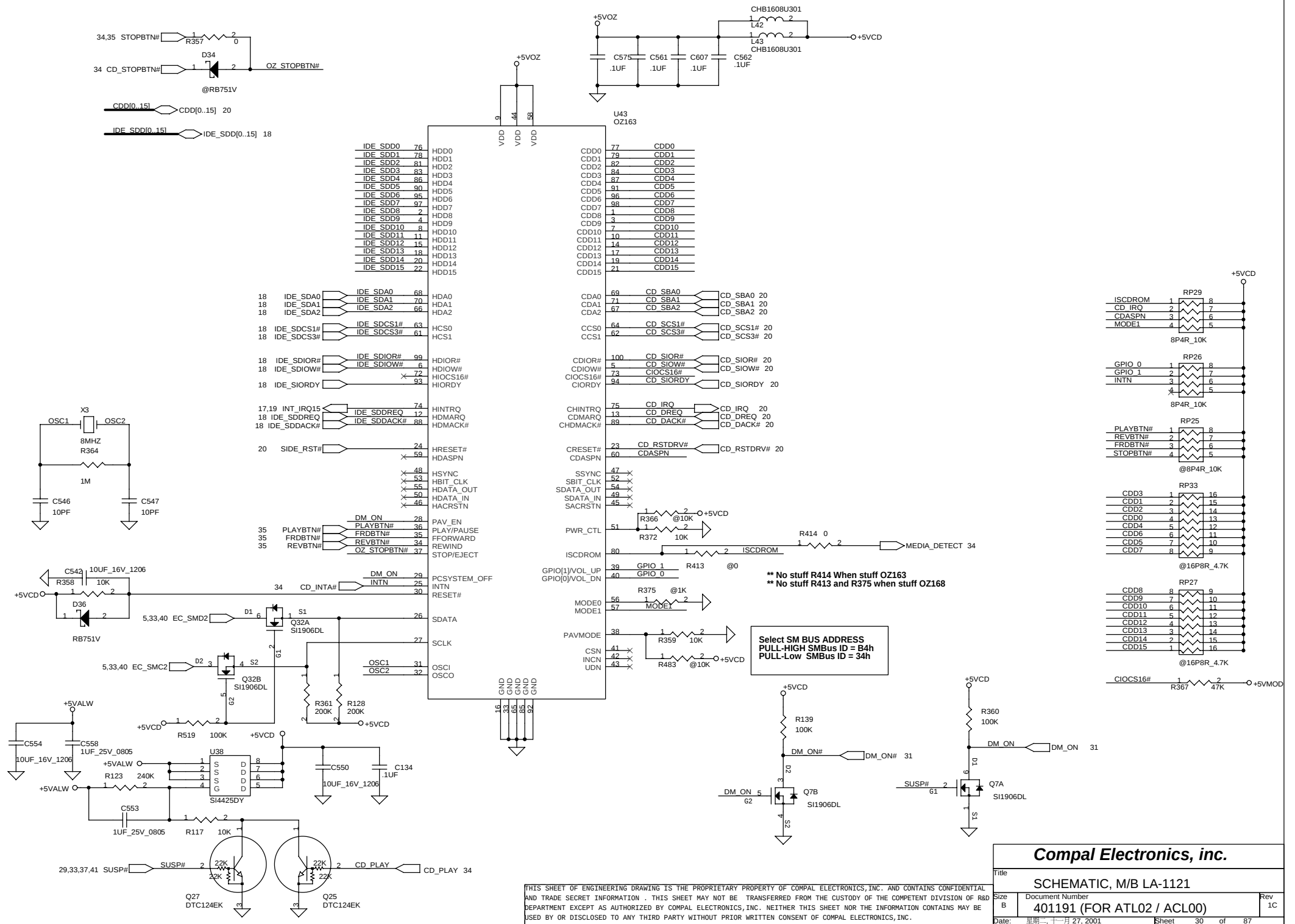


Bluetooth

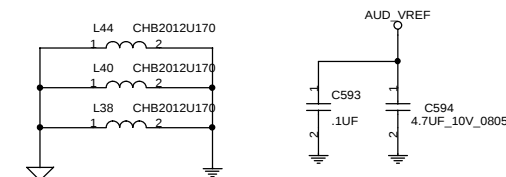
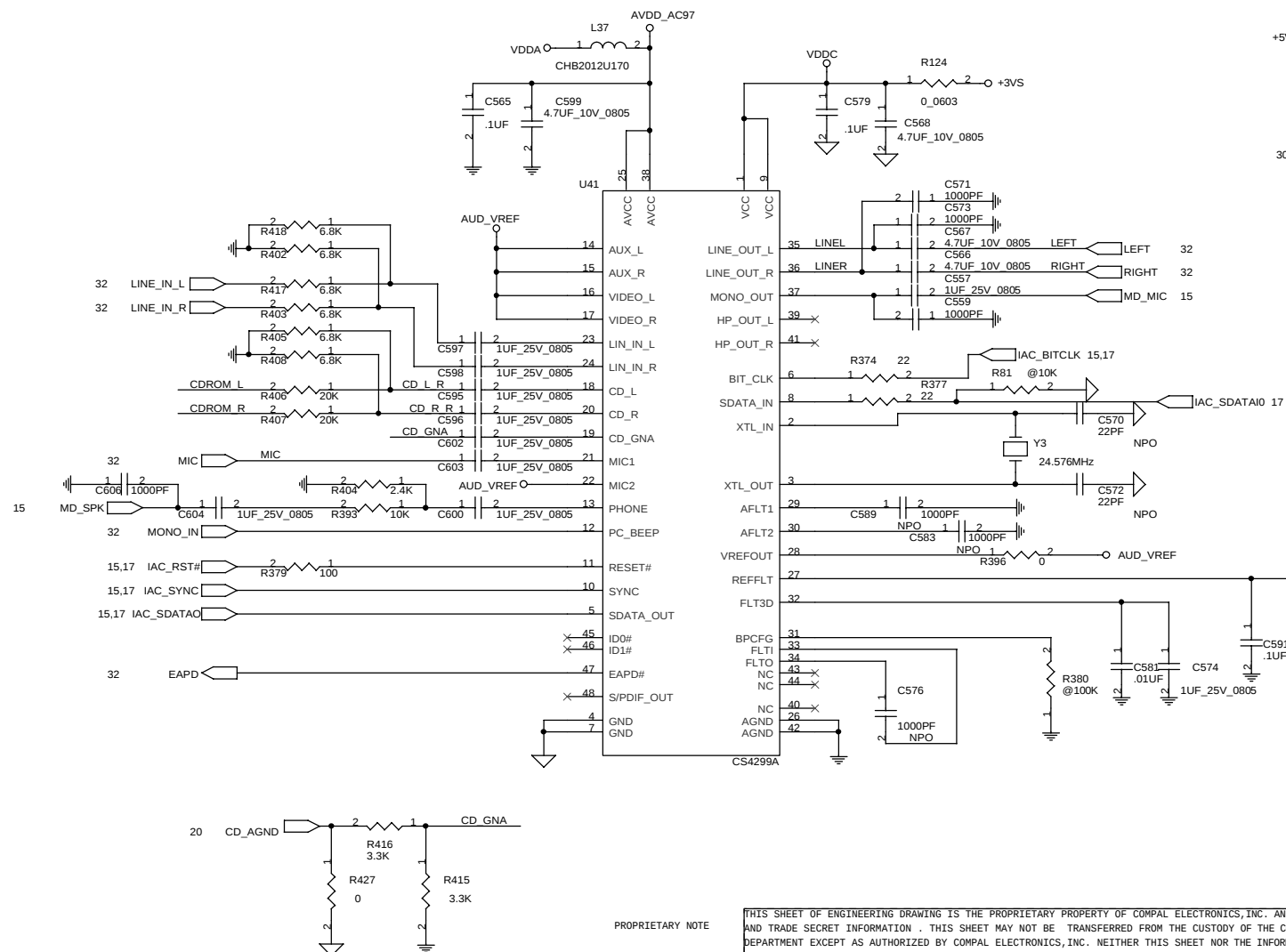
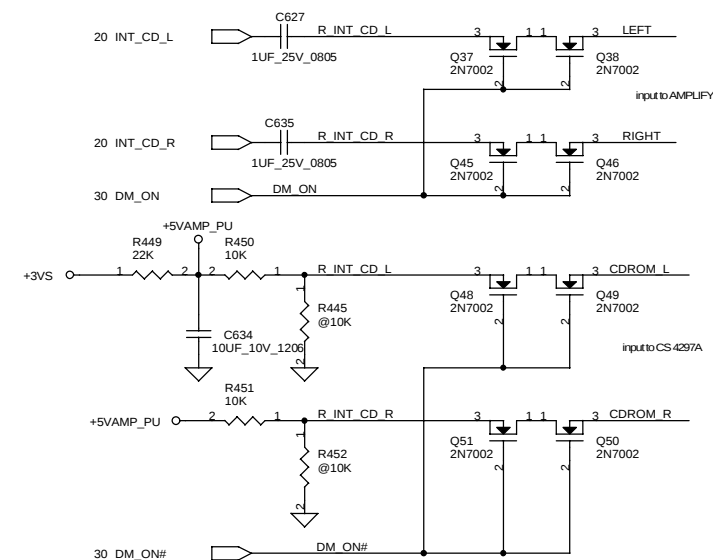
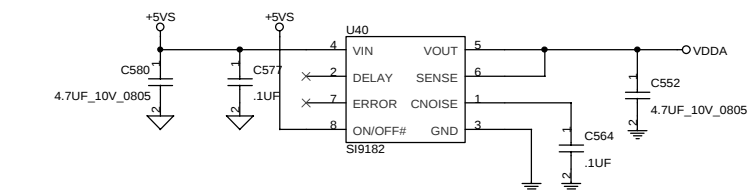
The diagram illustrates the power supply circuit for a Bluetooth module. A 5V regulator (5VALW) provides power to the base of a transistor (Q40, DTC124EK) through a 100K resistor (R163). The emitter of Q40 is grounded. The collector of Q40 is connected to the base of a MOSFET (Q10, Si2301DS). The gate of Q10 is connected to a 3V regulator (3VALW) through a 1uF capacitor (C172) and to the collector of Q40. The source of Q10 is connected to ground through a 4.7uF capacitor (C201) and to the BT_VCC pin of the Bluetooth module. The Bluetooth module also has an RFOFF# pin connected to pin 2 of a component.

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AC97 Codec



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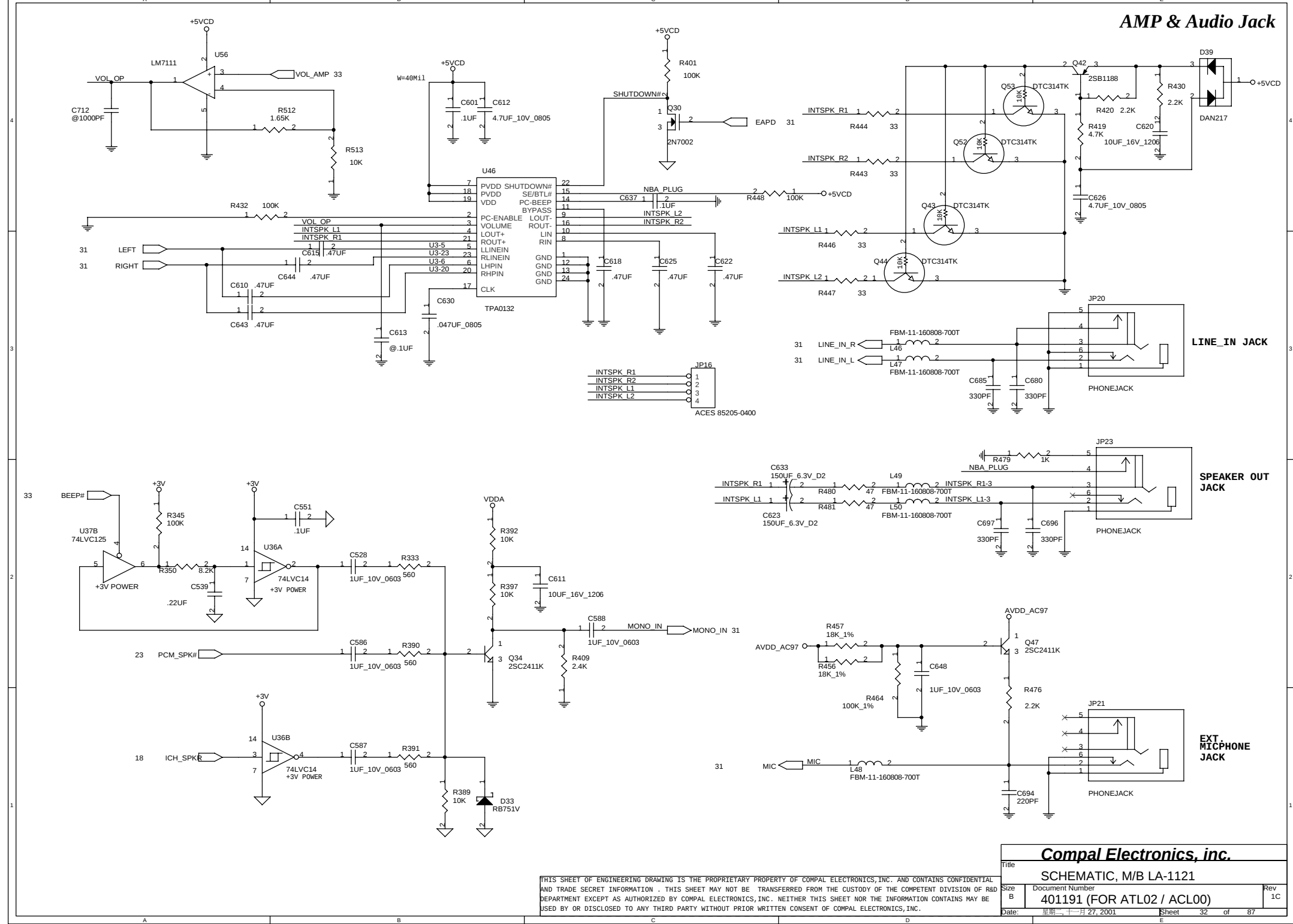
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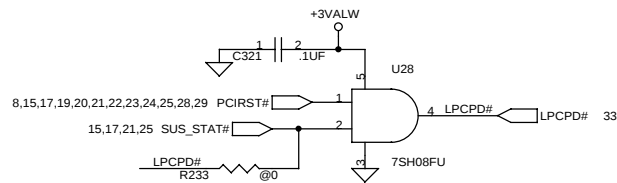
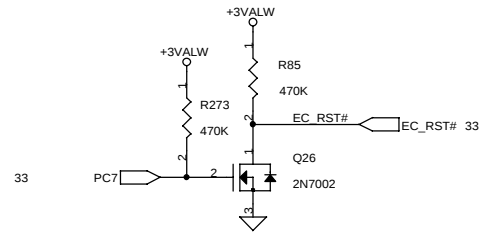
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AMP & Audio Jack

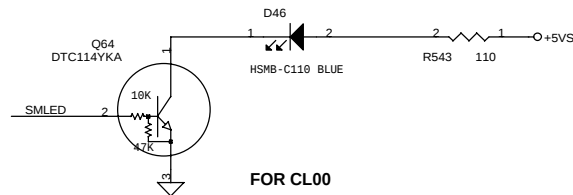


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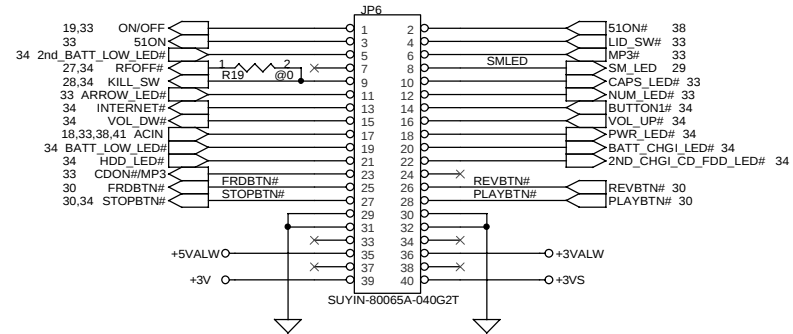
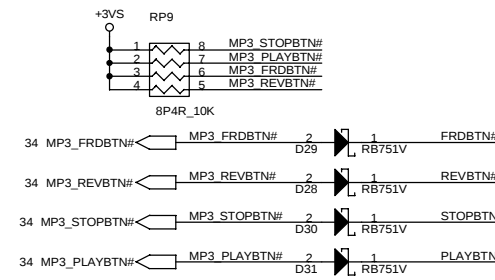
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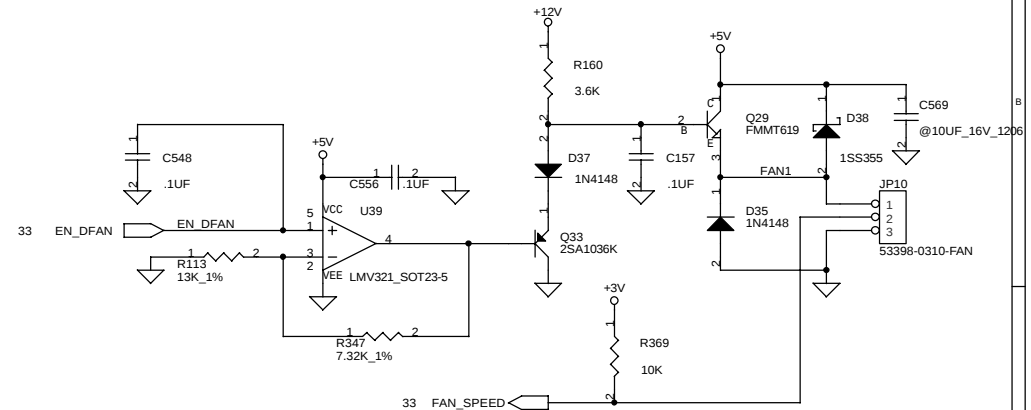
For PC87591 REV 0.A Only



FOR CL00



FAN CONN.



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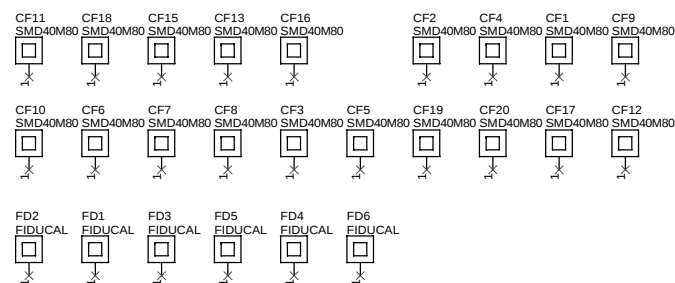
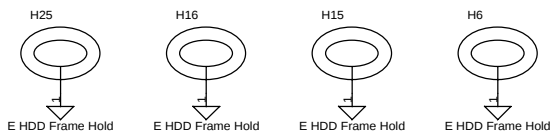
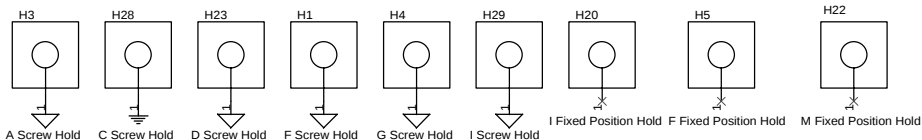
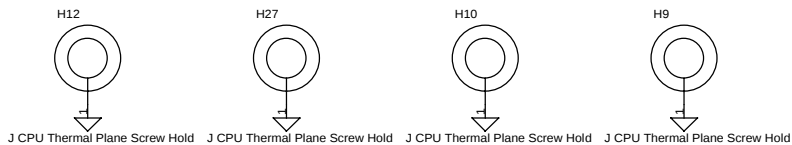
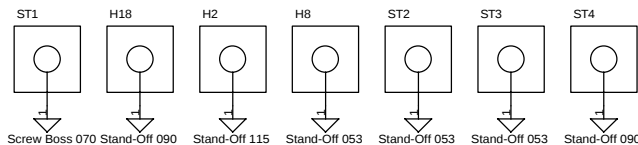
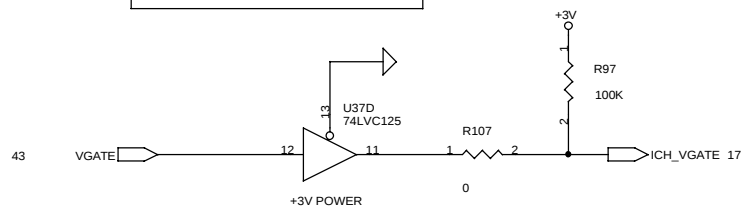
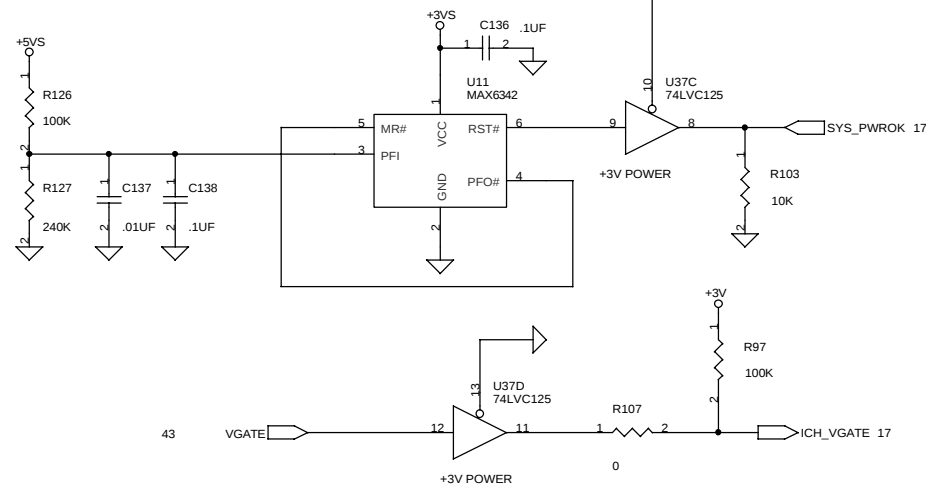
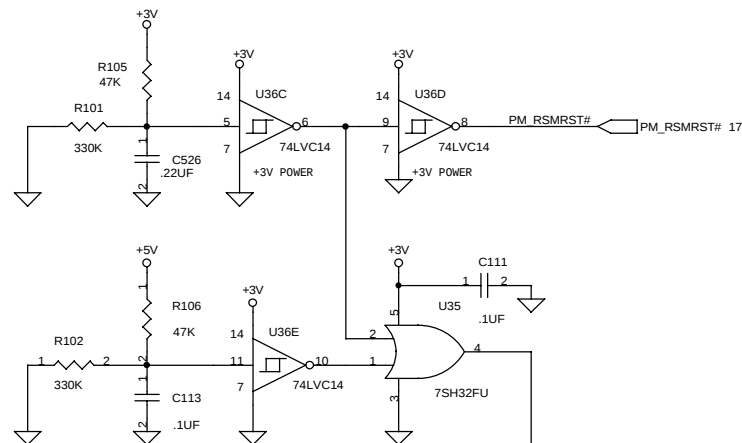
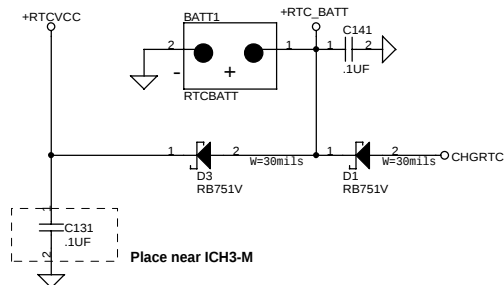
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RTC Batt. Connector

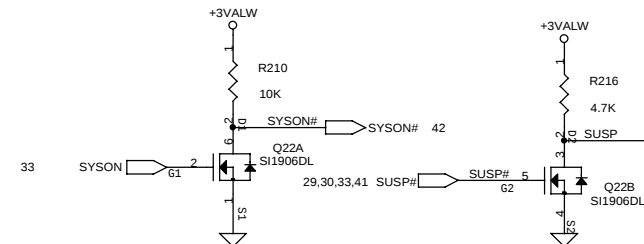
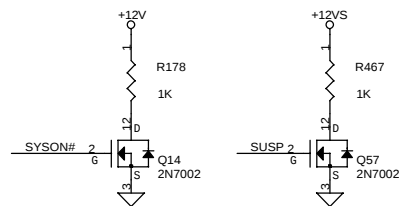
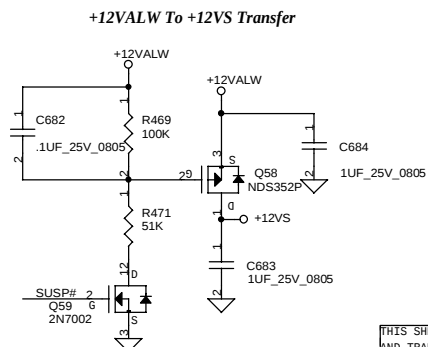
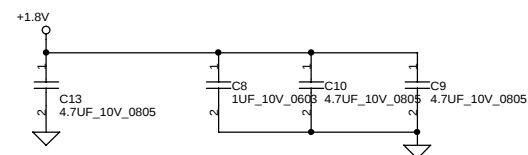
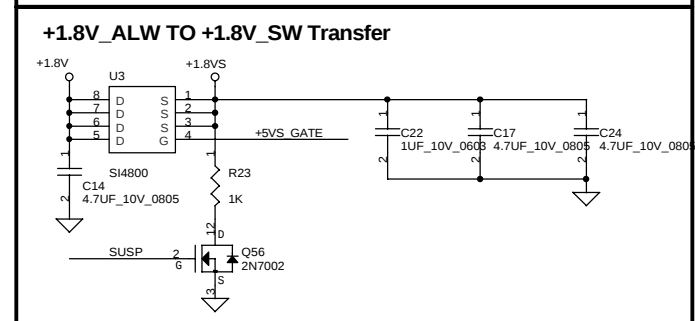
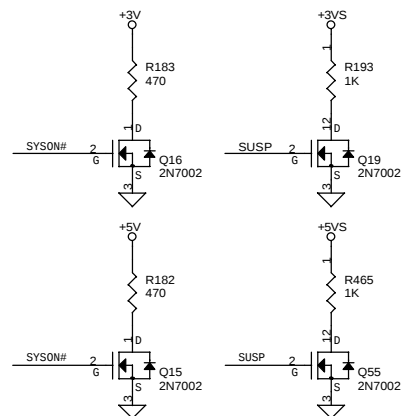
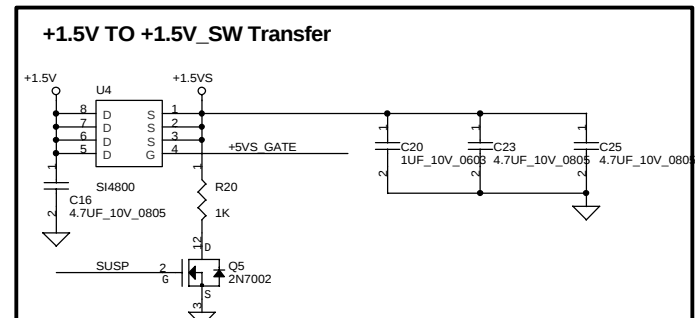
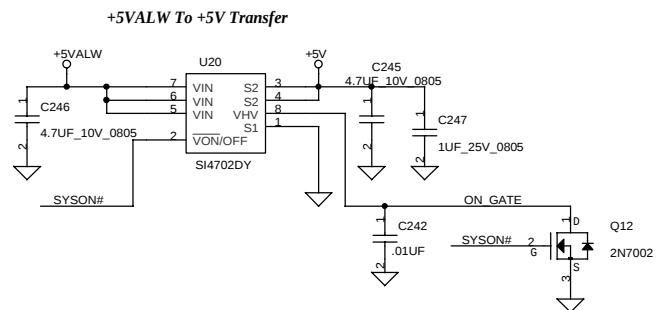


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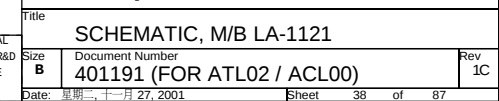
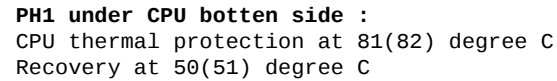
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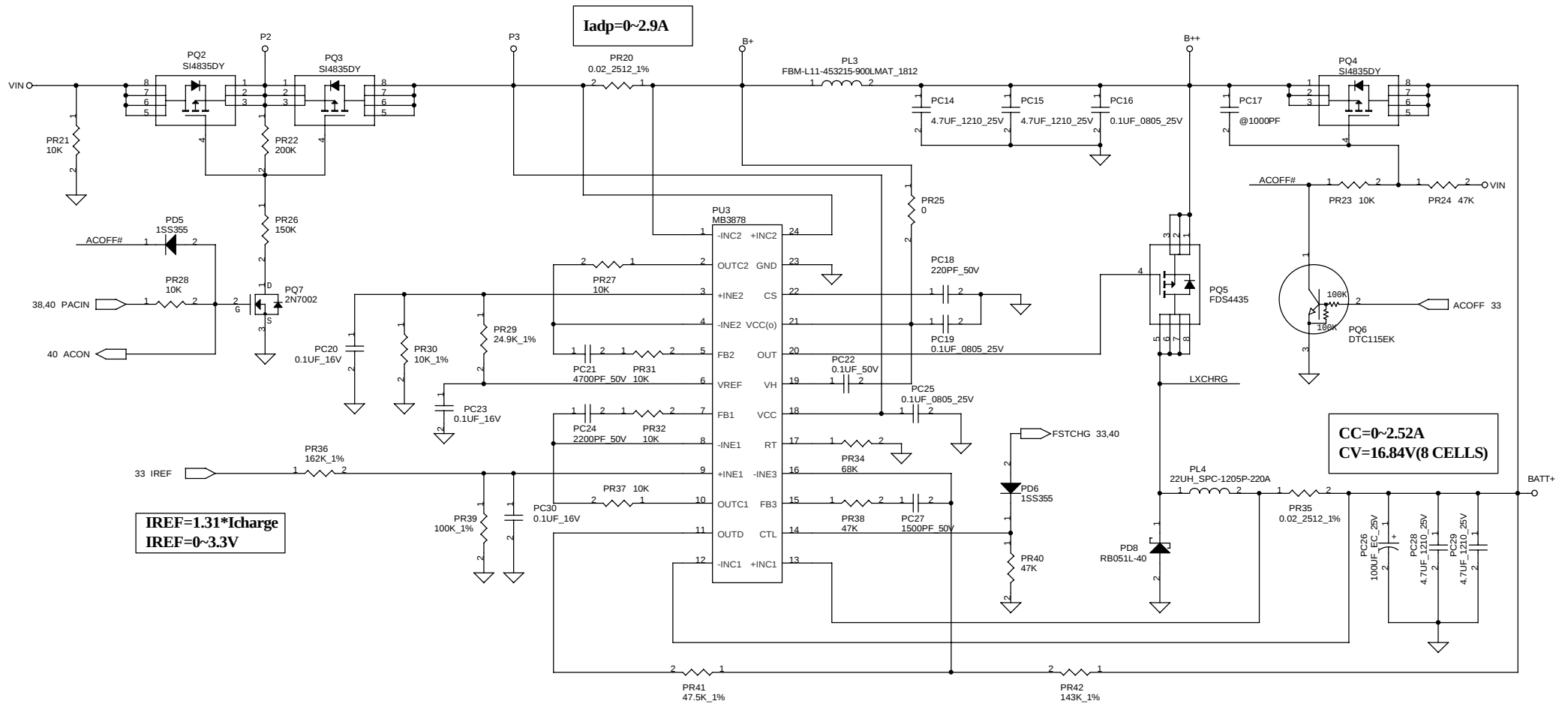
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High	18.764	17.901	17.063
Low	17.745	16.903	16.038



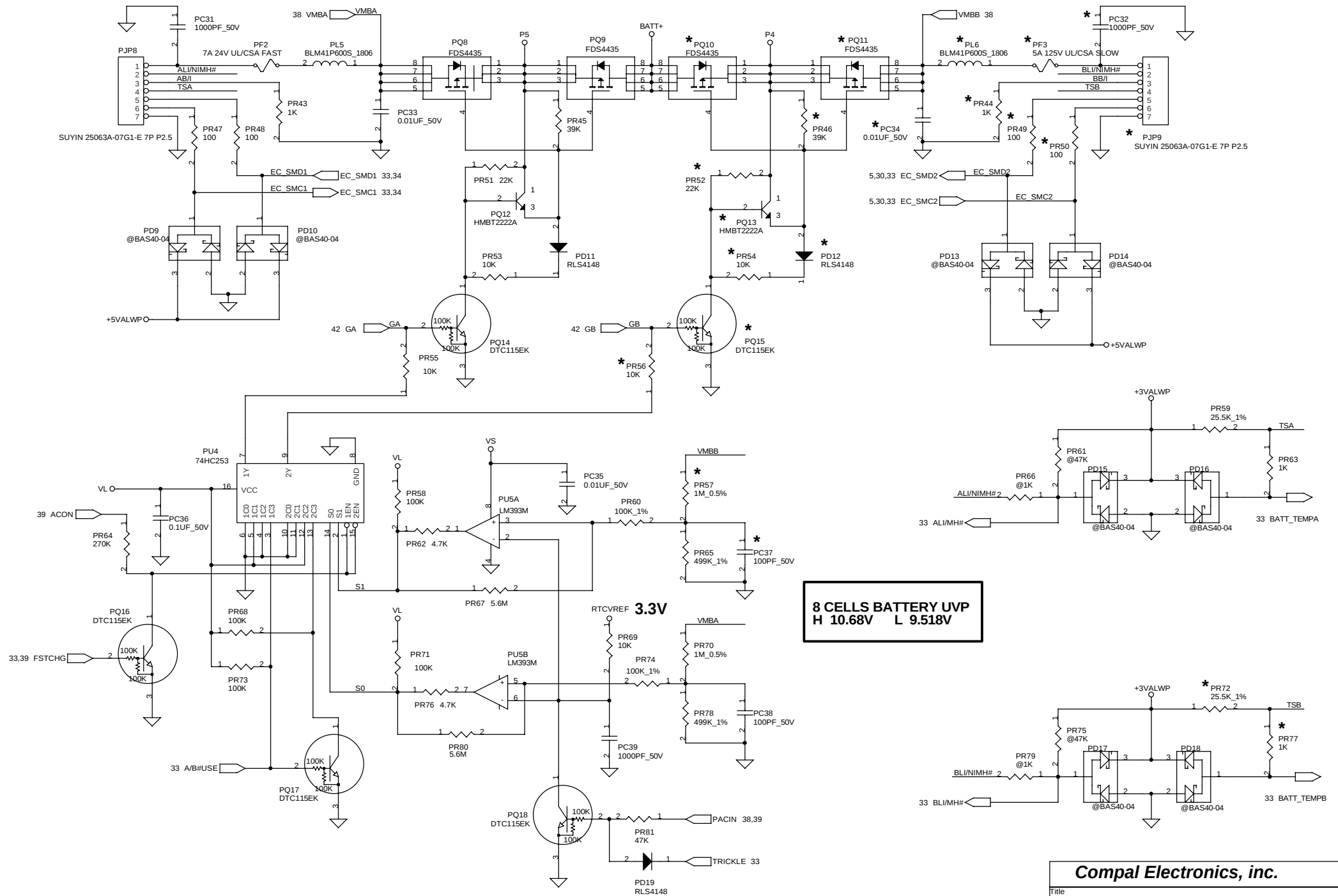
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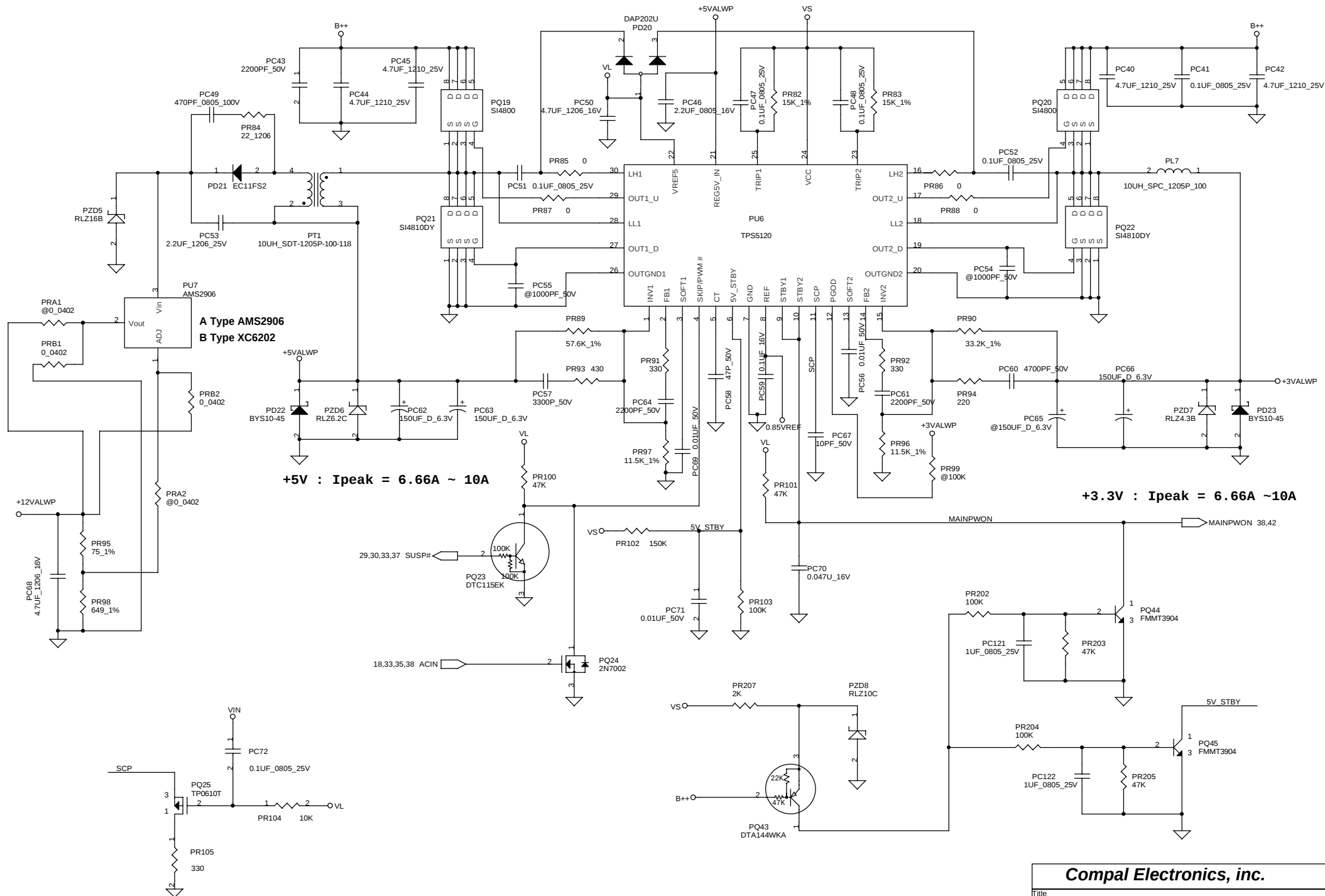
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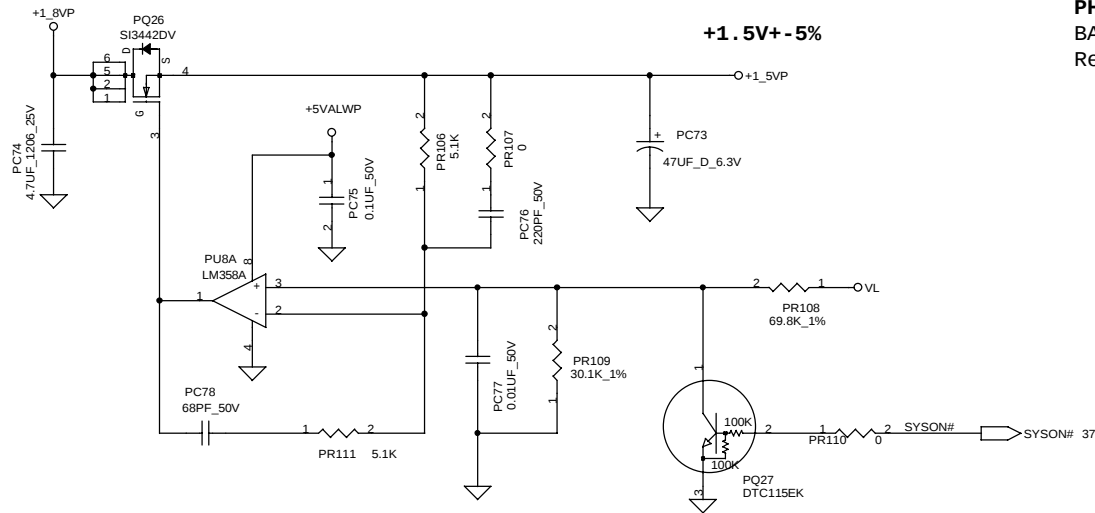
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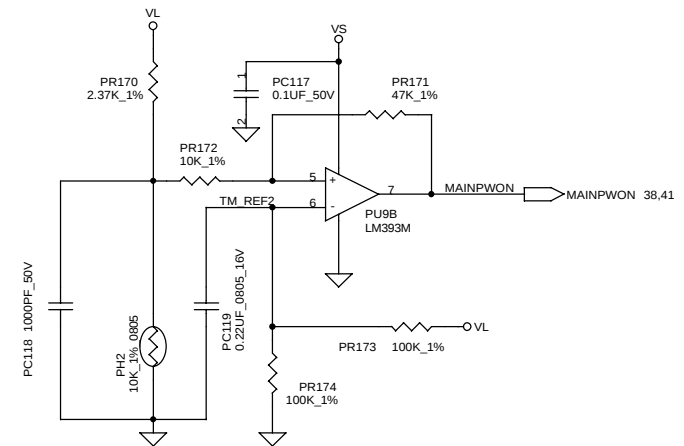
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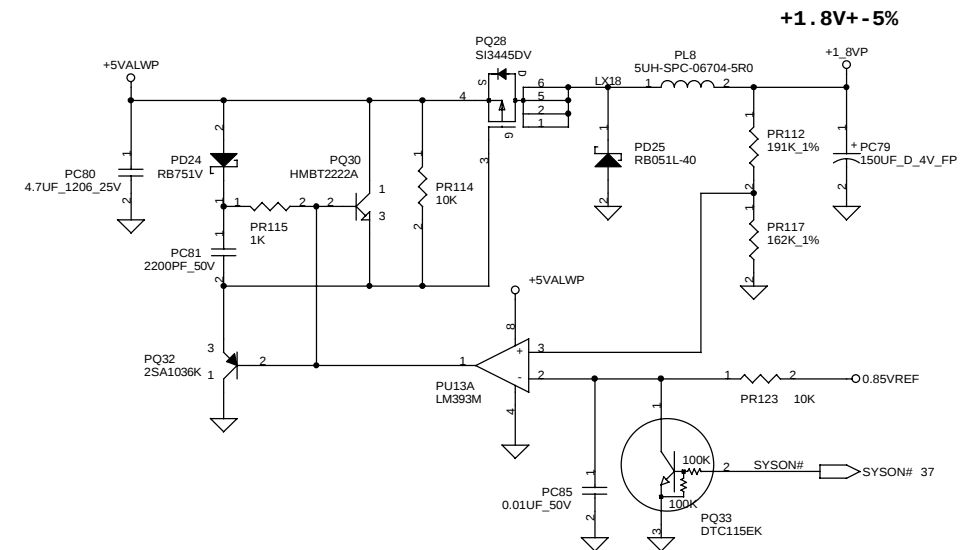
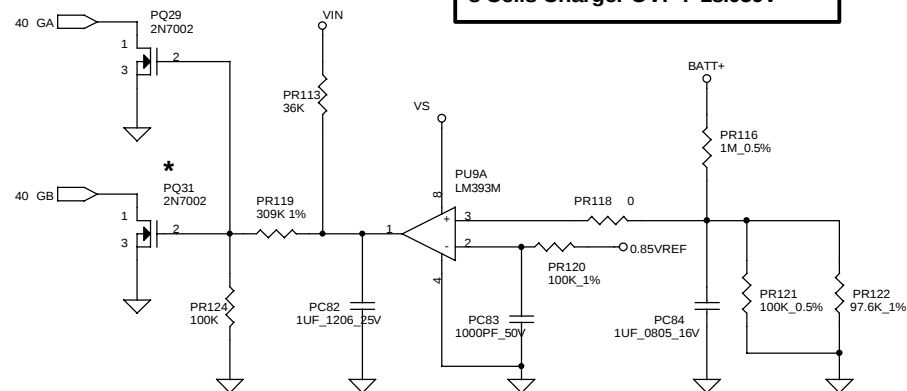


PH2 near main Battery CONN :
BAT. thermal protection at 73(74) degree C
Recovery at 50(51) degree C



The * is DEL item only for ACL00

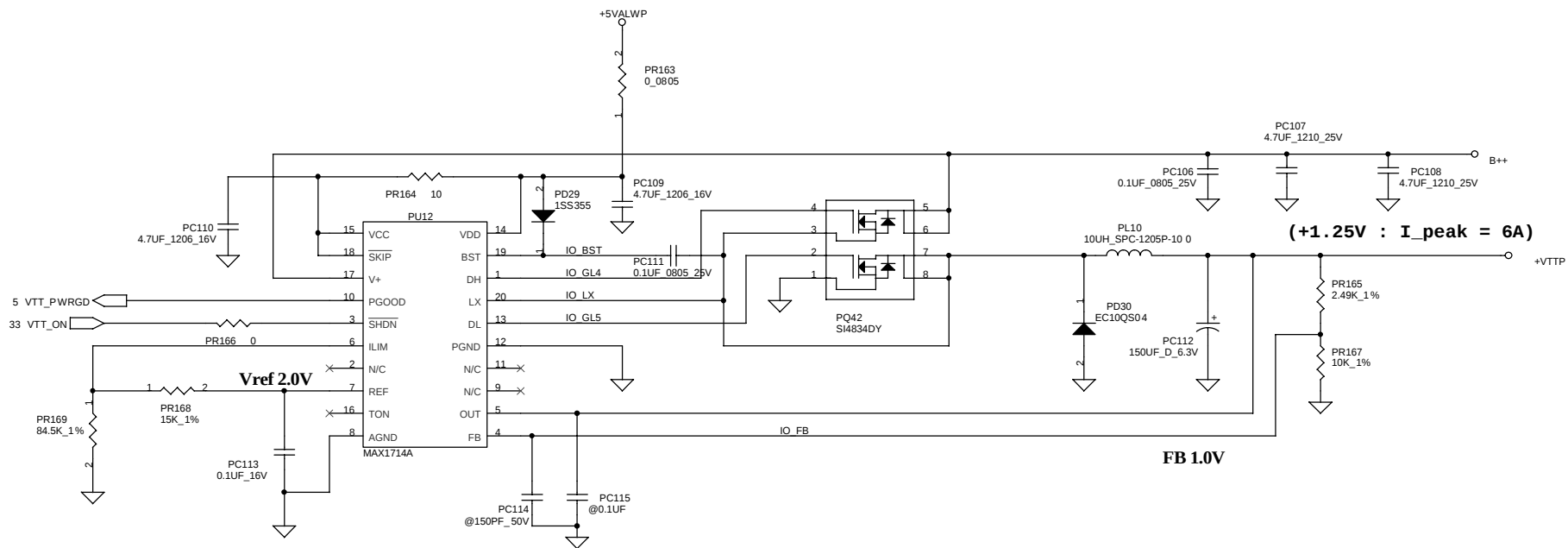
8 Cells Charger OVP : 18.059V



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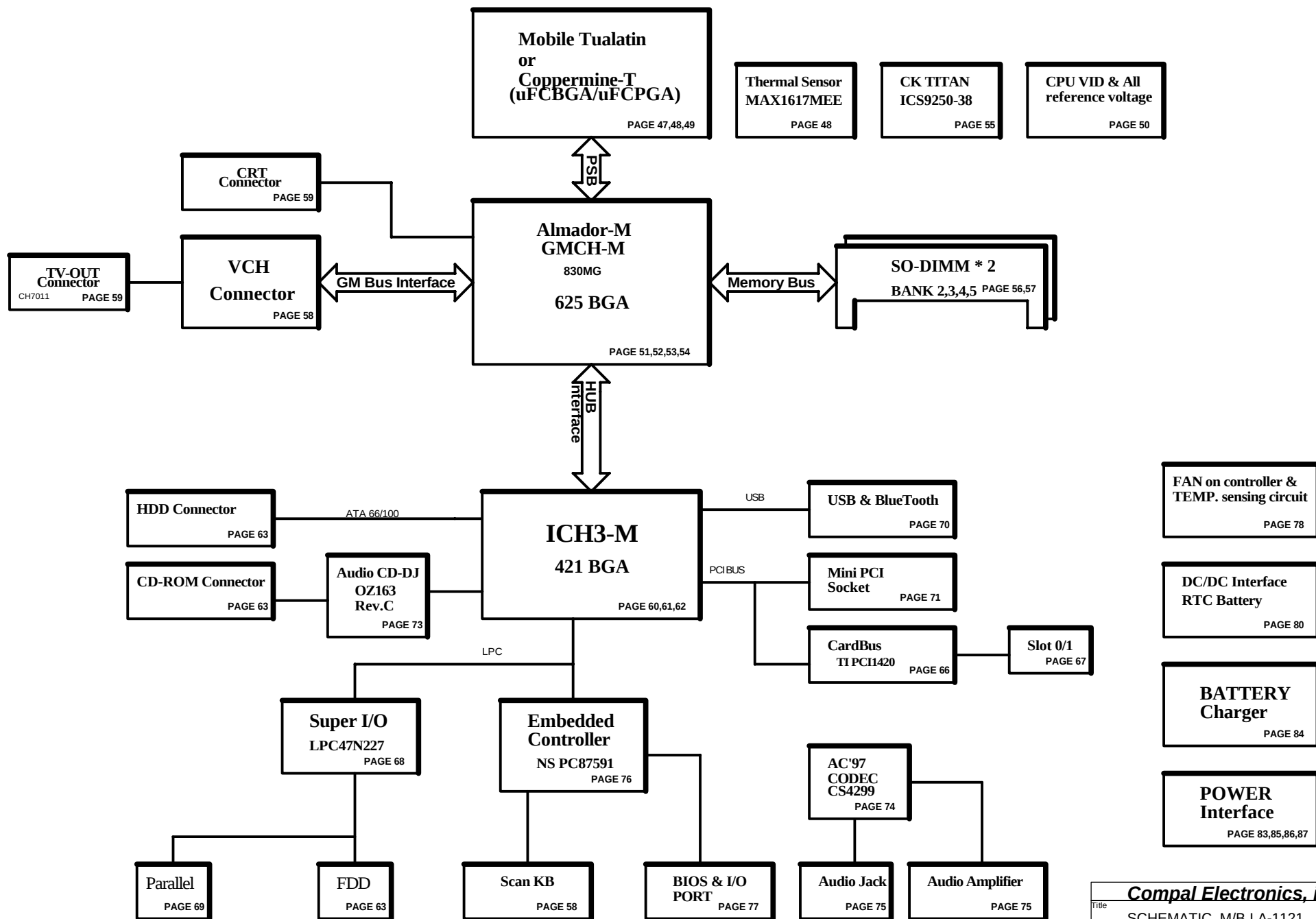
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTC VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ163	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

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PIR

REV 0.2

Date	Page	Description
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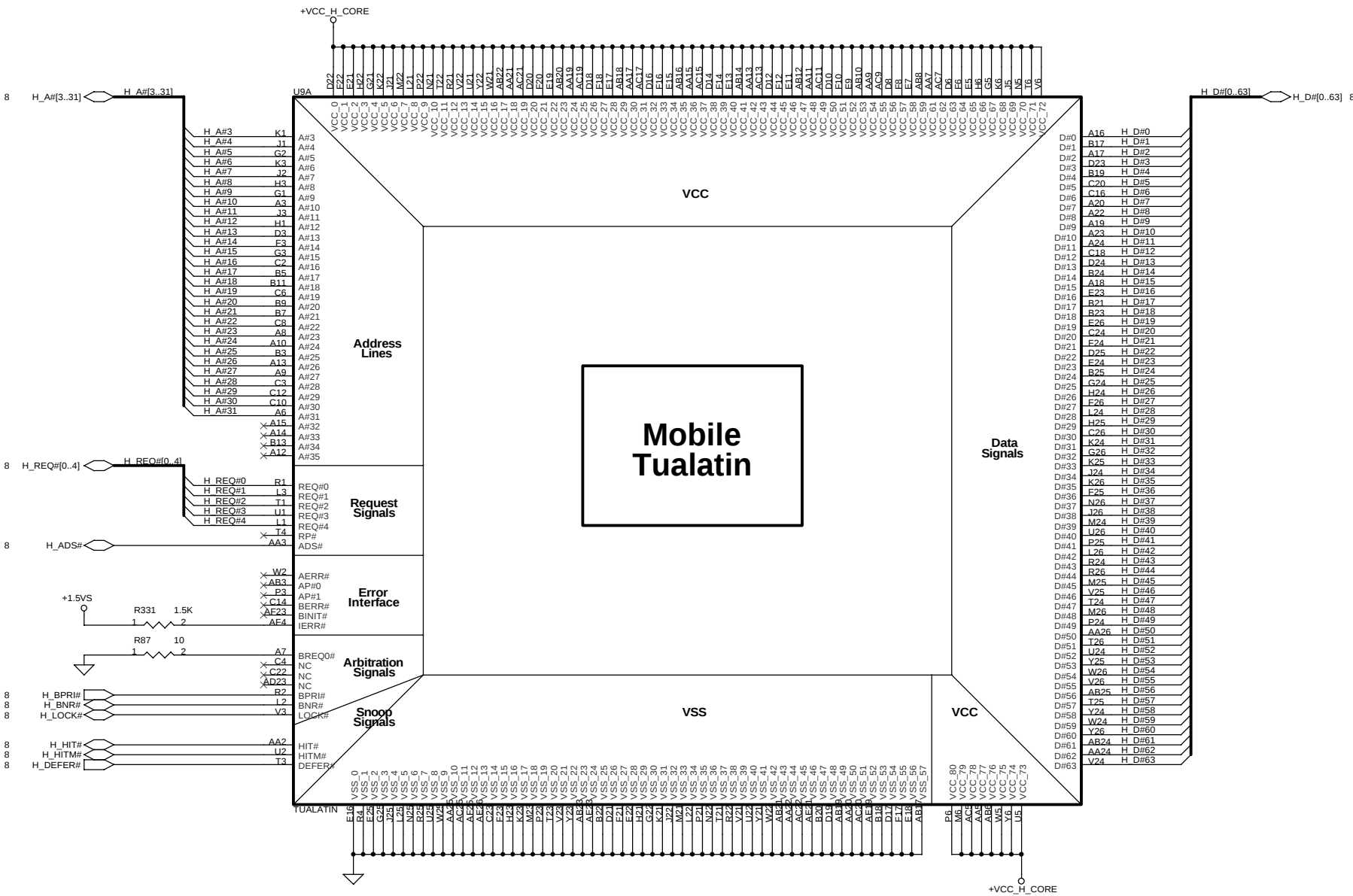
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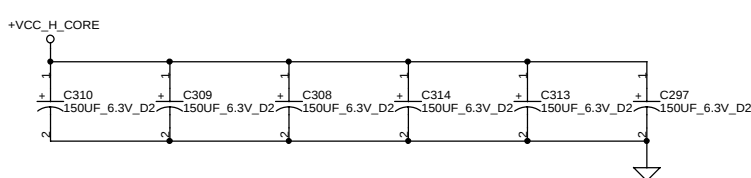
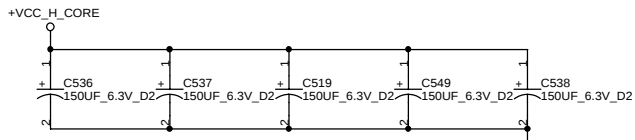
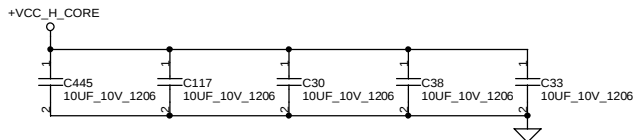
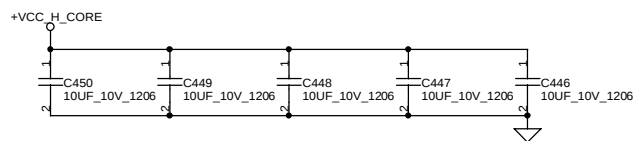
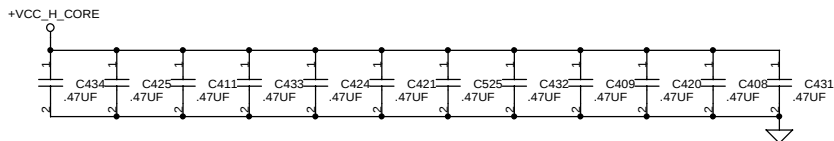
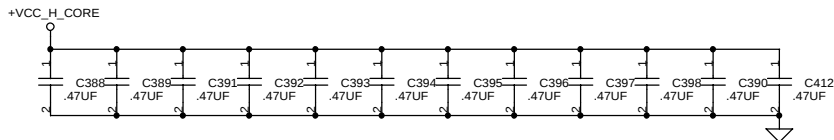


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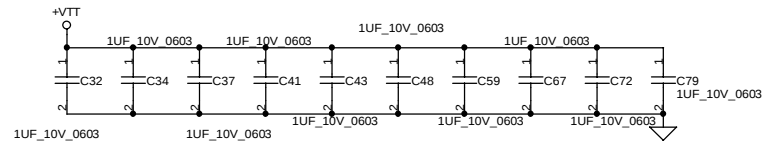
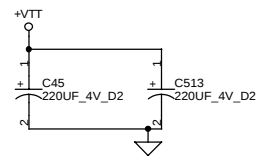
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.



Layout note :

Place close to CPU,
Use 2 vias per PAD.

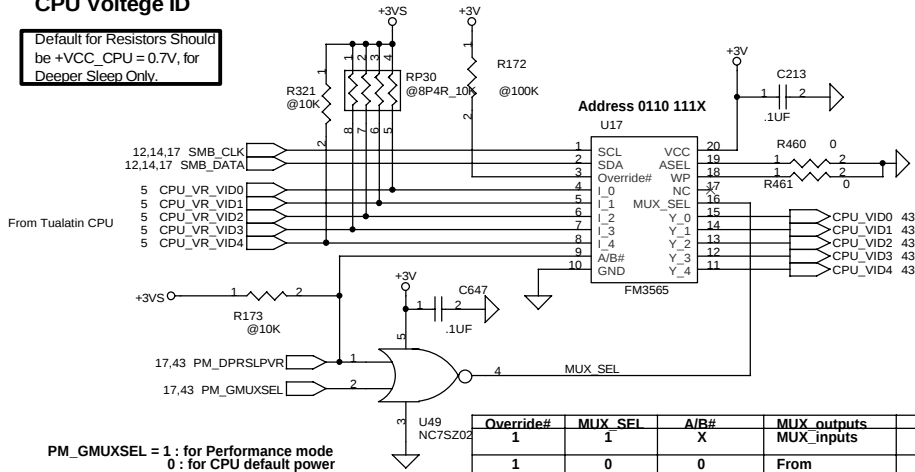


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CPU Voltage ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1 : for Deeper Sleep mode
0 : for Performance mode

Override#	MUX_SEL	A/B#	MUX_outputs MUX_inputs	Mode Battery
1	1	X	From Non-volatile register(SOPRB)	Performance
1	0	0	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

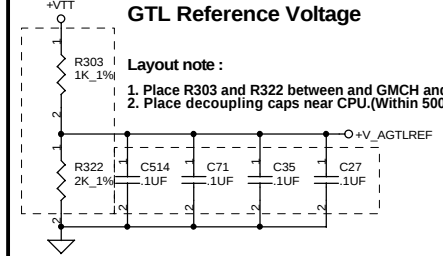
D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

GTL Reference Voltage

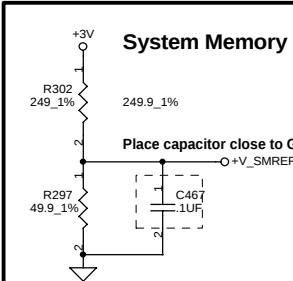
Layout note :

1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)



System Memory Reference

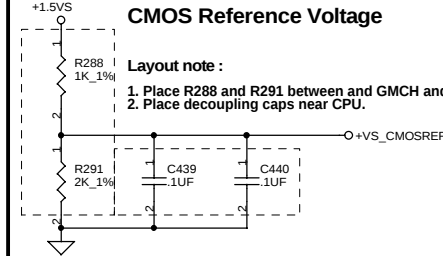
Place capacitor close to GMCH.



CMOS Reference Voltage

Layout note :

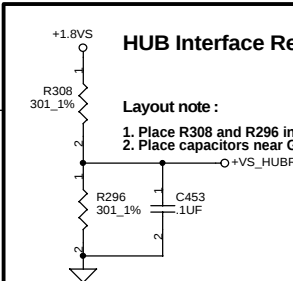
1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.



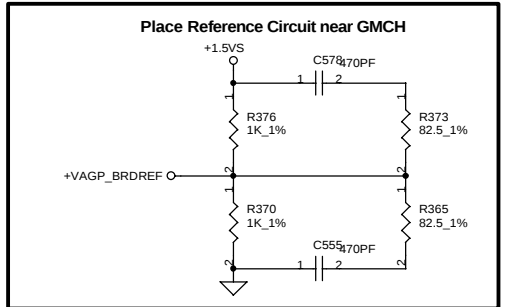
HUB Interface Reference

Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

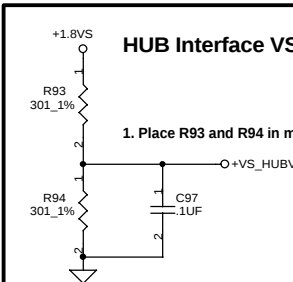


Place Reference Circuit near GMCH

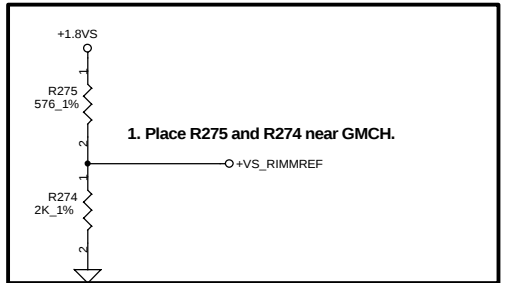


HUB Interface VSwing Voltage

1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.



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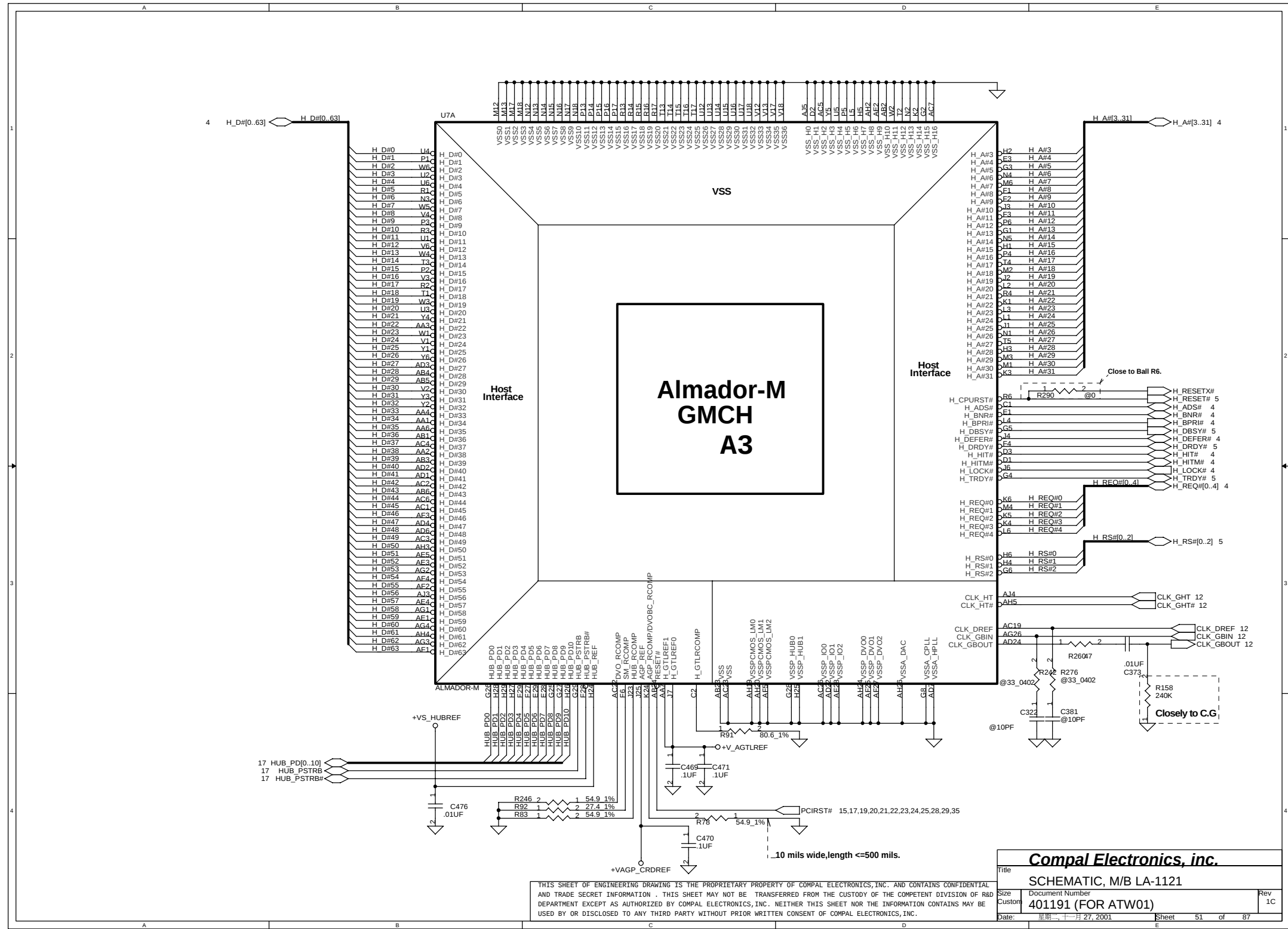
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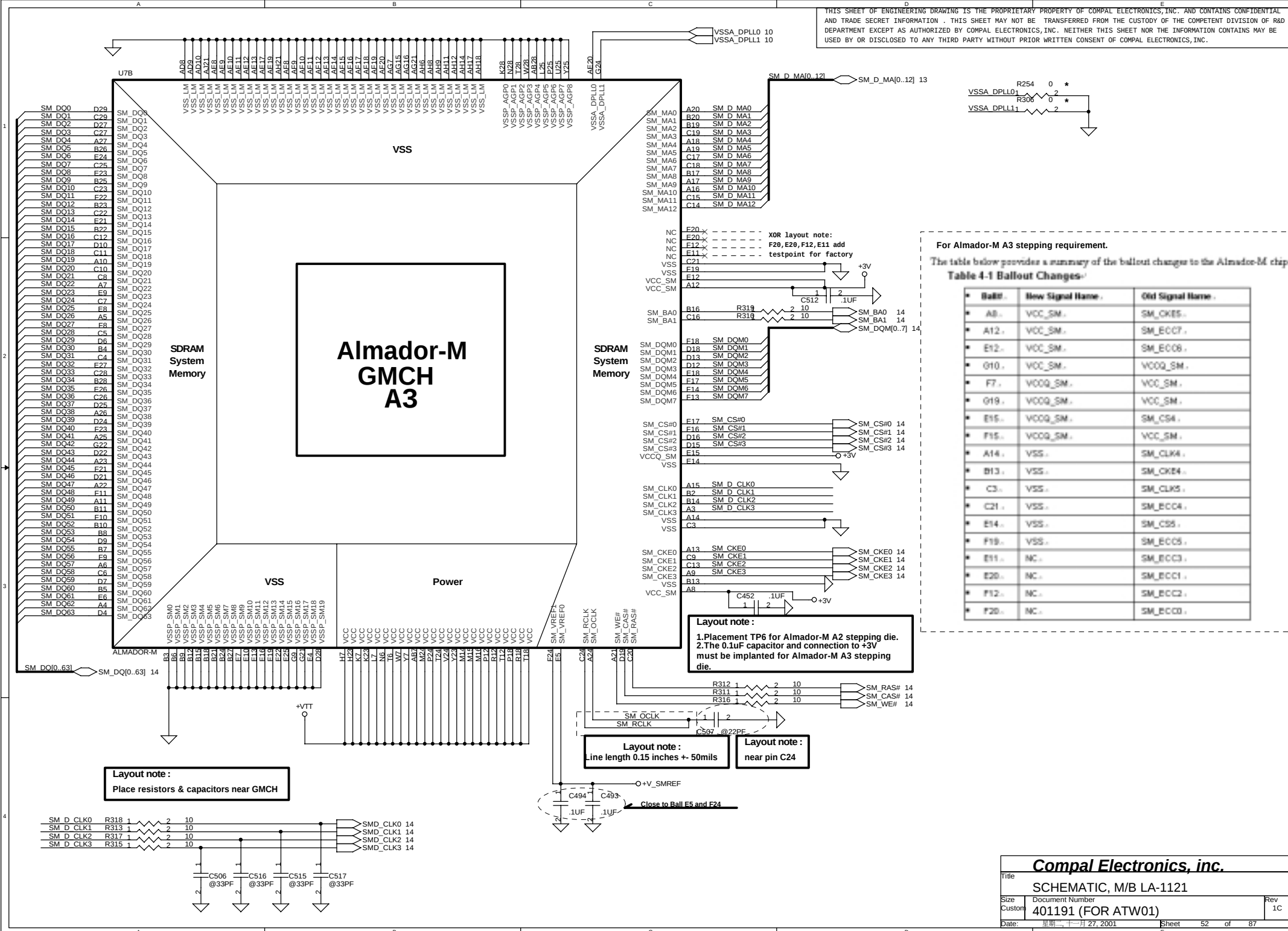
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For Almador-M A3 stepping requirement.

The table below provides a summary of the ballout changes to the Almador-M chip

Table 4-1 Ballout Changes

Ball#	New Signal Name	Old Signal Name
* A8	VCC_SM	SM_CKE5
* A12	VCC_SM	SM_ECC7
* E12	VCC_SM	SM_ECC8
* Q10	VCC_SM	VCCQ_SM
* F7	VCCQ_SM	VCC_SM
* Q19	VCCQ_SM	VCC_SM
* E15	VCCQ_SM	SM_CS4
* F15	VCCQ_SM	VCC_SM
* A14	VSS	SM_CLK4
* B13	VSS	SM_CKE4
* C3	VSS	SM_CLK5
* C21	VSS	SM_ECC4
* E14	VSS	SM_CS5
* F19	VSS	SM_ECC5
* E11	NC	SM_ECC3
* E20	NC	SM_ECC1
* F12	NC	SM_ECC2
* F20	NC	SM_ECC0

Layout note :

1.Placement TP6 for Almador-M A2 stepping die.
2.The 0.1uF capacitor and connection to +3V must be implanted for Almador-M A3 stepping die.

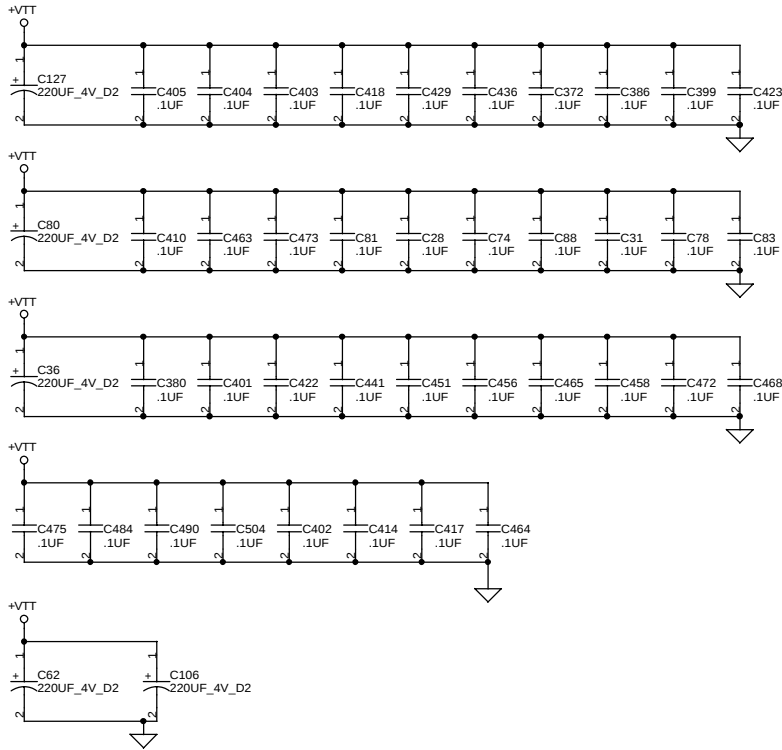
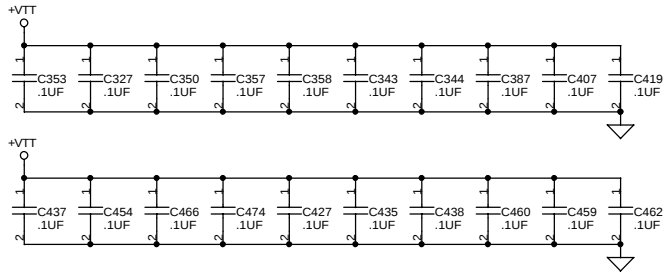
Layout note :
Line length 0.15 inches +/- 50mils

Layout note :
near pin C24

Layout note :
Place resistors & capacitors near GMCH

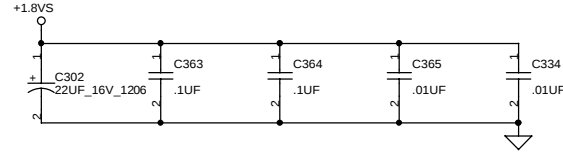
Layout note :

Distribute as close as possible
to GMCH Processor Quadrant .



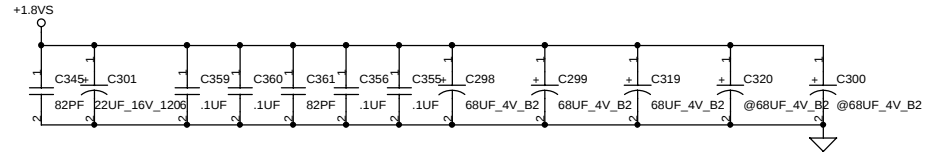
Layout note :

Distribute as close as possible
to VCCPCMOS_LM .



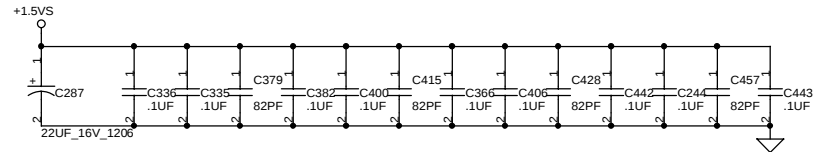
Layout note :

Distribute as close as possible
to GMCH Local Memory Quadrant .



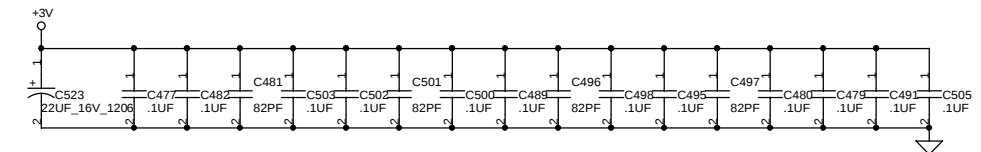
Layout note :

Distribute as close as possible
to GMCH AGP/DVO Quadrant .



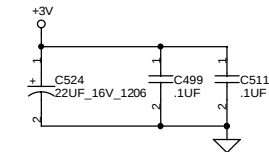
Layout note :

Distribute as close as possible
to GMCH System Memory Quadrant .



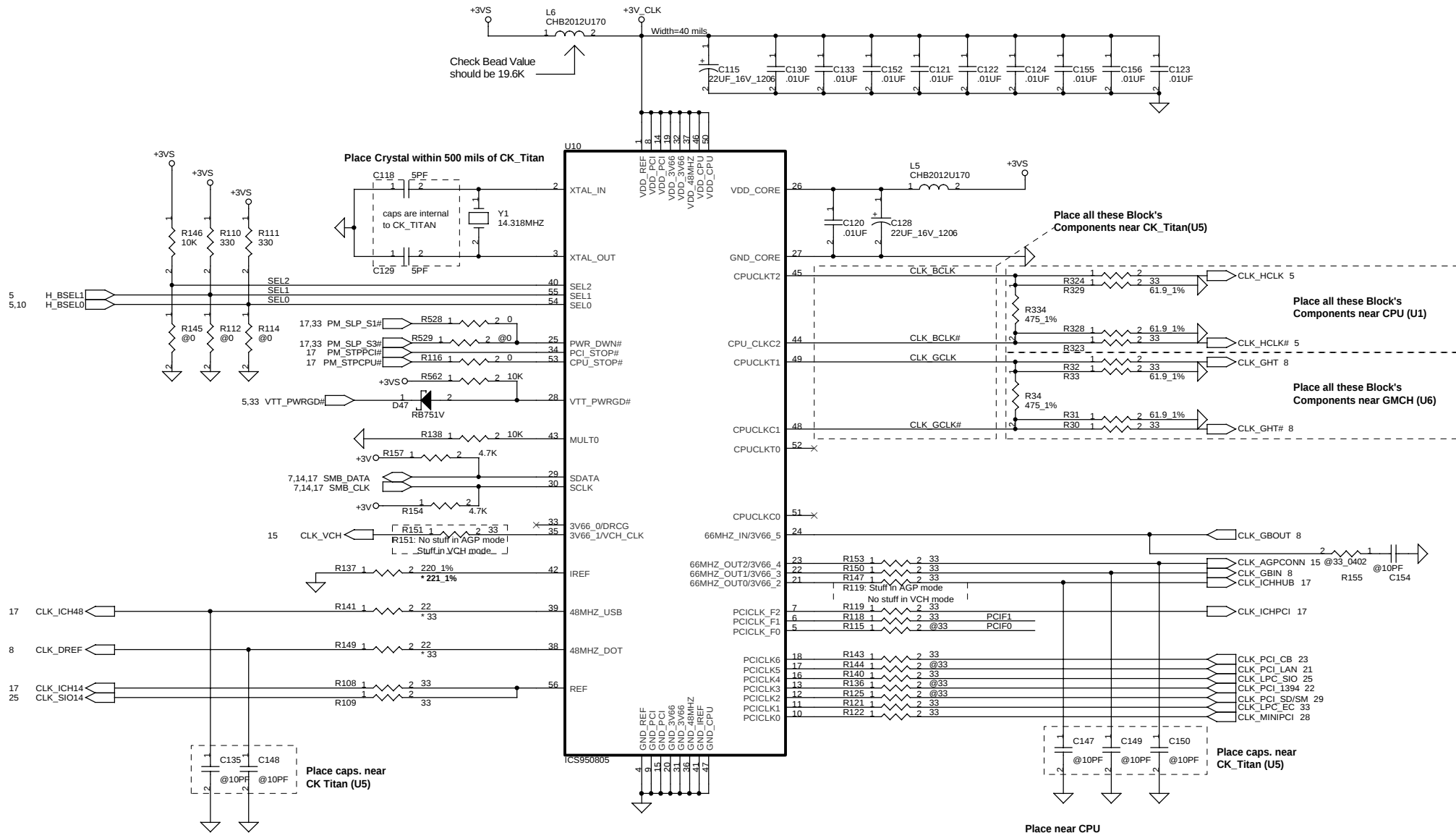
Layout note :

Distribute as close as possible
to IO Quadrant .



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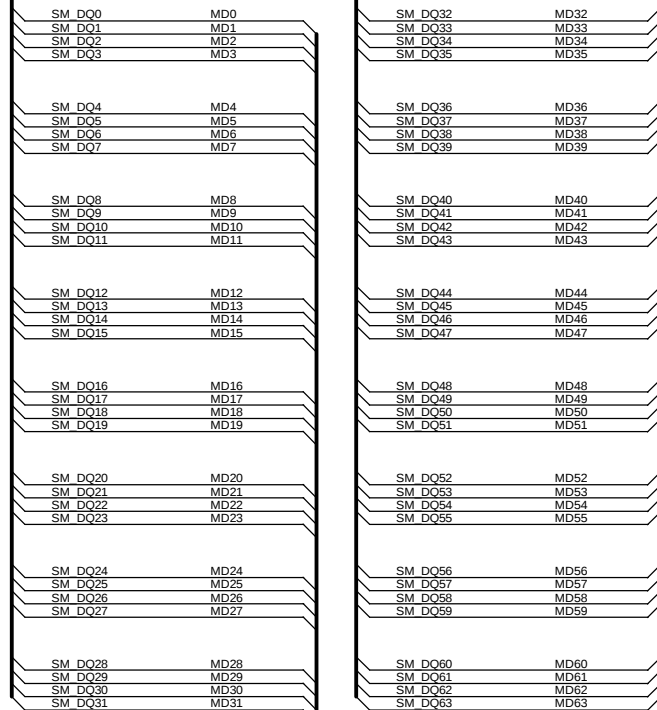


SEL2	SEL1	SEL0	CPUCCLKC0[0..2]	CPUCCLKT0[0..2]
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1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

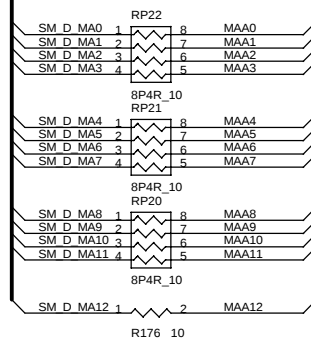
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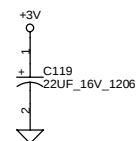
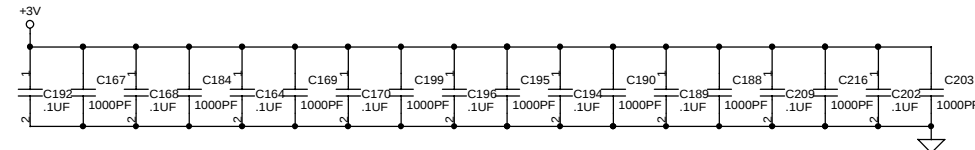
9,14 SM_DQ[0..63] MD[0..63] 9,14



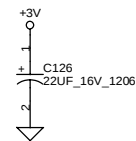
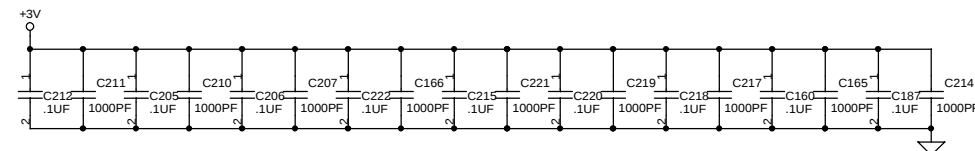
9 SM_D_MA[0..12] MAA[0..12] 14



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .

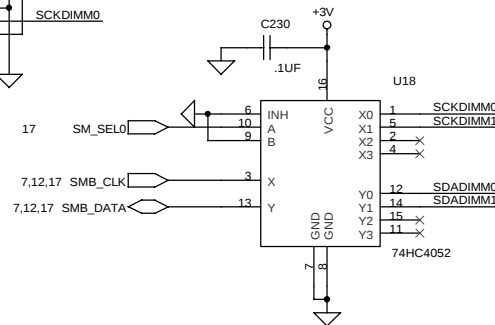
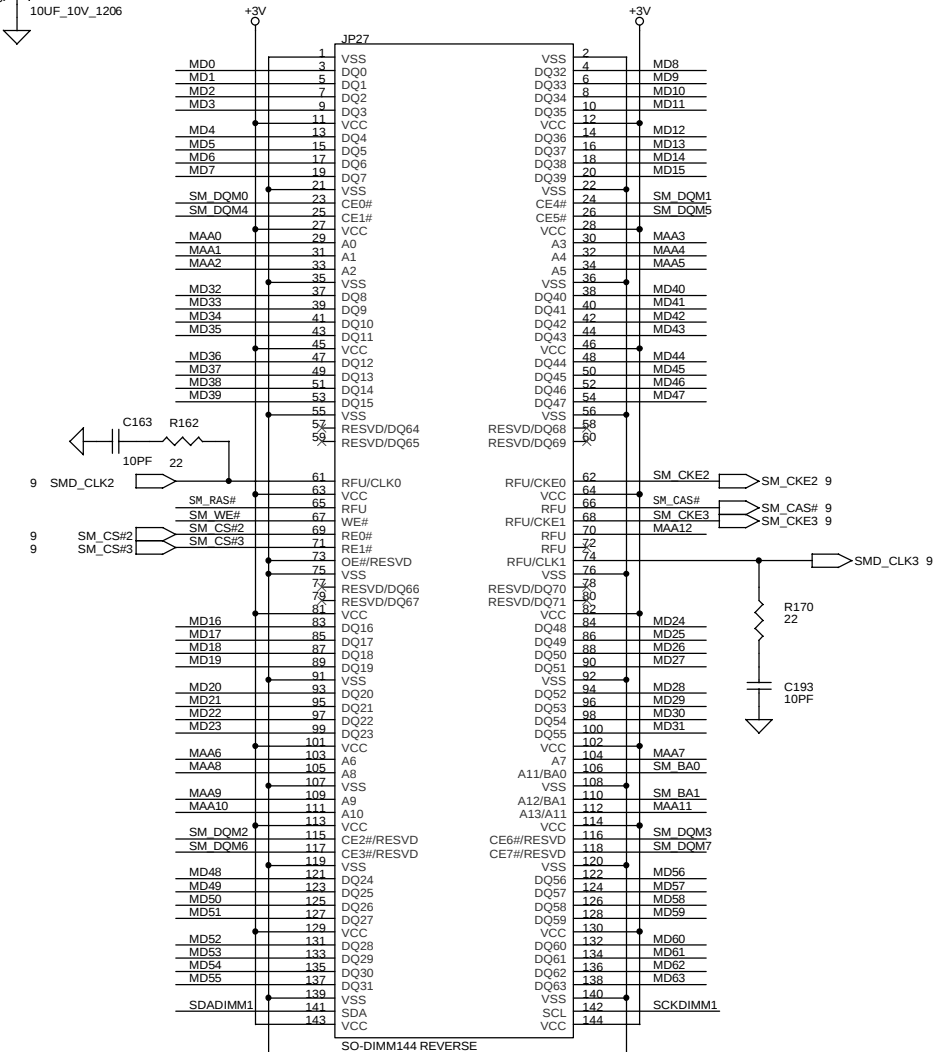


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BANK 0/1

BANK 2/3

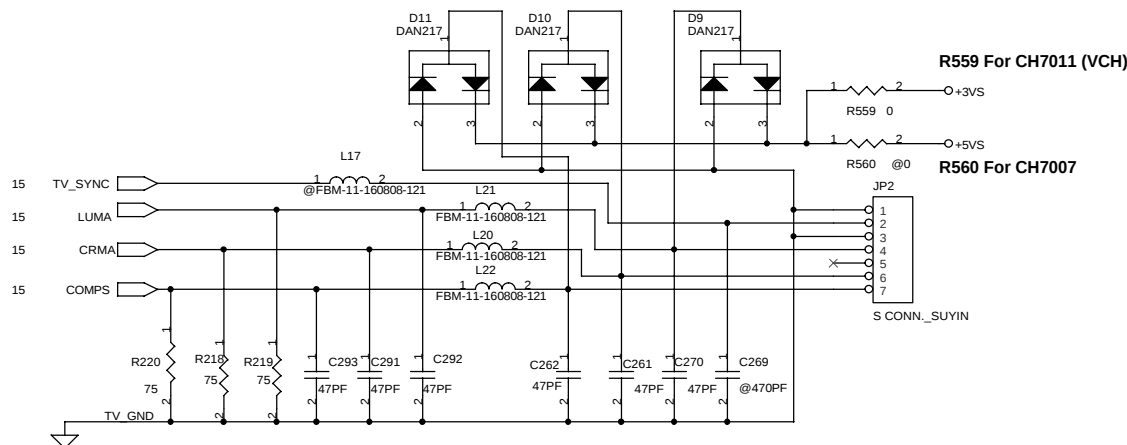


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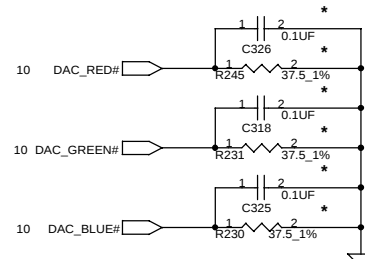
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TV_OUT CONN.

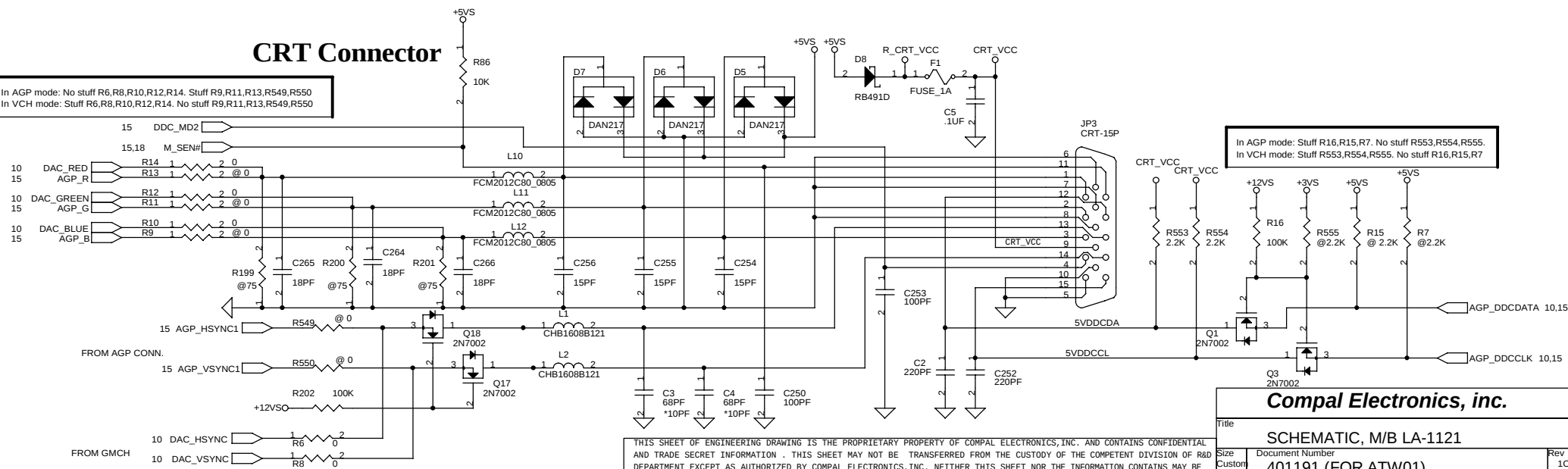


In AGP mode: No stuff C326,R245,C318,R231,C325,R230.
In VCH mode: Stuff C326,R245,C318,R231,C325,R230



CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550



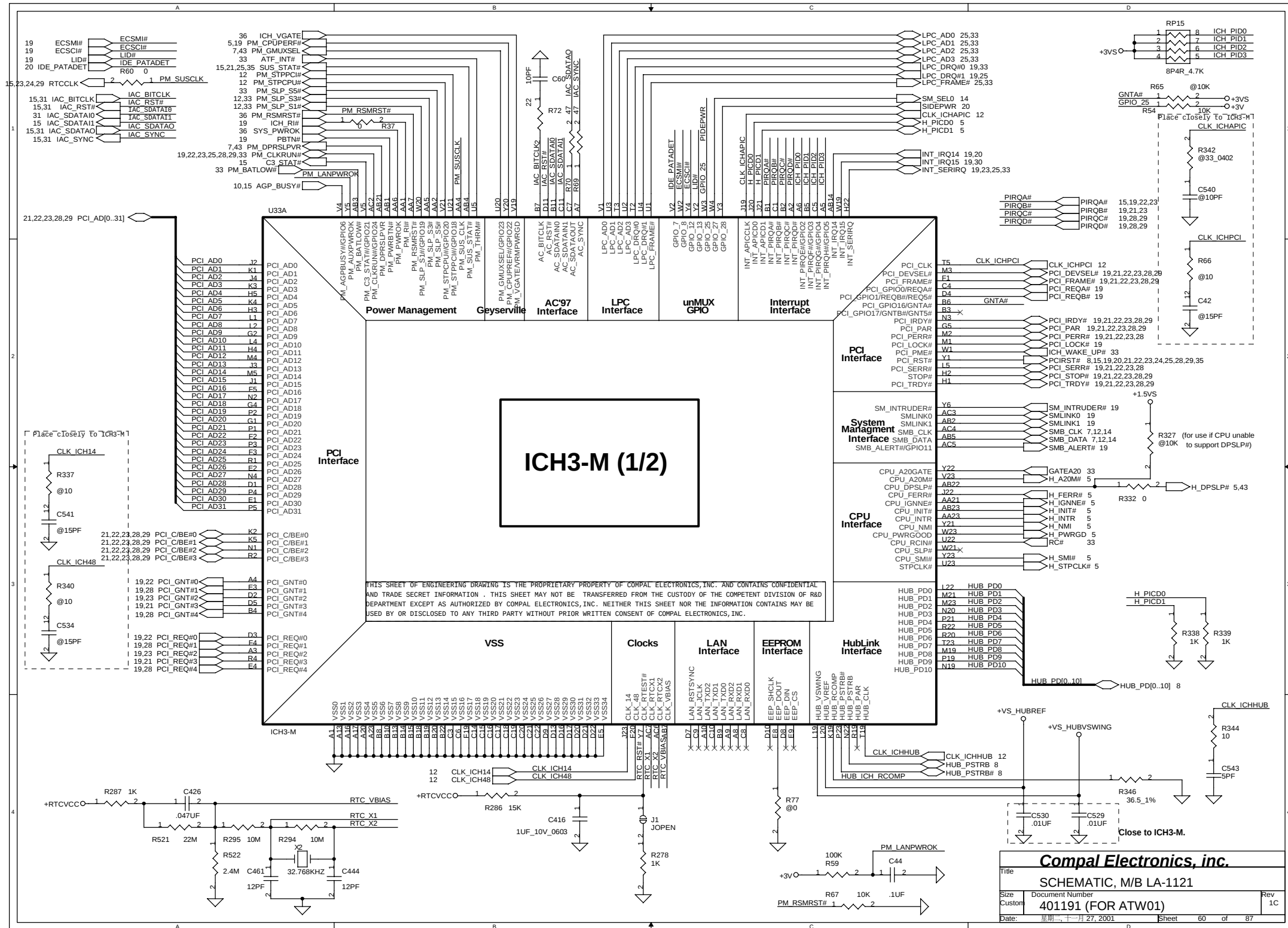
In AGP mode: Stuff R16,R15,R7. No stuff R553,R554,R555.
In VCH mode: Stuff R553,R554,R555. No stuff R16,R15,R7

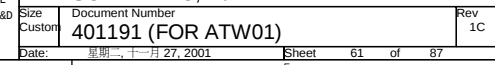
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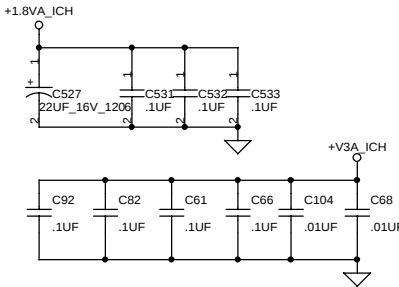
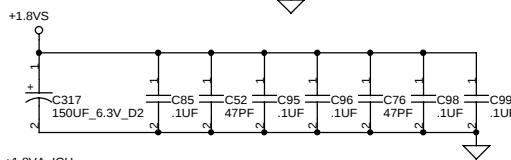
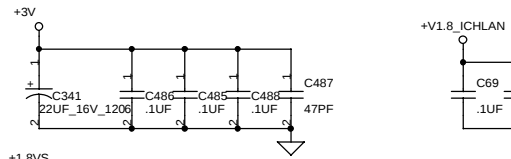
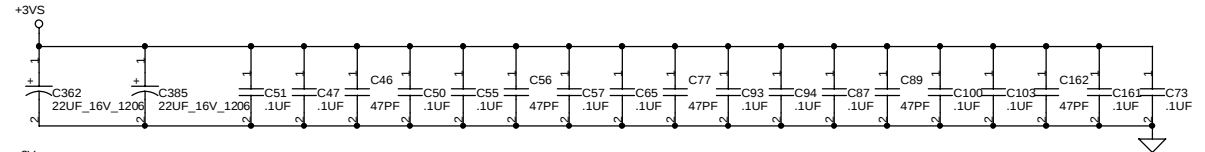
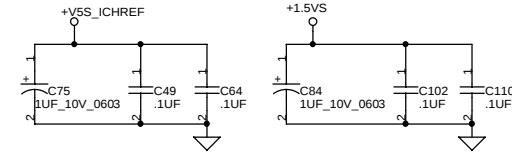
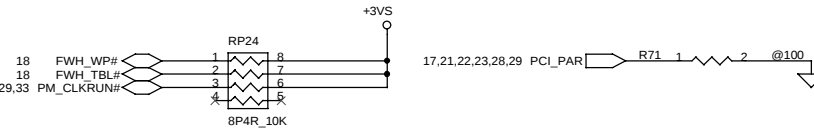
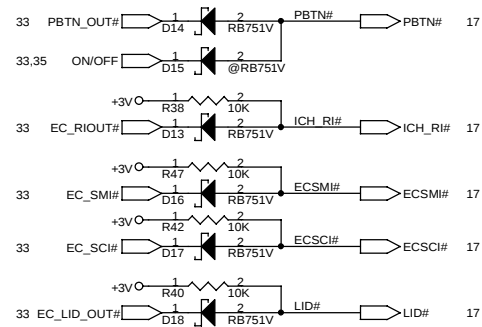
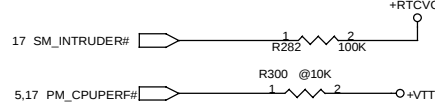
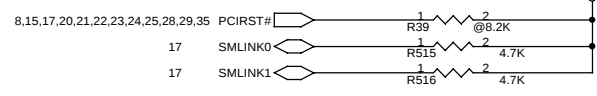
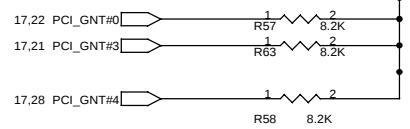
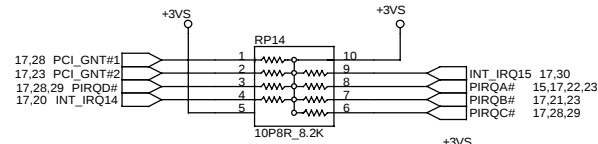
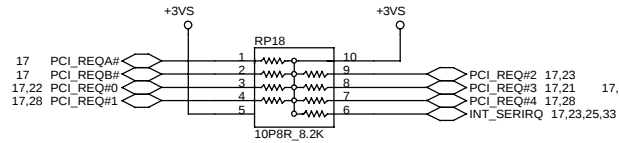
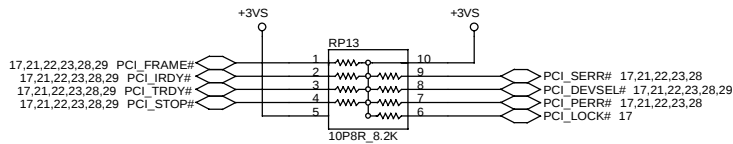
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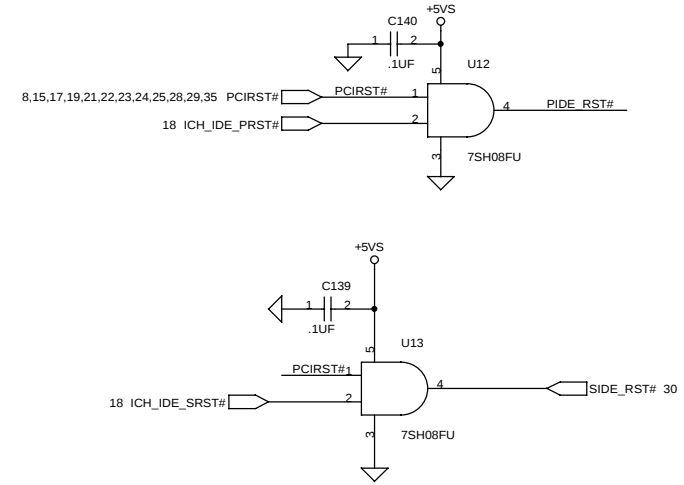
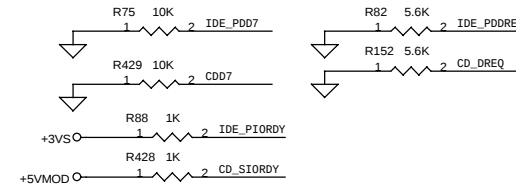
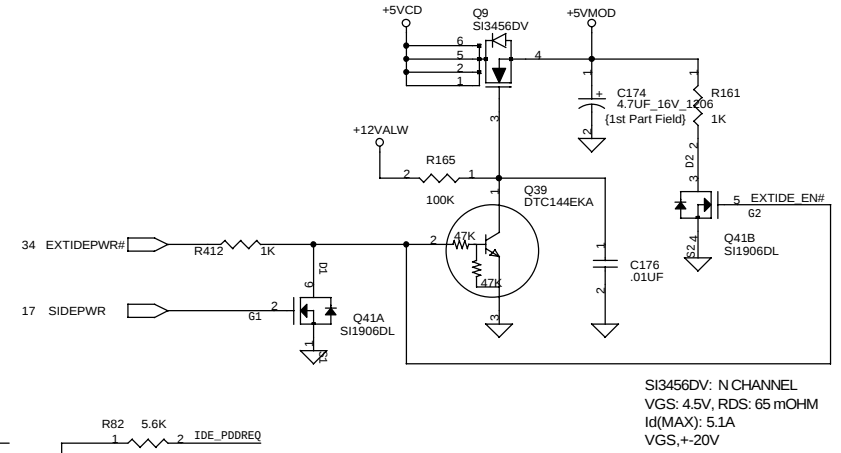
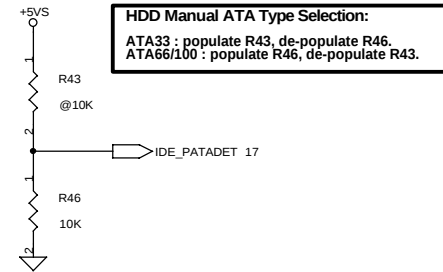
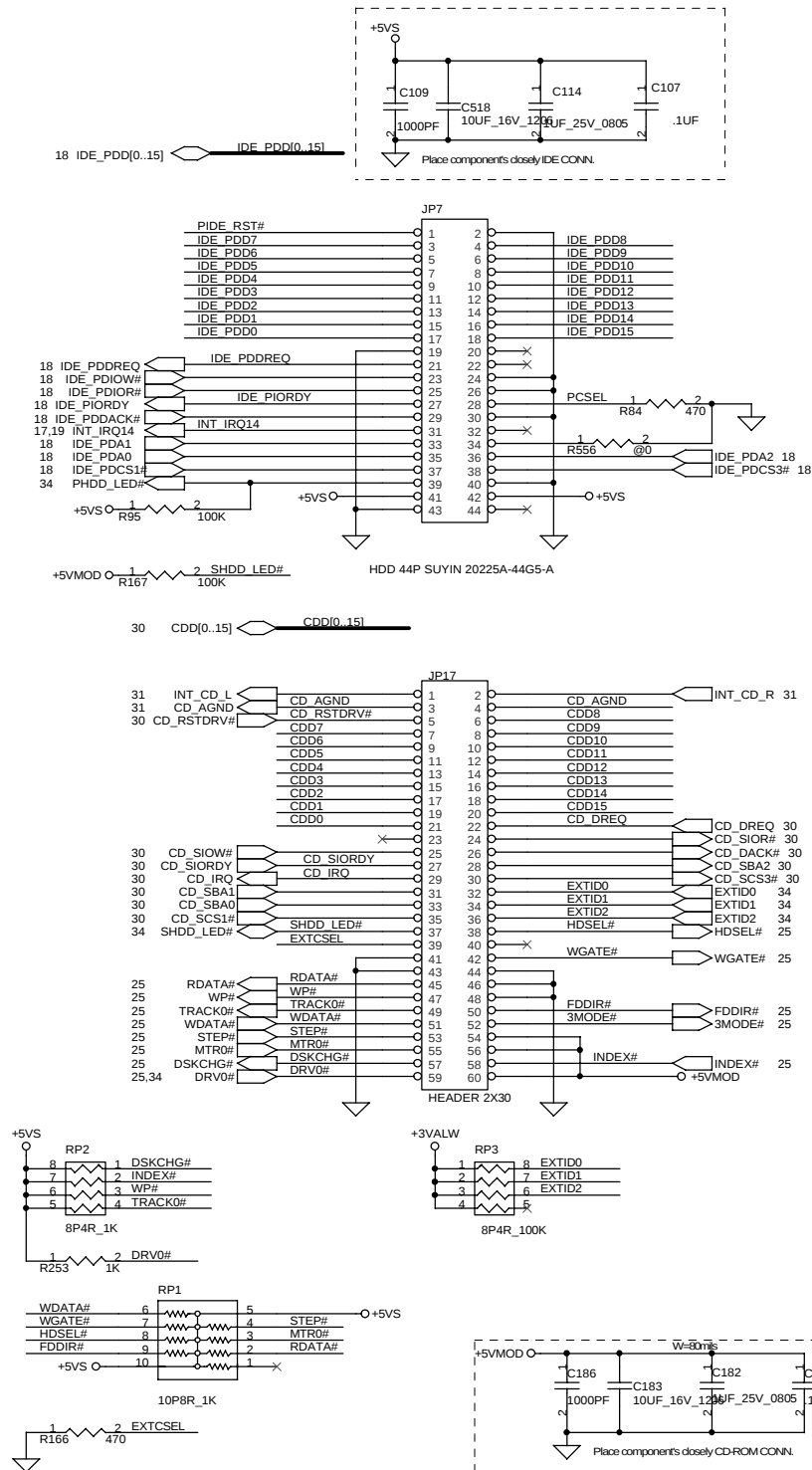
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IDE,CD-ROM Module CONN.



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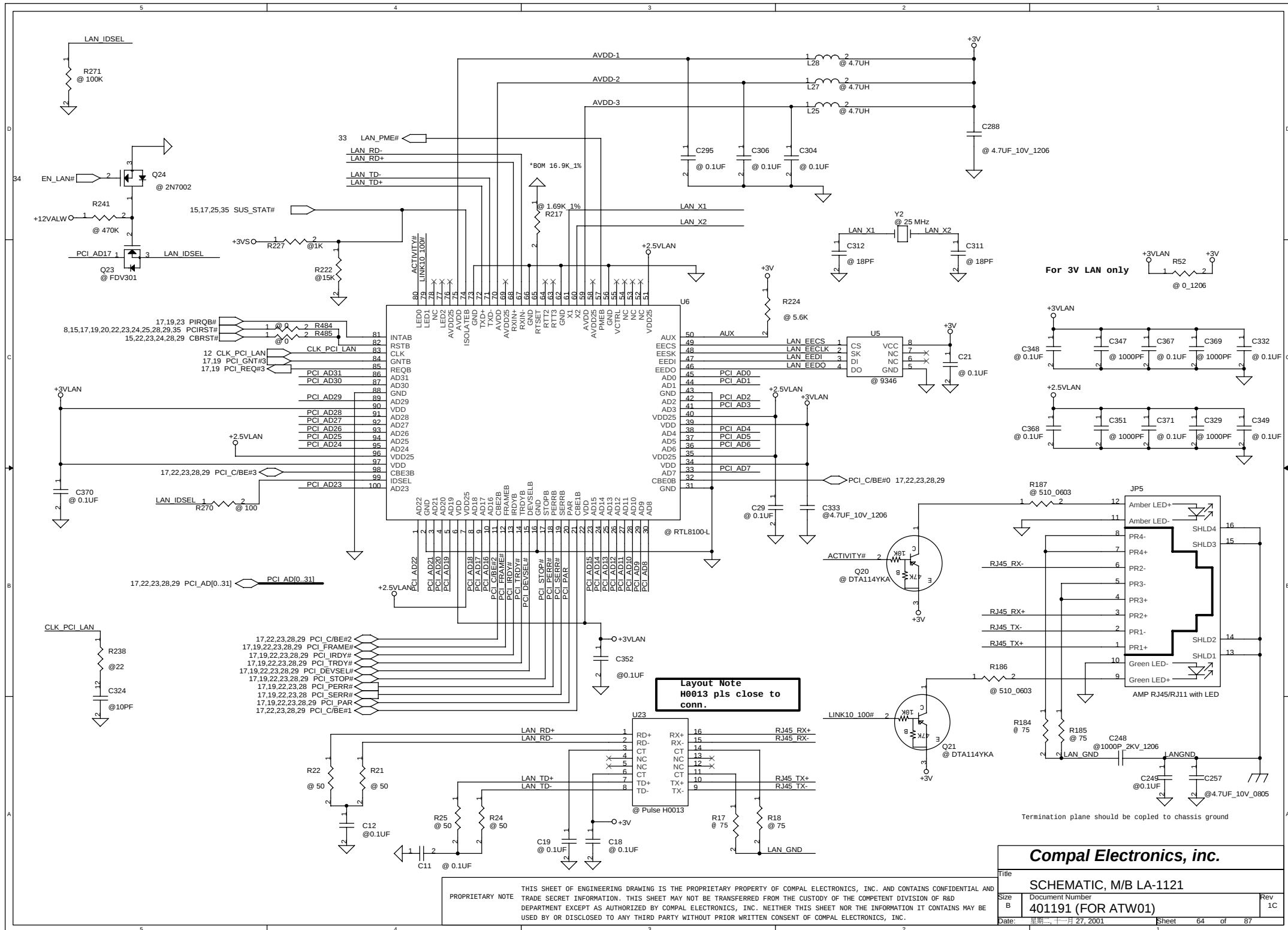
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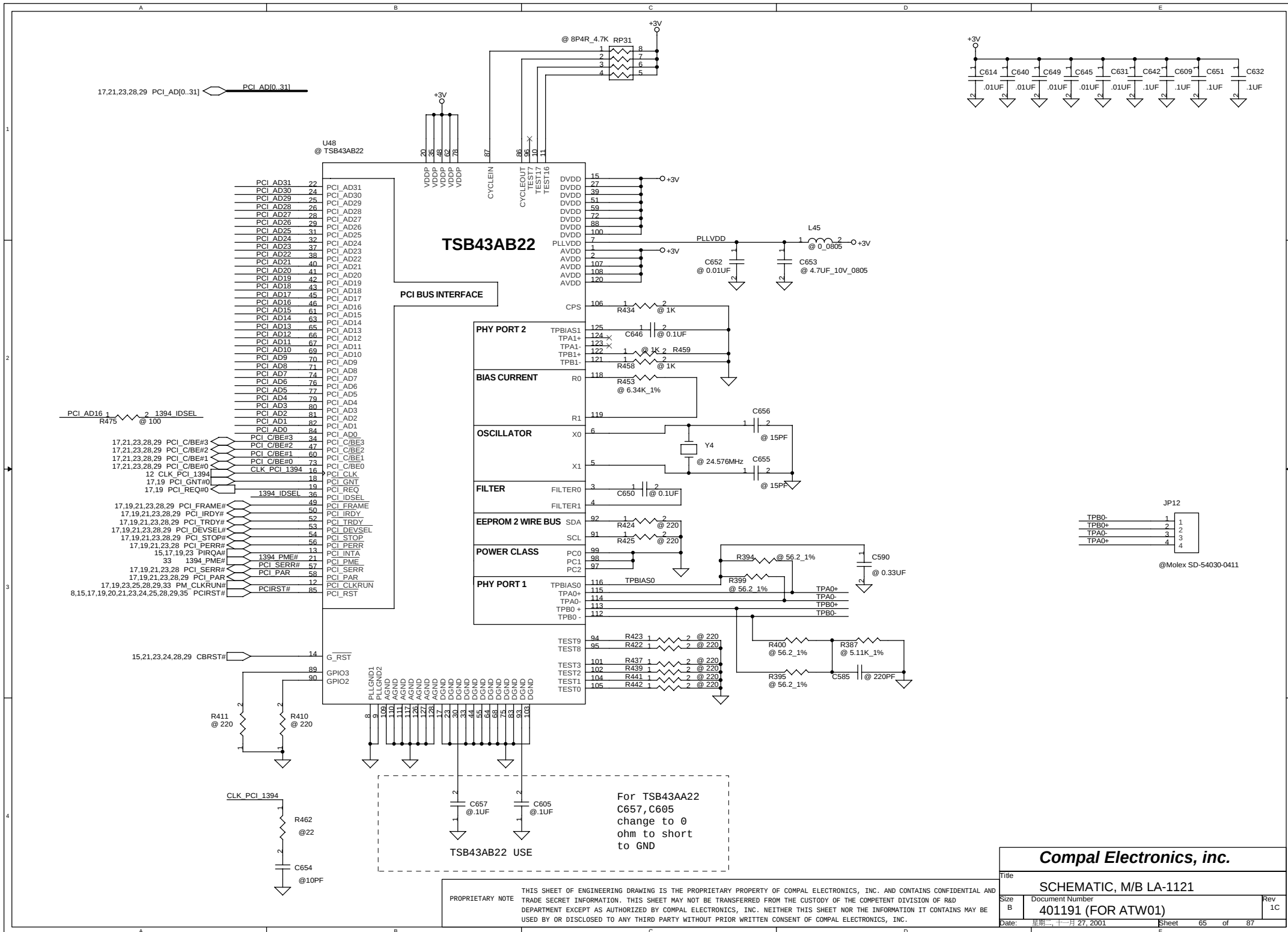
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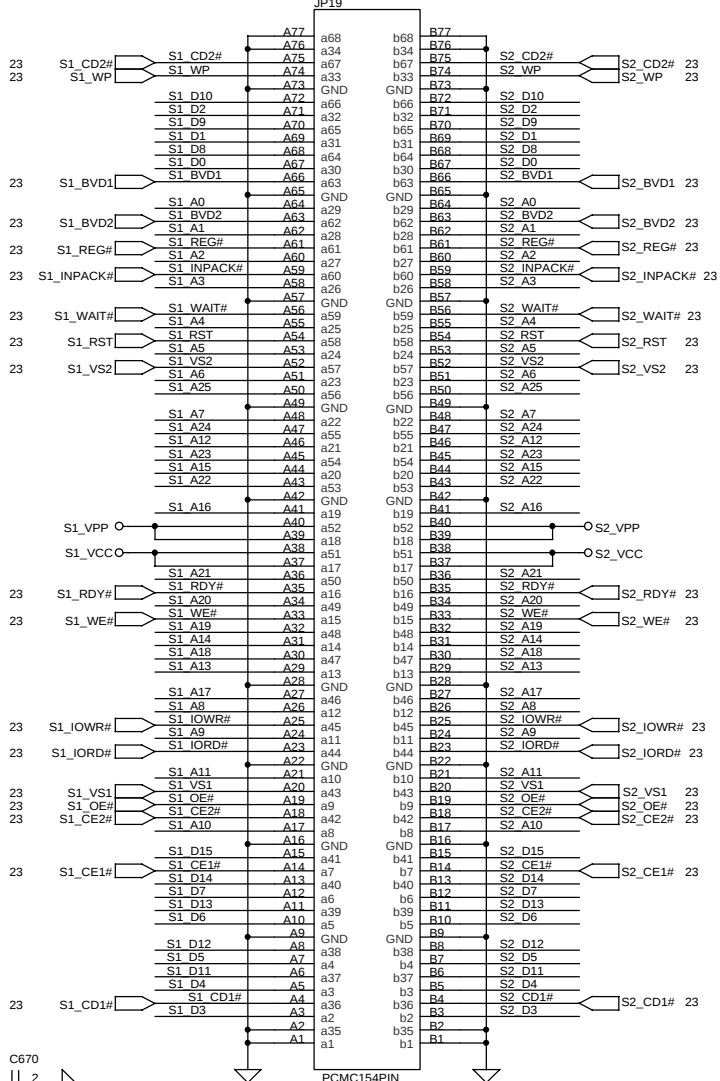
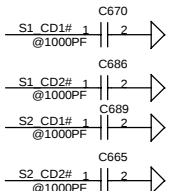
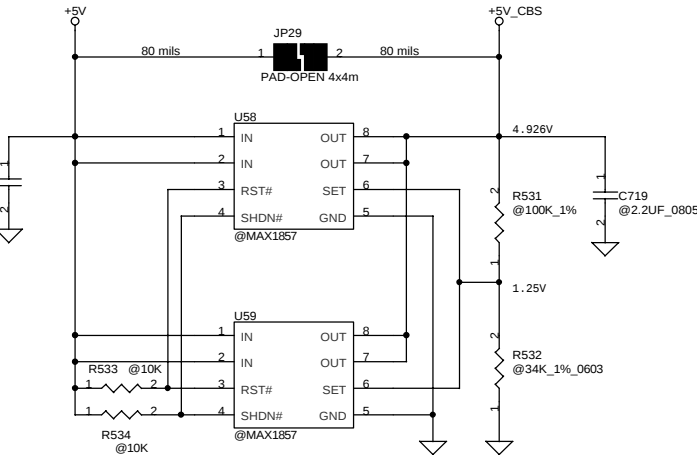
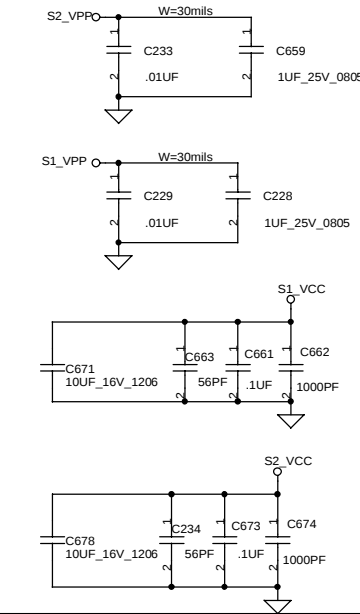
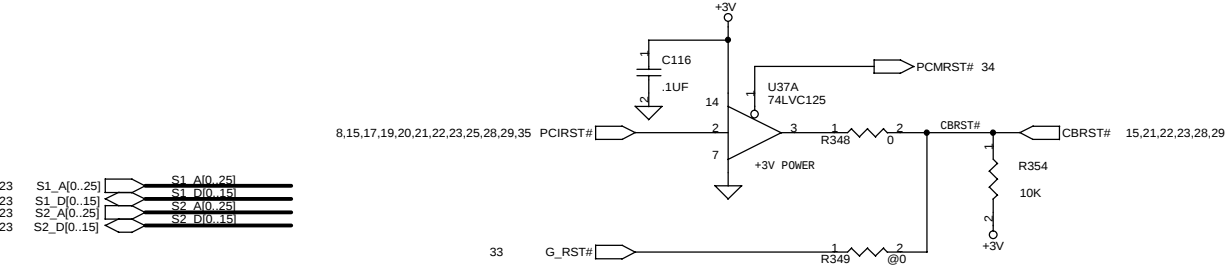
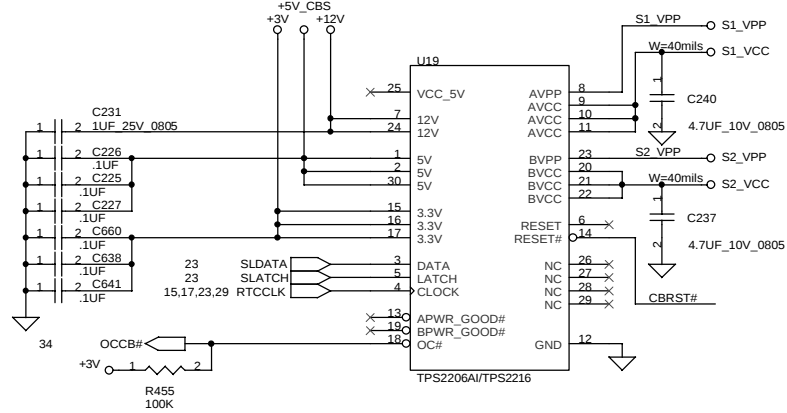
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PCMCIA POWER CTRL.

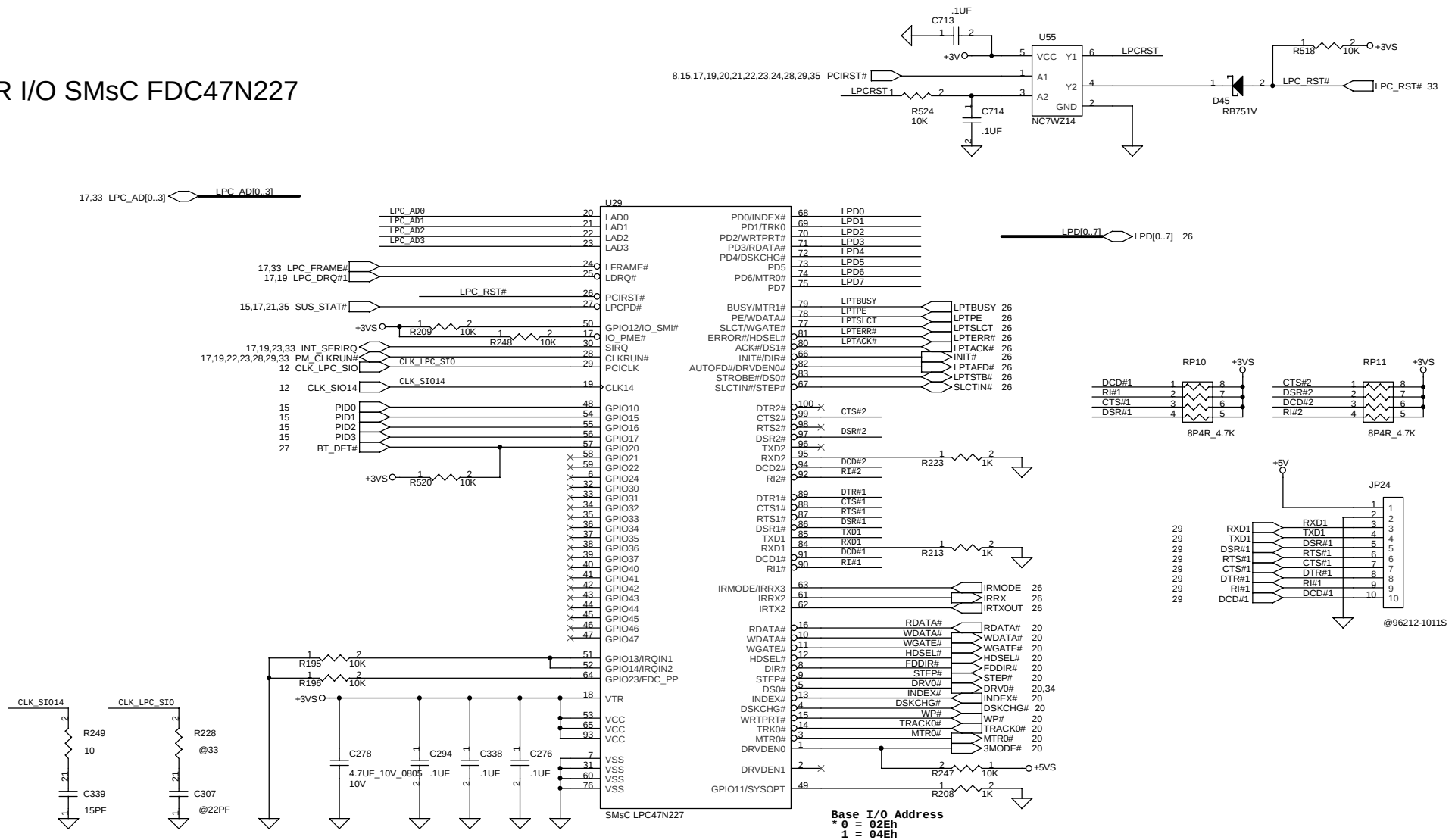
CARDBUS
SOCKET



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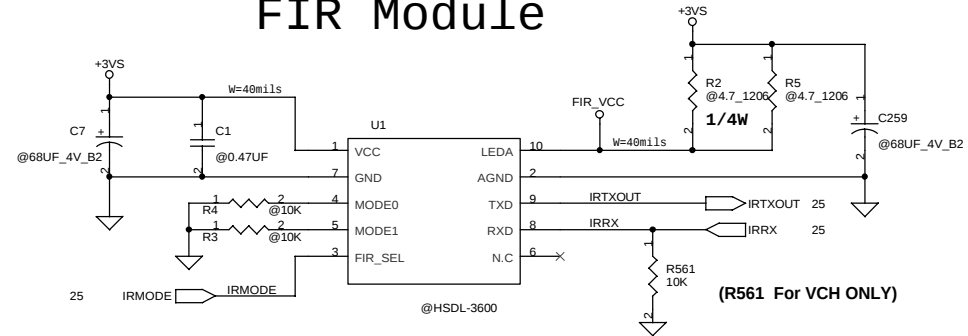
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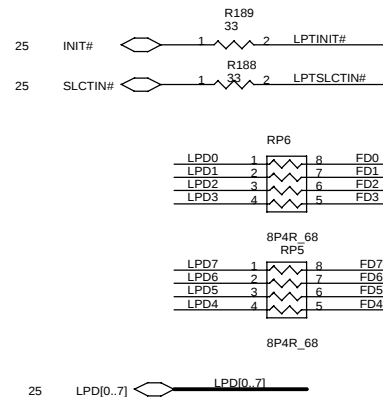
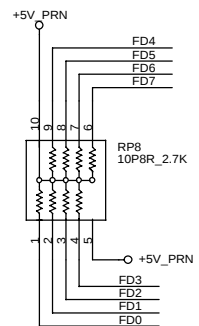
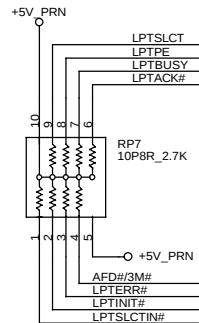
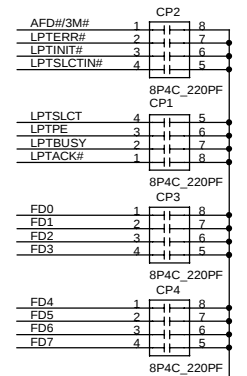
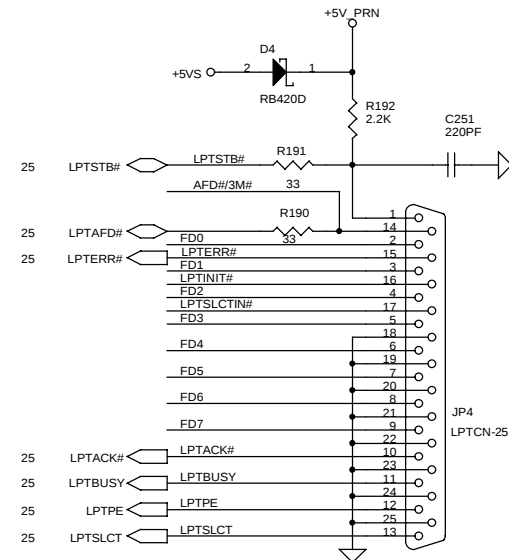
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FIR Module



The component's most place
cloely IRDA MODULE.

PARALLEL PORT

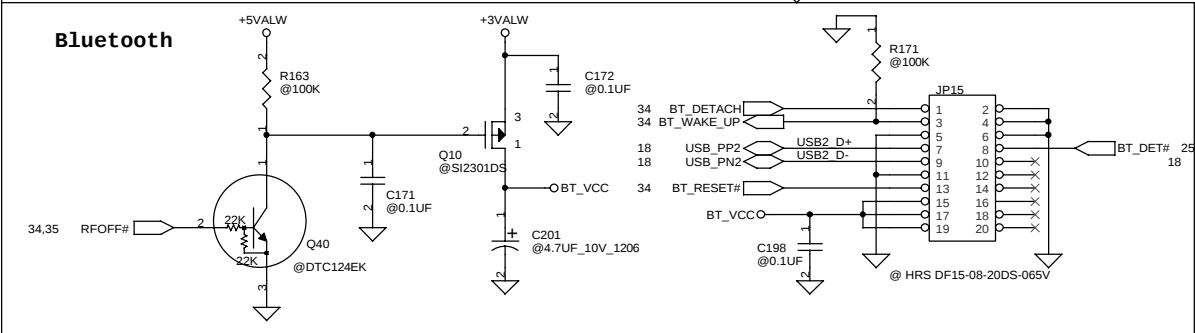


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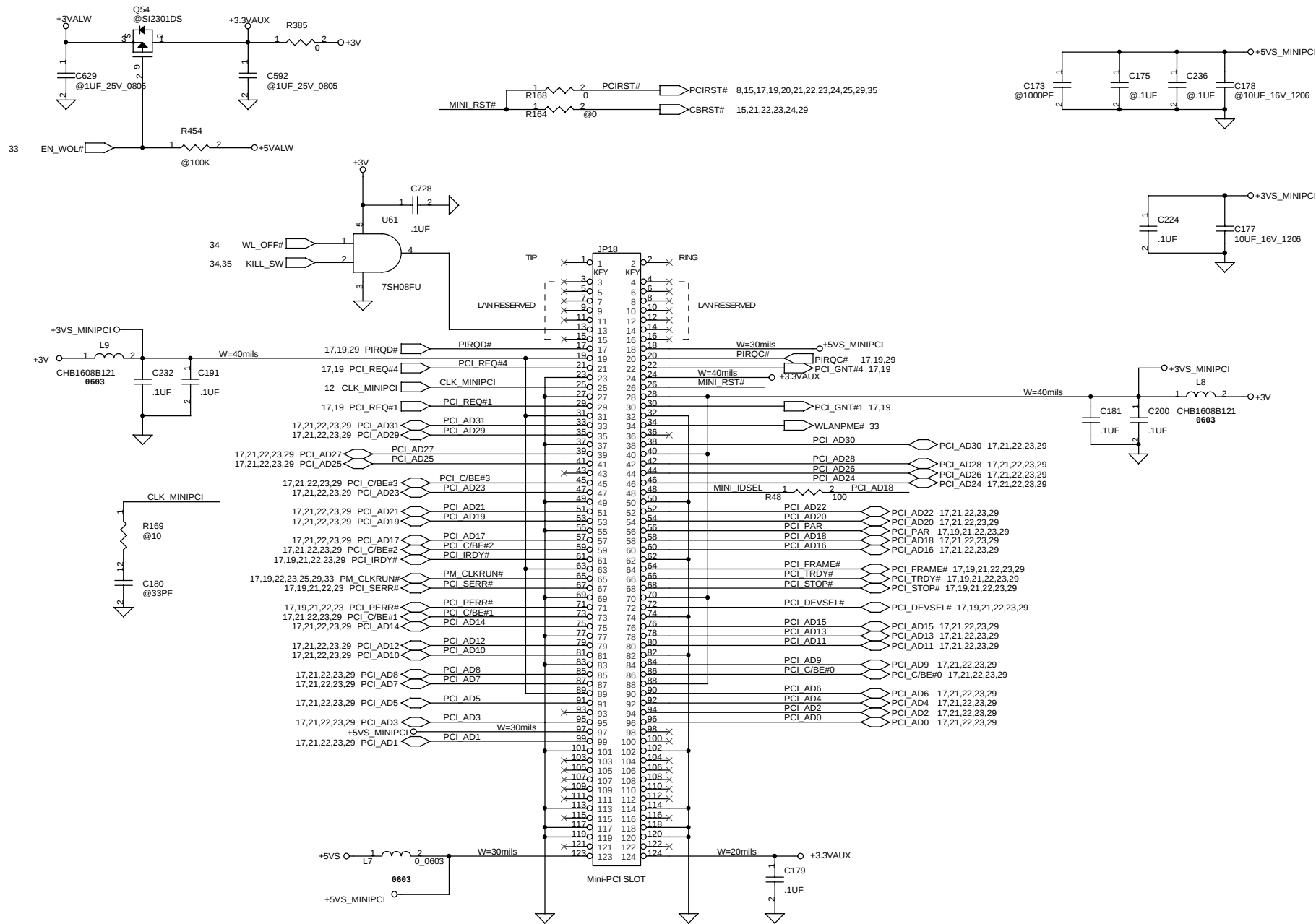
The schematic diagram illustrates the USB interface circuit. It features a USB_VCCA power supply connected to a POLYSWITCH_0.75A. A USB_OC#0 pin is connected to a network of resistors (R353, R355) and capacitors (C208, C153, C560). The circuit also includes a USB connector (JP9) and various passive components like resistors (R353, R355, C208, C153, C560, C720, C721, C535), inductors (L36, L34, L35), and a USB connector (JP9).



Bluetooth

The diagram illustrates the power supply and control circuitry for a Bluetooth module. A +5VALW supply is connected to a 100K resistor (R163) and the base of a BJT transistor (Q40, DTC124EK). The emitter of Q40 is grounded. The collector of Q40 is connected to the base of a MOSFET (Q10, SI2301DS). The gate of Q10 is connected to a +3VALW supply through a 0.1uF capacitor (C172) and to the collector of Q40 through a 22K resistor. The source of Q10 is connected to ground through a 0.1uF capacitor (C171) and to the BT_VCC pin of the Bluetooth module through a 4.7uF capacitor (C201). The Bluetooth module is also connected to pins 34 and 35, labeled RFOFF#.

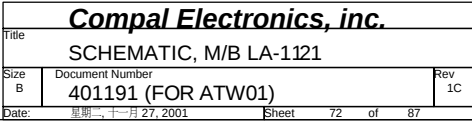
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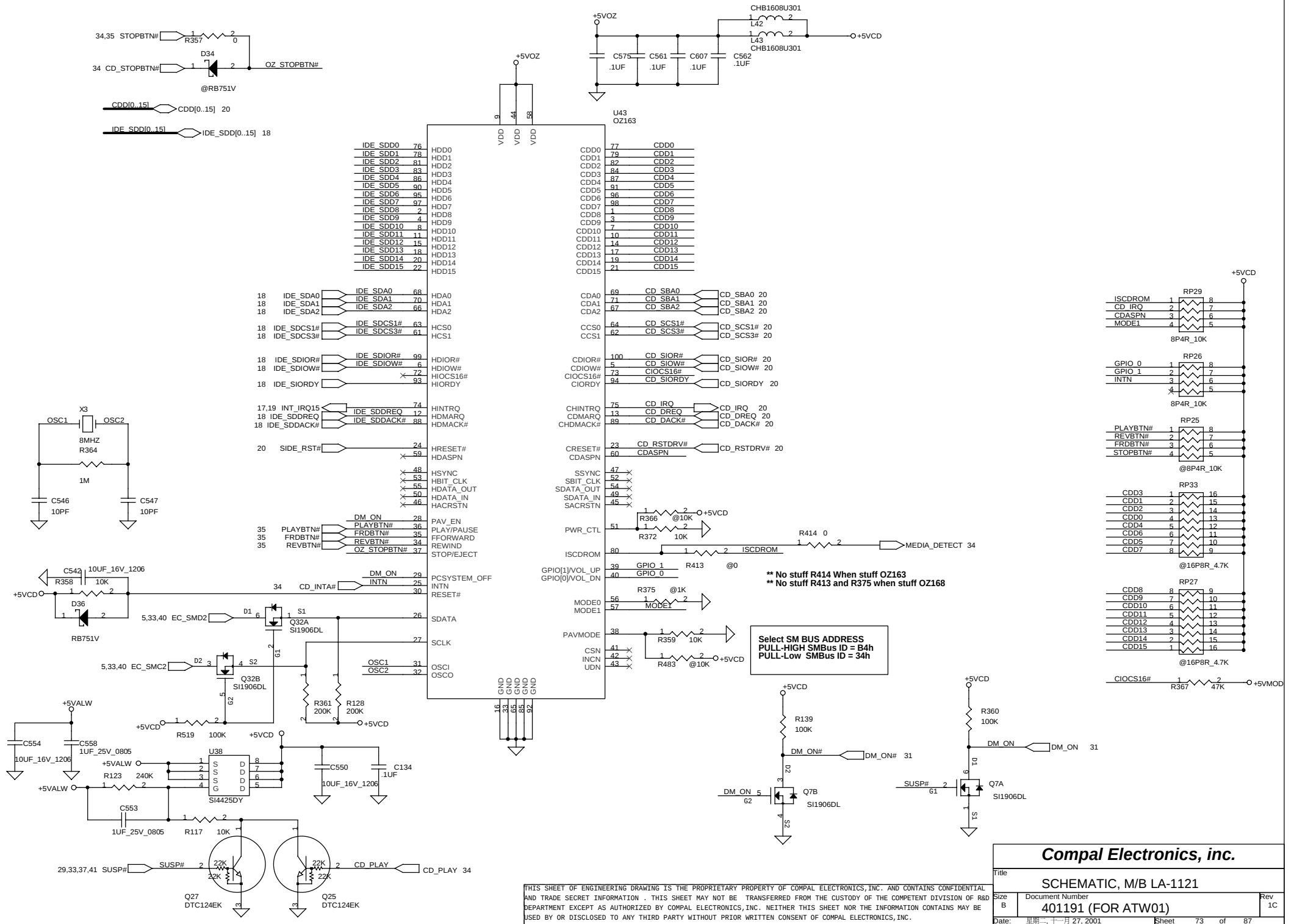


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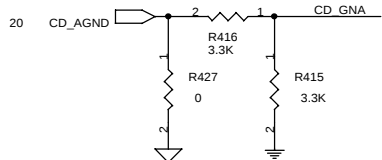
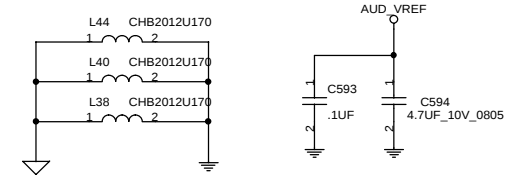
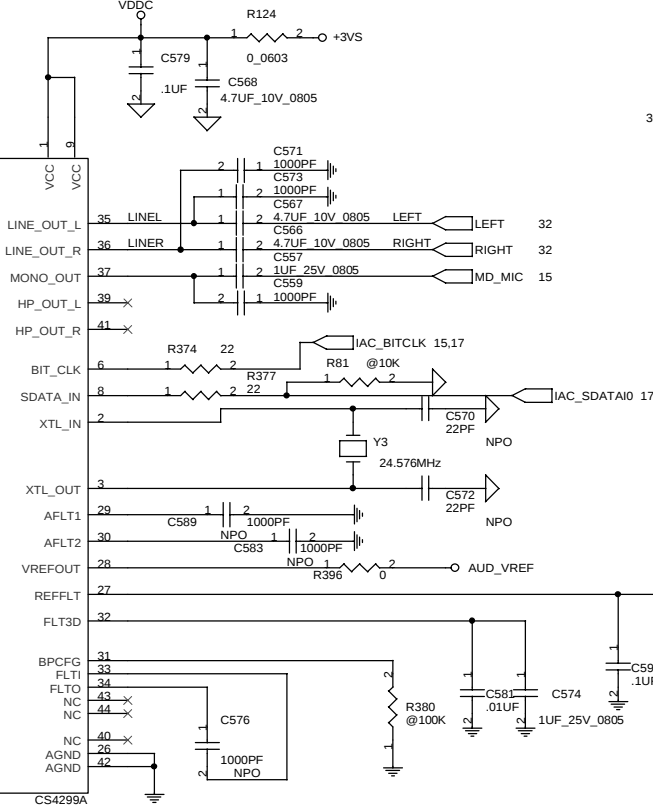
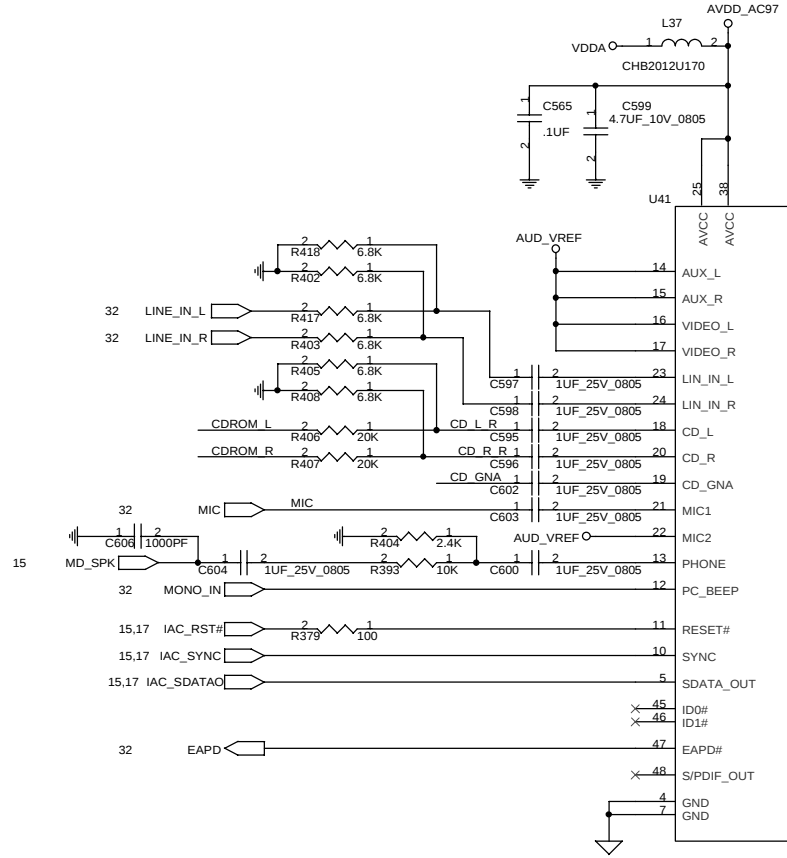
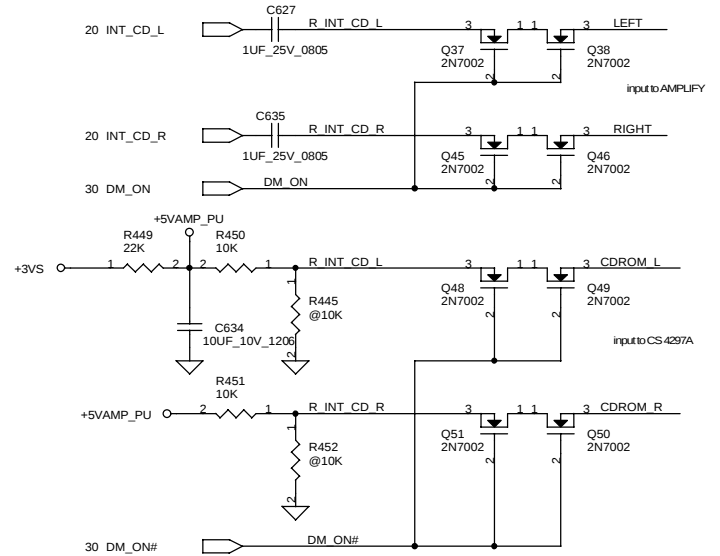
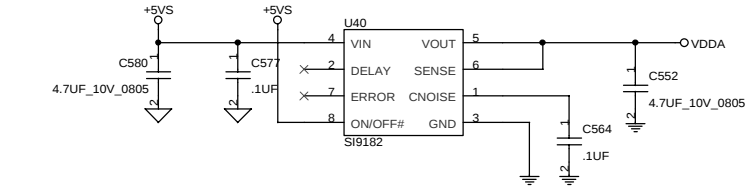
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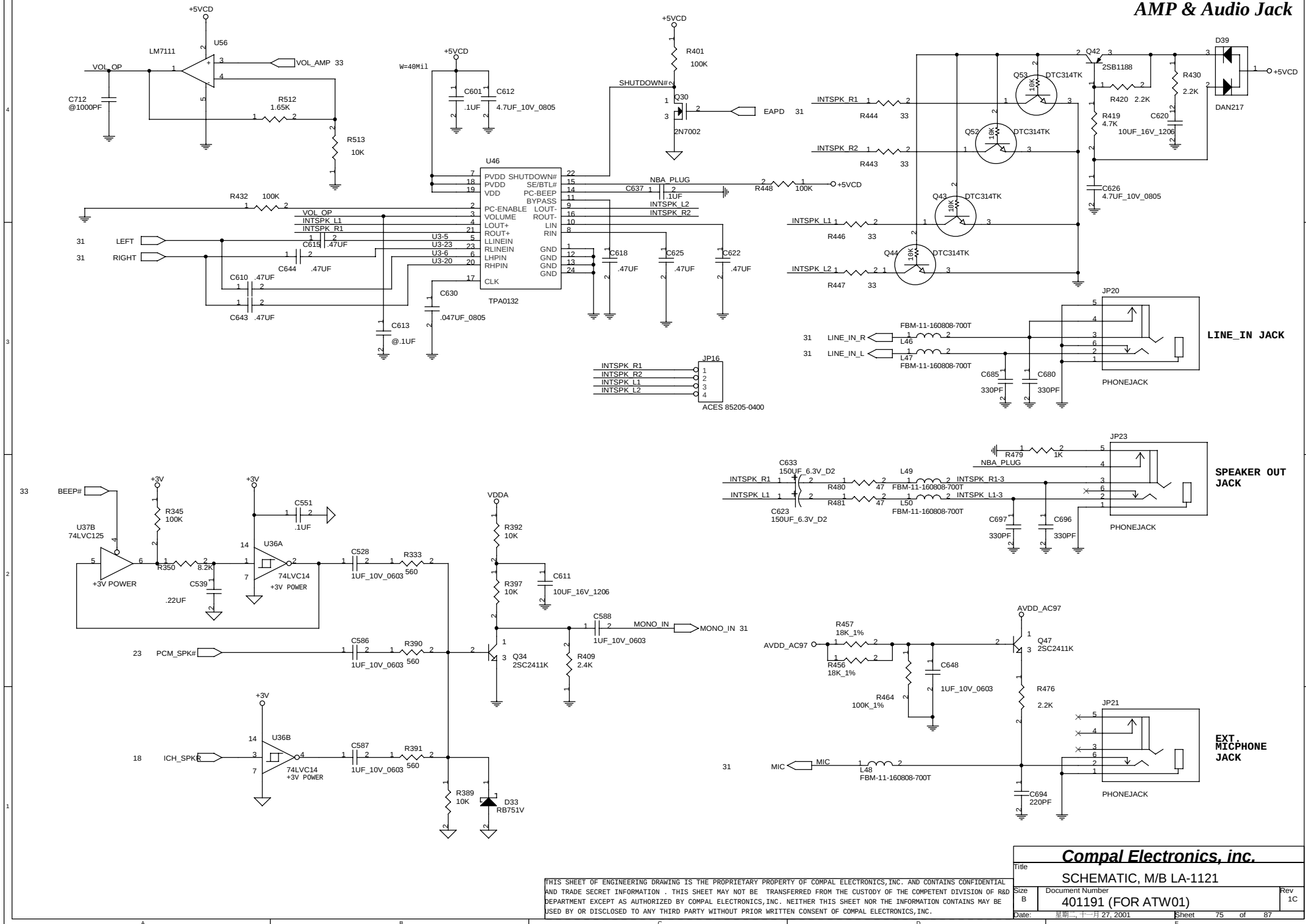
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AMP & Audio Jack

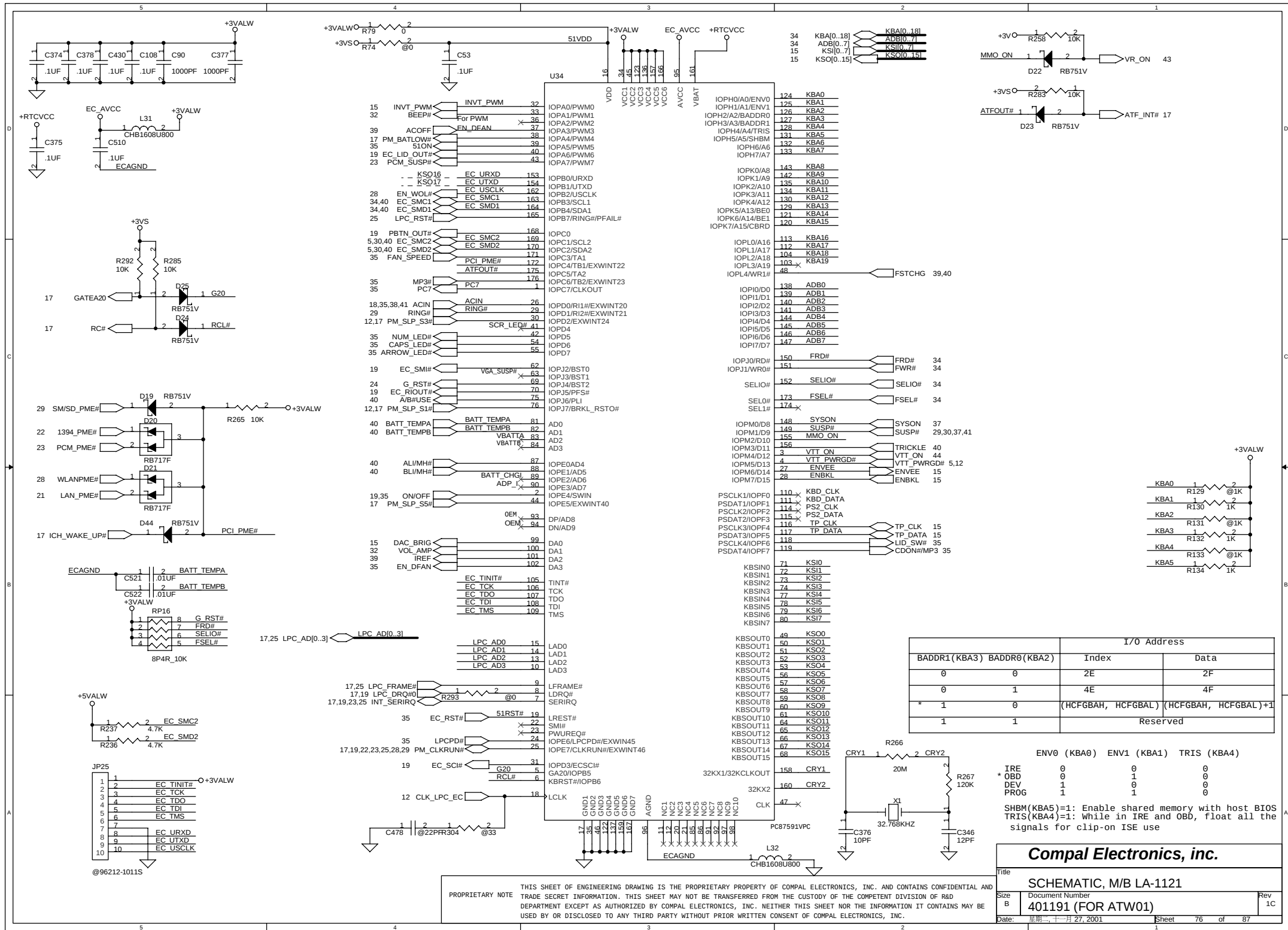


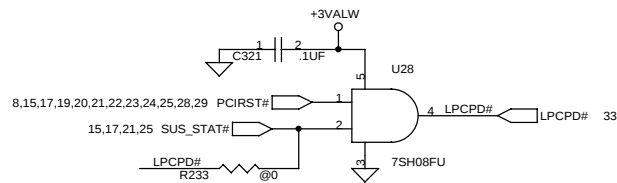
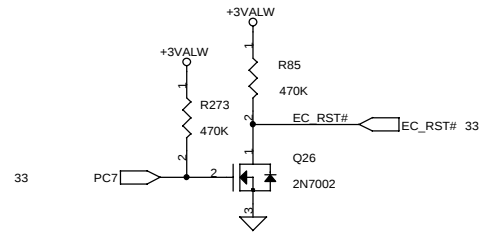
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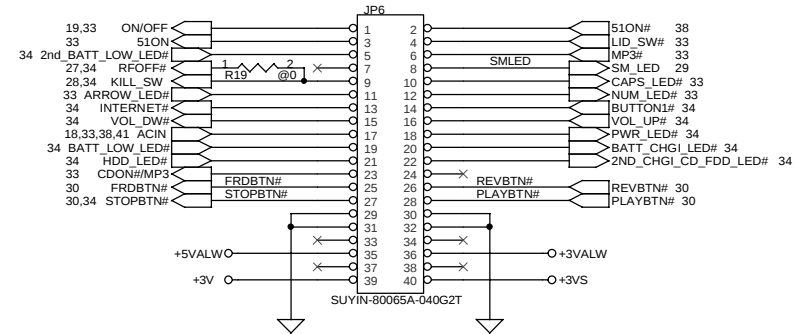
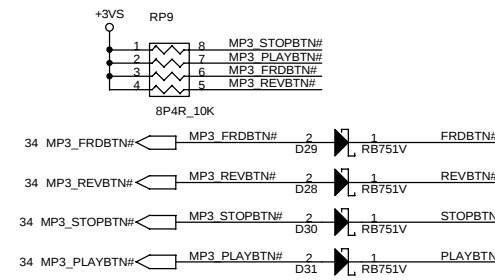
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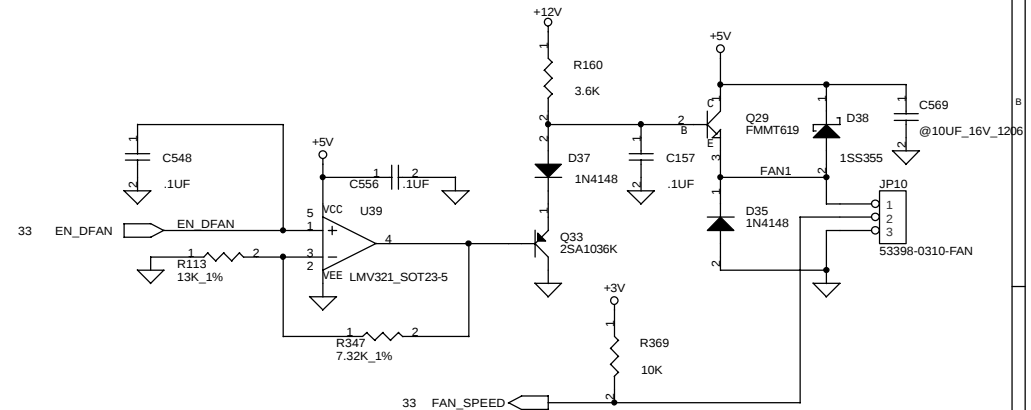




For PC87591 REV 0.A Only



FAN CONN.



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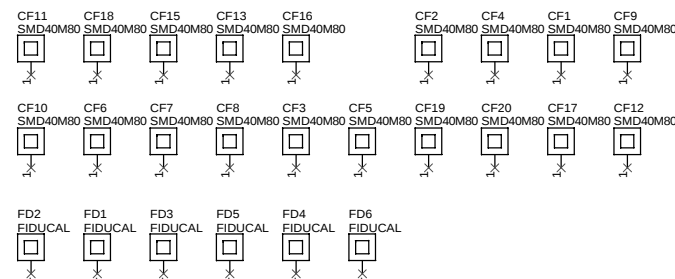
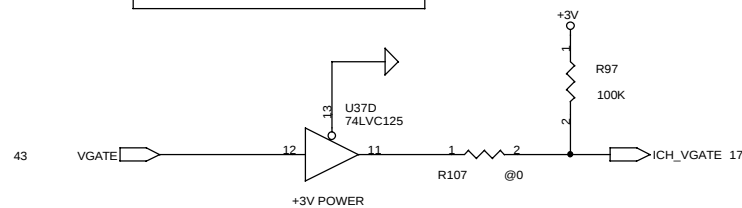
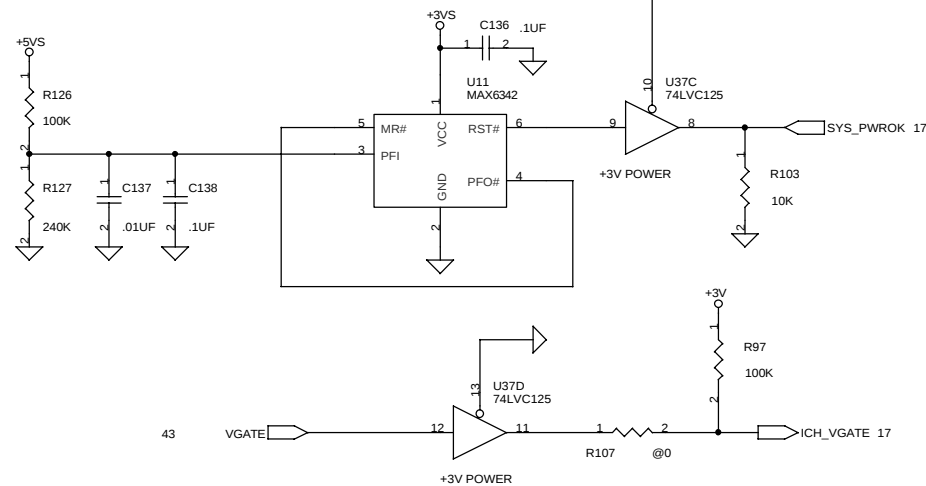
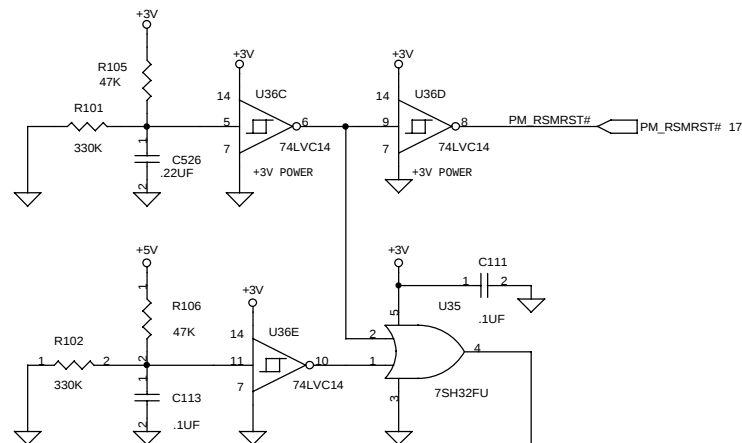
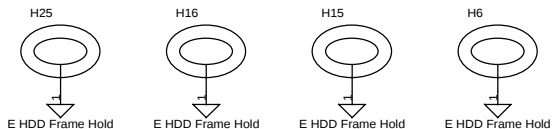
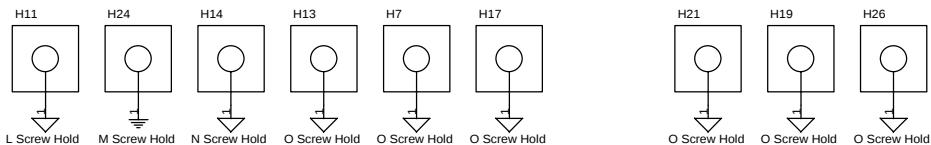
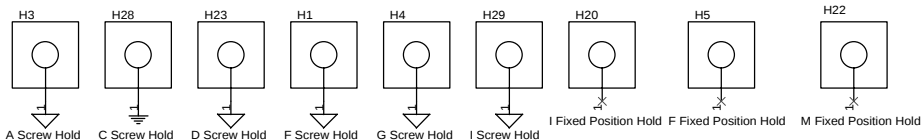
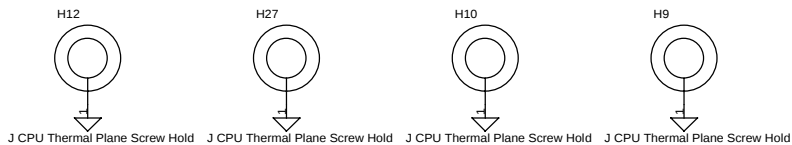
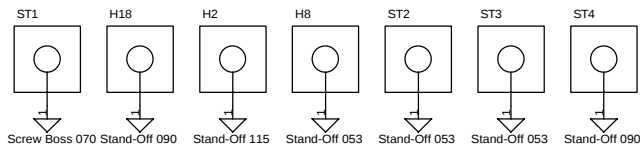
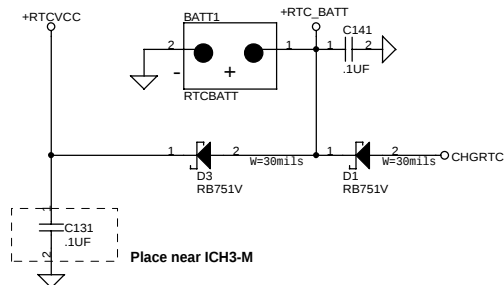
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RTC Batt. Connector

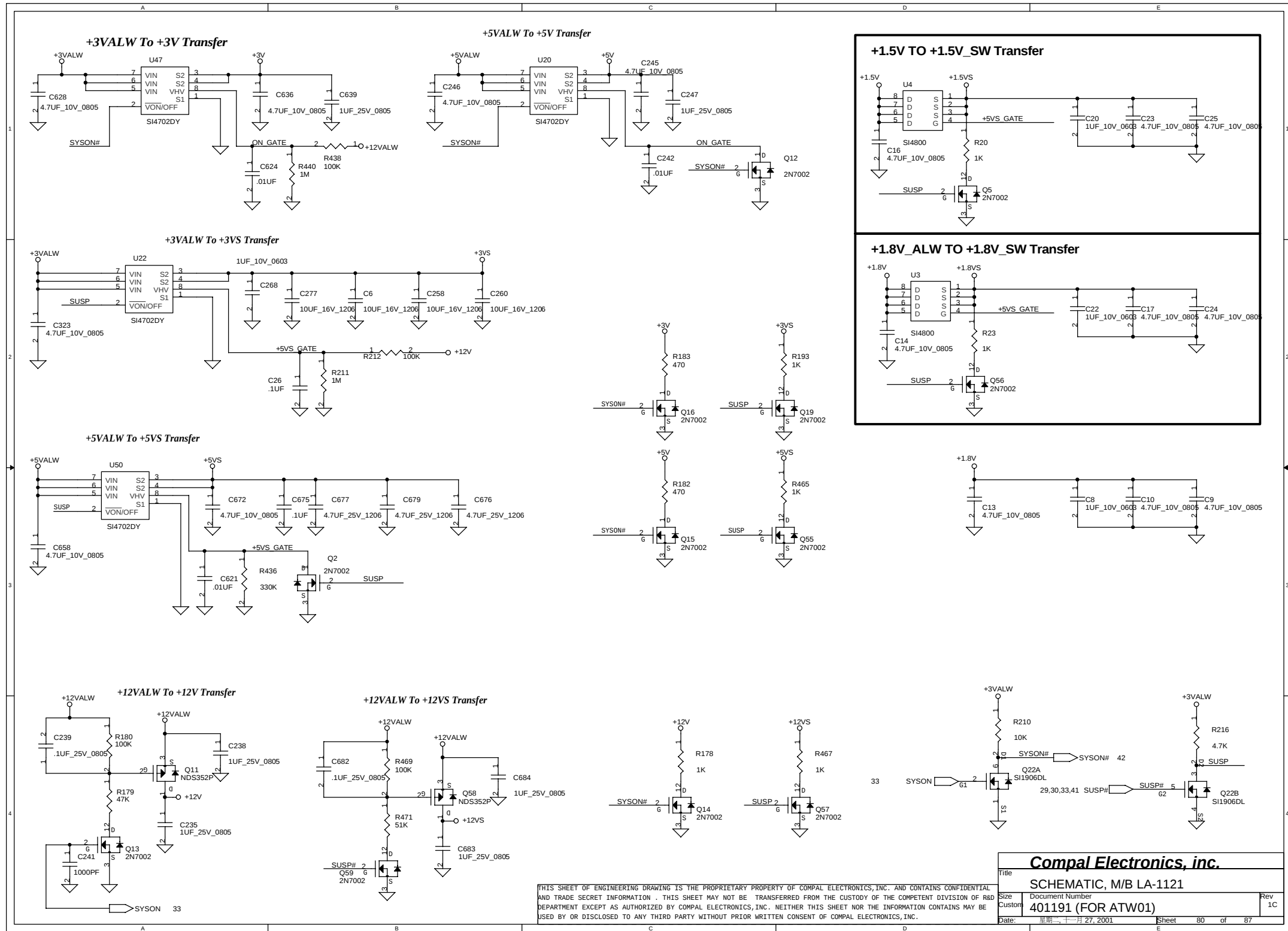


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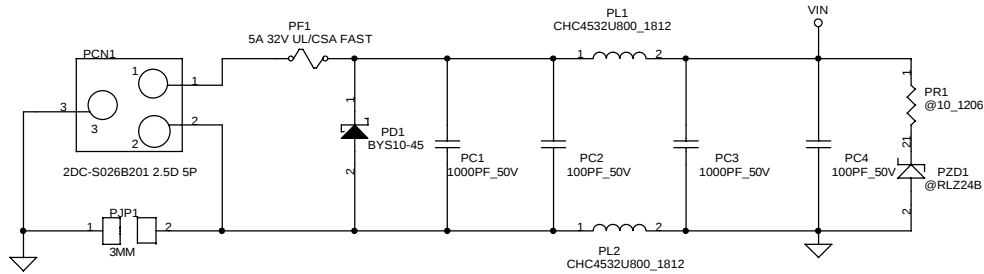
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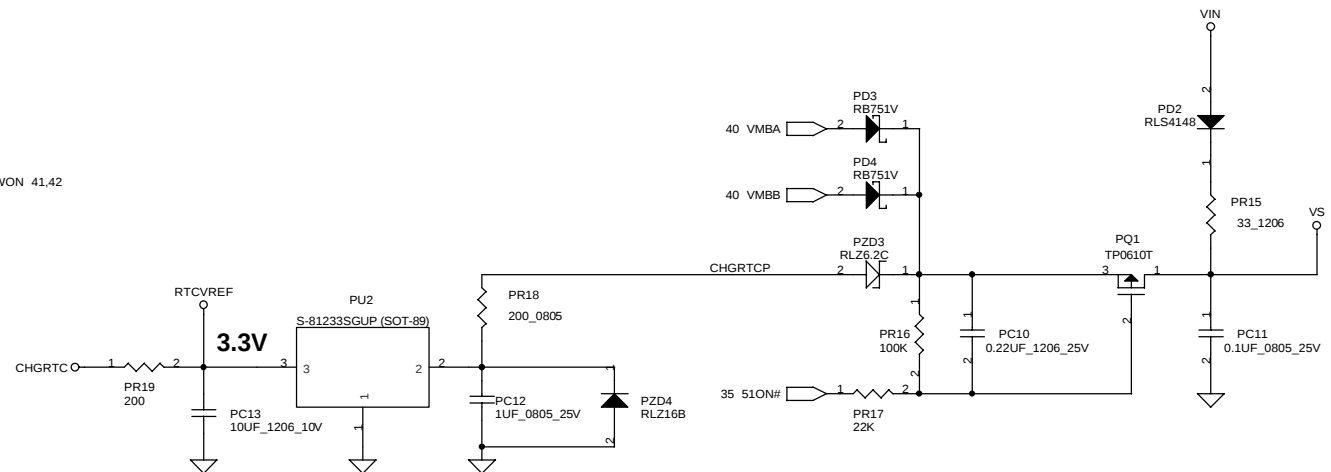
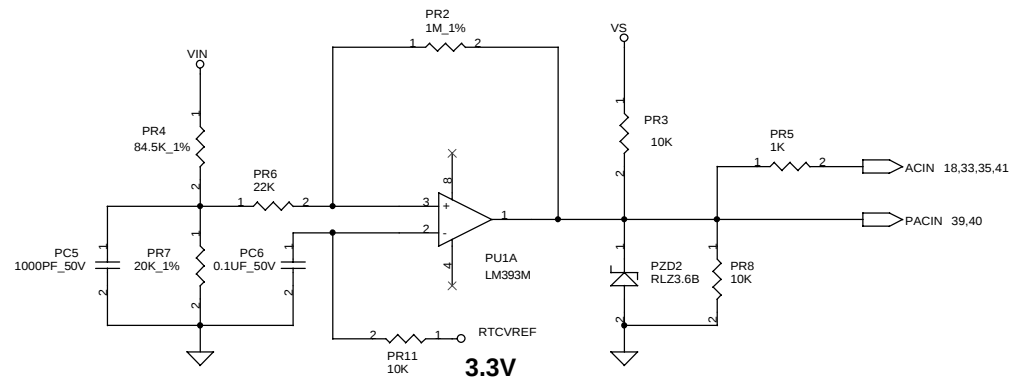
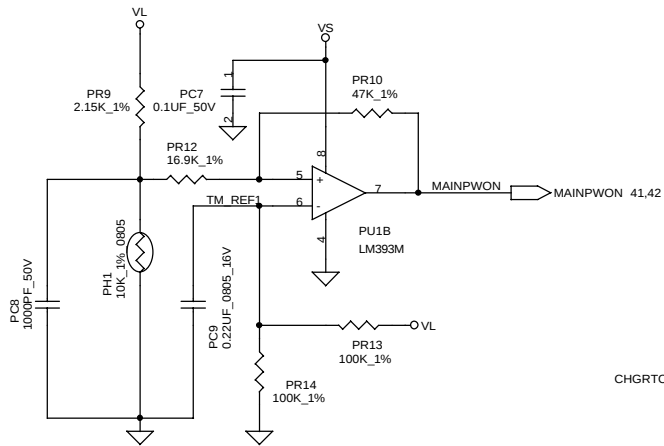


Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038



PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 50(51) degree C



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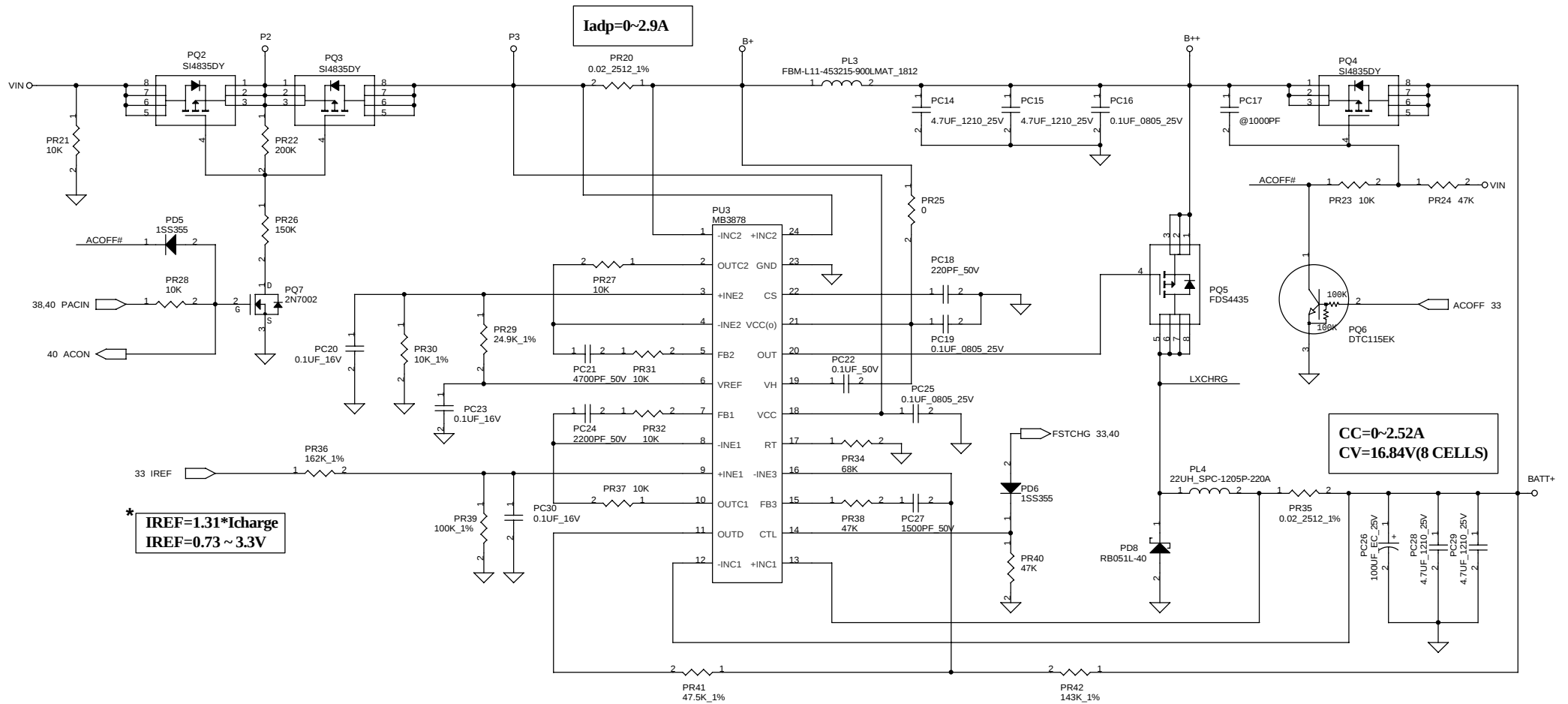
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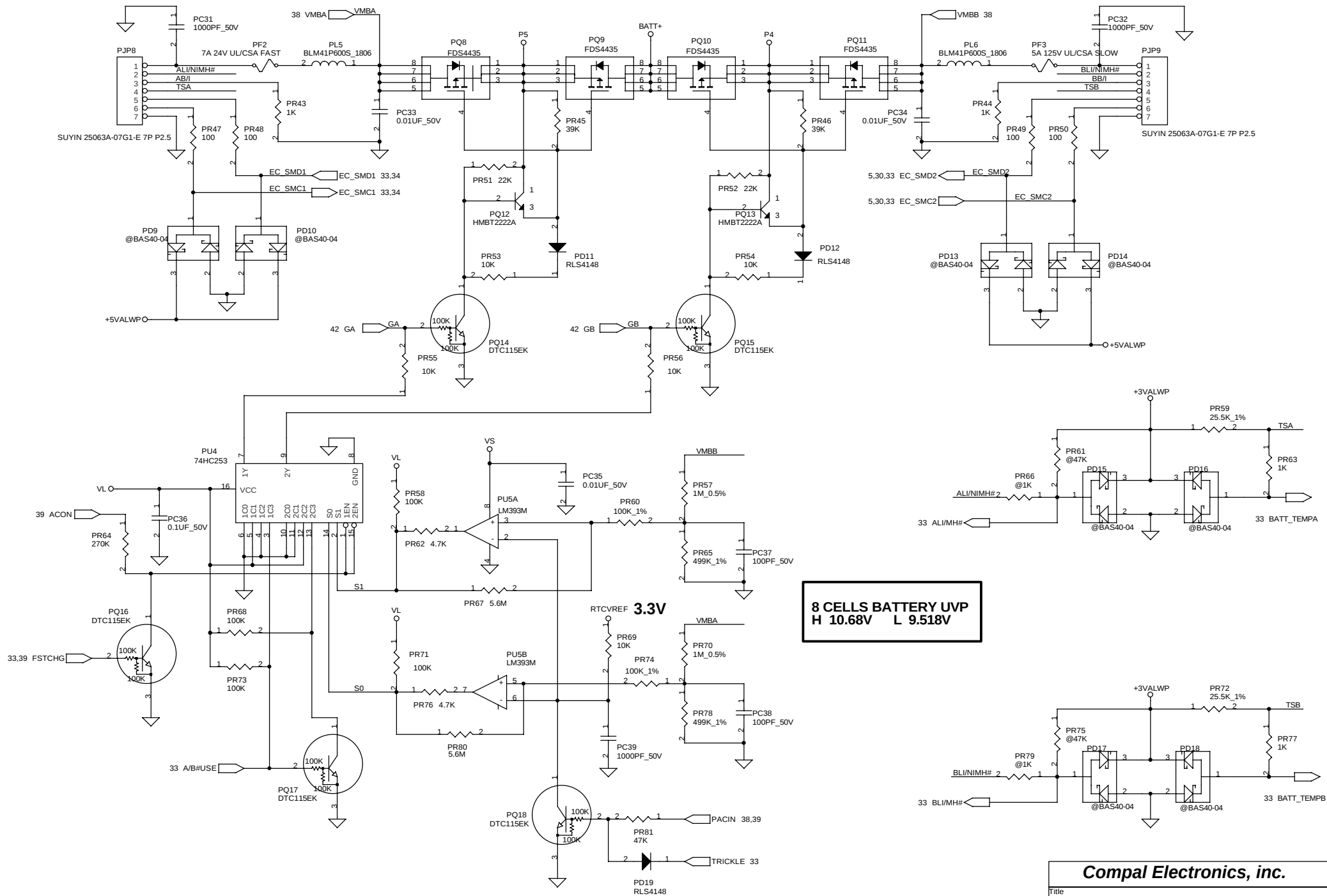
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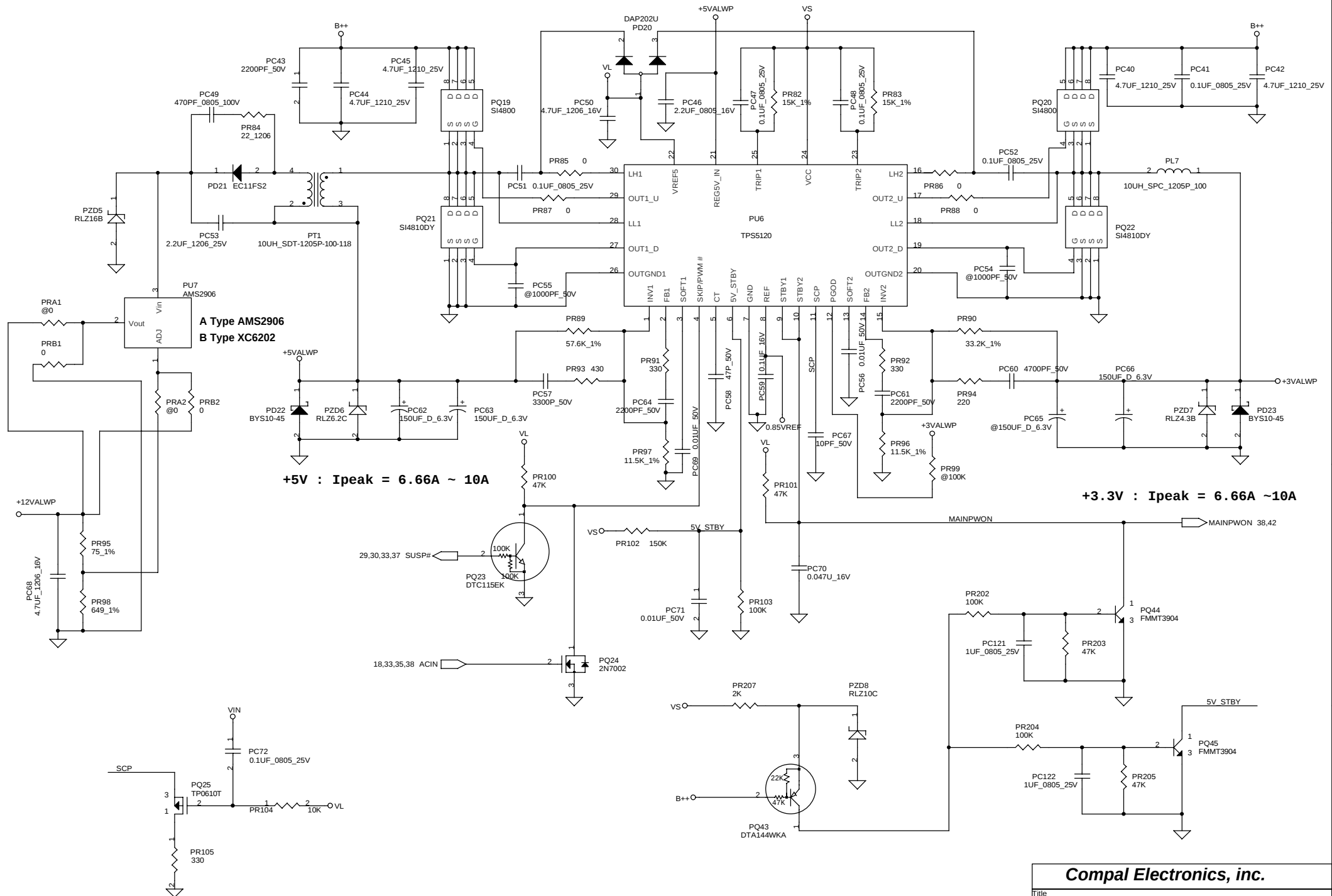
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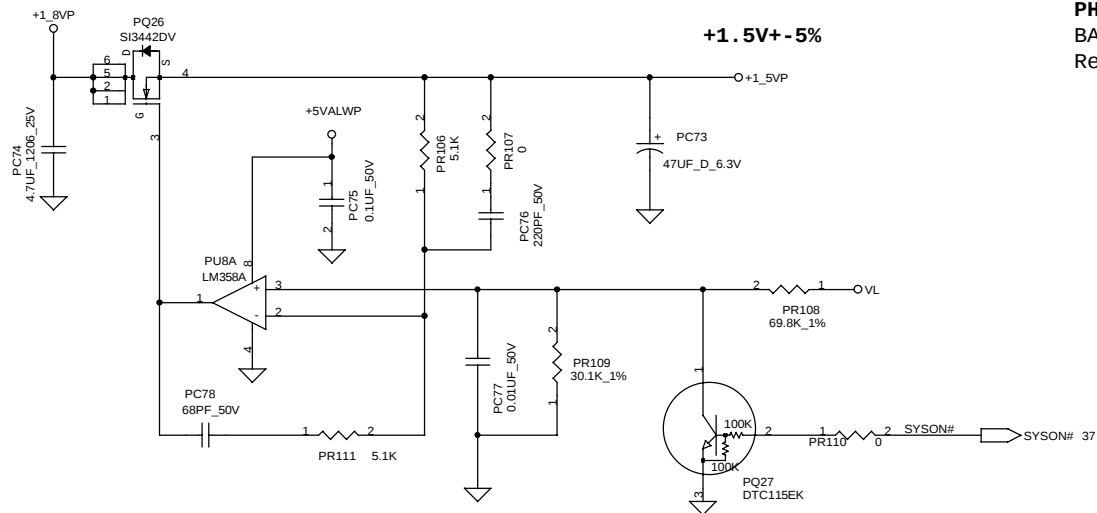
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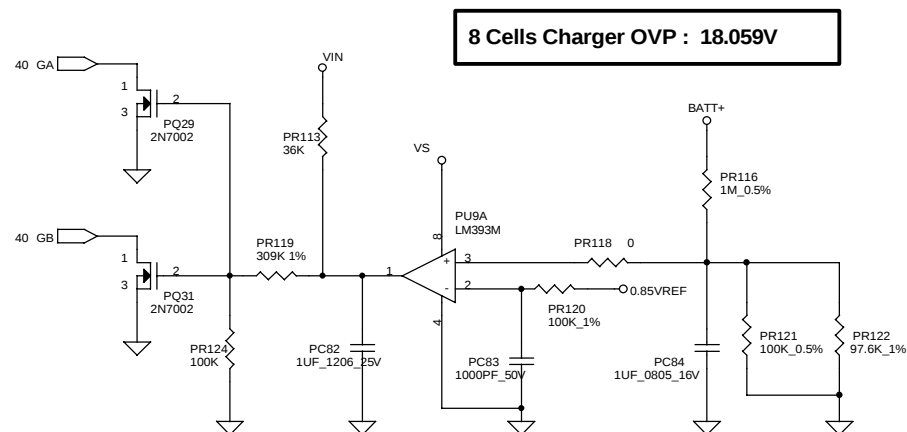
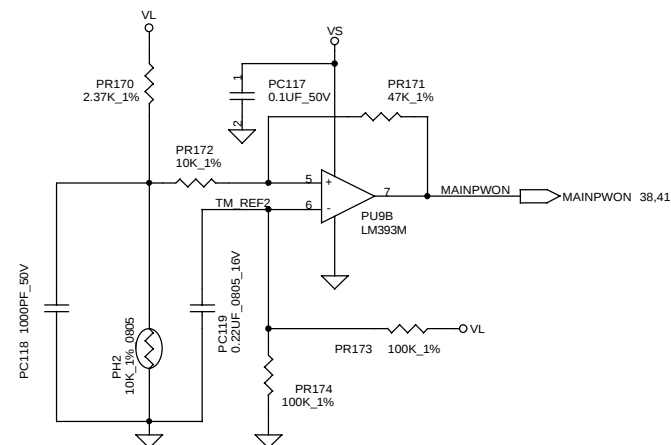


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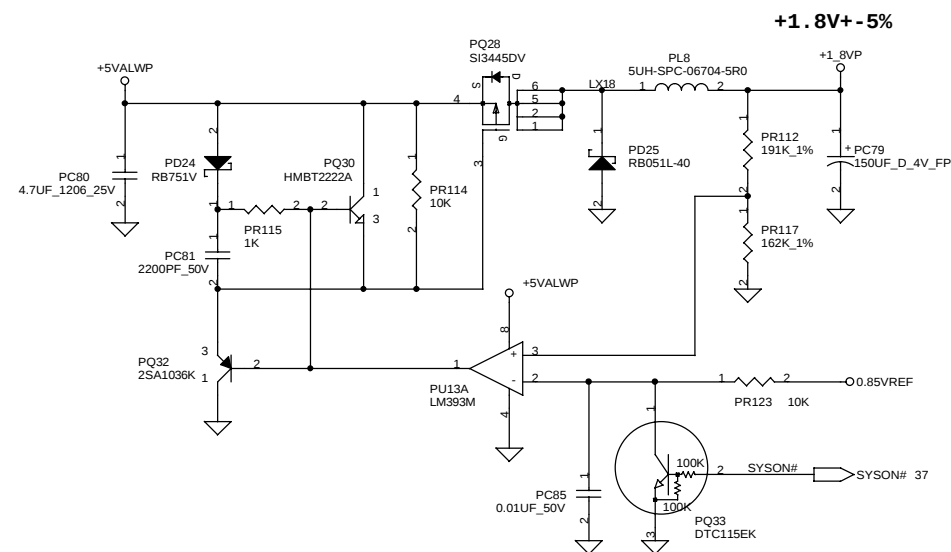
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PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C



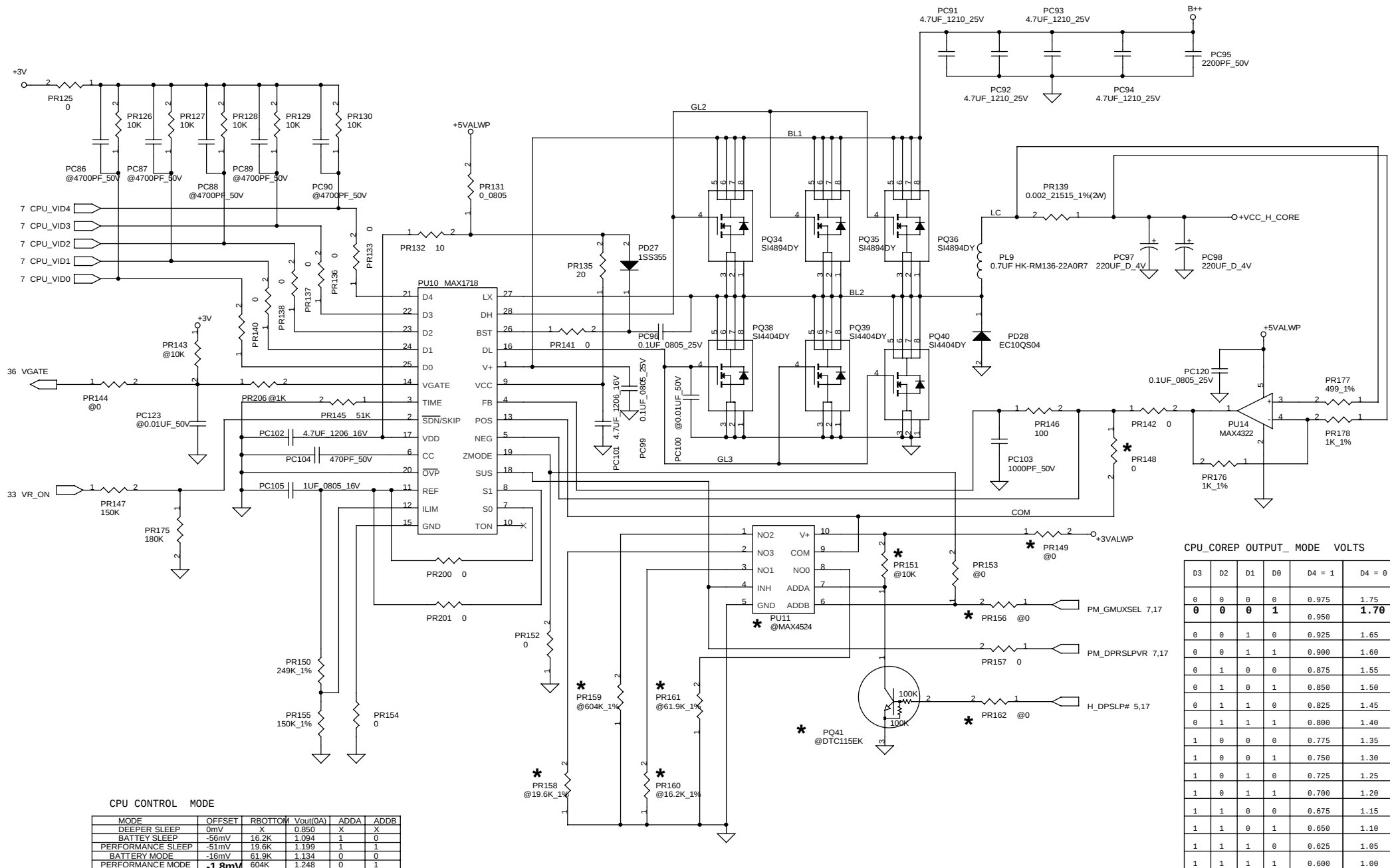
8 Cells Charger OVP : 18.059V



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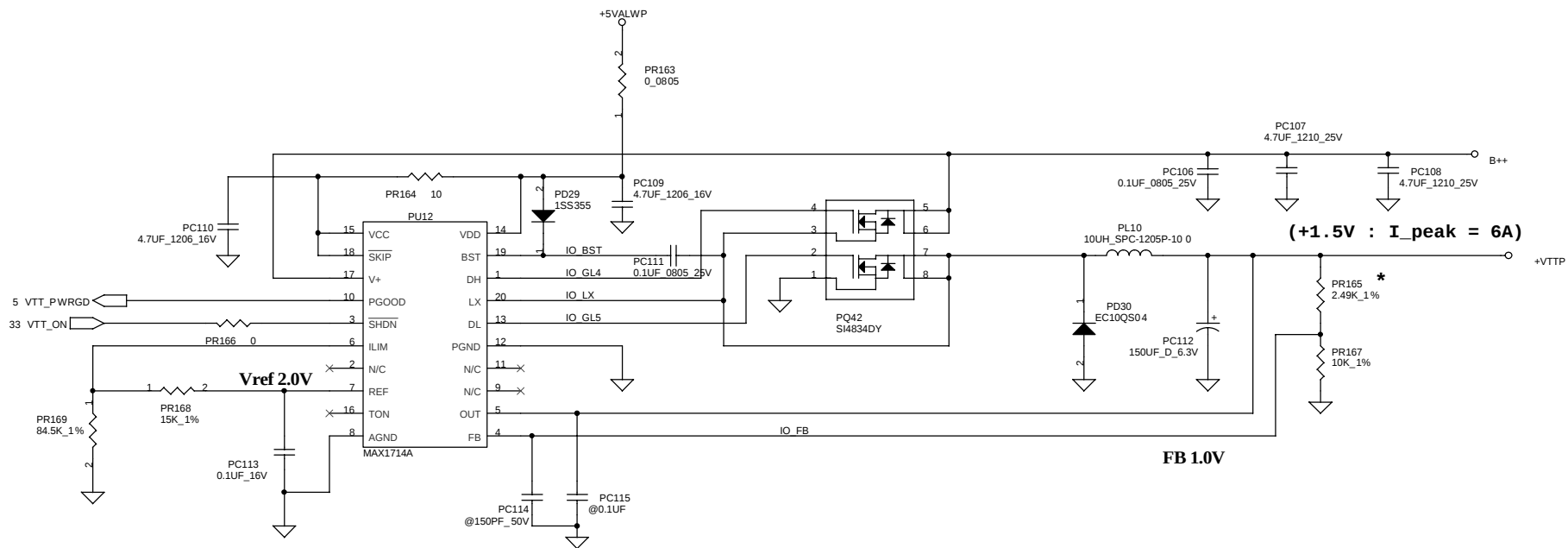
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