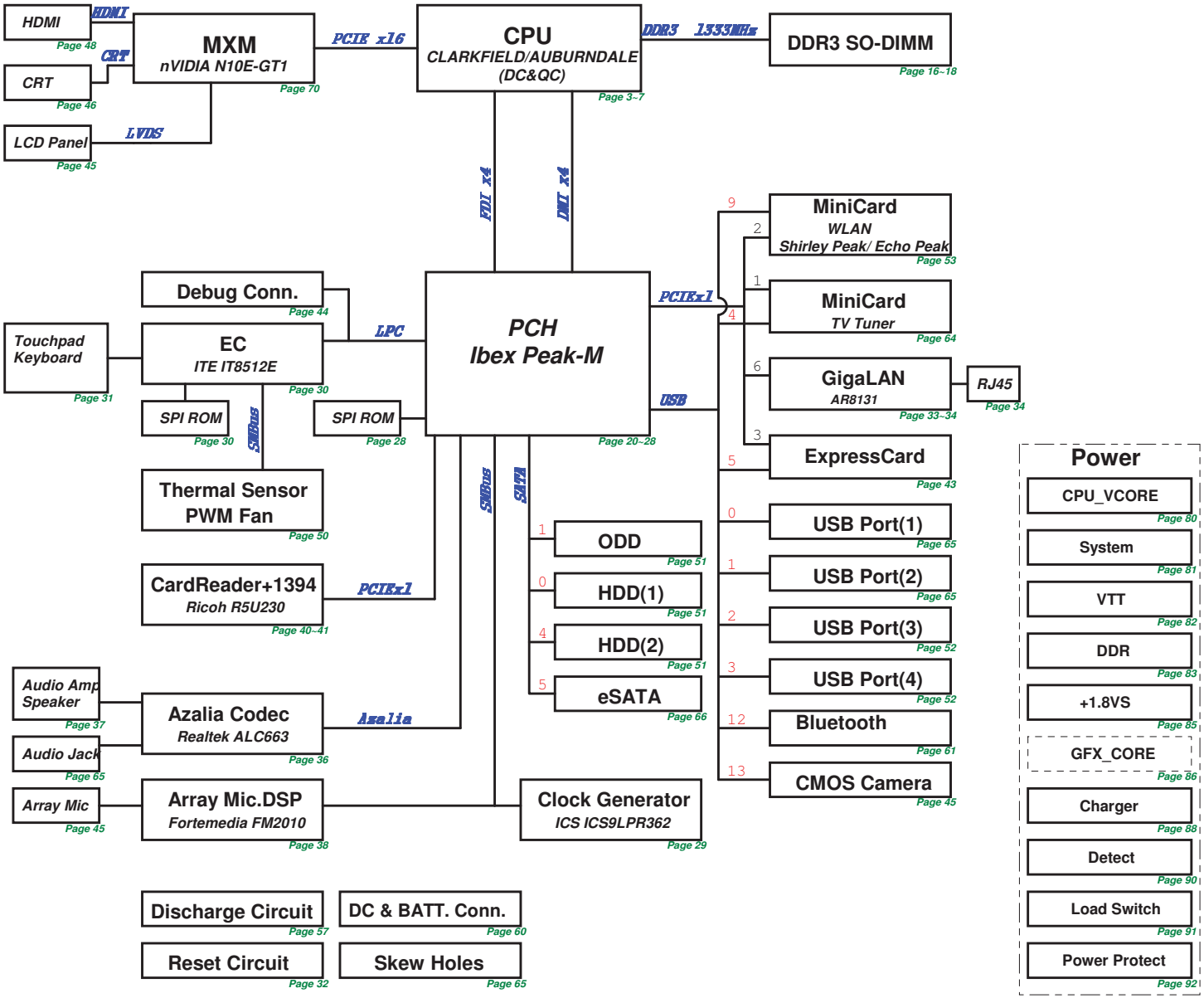
G60J Schematics for Calpella Platform Rev. 1.5

BLOCK DIAGRAM



SYSTEM PAGE REF.

PEGATRON Title : Block Diagram
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
Date: Friday, July 31, 2009 Sheet 1 of 99

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PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	PCH_GPIO0_R	–	+3VS
GPIO 01	–	–	INT TBD	+3VS
GPIO [2:5]	Native	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPI	DGPU_PWR_EN	INT TBD	+3VS
GPIO 07	–	–	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LANPHY_EN	EXT PU	+3VSUS
GPIO 13	–	–	–	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	–	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1_TV#	EXT PU(DNI)/PD	+3VS
GPIO 19	GPI	SATA_DET#1_R	–	+3VS
GPIO 20	Native	CLKREQ2_WLAN#	EXT PU(DNI)/PD	+3VS
GPIO 21	GPI	SATA_DET#0_R	–	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	–	–	–	+3VS
GPIO 24	GPO	OC_LAN_RST#	EXT PU	+3VSUS
GPIO 25	Native	CLKREQ3_NEWCARD#	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4_ESATA#	EXT PU(Not used)	+3VSUS
GPIO 27	–	–	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED/SPI_CS#2	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_SUSPWRDNACK / RTLAN_DSM#	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	–	–	–	+3VS
GPIO 34	Native	STP_PCI#	EXT PU	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	–	–	EXT PU (Not used)	+3VSUS
GPIO 45	–	–	EXT PU (Not used)	+3VSUS
GPIO 46	–	–	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	–	–	–	+3VS
GPIO 49	GPO	GPU_RST# / CRIT_TEMP_REP#_R	–	+3VS
GPIO 50	–	–	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#	EXT PU	+5VS
GPIO 53	–	–	INT PU	+3VS
GPIO 54	–	–	–	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	RTLAN_DSM_EN	EXT PU	+3VSUS
GPIO 61	–	–	–	+3VSUS
GPIO 62	–	–	–	+3VSUS
GPIO 63	–	–	–	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	–	–	INT TBD	+3VS
GPIO 67	–	–	INT TBD	+3VS
GPIO 72	–	–	–	+3VSUS
GPIO 73	–	–	EXT PU (Not used)	+3VSUS
GPIO 74	–	–	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DAT	EXT PU	+3VSUS

EC IT8512

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		–
GPA3	O	GAME_LED_EC#
GPA4	O	LCD_BL_PWM
GPA5	O	FAN_PWM
GPA6		–
GPA7		–
GPB0	O	SUSC_EC#
GPB1	O	SUSB_EC#
GPB2		–
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		–
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		–
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS# (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		–
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPF0		–
GPF1		–
GPF2	I	EXP_GATE#
GPF3		–
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	IO	H_PECI
GPG0		–
GPG1	I	PM_SUSB#
GPG2		–
GPG6		–
GPH0	IO	PM_CLKRUN#
GPH1		–
GPH2	O	GFX_VR_ON
GPH3	O	BAT_LEARN
GPH4	O	HSCK
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		–
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6		–
GPI7		–
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	TP_LED
GPJ5		–

EC IT8301

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SUSPWRDNACK
GPIO2		–
GPIO3		–
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		–
GPIO8		–
GPIO9		–
GPIO10		–
GPIO11		–
GPIO12	O	ME_PWROK
GPIO13		–
GPIO14	O	ME_SLP_M_EC#
GPIO15		–
GPIO16		–
GPIO17		–
GPIO18		–
GPIO19		–
GPIO20		–
GPIO21		–
GPIO22		–
GPIO23		–
GPIO24		–
GPIO25		–
GPIO26		–
GPIO27		–
GPIO28		–
GPIO29		–
GPIO30		–
GPIO31		–
GPIO32		–
GPIO33		–
GPIO34		–
GPIO35		–
GPIO36		–
GPIO37		–

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2h)
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001101x (9Ah)
VGA Thermal Sensor(NB9E-GE1)	1001111x (9Eh)
VID Controller ASM8272	0011011x (36h)
DSP FM2010	

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	N/A
PCIE 5	PCIE to SATA (SR)
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD(1)
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	SATA HDD(2)
SATA5	eSATA

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	Newcard
USB 6	Minicard TV Tuner
USB 7	N/A
USB 8	OLED
USB 9	WLAN
USB 10	N/A
USB 11	USB Port (5)
USB 12	Bluetooth
USB 13	Finger Print

PEGATRON Title : System Setting

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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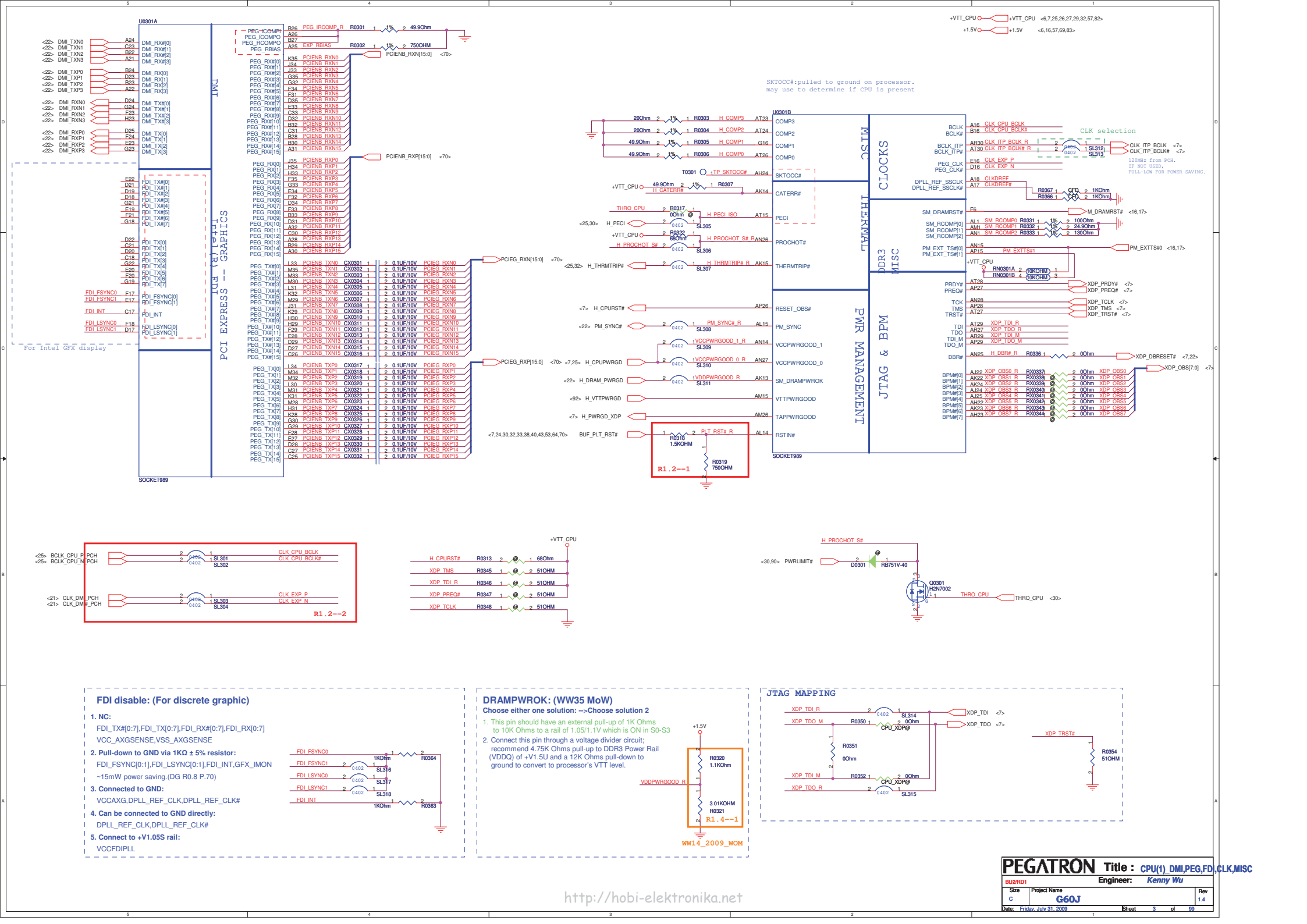
U0301A
DMI
PCI EXPRESS -- GRAPHICS
Intel(R) FDI
SOCKET989
For Intel GFX display
U0301B
MISC
CLOCKS
THERMAL
DDR3
JTAG & BPM
PWR MANAGEMENT
SOCKET989
SKTOCC#:pulled to ground on processor.
may use to determine if CPU is present
CLK selection
120MHz from PCH.
IF NOT USED,
PULL-LOW FOR POWER SAVING.
R1.2--1
R1.2--2
R1.4--1
FDI disable: (For discrete graphic)
1. NC:
FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]
VCC_AXGSENSE,VSS_AXGSENSE
2. Pull-down to GND via 1KΩ ± 5% resistor:
FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
~15mW power saving.(DG R0.8 P.70)
3. Connected to GND:
VCCAXG,DPLL_REF_CLK,DPLL_REF_CLK#
4. Can be connected to GND directly:
DPLL_REF_CLK,DPLL_REF_CLK#
5. Connect to +V1.05S rail:
VCCFDIPLL
DRAMPWROK: (WW35 MoW)
Choose either one solution: -->Choose solution 2
1. This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
2. Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.
WW14_2009_WOM
JTAG MAPPING
PEGATRON
Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
Engineer: Kenny Wu
BU2/RD1
Size C
Project Name G60J
Rev 1.4
Date: Friday, July 31, 2009
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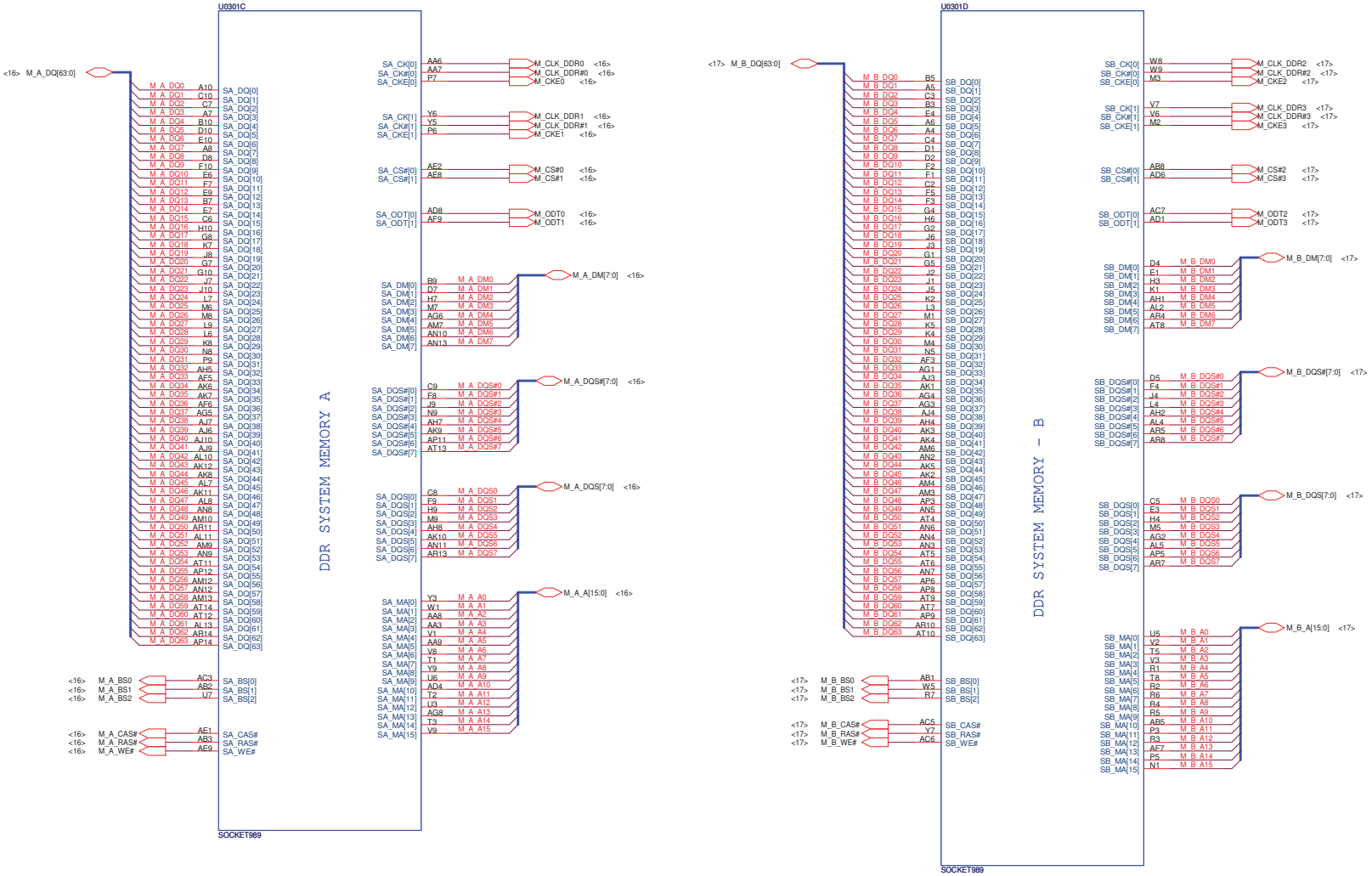

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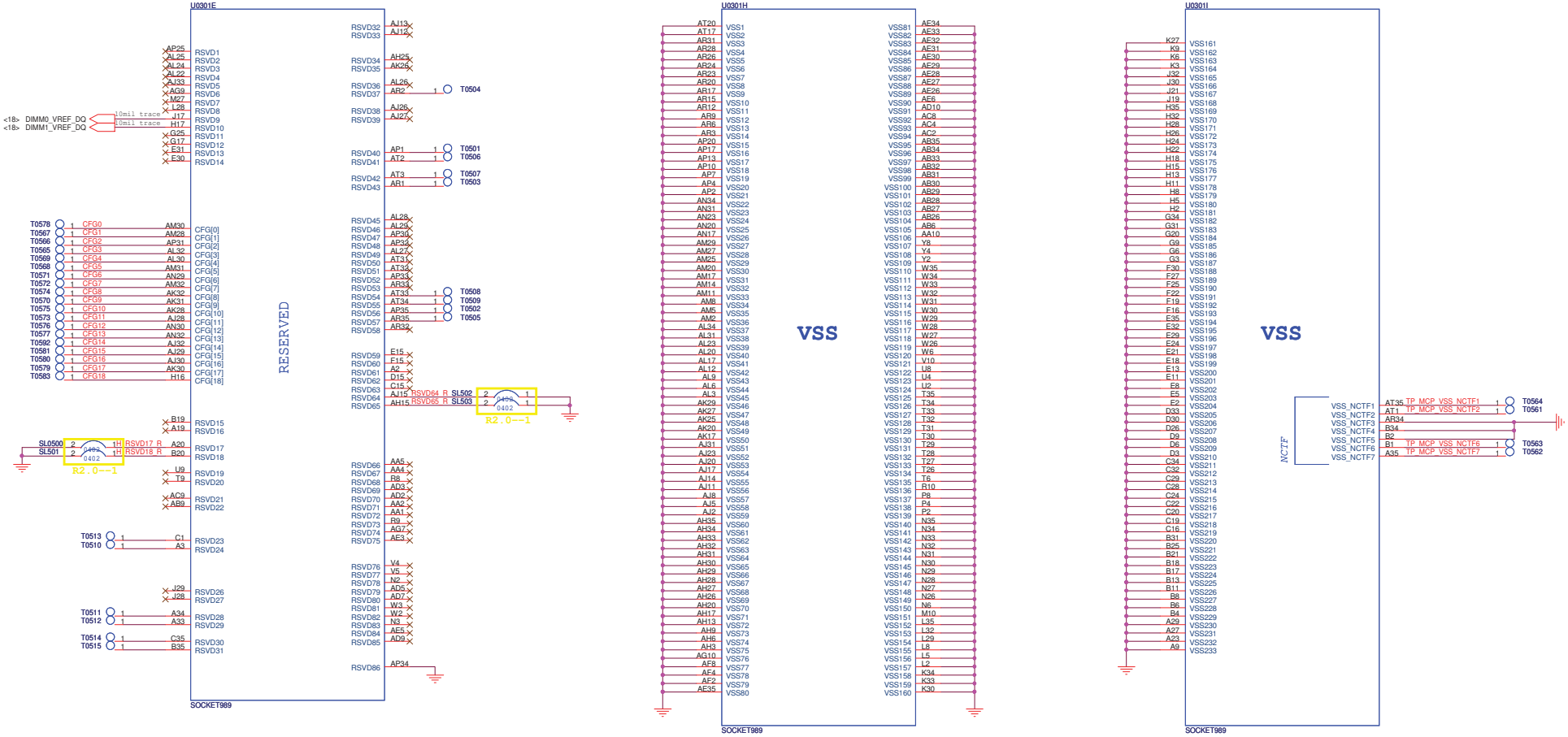
PEGATRON Title : CPU(2)_DDR3

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 4 of 99



CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

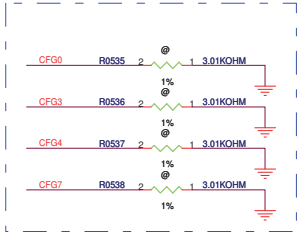
CFG[3]: PCIE Static Numbering Lane Reversal.(Auburndale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact AUB functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



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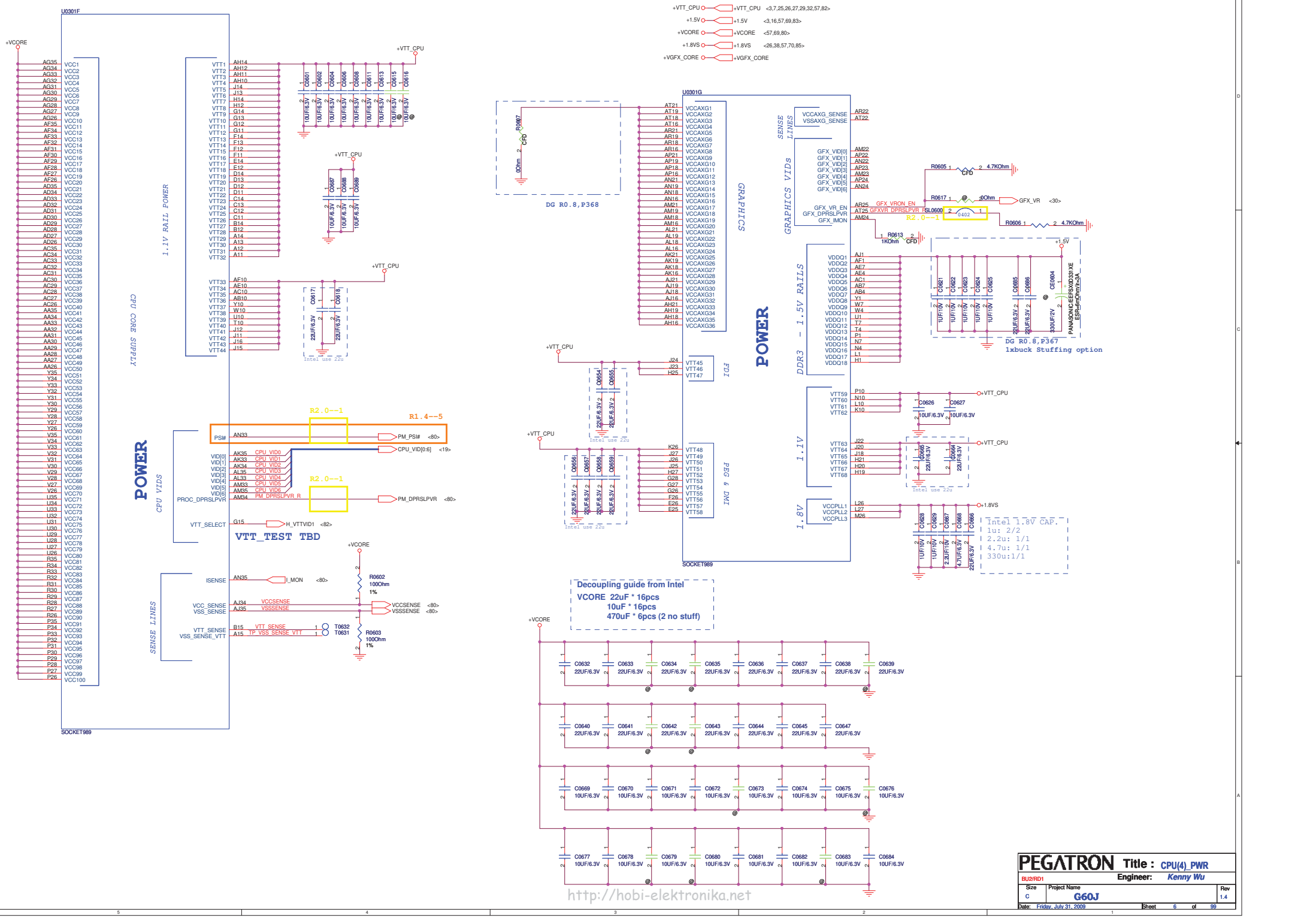
PEGATRON Title : CPU(3)_CFG,RSVD,GND
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
Date: Friday, July 31, 2009 Sheet 5 of 99



PEGATRON Title : CPU(4)_PWR

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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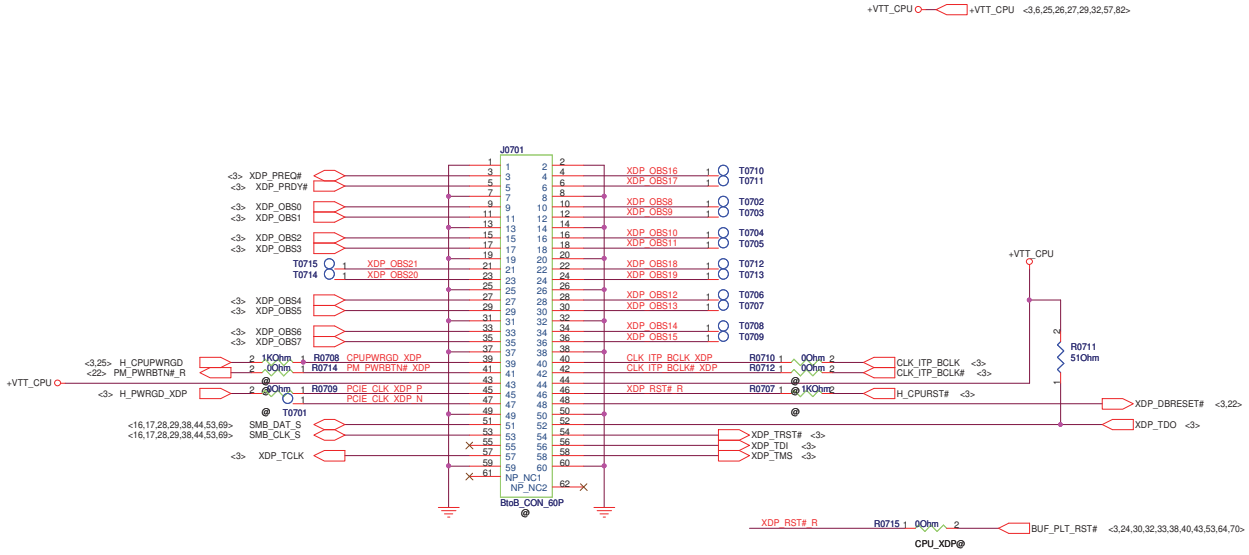

CPU XDP connector

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PEGATRON	Title : CPU(5)_XDP	
BU2/RD1	Engineer: Kenny Wu	
Size: C	Project Name: G60J	Rev: 1.4
Date: Friday, July 31, 2009	Sheet 7 of 99	

PEGATRON	Title : NB(1)_****			
BU2/RD1	Engineer: Kenny Wu			
Size: Custom	Project Name: G60J			Rev: 1.4
Date: Friday, July 31, 2009	Sheet 8 of 99			

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PEGATRON	Title : NB(2)_****			
BU2/RD1	Engineer: Kenny Wu			
Size: Custom	Project Name: G60J			Rev: 1.4
Date: Friday, July 31, 2009	Sheet 9 of 99			

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PEGATRON	Title : NB(3)_****				
BU2/RD1	Engineer: *Kenny Wu*				
Size: Custom	Project Name: G60J				Rev: 1.4
Date: Friday, July 31, 2009	Sheet 10 of 99				

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PEGATRON	Title : NB(4)_****		
BU2/RD1	Engineer: *Kenny Wu*		
Size: Custom	Project Name: G60J		Rev: 1.4
Date: Friday, July 31, 2009	Sheet 11 of 99		

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PEGATRON	Title : NB(5)_****			
BU2/RD1	Engineer: *Kenny Wu*			
Size: Custom	Project Name: G60J			Rev: 1.4
Date: Friday, July 31, 2009	Sheet 12 of 99			

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PEGATRON	Title : NB(6)_****		
BU2/RD1	Engineer: *Kenny Wu*		
Size: Custom	Project Name: G60J		Rev: 1.4
Date: Friday, July 31, 2009	Sheet 13 of 99		

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PEGATRON	Title : NB(7)_****
BU2/RD1	Engineer: Kenny Wu
Size: A	Project Name: G60J
Rev: 1.4	
Date: Friday, July 31, 2009	Sheet 14 of 99

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PEGATRON	Title : NB(8)_****
BU2/RD1	Engineer: Kenny Wu
Size: A	Project Name: G60J
Rev: 1.4	
Date: Friday, July 31, 2009	Sheet 15 of 99

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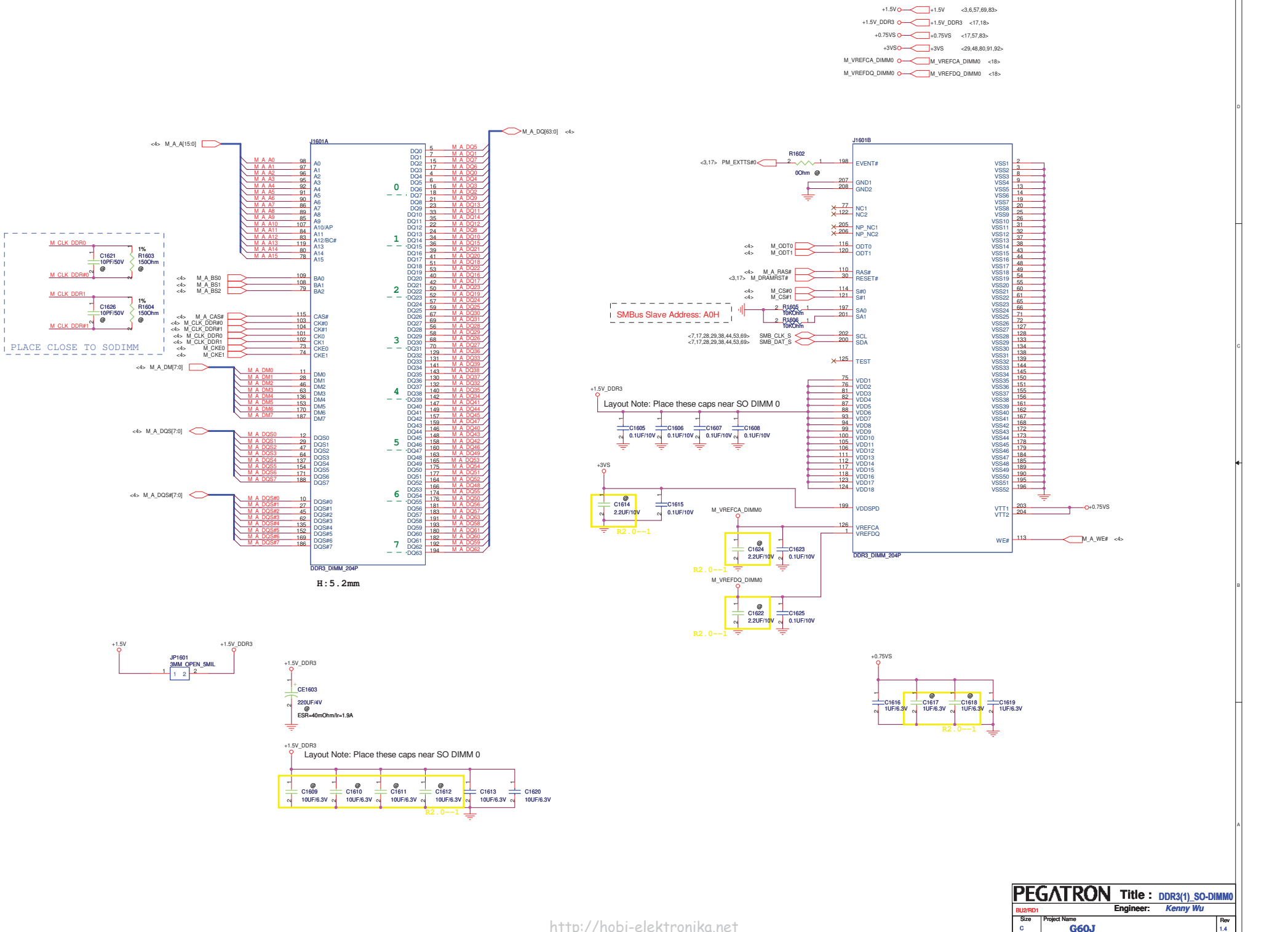

PEGATRON Title : DDR3(1)_SO-DIMM0

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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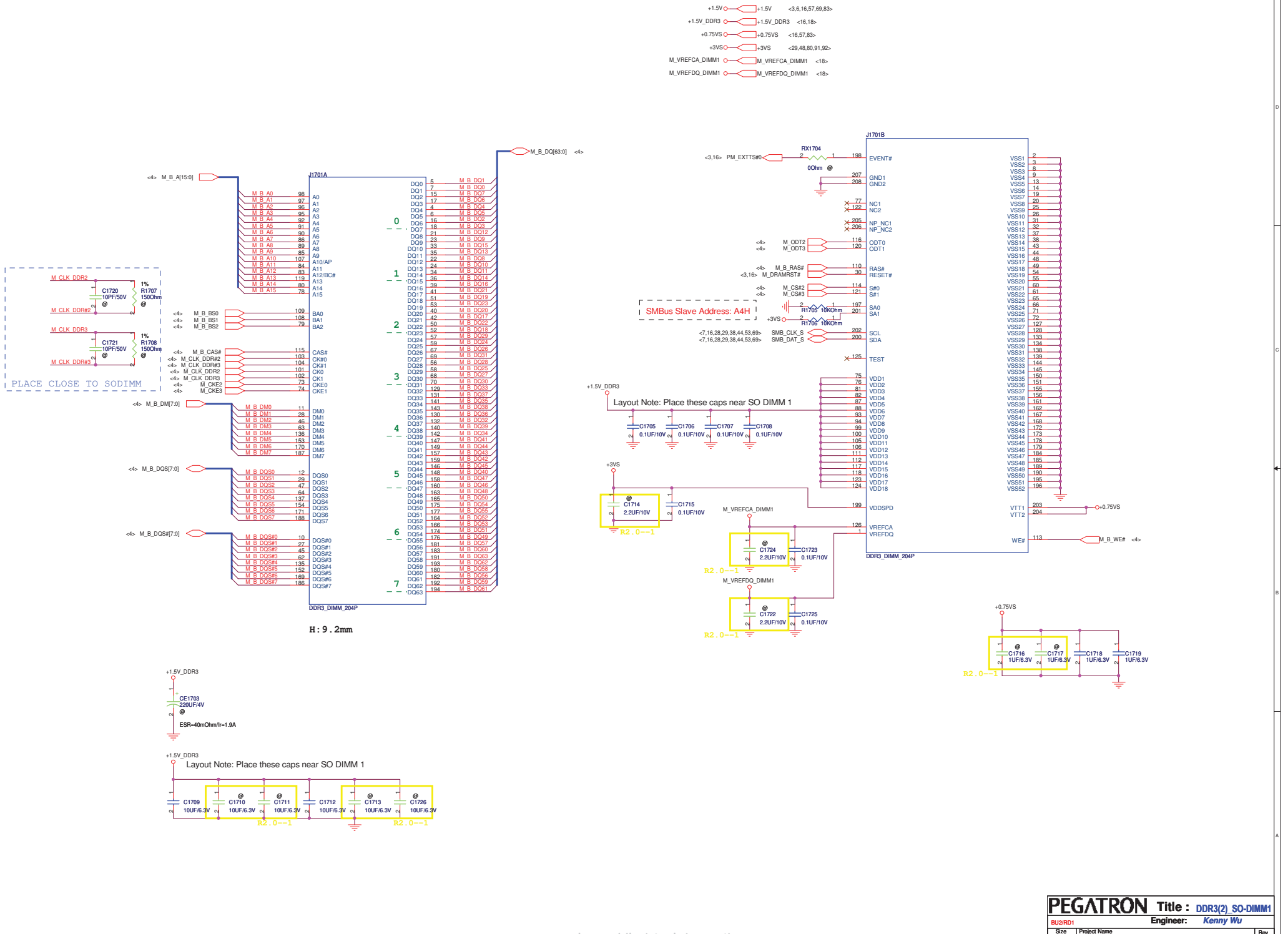

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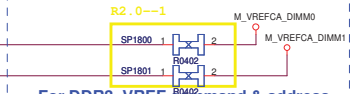
DDR3 Vref

Intel Document Number: 400755
Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

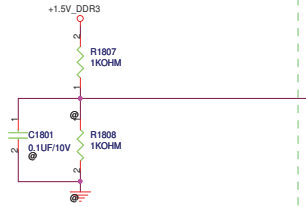
+1.5V_DDR3 — +1.5V_DDR3 <16,17>
M_VREFCA_DIMM0 — M_VREFCA_DIMM0 <16>
M_VREFDQ_DIMM0 — M_VREFDQ_DIMM0 <16>
M_VREFCA_DIMM1 — M_VREFCA_DIMM1 <17>
M_VREFDQ_DIMM1 — M_VREFDQ_DIMM1 <17>
+3V — +3V <24,33,43,45,57,61,64,69,91>
+5VSUS — +5VSUS <27,56,81,91>
+5VA — +5VA <31,56,81,82,83>

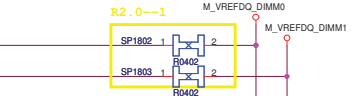
Default M1

M1: Fixed SO-DIMM VREF_DQ (Default Stuffing)
*Option: Mount=R1801,R1802,R1803,R1804,R1809
Unmount=R1805,R1806,R1807,R1808,C1801



For DDR3_VREF command & address.
R1802,R1803 are always mount.





M2

M2: Programmable SO-DIMM VREFDQ on motherboard– New Requirement
*Option: Mount=R1801,R1802,R1803,R1804,R1807,R1808,C1801
Unmount=R1805,R1806,R1809
*Range from 600 to 900 mV
*Default startup value needs to adhere to JEDEC spec. (power sequencing and +/-1% of Vdd/2)

Note: Use voltage divider instead of I2C solution.

M3

M3: Processor Generated SO-DIMM VREFDQ – New Requirement
Option: Mount=R1802,R1803,R1805,R1806
Unmount=R1801,R1804,R1809,R1807,R1808,C1801

R1.4--1

PEGATRON **Title : DDR3(3)_CA/DQ Voltage**
BU2/RD1 **Engineer: Kenny Wu**

Size	Project Name	Rev
C	G60J	1.4

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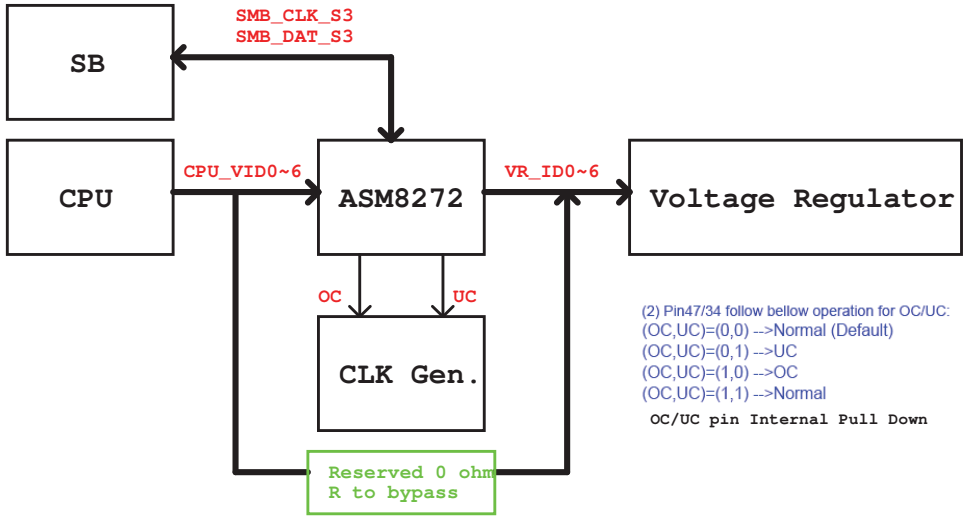
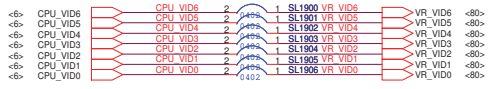
Block Diagram



(2) Pin47/34 follow bellow operation for OC/UC:
(OC,UC)=(0,0) -->Normal (Default)
(OC,UC)=(0,1) -->UC
(OC,UC)=(1,0) -->OC
(OC,UC)=(1,1) -->Normal

OC/UC pin Internal Pull Down

+VTT_CPU +VTT_CPU <3,6,7,25,26,27,29,32,57,82>
+3VS +3VS <29,48,80,91,92>



R1.4--2

PEGATRON Title : VID Controller
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
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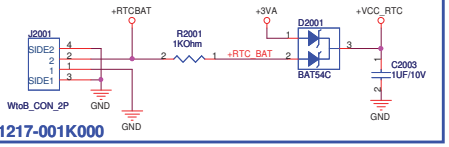
RTC battery



1217-001K000

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

HDA_SYNC: Select VCCVRM 1.5V or 1.8V

EDS 1.0: SATA port2,port3 may not be available in all PCH SKUs.

Strap information:

HDA_SPKR: No reboot strap
Low: Disable.
High:Enable

HDA_DOCK_EN#:
1.Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2.GPIO33 low on the rising edge of PWROK, Will also disable Intel ME.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)

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PEGATRON	Title : PCH(1)_SATA,IHDA,RTC,LPC		
BU2/RD1	Engineer: Kenny Wu		
Size: C	Project Name: G60J	Rev: 1.4	
Date: Friday, July 31, 2009	Sheet 20 of 99		

PCIE5: PCIE-->CB

+3VSUS <27,30,33,34,37,53,81,82,92>
+3VS <29,48,80,91,92>
+VTT_PCH_ORG <22,26,27>
+3VSUS_ORG <22,24,25,27>

U2001B

<64> PCIE_RXN1_TV
<64> PCIE_RXP1_TV
<64> PCIE_TXN1_C
<64> PCIE_TXP1_C
0.1UF/10V 2 1 CX2101 PCIE_TXN1_TV
0.1UF/10V 2 1 CX2102 PCIE_TXP1_TV

<53> PCIE_RXN2_WLAN
<53> PCIE_RXP2_WLAN
<53> PCIE_TXN2_C
<53> PCIE_TXP2_C
0.1UF/10V 2 1 CX2103 PCIE_TXN2_WLAN
0.1UF/10V 2 1 CX2104 PCIE_TXP2_WLAN

<43> PCIE_RXN3_NEWCARD
<43> PCIE_RXP3_NEWCARD
<43> PCIE_TXN3_C
<43> PCIE_TXP3_C
0.1UF/10V 2 1 CX2105 PCIE_TXN3_NEWCARD
0.1UF/10V 2 1 CX2106 PCIE_TXP3_NEWCARD

R1.2--5

<40> PCIE_RXN5_CR
<40> PCIE_RXP5_CR
<40> PCIE_TXN5_C
<40> PCIE_TXP5_C
0.1UF/16V 2 1 CX2115 PCIE_TXN5_CR
0.1UF/16V 2 1 CX2116 PCIE_TXP5_CR

<33> PCIE_RXN6_GLAN
<33> PCIE_RXP6_GLAN
<33> PCIE_TXN6_C
<33> PCIE_TXP6_C
0.1UF/10V 2 1 CX2111 PCIE_TXN6_GLAN
0.1UF/10V 2 1 CX2112 PCIE_TXP6_GLAN

EDS 1.0:
PCIE7,8 may not be availiable in all PCH SKUs.

PCI-E*

BG30 PERN1
BJ30 PERP1
BF29 PETN1
BH29 PETP1
AW30 PERN2
BA30 PERP2
BC30 PETN2
BD30 PETP2
AU30 PERN3
AT30 PERP3
AU32 PETN3
AV32 PETP3
BA32 PERN4
BB32 PERP4
BD32 PETN4
BE32 PETP4
BF33 PERN5
BH33 PERP5
BG32 PETN5
BJ32 PETP5
BA34 PERN6
AW34 PERP6
BC34 PETN6
BD34 PETP6
AT34 PERN7
AU34 PERP7
AU36 PETN7
AV36 PETP7
BG34 PERN8
BJ34 PERP8
BG36 PETN8
BJ36 PETP8

SMBus

SMBALERT#/GPIO11 B9 EXT_SCI# EXT_SCI# <30>
SMBCLK H14 SCL_3A SCL_3A <28>
SMBDATA C8 SDA_3A SDA_3A <28>
SML0ALERT#/GPIO60 J14 SML0ALERT# T2106
SML0CLK C6 SML0_CLK T2107
SML0DATA G8 SML0_DAT T2108
SML1ALERT#/GPIO74 M14 SML1ALERT# T2105
SML1CLK/GPIO58 E10 SML1_CLK SML1_CLK <28>
SML1DATA/GPIO75 G12 SML1_DAT SML1_DAT <28>

To EC

Controller Link

CL_CLK1 T13 CL_CLK <53>
CL_DATA1 T11 CL_DATA <53>
CL_RST1# T9 CL_RST# <53>

PEG

PEG_A_CLKRQ#/GPIO47 H1 CLKREQ_PEG# <70>
CLKOUT_PEG_A_N AD43 CLK_PCIE_PEG# <70>
CLKOUT_PEG_A_P AD45 CLK_PCIE_PEG <70>
CLKOUT_DMI_N AN4 CLK_DMI# <3>
CLKOUT_DMI_P AN2 CLK_DMI <3>
CLKOUT_DP_N/CLKOUT_BCLK1_N AT1
CLKOUT_DP_P/CLKOUT_BCLK1_P AT3

From Clk BUFFER

CLKOUT_PCIE0N AK48
CLKOUT_PCIE0P AK47
T2101 CLK_REQ0# P9 PCIECLKRQ0#/GPIO73
CLKIN_DMI_N AW24 CLK_DMI# <29>
CLKIN_DMI_P BA24 CLK_DMI <29>

<64> CLK_PCIE_TV# PCH
<64> CLK_PCIE_TV_PCH
CLK_PCH_SRC1_N AM43
CLK_PCH_SRC1_P AM45
CLKOUT_PCIE1N
CLKOUT_PCIE1P
<64> CLKREQ1_TV# U4 PCIECLKRQ1#/GPIO18
CLKIN_BCLK_N AP3 CLK_PCH_BCLK# <29>
CLKIN_BCLK_P AP1 CLK_PCH_BCLK <29>

<53> CLK_PCIE_WLAN# PCH
<53> CLK_PCIE_WLAN PCH
CLK_PCH_SRC2_N AM47
CLK_PCH_SRC2_P AM48
CLKOUT_PCIE2N
CLKOUT_PCIE2P
<53> CLKREQ2_WLAN# N4 PCIECLKRQ2#/GPIO20
CLKIN_DOT_96N F18 CLK_DOT96# <29>
CLKIN_DOT_96P E18 CLK_DOT96 <29>

<43> CLK_PCIE_NEWCARD# PCH
<43> CLK_PCIE_NEWCARD PCH
CLK_PCH_SRC3_N AH42
CLK_PCH_SRC3_P AH41
CLKOUT_PCIE3N
CLKOUT_PCIE3P
<43,44> CLKREQ3_NEWCARD# A8 PCIECLKRQ3#/GPIO25
CLKIN_SATA_N/CKSSCD_N AH13 CLK_SATA# <29>
CLKIN_SATA_P/CKSSCD_P AH12 CLK_SATA <29>
REFCLK14IN P41 CLK_ICH14 <29>
CLKIN_PCILOOPBACK J42 CLK_PCI_FB <24>

R1.2--5

<40> CLK_PCIE_CR#
<40> CLK_PCIE_CR
CLK_PCH_SRC4_N AM51
CLK_PCH_SRC4_P AM53
CLKOUT_PCIE4N
CLKOUT_PCIE4P
<40> CLK_REQ4#_CB CLKREQ4_CR# M9 PCIECLKRQ4#/GPIO26
XTAL25_IN AH51
XTAL25_OUT AH53
XCLK_RCOMP AF38 XCLK_COMP R2117 2 90.9Ohm 1% +VTT_PCH_ORG

R1.4--2

<33> CLK_PCIE_LAN#
<33> CLK_PCIE_LAN
CLK_PCH_SRC5_N AJ50
CLK_PCH_SRC5_P AJ52
CLKOUT_PCIE5N
CLKOUT_PCIE5P
<33> CLK_REQ5_LAN# CLK_REQ5_LAN# H6 PCIECLKRQ5#/GPIO44
CLKOUTFLEX0/GPIO64 T45 CLK_OUT0 R2118 47Ohm CLK_1394 <41>
CLKOUTFLEX1/GPIO65 P43 CLK_OUT1 T2112 R2.0
CLKOUTFLEX2/GPIO66 T42 CLK_OUT2 T2109
CLKOUTFLEX3/GPIO67 N50 CLK_OUT3 T2110

Clock Flex

AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P
T2104 CLKREQ_GLAN# R P13 PEG_B_CLKRQ#/GPIO56

IBEXPEAK-M

AUB C2101 27PF/50V
X2101 25Mhz
MOhm R2151
AUB AUB2102 27PF/50V
GND

+3VSUS_ORG

EXT_SCI# 10KOhm R2130
SCL_3A 2.2KOhm R2132
SDA_3A 2.2KOhm R2133
SML1ALERT# 10KOhm R2131
SML0_CLK 2.2KOhm R2140
SML0_DAT 2.2KOhm R2138
SML1_CLK 4.7KOhm R2136
SML1_DAT 4.7KOhm R2137
SML1ALERT# 10KOhm R2142

R1.2 --6

PCH CLKREQ Setting:

Not connected to device.

+3VSUS_ORG
CLK_REQ0# R2126 10KOhm
CLKREQ_GLAN# R R2129 10KOhm
R1.4--2

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

+3VS
CLKREQ1_TV# R2122 10KOhm
CLKREQ2_WLAN# R2123 10KOhm

+3VSUS_ORG
CLKREQ3_NEWCARD# R2124 10KOhm
CLK_REQ4#_CB R2127 10KOhm
CLK_REQ5_LAN# R2147 10KOhm
CLKREQ1_TV# R2145 10KOhm
CLKREQ2_WLAN# R2144 10KOhm
CLKREQ3_NEWCARD# R2143 10KOhm
CLK_REQ5_LAN# R2146 10KOhm
CLK_REQ4#_CB R2141 10KOhm
CLKREQ_PEG# R2139 10KOhm
R1.4--2
GND

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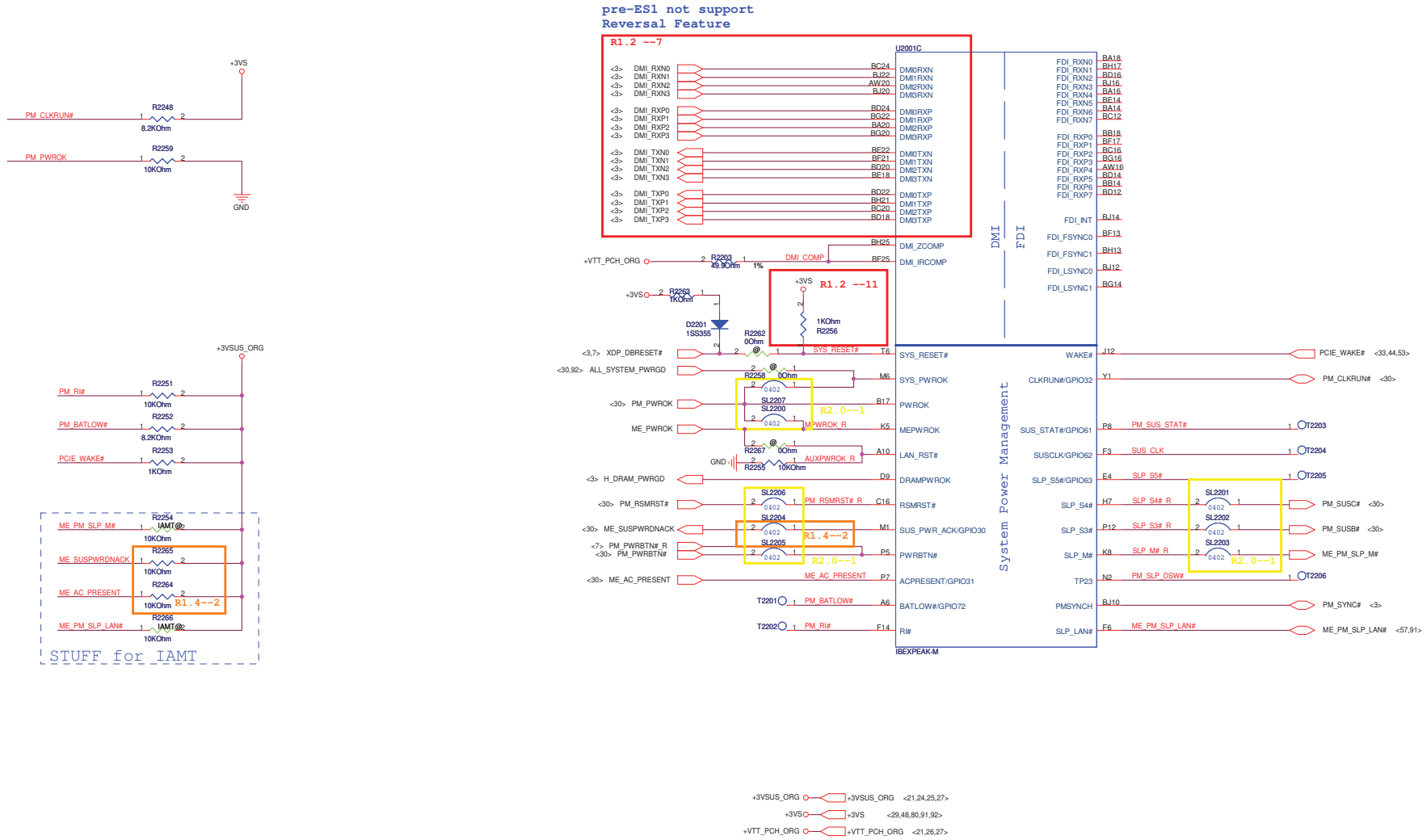
PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
Date: Friday, July 31, 2009 Sheet 21 of 99



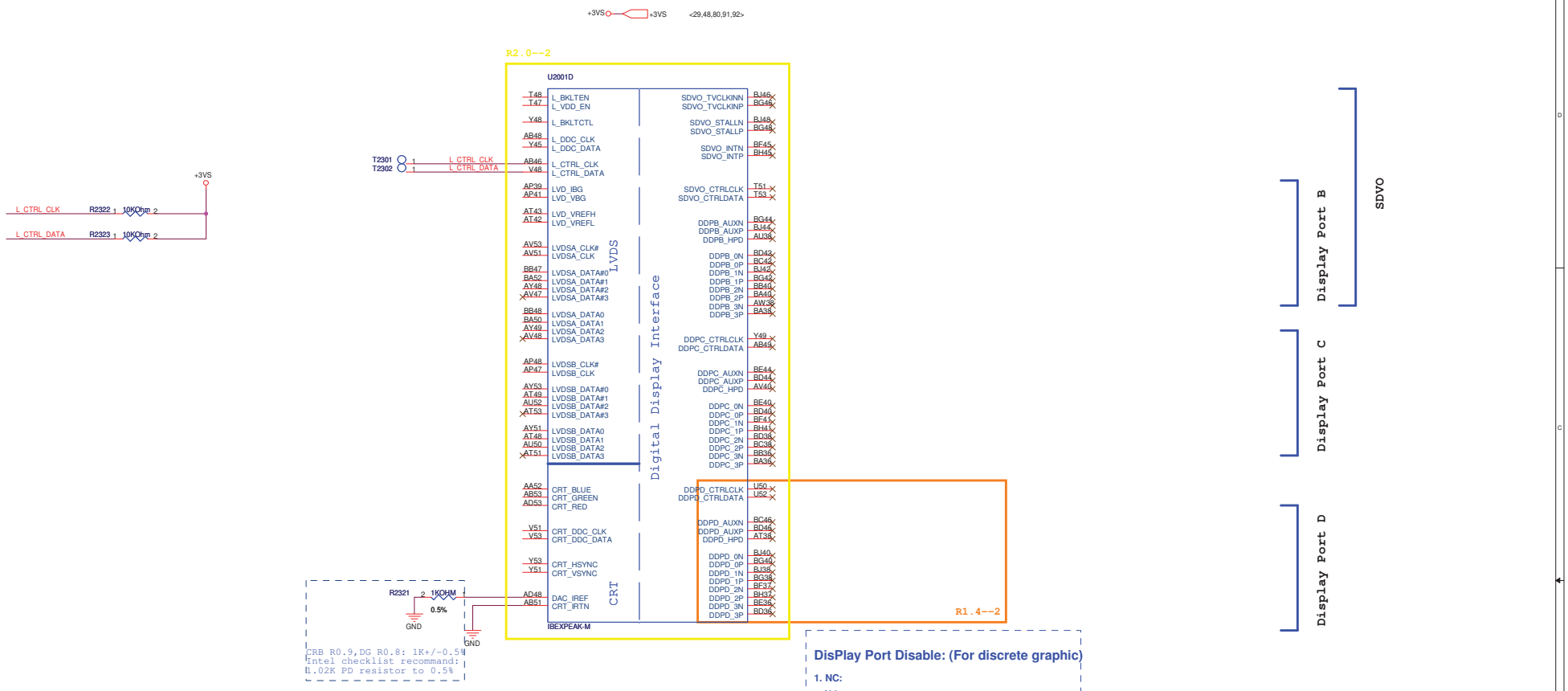
http://hobi-elektronika.net

PEGATRON Title : PCH(3)_FDI,DMI,SYS PWR

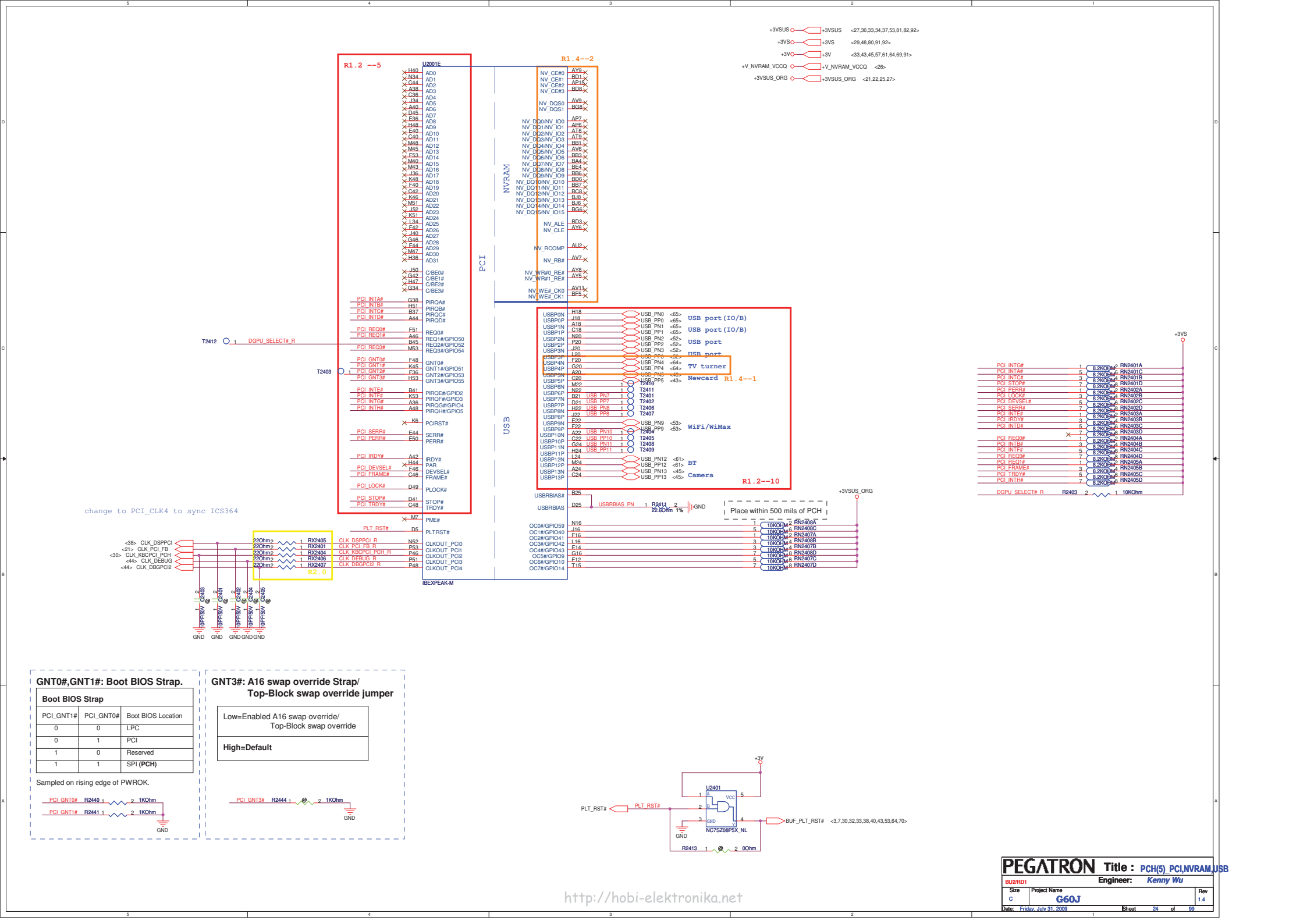
BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 22 of 99



http://hobi-elektronika.net



GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

PCI_GNT0# R2440 1KOhm
PCI_GNT1# R2441 1KOhm

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

PCI_GNT3# R2444 1KOhm

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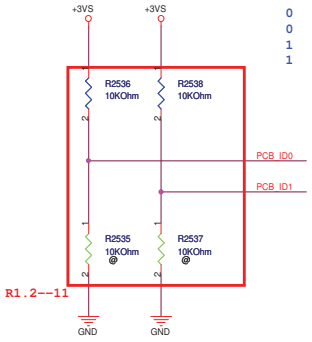
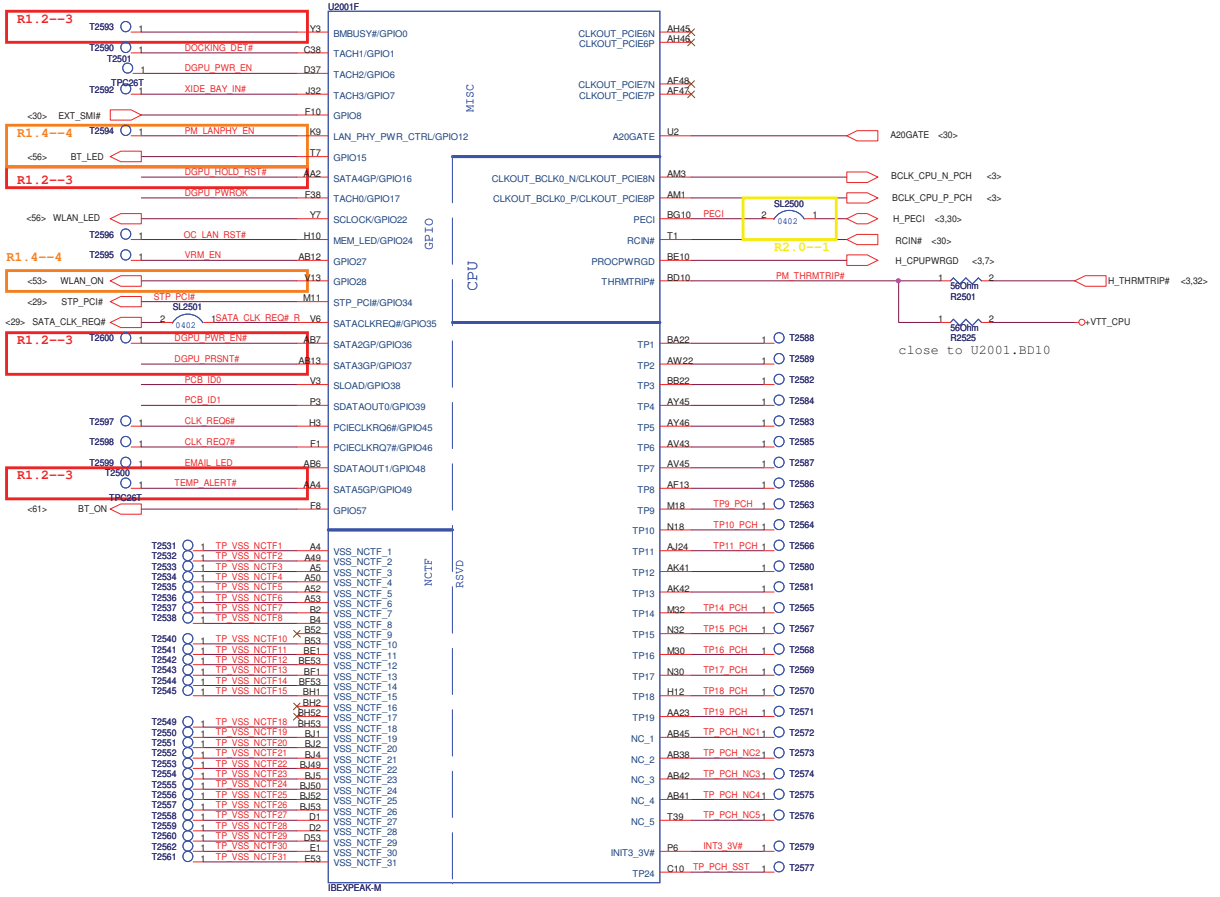
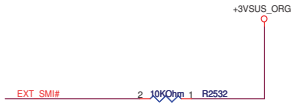
PEGATRON Title : PCH(5)_PCI,NVRAM,USB
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
Date: Friday, July 31, 2009 Sheet 24 of 99

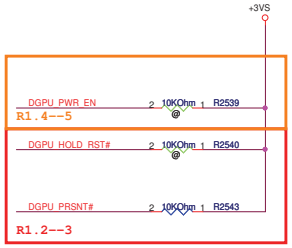
ID0	ID1	SKU
0	0	CFD_Non-IAMT
0	1	CFD_IAMT
1	0	AUB_Non-IAMT
1	1	AUB_IAMT

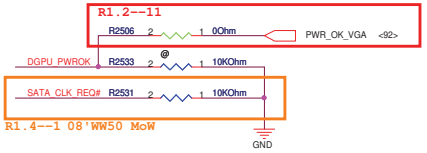


GPIO 27:Enable VCCVRM,Low=disable.
Default internal pull up.





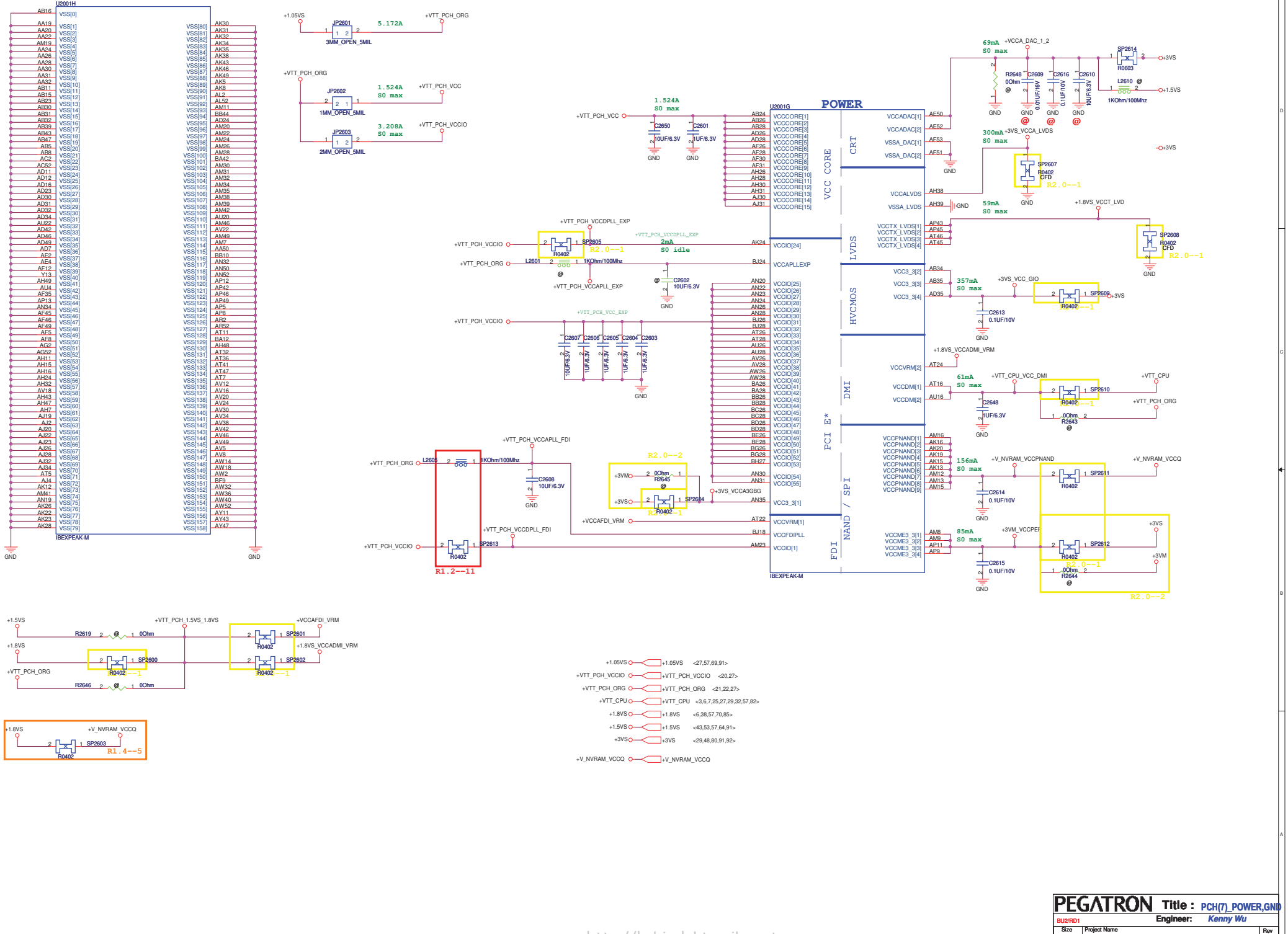


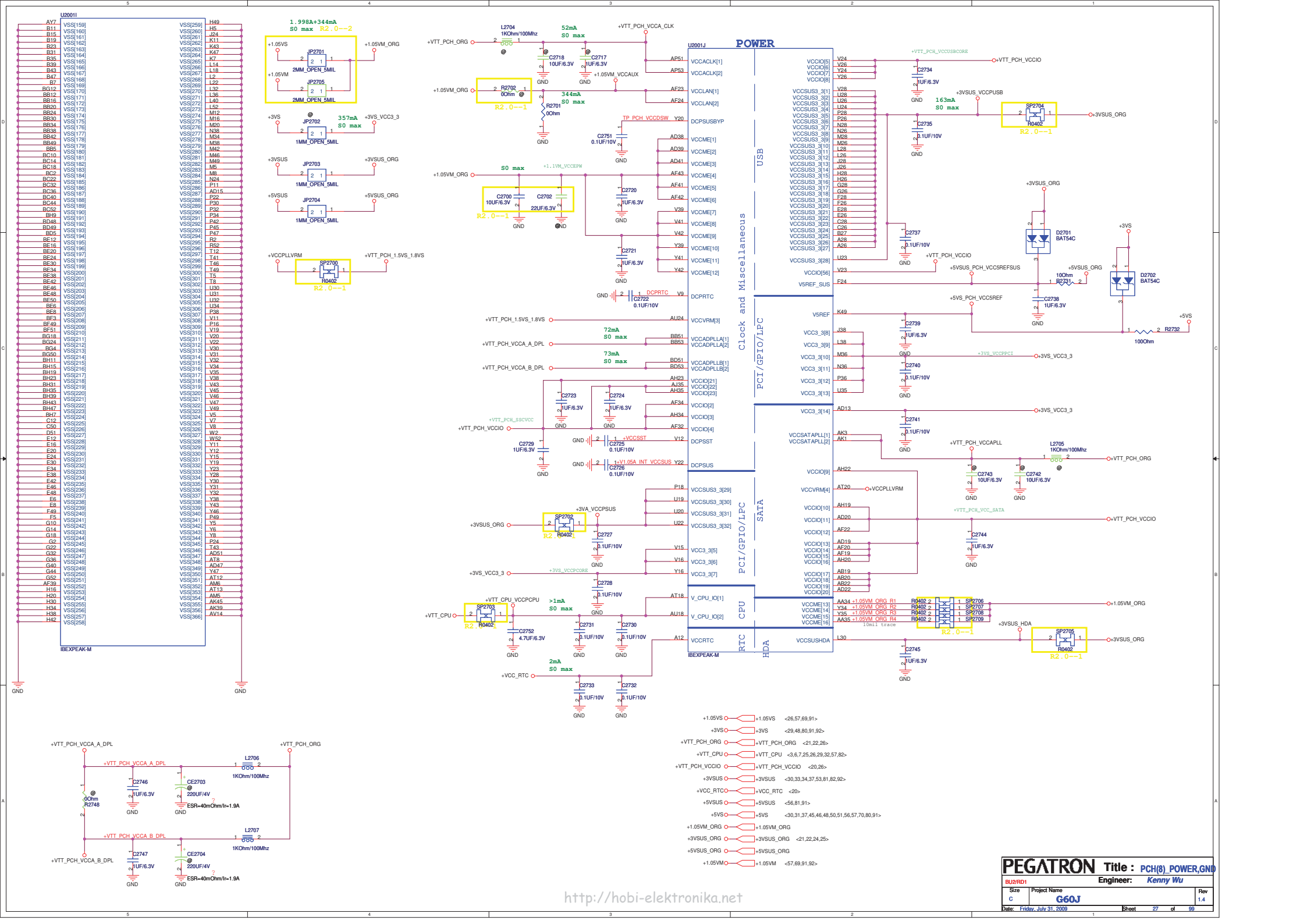


+3VS +3VS <29,48,80,91,92>
+3VSUS +3VSUS <27,30,33,34,37,53,81,82,92>
+VTT_CPU +VTT_CPU <3,6,7,26,27,29,32,57,82>
+3VSUS_ORG +3VSUS_ORG <21,22,24,27>

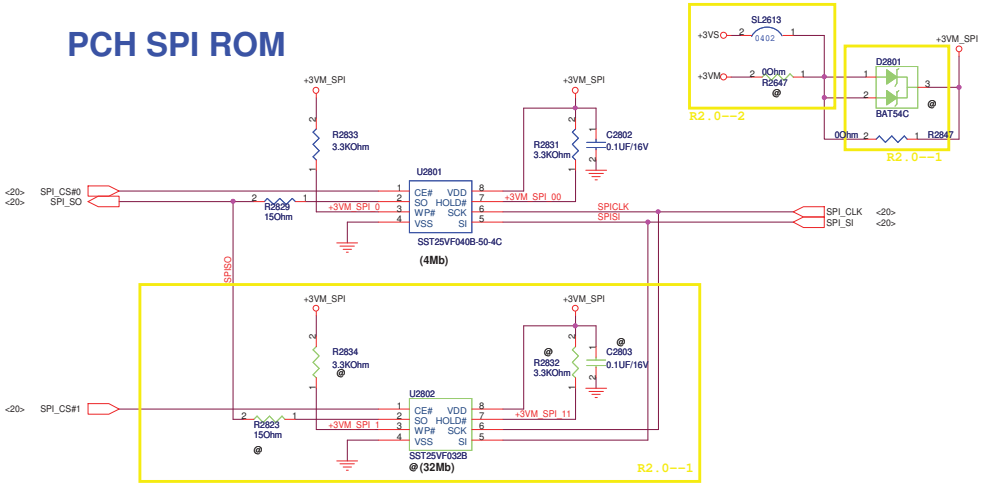
http://hobi-elektronika.net

PEGATRON Title : PCH(6)_CPU,GPIO,MISC
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
Date: Friday, July 31, 2009 | Sheet 25 of 99


U2001H
IBEXPEAK-M
U2001G
POWER
IBEXPEAK-M
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
JP2601
5.172A
3MIM_OPEN_5MIL
JP2602
1.524A
S0 max
1MM_OPEN_5MIL
JP2603
3.208A
S0 max
2MM_OPEN_5MIL
1.524A
S0 max
2mA
S0 idle
69mA
S0 max
300mA
S0 max
59mA
S0 max
357mA
S0 max
61mA
S0 max
156mA
S0 max
85mA
S0 max
R2.0--1
R2.0--2
R1.2--11
R1.4--5
http://hobi-elektronika.net
PEGATRON
Title : PCH(7)_POWER,GND
Engineer: Kenny Wu
BU2/RD1
Size C
Project Name G60J
Rev 1.4
Date: Friday, July 31, 2009
Sheet 26 of 99


POWER
U2001J
IBEXPEAK-M
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
1.998A+344mA
S0 max R2.0--2
357mA
S0 max
52mA
S0 max
344mA
S0 max
72mA
S0 max
73mA
S0 max
163mA
S0 max
>1mA
S0 max
2mA
S0 max
R2.0--1
R2.0--2
ESR=40mOhm/fr=1.9A
1KOhm/100Mhz
100Ohm
10Ohm
0Ohm
1mil trace
http://hobi-elektronika.net
PEGATRON
Title : PCH(8)_POWER,GND
Engineer: Kenny Wu
BU2/RD1
Size C
Project Name G60J
Rev 1.4
Date: Friday, July 31, 2009
Sheet 27 of 99

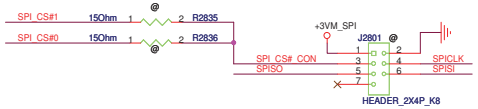
PCH SPI ROM



SPI FROM EC

For EC request.

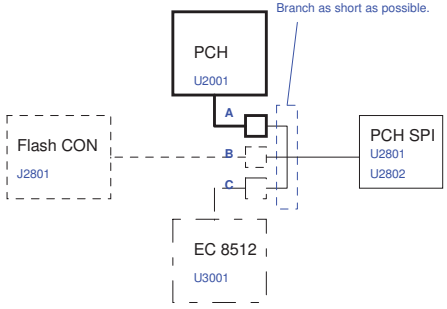
SPI FLASH CON

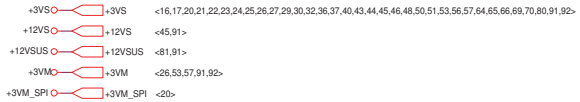


1206-000C000

Put near U2801,U2802

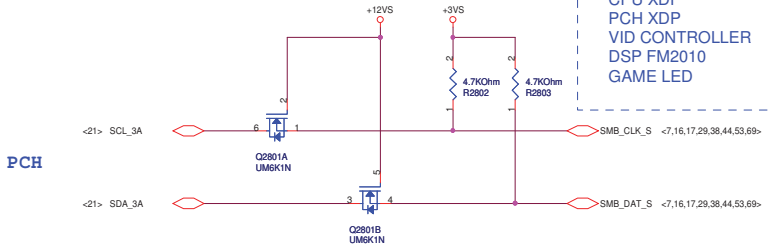
SPI Setting for layout:

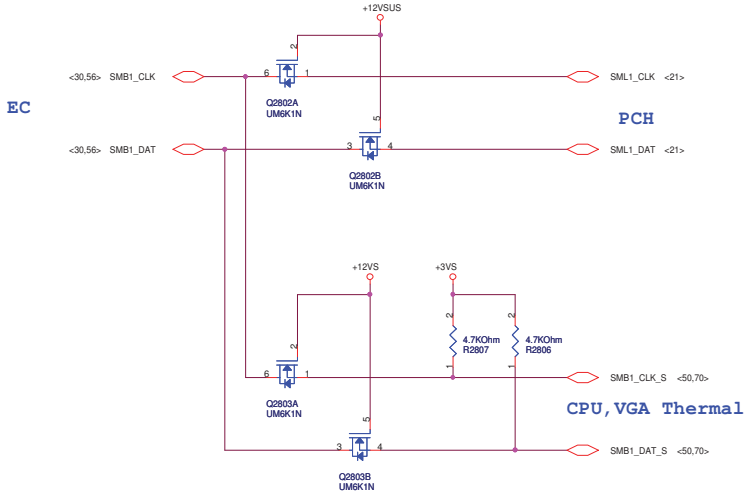




SMBUS Link device

- SPD
- CLKGEN
- DEBUG
- WLAN
- CPU XDP
- PCH XDP
- VID CONTROLLER
- DSP FM2010
- GAME LED





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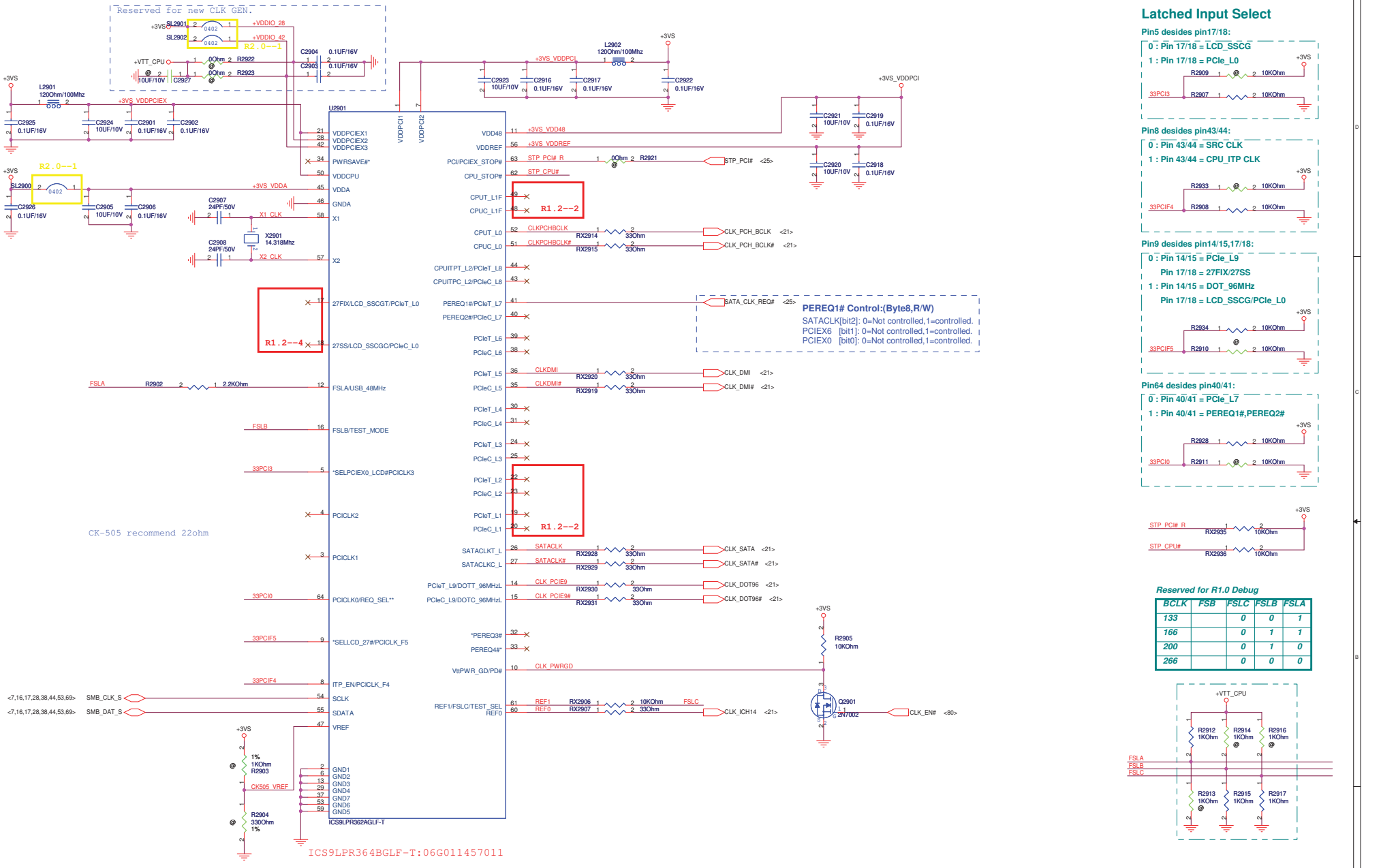
PEGATRON Title : PCH(9)_SPI,SMB

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 28 of 99



Latched Input Select

Pin5 desides pin17/18:

0 : Pin 17/18 = LCD_SSCG

1 : Pin 17/18 = PCIe_L0

Pin8 desides pin43/44:

0 : Pin 43/44 = SRC CLK

1 : Pin 43/44 = CPU_ITP CLK

Pin9 desides pin14/15,17/18:

0 : Pin 14/15 = PCIe_L9

Pin 17/18 = 27FIX/27SS

1 : Pin 14/15 = DOT_96MHz

Pin 17/18 = LCD_SSCG/PCIe_L0

Pin64 desides pin40/41:

0 : Pin 40/41 = PCIe_L7

1 : Pin 40/41 = PEREQ1#,PEREQ2#

Reserved for R1.0 Debug

BCLK	FSB	FSLC	FSLB	FSLA
133		0	0	1
166		0	1	1
200		0	1	0
266		0	0	0

	R2903	R2904	R2925
363:VREF	1K	330	@
364:TURBO	@	10K	0
364:NO TURBO	@	@	@

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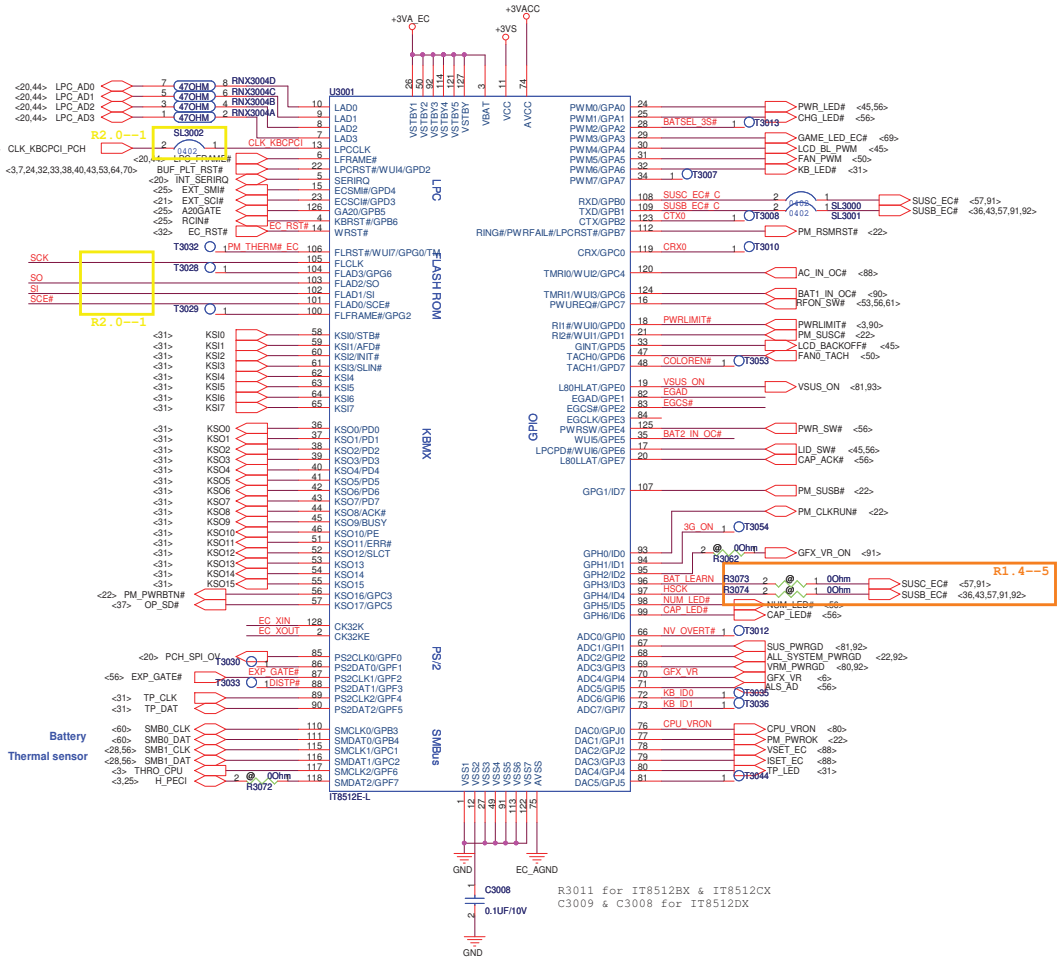
PEGATRON Title : CLK_ICS9LPR362

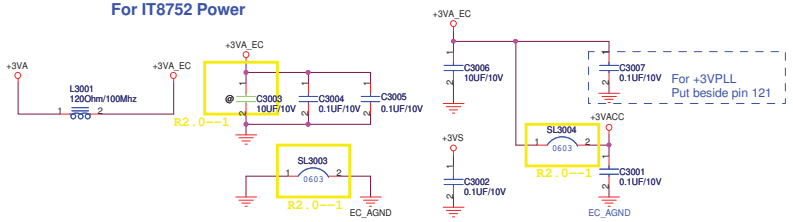
BU2/RD1 Engineer: Gary Tsai

Size	Project Name	Rev
C	G50J	1.2

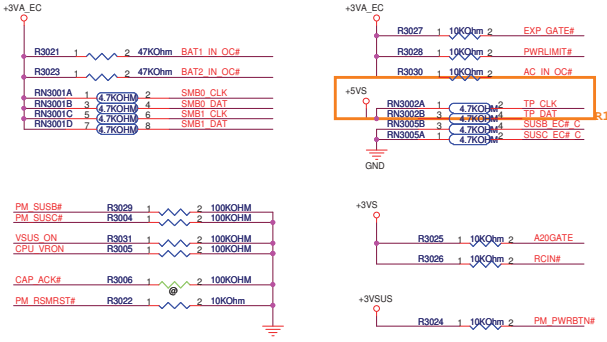
Date: Friday, July 31, 2009 Sheet 29 of 99



For IT8752 Power



For PU / PD

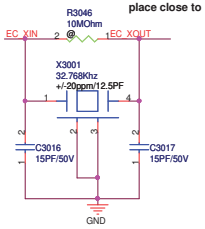


iAMT EC strapping need to check

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For X'tal

Note:
Cload=12.5PF place close to EC



For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

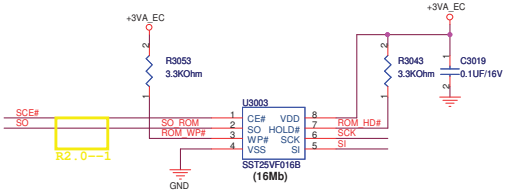
Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK



+3VA_EC	+3VA_EC	<32>
+3VS	+3VS	<16,17,20,21,22,23,24,25,26,27,28,29,32,36,37,40,43,44,45,46,48,50,51,53,56,57,64,65,66,69,70,80,91,92>
+3VSUS	+3VSUS	<27,33,34,37,53,81,82,92>

PEGATRON **Title : EC_IT8512(1)**

BU2/RD1 **Engineer: Kenny Wu**

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 30 of 99

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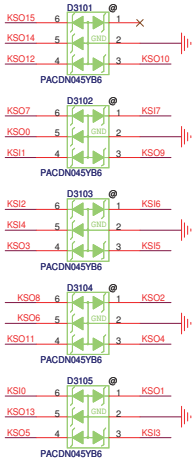

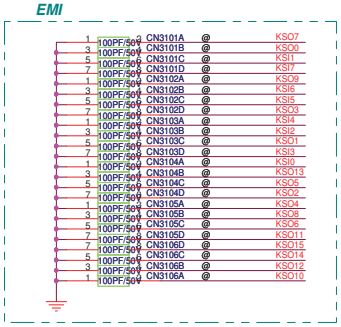

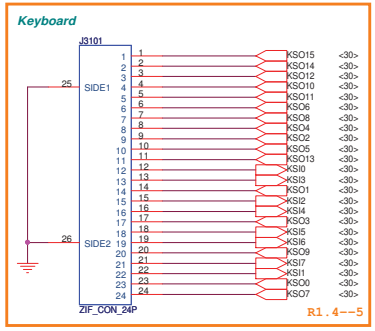

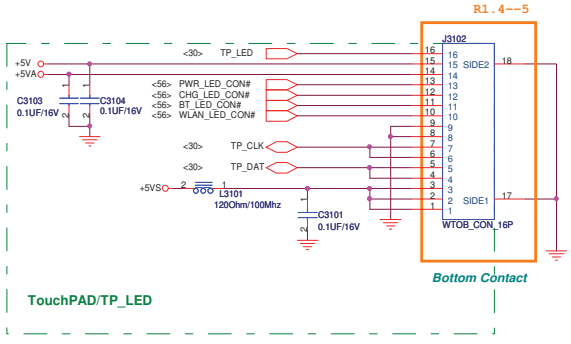

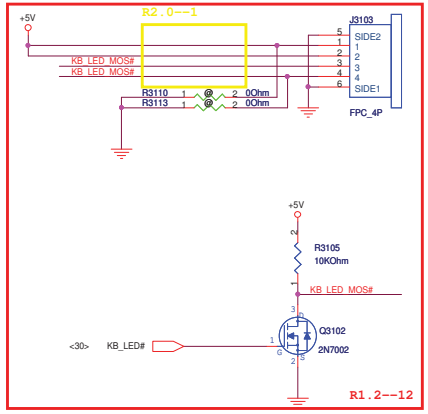

+3VA_EC	+3VA_EC	<30,32>
+3V	+3V	<24,33,43,45,57,61,64,69,91>
+3VS	+3VS	<29,48,80,91,92>
+5VA	+5VA	<56,81,82,83>
+5V	+5V	<36,44,45,52,56,57,65,69,91>
+5VS	+5VS	<27,30,37,45,46,48,50,51,56,57,70,80,91>

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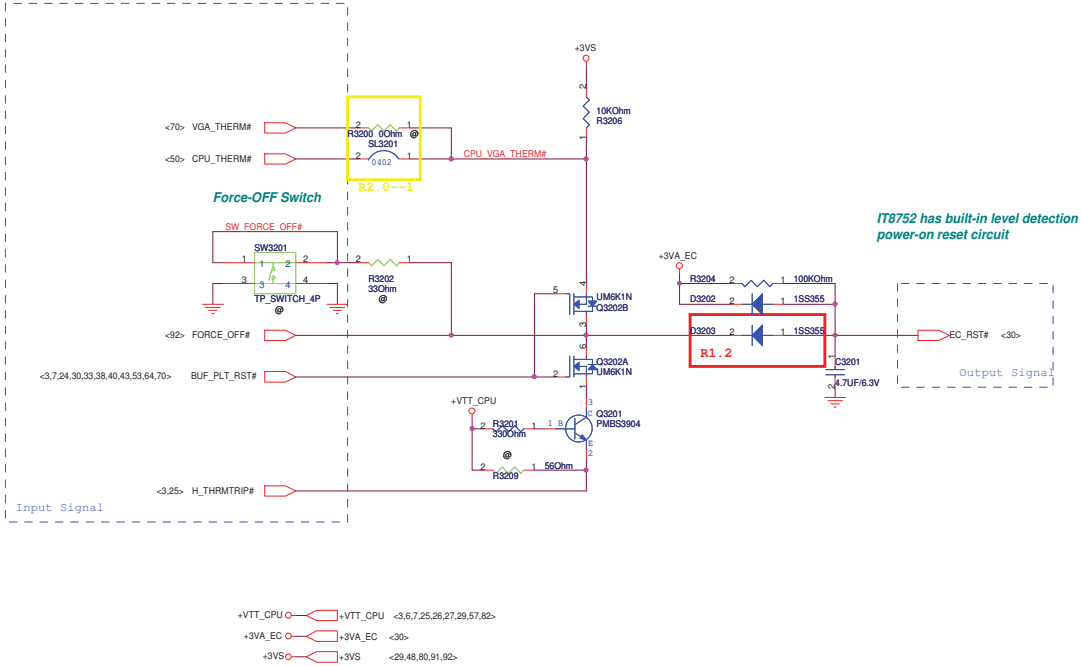
PEGATRON Title : EC_IT8512(2)KB, TP,FP

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 31 of 99

Thermal Policy



+VTT_CPU — +VTT_CPU <3,6,7,25,26,27,29,57,82>

+3VA_EC — +3VA_EC <30>

+3VS — +3VS <29,48,80,91,92>

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PEGATRON Title : RST_Reset Circuit

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 32 of 99

+3VS <29,48,80,91,92>

+3VSUS <27,30,34,37,53,81,82,92>

AR8131:Remove R3301,C3318,C3319

AR8121:Remove L3302,C3317,R3302,C3336

R3301 0Ohm

C3318 close to Pin 1

L3302 4.7UH

+1.7_Pin1

C3316 0.1UF/16V

C3317 10UF/6.3V

C3318 1UF/10V

+AVDD_CEN_LAN

SP3300

R0402

+1.7_Pin6

C3319 1UF/10V

C3336 0.1UF/16V

GND

AR8131 with overclock: Remove R3315

AR8121:Remove R3315

ground pad要打散熱孔

R3315 5.1KOHM

PCIE_TXN6_C <21>

PCIE_TXP6_C <21>

CLK_PCIE_LAN <21>

CLK_PCIE_LAN# <21>

PCIE_RXP6_GLAN <21>

PCIE_RXN6_GLAN <21>

C3335 0.1UF/16V

C3334 0.1UF/16V

PCIE Tx,Rx方向是以南橋爲觀點

Chip pin Tx,Rx是以chip爲觀點

AR8131:Remove C3322,C3321,L3303,L3304

AR8121:Remove C3337,R3324

+AVDDL1 R3303 0Ohm

SP3301 R0402

+AVDD_VCO1

C3337 0.1UF/16V

SP3302 R0402

+AVDD_VCO2

C3323 0.1UF/16V

With overclock:Remove R3303

Not overclock:Remove R3304

For AR8131: Remove R3305,R3306,C3324,C3325,C3326,Q3301

For AR8121: Remove C3327 R3308

Q3301 close to Pin8

R3305 0Ohm

+3V_LAN

C3324 0.1UF/16V

BC807-25 Q3301

R3306 10KOhm

+2.5_Pin5

C3327 0.1UF/16V

C3325 0.1UF/16V

C3326 10UF/6.3V

SP3303 R0402

VDD +2.5V

U3301A

AR8131-AL1E

+1.7_Pin1

+2.5_Pin5

+1.7_Pin6

<22,44,53> PCIE_WAKE#

pin#5的pin name應爲 2.5V

SEL_25M

R3310 4.7KOhm

C3333 1000PF/16V

C3332 1UF/10V

C3331 0.1UF/16V

AR8121:Remove R3310

AR8131/25MHz:Remove R3310 C3333

RBIAS

R3311 2.37KOHM

AR8121: Remove R3313

AR8131: Remove R3314

SL3302

CLK_REQ_LAN

CLK_REQ5_LAN# <21>

R3314 0Ohm

VDD +2.5V

SL3312

Q3300 2N7002

<3,7,24,30,32,38,40,43,53,64,70> BUF_PLT_RST#

U3301B

AR8131-AL1E

L_TRDP0

L_TRDN0

L_TRDP1

L_TRDN1

L_TRDP2

L_TRDN2

L_TRDP3

L_TRDN3

RN3301A 49.9OHM

RN3301B 49.9OHM

RN3301C 49.9OHM

RN3301D 49.9OHM

RN3302A 49.9OHM

RN3302B 49.9OHM

RN3302C 49.9OHM

RN3302D 49.9OHM

0.1UF/25V

CX3301A

CX3301B

CX3301C

CX3301D

+3VSUS

L3301 80Ohm/100Mhz

+3V_LAN

C3301 10UF/6.3V

C3302 10UF/6.3V

C3303 1UF/10V

C3304 0.1UF/16V

C3301 C3302 C3303 C3304 close to pin2

VDD +2.5V

C3305 1UF/10V

C3306 0.1UF/16V

C3307 0.1UF/16V

C3305 close to pin15

+3VDDL

C3308 1UF/10V

C3309 0.1UF/16V

C3310 0.1UF/16V

C3311 0.1UF/16V

C3308 close to pin45/46

+AVDDL

C3312 0.1UF/16V

C3313 0.1UF/16V

C3314 0.1UF/16V

C3315 0.1UF/16V

X2_LAN

X1_LAN

C3328 10PF/50V

T3300 EXT_25/48

X3301 25Mhz

C3329 27PF/50V

C3330 27PF/50V

AR8121:Remove C3328

AR8131/25MHz: Remove C3328

For AR8131 : Remove R3309

+1.7_Pin6

R3309 0Ohm

VDD +2.5V

R1.4--5

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PEGATRON Title : LAN_AR8131

BU2/RD1 Engineer: Kenny Wu

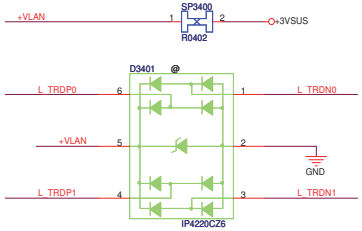
Size	Project Name	Rev
C	G60J	1.4

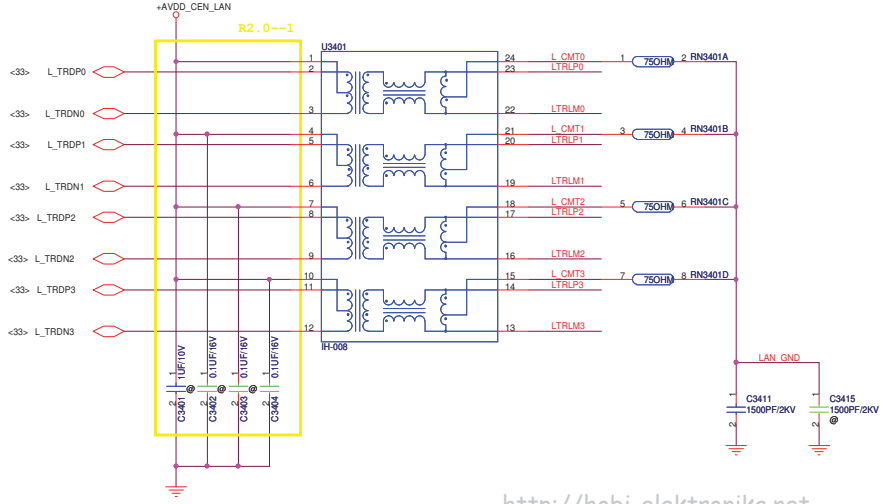
Date: Friday, July 31, 2009 Sheet 33 of 99

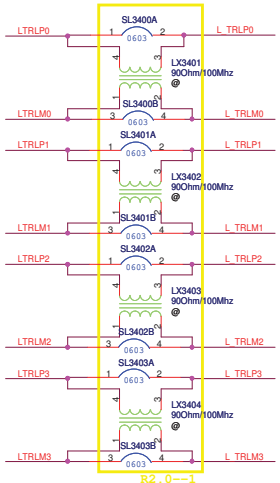
STUFF for NON_IAMT

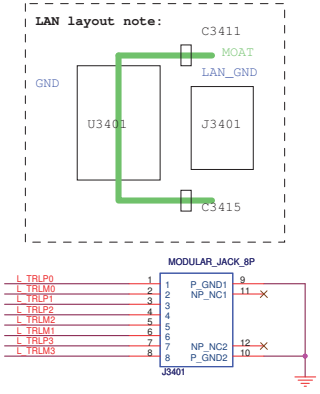
STUFF for IAMT

R1.4-2









PEGATRON Title : LAN_HVL_RJ45

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : MDC_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 35 of 99

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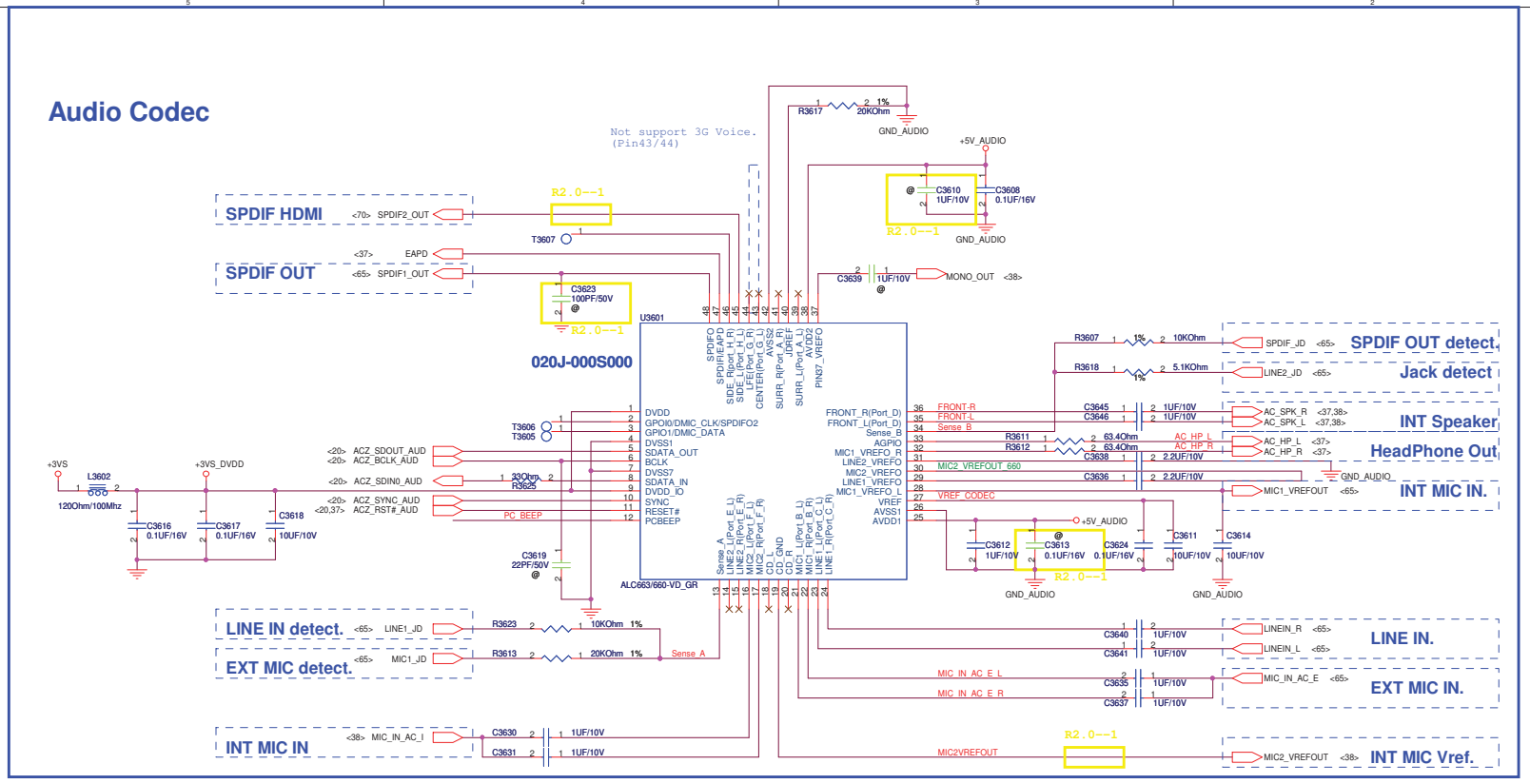
Audio Codec

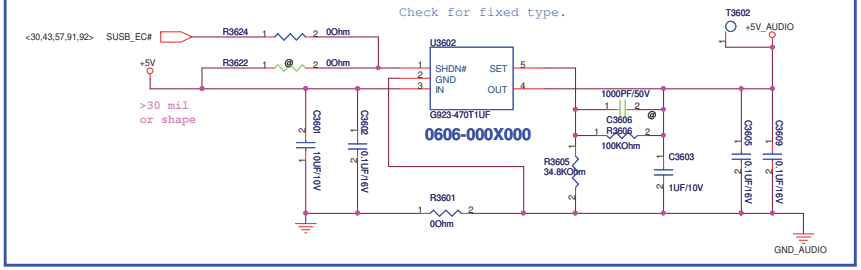


Audio Power

FOR ADJUST MODE:

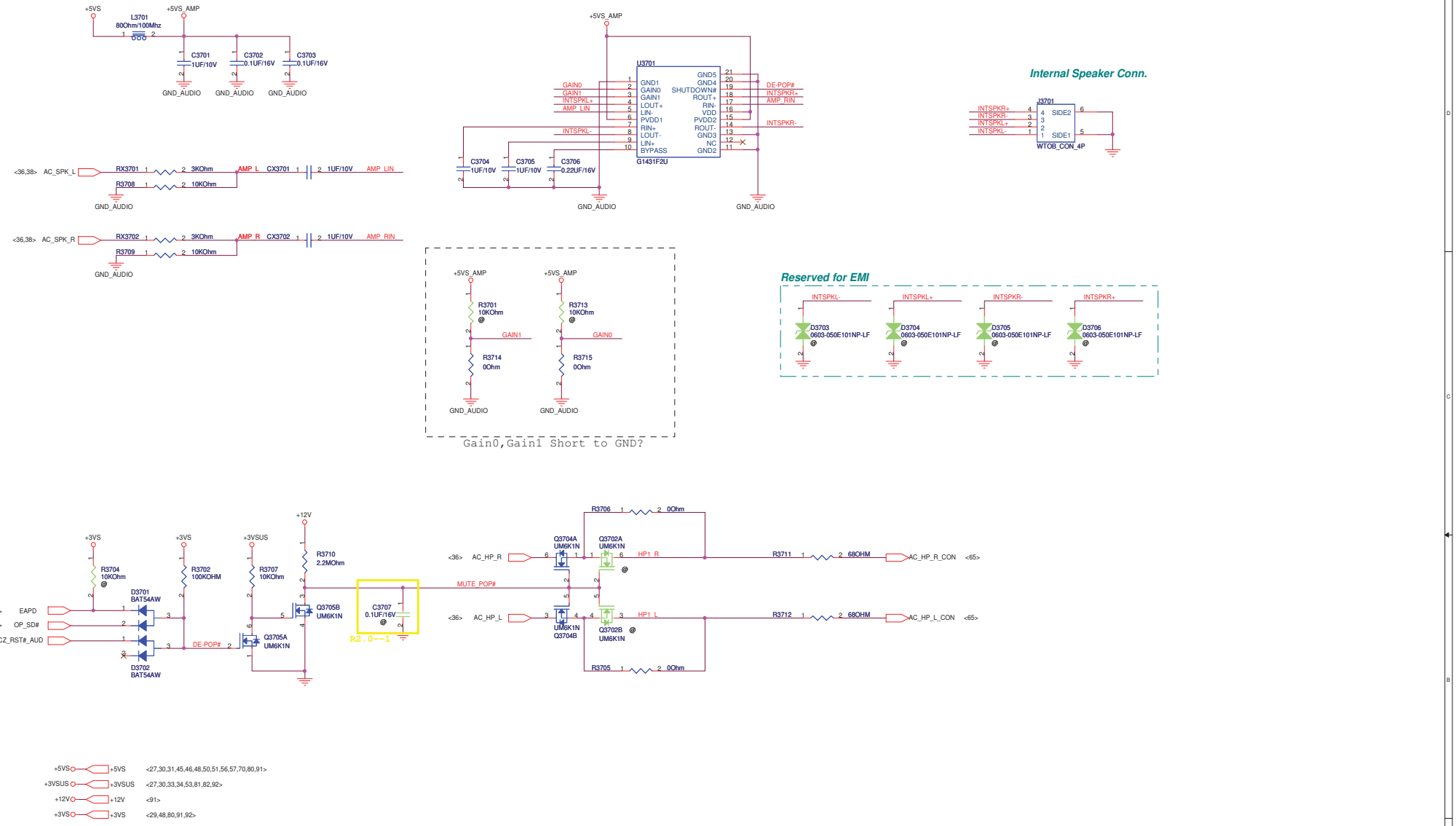
Vo=1.25*(1+R3706/R3705)

=1.25*(1+ 100K/34.8K) = 4.84



http://hobi-elektronika.net

PEGATRON	Title : AUD(1)_ALC663VD		
BU2/RD1	Engineer: Kenny Wu		
Size: C	Project Name: G60J		Rev: 1.4
Date: Friday, July 31, 2009	Sheet 36 of 99		



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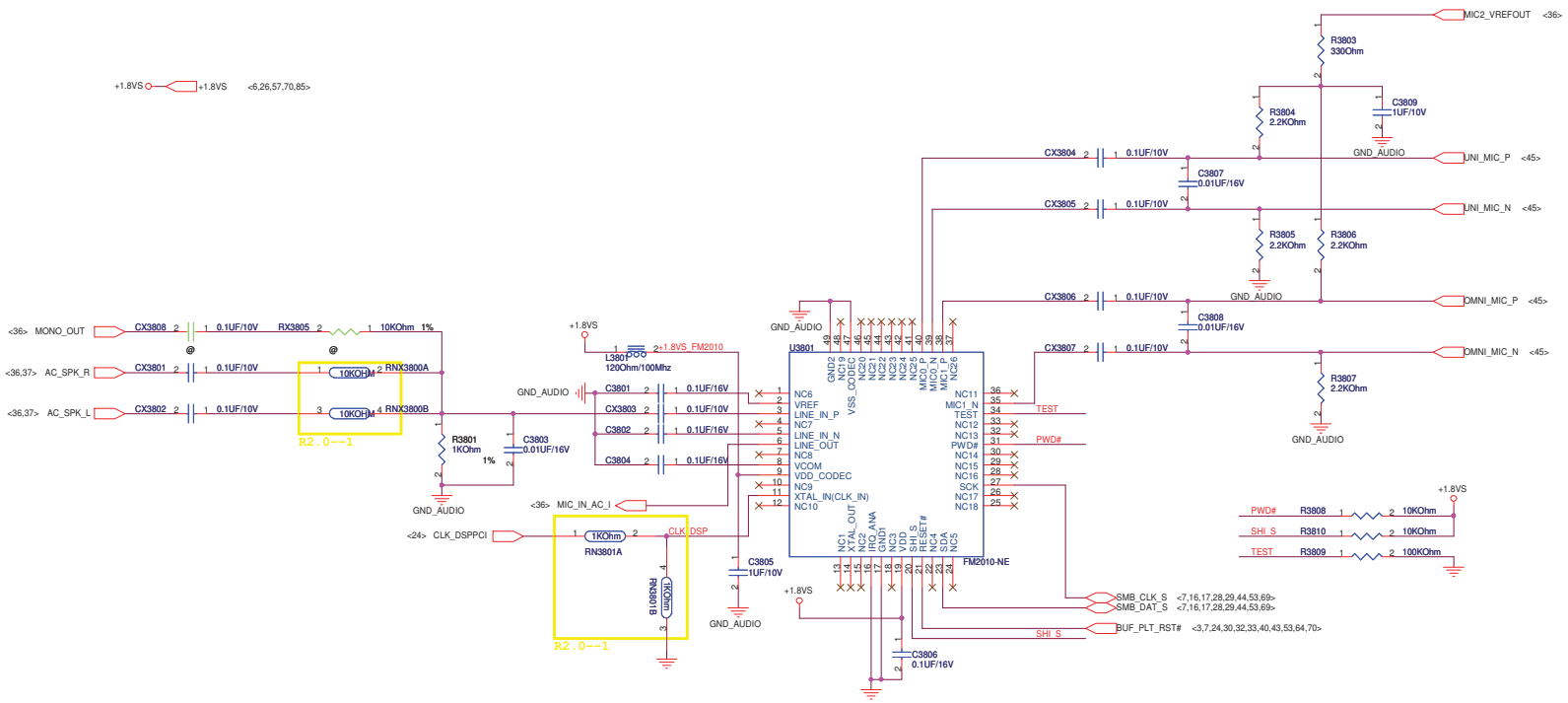
PEGATRON Title : AUD(2)_AMP,JACK

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 37 of 99



http://hobi-elektronika.net

PEGATRON Title : AUD(3)_FM2010

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 38 of 99

PEGATRON	Title : AUD(4)_****				
BU2/RD1	Engineer: Kenny Wu				
Size: Custom	Project Name: G60J				Rev: 1.4
Date: Friday, July 31, 2009	Sheet 39 of 99				

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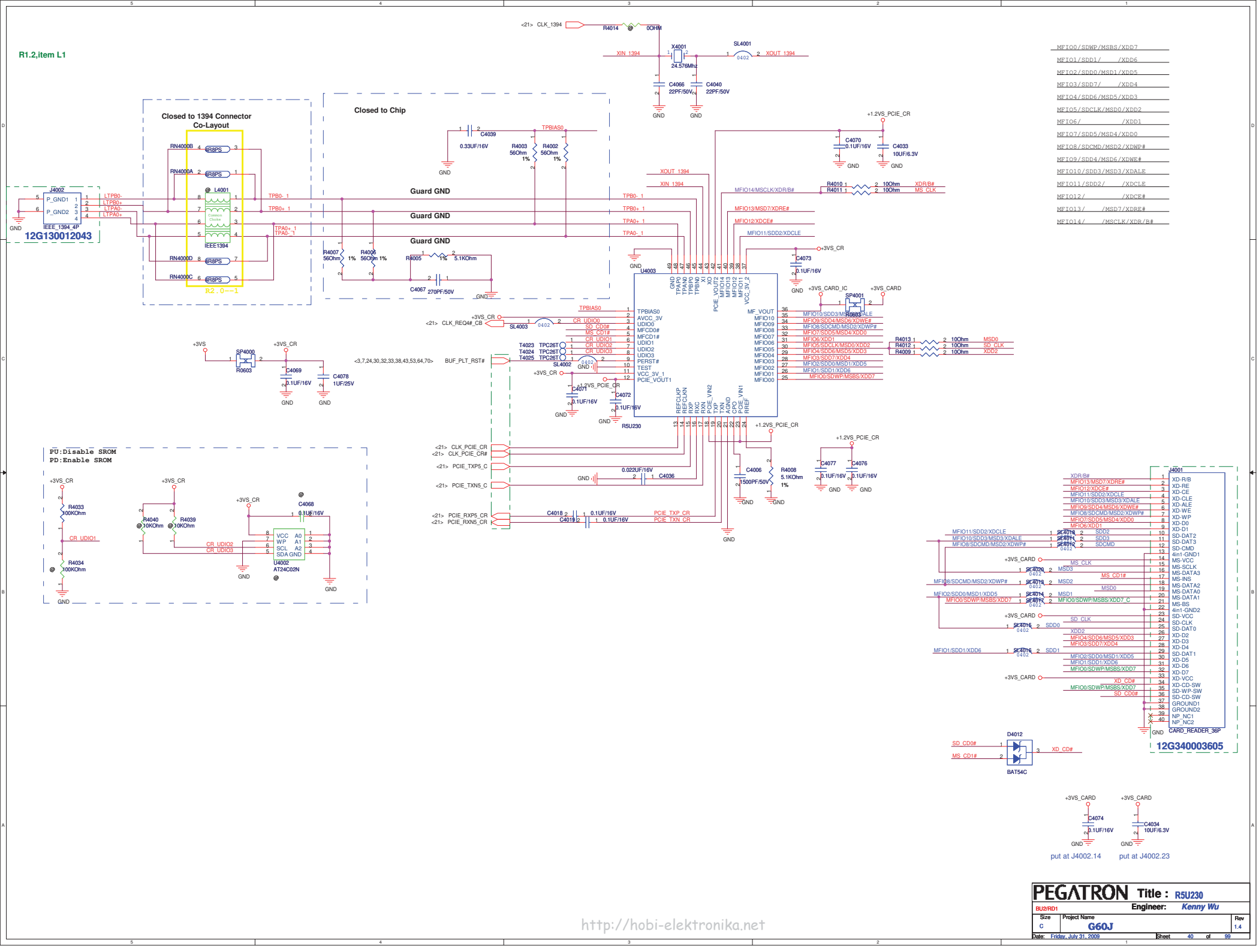
R1.2,item L1


Closed to 1394 Connector Co-Layout
Closed to Chip
Guard GND
Guard GND
Guard GND
R2.0--1
12G130012043
12G340003605
U4003
R5U230
U4002
AT24C02N
SP4000
SP4001
SL4001
SL4002
SL4003
J4002
J4001
IEEE_1394_4P
IEEE1394
CARD_READER_36P
BAT54C
PU:Disable SROM
PD:Enable SROM
put at J4002.14
put at J4002.23
http://hobi-elektronika.net
PEGATRON
Title : R5U230
Engineer: Kenny Wu
BU2/RD1
Size C
Project Name G60J
Rev 1.4
Date: Friday, July 31, 2009
Sheet 40 of 99

<29,48,80,91,92>

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PEGATRON Title : CB(2)_R5C833

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 41 of 99

<29,48,80,91,92>

<37,91>

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PEGATRON Title : CB(3)_4in1 CardReader

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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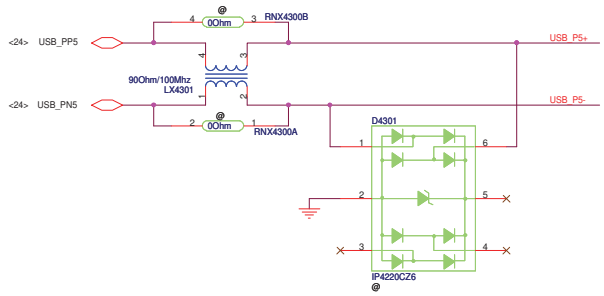
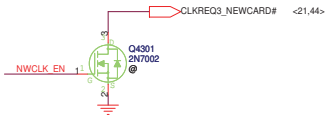
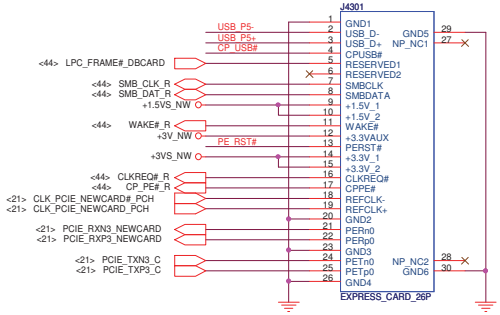
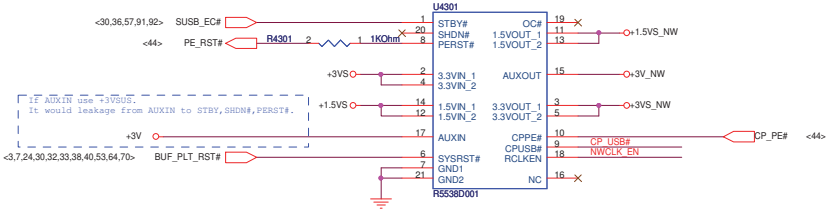
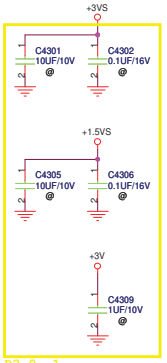


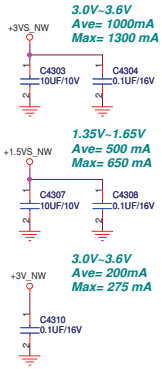


NewCard Header

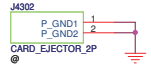








NewCard Ejecter



http://hobi-elektronika.net

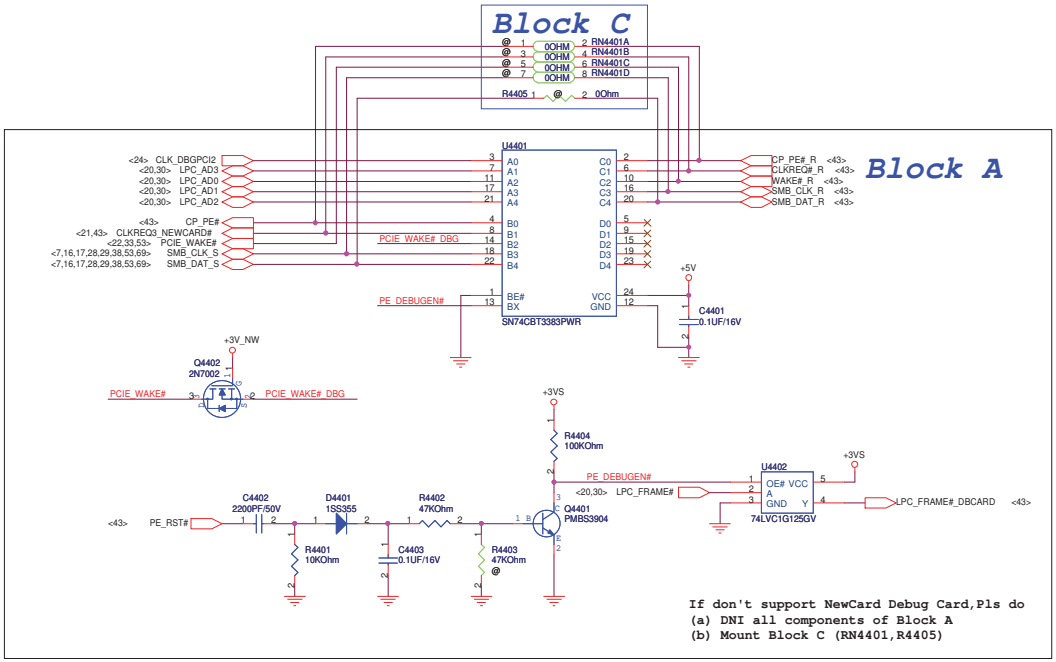
PEGATRON Title : CB(4)_NewCard

BU2/RD1 Engineer: Kenny Wu

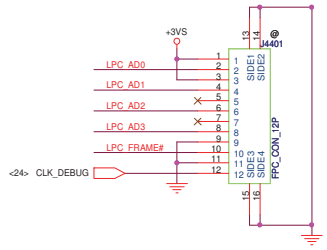
Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 43 of 99

For NewCard Debug Card



LPC Debug Port



+5V +5V <31,36,45,52,56,57,65,69,91>

+3VS +3VS <29,48,80,91,92>

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PEGATRON Title : BUG_Debug

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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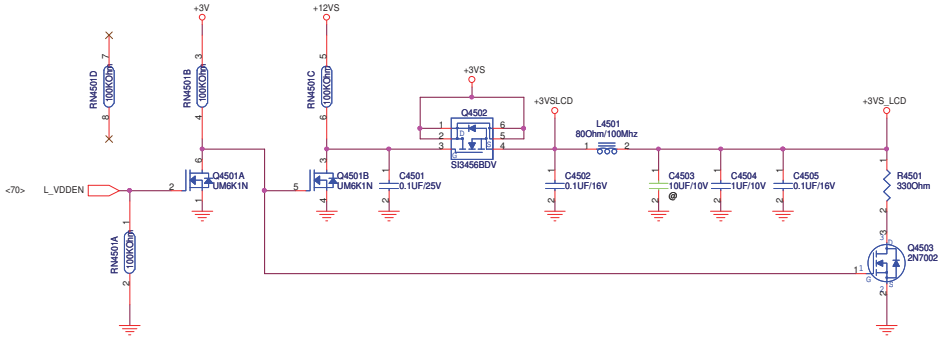
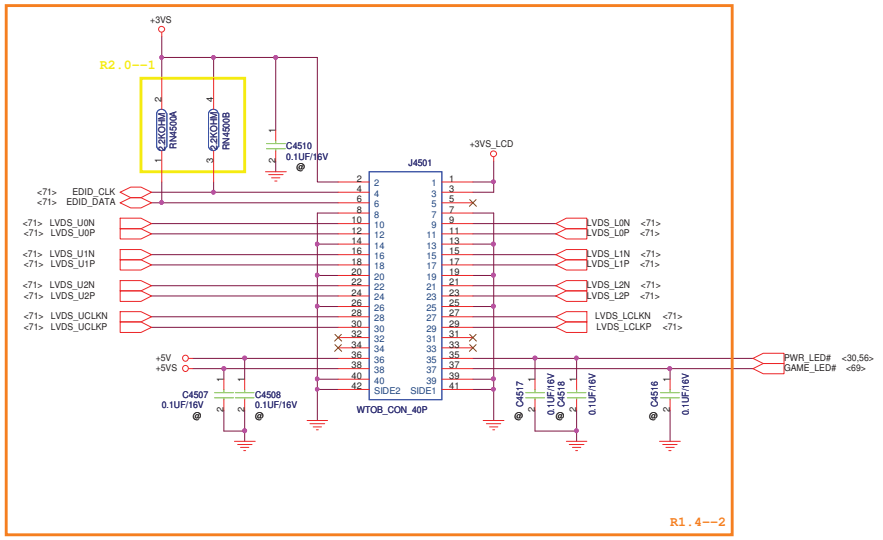
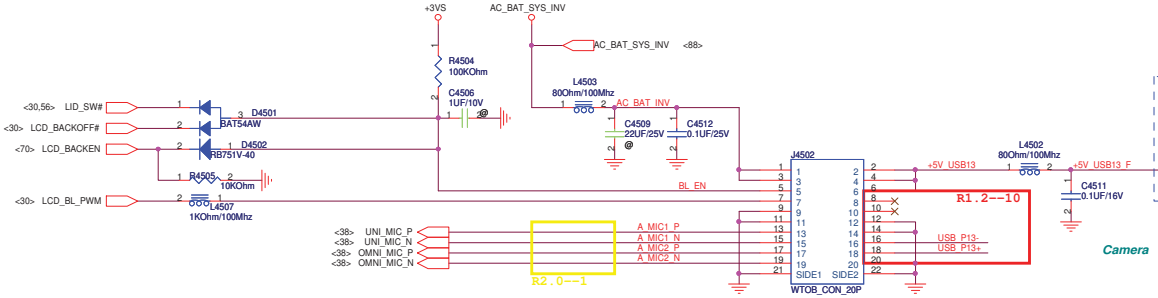
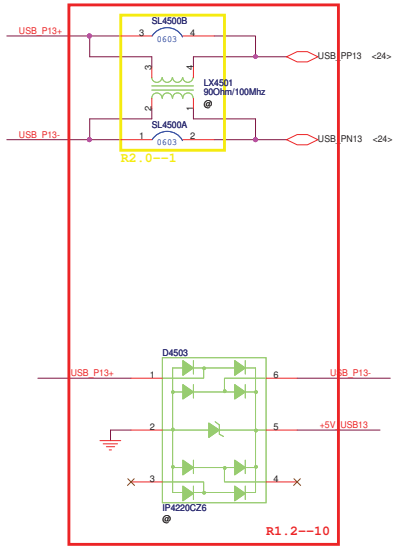




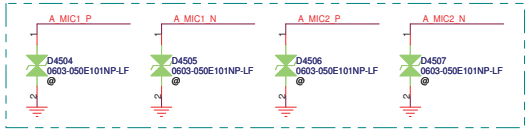


This setting is for M52J/G50J colay:
M52J:Camera*1 (F4501,L4502 can cost down)
G50J: USB portx1,Camerax1.

Camera



Reserved for EMI



+3VS	+3VS	<29,48,80,91,92>
+3V	+3V	<24,33,43,57,61,64,69,91>
+12VS	+12VS	<28,91>
+5V	+5V	<31,36,44,52,56,57,65,69,91>
+5VS	+5VS	<27,30,31,37,46,48,50,51,56,57,70,80,91>

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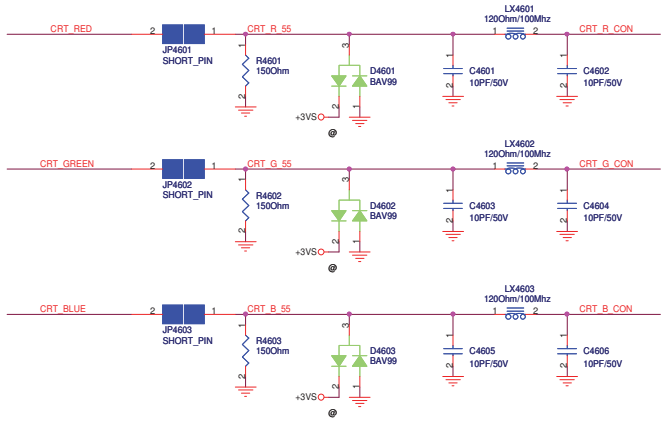
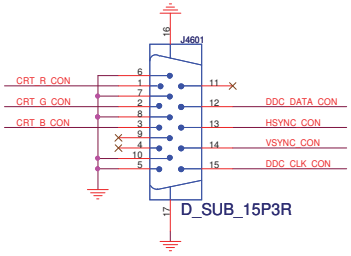
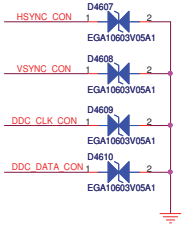
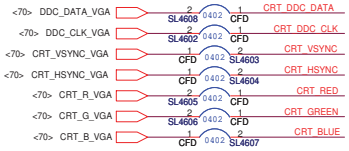
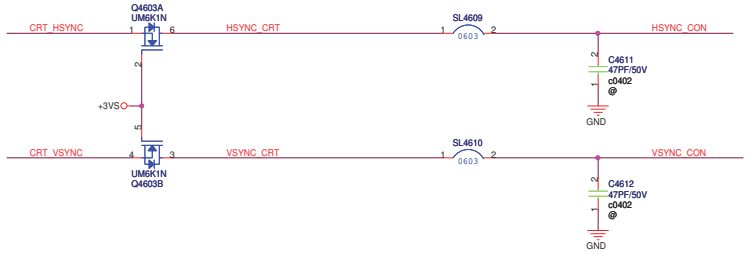
PEGATRON	Title : CRT(1)_LVDS	
BU2/RD1	Engineer: Kenny Wu	
Size: C	Project Name: G60J	Rev: 1.4
Date: Friday, July 31, 2009	Sheet 45 of 99	

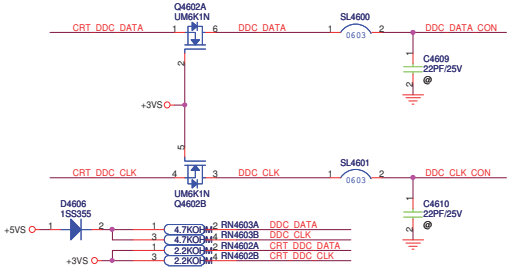












+3VS — +3VS <29,48,80,91,92>

+5V — +5V <31,36,44,45,52,56,57,65,69,91>

+5VS — +5VS <27,30,31,37,45,48,50,51,56,57,70,80,91>

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PEGATRON Title : CRT(2)_D-Sub

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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R2.0

+3VS +3VS <29,48,80,91,92>

+5VS +5VS <27,30,31,37,45,46,48,50,51,56,57,70,80,91>

http://hobi-elektronika.net

PEGATRON Title : CRT(3)_Display Port

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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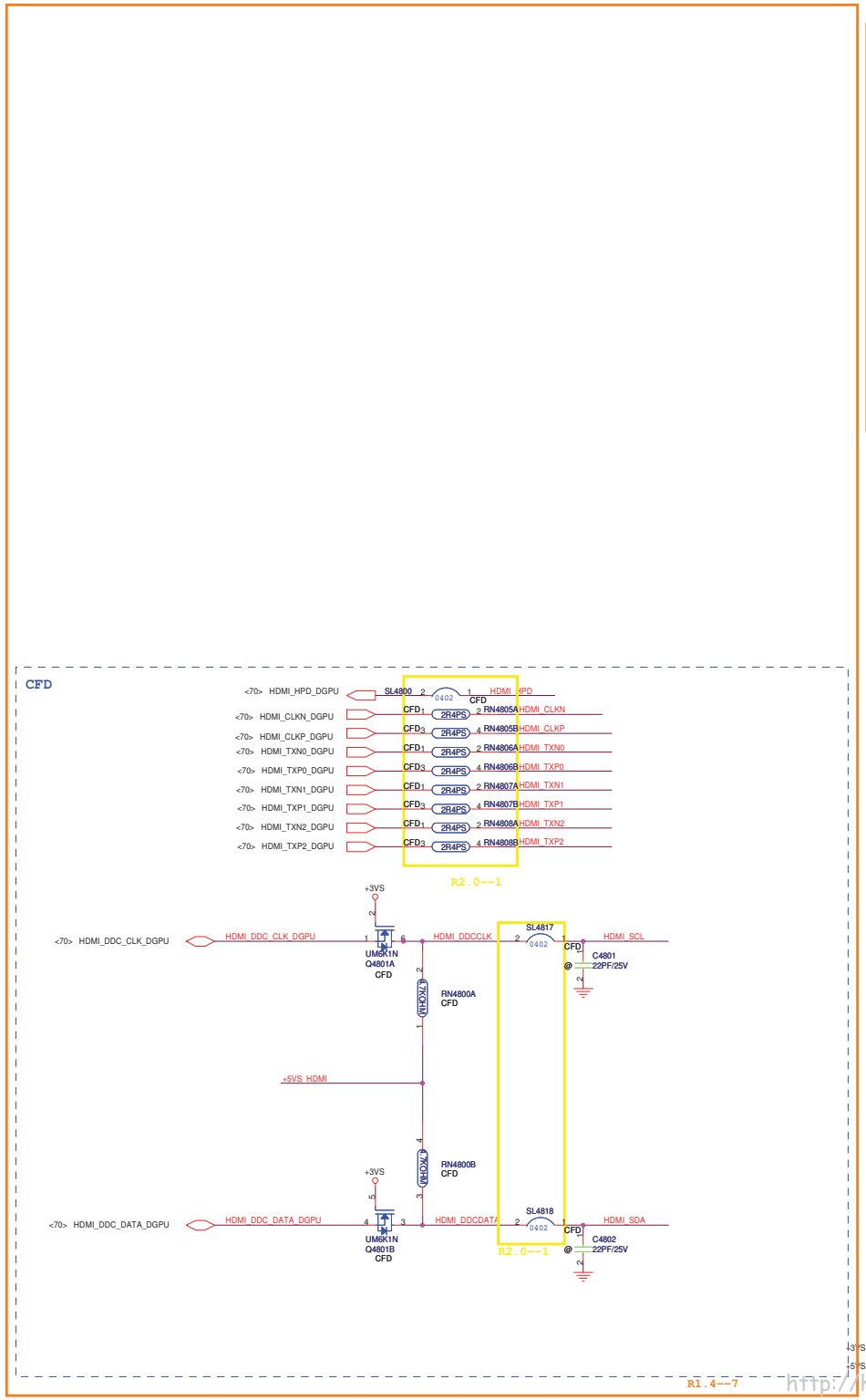

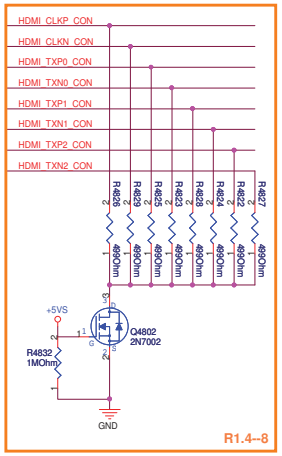

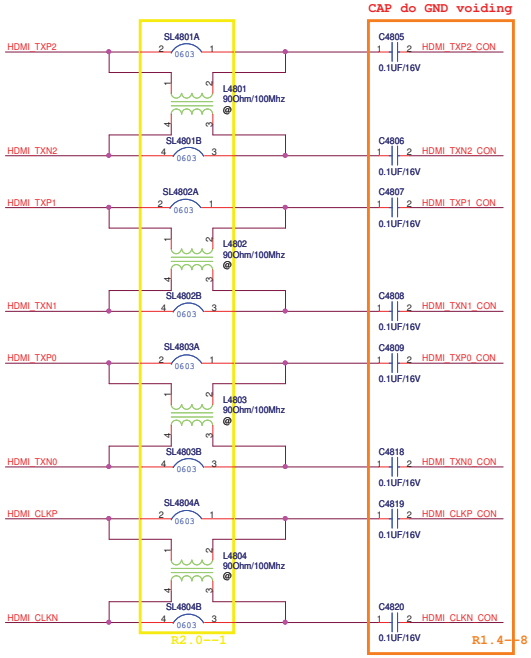

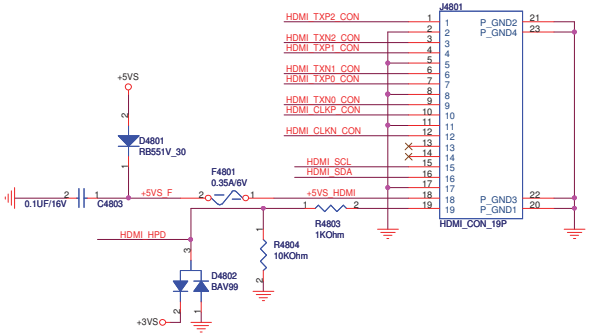

+3VS +3VS <29,80,91,92>
+5VS +5VS <27,30,31,37,45,46,50,51,56,57,70,80,91>

http://hobi-elektronika.net

PEGATRON	Title : TV(1)_HDMI	
BU2/RD1	Engineer: Kenny Wu	
Size: C	Project Name: G60J	Rev: 1.4
Date: Friday, July 31, 2009	Sheet 48 of 99	

PEGATRON Title : TV(2)_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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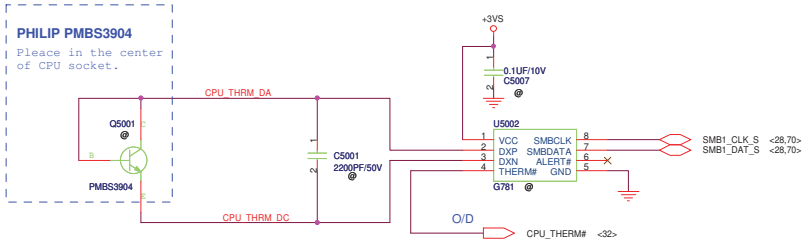
+3VS +3VS <29,48,80,91,92>

+5VS +5VS <27,30,31,37,45,46,48,51,56,57,70,80,91>

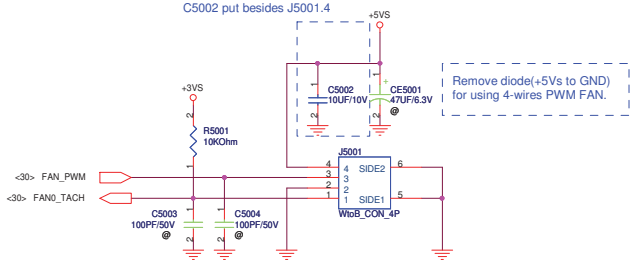
CPU Thermal Sensor



SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan



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PEGATRON Title : FAN_Fan,Sensor

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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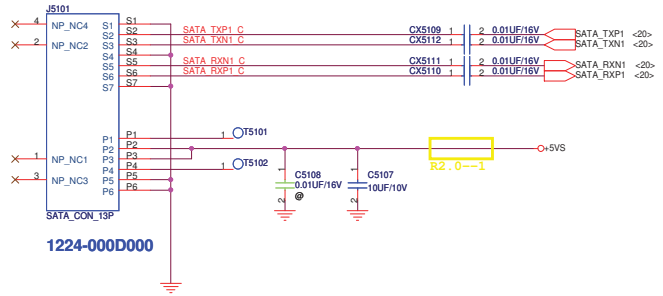
ODD

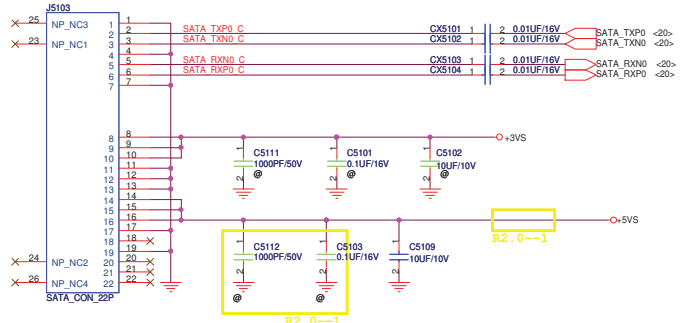


1224-000D000

+3VS <29,48,80,91,92>

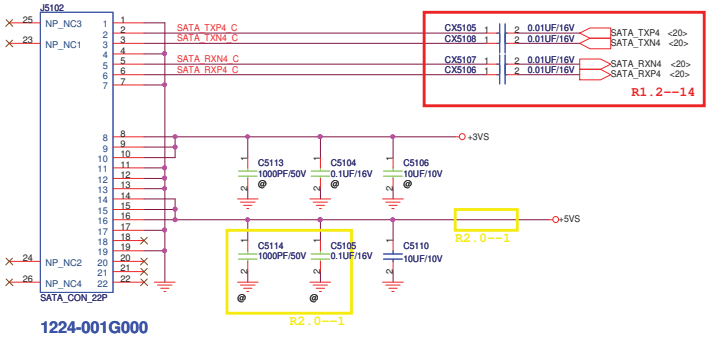
+5VS <27,30,31,37,45,46,48,50,56,57,70,80,91>

HDD (1st)



1224-000W000

HDD (2nd)



1224-001G000

http://hobi-elektronika.net

PEGATRON Title : XDD_HDD,ODD

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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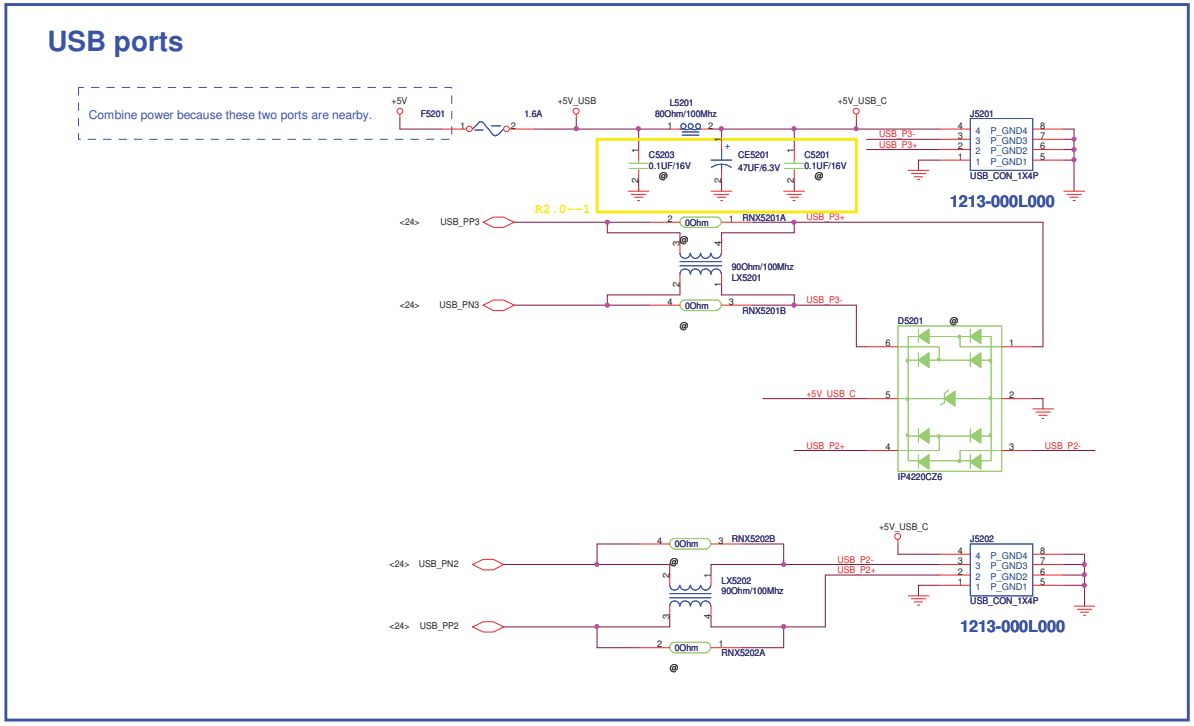
+5V +5V <31,36,44,45,56,57,65,69,91>

USB ports

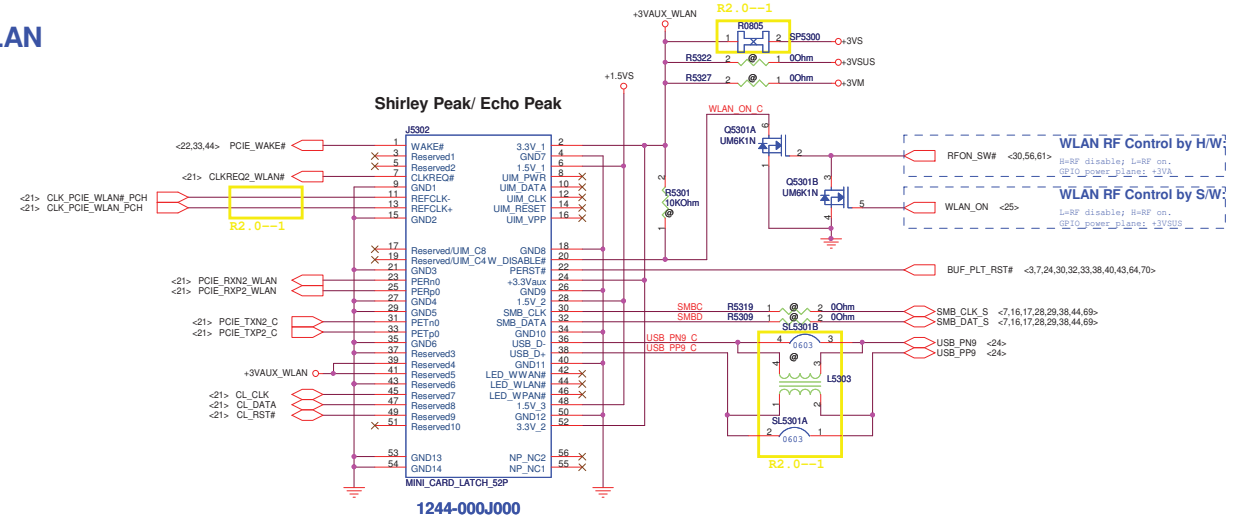


http://hobi-elektronika.net

PEGATRON	Title : USB_USB Port	
BU2/RD1	Engineer: Kenny Wu	
Size: C	Project Name: G60J	Rev: 1.4
Date: Friday, July 31, 2009	Sheet 52 of 99	

+3VS +3VS <29,48,80,91,92>
+3VSUS +3VSUS <27,30,33,34,37,81,82,92>
+1.5VS +1.5VS <26,43,57,64,91>
+3VM +3VM <26,28,57,91,92>

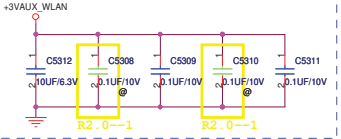
WLAN



WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

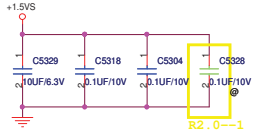
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

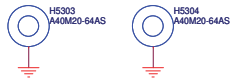


WLAN nuts:

Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.



http://hobi-elektronika.net

PEGATRON Title : MINICARD_WLAN

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : BAR_****

BU2/RD1 Engineer: *Kenny Wu*

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : SIO_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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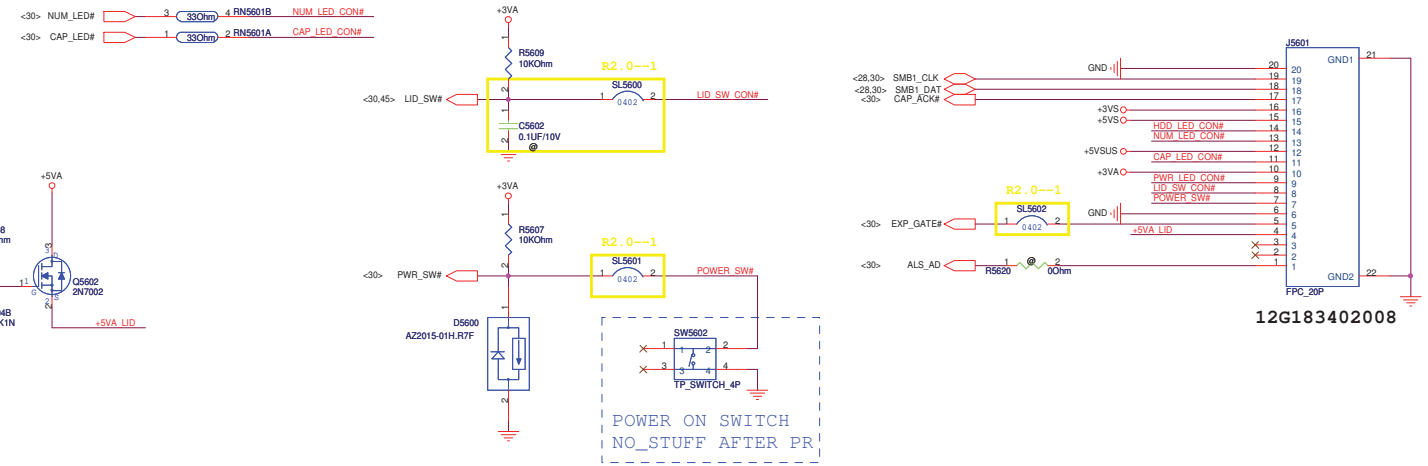
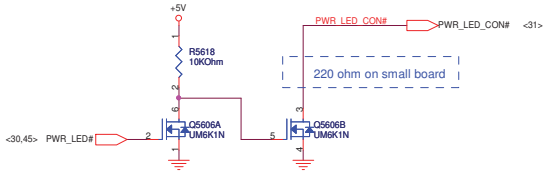
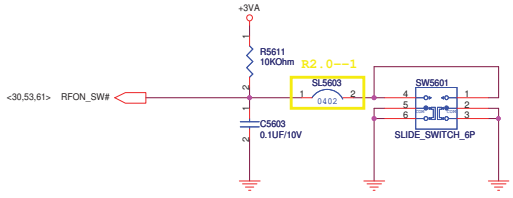
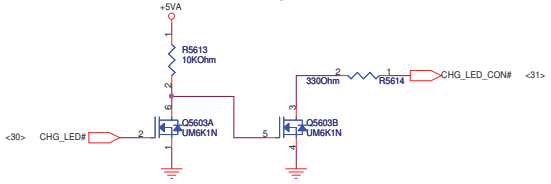


Power LED

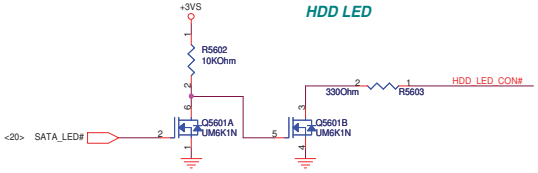




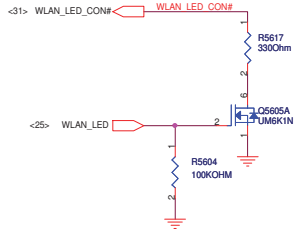
Charger LED



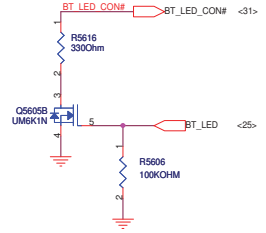
HDD LED



WLAN LED



BT LED



+3VA	+3VA	<20,30,57,81,90,93>
+3VS	+3VS	<29,48,80,91,92>
+5VSUS	+5VSUS	<27,81,91>
+5VA	+5VA	<31,81,82,83>
+5V	+5V	<31,36,44,45,52,57,65,69,91>
+5VS	+5VS	<27,30,31,37,45,46,48,50,51,57,70,80,91>
AC_BAT_SYS	AC_BAT_SYS	<70,80,81,82,83,88>

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PEGATRON Title : LED_Indicator

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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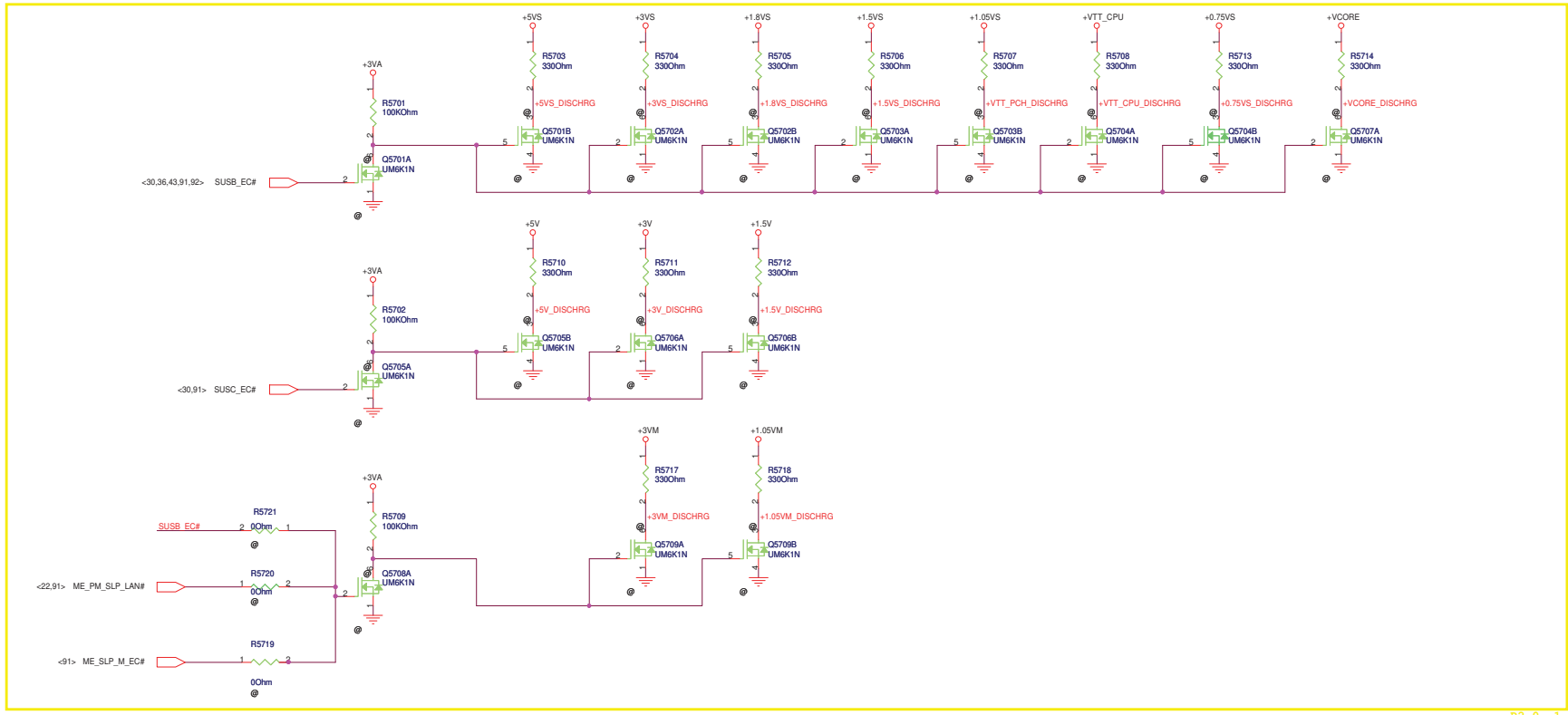
+3VA +3VA <20,30,56,81,90,93>
+VCORE +VCORE <6,69,80>
+VGFX_CORE +VGFX_CORE
+VTT_CPU +VTT_CPU <3,6,7,25,26,27,29,32,82>
+0.75VS +0.75VS <16,17,83>
+1.05VS +1.05VS <26,27,69,91>
+1.5VS +1.5VS <26,43,53,64,91>
+1.8VS +1.8VS <6,26,38,70,85>
+3VS +3VS <29,48,80,91,92>
+5VS +5VS <27,30,31,37,45,46,48,50,51,56,70,80,91>
+1.5V +1.5V <3,6,16,69,83>
+3V +3V <24,33,43,45,61,64,69,91>
+5V +5V <31,36,44,45,52,56,65,69,91>
+1.05VM_LAN +1.05VM_LAN
+3VM +3VM <26,28,53,91,92>
+1.05VM +1.05VM <27,69,91,92>



R2.0--1

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PEGATRON Title : DSG_Discharge
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
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PEGATRON Title : PCI_****

BU2/RD1 Engineer: *Kenny Wu*

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : DJ_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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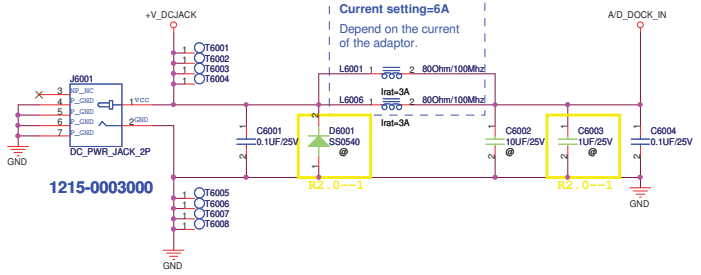
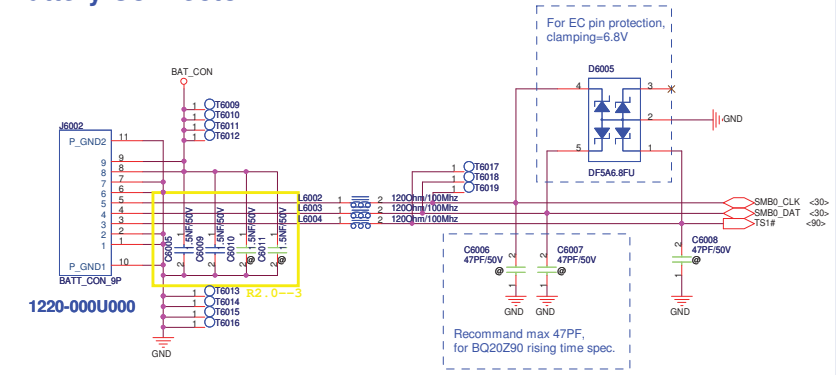
DC Jack



Battery Connector



+VCC_RTC — +VCC_RTC <20,27>
+3VA_EC — +3VA_EC <30,32>
+3VA — +3VA <20,30,56,57,81,90,93>
+5VA — +5VA <31,56,81,82,83>

+3VSUS — +3VSUS <27,30,33,34,37,53,81,82,92>
+5VSUS — +5VSUS <27,56,81,91>
+12VSUS — +12VSUS <28,81,91>

+1.5V — +1.5V <3,6,16,57,69,83>
+3V — +3V <24,33,43,45,57,61,64,69,91>
+5V — +5V <31,36,44,45,52,56,57,65,69,91>
+12V — +12V <37,91>

+0.75VS — +0.75VS <16,17,57,83>
+1.05VS — +1.05VS <26,27,57,69,91>
+1.5VS — +1.5VS <26,43,53,57,64,91>
+1.8VS — +1.8VS <6,26,38,57,70,85>
+3VS — +3VS <29,48,80,91,92>
+5VS — +5VS <27,30,31,37,45,46,48,50,51,56,57,70,80,91>
+12VS — +12VS <28,45,91>

AC_BAT_SYS_INV — AC_BAT_SYS_INV <45,88>
AC_BAT_SYS — AC_BAT_SYS <56,70,80,81,82,83,88>
A/D_DOCK_IN — A/D_DOCK_IN <88>
BAT_CON — BAT_CON <88>

+1.5V_DDR3 — +1.5V_DDR3 <16,17,18>
+VTT_CPU — +VTT_CPU <3,6,7,25,26,27,29,32,57,82>
+VCORE — +VCORE <6,57,69,80>
+VGFX_CORE — +VGFX_CORE
+VTT_PCH_ORG — +VTT_PCH_ORG <21,22,26,27>
+VTT_PCH_VCCIO — +VTT_PCH_VCCIO <20,26,27>
+1.05VM_ORG — +1.05VM_ORG <27>
+V_NVRAM_VCCQ — +V_NVRAM_VCCQ <26>
M_VREFCA_DIMM0 — M_VREFCA_DIMM0 <16,18>
M_VREFDQ_DIMM0 — M_VREFDQ_DIMM0 <16,18>
M_VREFCA_DIMM1 — M_VREFCA_DIMM1 <17,18>
M_VREFDQ_DIMM1 — M_VREFDQ_DIMM1 <17,18>

PEGATRON Title : DC_DC/BAT CONN
BU2/RD1 Engineer: Kenny Wu
Size C | Project Name G60J | Rev 1.4
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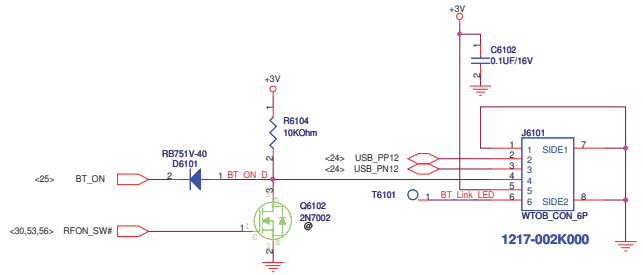
+3V +3V <24,33,43,45,57,64,69,91>

BLUETOOTH



http://hobi-elektronika.net

PEGATRON Title : BT_Bluetooth

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : TPM_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : FP_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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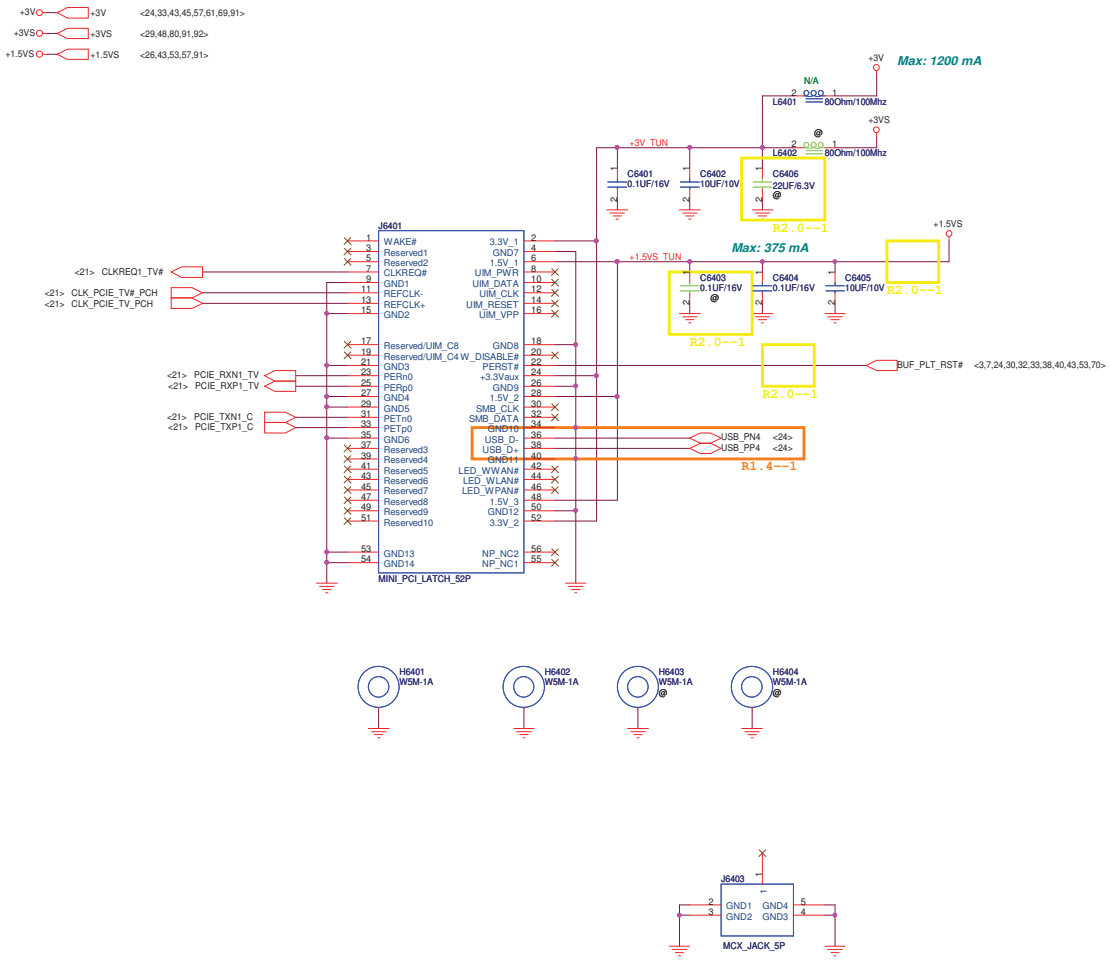

http://hobi-elektronika.net

PEGATRON Title : TUN_TV Tuner

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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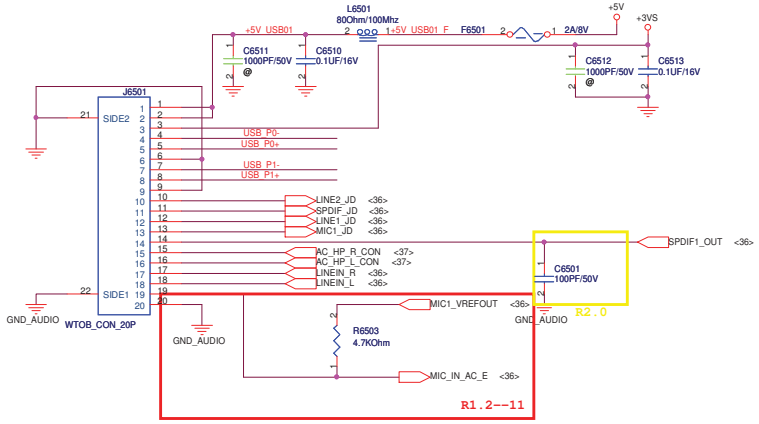
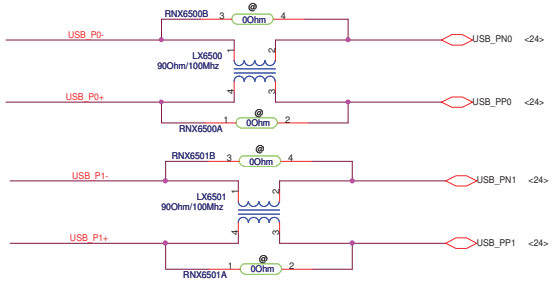
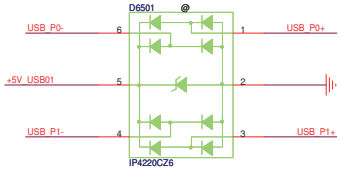
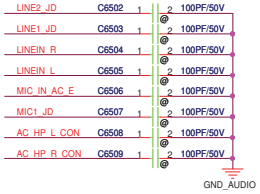


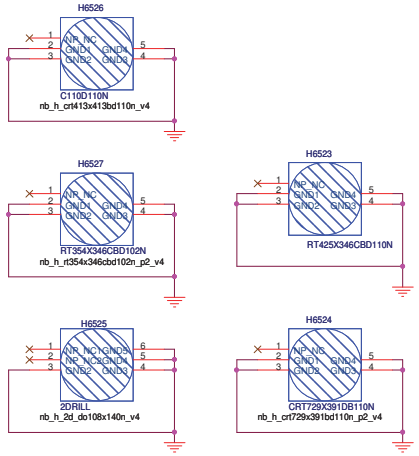


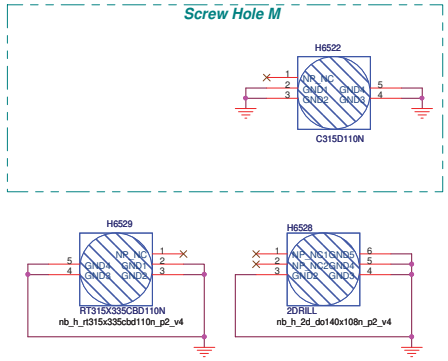


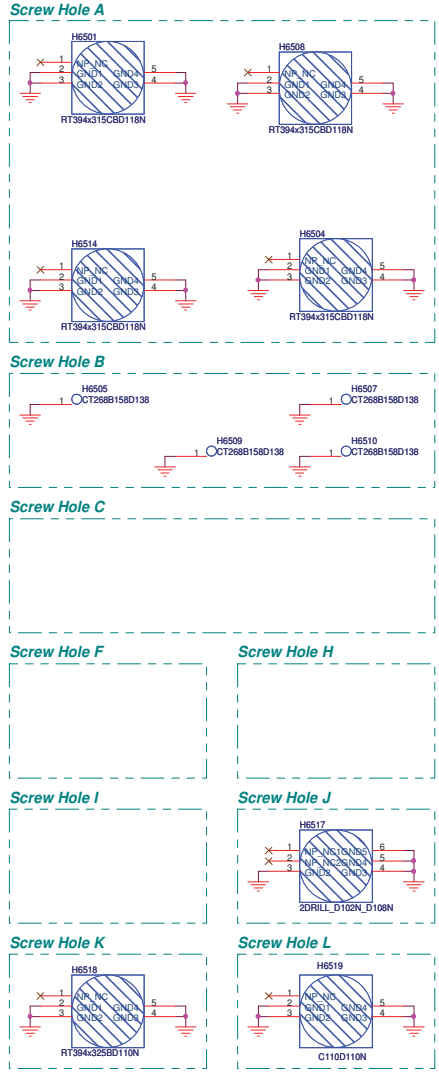


+3VS +3VS <29,48,80,91,92>

+5V +5V <31,36,44,45,52,56,57,69,91>







http://hobi-elektronika.net

PEGATRON Title : ME_CONN,Skew Hole

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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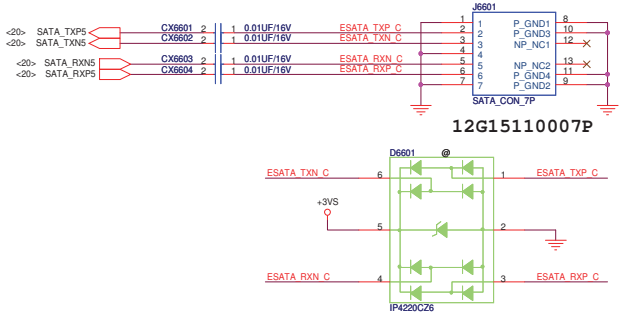
+3VS +3VS <29,48,80,91,92>

+1.8VS +1.8VS <6,26,38,57,70,85>

E-SATA connector



http://hobi-elektronika.net

PEGATRON Title : ESA_ESATA

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : ONFI

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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PEGATRON Title : OTH_LCM

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

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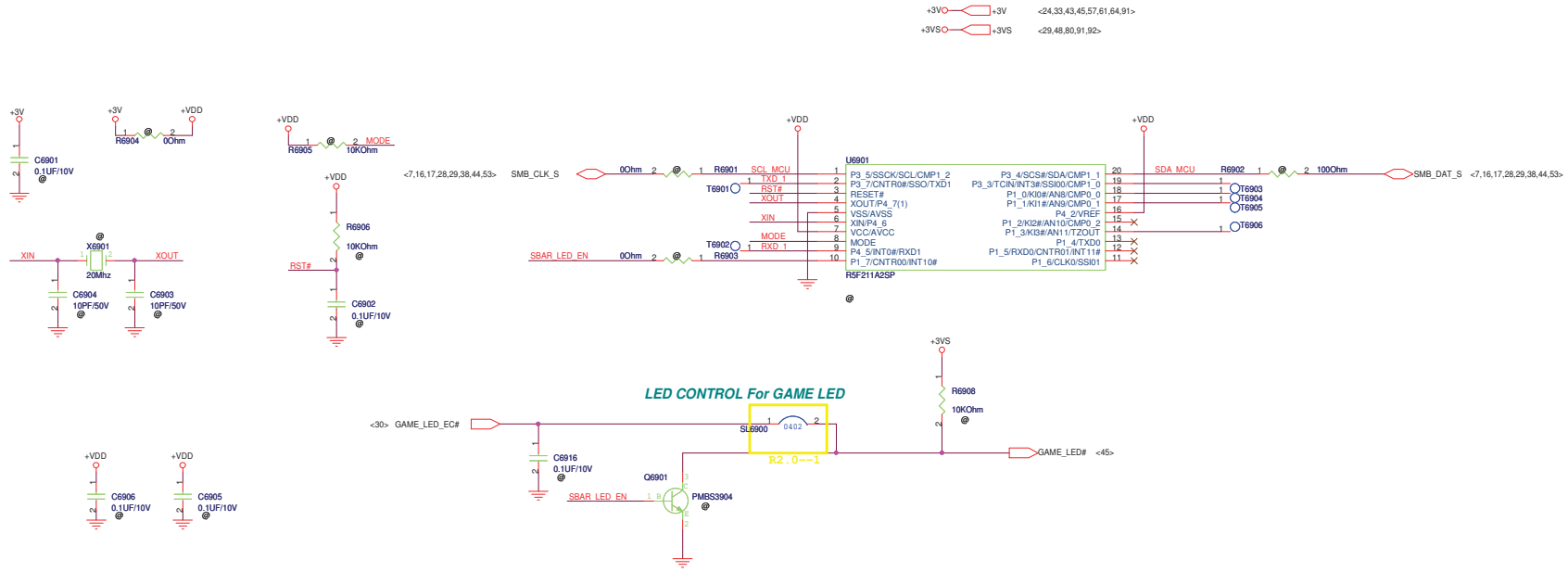
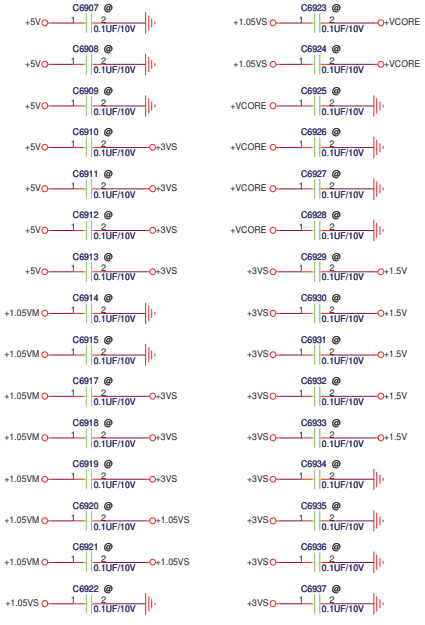
May to be deleted..



For EMI request



http://hobi-elektronika.net

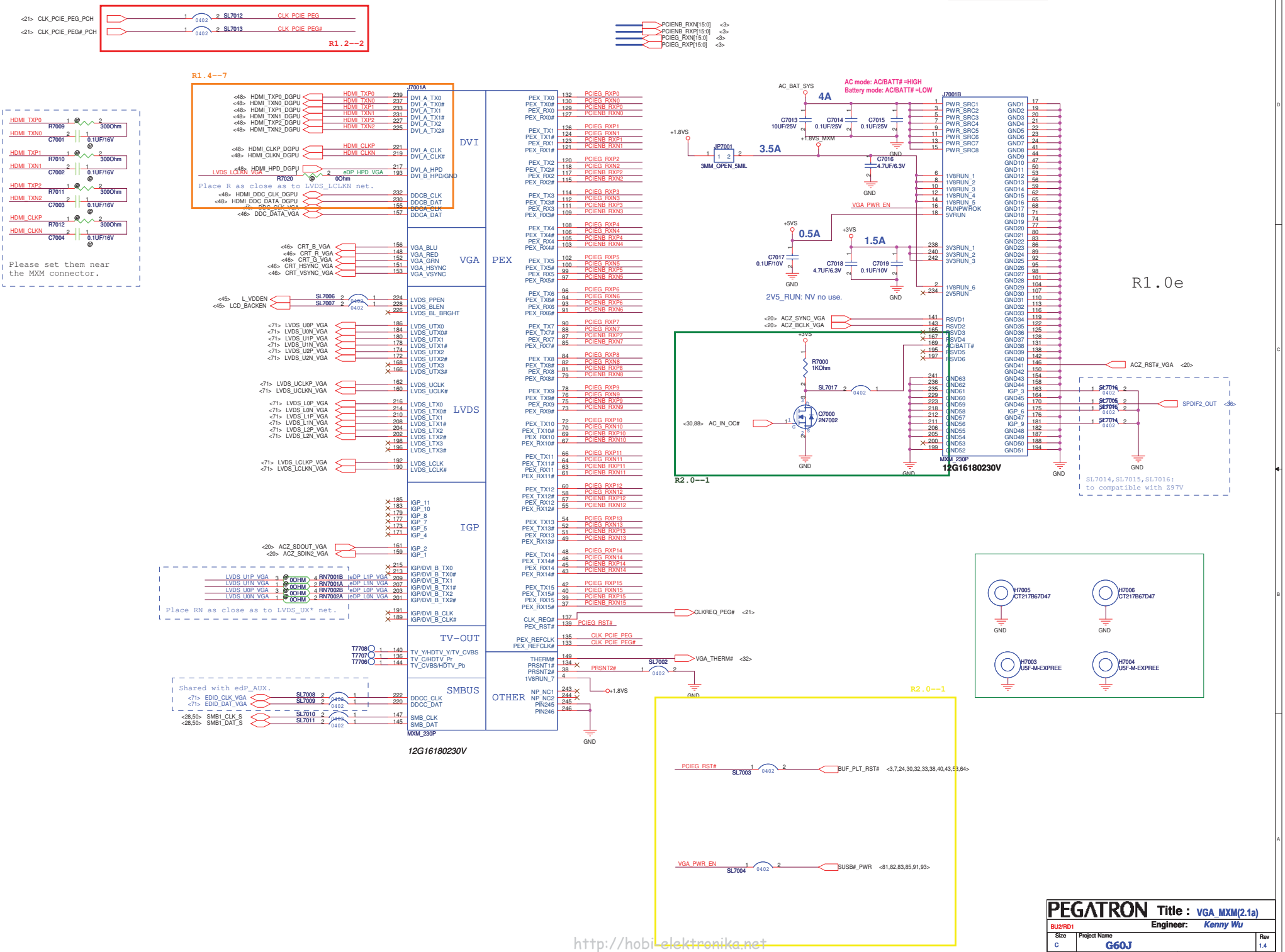
PEGATRON Title : OTH_GAME-LED

BU2/RD1 Engineer: Kenny Wu

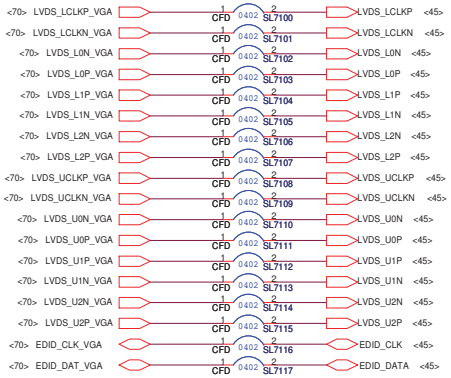
Size	Project Name	Rev
C	G60J	1.4

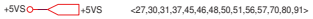
Date: Friday, July 31, 2009 Sheet 69 of 99

Main Board



PEGATRON	Title : VGA_MXM(2.1a)
BU2/RD1	Engineer: Kenny Wu
Size: C	Project Name: G60J
Rev: 1.4	
Date: Friday, July 31, 2009	Sheet 70 of 99





http://hobi-elektronika.net

PEGATRON Title : VGA(2)_LVDS Switch

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
C	G60J	1.4

Date: Friday, July 31, 2009 Sheet 71 of 99

PEGATRON Title : VGA(3)_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
Custom	G60J	1.4

Date: Friday, July 31, 2009 Sheet 72 of 99

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PEGATRON Title : VGA(4)_****

BU2/RD1 Engineer: Kenny Wu

Size	Project Name	Rev
Custom	G60J	1.4

Date: Friday, July 31, 2009 Sheet 73 of 99

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PEGATRON	Title : VGA(5)_****				
BU2/RD1	Engineer: Kenny Wu				
Size: Custom	Project Name: G60J				Rev: 1.4
Date: Friday, July 31, 2009	Sheet 74 of 99				

http://hobi-elektronika.net

PEGATRON	Title : VGA(6)_****			
BU2/RD1	Engineer: Kenny Wu			
Size: Custom	Project Name: G60J			Rev: 1.4
Date: Friday, July 31, 2009		Sheet 75 of 99		

http://hobi-elektronika.net

PEGATRON	Title : VGA(7)_****			
BU2/RD1	Engineer: Kenny Wu			
Size: Custom	Project Name: G60J			Rev: 1.4
Date: Friday, July 31, 2009	Sheet 76 of 99			

http://hobi-elektronika.net

PEGATRON	Title : VGA(8)_****				
BU2/RD1	Engineer: Kenny Wu				
Size: Custom	Project Name: G60J				Rev: 1.4
Date: Friday, July 31, 2009	Sheet 77 of 99				

http://hobi-elektronika.net

PEGATRON Title : VGA(9)_****

BU2/RD1 Engineer: Kenny Wu

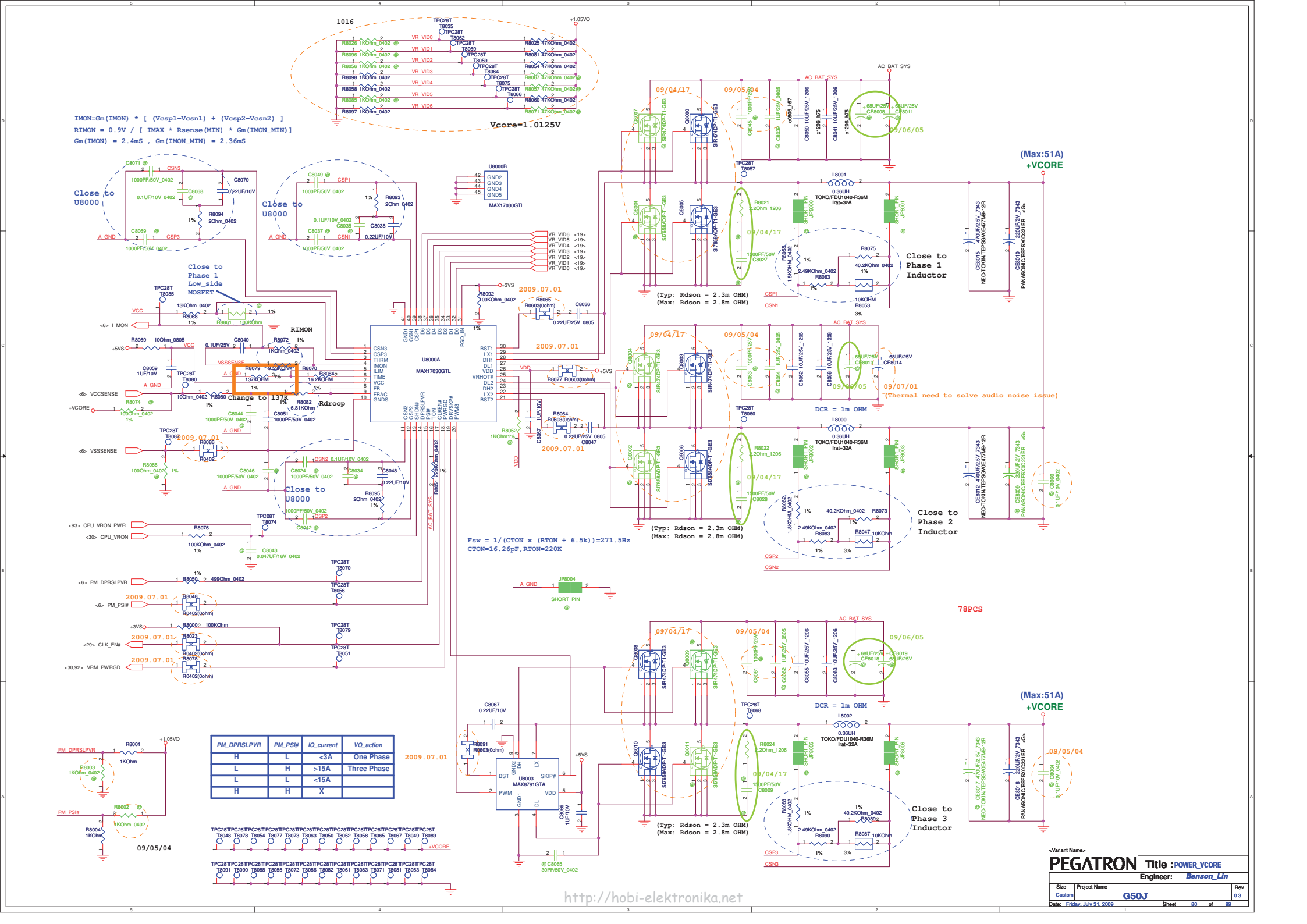
Size	Project Name	Rev
Custom	G60J	1.4

Date: Friday, July 31, 2009 Sheet 78 of 99

http://hobi-elektronika.net

PEGATRON	Title : VGA(10)_****			
BU2/RD1	Engineer: Kenny Wu			
Size: Custom	Project Name: G60J			Rev: 1.4
Date: Friday, July 31, 2009	Sheet 79 of 99			

http://hobi-elektronika.net



PM_DPRSLPVR	PM_PSI#	IO_current	VO_action
H	L	<3A	One Phase
L	H	>15A	Three Phase
L	L	<15A	
H	H	X	

SKIP:
GND : DEM operation;
REF : Ultrasonic Mode operation;
VCC : PWM operation.

TON:(5V/3.3V)
VCC:(200kHz/250kHz)
REF:(300kHz/375kHz)
GND:(400kHz/500kHz)

VENLDO:
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V

AC_BAT_SYS

AC:LIR=0.47;Iripple=2.61A;Ipk=6.8A
DC:LIR=0.29;Iripple=1.58A;Ipk=6.29A

VOUT:Typ.=5.09V;Max.=5.217V;Min.=4.966V;T=2.5%

OCP>7.15A

+5VO
(Max:5.5A)

+5VSUS
(0.01A)

DCR:Typ=13.2mOhm;Max=15mOhm

Isat=13A

(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)

FB1=2V(T=1.25%)

(5V:300kHz)

(3.3V:375kHz)

+5VA
(0.12A)

AC:LIR=0.33;Iripple=3.31A;Ipk=11.6A
DC:LIR=0.25;Iripple=2.53A;Ipk=11.22A

VOUT:Typ.=3.32V;Max.=3.388V;Min.=3.253V;T=2.05%

OCP>12.2A=>OCP setting 8.2A

+3VO
(Max:9.95A)

DCR:Typ=5.8mOhm;Max=7mOhm

Isat=16A

(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)

FB1=2V(T=1.25%)

53PCS

+3VSUS

JP8107 close to Q8104

+3VSUS (Max:0.919A)

2009/01/10
Check have or not

+12VSUS

(Max:0.02A)

VOUT:Typ.=12.256V;Max.=12.962V;Min.=11.571V;T=5.76%

TOTAL COUNT : 38 PCS

<Variant Name>

PEGATRON Title :POWER_SYSTEM
Engineer: Benson_Lin
Size: Custom | Project Name: G50J | Rev: 0.1
Date: Friday, July 31, 2009 | Sheet 81 of 94

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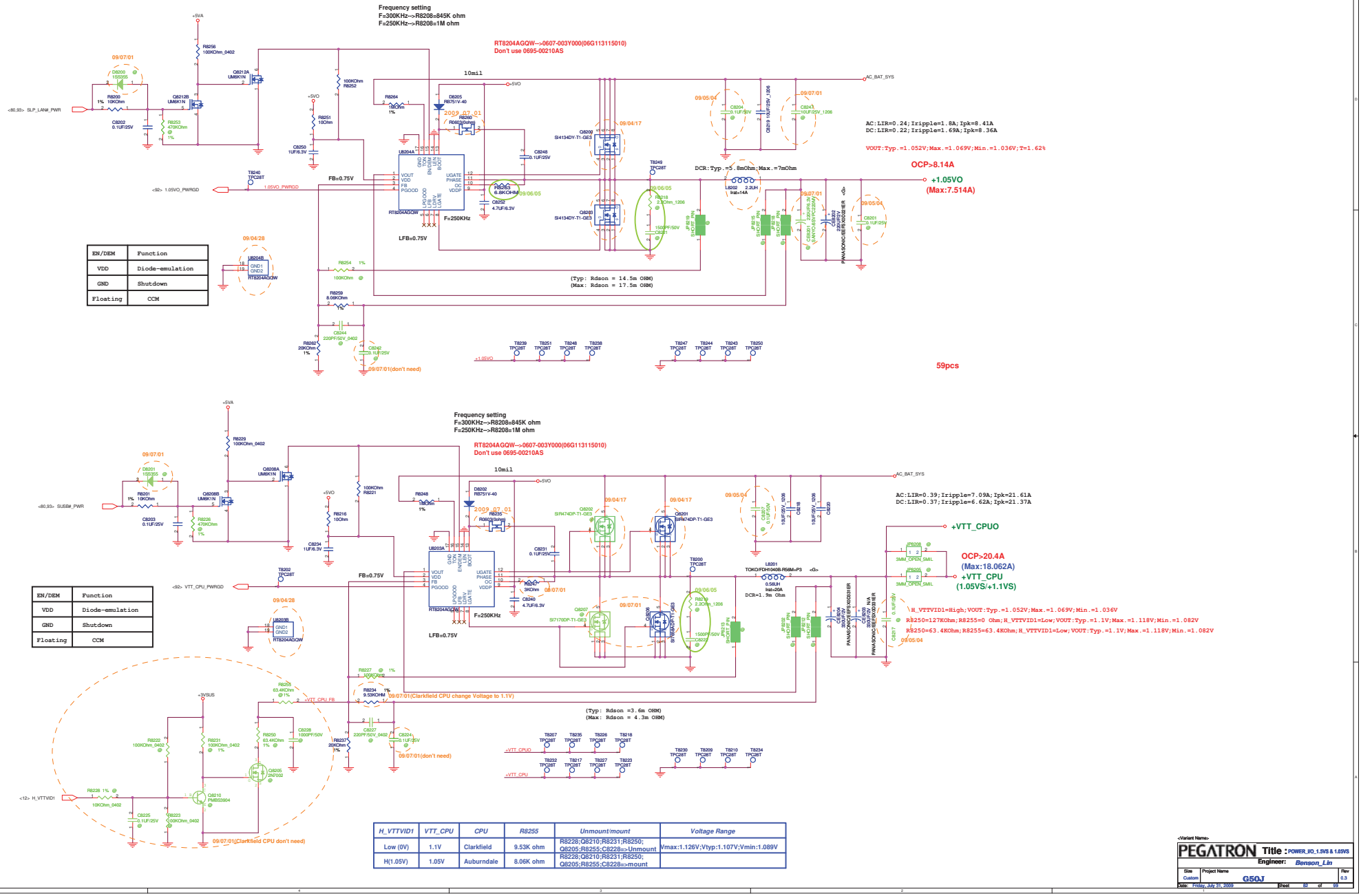
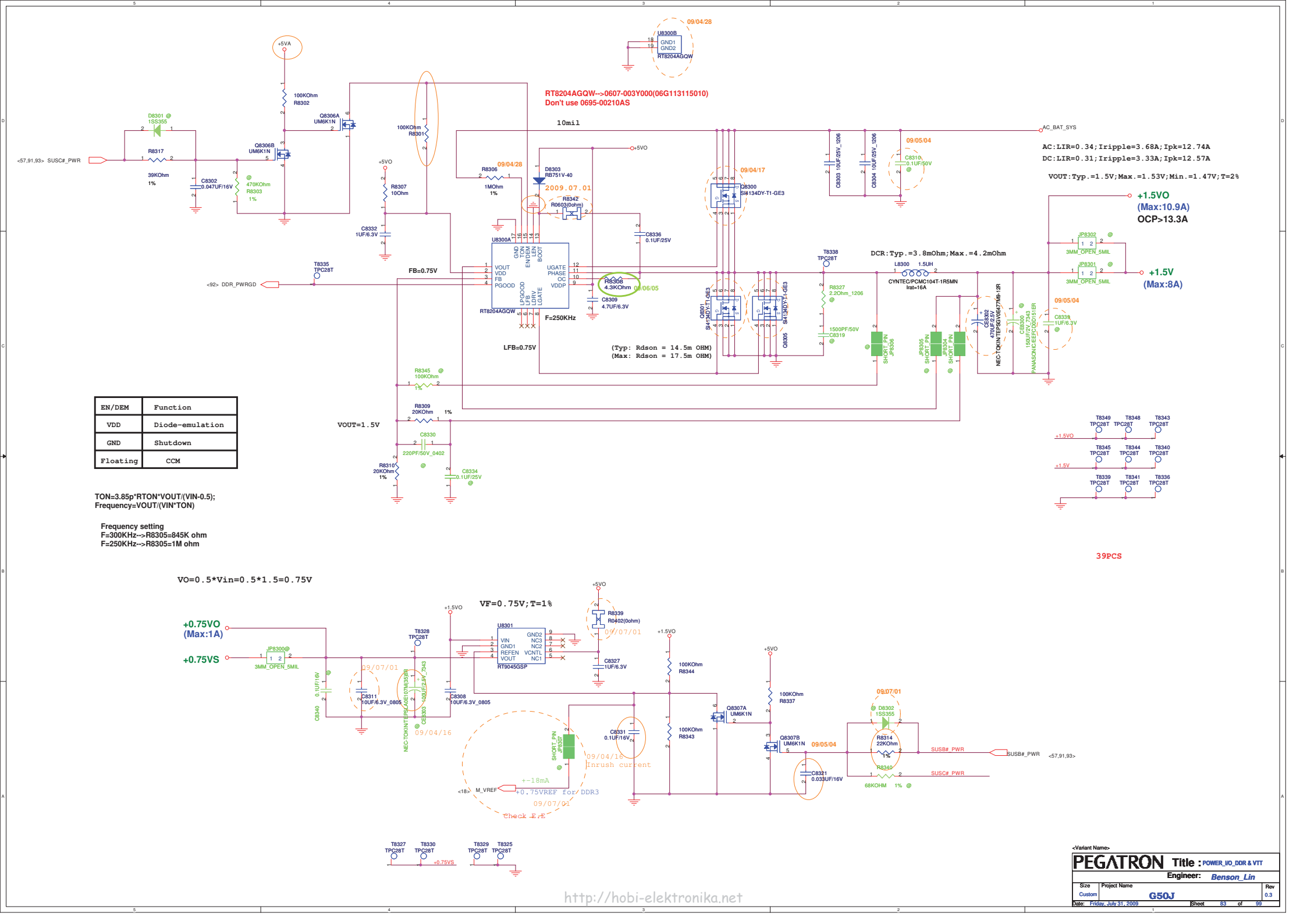


http://hobi-elektronika.net



EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM

TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8305=845K ohm
F=250KHz-->R8305=1M ohm

39PCS

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<Variant Name>

PEGATRON Title : POWER_I/O_DDR & VTT

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	G50J	0.3

Date: Friday, July 31, 2009 Sheet 83 of 99

<Variant Name>

PEGATRON Title : POWER_N/A

Engineer: *Benson_Lin*

Size	Project Name	Rev
A	G50J	0.3

Date: Friday, July 31, 2009 Sheet 84 of 99

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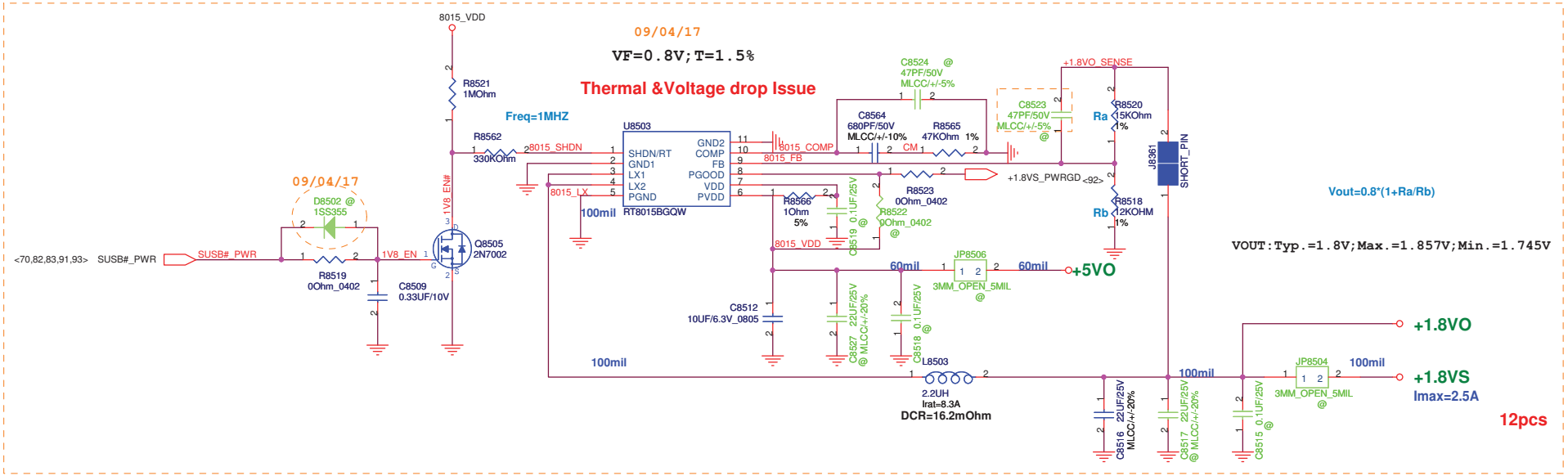
@---R1.3(ASUS P.M Change K/P,E.E Change power budget)



RT8015B=>R8523mount;R8522unmount;
RT8015A=>R8522mount;R8523unmount

<Variant Name>

PEGATRON Title : POWER_+1.8VS

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	G50J	0.3

Date: Friday, July 31, 2009 Sheet 85 of 99

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44pcs

G60J CPU use Clarkfiel,so don't need VGA power

<Variant Name>

PEGATRON Title :POWER_+VGFX_CORE

Engineer: Benson Lin

Size	Project Name	Rev
Custom	G50J	0.3

Date: Friday, July 31, 2009 Sheet 86 of 99

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<Variant Name>

PEGATRON Title : POWER_N/A

Engineer: Jeff_Du

Size	Project Name	Rev
A	G50J	0.3

Date: Friday, July 31, 2009 Sheet 87 of 99

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Adaptor =120W, 19V/6.32A

16.857V < ACIN <18.014V

120W/90W:R8801=15m OHM(11G21DR01515110)

65W:R8801=20m OHM(10G21DR02015110)

09/07/01(change 1206 size for cost down)

09/07/03(for EMI)

AC_BAT_SYS

BAT_CON

AC_BAT_SYS_INV

AC_BAT_SYS to Inverter connect,
Power trace =60mil(min), Put JP8804 close to Q8800

120W: R8807 = 1.82K
90W: R8807 = 6.98K
65W: R8807 = 17.8K

09.01.13

09/07/01(for EMI)

09/07/01

09/07/01(change 1206 size for cost down)

12.641V(min) < VBAT-12.515(Typ) < 12.768V(Max)

BAT

2P/3P, 2400mAh

Close to Q8805

09/07/28 PR

0113

1024

1027

ISET_EC	ISET(Voltage)	CHG_CURRENT	
0.1294V	0.055V	0.157A	PRECHG
2.0188V	0.865V	2.472A(0.52C)	Quick CHG

Ichg=(240m/RS2)*(VISET/VAA)
Ichg=(240m/20m)*(0.055/4.2)=0.157A
Ichg=(240m/20m)*(0.865/4.2)=2.4714A

VCTL connect to GND,VFB=2.1V
VBAT=2.1*(R8819+R8828)/R8828

VSET_EC	BAT	
1.4106V	12.545V	ON
3.2871V	5.519V	OFF

12.641V(min)<VBAT-12.515(Typ)<12.768V(Max)

MAX17015 VBAT setting:
VCTL connect to GND,VFB=2.1V
VBAT=2.1*(R8819+R8828)/R8828
Fix R8828 to 10K, adjust R8819
R8819=30K,VBAT=8.4V(2cell)
R8819=49.9K,VBAT=12.579V(3cell)
R8819=69.8K,VBAT=16.758V(4cell)

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<Variant Name>

PEGATRON Title :CHARGER_201

Engineer: Benson_Lin

Size	Project Name	Rev
C	G50J	0.3

Date: Friday, July 31, 2009 Sheet 88 of 99

<Variant Name>

PEGATRON Title : POWER_N/A

Engineer: *Jeff_Du*

Size	Project Name	Rev
A	G50J	0.3

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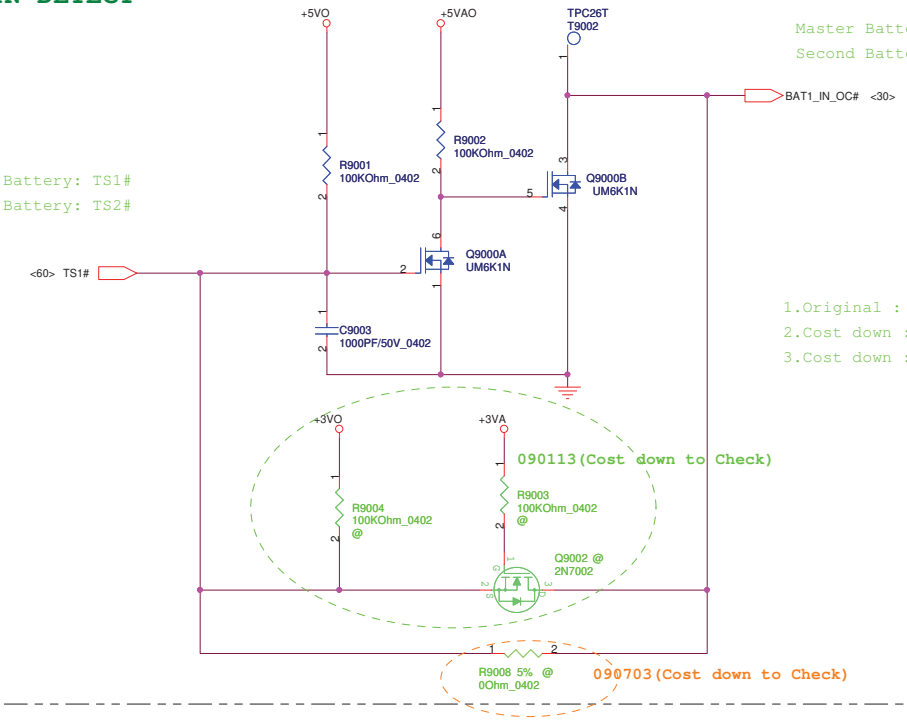
BATTERY IN DETECT



Master Battery: TS1#
Second Battery: TS2#

Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

ADAPTER IN DETECT

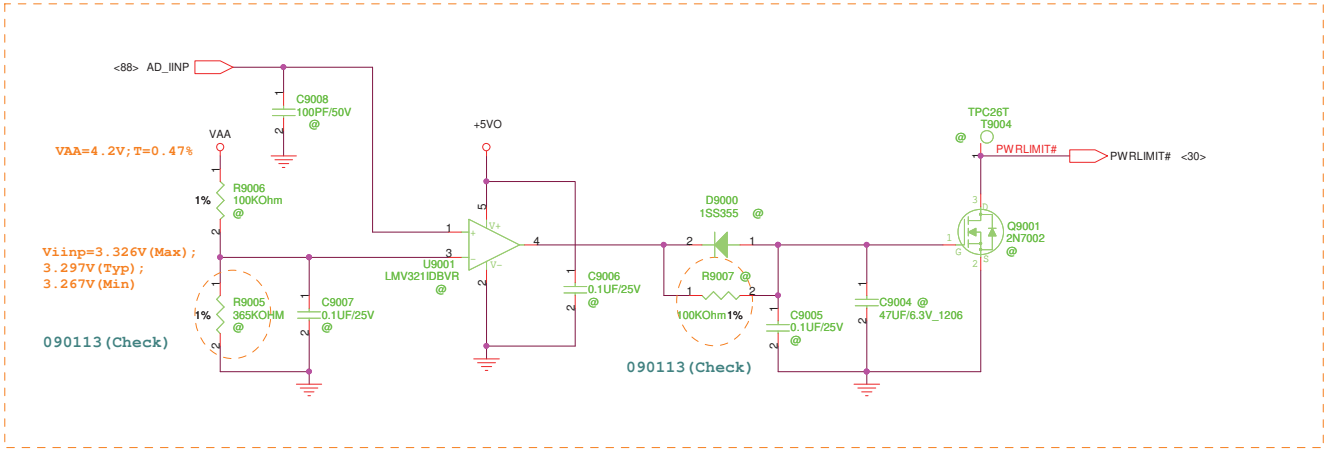
Use MAX17015 IC function to Cost down component

1.Original : mount R9001.R9002.C9003.Q9000A.Q9000B
2.Cost down : mount R9004.R9003.Q9002.C9003
3.Cost down : mount R9008.C9003

POWER LIMIT CIRCUIT

@---09.07.01(Cost Down)

+2.5Vref delete



Pinput=111.8625W----->Iinput=5.8875A
RS1=20mohm,Glinp=2.8uA/mV,Riinp=10K
Iinput=Viinp/(RS1*Giinp*Riinp)=Viinp/(20m*2.8uA/mV*10K)=5.8875A----->Viinp=3.297V

4pcs

<Variant Name>

PEGATRON Title : POWER_DETECT
Engineer: Benson_Lin

Size	Project Name	Rev
Custom	G50J	0.3

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SUSB#_PWR POWER

Thermal &Voltage drop Issue

2009/06/05 Q9108 SI4134DY-T1-GE3 — +3VO → R9108 47KOHM, C9104 0.1UF/25V, C9102 0.1UF/25V @ → TPC26T T9109, TPC26T T9114 → +1.8VS=1.395A (Max:6.825A) +3VS

2009/06/05 Q9106 SI4134DY-T1-GE3 — +5VO → R9107 47KOHM, C9109 0.033UF/16V, C9107 0.1UF/25V @ → TPC26T T9101, TPC26T T9127 → (Max:3.28A) +5VS

2009/06/05 Q9109 SI4134DY-T1-GE3 — +1.5VO → R9117 47KOHM, C9111 0.033UF/16V, C9108 0.1UF/25V @ → TPC26T T9103, TPC26T T9128 → (Max:2.9A) +1.5VS

Thermal &Voltage drop Issue

2009/06/05 Q9110 SI4134DY-T1-GE3 — +1.05VO → R9118 47KOHM, C9112 0.033UF/16V, C9114 0.1UF/25V @ → TPC26T T9104, TPC26T T9130 → +1.05VS=+VTT_PCH (Max:5.172A) +1.05VS

UMC4N Q9105 — +12VSUS → TPC26T T9129 SUSB#_PWR; R9102 100KOhm 1% → TPC26T T9102 → (Max:0.02A) +12VS

SUSC#_PWR POWER

2009/06/05 Q9115 SI4134DY-T1-GE3 — +3VO → R9109 22KOhm, C9110 0.033UF/16V → TPC26T T9126, TPC26T T9108 → (Max:1.25A) +3V; C9106 0.1UF/25V @

2009/06/05 Q9101 SI4134DY-T1-GE3 — +5VO → R9110 22KOhm, C9105 0.033UF/16V → TPC26T T9124, TPC26T T9113 → (Max:2.21A) +5V; C9113 0.1UF/25V @

UMC4N Q9107 — +12VSUS → TPC26T T9119 SUSC#_PWR; R9103 100KOhm 1% → TPC26T T9112 → +12V

IAMT POWER @Cost down---PR Unmount(combine with SUSB#_PWR)

2009/06/05 Q9116 @ SI4134DY-T1-GE3 — +3VO → R9124 @ 10mOhm_1508 1%, R9125 22KOhm @, C9117 0.033UF/16V @ → TPC26T T9132@, TPC26T T9110@ → (Max:1.3A) +3VM 09.04.09; C9115 0.1UF/25V @

2009/06/05 Q9102 @ SI4134DY-T1-GE3 — +1.05VO → R9123 @ 10mOhm_1508 1%, R9120 22KOhm @, C9118 0.033UF/16V @ → TPC26T T9125@, TPC26T T9115@ → (Max:2.342A) +1.05VM 09.04.09; C9116 0.1UF/25V @

UMC4N @ Q9111 — +12VSUS → TPC26T T9116@ → +12VM; No circuit connect to E.E circuit

SLP_LAN#_PWR → R9130 0Ohm @ → TPC26T T9120@

SLP_M#_PWR → R9129 0Ohm @

R9134 100KOhm @; R9122 100KOhm 1% @

+5VSUS → R9133 @ 100KOhm → Q9112B UM6K1N @; Q9112A UM6K1N @

2009/01/10(unmount)

2009/01/10(add)

2009/07/01_For power +3VA test; If short +3VA JP point to check power; should be cut off this temp line.

2009/07/01 R9105 R0603(1KOhm): TPC26T T9131 / TPC26T T9135 — <30,36,43,57,92> SUSB_EC# / <70,82,83,85,93> SUSB#_PWR

2009/07/01 R9104 R0603(1KOhm): TPC26T T9121 / TPC26T T9134 — <30,57> SUSC_EC# / <83,93> SUSC#_PWR

2009/07/01 R9106 R0603(1KOhm): TPC26T T9139 / TPC26T T9133 — NON_IAMT — <30,57> SUSB_EC# / <30,36,43,57,92> ME_PM_SLP_LAN#

R9126 @ 1KOhm IAMT: TPC26T T9133 / TPC26T T9137 — <30,36,43,57,92> ME_PM_SLP_LAN# / <70,82,83,85,93> SLP_LAN#_PWR

2009/01/13_R9106(mount); R9126(unmount)for test

2009/07/01 R9127 R0603(1KOhm): TPC26T T9122 / TPC26T T9136 — <30,57> ME_SLP_M_EC# / <83,93> SLP_M#_PWR

2009/07/01 R9128 R0603(1KOhm): TPC26T T9123 / TPC26T T9138 — <30,57> GFX_VR_ON / <83,93> GFX_VRON_PWR

54pcs

<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	G50J	0.3

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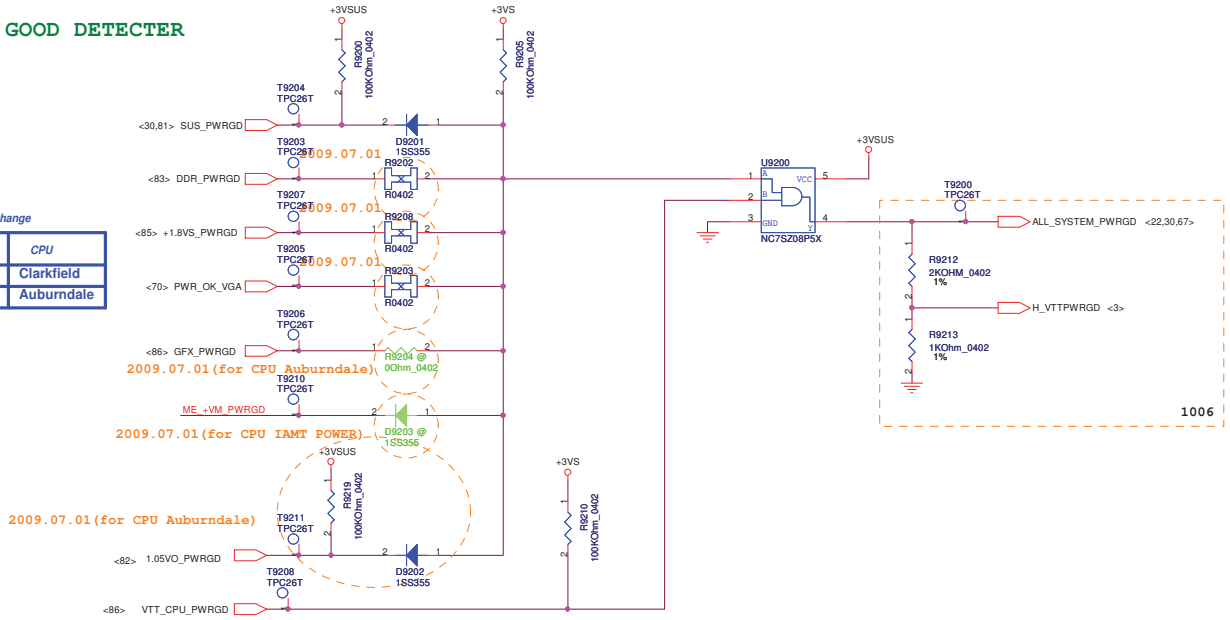
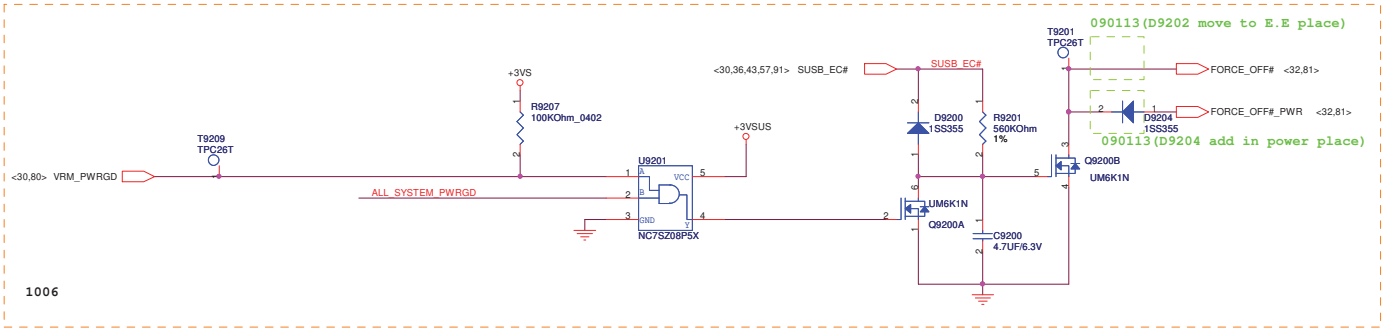
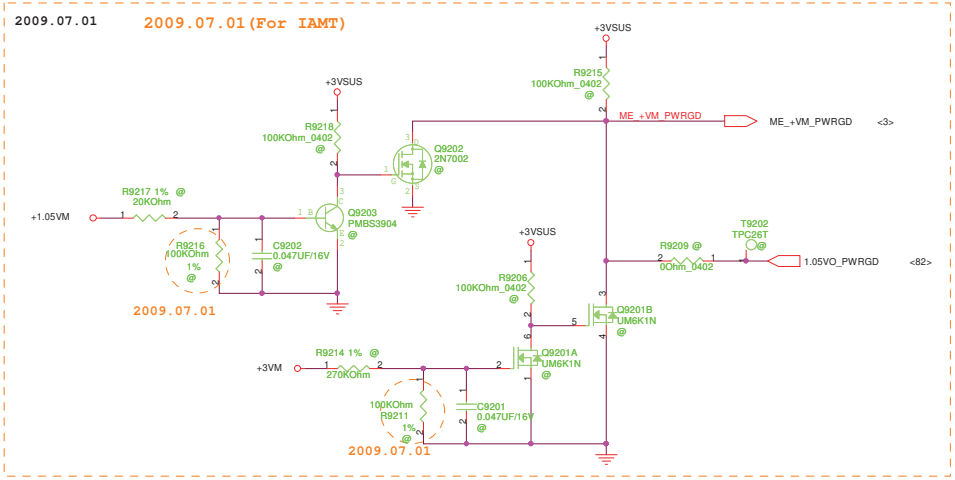
POWER GOOD DETECTER

BOM change

YES/NO	CPU
X	Clarkfield
R9204	Auburndale







42pcs

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<Variant Name>

PEGATRON Title :POWER_PROTECT

Engineer: Benson Lin

Size	Project Name	Rev
Custom	G50J	0.3

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AC_BAT_SYS → AC_BAT_SYS <70,80,81,82,83,86,88>

BAT → BAT <88>

BAT_CON → BAT_CON <60,88>

+3VA → +3VA <20,30,56,57,81>

+5VAO → +5VAO <81,85,90>

+5VA → +5VA <31,56,81>

+5VO → +5VO <81,82,83,90,91>

+3VO → +3VO <81,91>

+1.8VO → +1.8VO

+0.9VO → +0.9VO

+1.05VO → +1.05VO <80,82>

+1.5VO → +1.5VO <83,91>

+5VSUS → +5VSUS <27,56,81,86>

+3VSUS → +3VSUS <3,21,22,24,25,27,30,33,37,53,70,81,82,92>

+12VSUS → +12VSUS <28,70,81,91>

+5V → +5V <31,36,44,45,46,52,56,57,65,68,70,85,91>

+3V → +3V <24,31,43,45,57,61,64,68,69,91>

+12V → +12V <37,42,68,91>

+1.8V → +1.8V

+0.9V → +0.9V

+3VS → +3VS <16,17,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,36,37,40,41,42,43,44,45,46,47,48,50,51,53,56,57,64,65,66,67,70,80,85,91,92>

+5VS → +5VS <27,31,37,45,46,47,48,50,51,56,57,71,80,91>

+12VS → +12VS <28,45,70,91>

+1.5VS → +1.5VS <26,43,53,57,64,70,91>

+VCCP → +VCCP

+VCORE → +VCORE <6,57,80>

FOR POWER TEST

+3VA → JP9300 @ (1 2 2) SGL_JUMP → TPC26T T9301 → CPU_VRON_PWR <80>

+3VA → JP9301 @ (1 2 2) SGL_JUMP → TPC26T T9302 → SUSB#_PWR <70,82,83,85,91>

+3VA → JP9302 @ (1 2 2) SGL_JUMP → TPC26T T9303 → SUSC#_PWR <83,91>

+3VA → JP9303 @ (1 2 2) SGL_JUMP → TPC26T T9304 → VSUS_ON <30,81>

+3VA → JP9304 @ (1 2 2) SGL_JUMP → TPC26T T9305 → SLP_M#_PWR <30,81>

+3VA → JP9305 @ (1 2 2) SGL_JUMP → TPC26T T9306 → SLP_LAN#_PWR <30,81>

+3VA → JP9306 @ (1 2 2) SGL_JUMP → TPC26T T9307 → GFX_VRON_PWR <30,81>

<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	G50J	0.3

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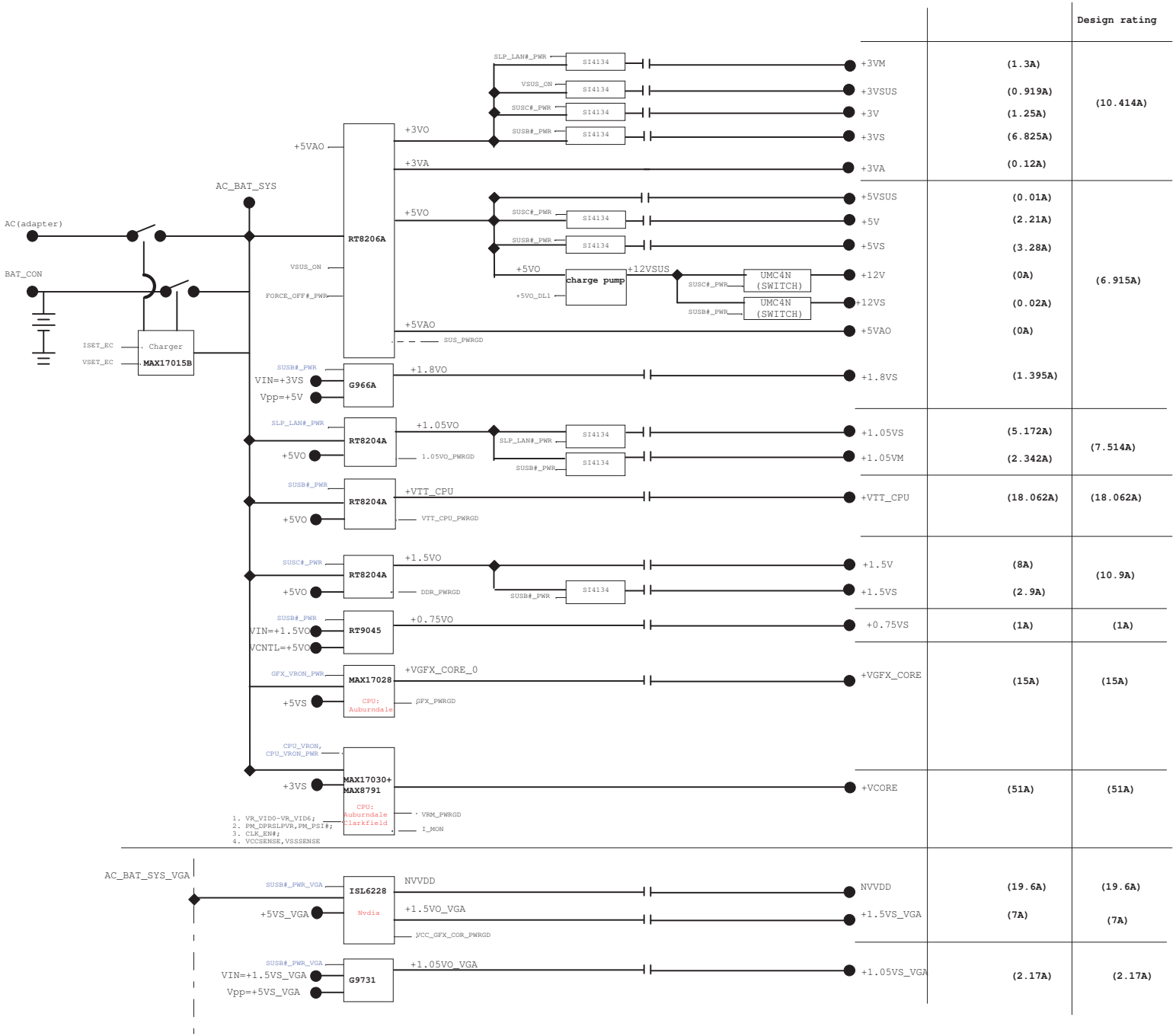

		Design rating
+3VM	(1.3A)	(10.414A)
+3VSUS	(0.919A)	
+3V	(1.25A)	
+3VS	(6.825A)	
+3VA	(0.12A)	
+5VSUS	(0.01A)	(6.915A)
+5V	(2.21A)	
+5VS	(3.28A)	
+12V	(0A)	
+12VS	(0.02A)	
+5VAO	(0A)	
+1.8VS	(1.395A)	
+1.05VS	(5.172A)	(7.514A)
+1.05VM	(2.342A)	
+VTT_CPU	(18.062A)	(18.062A)
+1.5V	(8A)	(10.9A)
+1.5VS	(2.9A)	
+0.75VS	(1A)	(1A)
+VGFX_CORE	(15A)	(15A)
+VCORE	(51A)	(51A)
NVVDD	(19.6A)	(19.6A)
+1.5VS_VGA	(7A)	(7A)
+1.05VS_VGA	(2.17A)	(2.17A)

<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: Benson_Lin

Size	Project Name	Rev
Custom	G50J	0.3

Date: Friday, July 31, 2009 Sheet 94 of 99

http://laptopschematics.net

JUMP must be shorted:

JP1601,JP1801,JP1802,JP2601,JP2602,JP2603,
JP2701,JP2702,JP2703,JP2704,JP8100,JP8101,
JP8102,JP8106,JP8205,JP8301,JP8504.

OPTIONAL selection:

@ -> no-stuff for all
CFD -> stuff for Clarkfield with MXM
CFD@ -> no-stuff for Clarkfield with MXM
AUB -> stuff for Auburndale with MXM (switchable GFX)
AUB@ -> no-stuff for Auburndale with MXM (switchable GFX)
IAMT -> stuff for IAMT sku
IAMT@ -> no-stuff for IAMT sku
NON_IAMT -> stuff for non-IAMT sku
NON_IAMT@ -> no stuff for non-IAMT sku
CPU_XDP -> stuff for CPU XDP using
CPU_XDP@ -> no-stuff for CPU XDP using
PCH_XDP -> stuff for PCH XDP using
PCH_XDP@ -> no-stuff for PCH XDP using

R1.1--> R1.2 Changed List:

1.Refer to #413686.
2.For the buffered mode is stable.
3.For Deleting PCH XDP, modify P20,P67.
4.For MXM 2.1a, modify P21, P70.
5.For PCIE CB,modify P40, P24.
6.Refer to DG R1.0.
7.Del the tested 0ohm.
8.For LVDS display on AUB.
9.Change DP port from B to D by Intel recommendation.
10.For reassigning USB Port, modify P24.
11.Repair R1.1 bug.
12.For Lighting Keyboard.
13.For Non-IAMT.
14.Remove PCIE<-->SATA Circuit(P66) for PCH SATA stable.
15.For Project SPEC, Del P68.
16.Add Second Source.

R1.3--> R1.4 Changed List:

1.Intel recommended.
2.For G60J SPEC.
3.Change CK505 from ICS3362 to ICS3197.
4.For PCH GPIO Definition.
5.R1.3 bug fixed.
6.GLAN from RTL8111C to AR8131
7.Add HDMI Switch(PI3HDMI201).
8.NV recommonded.

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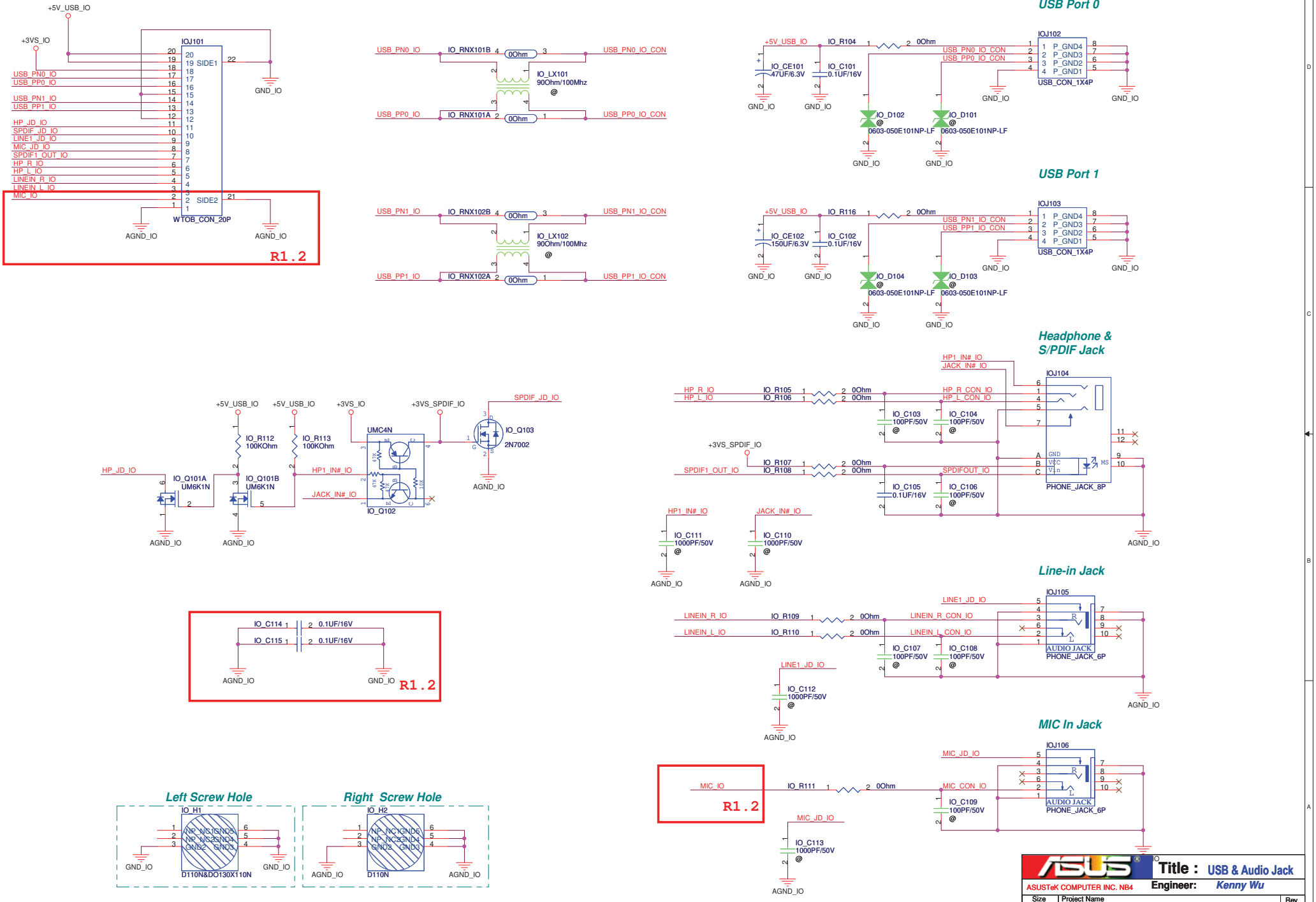
PEGATRON Title : System History
BU2/RD1 Engineer: Gary Tsai
Size C | Project Name G60J | Rev 1.1
Date: Friday, July 31, 2009 Sheet 95 of 99

I/O Board



http://hobi-elektronika.net

ASUSTeK COMPUTER INC. NB4	Title : USB & Audio Jack	
	Engineer: Kenny Wu	
Size: Custom	Project Name: G60J	Rev: 1.1
Date: Friday, July 31, 2009	Sheet 96 of 99	

PEGATRON	Title : ****			
BU2/RD1	Engineer: *Gary Tsai*			
Size: Custom	Project Name: G60J			Rev: 1.1
Date: Friday, July 31, 2009	Sheet 97 of 99			

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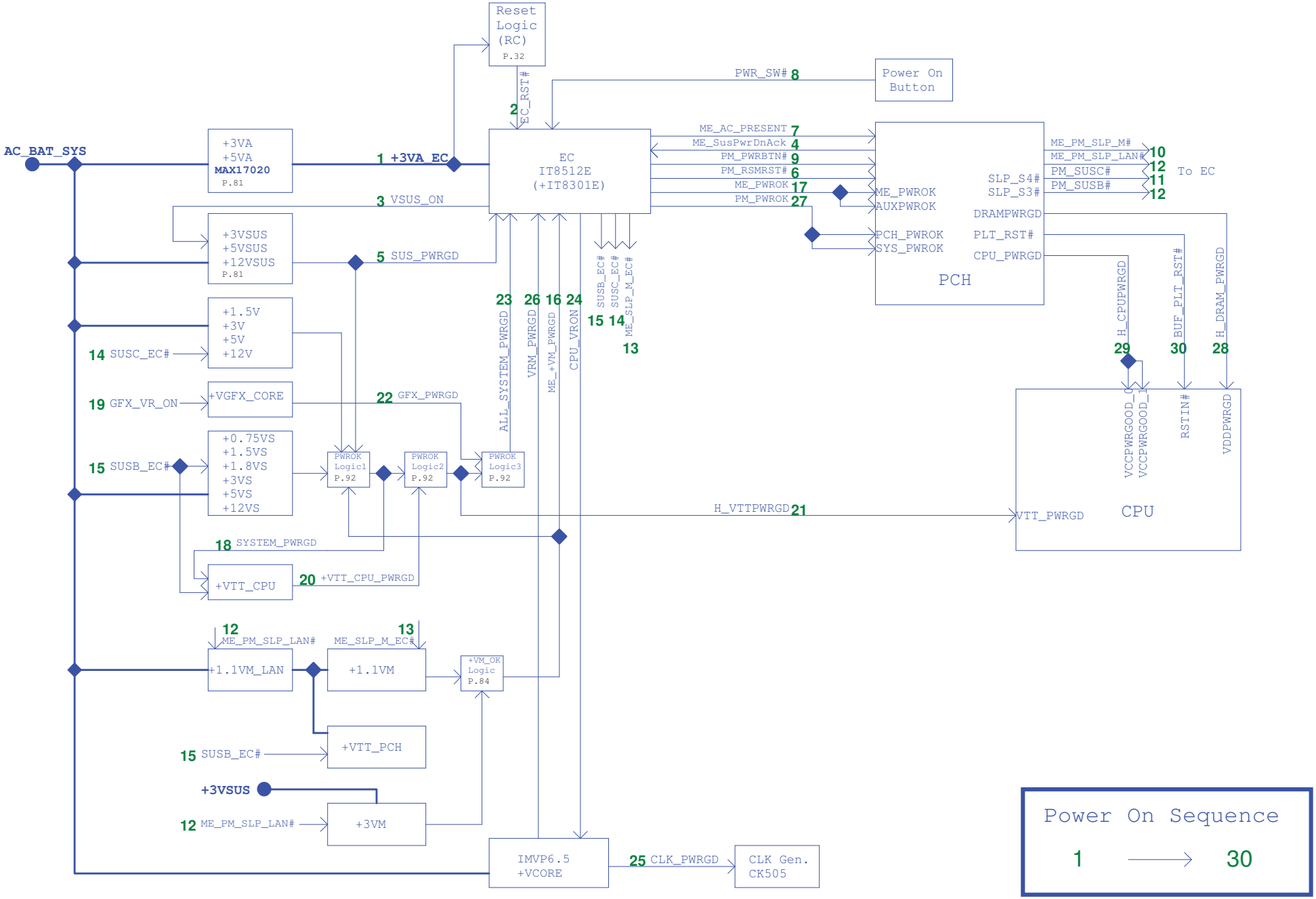
Power On Sequence Diagram Rev. 0.2



Power On Sequence

1 → 30

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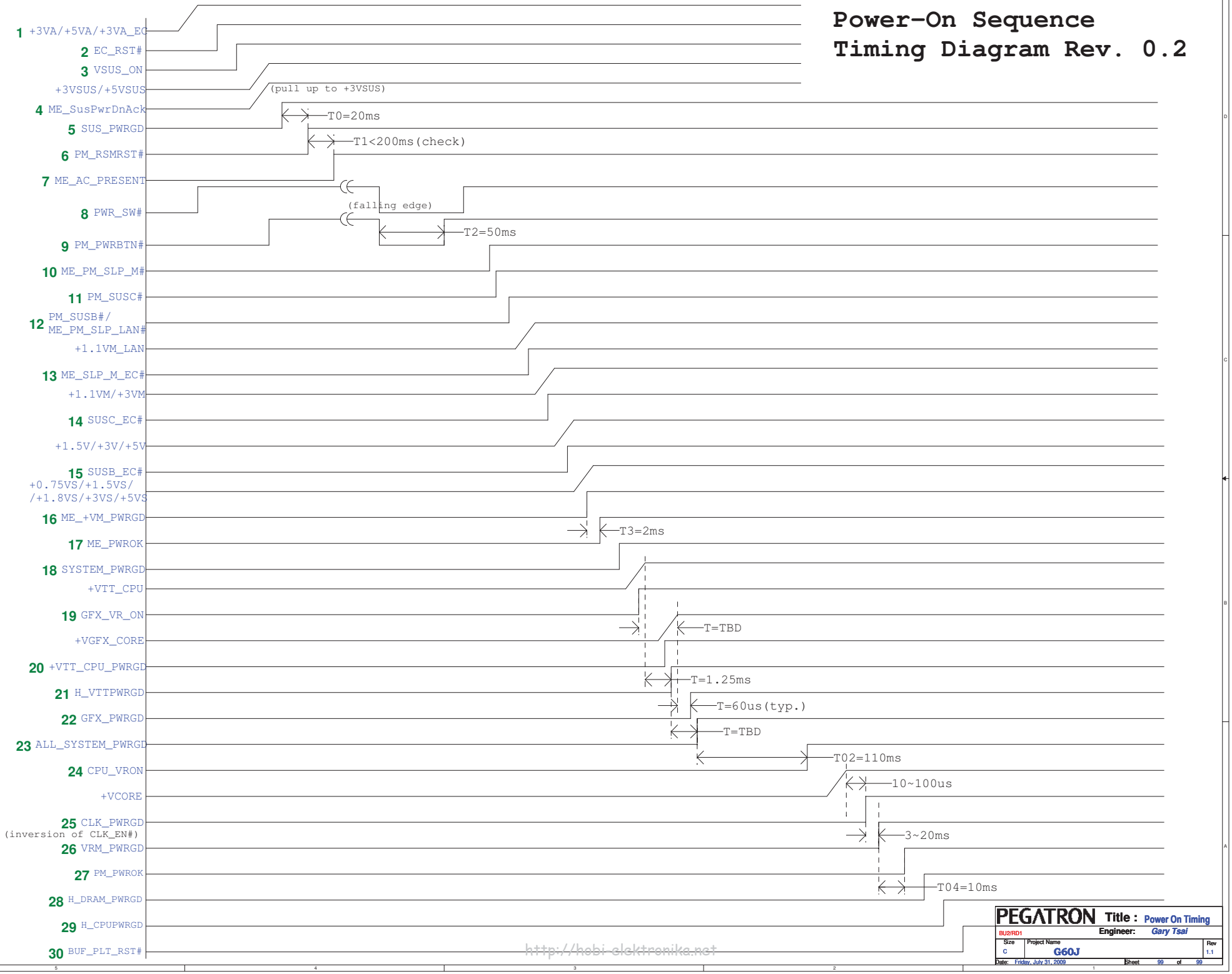
PEGATRON Title : Power On Sequence
BU2/RD1 Engineer: Gary Tsai
Size C | Project Name G60J | Rev 1.1
Date: Friday, July 31, 2009 | Sheet 98 of 99

Power-On Sequence Timing Diagram Rev. 0.2



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PEGATRON Title : Power On Timing
BU2/RD1 Engineer: Gary Tsai
Size C | Project Name G60J | Rev 1.1
Date: Friday, July 31, 2009 | Sheet 99 of 99