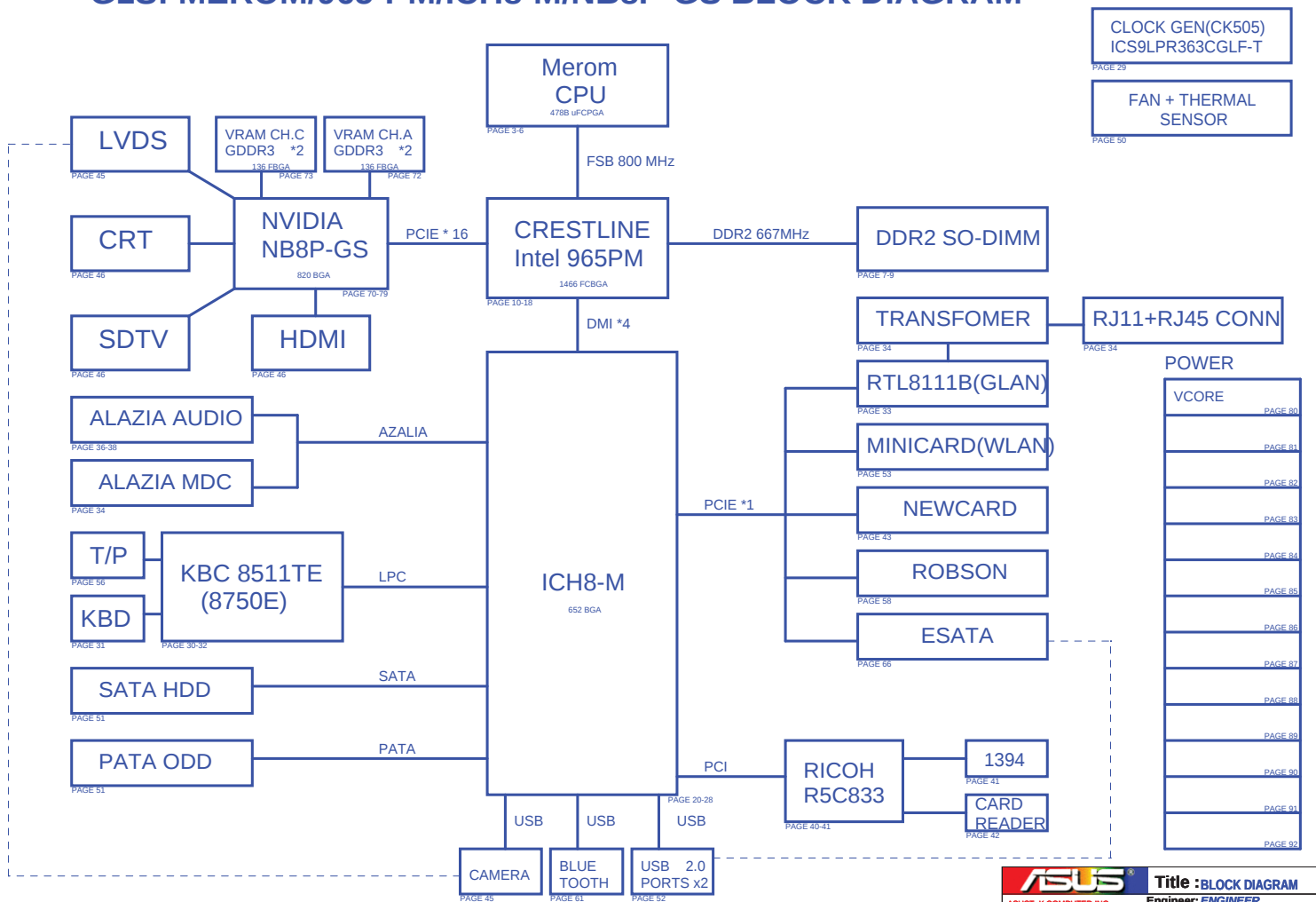
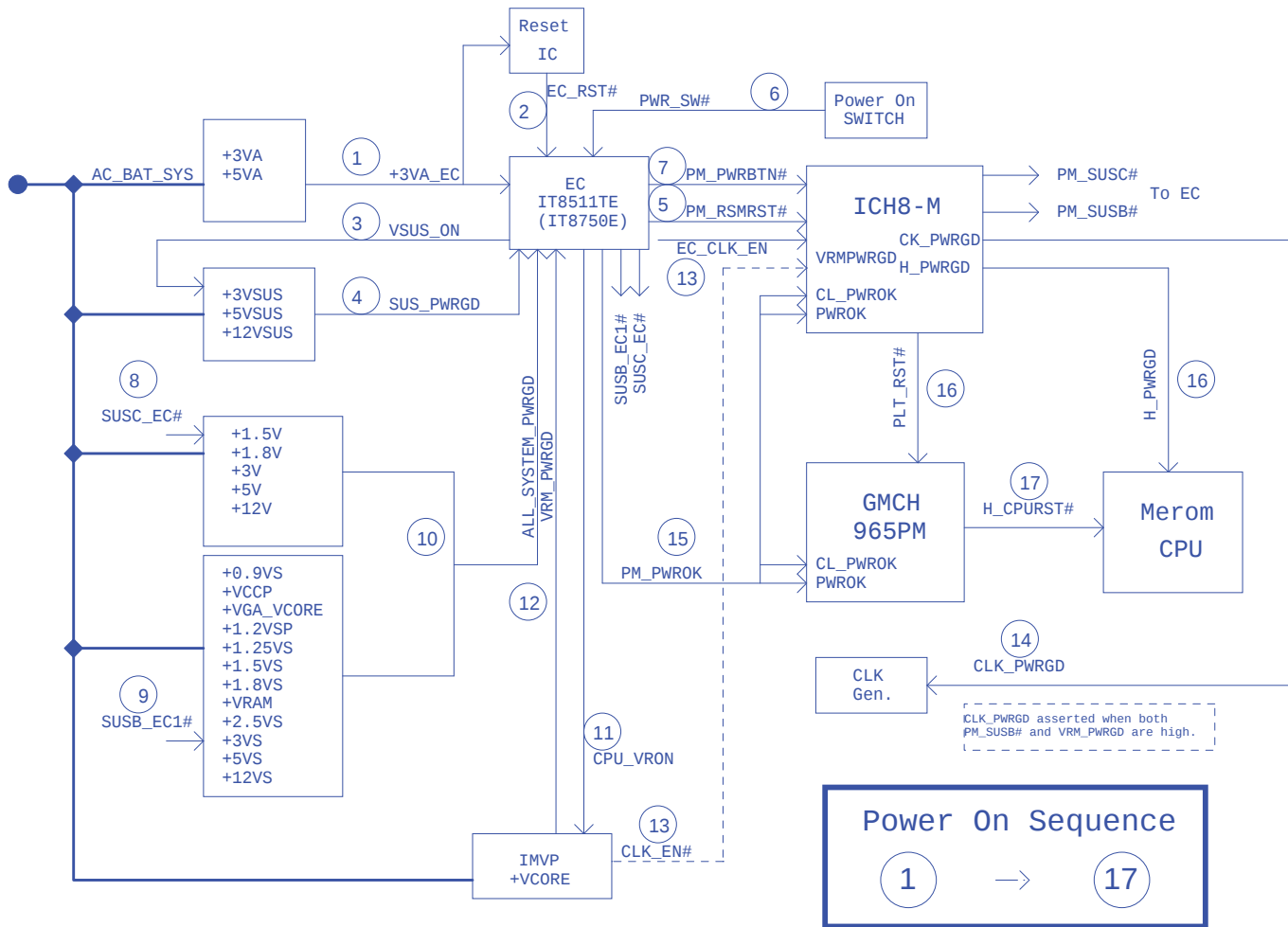
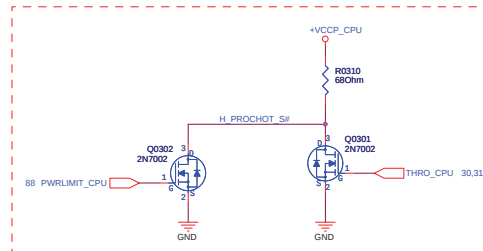
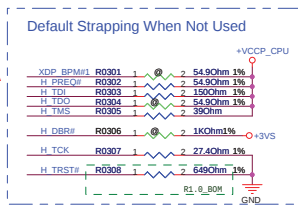
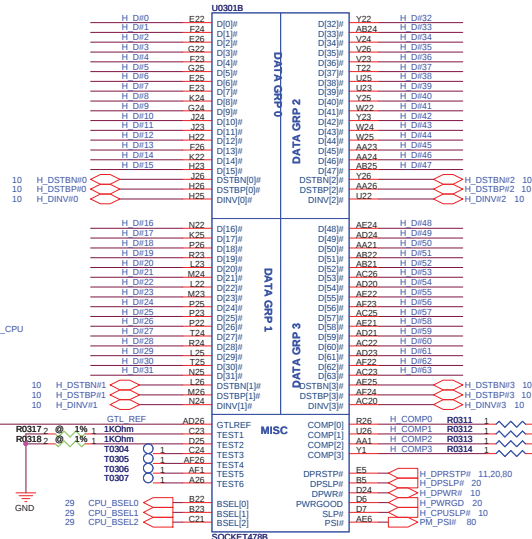
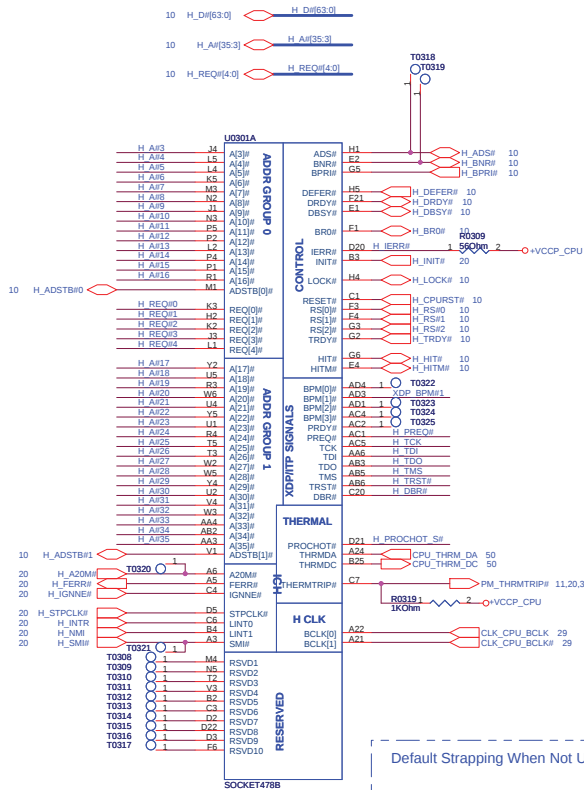
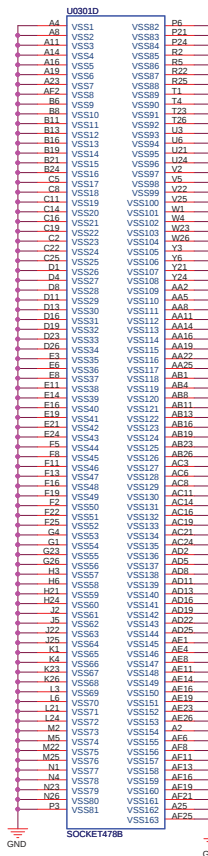


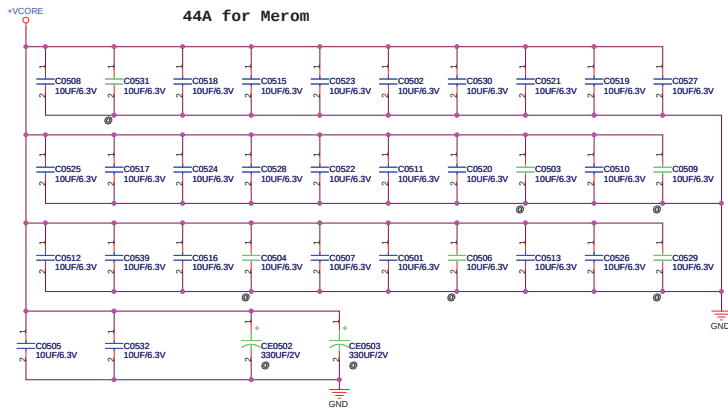
G1S: MEROM/965-PM/ICH8-M/NB8P-GS BLOCK DIAGRAM



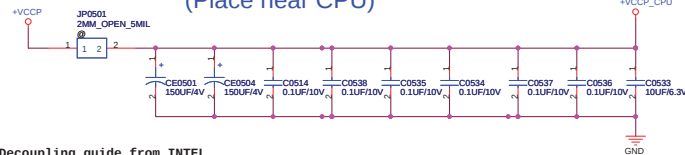






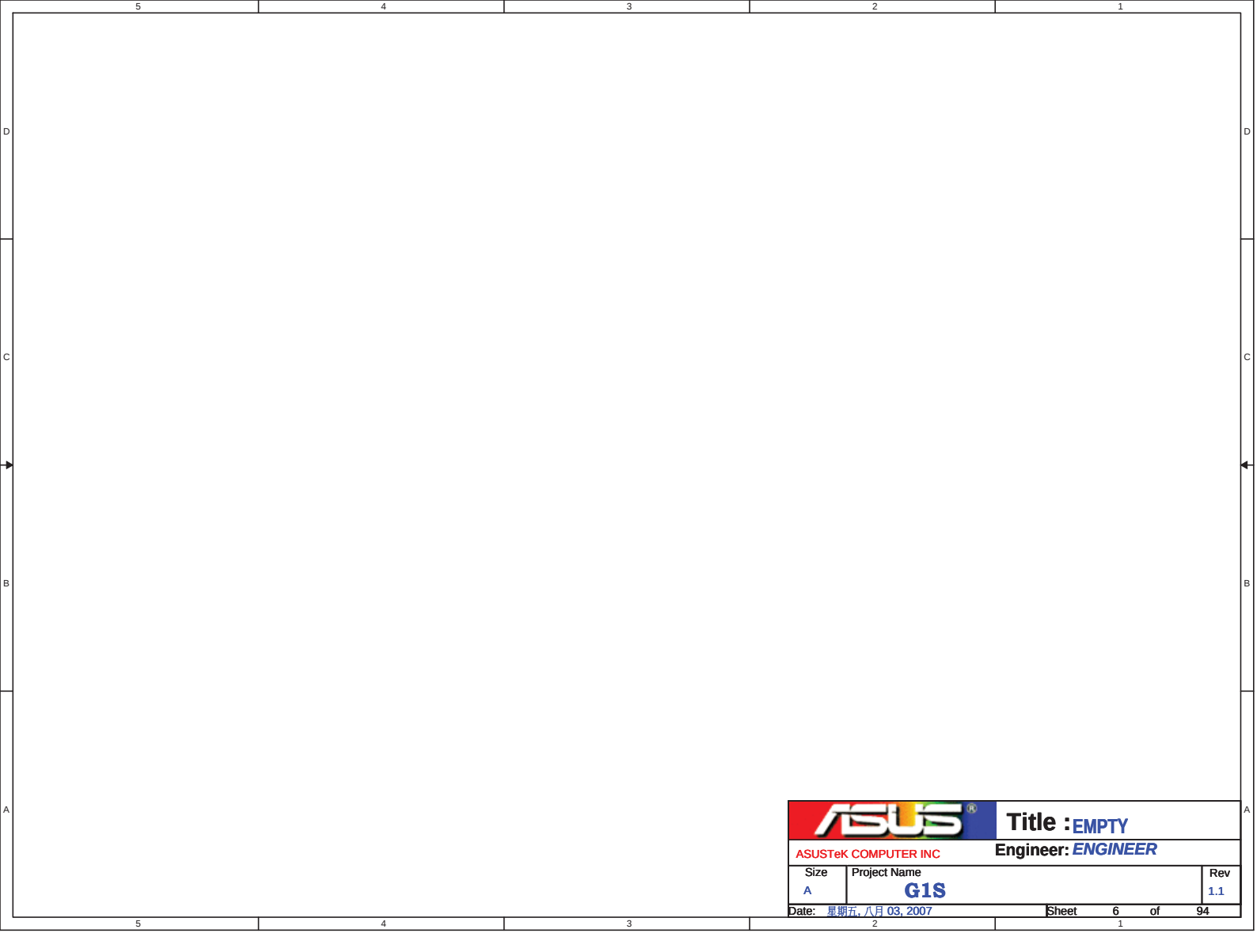


+VCCP Decoupling Capacitor (Place near CPU)

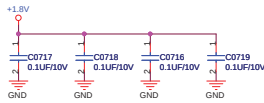


Decoupling guide from INTEL

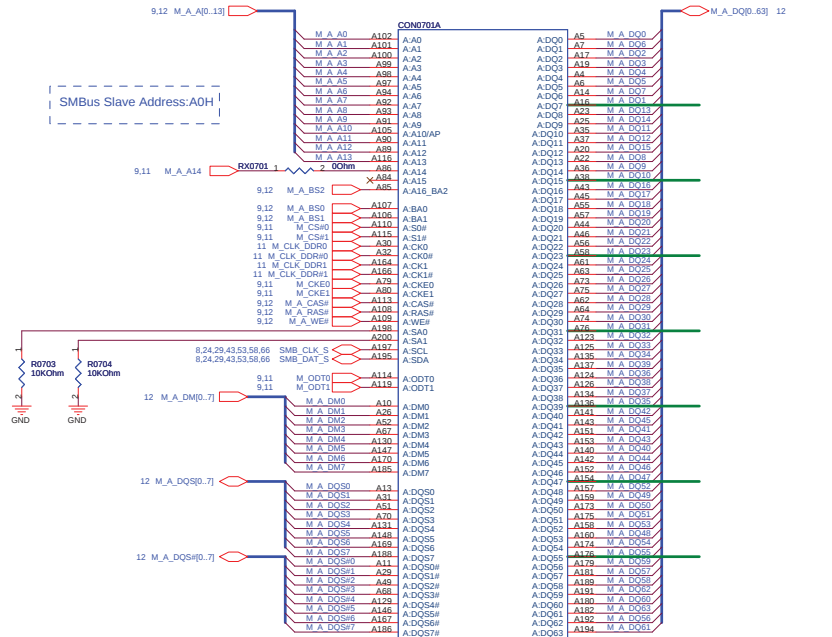
VCORE 22uF/10V	* 32pcs
330uF/2V	* 6pcs
VCCP 0.1uF	* 6pcs for CPU
150uF	* 1pcs for CPU



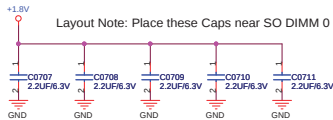
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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	6 of 94



Address reference +1.8V, add four 0.1uF decoupling CAP.

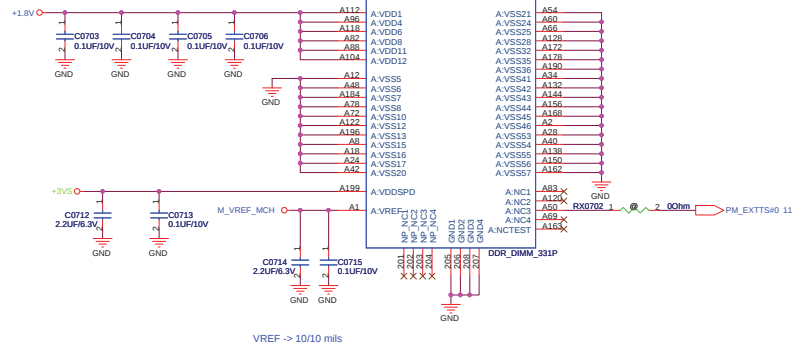


Layout Note: Place these Caps near SO DIMM 0



Layout Note: Place these Caps near SO DIMM 0

SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

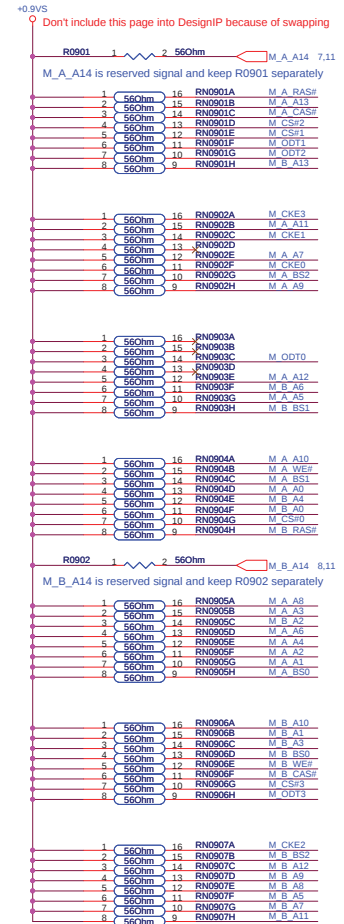
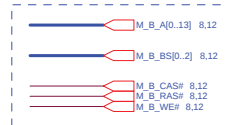
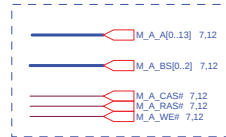
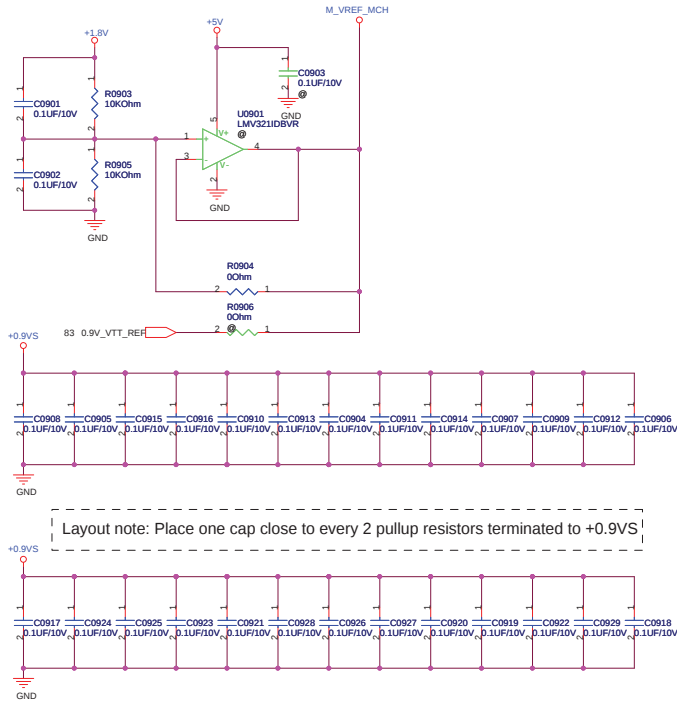


VREF -> 10/10 mils

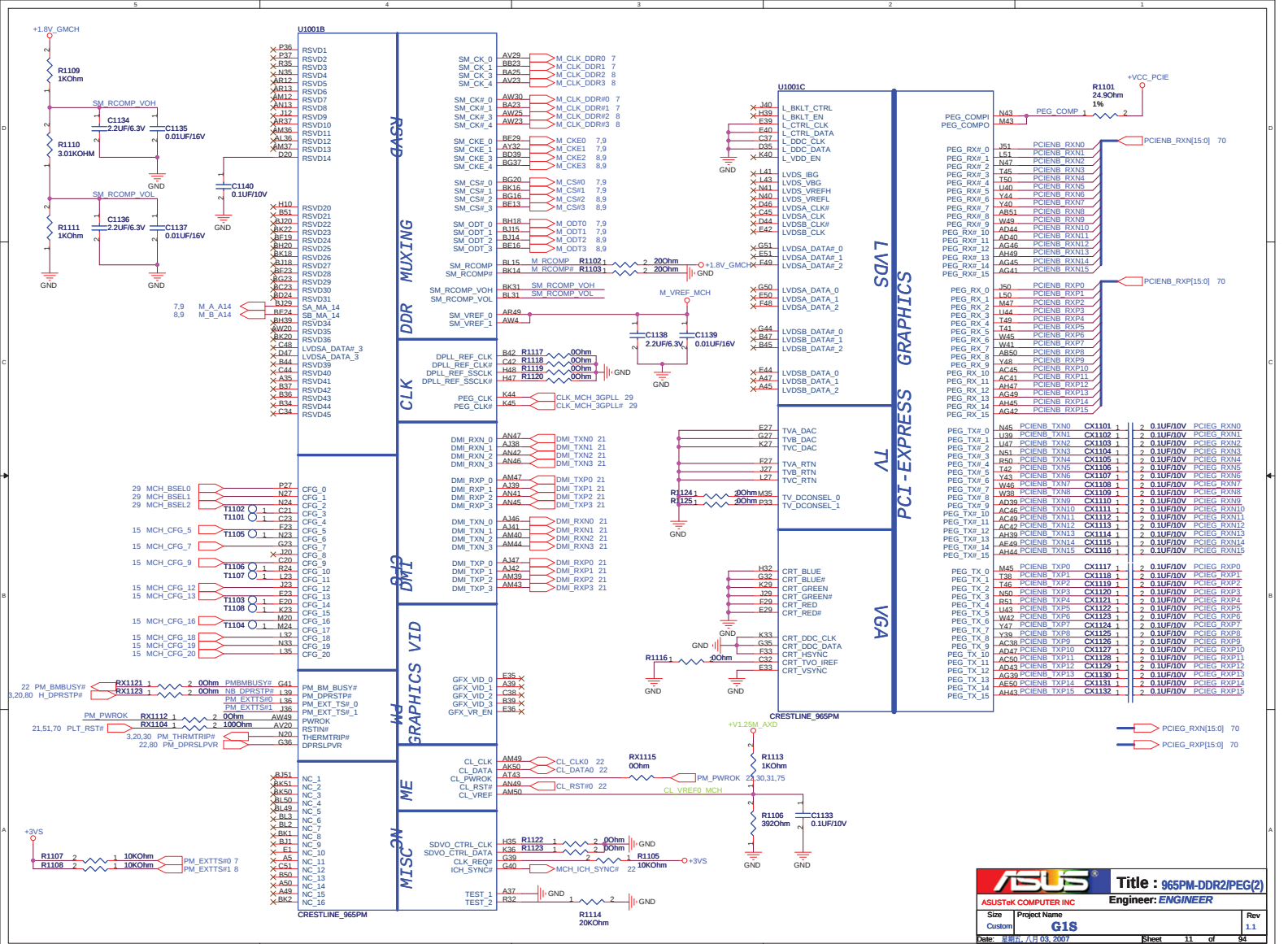


+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve SUSB# and SUSC#

HAD SWAPED







7 M_A_DQ[0:63]

U1001D

M_A DQ0 AR43 SA_DQ_0
M_A DQ1 AR44 SA_DQ_1
M_A DQ2 AR45 SA_DQ_2
M_A DQ3 AY46 SA_DQ_3
M_A DQ4 AR41 SA_DQ_4
M_A DQ5 AR45 SA_DQ_5
M_A DQ6 AT42 SA_DQ_6
M_A DQ7 AW41 SA_DQ_7
M_A DQ8 BR45 SA_DQ_8
M_A DQ9 BF48 SA_DQ_9
M_A DQ10 BC47 SA_DQ_10
M_A DQ11 BJ45 SA_DQ_11
M_A DQ12 BR47 SA_DQ_12
M_A DQ13 BG50 SA_DQ_13
M_A DQ14 BR49 SA_DQ_14
M_A DQ15 BE45 SA_DQ_15
M_A DQ16 AW43 SA_DQ_16
M_A DQ17 BE44 SA_DQ_17
M_A DQ18 BG42 SA_DQ_18
M_A DQ19 BE40 SA_DQ_19
M_A DQ20 BF44 SA_DQ_20
M_A DQ21 BR45 SA_DQ_21
M_A DQ22 BG40 SA_DQ_22
M_A DQ23 BF40 SA_DQ_23
M_A DQ24 AR40 SA_DQ_24
M_A DQ25 AW40 SA_DQ_25
M_A DQ26 AT39 SA_DQ_26
M_A DQ27 AW36 SA_DQ_27
M_A DQ28 AW41 SA_DQ_28
M_A DQ29 AV41 SA_DQ_29
M_A DQ30 AV38 SA_DQ_30
M_A DQ31 AT38 SA_DQ_31
M_A DQ32 AV33 SA_DQ_32
M_A DQ33 AT13 SA_DQ_33
M_A DQ34 AW11 SA_DQ_34
M_A DQ35 AV11 SA_DQ_35
M_A DQ36 AU15 SA_DQ_36
M_A DQ37 AT11 SA_DQ_37
M_A DQ38 BA13 SA_DQ_38
M_A DQ39 BA11 SA_DQ_39
M_A DQ40 BC10 SA_DQ_40
M_A DQ41 BD10 SA_DQ_41
M_A DQ42 BD8 SA_DQ_42
M_A DQ43 A19 SA_DQ_43
M_A DQ44 BG10 SA_DQ_44
M_A DQ45 AW9 SA_DQ_45
M_A DQ46 BD7 SA_DQ_46
M_A DQ47 BR9 SA_DQ_47
M_A DQ48 BR5 SA_DQ_48
M_A DQ49 AV7 SA_DQ_49
M_A DQ50 AT5 SA_DQ_50
M_A DQ51 AT7 SA_DQ_51
M_A DQ52 AV6 SA_DQ_52
M_A DQ53 BR7 SA_DQ_53
M_A DQ54 AR5 SA_DQ_54
M_A DQ55 AR8 SA_DQ_55
M_A DQ56 AR9 SA_DQ_56
M_A DQ57 AN3 SA_DQ_57
M_A DQ58 AM5 SA_DQ_58
M_A DQ59 AN10 SA_DQ_59
M_A DQ60 AT9 SA_DQ_60
M_A DQ61 AN9 SA_DQ_61
M_A DQ62 AM9 SA_DQ_62
M_A DQ63 AN11 SA_DQ_63

CRESTLINE_965PM

DDR SYSTEM MEMORY A

SA_BS_0 BB19 M_A_BS0 7.9
SA_BS_1 BA45 M_A_BS1 7.9
SA_BS_2 BF29 M_A_BS2 7.9
SA_CAS# BL17 M_A_CAS# 7.9
SA_DM_0 AT45 M_A_DM0
SA_DM_1 BD44 M_A_DM1
SA_DM_2 BD42 M_A_DM2
SA_DM_3 AW38 M_A_DM3
SA_DM_4 AW13 M_A_DM4
SA_DM_5 BG38 M_A_DM5
SA_DM_6 AT5 M_A_DM6
SA_DM_7 AN6 M_A_DM7
SA_DQS_0 AT45 M_A_DQS0
SA_DQS_1 BE48 M_A_DQS1
SA_DQS_2 BR43 M_A_DQS2
SA_DQS_3 BC37 M_A_DQS3
SA_DQS_4 BR16 M_A_DQS4
SA_DQS_5 RH46 M_A_DQS5
SA_DQS_6 BR2 M_A_DQS6
SA_DQS_7 AP3 M_A_DQS7
SA_DQS_8 AT47 M_A_DQS8
SA_DQS_9 BD47 M_A_DQS9
SA_DQS_10 BA37 M_A_DQS10
SA_DQS_11 BA16 M_A_DQS11
SA_DQS_12 BH47 M_A_DQS12
SA_DQS_13 BC1 M_A_DQS13
SA_DQS_14 AF2 M_A_DQS14
SA_DQS_15
SA_MA_0 B119 M_A_A0
SA_MA_1 BD20 M_A_A1
SA_MA_2 BK27 M_A_A2
SA_MA_3 BH26 M_A_A3
SA_MA_4 BL24 M_A_A4
SA_MA_5 BK28 M_A_A5
SA_MA_6 B127 M_A_A6
SA_MA_7 B125 M_A_A7
SA_MA_8 BL28 M_A_A8
SA_MA_9 BA28 M_A_A9
SA_MA_10 BC19 M_A_A10
SA_MA_11 BE26 M_A_A11
SA_MA_12 BC30 M_A_A12
SA_MA_13 B116 M_A_A13
SA_RAS# BE18 M_A_RAS# 7.9
SA_RCVEN# AY23 M_A_RCVEN#
SA_WE# BA19 M_A_WE# 7.9

8 M_B_DQ[0:63]

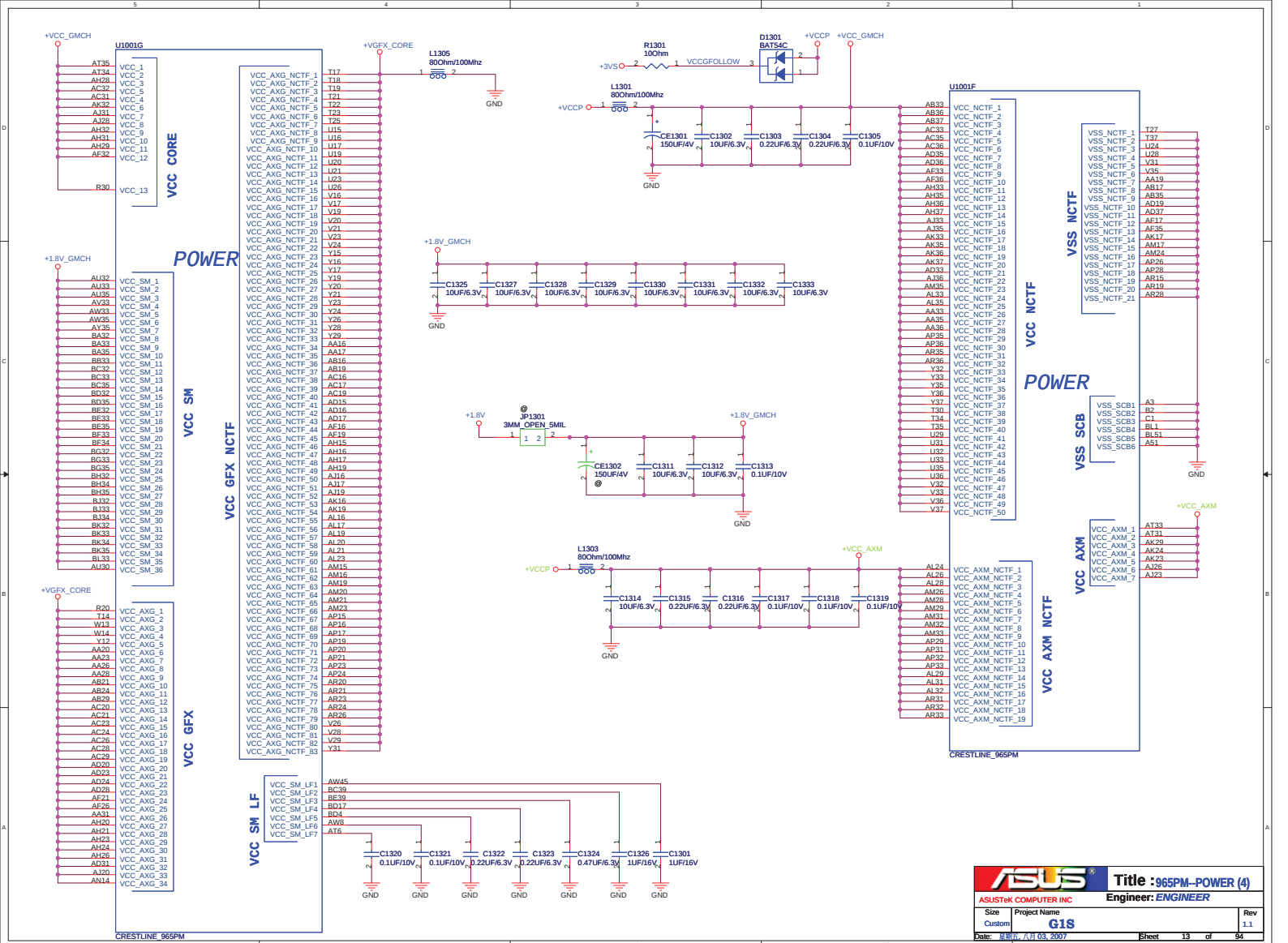
U1001E

M_B DQ0 AP49 SB_DQ_0
M_B DQ1 AR51 SB_DQ_1
M_B DQ2 AW50 SB_DQ_2
M_B DQ3 AW51 SB_DQ_3
M_B DQ4 AN51 SB_DQ_4
M_B DQ5 AN50 SB_DQ_5
M_B DQ6 AV50 SB_DQ_6
M_B DQ7 AV49 SB_DQ_7
M_B DQ8 BA50 SB_DQ_8
M_B DQ9 BR50 SB_DQ_9
M_B DQ10 BA49 SB_DQ_10
M_B DQ11 AE50 SB_DQ_11
M_B DQ12 BA51 SB_DQ_12
M_B DQ13 AV49 SB_DQ_13
M_B DQ14 BE50 SB_DQ_14
M_B DQ15 BE49 SB_DQ_15
M_B DQ16 B150 SB_DQ_16
M_B DQ17 B144 SB_DQ_17
M_B DQ18 B143 SB_DQ_18
M_B DQ19 BL43 SB_DQ_19
M_B DQ20 BK47 SB_DQ_20
M_B DQ21 BK49 SB_DQ_21
M_B DQ22 BK43 SB_DQ_22
M_B DQ23 BK42 SB_DQ_23
M_B DQ24 B141 SB_DQ_24
M_B DQ25 BL41 SB_DQ_25
M_B DQ26 B137 SB_DQ_26
M_B DQ27 B136 SB_DQ_27
M_B DQ28 BK41 SB_DQ_28
M_B DQ29 BK40 SB_DQ_29
M_B DQ30 BL35 SB_DQ_30
M_B DQ31 BK37 SB_DQ_31
M_B DQ32 BK13 SB_DQ_32
M_B DQ33 BE11 SB_DQ_33
M_B DQ34 BK11 SB_DQ_34
M_B DQ35 BC11 SB_DQ_35
M_B DQ36 BK13 SB_DQ_36
M_B DQ37 BE12 SB_DQ_37
M_B DQ38 BC12 SB_DQ_38
M_B DQ39 BG12 SB_DQ_39
M_B DQ40 BL9 SB_DQ_40
M_B DQ41 BL9 SB_DQ_41
M_B DQ42 BE5 SB_DQ_42
M_B DQ43 BL9 SB_DQ_43
M_B DQ44 BK9 SB_DQ_44
M_B DQ45 BK10 SB_DQ_45
M_B DQ46 BL8 SB_DQ_46
M_B DQ47 BL6 SB_DQ_47
M_B DQ48 BE4 SB_DQ_48
M_B DQ49 BH5 SB_DQ_49
M_B DQ50 BG1 SB_DQ_50
M_B DQ51 BE2 SB_DQ_51
M_B DQ52 BK3 SB_DQ_52
M_B DQ53 BE4 SB_DQ_53
M_B DQ54 BD3 SB_DQ_54
M_B DQ55 B12 SB_DQ_55
M_B DQ56 BA3 SB_DQ_56
M_B DQ57 BE3 SB_DQ_57
M_B DQ58 AR1 SB_DQ_58
M_B DQ59 AT3 SB_DQ_59
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M_B DQ62 AU2 SB_DQ_62
M_B DQ63 AT2 SB_DQ_63

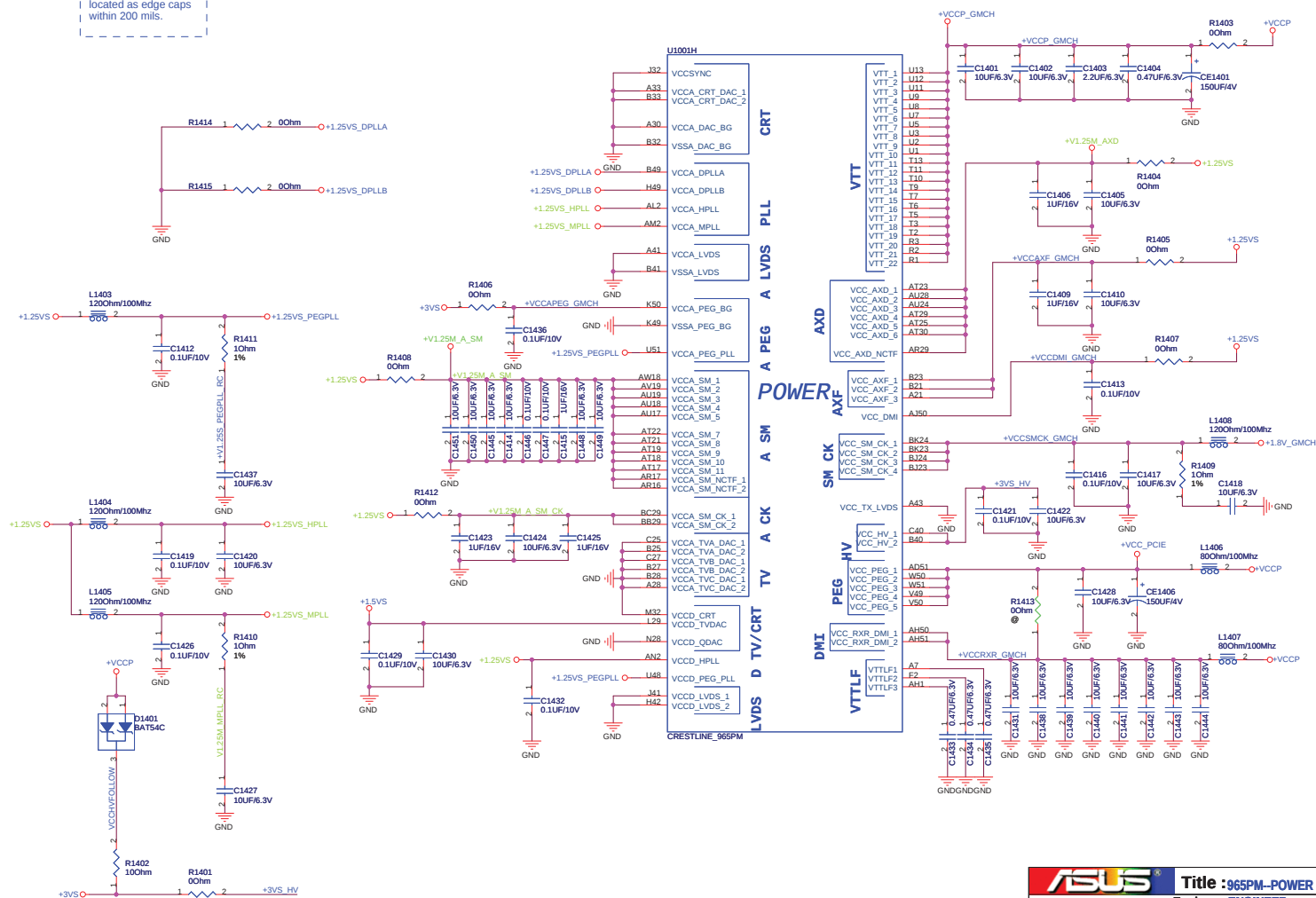
CRESTLINE_965PM

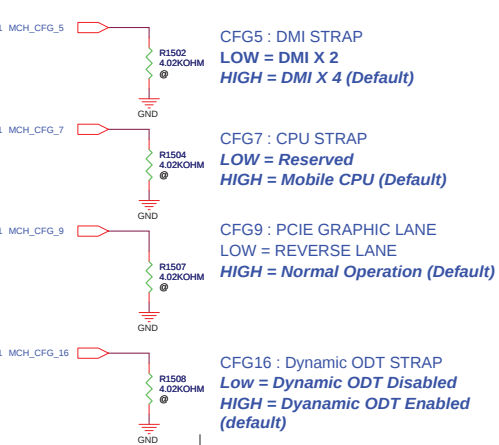
DDR SYSTEM MEMORY B

SB_BS_0 AY17 M_B_BS0 8.9
SB_BS_1 BG36 M_B_BS1 8.9
SB_BS_2 BG36 M_B_BS2 8.9
SB_CAS# BE17 M_B_CAS# 8.9
SB_DM_0 AR50 M_B_DM0
SB_DM_1 BD49 M_B_DM1
SB_DM_2 BR45 M_B_DM2
SB_DM_3 BL39 M_B_DM3
SB_DM_4 BH12 M_B_DM4
SB_DM_5 BJ7 M_B_DM5
SB_DM_6 BE3 M_B_DM6
SB_DM_7 AW2 M_B_DM7
SB_DQS_0 AT50 M_B_DQS0
SB_DQS_1 BD50 M_B_DQS1
SB_DQS_2 BK46 M_B_DQS2
SB_DQS_3 BK39 M_B_DQS3
SB_DQS_4 B112 M_B_DQS4
SB_DQS_5 BL7 M_B_DQS5
SB_DQS_6 AY2 M_B_DQS6
SB_DQS_7 AV2 M_B_DQS7
SB_DQS_8 AU50 M_B_DQS8
SB_DQS_9 BV2 M_B_DQS9
SB_DQS_10 BL45 M_B_DQS10
SB_DQS_11 BK38 M_B_DQS11
SB_DQS_12 BK12 M_B_DQS12
SB_DQS_13 BK1 M_B_DQS13
SB_DQS_14 BE1 M_B_DQS14
SB_DQS_15 AV3 M_B_DQS15
SB_MA_0 BC18 M_B_A0
SB_MA_1 BG28 M_B_A1
SB_MA_2 BG25 M_B_A2
SB_MA_3 AW17 M_B_A3
SB_MA_4 BE25 M_B_A4
SB_MA_5 BA29 M_B_A5
SB_MA_6 BC28 M_B_A6
SB_MA_7 AY28 M_B_A7
SB_MA_8 BD37 M_B_A8
SB_MA_9 BG17 M_B_A9
SB_MA_10 BE37 M_B_A10
SB_MA_11 BG19 M_B_A11
SB_MA_12 BA33 M_B_A12
SB_MA_13 BG13 M_B_A13
SB_RAS# AV16 M_B_RAS# 8.9
SB_RCVEN# AY15 M_B_RCVEN#
SB_WE# BC17 M_B_WE# 8.9



NOTE: 0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.





CFG5 : DMI STRAP
LOW = DMI X 2
HIGH = DMI X 4 (Default)

CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobile CPU (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = Normal Operation (Default)

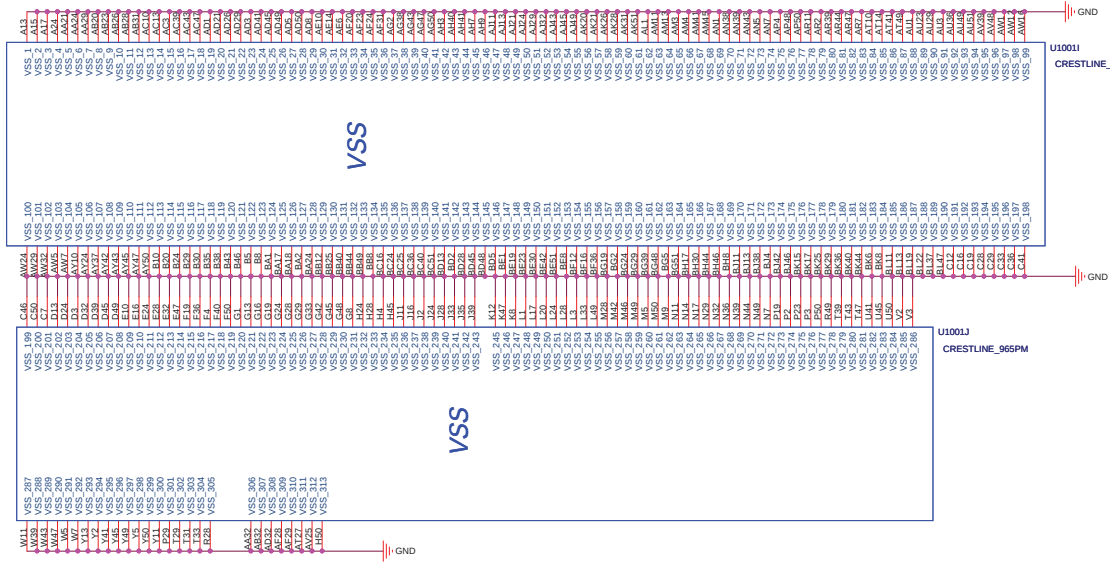
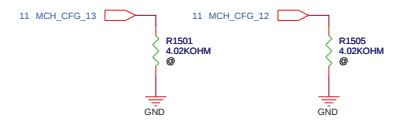
CFG16 : Dynamic ODT STRAP
Low = Dynamic ODT Disabled
HIGH = Dyanamic ODT Enabled (default)

CFG18 : VCC SELECT
LOW = 1.05V (default)
HIGH = 1.5V

CFG19 : DMI LANE REVERSAL
LOW = NORMAL (default)
HIGH = LANES REVERSED

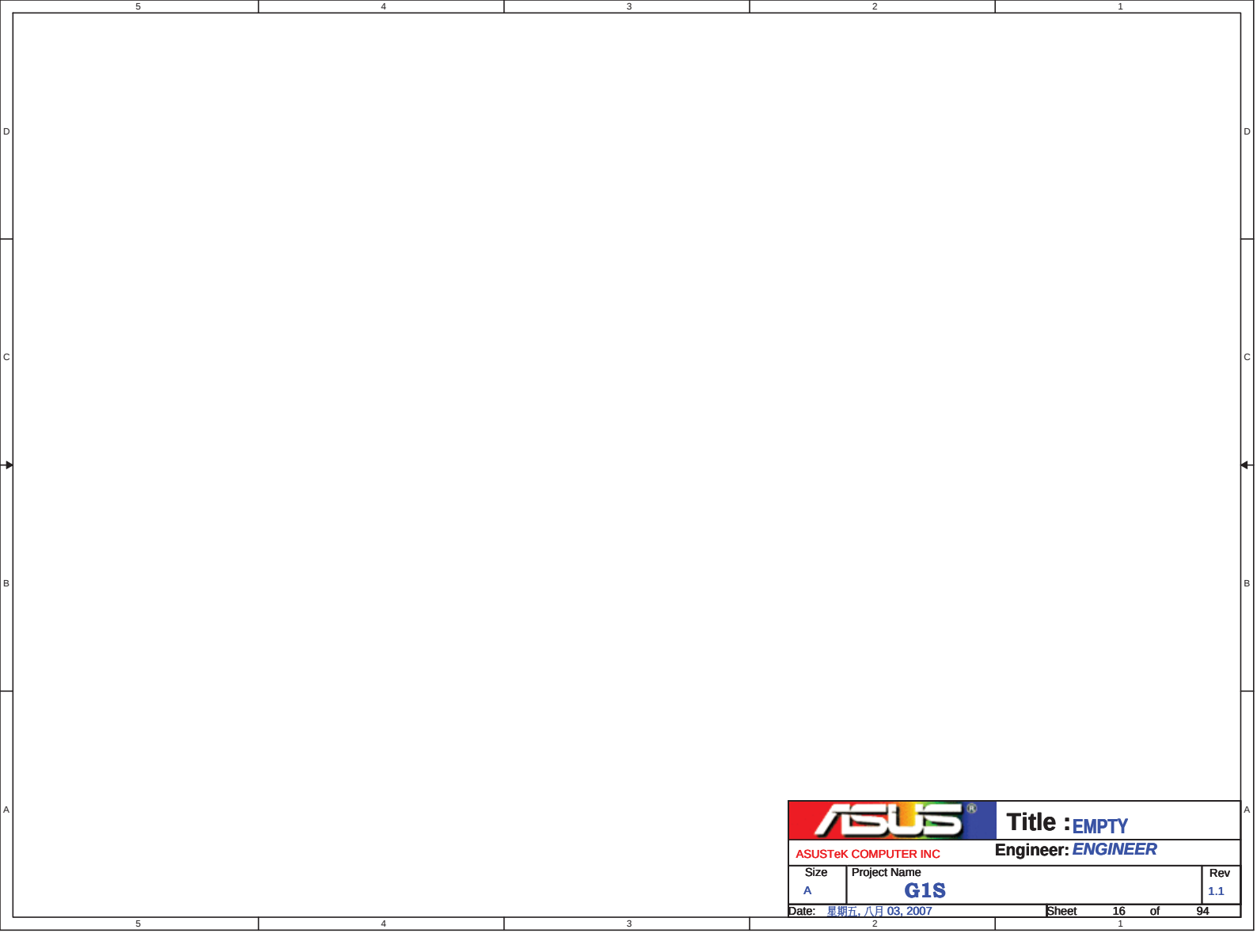
CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

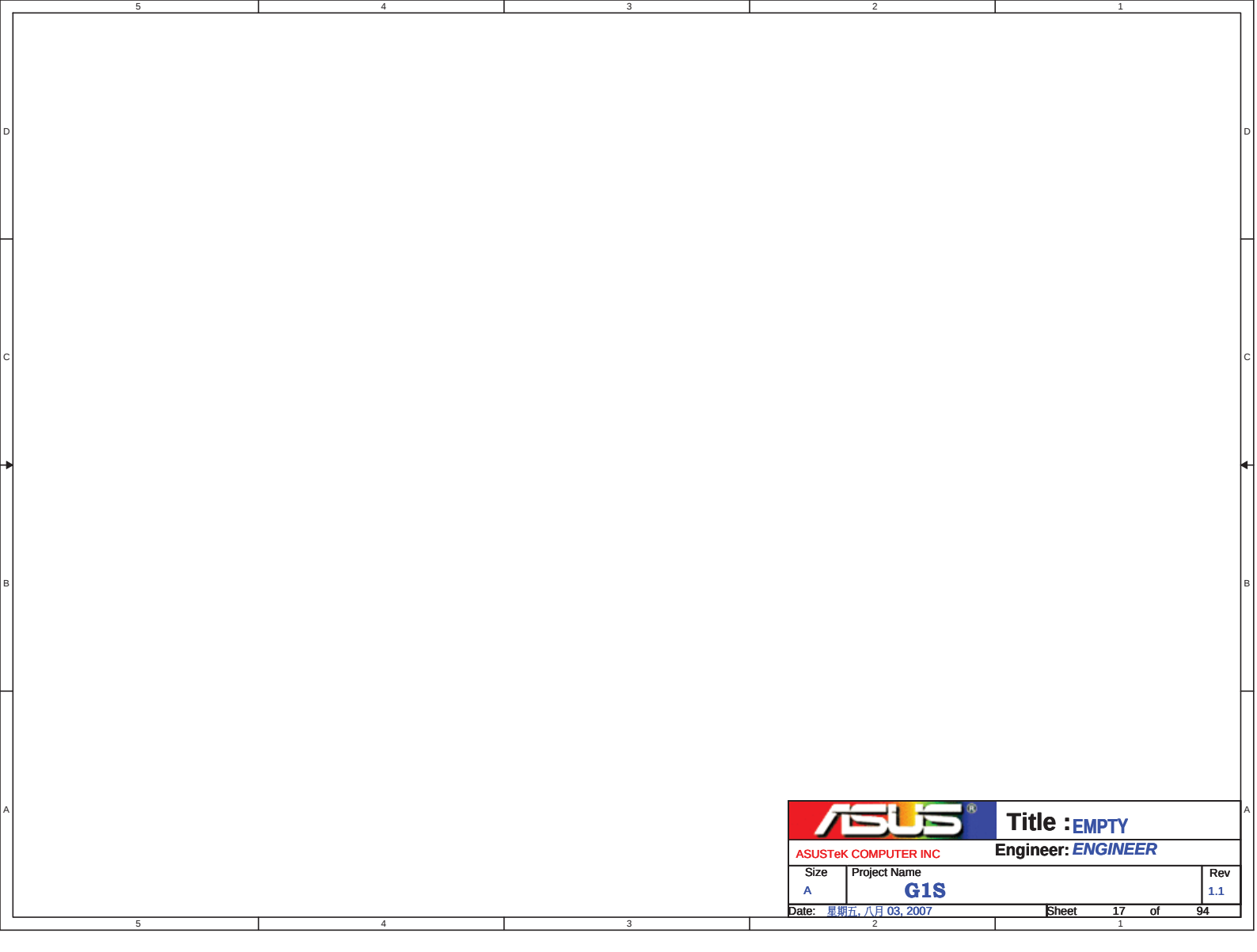


U1001J
CRESTLINE_965PM

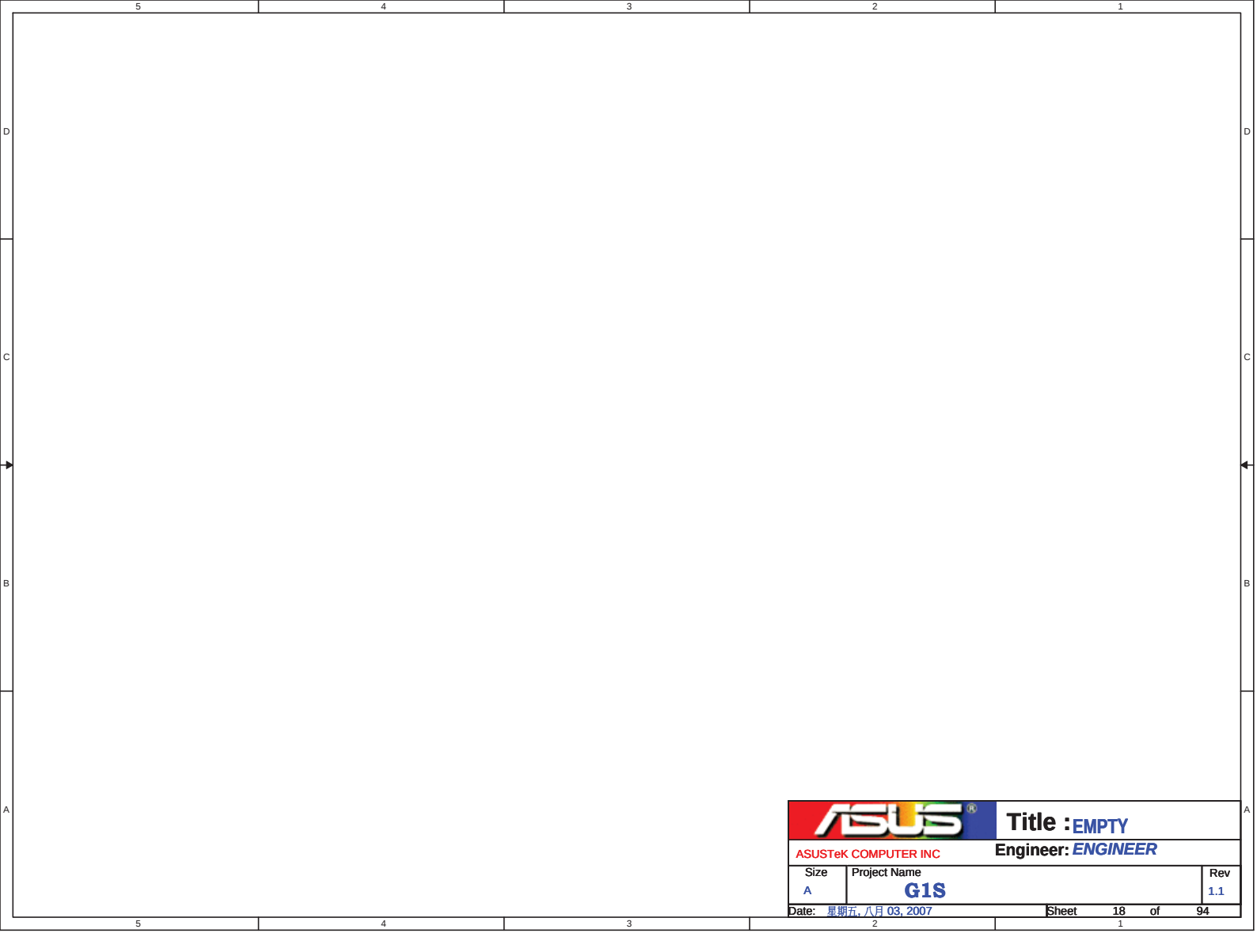
U1001J
CRESTLINE_965PM



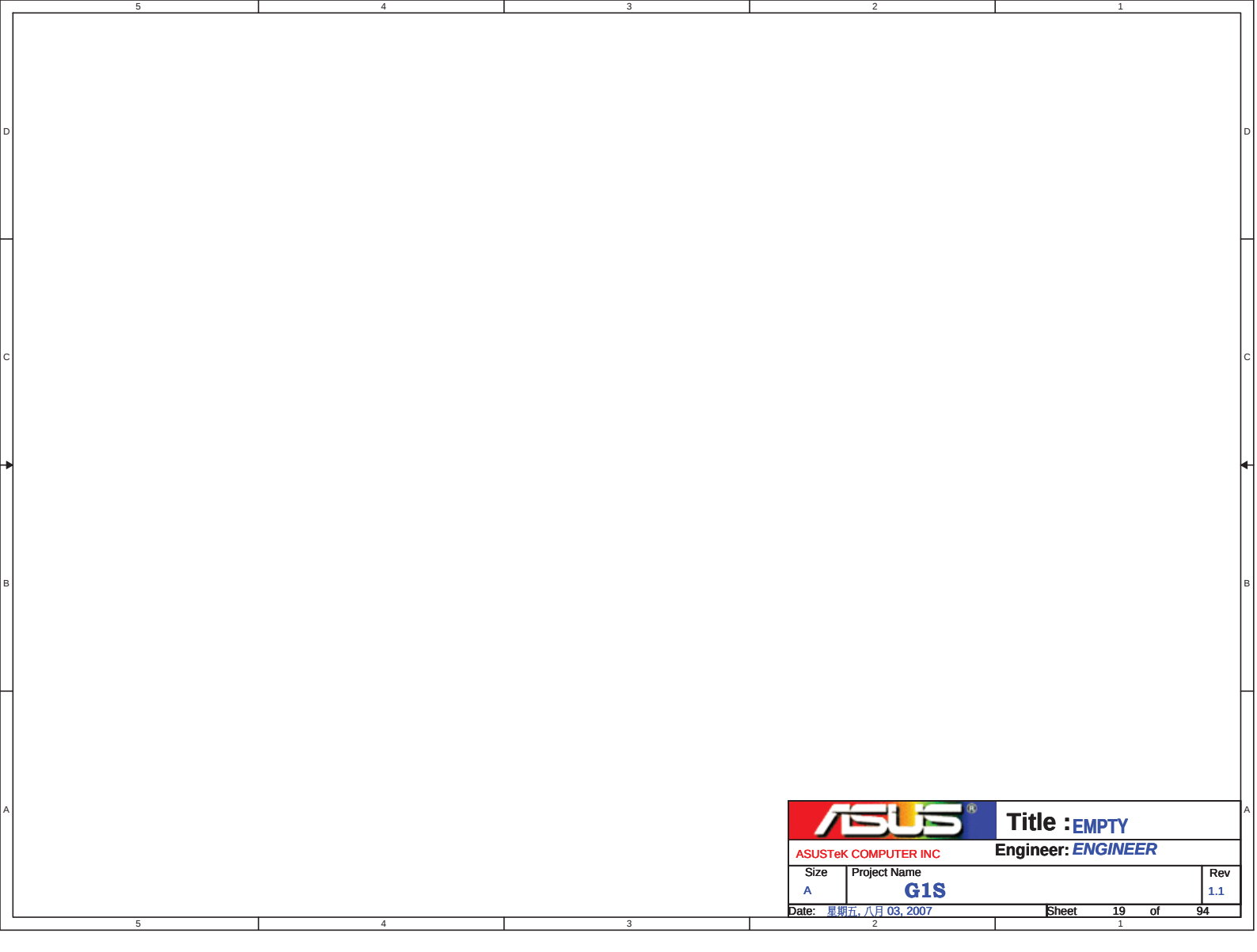
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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	16 of 94



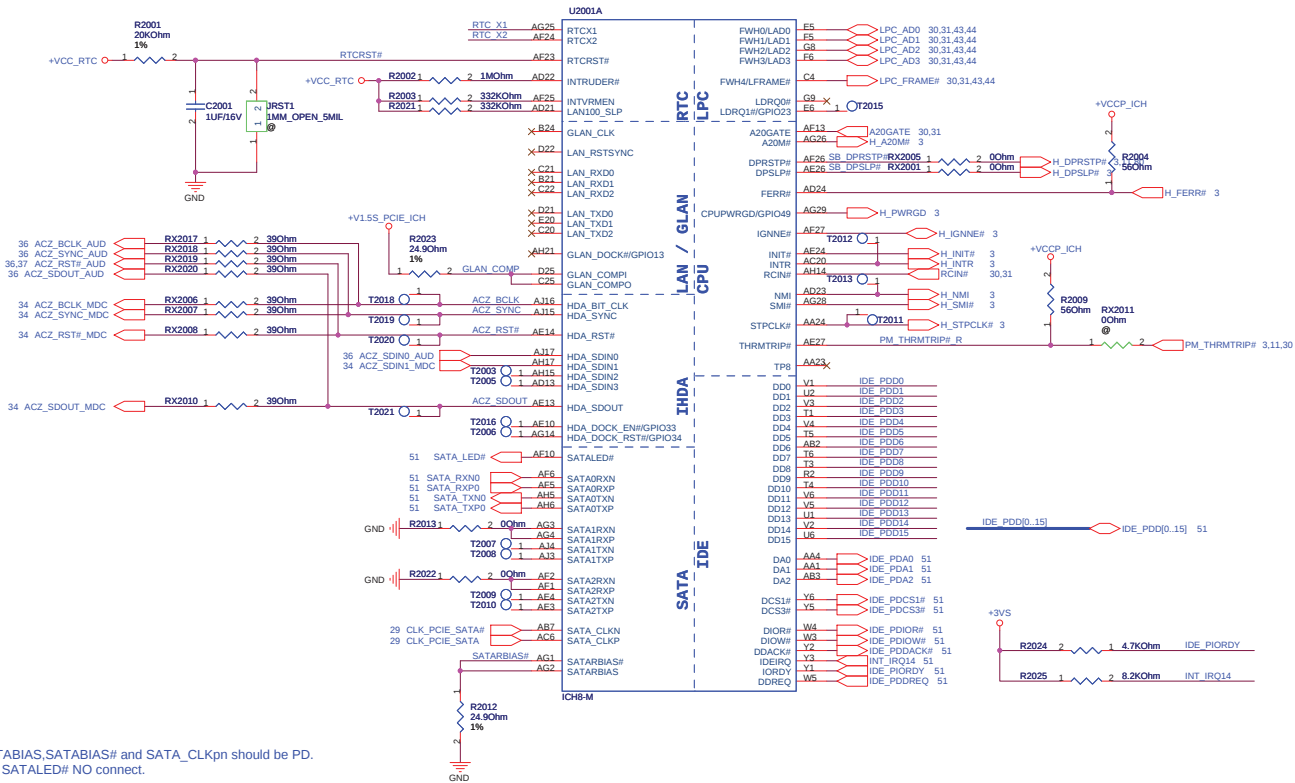
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Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	17 of 94



		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	18 of 94

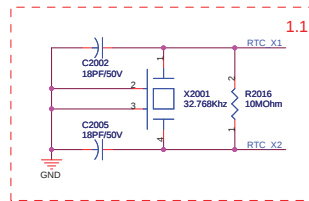
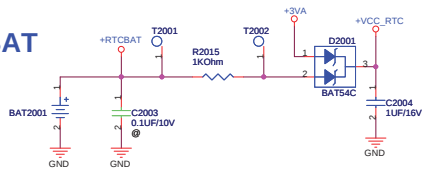


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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	19 of 94

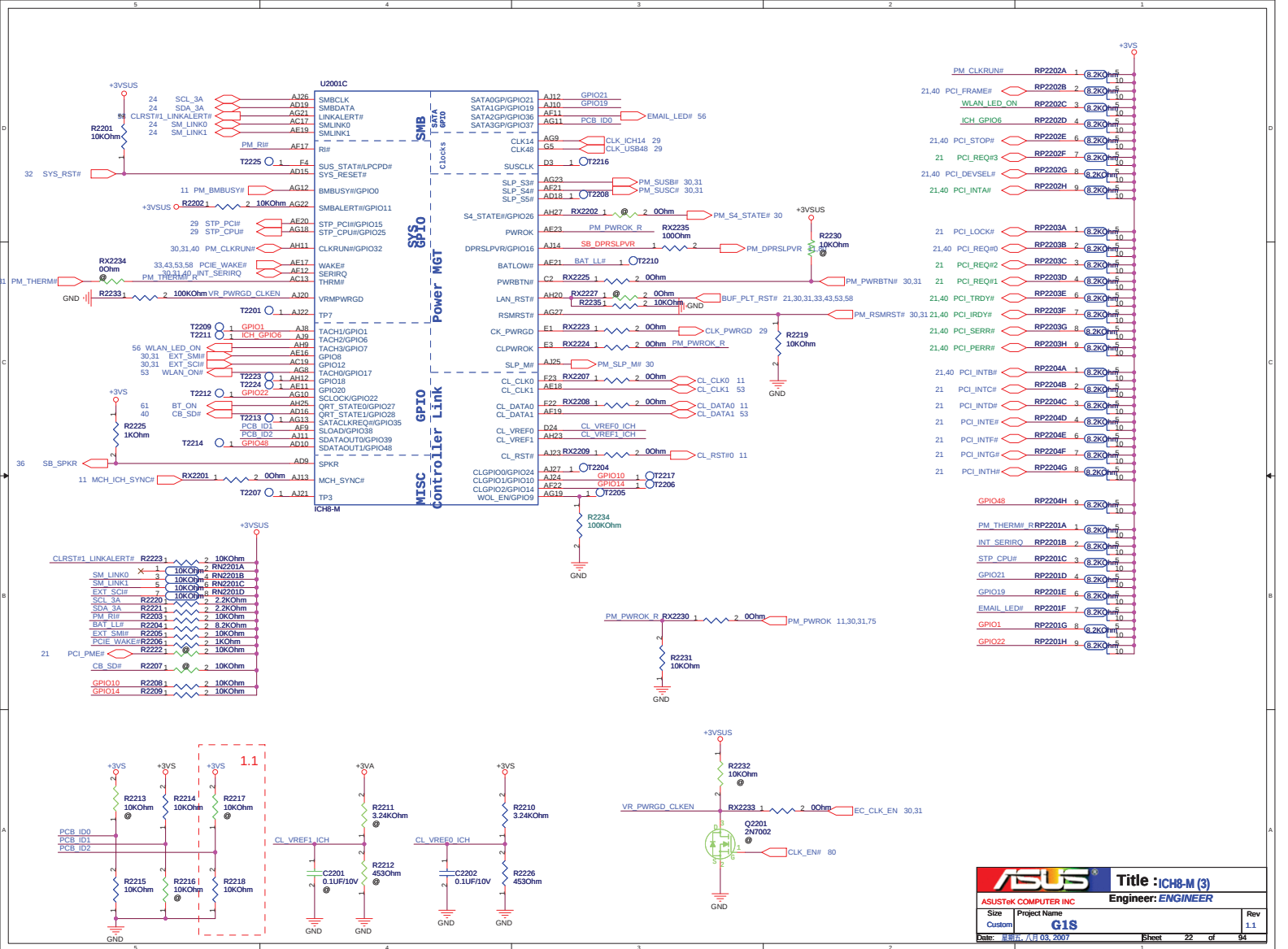


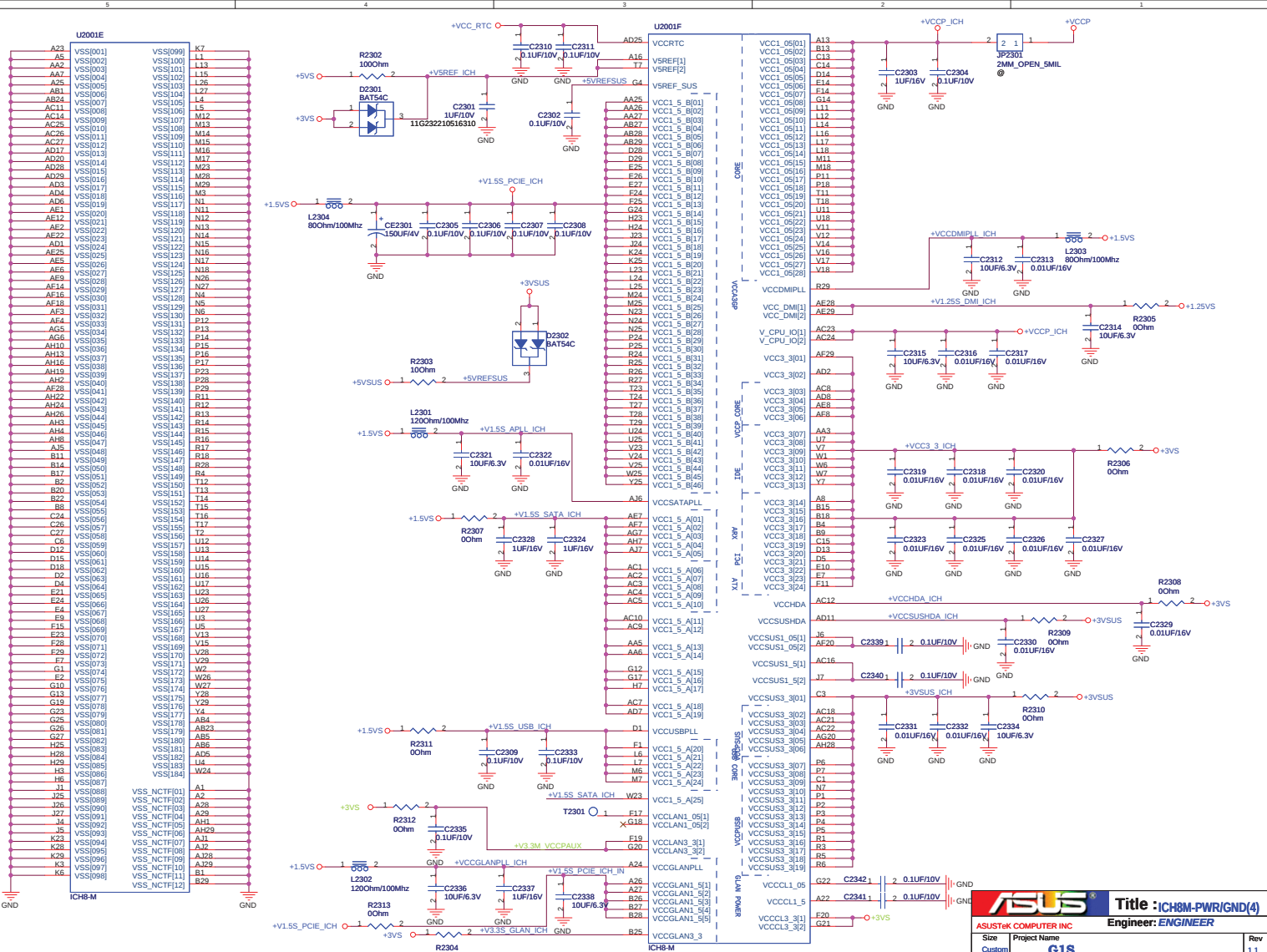
RTC BAT

RTC Battery
P/N=07G016102032



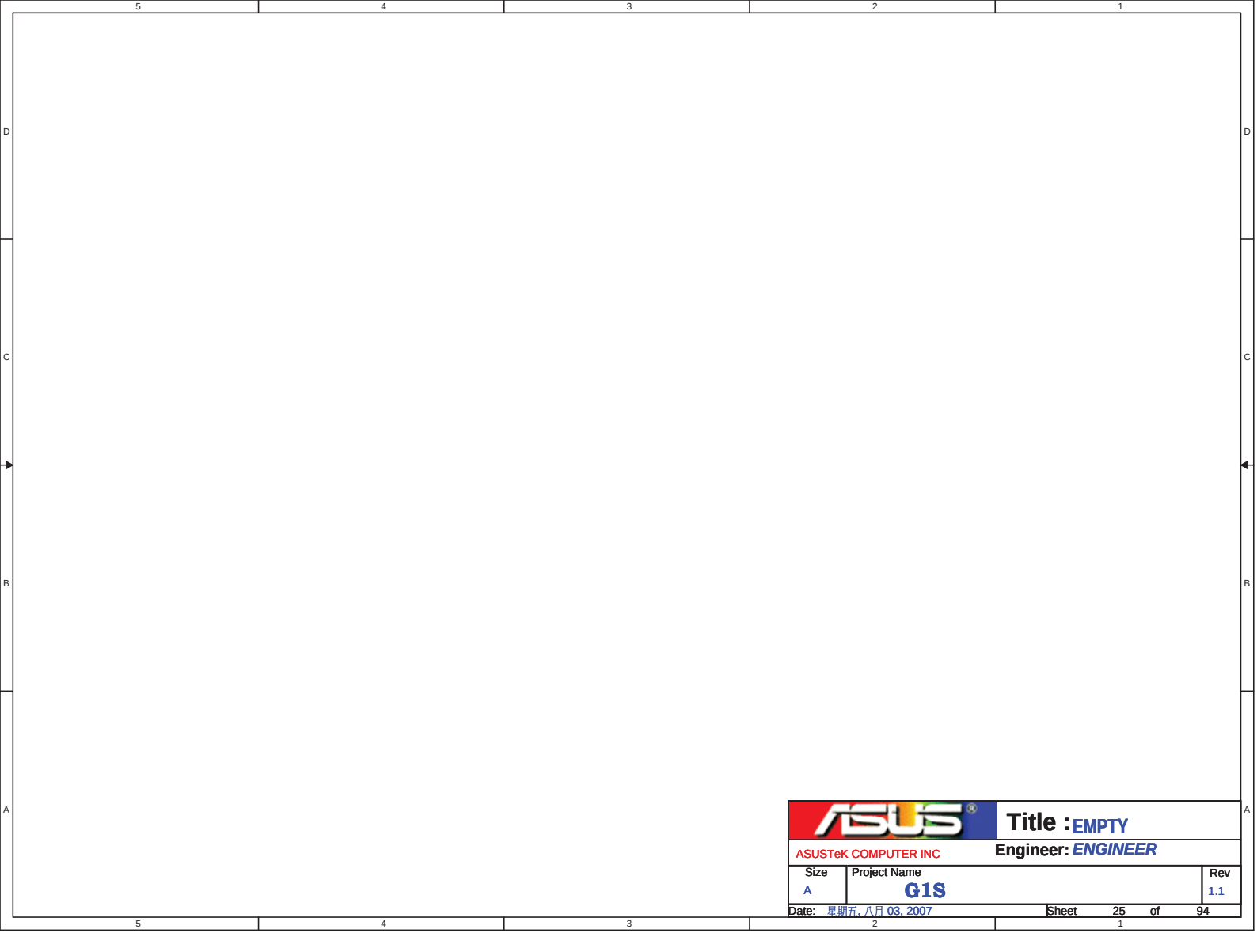




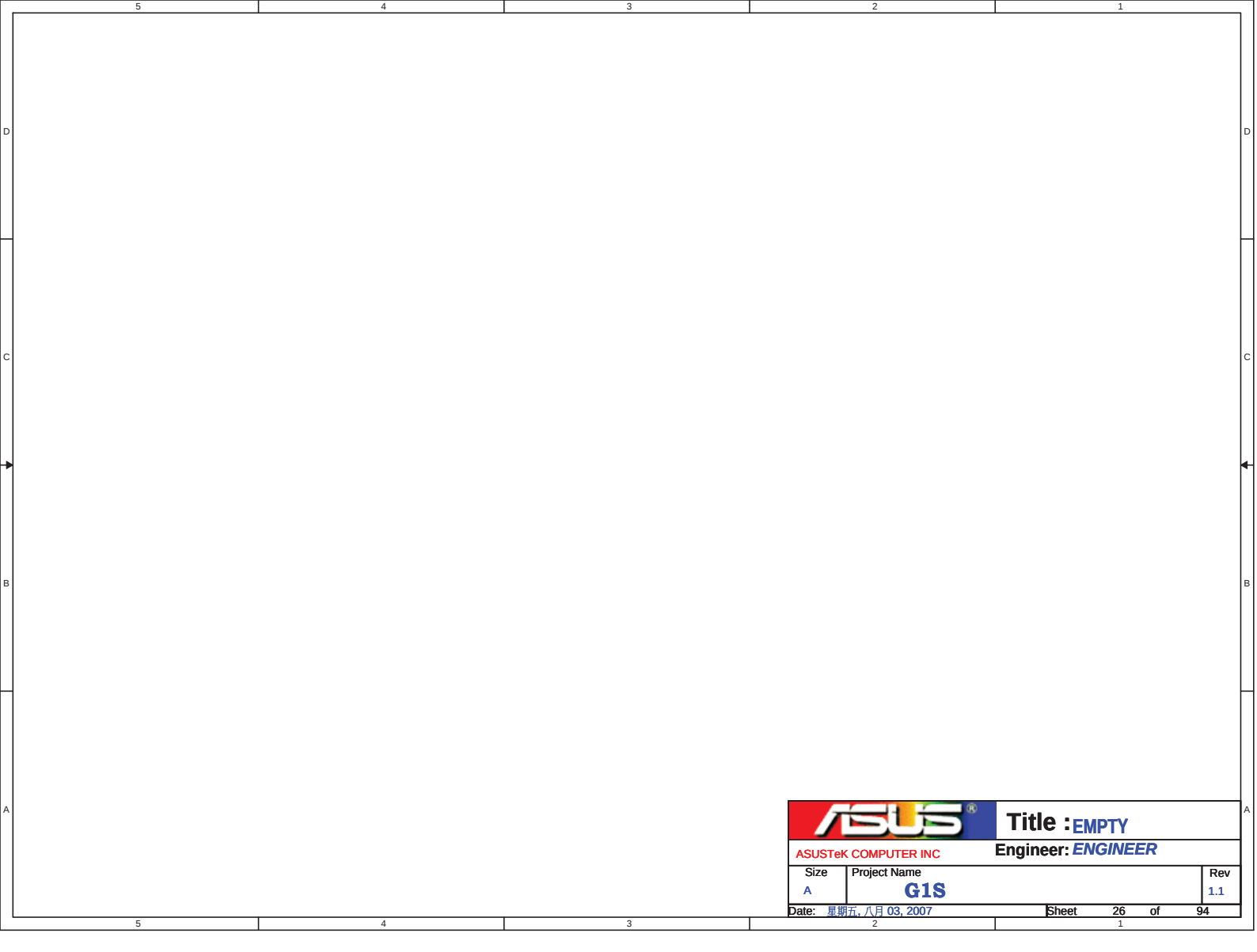


ICH8-M

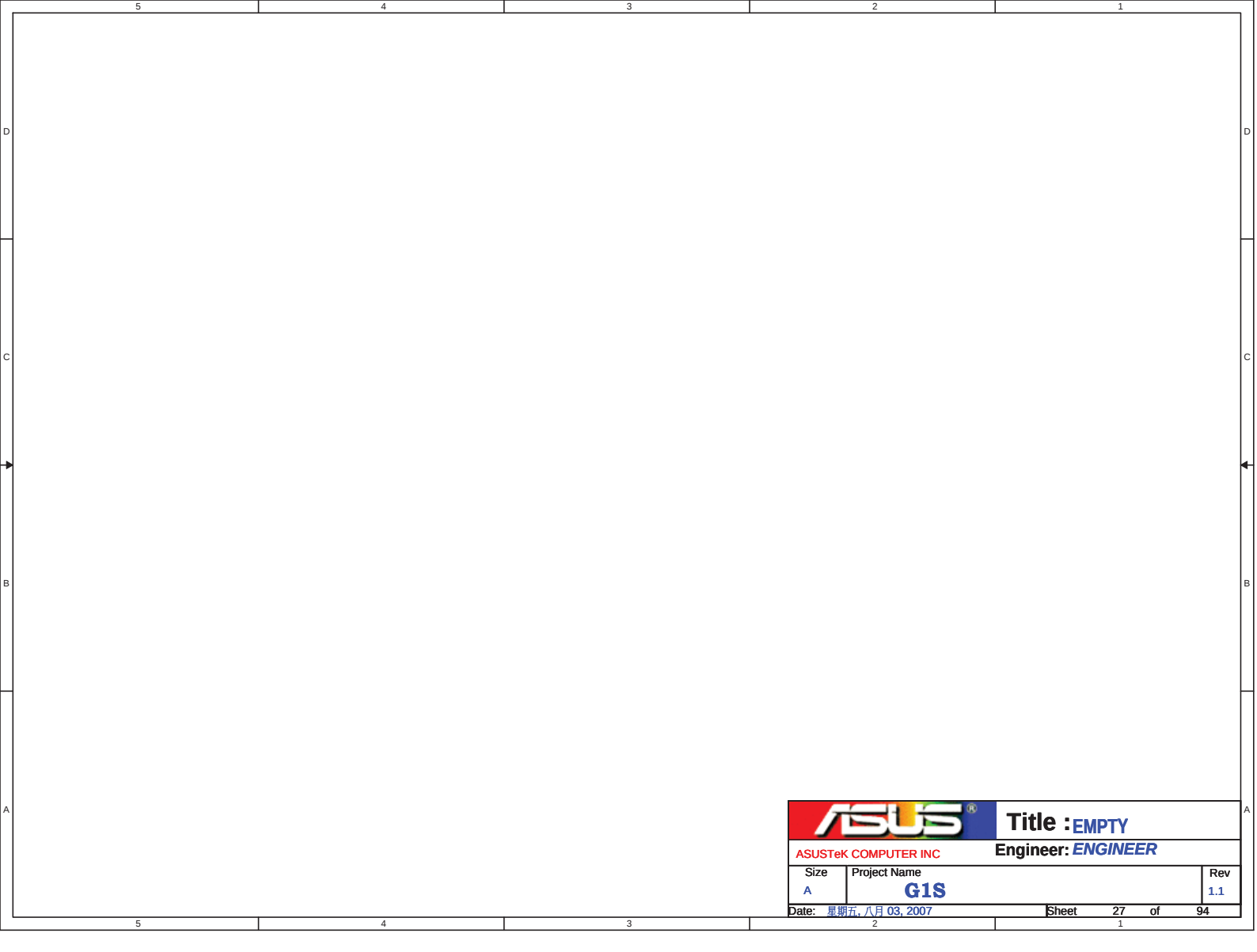




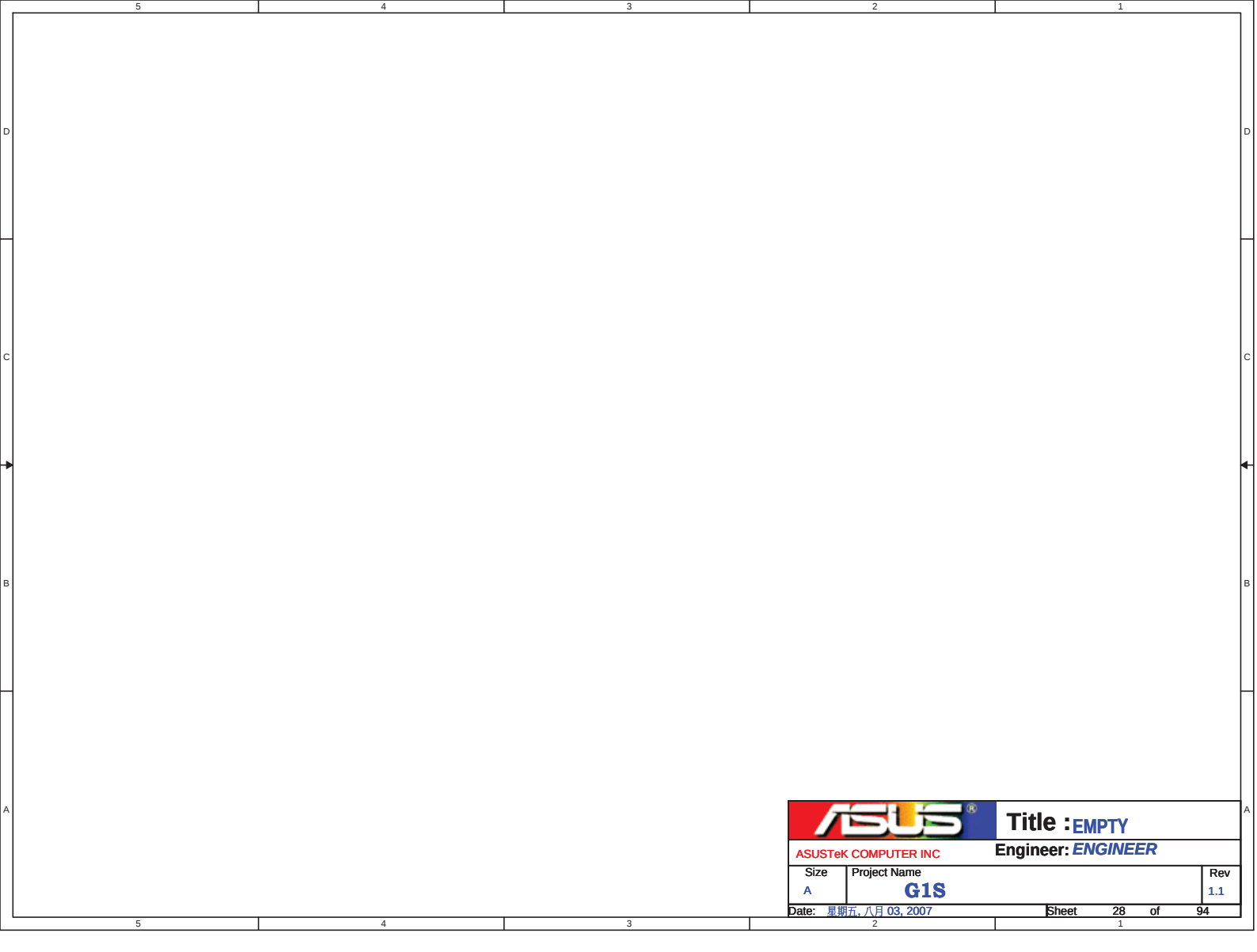
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Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	25 of 94



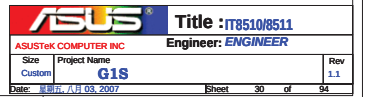
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Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	26 of 94



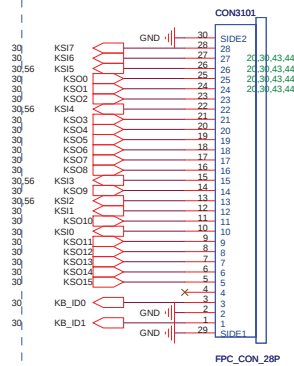
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Date: 星期五, 八月 03, 2007		Sheet	27 of 94



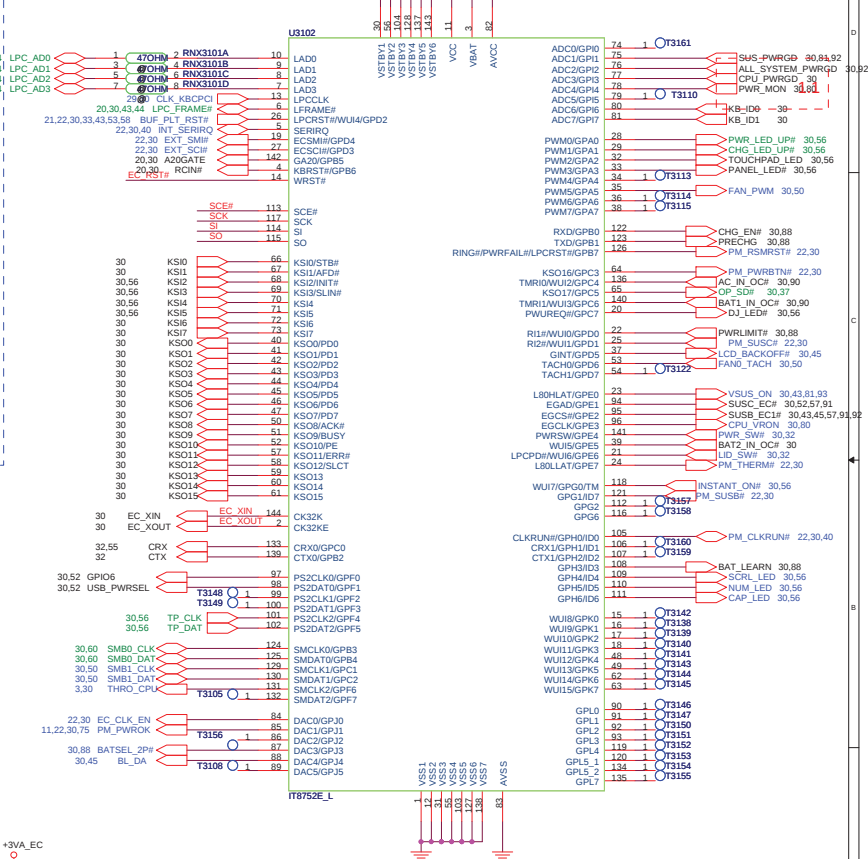
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ASUSTeK COMPUTER INC		Engineer: ENGINEER	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	28 of 94



KBD CONN



Colay IT8752E



1MB SPI ROM

