ZR6E SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:A

DDR2 PWR TPS51116 P35 | CHARGER ISL6251 P31
THERMAL PROTECTION P38 | 3/5V SYS PWR ISL6237 P32
DISCHARGER P37 | CPU CORE PWR OZ8116LN P34
VGA CORE OZ8118 P36 | +1.05V UP6111AQDD P33

X'TAL 14.318MHz
CLOCK GENERATOR
ICS:
SELGO: SLG8SP512TTR
P2

Penryn 479
uFCPGA
P3, P4

Thermal Sensor
(G780-1P81U) P3

Fan Driver
(G991) P24

FSB
667/800 MHz

NVIDIA N10M-GE1
VRAM DDRII 1GB P17-P23

PCIE 16X

EXT_LVDS
EXT_CRT

SWITCH CIRCUIT P23

CRT P23

LVDS P23

DDRII
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR2
667/800 MHz

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

LVDS — INT_LVDS
RGB — INT_CRT

X4 DMI interface

HDD (SATA) *1 P24

ODD (SATA) P24

Ext USB Port x 2 USB 0,1 P25
Int USB Port x 1 USB 7 P25
Bluetooth USB5 P25
CCD USB11 P23

SATA0
SATA1
USB 2.0
Azalia

SB ICH9M
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-1

Mini Card WLAN P25

USB8

PCIE-6

X'TAL 25MHz

Media Cardreader
(RTS5159)
USB2 P29

Atheros Giga-LAN
(AR8131) P27

Card Reader Connector P29

Transformer P28

RJ45 P28

LPC

EC (WPC775LDG) P30

X'TAL 32.768KHz

SPI ROM P30

Touch Pad P24

K/B COON. P30

Audio CODEC (CX20561) P26

Audio Amplifier G1453L P26

MIC Jack P26

Int. MIC P26

Int. Speaker P26

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PROJECT : ZR6E
Size | Document Number: Block Diagram | Rev 1A
Date: Tuesday, May 19, 2009 | Sheet 1 of 39

Clock Generator (CLK)

02

CLK VDD power range 1.05V~3.3V

Pin 56 : It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.

PCI/48M RS=33 ohm when one loading
=22 ohm when two loading

From GMCH

From Deiseret

CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

CLKREQ_A# Control SRC_0 & SRC_2

CLKREQ_B# Control LCDCLK & SRC_4

Reserve overclocking

Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

CLK-GEN_SLG8SP512TTR

CLOCK GENERATOR

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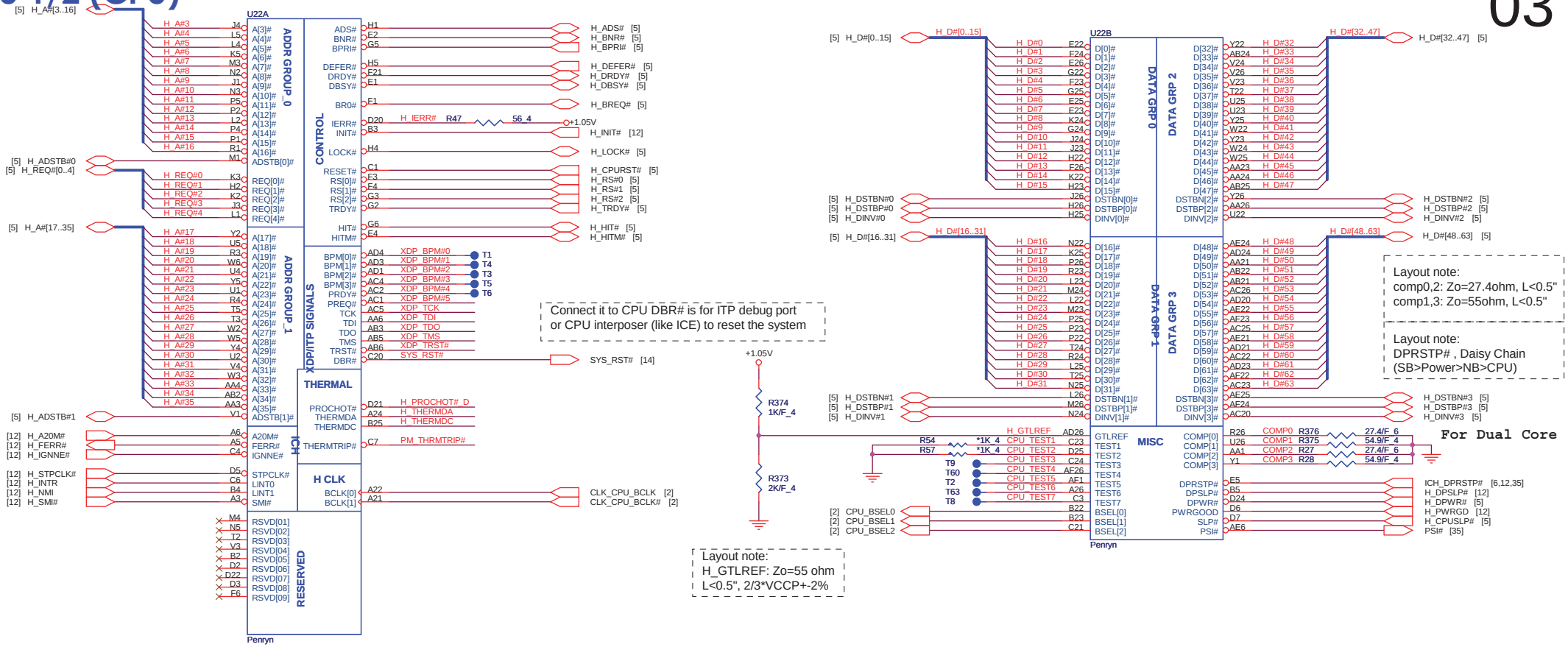
PROJECT : ZR6E

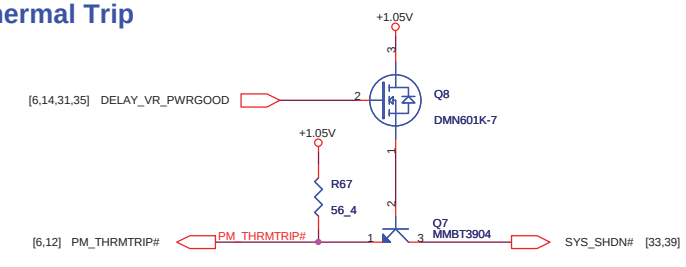
Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Tuesday, May 19, 2009	Sheet 2 of 39	

CPU 1/2 (CPU)

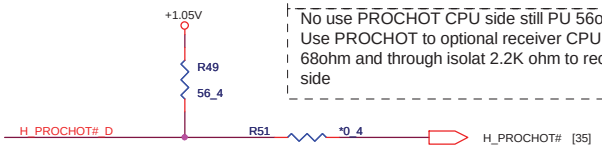
03



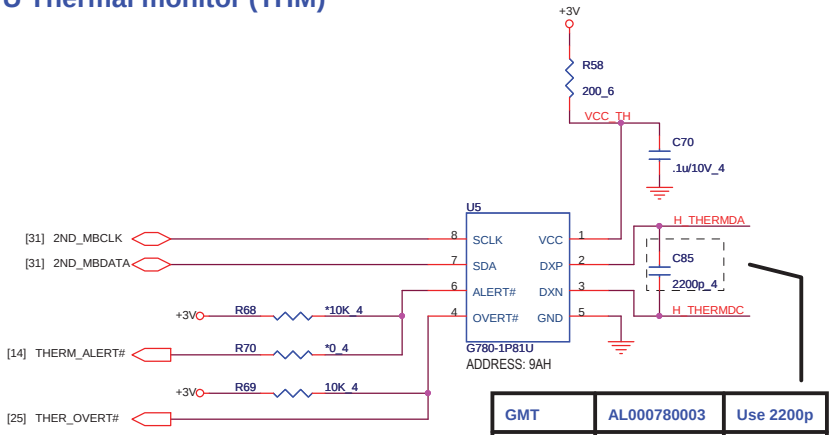
Thermal Trip



Processor hot

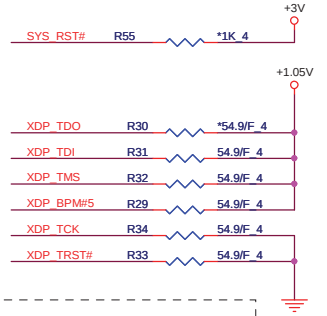


CPU Thermal monitor (THM)



GMT	AL000780003	Use 2200p
WINDBOND	AL83L771001	Check

XDP PU/PD



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PROJECT : ZR6E

Size	Document Number	Rev
	CPU Host Bus	1A
Date: Tuesday, May 19, 2009	Sheet 3 of 39	

CPU 2/2 (CPU)

04

U22D

A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3

VSS[001] VSS[002] VSS[003] VSS[004] VSS[005] VSS[006] VSS[007] VSS[008] VSS[009] VSS[010] VSS[011] VSS[012] VSS[013] VSS[014] VSS[015] VSS[016] VSS[017] VSS[018] VSS[019] VSS[020] VSS[021] VSS[022] VSS[023] VSS[024] VSS[025] VSS[026] VSS[027] VSS[028] VSS[029] VSS[030] VSS[031] VSS[032] VSS[033] VSS[034] VSS[035] VSS[036] VSS[037] VSS[038] VSS[039] VSS[040] VSS[041] VSS[042] VSS[043] VSS[044] VSS[045] VSS[046] VSS[047] VSS[048] VSS[049] VSS[050] VSS[051] VSS[052] VSS[053] VSS[054] VSS[055] VSS[056] VSS[057] VSS[058] VSS[059] VSS[060] VSS[061] VSS[062] VSS[063] VSS[064] VSS[065] VSS[066] VSS[067] VSS[068] VSS[069] VSS[070] VSS[071] VSS[072] VSS[073] VSS[074] VSS[075] VSS[076] VSS[077] VSS[078] VSS[079] VSS[080] VSS[081]

VSS[082] VSS[083] VSS[084] VSS[085] VSS[086] VSS[087] VSS[088] VSS[089] VSS[090] VSS[091] VSS[092] VSS[093] VSS[094] VSS[095] VSS[096] VSS[097] VSS[098] VSS[099] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163]

P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

Penryn

VCC_CORE

C25 C49 C50 C48 C26 C487 C488 C62 — *10u/10V_8 10u/6.3V_8 10u/6.3V_8 *10u/10V_8 10u/6.3V_8 *10u/10V_8 *10u/10V_8 *10u/10V_8

C489 C495 C496 C497 C23 C480 C59 C483 — 10u/6.3V_8 *10u/10V_8 10u/6.3V_8 *10u/10V_8 *10u/10V_8 10u/6.3V_8 *10u/10V_8 *10u/10V_8

C53 C52 C479 C482 C66 — *10u/10V_8 *10u/10V_8 *10u/10V_8 10u/6.3V_8 10u/6.3V_8

Layout Note:
Place these parts reference to Intel demo board.

C55 C51 C65 — *10u/10V_8 *10u/10V_8 10u/6.3V_8

C63 C64 C60 C61 C492 C490 — *10u/10V_8 *10u/10V_8 10u/6.3V_8 *10u/10V_8 10u/6.3V_8 *10u/10V_8

C491 C494 C498 C499 C24 C481 — 10u/6.3V_8 10u/6.3V_8 10u/6.3V_8 *10u/10V_8 10u/6.3V_8 *10u/10V_8

C484 C493 C58 C27 — *330u/2V_7343 *330u/2V_7343 *330u/2V_7343 *330u/2V_7343

U22C

A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC[001] VCC[002] VCC[003] VCC[004] VCC[005] VCC[006] VCC[007] VCC[008] VCC[009] VCC[010] VCC[011] VCC[012] VCC[013] VCC[014] VCC[015] VCC[016] VCC[017] VCC[018] VCC[019] VCC[020] VCC[021] VCC[022] VCC[023] VCC[024] VCC[025] VCC[026] VCC[027] VCC[028] VCC[029] VCC[030] VCC[031] VCC[032] VCC[033] VCC[034] VCC[035] VCC[036] VCC[037] VCC[038] VCC[039] VCC[040] VCC[041] VCC[042] VCC[043] VCC[044] VCC[045] VCC[046] VCC[047] VCC[048] VCC[049] VCC[050] VCC[051] VCC[052] VCC[053] VCC[054] VCC[055] VCC[056] VCC[057] VCC[058] VCC[059] VCC[060] VCC[061] VCC[062] VCC[063] VCC[064] VCC[065] VCC[066] VCC[067]

VCC[068] VCC[069] VCC[070] VCC[071] VCC[072] VCC[073] VCC[074] VCC[075] VCC[076] VCC[077] VCC[078] VCC[079] VCC[080] VCC[081] VCC[082] VCC[083] VCC[084] VCC[085] VCC[086] VCC[087] VCC[088] VCC[089] VCC[090] VCC[091] VCC[092] VCC[093] VCC[094] VCC[095] VCC[096] VCC[097] VCC[098] VCC[099] VCC[100]

VCCP[01] VCCP[02] VCCP[03] VCCP[04] VCCP[05] VCCP[06] VCCP[07] VCCP[08] VCCP[09] VCCP[10] VCCP[11] VCCP[12] VCCP[13] VCCP[14] VCCP[15] VCCP[16]

VCCA[01] VCCA[02]

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]

VCCSENSE

VSSSENSE

Penryn

VCC_CORE

AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

B26 C26

AD6 AF5 AE5 AF4 AE3 AF3 AE2

H_VID0 [35] H_VID1 [35] H_VID2 [35] H_VID3 [35] H_VID4 [35] H_VID5 [35] H_VID6 [35]

AF7

AE7

VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)

+1.05V

C57 C56 C54 C500 — .1u/16V_6 .1u/16V_6 .1u/16V_6 330u/2V_7343

C67 C486 C485 — *.1u/16V_6 .1u/16V_6 .1u/16V_6

VCCA:130mA

+1.5V

C69 C68 — .01u/25V_4 10u/6.3V_8

R371 100/F_6 VCC_CORE

VCCSENSE [35]

VSSSENSE [35]

R372 100/F_6

Layout Note:
Z0=27.4,PU/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

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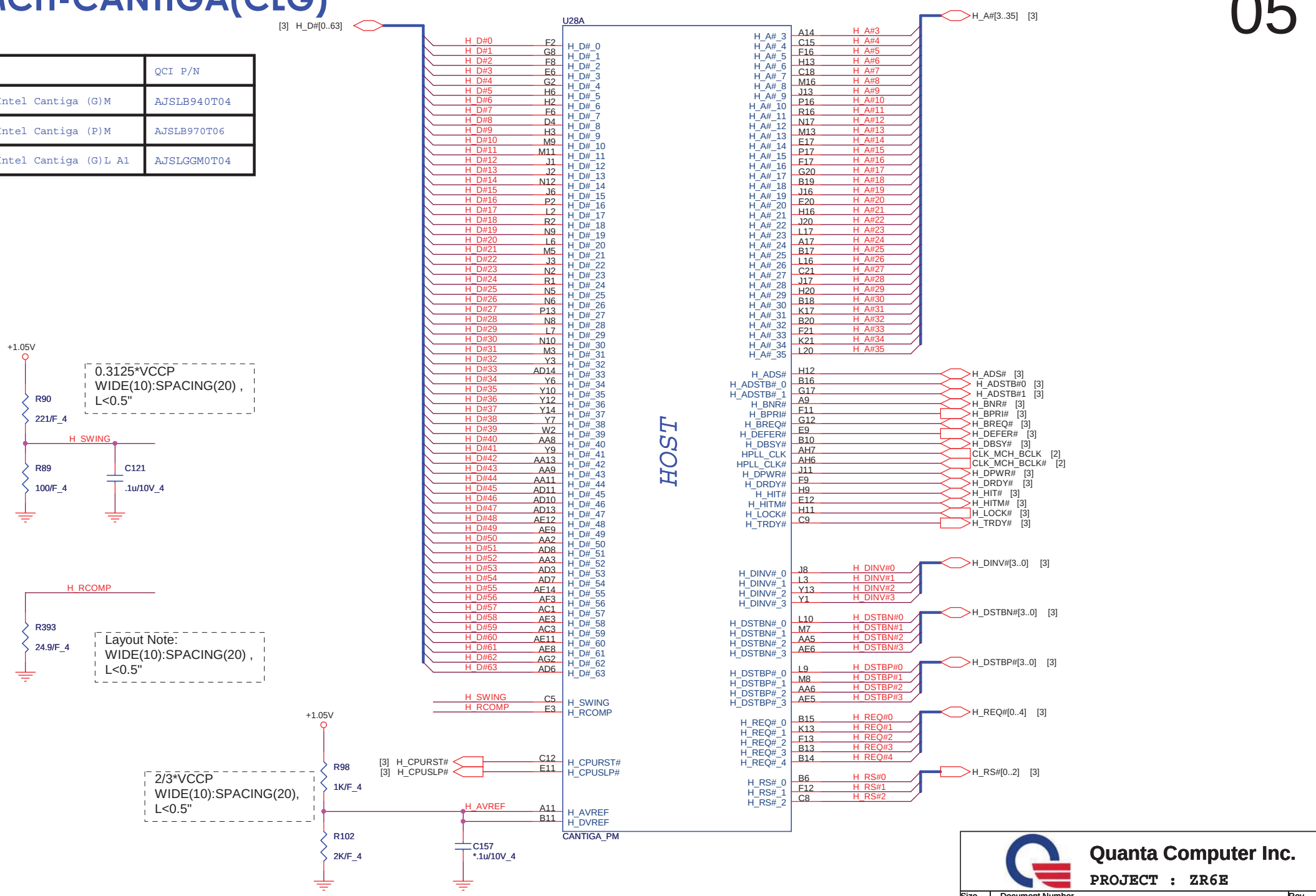
PROJECT : ZR6E

Size	Document Number	Rev
	CPU Power	1A
Date: Tuesday, May 19, 2009	Sheet 4 of 39	

GMCH-CANTIGA(CLG)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



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PROJECT : ZR6E

Size	Document Number	Rev
	GMCH HOST	1A
Date: Tuesday, May 19, 2009	Sheet 5 of 39	

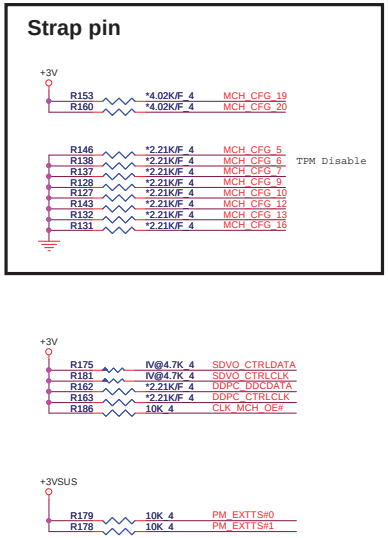
GMCH-CANTIGA(CLG)

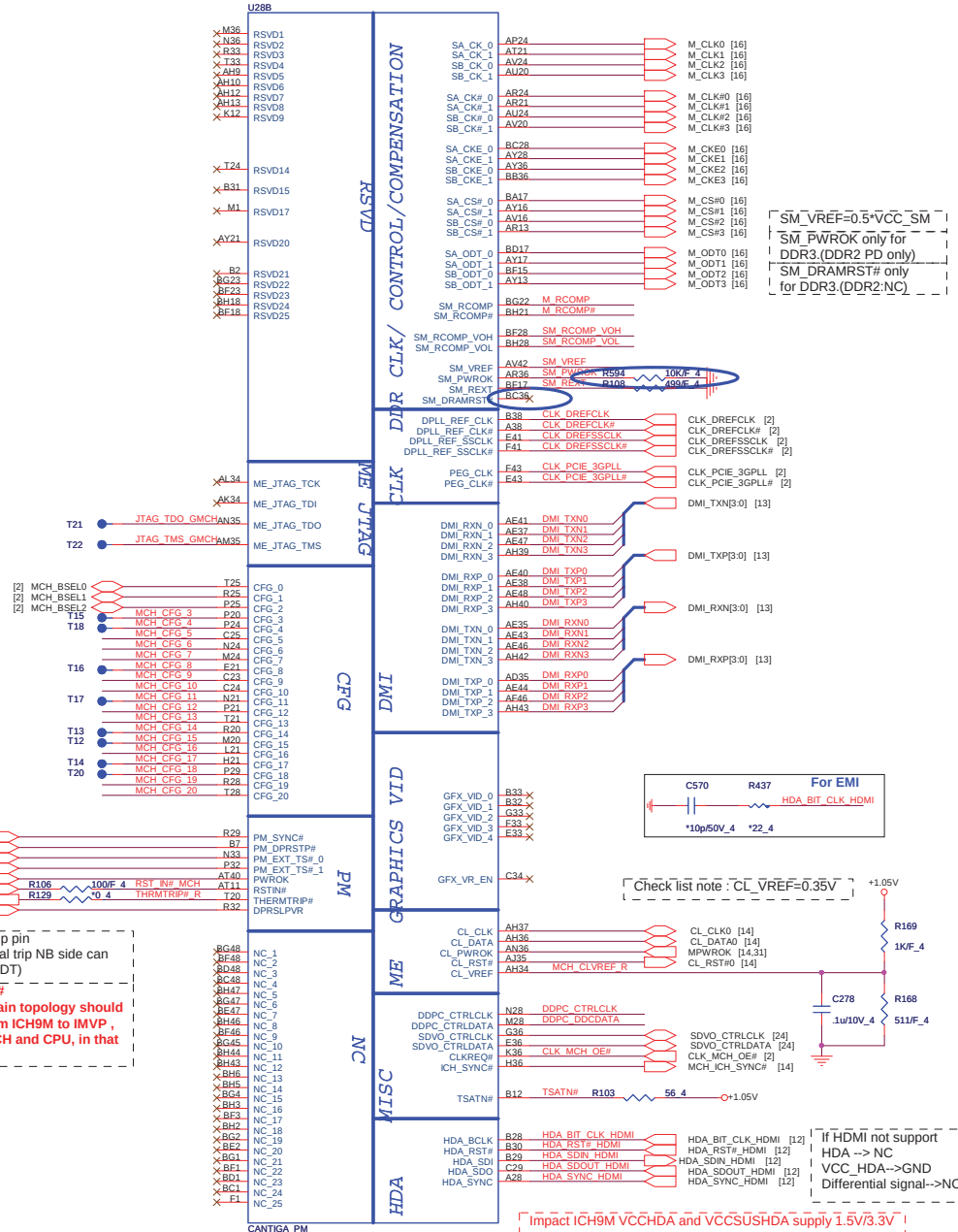
IV@
EV@

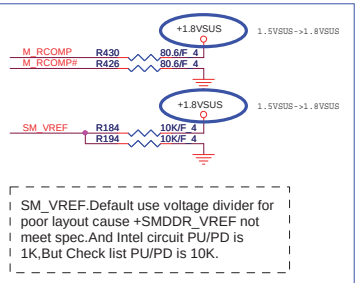
Strap table

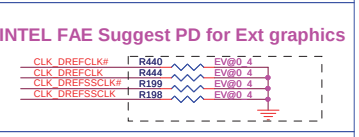
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

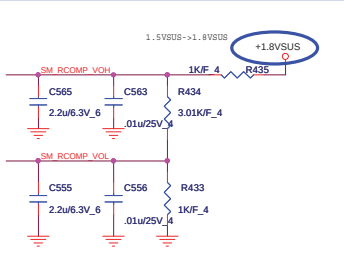
Strap pin

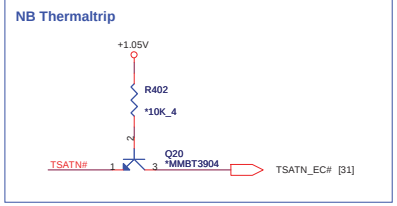












DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

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PROJECT : ZR6E
Size | Document Number: GMCH DMI | Rev: 1A
Date: Tuesday, May 19, 2009 | Sheet 6 of 39

GMCH-CANTIGA(CLG)

07

IV@
EV@
SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U28C

[24] L_BKLT_CTRL
[24] INT_LVDS_BLON
R171 IV@10K_4 L_CTRL_CLK
+3V
R172 IV@10K_4 L_CTRL_DATA
[24] INT_LVDS_EDIDCLK
[24] INT_LVDS_EDIDDATA
[24] INT_LVDS_DIGON
R195 IV@2.4K/F_4 LVDS_IBG
[24] INT_TXLCLKOUT-
[24] INT_TXLCLKOUT+
[24] INT_TXLOUT0-
[24] INT_TXLOUT1-
[24] INT_TXLOUT2-
[24] INT_TXLOUT0+
[24] INT_TXLOUT1+
[24] INT_TXLOUT2+

L32 L_BKLT_CTRL
G32 L_BKLT_EN
M32 L_CTRL_CLK
M33 L_CTRL_DATA
K33 L_DDC_CLK
J33 L_DDC_DATA
M29 L_VDD_EN
C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
C41 LVDSA_CLK#
C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK
H47 LVDSA_DATA#_0
E46 LVDSA_DATA#_1
G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
H48 LVDSA_DATA_0
D45 LVDSA_DATA_1
F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

SDVT

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm

R147 SP@75_4 INT_TV_COMP F25
R136 SP@75_4 INT_TV_Y/G H25
R151 SP@75_4 INT_TV_C/R K25
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TVA_DAC
TVB_DAC
TVC_DAC

[24] INT_CRT_BLU INT_CRT_BLU E28 CRT_BLUE
[24] INT_CRT_GRN INT_CRT_GRN G28 CRT_GREEN
[24] INT_CRT_RED INT_CRT_RED J28 CRT_RED
G29 CRT_IRTN
H32 CRT_DDC_CLK
J32 CRT_DDC_DATA
J29 CRT_HSYNC
E29 CRT_TVO_IREF
L29 CRT_VSYNC

[24] INT_CRT_DDCCLK
[24] INT_CRT_DDCDAT
[24] INT_HSYNC
R158 IV@30.1_4 HSYNC_G
CRTIREF
[24] INT_VSYNC
R165 IV@30.1_4 VSYNC_G

HSYNC/VSYNC serial R place close to NB

Discrete Stuffed. (CRT)

HSYNC_G
VSYNC_G
R159 EV@0_4
R166 EV@0_4

CRTIREF pull down
for IV cantiga 1.02k ohm/F

CANTIGA_PM

PCI-EXPRESS GRAPHICS

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V
T37 EXP_A_COMPX R176 49.9/F_4
T36
PEG_COMPI
PEG_COMPO

PEG_RXN[15:0] [18]

PEG_RX#_0	H44	PEG_RXN0
PEG_RX#_1	J46	PEG_RXN1
PEG_RX#_2	L44	PEG_RXN2
PEG_RX#_3	L40	PEG_RXN3
PEG_RX#_4	N41	PEG_RXN4
PEG_RX#_5	P48	PEG_RXN5
PEG_RX#_6	N44	PEG_RXN6
PEG_RX#_7	T43	PEG_RXN7
PEG_RX#_8	U43	PEG_RXN8
PEG_RX#_9	Y43	PEG_RXN9
PEG_RX#_10	Y48	PEG_RXN10
PEG_RX#_11	Y36	PEG_RXN11
PEG_RX#_12	AA43	PEG_RXN12
PEG_RX#_13	AD37	PEG_RXN13
PEG_RX#_14	AC47	PEG_RXN14
PEG_RX#_15	AD39	PEG_RXN15

PEG_RXP[15:0] [18,24]

PEG_RX_0	H43	PEG_RXP0
PEG_RX_1	J44	PEG_RXP1
PEG_RX_2	L43	PEG_RXP2
PEG_RX_3	L41	PEG_RXP3
PEG_RX_4	N40	PEG_RXP4
PEG_RX_5	P47	PEG_RXP5
PEG_RX_6	N43	PEG_RXP6
PEG_RX_7	T42	PEG_RXP7
PEG_RX_8	U42	PEG_RXP8
PEG_RX_9	Y42	PEG_RXP9
PEG_RX_10	W47	PEG_RXP10
PEG_RX_11	Y37	PEG_RXP11
PEG_RX_12	AA42	PEG_RXP12
PEG_RX_13	AD36	PEG_RXP13
PEG_RX_14	AC48	PEG_RXP14
PEG_RX_15	AD40	PEG_RXP15

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_TXN[15:0] [18,24]

PEG_TX#_0	J41	C_PEG_TXN0	C583	.1u/10V_4 PEG_TXN0
PEG_TX#_1	M46	C_PEG_TXN1	C587	.1u/10V_4 PEG_TXN1
PEG_TX#_2	M47	C_PEG_TXN2	C591	.1u/10V_4 PEG_TXN2
PEG_TX#_3	M40	C_PEG_TXN3	C596	.1u/10V_4 PEG_TXN3
PEG_TX#_4	M42	C_PEG_TXN4	C618	EV@.1U/10V_4 PEG_TXN4
PEG_TX#_5	R48	C_PEG_TXN5	C588	EV@.1U/10V_4 PEG_TXN5
PEG_TX#_6	N38	C_PEG_TXN6	C600	EV@.1U/10V_4 PEG_TXN6
PEG_TX#_7	T40	C_PEG_TXN7	C598	EV@.1U/10V_4 PEG_TXN7
PEG_TX#_8	U37	C_PEG_TXN8	C604	EV@.1U/10V_4 PEG_TXN8
PEG_TX#_9	U40	C_PEG_TXN9	C603	EV@.1U/10V_4 PEG_TXN9
PEG_TX#_10	Y40	C_PEG_TXN10	C608	EV@.1U/10V_4 PEG_TXN10
PEG_TX#_11	AA46	C_PEG_TXN11	C594	EV@.1U/10V_4 PEG_TXN11
PEG_TX#_12	AA37	C_PEG_TXN12	C616	EV@.1U/10V_4 PEG_TXN12
PEG_TX#_13	AA40	C_PEG_TXN13	C619	EV@.1U/10V_4 PEG_TXN13
PEG_TX#_14	AD43	C_PEG_TXN14	C614	EV@.1U/10V_4 PEG_TXN14
PEG_TX#_15	AC46	C_PEG_TXN15	C593	EV@.1U/10V_4 PEG_TXN15

PEG_TXP[15:0] [18,24]

PEG_TX_0	J42	C_PEG_TXP0	C580	.1u/10V_4 PEG_TXP0
PEG_TX_1	L46	C_PEG_TXP1	C585	.1u/10V_4 PEG_TXP1
PEG_TX_2	M48	C_PEG_TXP2	C590	.1u/10V_4 PEG_TXP2
PEG_TX_3	M39	C_PEG_TXP3	C597	.1u/10V_4 PEG_TXP3
PEG_TX_4	M43	C_PEG_TXP4	C611	EV@.1U/10V_4 PEG_TXP4
PEG_TX_5	R47	C_PEG_TXP5	C586	EV@.1U/10V_4 PEG_TXP5
PEG_TX_6	N37	C_PEG_TXP6	C601	EV@.1U/10V_4 PEG_TXP6
PEG_TX_7	T39	C_PEG_TXP7	C599	EV@.1U/10V_4 PEG_TXP7
PEG_TX_8	U36	C_PEG_TXP8	C605	EV@.1U/10V_4 PEG_TXP8
PEG_TX_9	U39	C_PEG_TXP9	C602	EV@.1U/10V_4 PEG_TXP9
PEG_TX_10	Y39	C_PEG_TXP10	C609	EV@.1U/10V_4 PEG_TXP10
PEG_TX_11	Y46	C_PEG_TXP11	C595	EV@.1U/10V_4 PEG_TXP11
PEG_TX_12	AA36	C_PEG_TXP12	C617	EV@.1U/10V_4 PEG_TXP12
PEG_TX_13	AA39	C_PEG_TXP13	C620	EV@.1U/10V_4 PEG_TXP13
PEG_TX_14	AD42	C_PEG_TXP14	C615	EV@.1U/10V_4 PEG_TXP14
PEG_TX_15	AD46	C_PEG_TXP15	C592	EV@.1U/10V_4 PEG_TXP15

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm

R161 SP@1K/F_4 CRTIREF

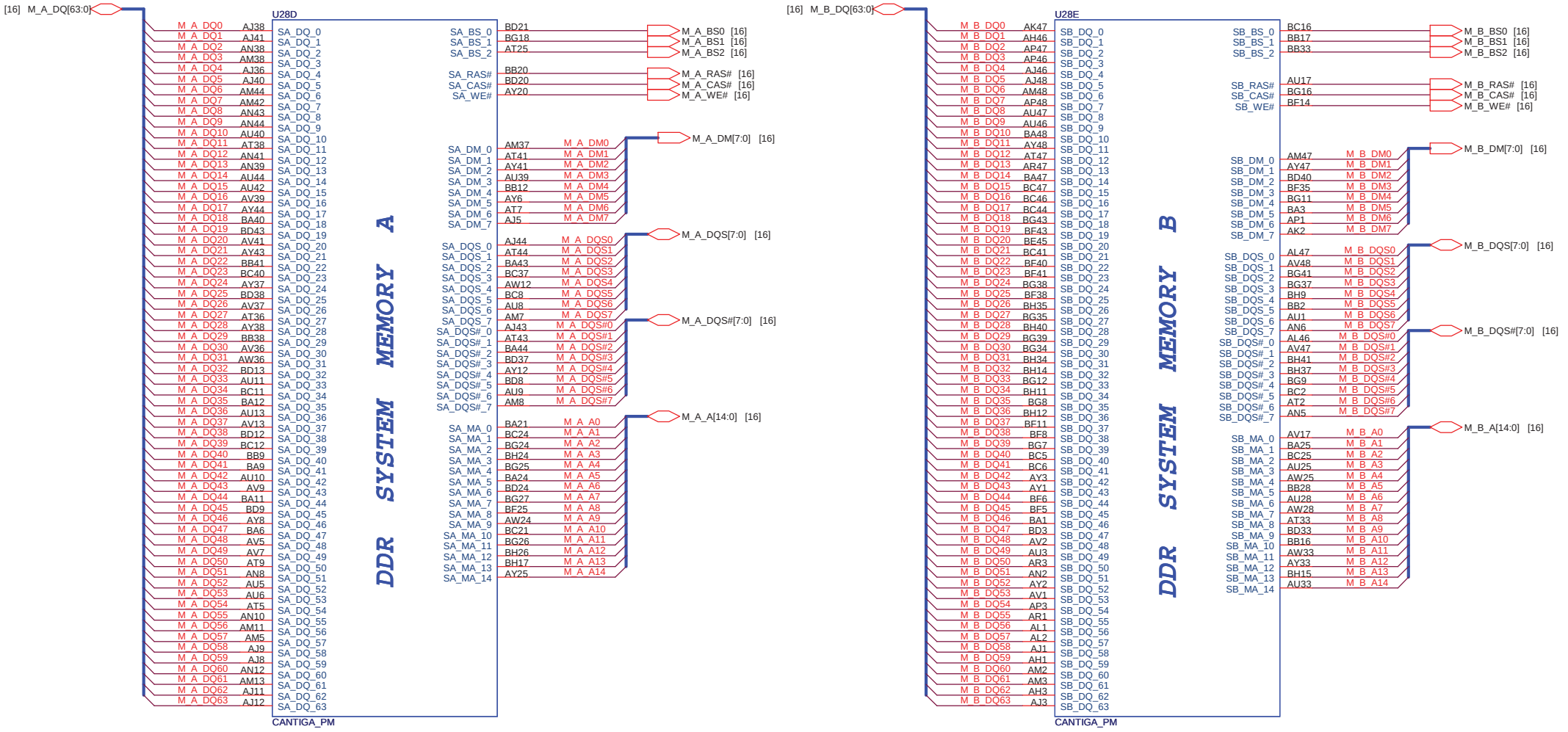
SP@ CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R155 SP@150/F_4 INT_CRT_BLU
R154 SP@150/F_4 INT_CRT_GRN
R150 SP@150/F_4 INT_CRT_RED

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VGA	1A
Date: Tuesday, May 19, 2009	Sheet 7 of 39	

GMCH-CANTIGA(CLG)



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	GMCH DDRII	1A
Date: Tuesday, May 19, 2009	Sheet 8 of 39	

GMCH-CANTIGA(CLG)

IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

+1.8VSUS

+1.5VSUS to +1.8VSUS

C606 22u/6.3V_8 | C612 *22u/6.3V_8 | C264 .1u/10V_4 | C624 330u/2V_7343

VCC_SM(1.8V) DDR2

U28G

VCC_SM_1 … VCC_SM_42 — POWER — VCC SM

VCC_SM_36/NC … VCC_SM_42/NC

+1.05V_AXG

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60 — VCC GFX NCTF

VCC_AXG_1 … VCC_AXG_42 — VCC GFX

VCC_AXG_SENSE
VSS_AXG_SENSE

VCC_SM_LF1 … VCC_SM_LF7 — VCC SM LF

CANTIGA_PM

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

+1.05V_AXG

IV@ R112 IV@10/F_4 AJ14 | R110 IV@10/F_4 AH14

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

1.8V
Internal connect to power

C163 .1u/10V_4 | C151 .1u/10V_4 | C142 .22u/6.3V_4 | C211 .22u/6.3V_4 | C292 .47u/6.3V_4 | C290 1u/10V_4 | C319 1u/10V_4

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+1.05V

C267 .1u/10V_4 | C283 *.22u/6.3V_4 | C266 .22u/6.3V_4 | C286 22u/6.3V_8 | C610 330u/2V_7343

Place close to the GMCH

U28F

VCC_1 … VCC_35 — VCC CORE

CANTIGA_PM

+1.05V

IV@ R156 IV@0_8 | R83 IV@0_8 | R80 IV@0_8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG

+C505 IV@330u/2V_7343 | +C501 IV@330u/2V_7343 | C219 IV@.47u/6.3V_4 | SP@ C168 SP@1u/10V_6 | C149 IV@10u/6.3V_8 | C187 IV@22u/6.3V_8 | C223 IV@.1u/10V_4 | C107 IV@.1u/10V_4 | C166 IV@.1u/10V_4

Place close to the GMCH

SP@IV Sutff 1uf
EVstuff 0 ohm

Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

+1.05V

VCC_NCTF_1 … VCC_NCTF_44 — VCC NCTF

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev1.0 Section 10.2 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.
PROJECT : ZR6E
Size | Document Number: GMCH VCC,NCTF | Rev 1A
Date: Tuesday, May 19, 2009 | Sheet 9 of 39

GMCH-CANTIGA(CLG)

Power consumption reference to Intel Cantiga_chipset EDS Volume1. Section 10

IV@
EV@
SP@

If CRT have Flicker issue
STUFF 5.6 ohm

IV&EV Dis/Enable setting

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

1210 10UH, 10%
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL_A/B

3.3V
73mA

3.3V
5mA

USE same GND plane

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

1.8V
13.2mA

1.5V
414uA

1.05V
24mA

1.05V
139.2mA

1.05V
DDR2-800
720mA

1.05V
50mA

3.9 nH, 0.2 nH, 1A
DCR_max=32 m

VCCA_PEG_PLL
+1.25V for Teenah use(100mA)

1210 0.1uH, 20%, 1A,
DCR_max=0.078Ω

1.05V
DDR2-800
26mA

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

CRB : 0 ohm
Check list : 2.2nH

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

3.3V
79mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V
50mA

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
35mA

VCCD_QDAC share to TV and CRT

1.5V
48.363mA for CRT
5mA for TV

1.5V
157.2mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

1.5V
0.5mA

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

MODIFY

FB 220 @100 MHz, 25%, 2A

1.05V
50mA

ESR=60m ohm

1.05V
321.35mA

1.8V
DDR2-800
124mA

0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA

1.8V
118.8mA

3.3V
105.3mA

1.05V
1782mA

1.05V
456mA

1.05V
Internal connect to power

1.8V
60.31mA

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

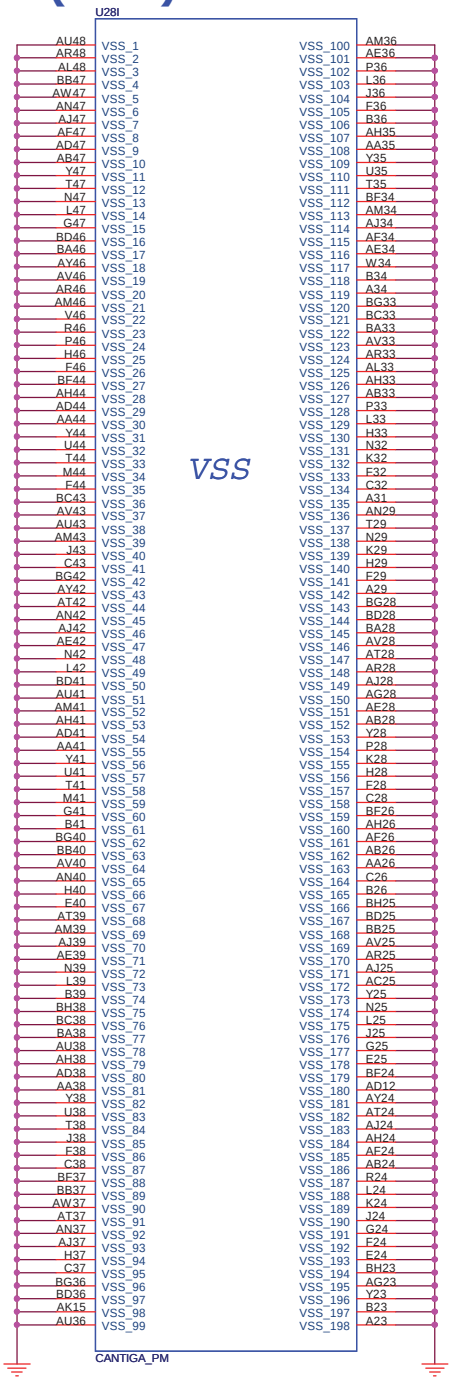
Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_#	1.05V
VCCD_PEG_PLL	1.05V

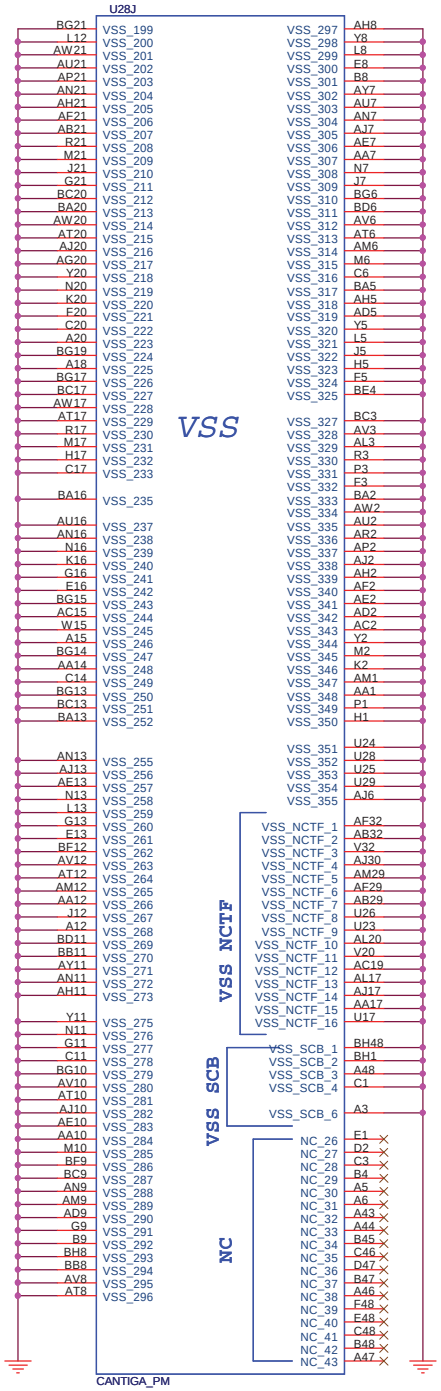
Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH POWER	1A

Date: Tuesday, May 19, 2009 Sheet 10 of 39

GMCH-CANTIGA(CLG)





Quanta Computer Inc.

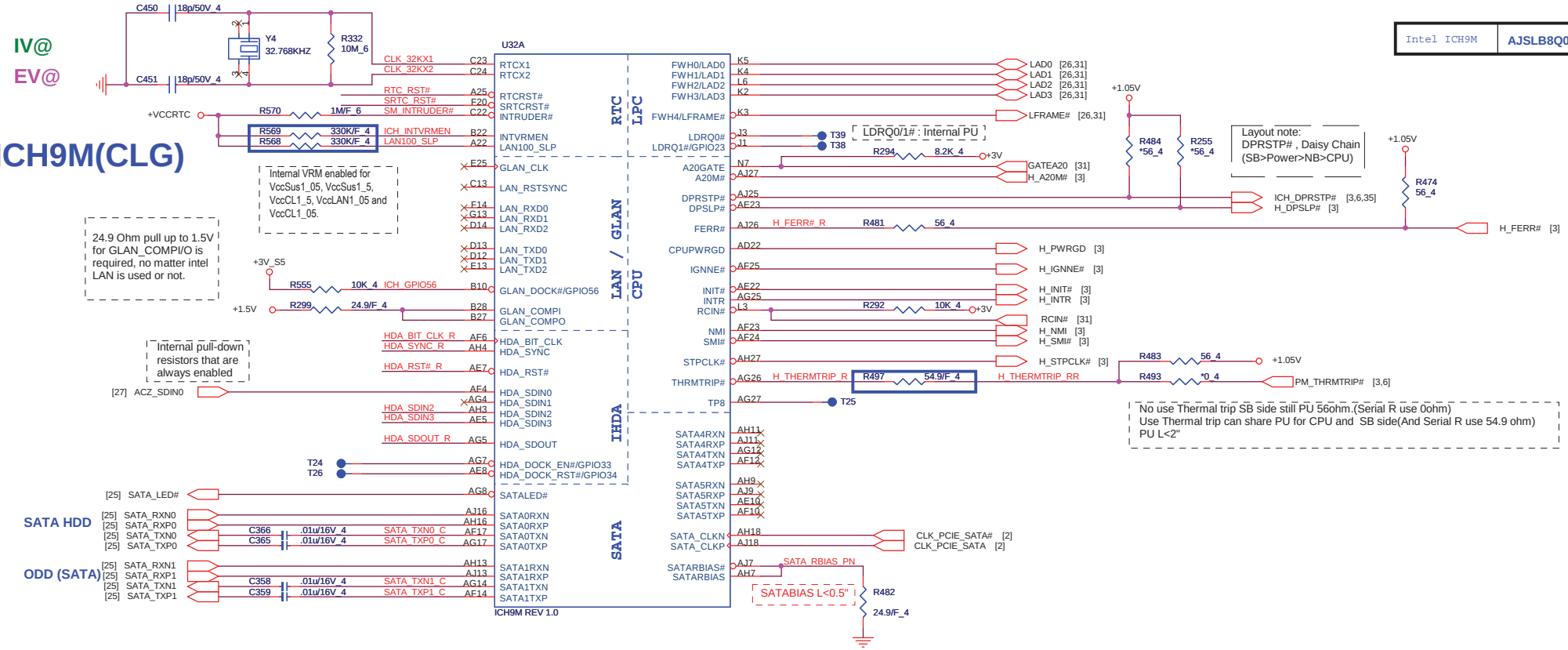
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VSS	1A
Date: Tuesday, May 19, 2009	Sheet 11 of 39	

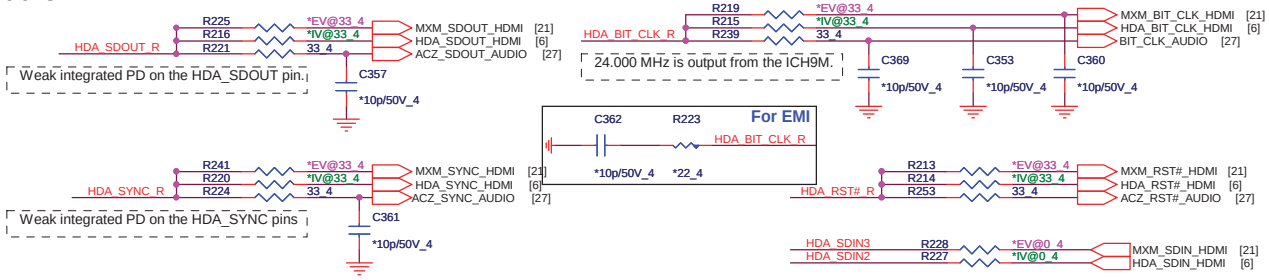
Intel ICH9M	AJSLB8Q0T03

IV@
EV@

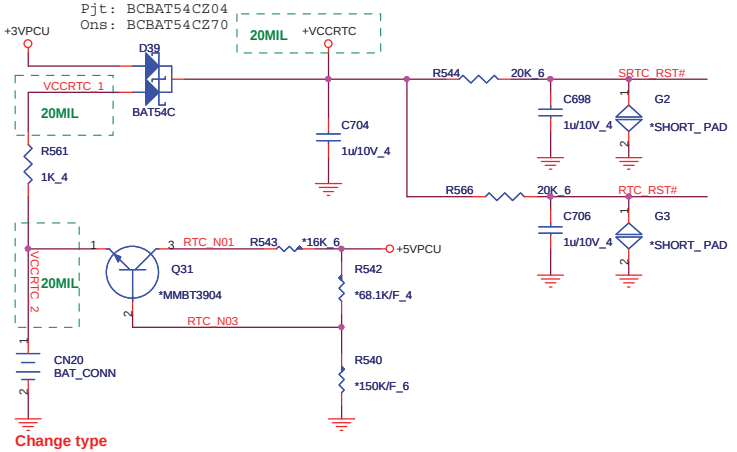
ICH9M(CLG)



HD Audio



RTC

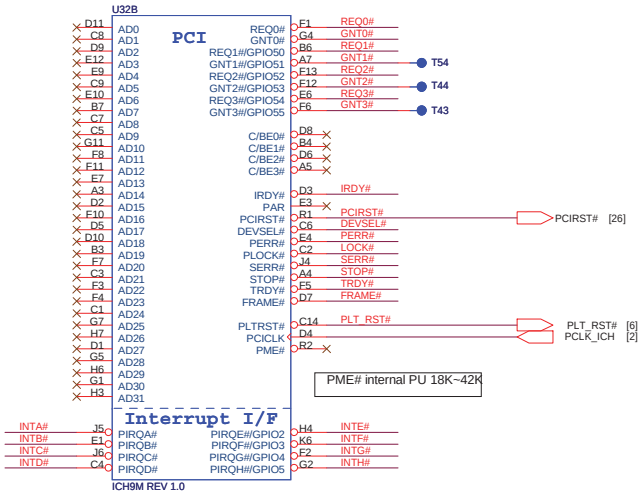


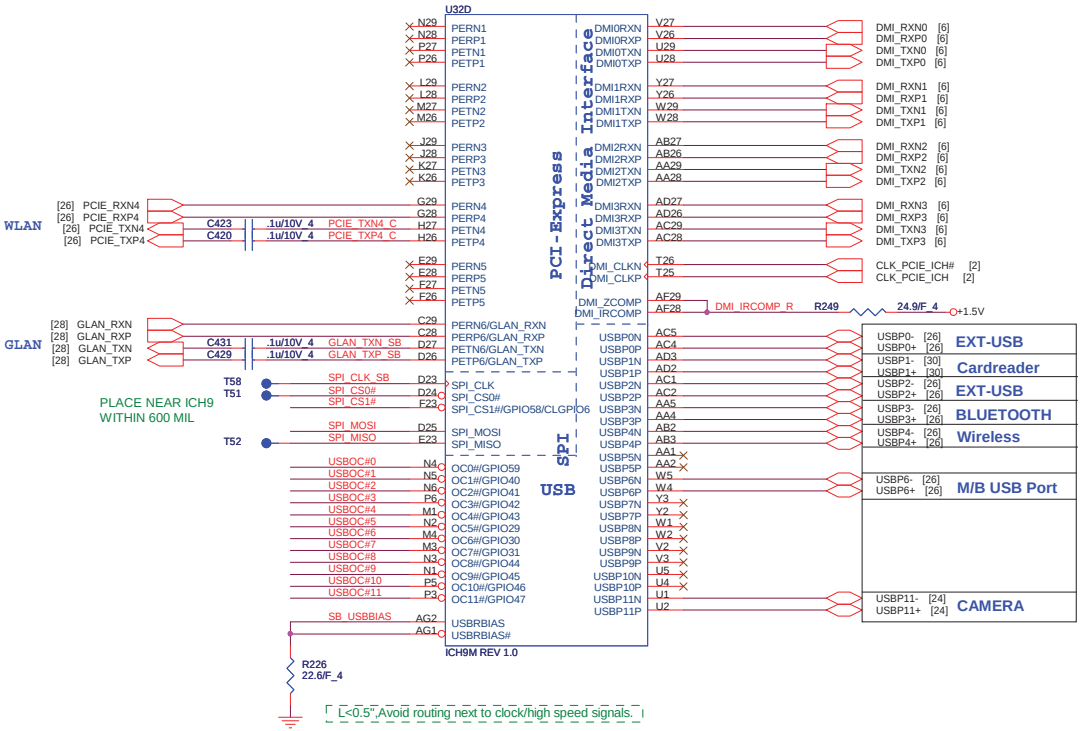
South Bridge Strap Pin (1/3)

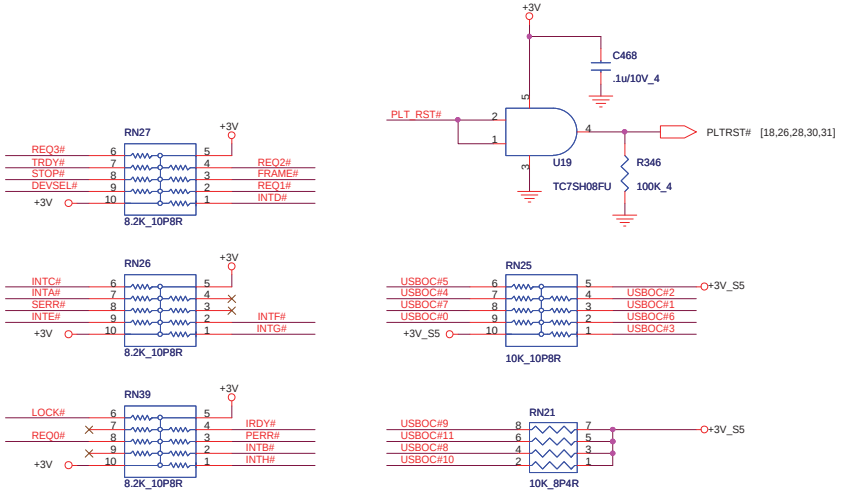
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	[14] ICH_TP3 — ICH_TP3 — R545 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R240 *1K_4 — +3V

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	ICH9M HOST	1A
Date: Tuesday, May 19, 2009	Sheet 12 of 39	







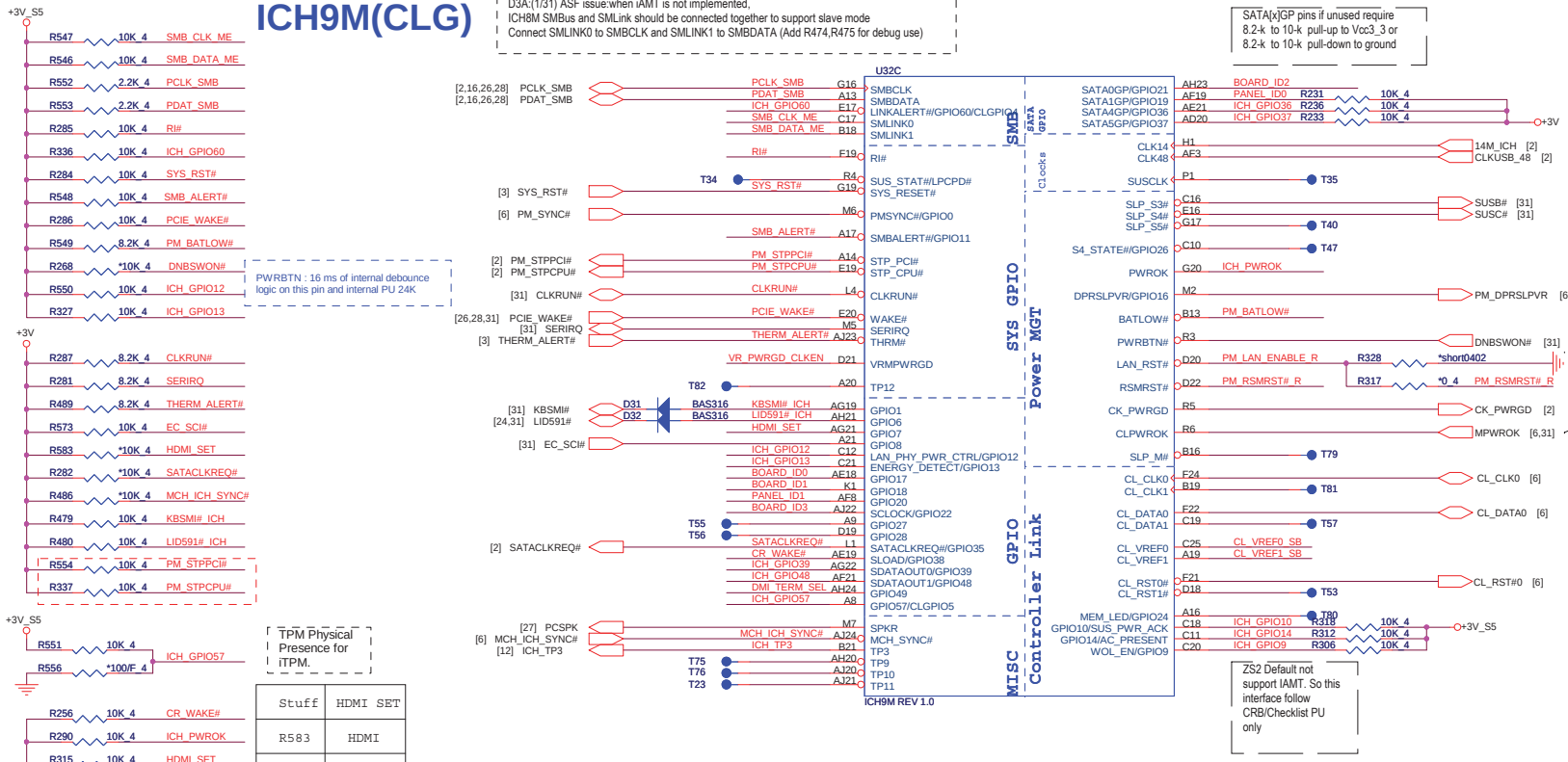
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R309 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R277 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R293 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R274 *1K_4

ICH9M(CLG)

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground



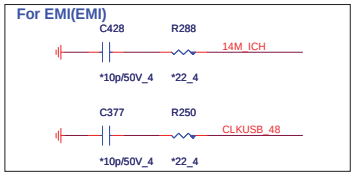
PWRBTN : 16 ms of internal debounce logic on this pin and internal PU 24K

TPM Physical Presence for iTPM.

Stuff	HDMI SET
R583	HDMI
R315	No HDMI

ZS2 Default not support IAMT. So this interface follow CRB/Checklist PU only

For EMI(EMI)



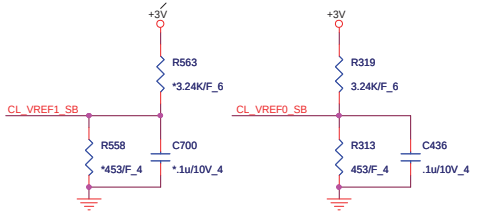
<Checklist ver0.8>
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no IAMT

CL VREF

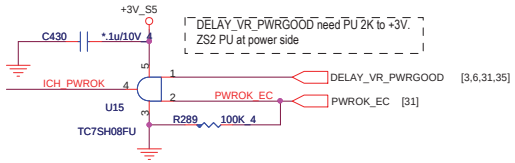
VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

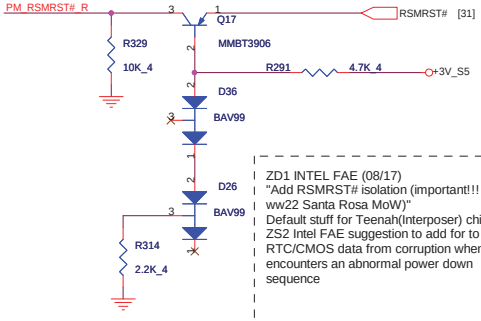


Follow CHECK LIST V1.5

ICH PWROK



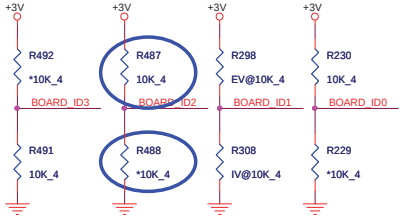
Resume RST



ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

ID0=0 -->ZK6 ,ID0=1 -->ZR6
ID1=0 -->UMA ,ID1=1 -->Discrete

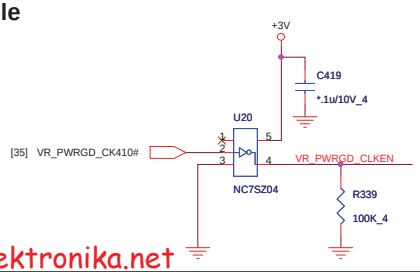


Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R271 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R485 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZR6E
Size | Document Number | ICH9M GPIO | Rev 1A
Date: Tuesday, May 19, 2009 | Sheet 14 of 39

ICH9M(CLG)

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

2~3.456v 3.6uA_G3

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

MODIFY

MODIFY

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

1.05V , Powered by VCC1_05 in S0

If use SB MAC for LAN function. And support wake up need connect to relation power.

If use SB MAC for LAN function. And support wake up need connect to relation power.

ICH9M REV 1.0

ICH9M REV 1.0

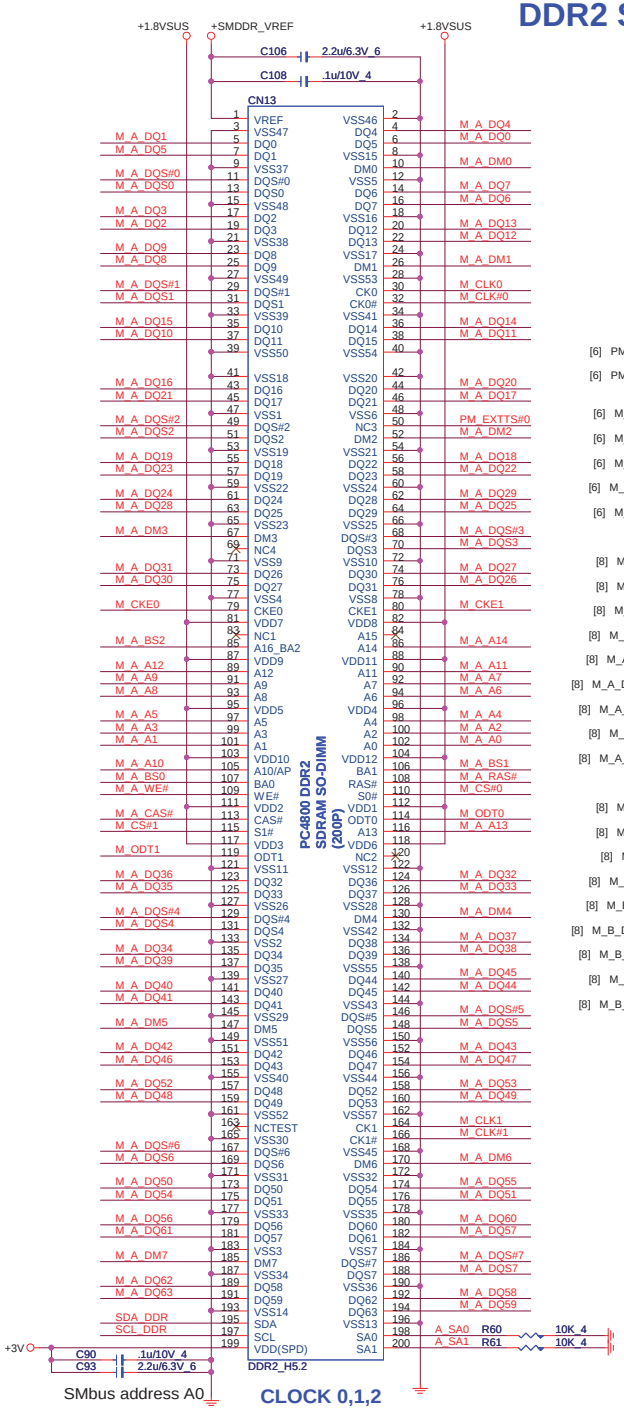
Quanta Computer Inc.

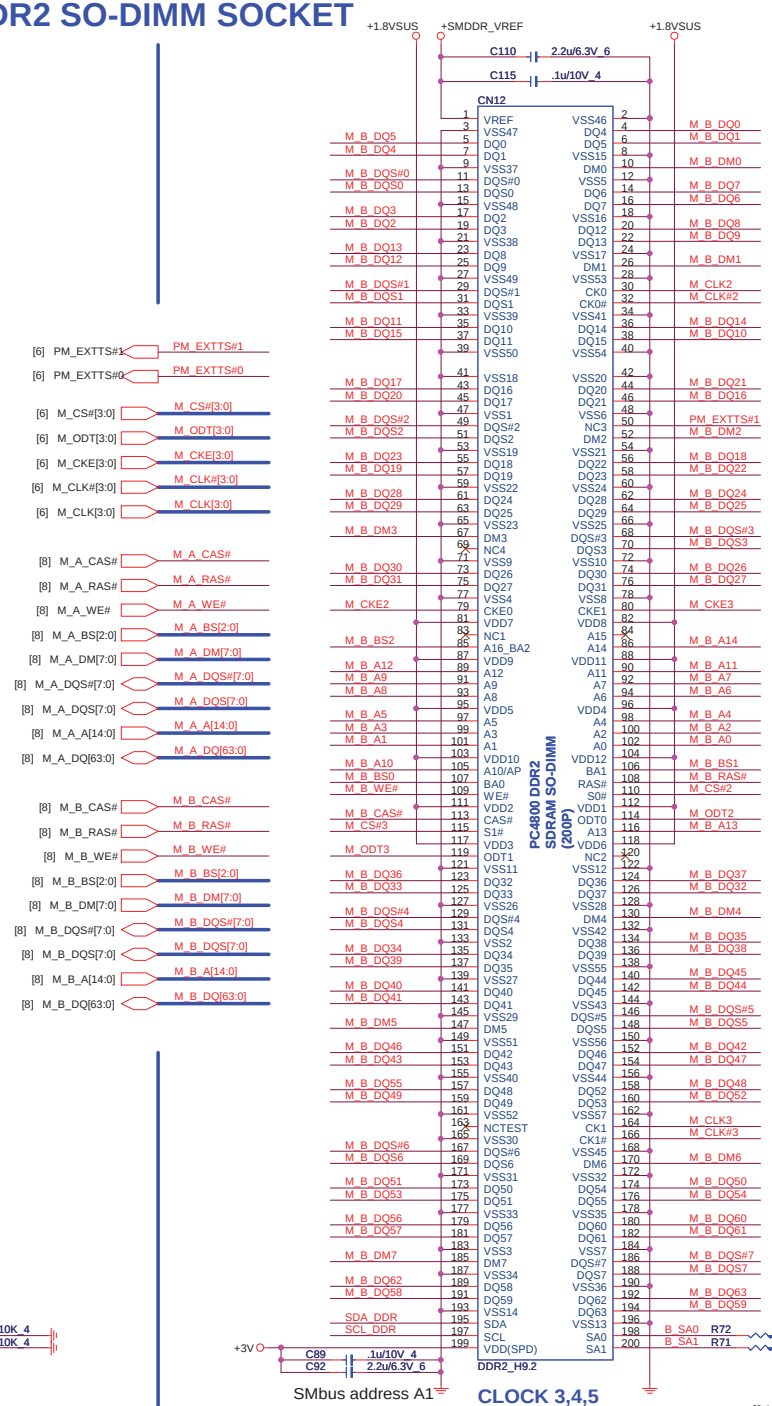
PROJECT : ZR6E

Size	Document Number	Rev
	ICH9 POWER	1A

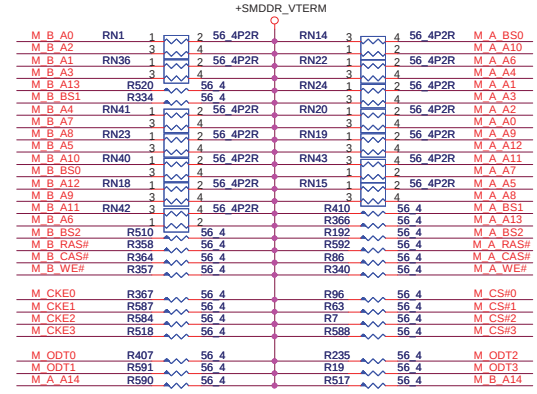
Date: Tuesday, May 19, 2009 Sheet 15 of 39

DDR2 SO-DIMM SOCKET

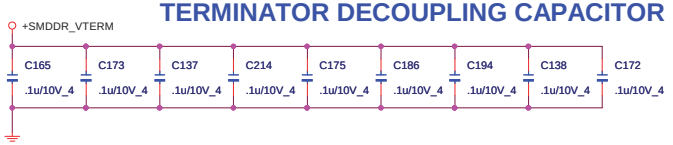




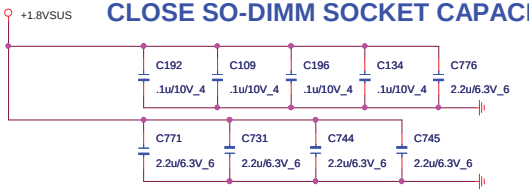
DDR2 TERMINATOR



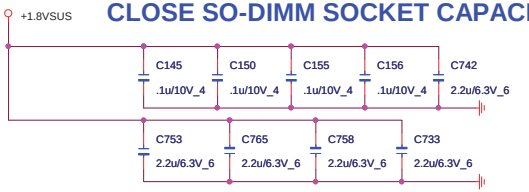
TERMINATOR DECOUPLING CAPACITOR

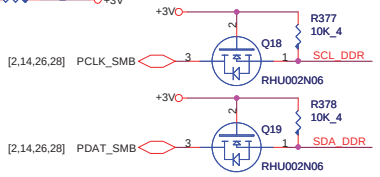


CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS





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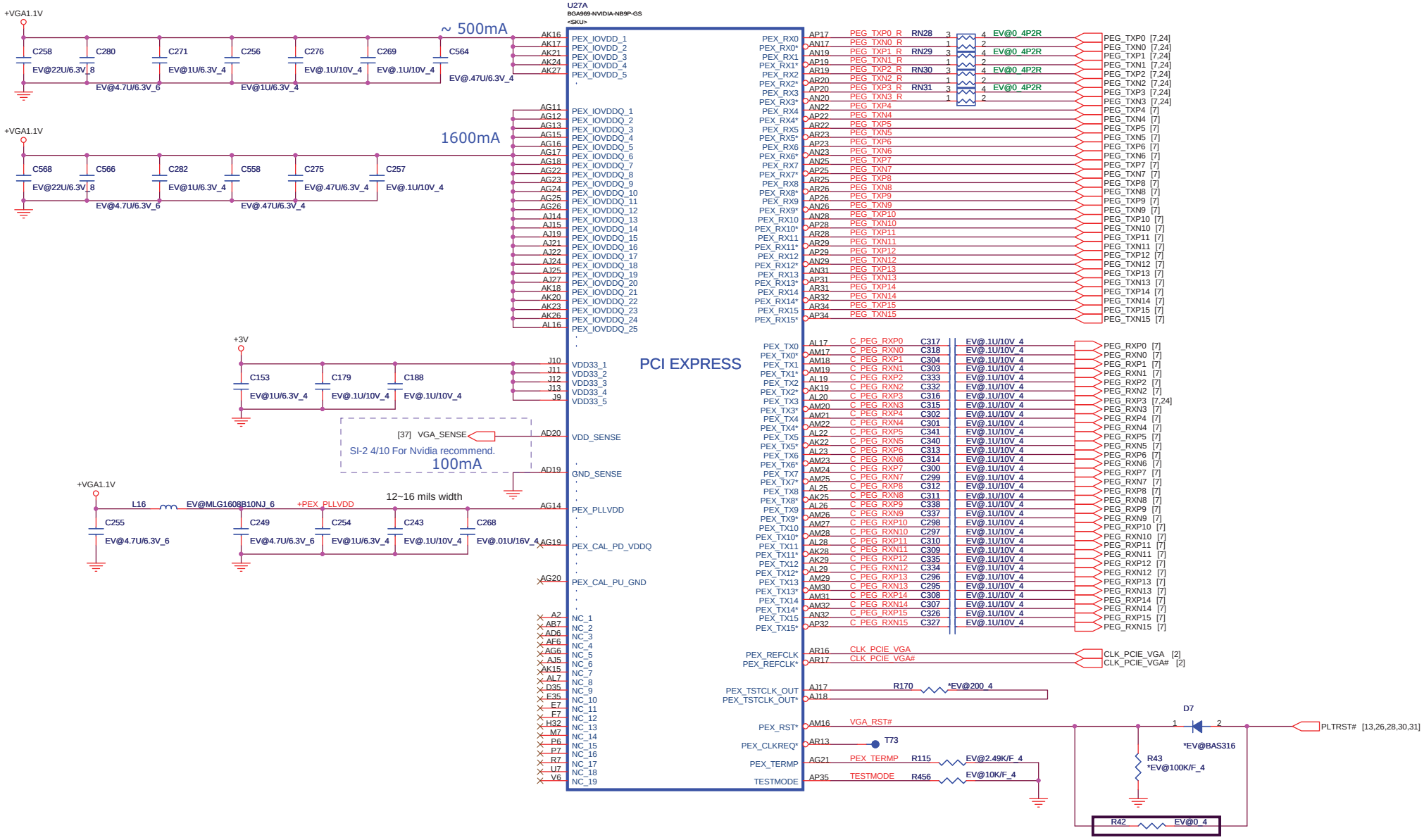
PROJECT : ZR6E

Size	Document Number	Rev
	DDRII SO-DIMM	1A

Date: Tuesday, May 19, 2009 Sheet 16 of 39

NV10M (VGA)



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X (PCIE I/F) 1/5	1A

Date: Tuesday, May 19, 2009 Sheet 17 of 39

NV10M (VGA)

U27B

BGA969-NVIDIA-NB9P-GS
<SKU>

MEMORY I/F A

U27C

BGA969-NVIDIA-NB9P-GS
<SKU>

MEMORY I/F B

Add for 64x16 vram

for DDR2 need use
CMD11(CKE) and
CMD12(ODT)

use internal Vref, ext
divider no stuff

15mils width

For Debug only

R91 Install for DDR3

R86 no stuff

G96 only

Quanta Computer Inc.	
PROJECT : ZR6E	
Size	Document Number: NV10X (MEMORY I/F) 2/5
Rev	1A
Date: Tuesday, May 19, 2009	Sheet 18 of 39

NV10M (VGA)

U27D
BGA969-NVIDIA-N89P-GS
<SKU>

IFPAB(LVDS)

100 mA
50 mA
50 mA

+1.8V
L41 EV@HCB1608KF-181T15_6 +IFPAB_PLLVDD AK9
C578 EV@4.7U/6.3V_6 C575 EV@4700P/25V_4 C279 EV@470P/50V_4
R173 *EV@1K/F_4 AJ11 IFPAB_RSET
L14 EV@HCB1608KF-181T15_6 +IFPAB_IOVDD AG9 AG10
C247 EV@4.7U/6.3V_6 C246 EV@4.7U/6.3V_6 C251 EV@4700P/25V_4 C265 EV@4700P/25V_4 C250 EV@470P/50V_4 C259 EV@470P/50V_4

IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD

IFPA_TXC+ AM11 → EV_TXLCLKOUT+ [24]
IFPA_TXC- AM12 → EV_TXLCLKOUT- [24]
IFPA_TXD0+ AM8 → EV_TXLOUT0+ [24]
IFPA_TXD0- AL8 → EV_TXLOUT0- [24]
IFPA_TXD1+ AM10 → EV_TXLOUT1+ [24]
IFPA_TXD1- AM9 → EV_TXLOUT1- [24]
IFPA_TXD2+ AK10 → EV_TXLOUT2+ [24]
IFPA_TXD2- AL10 → EV_TXLOUT2- [24]
IFPA_TXD3+ AK11
IFPA_TXD3- AL11
IFPB_TXC+ AP13
IFPB_TXC- AN13
IFPB_TXD0+ AN8
IFPB_TXD0- AP8
IFPB_TXD1+ AP10
IFPB_TXD1- AN10
IFPB_TXD2+ AR11
IFPB_TXD2- AR10
IFPB_TXD3+ AN11
IFPB_TXD3- AP11

IFPCD

+1.8V
L40 EV@HCB1608KF-181T15_6 +IFPCD_PLLVDD AJ9
C132 EV@1U/6.3V_4 C572 EV@4.7U/6.3V_6 C260 EV@4700P/25V_4 C261 EV@470P/50V_4
R432 EV@1K/F_4 AK7 IFPCD_RSET
+VGA1.1V
L42 EV@HCB1608KF-181T15_6 +IFPCD_IOVDD AJ8 AK8
C579 EV@4.7U/6.3V_6 C581 EV@1U/6.3V_4 C576 EV@1U/6.3V_6 C584 EV@4700P/25V_4 C287 EV@470P/50V_4 C274 EV@470P/50V_4

IFPCD_PLLVDD
IFPCD_RSET
IFPC_IOVDD
IFPD_IOVDD

IFPC

AUX+ AP2
AUX- AR2
DPL3_TXC+ AP1
DPL3_TXC- AM4
DPL2_TXD0+ AM3
DPL2_TXD0- AM5
DPL1_TXD1+ AL5
DPL1_TXD1- AM6
DPL0_TXD2+ AM7
DPL0_TXD2- AN4

HDMI_CLK- R C293 EV@.1U/10V_4 → HDMI_CLK- [24]
HDMI_CLK+ R C294 EV@.1U/10V_4 → HDMI_CLK+ [24]
HDMI_TX0N R C305 EV@.1U/10V_4 → HDMI_TX0N [24]
HDMI_TX0P R C306 EV@.1U/10V_4 → HDMI_TX0P [24]
HDMI_TX1N R C323 EV@.1U/10V_4 → HDMI_TX1N [24]
HDMI_TX1P R C324 EV@.1U/10V_4 → HDMI_TX1P [24]
HDMI_TX2N R C322 EV@.1U/10V_4 → HDMI_TX2N [24]
HDMI_TX2P R C321 EV@.1U/10V_4 → HDMI_TX2P [24]

Fix Ball out and Pin Name

IFPD

AUX+ AN4
AUX- AP4
DPL3_TXC+ AR4
DPL3_TXC- AR5
DPL2_TXD0+ AP5
DPL2_TXD0- AN5
DPL1_TXD1+ AM7
DPL1_TXD1- AP7
DPL0_TXD2+ AR7
DPL0_TXD2- AR8

TMDS channel two

IFPEF

IFPEF_PLLVDD AJ6
R164 EV@10K/F_4 T72 AL1 IFPEF_RSET
IFPEF_IOVDD AE7
R425 EV@10K/F_4 AD7 IFPF_IOVDD

IFPE_AUX+ AE4
IFPE_AUX- AD4
IFPE_L0+ AH6
IFPE_L0- AH5
IFPE_L1+ AH4
IFPE_L1- AG4
IFPE_L2+ AF4
IFPE_L2- AF5
IFPE_L3+ AE6
IFPE_L3- AE5
IFPF_AUX+ AF3
IFPF_AUX- AE3
IFPF_L0+ AE2
IFPF_L0- AL2
IFPF_L1+ AL3
IFPF_L1- AJ3
IFPF_L2+ AJ2
IFPF_L2- AJ1
IFPF_L3+ AH1
IFPF_L3- AH2

Display port output

DACA(CRT)

+3V
L17 EV@HCB1608KF-181T15_6 +DACA_VDD AJ12
C285 EV@4.7U/6.3V_6 C270 EV@4700P/25V_4 C284 EV@470P/50V_4 C281 EV@.1U/10V_4 R454 EV@124/F_4
DACA_VREF AK12
DACA_RSET AK13

DACA_VDD
DACA_VREF
DACA_RSET

DACA_RED AM15 → EV_VGA_RED [24]
DACA_GREEN AM14 → EV_VGA_GRN [24]
DACA_BLUE AL14 → EV_VGA_BLU [24]
DACA_HSYNC AM13 — CRT_HSYNC R190 EV@33_4 → EV_HSYNC [24]
DACA_VSYNC AL13 — CRT_VSYNC R191 EV@33_4 → EV_VSYNC [24]
I2CA_SCL G1 → EV_CRTDCLK [24]
I2CA_SDA G4 → EV_CRTDDAT [24]

EV_VGA_RED R187 EV@150/F_4
EV_VGA_GRN R188 EV@150/F_4
EV_VGA_BLU R189 EV@150/F_4
Close to GPU

DACC(CRT2)

+DACB_VDD AG7
R431 EV@10K/F_4 T71 AK6 T70 AH7

DACC_VDD
DACC_VREF
DACC_RSET

DACC_RED AK4
DACC_GREEN AL4
DACC_BLUE AJ4
DACC_HSYNC AM1
DACC_VSYNC AM2
I2CB_SCL G3 — I2CB_SCL R404 EV@2.2K_4 → +3V
I2CB_SDA G2 — I2CB_SDA R405 EV@2.2K_4 → +3V

DACB(TV)

+DACC_VD AC6
R145 EV@10K/F_4 T68 AC5 T67 AB6

DACB_VDD
DACB_VREF
DACB_RSET

DACB_RED AA4
DACB_GREEN AB4
DACB_BLUE Y4
DACB_CSYNC AB5 T69

SI Build

XTAL_PLL

+VGA1.1V
L13 EV@HCB1608KF-181T15_6 +NV_PLLVDD AE9
C227 EV@1U/6.3V_4 C224 EV@1U/6.3V_4 C238 EV@1U/6.3V_4 C241 EV@.1U/10V_4 C245 EV@.1U/10V_4
65mA
50mA
25mA
AD9
AF9

PLLVDD
VID_PLLVDD
SP_PLLVDD

XTAL_SSIN D2 — 27M_SS [2]
XTAL_OUTBUFF D1 — BXTALOUT
XTAL_IN B1 — 27M_NONSS [2]
XTAL_OUT B2

NVidia suggest:
10 kΩ pull-down only if
no spread chip used.

27M_SS
BXTALOUT
R391 EV@10K/F_4
R396 EV@10K/F_4

SPREAD SPECTRUM

+3V
R379 *EV@10K/F_4
R392 *EV@10K/F_4
SI Build
R395 *EV@22_4 27M_SS
C520 *EV@10P/50V_4
GFX27M_L
+3V_SSC
R394 *EV@4.7_6 +3V

U23
ICSS_PD 8 PD# VDD 2
BXTALOUT 1 CLKIN CLKOUT 4
REFOUT 5 ICSS_RFO
SCL 7 EV_LVDS_DDCCLK
SDA 6 EV_LVDS_DDCDAT
GND 3
*EV@ICS91730AMLF-T

R397 *EV@10K/F_4
C506 *EV@470P/50V_4
C503 *EV@.1U/10V_4
C514 *EV@4.7U/6.3V_6
C513 *EV@4.7U/6.3V_6

[2..24] EV_LVDS_DDCCLK
[2..24] EV_LVDS_DDCDAT

I2C ADDRESS: 0xD4H

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Quanta Computer Inc.
PROJECT : ZR6E
Size | Document Number | Rev
NV10X (DISPLAY) 3/5 | 1A
Date: Tuesday, May 19, 2009 | Sheet 19 of 39

NV10M (VGA)

N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR

SEE Datasheet for details on G10x Straps!

NVidia Propose Remove C3134,C3681,R3092,R3402,R3063,R3064,C3076

Delete T31

HD Audio Level :3V

SI Build

NVidia Request

CLOSE U38 EMI

Logical Strap Bit Mapping

PCI_DEVID: STRAP2

NB9M-GE	0x06E	8	1000
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	0x064	9	1001
N10P-GE1	0x065	2	0010
N10M-GE1	0x06E	C	1100 default

R414 PU-VDD	PD
5K 1000	0000
10K 1001	0001
15K 1010	0010
20K 1011	0011
25K 1100	0100
30K 1101	0101
35K 1110	0110
45K 1111	0111

R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E

I2C ADDRESS: 0x98H

VGA THERMAIL CIRCUIT Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

THERMAL TRACE CONSTRAINTS

HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

SI Build

Waiting Confirm from Nvidia

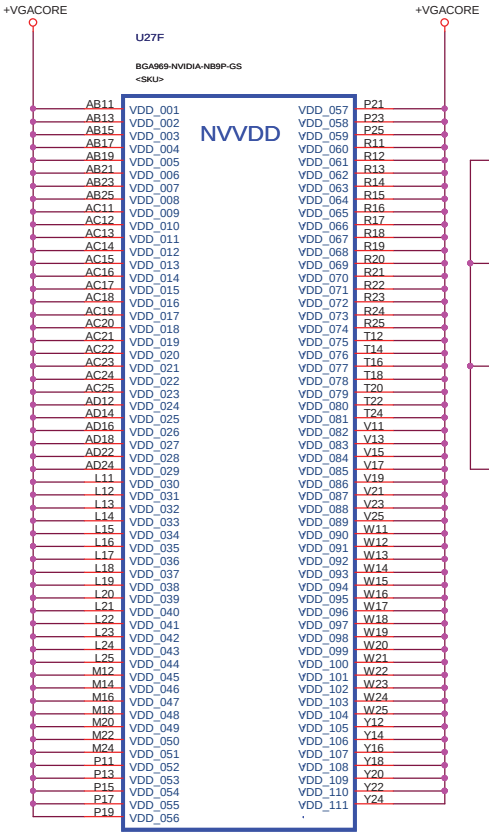
Quanta Computer Inc.

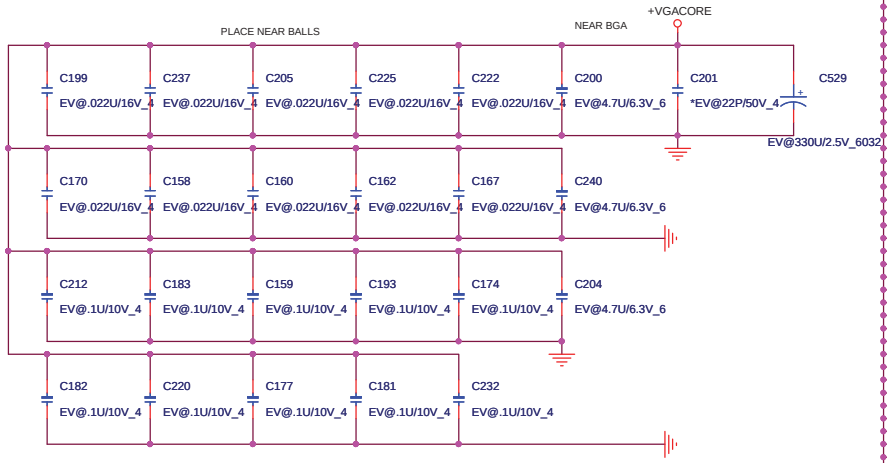
PROJECT : ZR6E

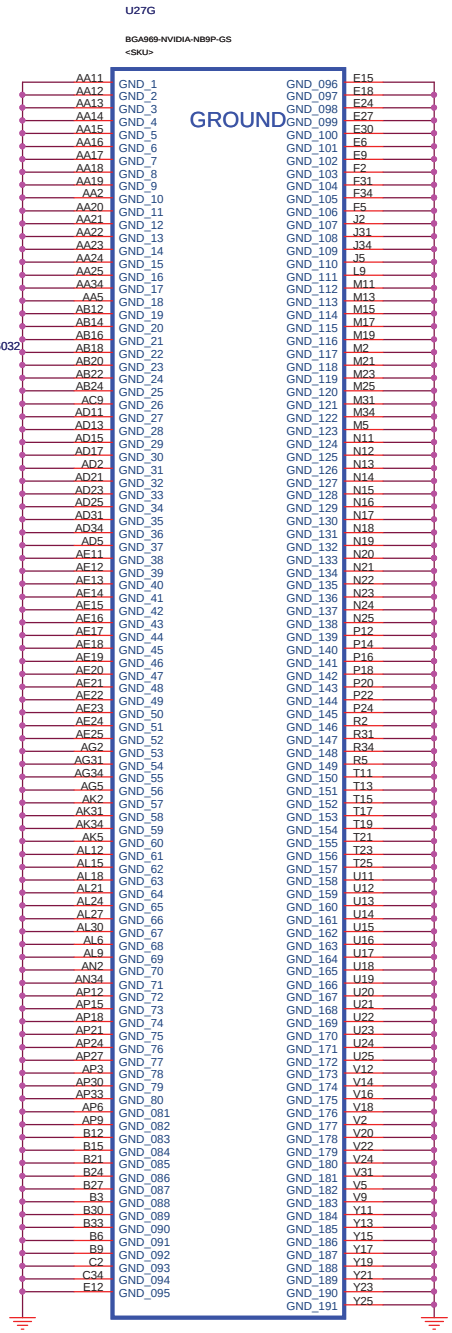
Size	Document Number	Rev
	NV10X (GPIO & STRRAPS) 4/5	1A

Date: Tuesday, May 19, 2009 Sheet 20 of 39

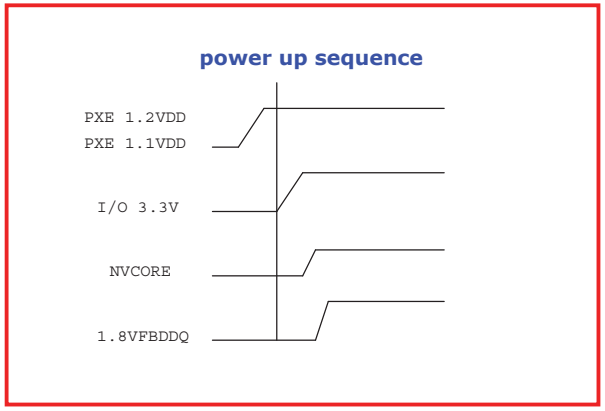
NVVDD Decoupling







Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10

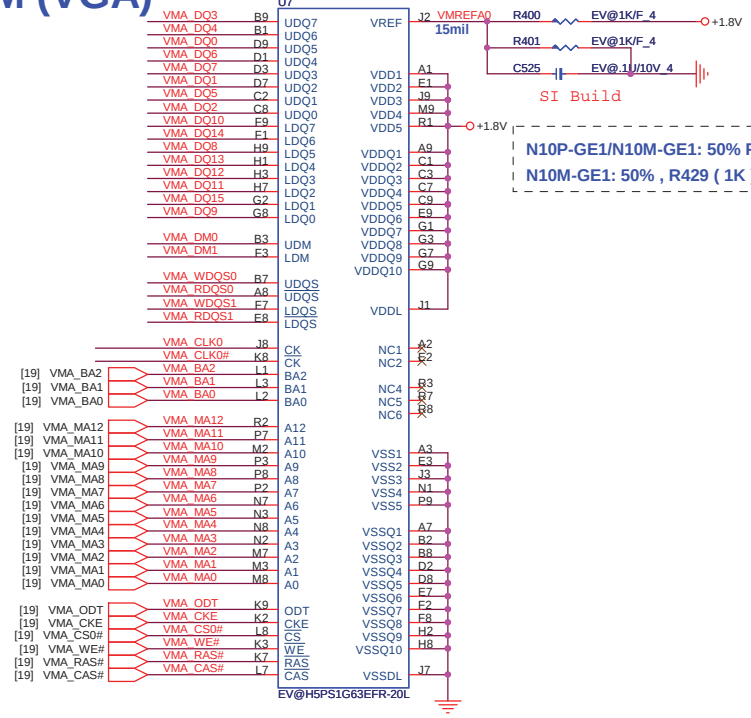


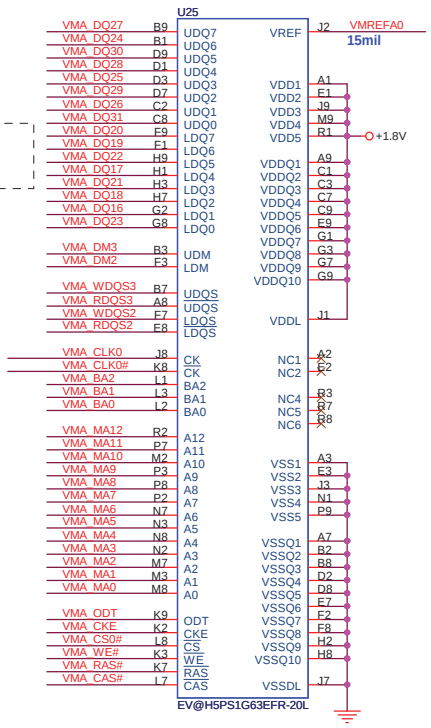
Quanta Computer Inc.

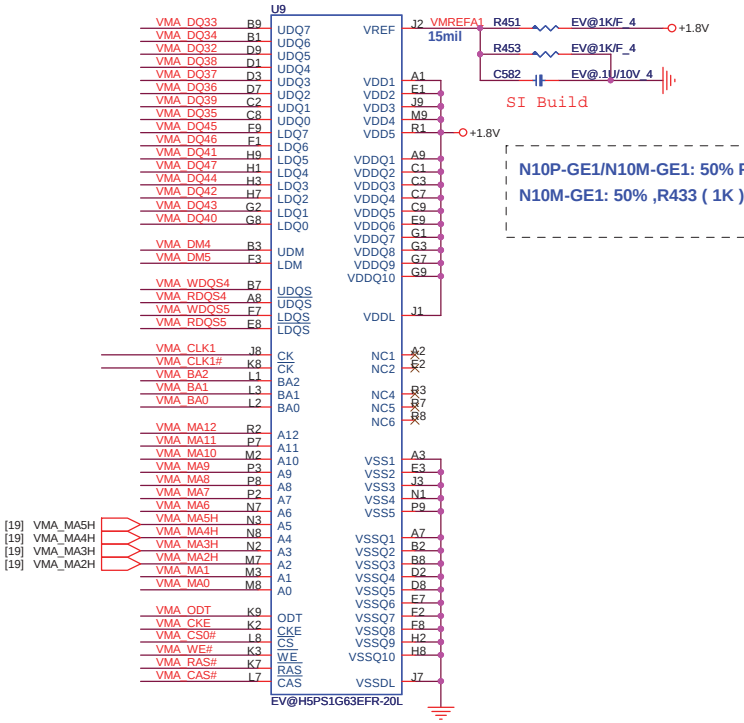
PROJECT : ZR6E

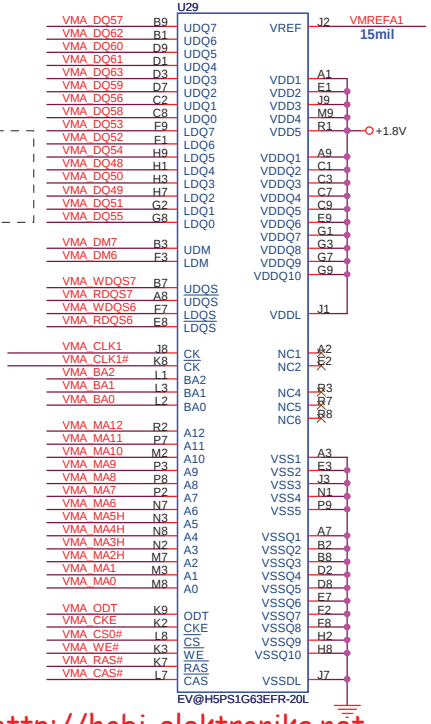
Size	Document Number	Rev
	NV10X (POWER & GND) 5/5	1A
Date: Tuesday, May 19, 2009	Sheet 21 of 39	

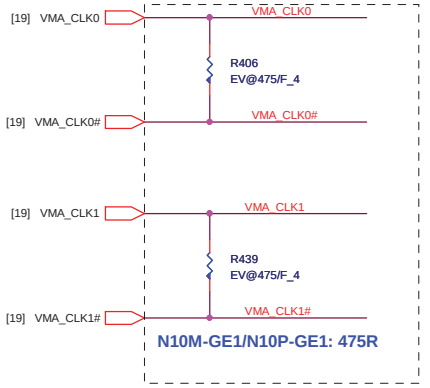
NV10M (VGA)





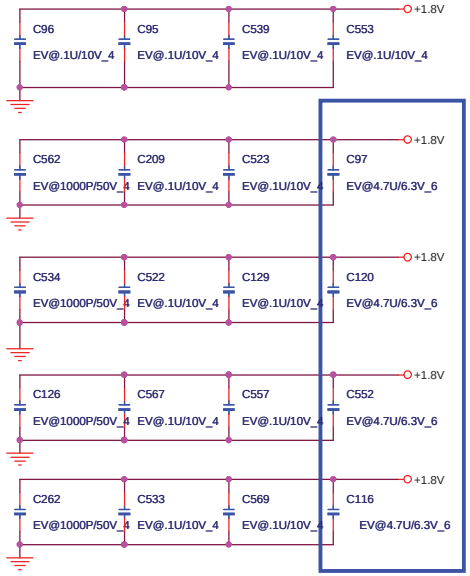


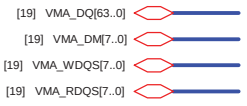




CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)



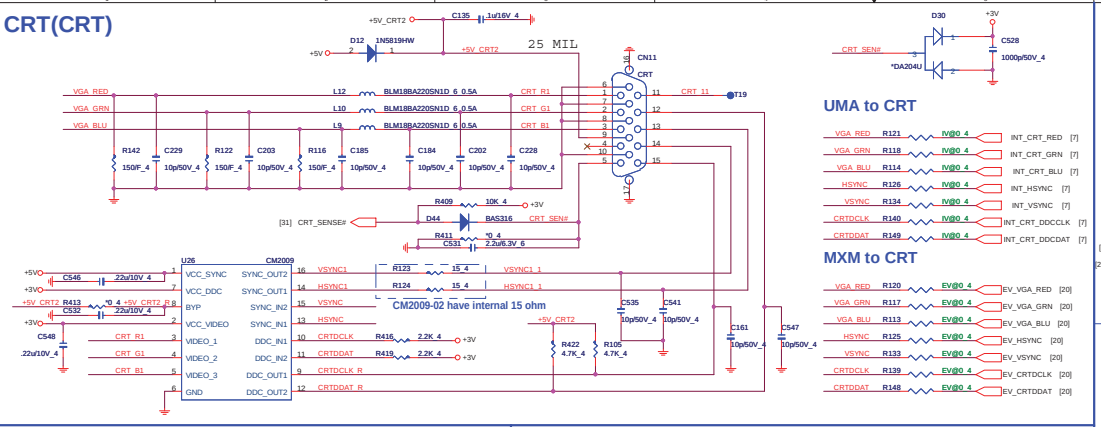


For DB:
N10P/N10M : AKD5LG-T510(Samsung,64M*16)
AKD5LG-TW02(Hynix,64M*16)

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	NV10X VRAM-1(GDDR2 BGA84)	1A
Date: Tuesday, May 19, 2009	Sheet 22 of 39	

CRT(CRT)



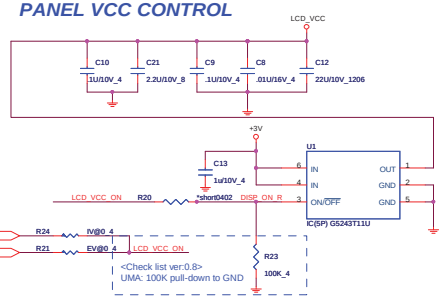
UMA to CRT

VGA_RED	R121 IV@0_4	INT_CRT_RED	[7]
VGA_GRN	R118 IV@0_4	INT_CRT_GRN	[7]
VGA_BLU	R114 IV@0_4	INT_CRT_BLU	[7]
HSYNC	R126 IV@0_4	INT_HSYNC	[7]
VSYNC	R134 IV@0_4	INT_VSYNC	[7]
CRTDCLK	R140 IV@0_4	INT_CRT_DDCCLK	[7]
CRTDDAT	R149 IV@0_4	INT_CRT_DDCDAT	[7]

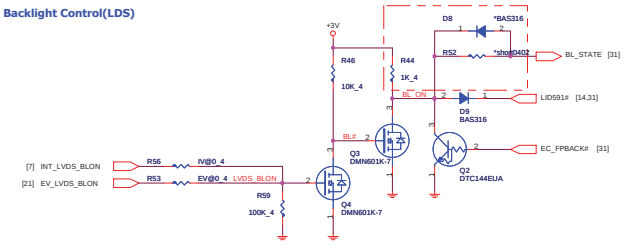
MXM to CRT

VGA_RED	R120 EV@0_4	EV_VGA_RED	[20]
VGA_GRN	R117 EV@0_4	EV_VGA_GRN	[20]
VGA_BLU	R113 EV@0_4	EV_VGA_BLU	[20]
HSYNC	R125 EV@0_4	EV_HSYNC	[20]
VSYNC	R133 EV@0_4	EV_VSYNC	[20]
CRTDCLK	R139 EV@0_4	EV_CRTDCLK	[20]
CRTDDAT	R148 EV@0_4	EV_CRTDDAT	[20]

LCD_ON(LDS) PANEL VCC CONTROL



Backlight Control(LDS)



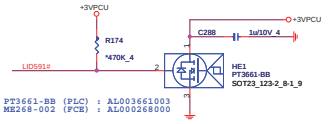
LVDS(LDS)

BRIGHTNESS
DPST

[21] EV_LVDS_BL_BRGHT — R50 *EV@0_4
[7] L_BKLT_CTRL — R48 IV@0_4
[31] CONTRAST — R45 EV@0_4
BRIGHTNESS

=> MXM
=> UMA
=> EC

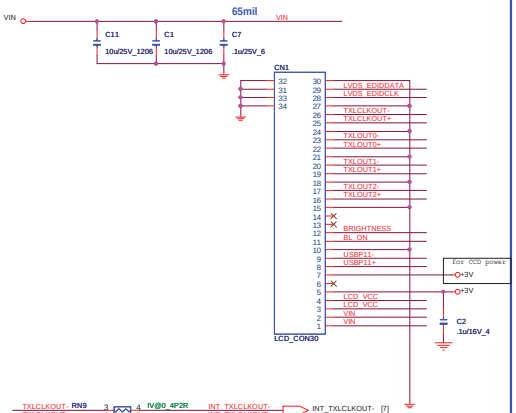
Lid Switch (HSR)



PT3661-BB (PLC) : AL003661003
MS268-002 (PCB) : AL000268000

LCD EDID SMBus PU

[20,21] EV_LVDS_DDCCLK — R8 EV@0_4
[7] INT_LVDS_EDIDCLK — R2 IV@0_4 — LVDS_EDIDCLK — R5 2.2K_4 — +3V
[20,21] EV_LVDS_DDCDAT — R9 EV@0_4
[7] INT_LVDS_EDIDDATA — R3 IV@0_4 — LVDS_EDIDDATA — R6 2.2K_4 — +3V



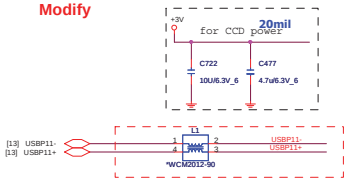
UMA to LVDS

TXLCLKOUT- / TXLCLKOUT+	RN9 IV@0_4P2R	INT_TXLCLKOUT- / INT_TXLCLKOUT+	[7]
TXLOUT0- / TXLOUT0+	RN5 IV@0_4P2R	INT_TXLOUT0- / INT_TXLOUT0+	[7]
TXLOUT1- / TXLOUT1+	RN7 IV@0_4P2R	INT_TXLOUT1- / INT_TXLOUT1+	[7]
TXLOUT2- / TXLOUT2+	RN3 IV@0_4P2R	INT_TXLOUT2- / INT_TXLOUT2+	[7]

MXM to LVDS

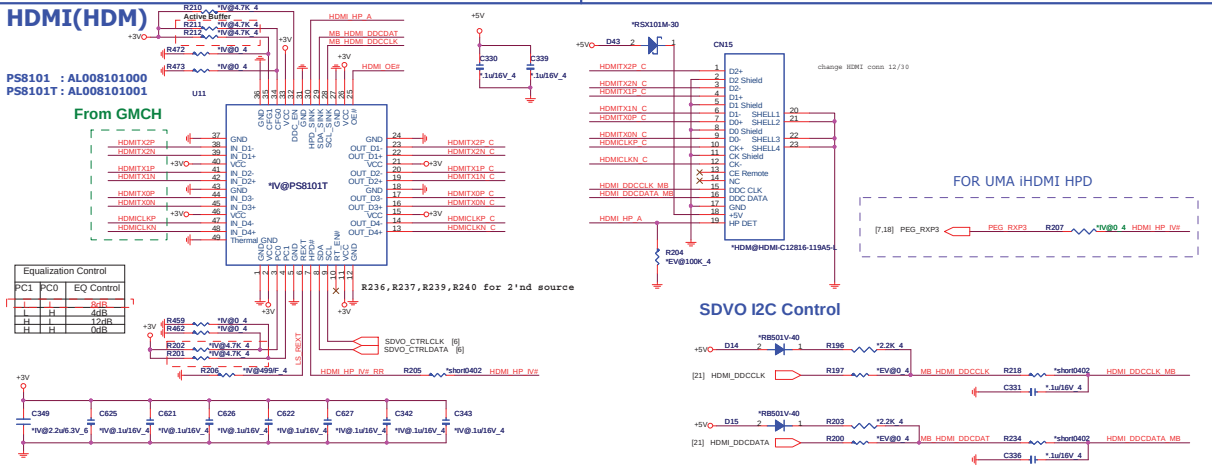
TXLCLKOUT- / TXLCLKOUT+	RN8 EV@0_4P2R	EV_TXLCLKOUT- / EV_TXLCLKOUT+	[20]
TXLOUT0- / TXLOUT0+	RN4 EV@0_4P2R	EV_TXLOUT0- / EV_TXLOUT0+	[20]
TXLOUT1- / TXLOUT1+	RN6 EV@0_4P2R	EV_TXLOUT1- / EV_TXLOUT1+	[20]
TXLOUT2- / TXLOUT2+	RN2 EV@0_4P2R	EV_TXLOUT2- / EV_TXLOUT2+	[20]

Camera(CCD) Modify



HDMI(HDM)

PS8101 : AL008101000
PS8101T : AL008101001



From MXM

HDMI_TX0N / HDMI_TX0P	RN33 *EV@0_4P2R	HDMITX0N_C / HDMITX0P_C	
HDMI_TX1N / HDMI_TX1P	RN34 *EV@0_4P2R	HDMITX1N_C / HDMITX1P_C	
HDMI_TX2N / HDMI_TX2P	RN35 *EV@0_4P2R	HDMITX2N_C / HDMITX2P_C	
HDMI_CLK- / HDMI_CLK+	RN32 *EV@0_4P2R	HDMICLKN_C / HDMICLKP_C	

From GMCH (iHDMI)

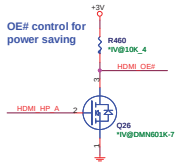
PEG_TXP2 / PEG_TXN2	RN12 *IV@0_4P2R	HDMITX0P / HDMITX0N	
PEG_TXP1 / PEG_TXN1	RN11 *IV@0_4P2R	HDMITX1P / HDMITX1N	
PEG_TXP0 / PEG_TXN0	RN10 *IV@0_4P2R	HDMITX2P / HDMITX2N	
PEG_TXP3 / PEG_TXN3	RN13 *IV@0_4P2R	HDMICLKP / HDMICLKN	

FOR UMA iHDMI HPD

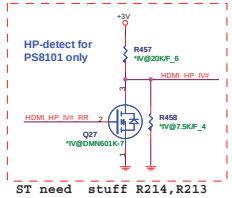
[7,18] PEG_RXP3 — PEG_RXP3 — R207 *IV@0_4 — HDMI_HP_IV#

SDVO I2C Control

OE# control for power saving

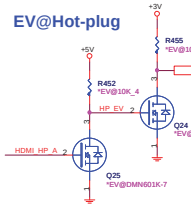


HP-detect for PS8101 only



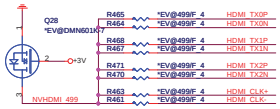
ST need stuff R214,R213

EV@Hot-plug



FOR NV HDMI

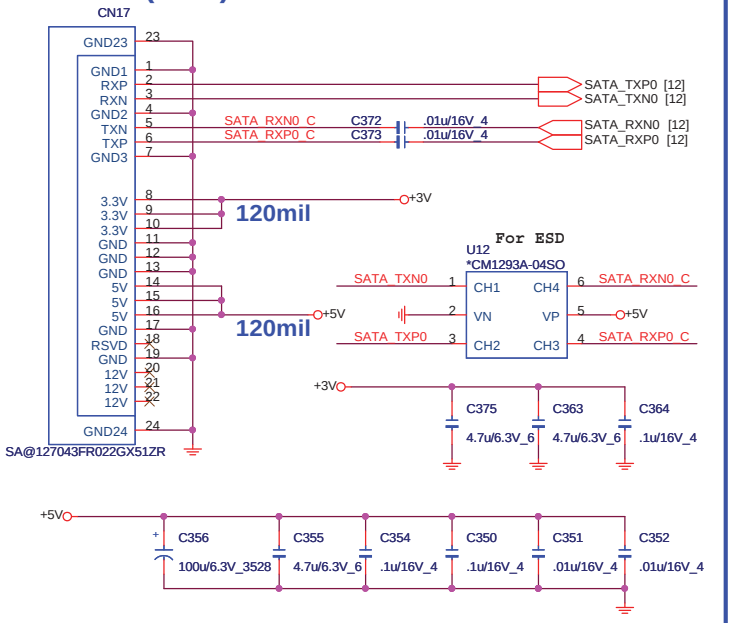
NV suggestion near HDMI connector



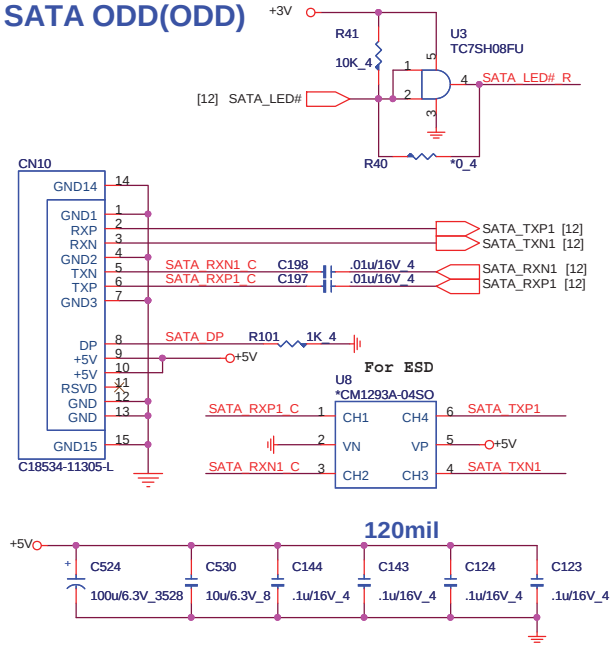
http://hobi-elektronika.net

Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number	Rev
	LVDS/CRT/CCD/HDMI/MIC	1A
Date: Tuesday, May 19, 2009	Sheet 23 of 39	

SATA HDD(HDD)

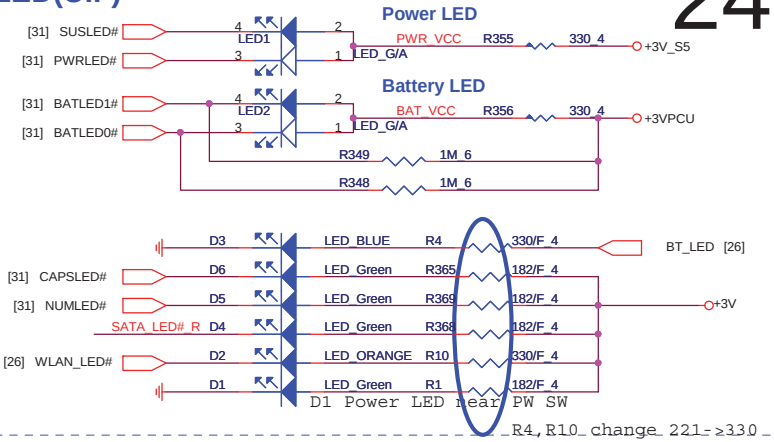


SATA ODD(ODD)



LED(UIF)

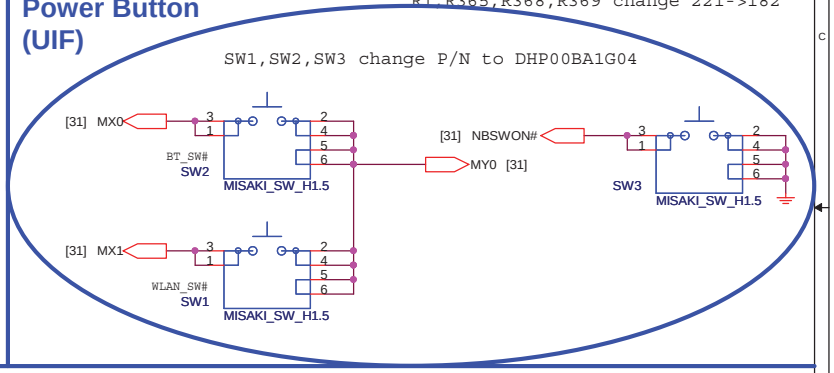
Power/Suspend: Green/Amber



R4,R10 change 221->330

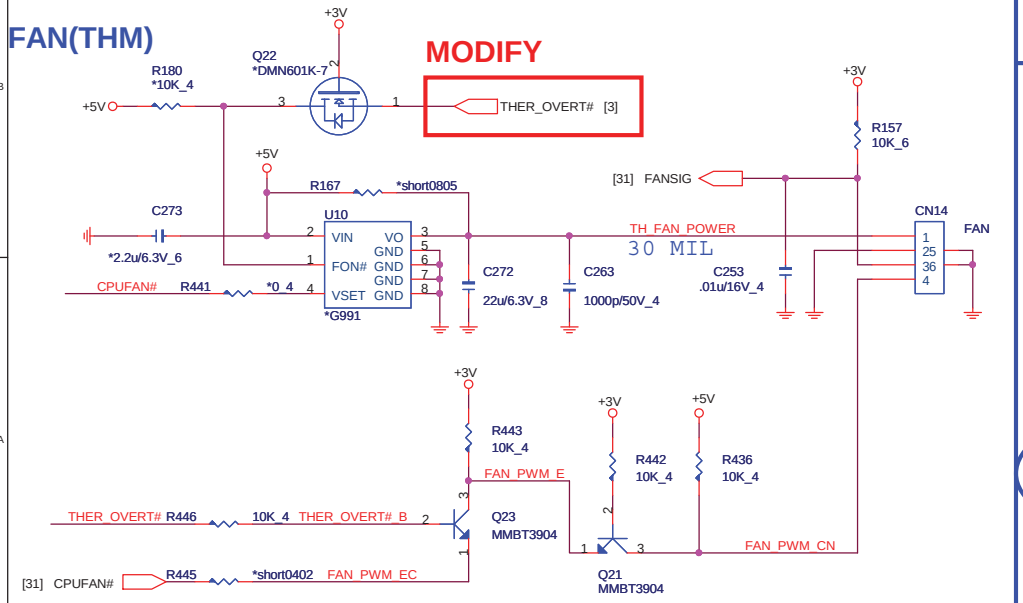
R1,R365,R368,R369 change 221->182

Power Button (UIF)



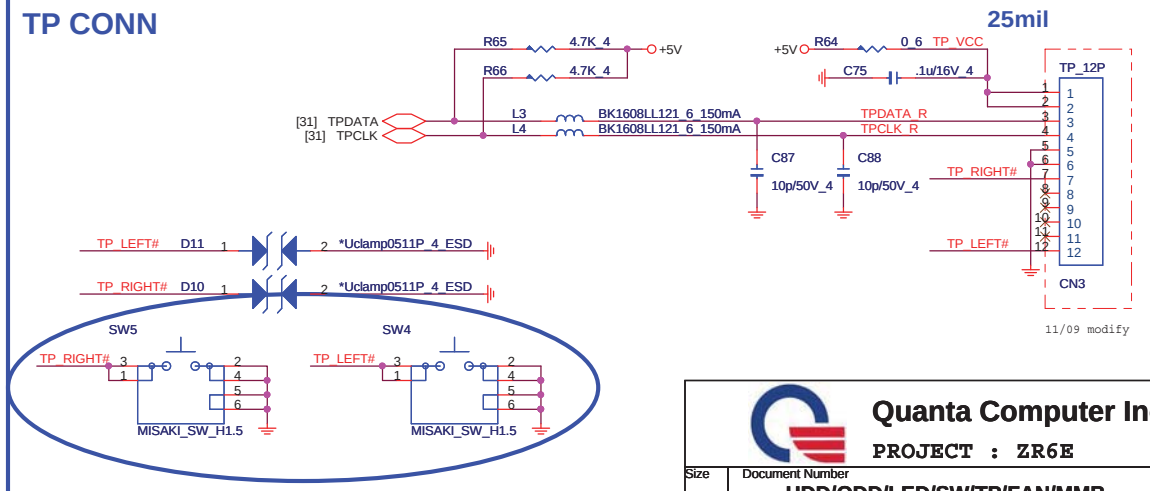
FAN(THM)

MODIFY



TP CONN

25mil



SW4,SW5 change P/N to DHP00BA1G04

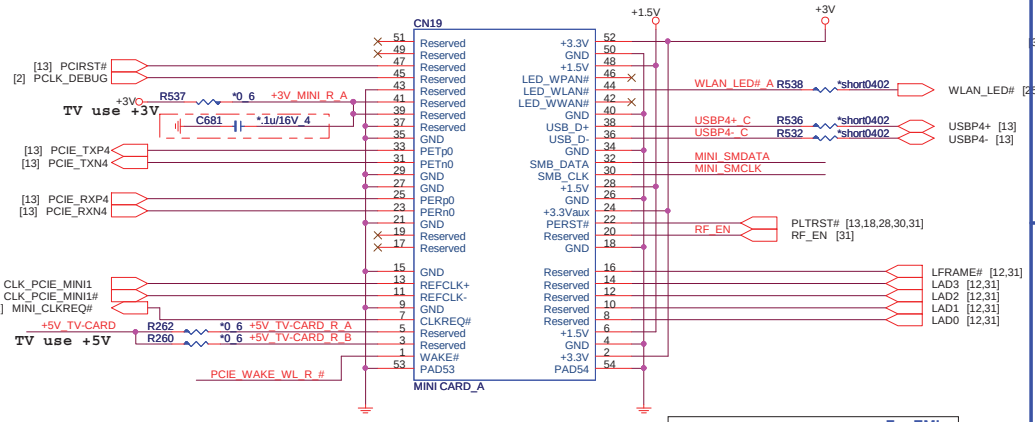
Quanta Computer Inc.

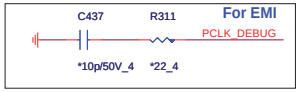
PROJECT : ZR6E

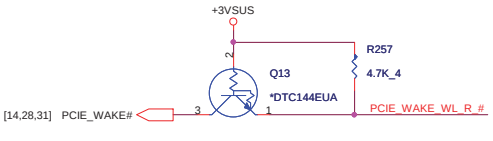
Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A

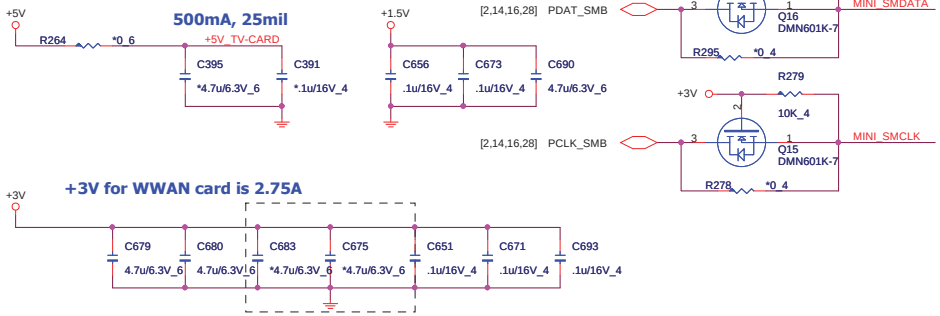
Date: Tuesday, May 19, 2009 Sheet 24 of 39

MINI-CARD(MPC)

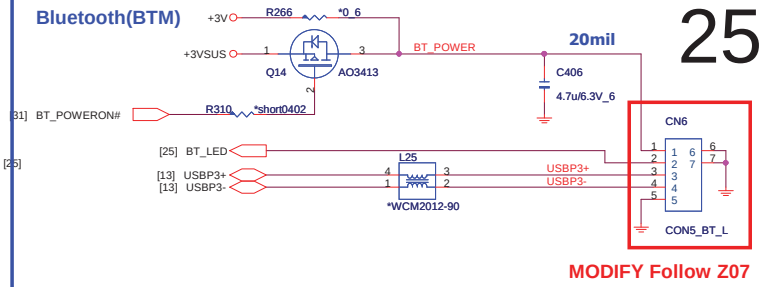




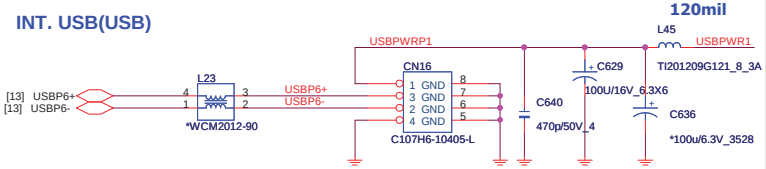


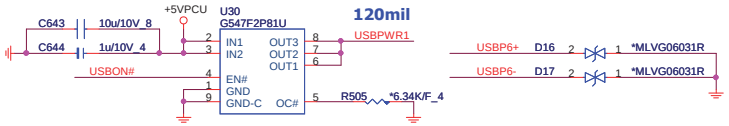


Bluetooth(BTM)

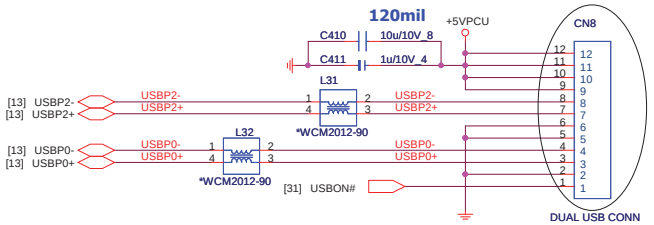


INT. USB(USB)



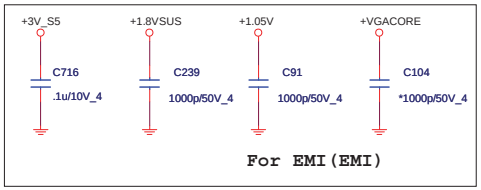


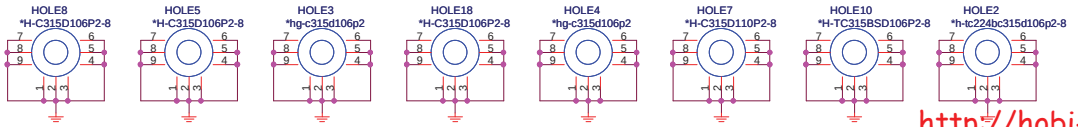
EXT. USB(USB)



Modfiy C

(OTH)





Quanta Computer Inc.

PROJECT : ZR6E

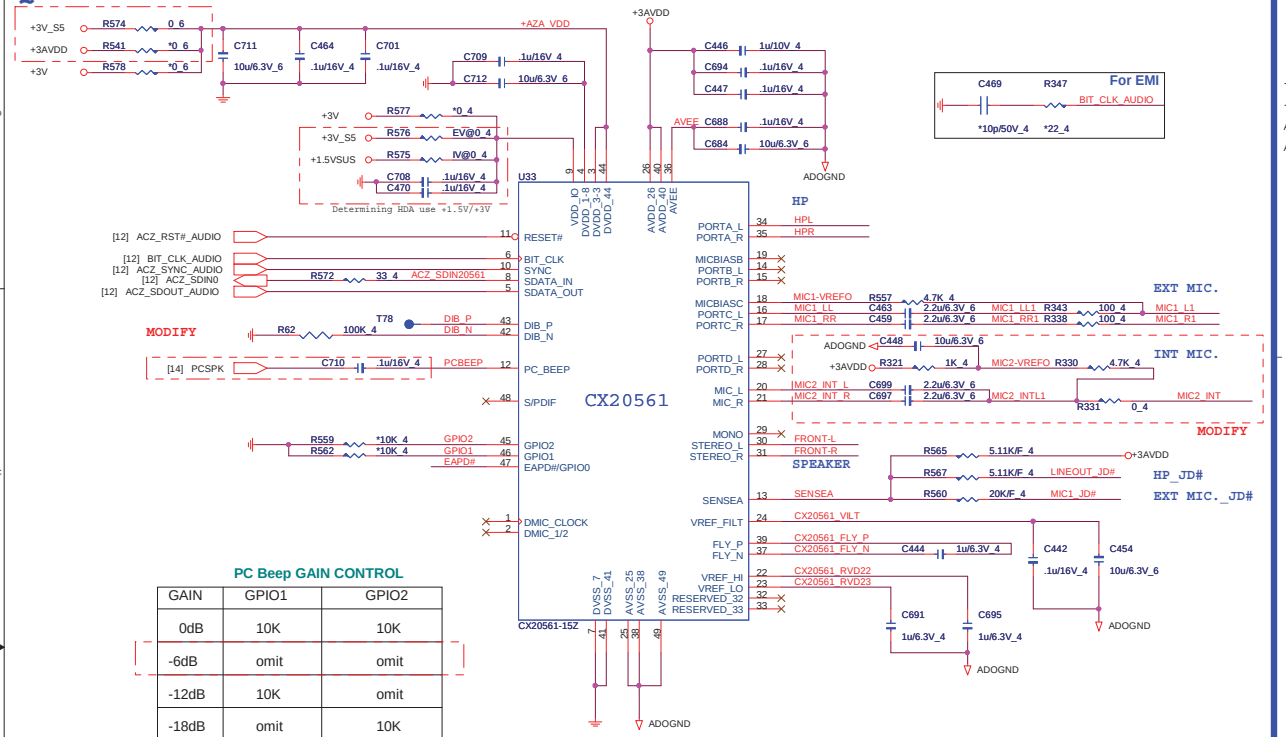
Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A

Date: Tuesday, May 19, 2009 Sheet 25 of 39

Codec CX20561-15Z (ADO)

QFN

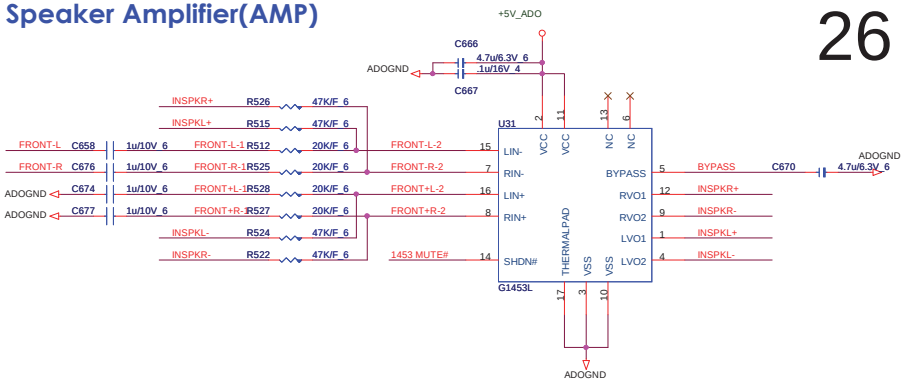
MODIFY REV:C



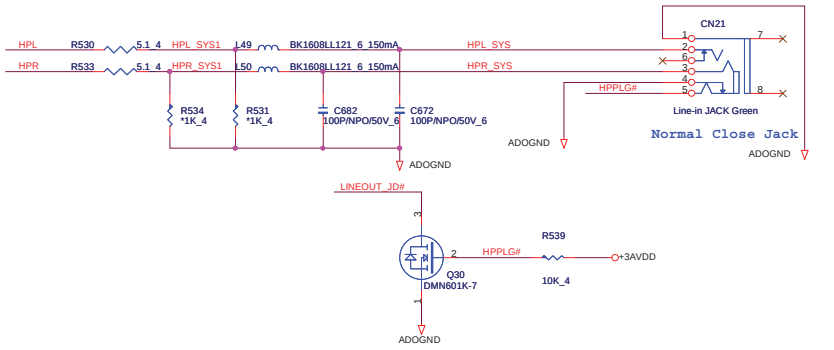
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

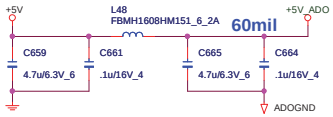
Speaker Amplifier(AMP)



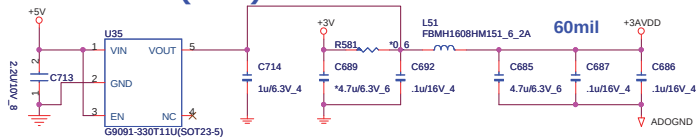
LINE OUT(AMP)



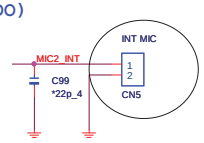
AMP Power(AMP)



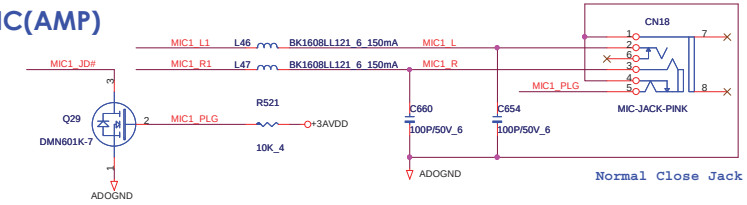
CODER Power(ADO)



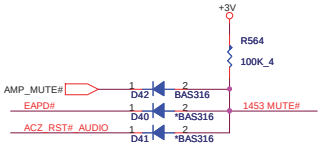
INT MIC.(ADO)



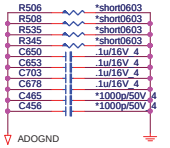
MIC(AMP)



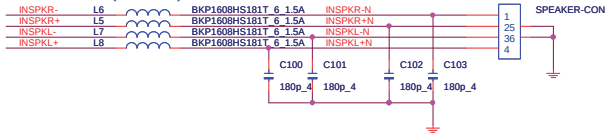
MUTE(AMP)



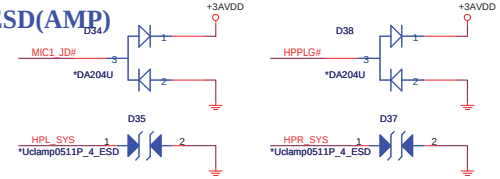
(ADO)



SPEAKER(AMP)



ESD(AMP)



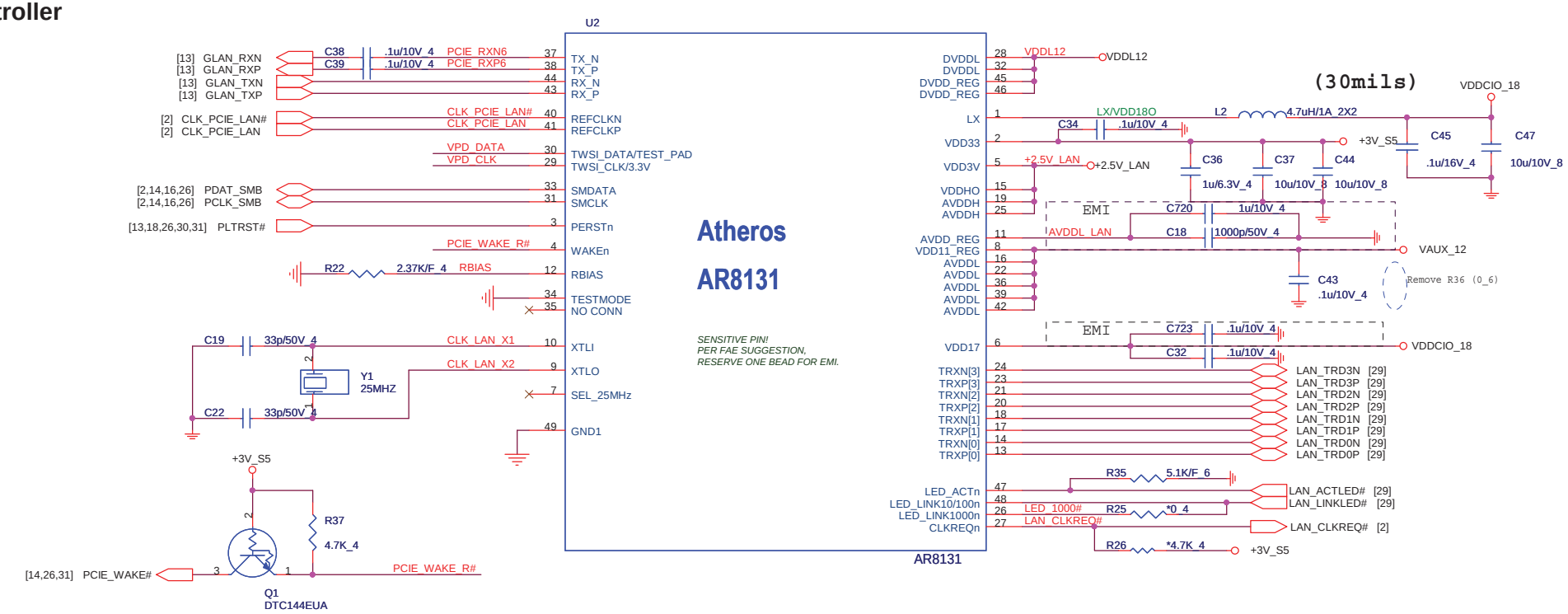
Quanta Computer Inc.

PROJECT : ZR6E

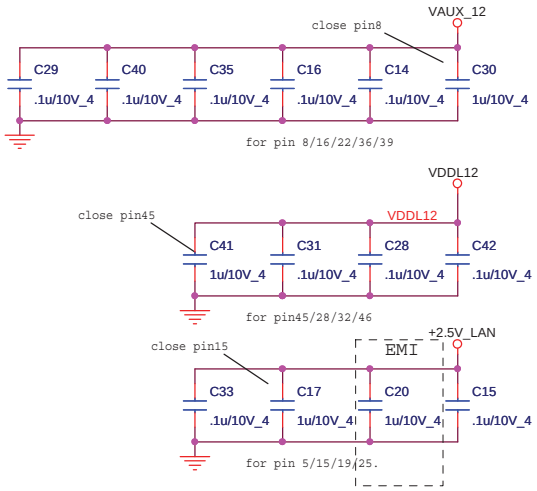
Size	Document Number	Rev
	CODEC/AMP/MDC	1A

Date: Tuesday, May 19, 2009 Sheet 26 of 39

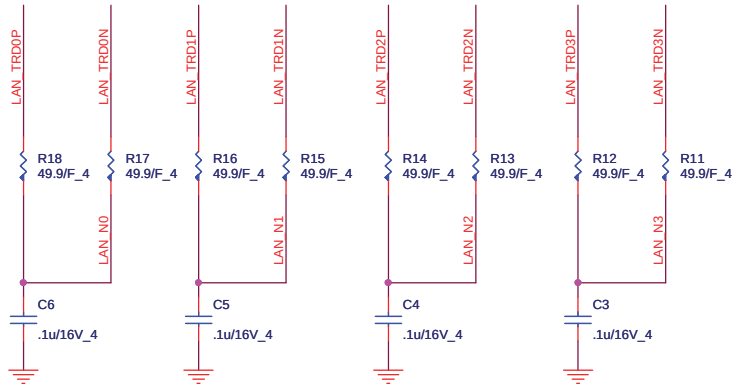
LAN Controller



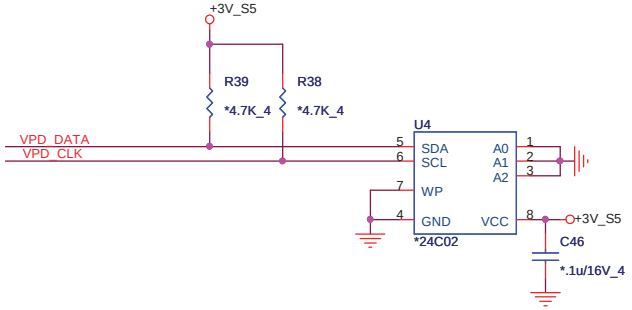
Decoupling CAP



PLACE NEAR IC SIDE



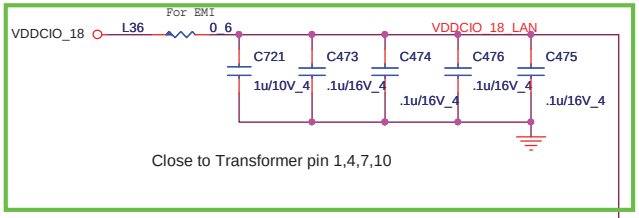
EEPROM



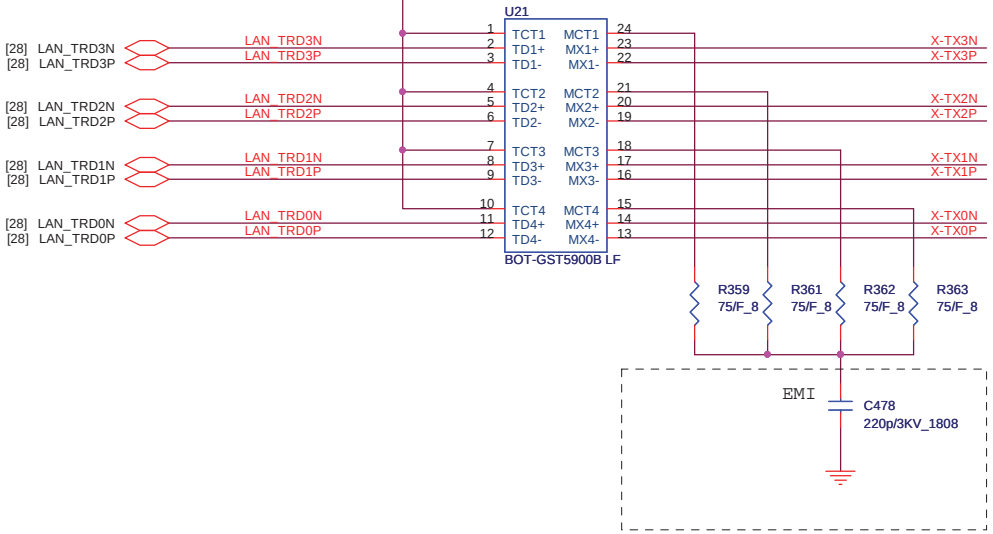
Quanta Computer Inc.

PROJECT : ZR6E

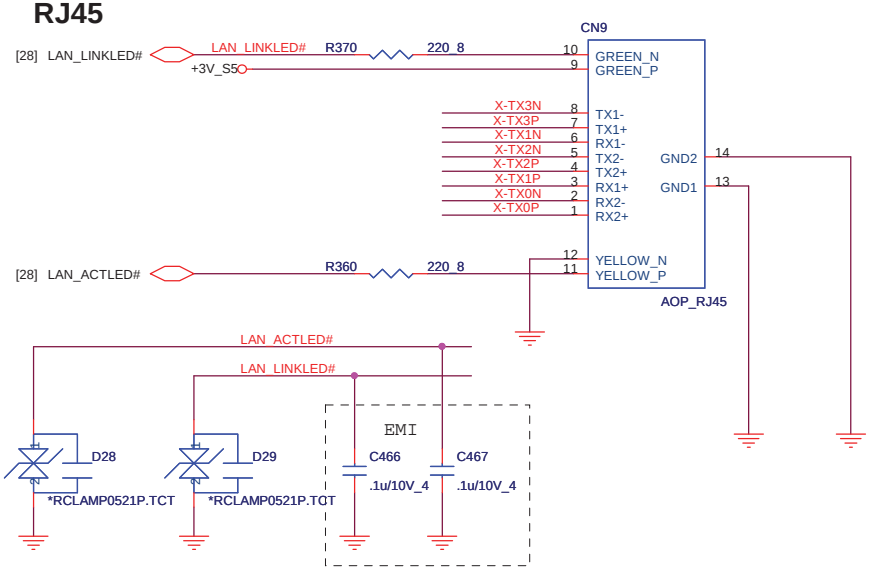
Size	Document Number	Rev
	AR8131 GLAN	1A
Date: Tuesday, May 19, 2009	Sheet 27 of 39	



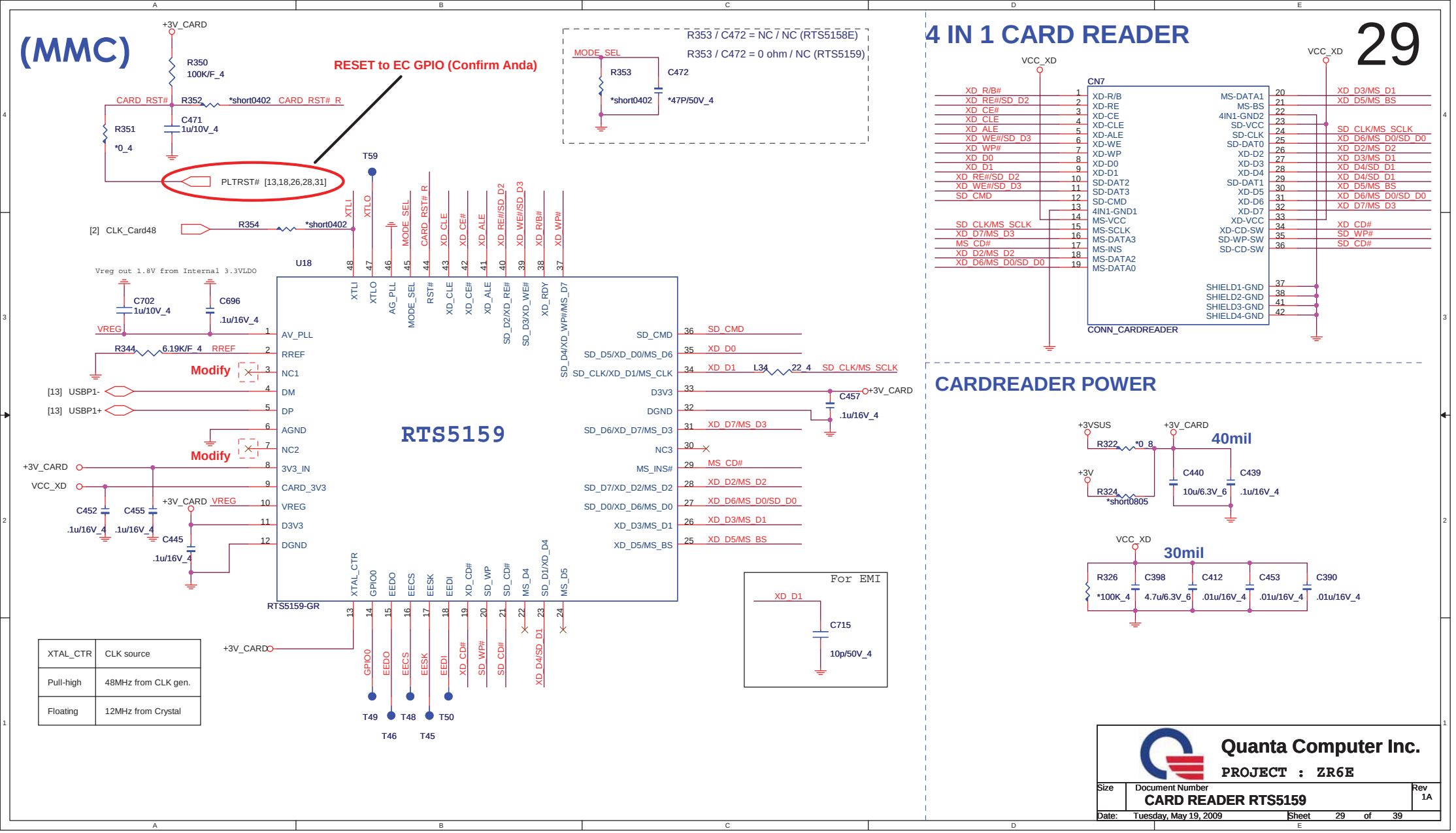
TRANSFORMER



RJ45



Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: LAN Transformer and RJ45/BT	Rev 1A
Date: Tuesday, May 19, 2009	Sheet 28 of 39	



EC(KBC)

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 — R303 10K_4
BADDR1 — uR_SOUT_CR — R302 *10K_4
SHBM — SHBM — R269 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

+3VPCU
MBCLK — R513 4.7K_4
MBDATA — R509 4.7K_4
MXM_SMCLK — R304 4.7K_4
MXM_SMDATA — R305 4.7K_4

+3V
2ND_MBCLK — R259 4.7K_4
2ND_MBDATA — R261 4.7K_4
CRT_SENSE# — R523 4.7K_4

ACER ID

MXM_SMCLK
MXM_SMDATA
U16 24C02 (SCL, SDA, A0, A1, A2, WP, VCC, GND)
+3VPCU — R316 *0_4
+3V_S5 — R323 *short0402
C449 *.1u/16V_4_X7R

SPI FLASH

2'nd Source AKE38ZA0Q00

SPI_SDI_uR R325 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
R333 10K_4 SPI_CS0#_uR
U17 W25X16AVSSIG (SO, SI, SCK, CE, VDD, HOLD, WP, VSS)
C443 .1u/16V_4_X7R

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

+3V — R273 10K_4

[37] 1V8_ON — D19 EV@BAS316
[38] HWPG_1.5V — D24 BAS316
[34] HWPG_1.05V — D20 BAS316
[36] HWPG_1.8V — D25 BAS316
[33] SYS_HWPG — D21 BAS316
[3,6,14,35] DELAY_VR_PWRGOOD — D22 *BAS316
[37] HWPG_1.1V — D23 EV@BAS316
HWPG — R263 *short0402 — MPWROK [6,14]

1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

POWER-ON PAD(UIF)

G1 — NBSWON# — *SHORT_PAD

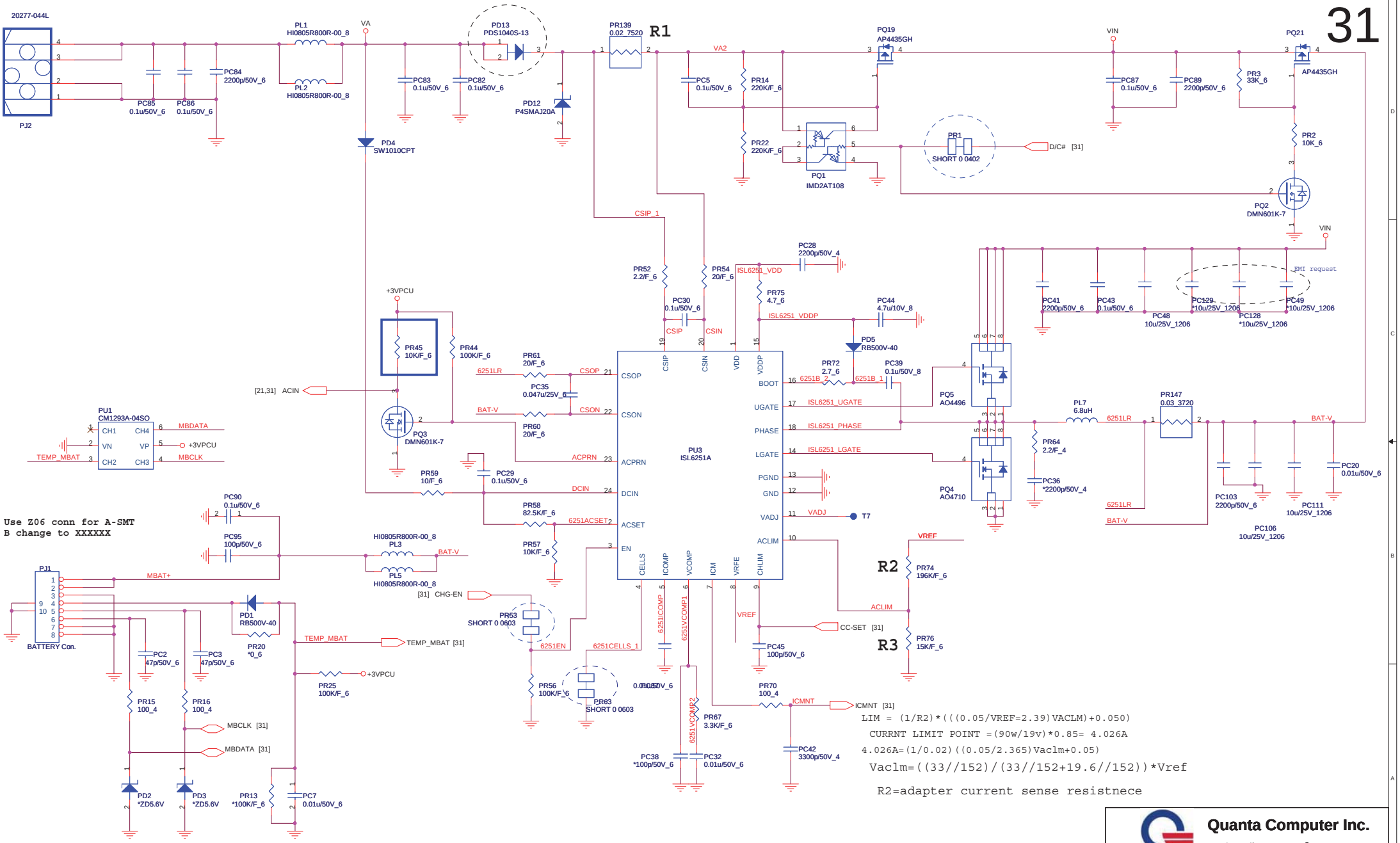
Thermal Sensor(THM)

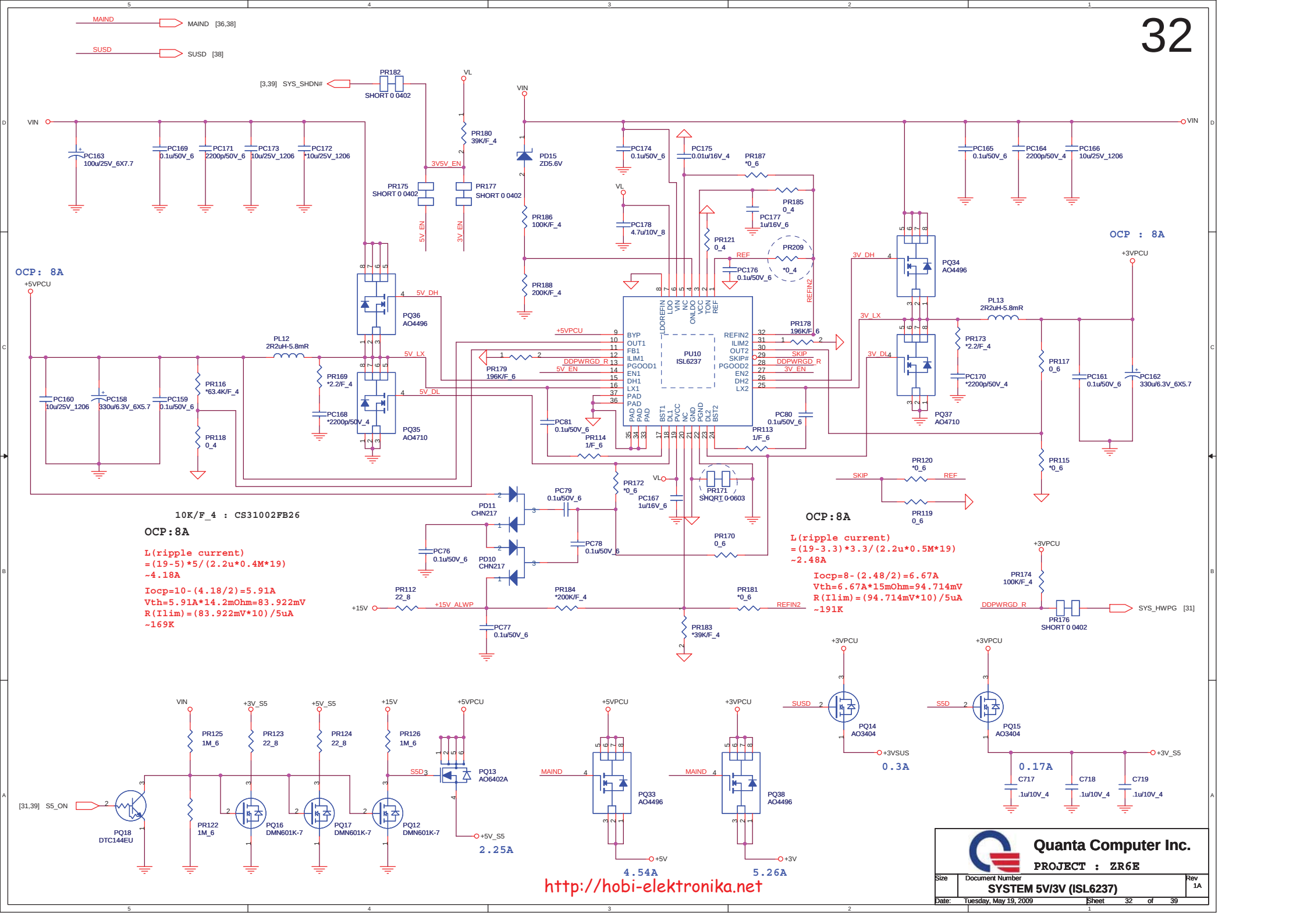
+3V — R300 47K/F_4 — R301 100K/F_4 NTC — TPD_TRIP

INTERNAL KEYBOARD STRIP SET

+3VPCU — MY0 — R247 10K_4

Quanta Computer Inc.
PROJECT : ZR6E
Size | Document Number: WPCE775C_0DG & FLASH | Rev 1A
Date: Tuesday, May 19, 2009 | Sheet 30 of 39




MAIND
MAIND [36,38]
SUSD
SUSD [38]
[3,39] SYS_SHDN#
PR182
SHORT 0 0402
VL
VIN
PR180
39K/F_4
PD15
ZD5.6V
3V5V_EN
PR175
SHORT 0 0402
PR177
SHORT 0 0402
5V_EN
3V_EN
PR186
100K/F_4
PR188
200K/F_4
PC163
100u/25V_6X7.7
PC169
0.1u/50V_6
PC171
2200p/50V_6
PC173
10u/25V_1206
PC172
*10u/25V_1206
PC174
0.1u/50V_6
PC175
0.01u/16V_4
PR187
*0_6
PR185
0_4
PC177
1u/16V_6
PC178
4.7u/10V_8
PR121
0_4
REF
PR209
*0_4
PC176
0.1u/50V_6
REFIN2
PC165
0.1u/50V_6
PC164
2200p/50V_4
PC166
10u/25V_1206
OCP : 8A
OCP: 8A
+5VPCU
PQ36
AO4496
5V_DH
5V_LX
5V_DL
PQ35
AO4710
PL12
2R2uH-5.8mR
PR169
*2.2/F_4
PC168
*2200p/50V_4
PR116
*63.4K/F_4
PR118
0_4
PC160
10u/25V_1206
PC158
330u/6.3V_6X5.7
PC159
0.1u/50V_6
PU10
ISL6237
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
BST1
DL1
PVCC
NC
GND
PSN
DL2
BST2
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR179
196K/F_6
DDPWRGD_R
PR178
196K/F_6
SKIP
3V_EN
PC81
0.1u/50V_6
PR114
1/F_6
PC80
0.1u/50V_6
PR113
1/F_6
3V_DH
3V_LX
3V_DL
PQ34
AO4496
PQ37
AO4710
PL13
2R2uH-5.8mR
PR173
*2.2/F_4
PC170
*2200p/50V_4
PR117
0_6
PC161
0.1u/50V_6
PC162
330u/6.3V_6X5.7
PR115
*0_6
PR120
*0_6
PR119
0_6
PR172
*0_6
PC167
1u/16V_6
PR171
SHORT 0 0603
PR170
0_6
10K/F_4 : CS31002FB26
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=5.91A
Vth=5.91A*14.2mOhm=83.922mV
R(Ilim)=(83.922mV*10)/5uA
~169K
PD11
CHN217
PD10
CHN217
PC79
0.1u/50V_6
PC78
0.1u/50V_6
PC76
0.1u/50V_6
PC77
0.1u/50V_6
PR112
22_8
+15V
+15V_ALWP
PR184
*200K/F_4
PR181
*0_6
REFIN2
PR183
*39K/F_4
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR174
100K/F_4
DDPWRGD_R
PR176
SHORT 0 0402
SYS_HWPG [31]
[31,39] S5_ON
PQ18
DTC144EU
PR125
1M_6
PR122
1M_6
PR123
22_8
PR124
22_8
PR126
1M_6
PQ16
DMN601K-7
PQ17
DMN601K-7
PQ12
DMN601K-7
S5D
PQ13
AO6402A
+5V_S5
2.25A
MAIND
PQ33
AO4496
+5V
4.54A
PQ38
AO4496
+3V
5.26A
SUSD
PQ14
AO3404
+3VSUS
0.3A
PQ15
AO3404
+3V_S5
0.17A
C717
.1u/10V_4
C718
.1u/10V_4
C719
.1u/10V_4
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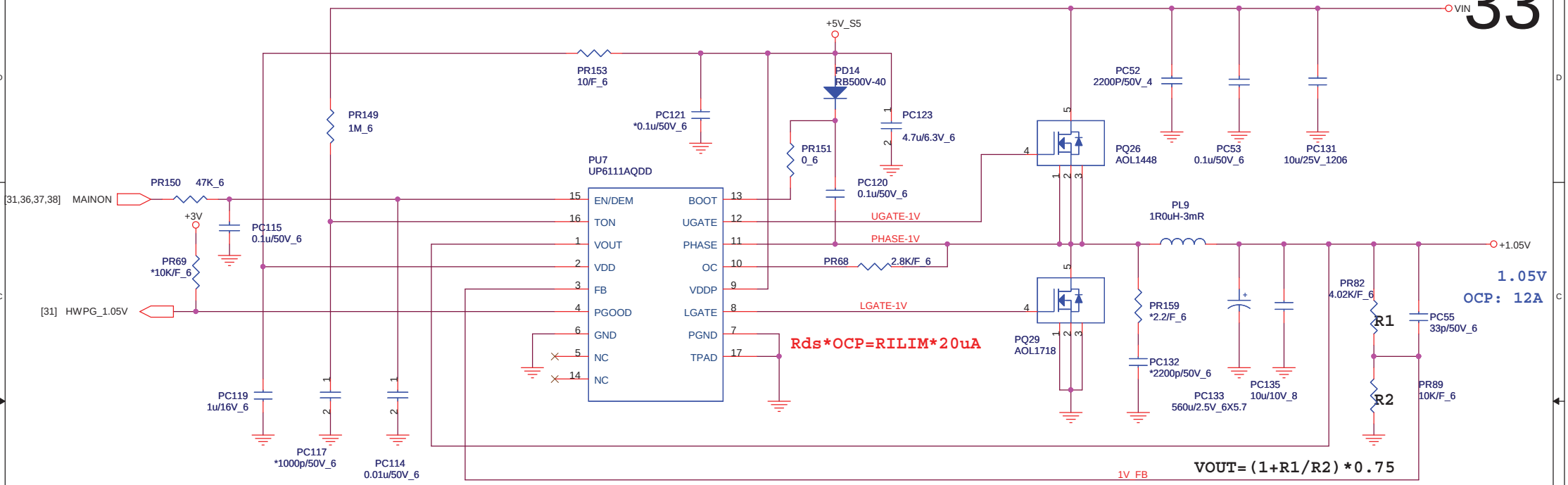
Quanta Computer Inc.
PROJECT : ZR6E
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev
1A
Date: Tuesday, May 19, 2009
Sheet 32 of 39



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

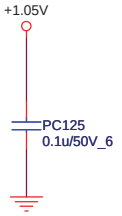
AOL1412 Rdson=4.6mOhm

OCP=16-0.8A

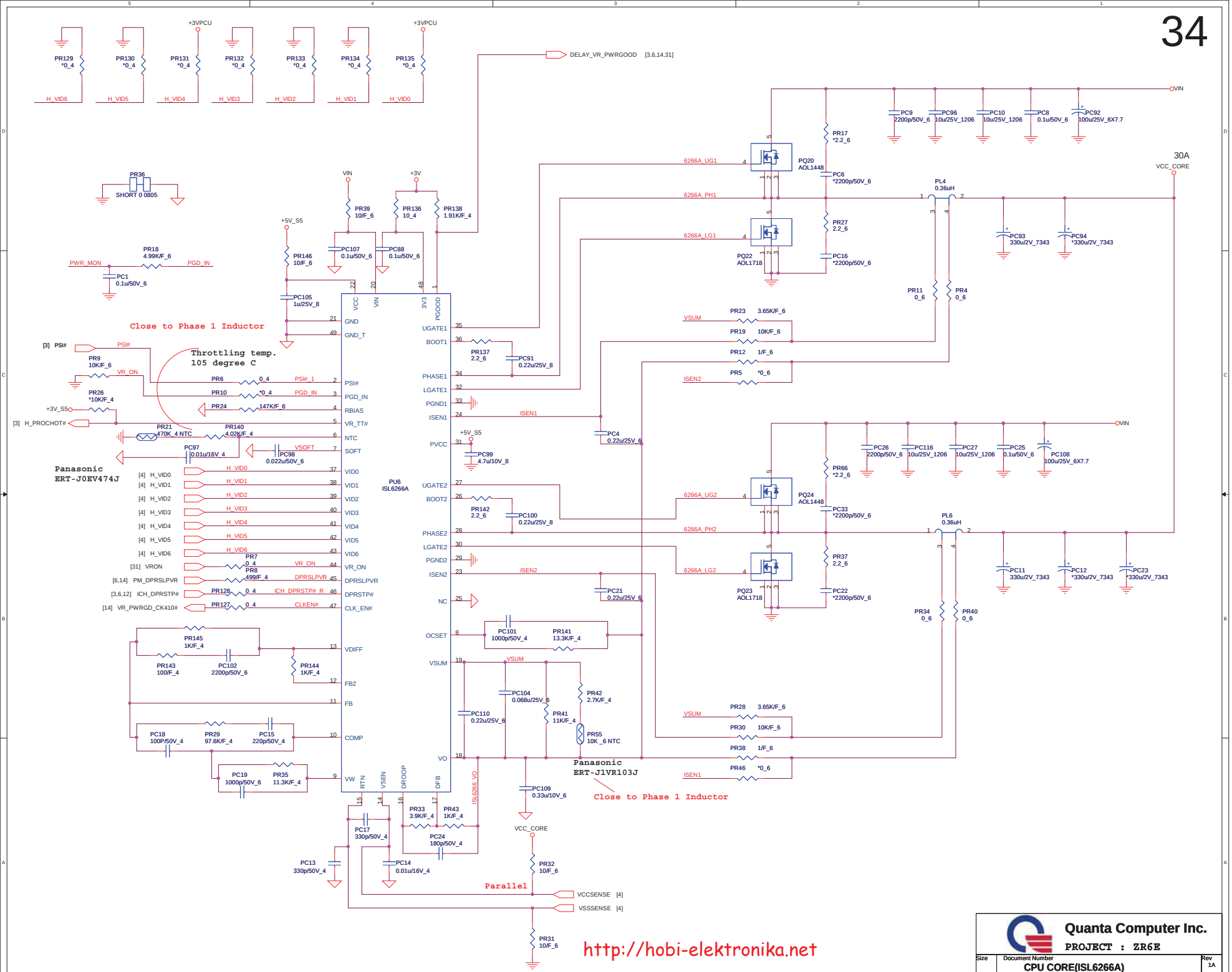
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA

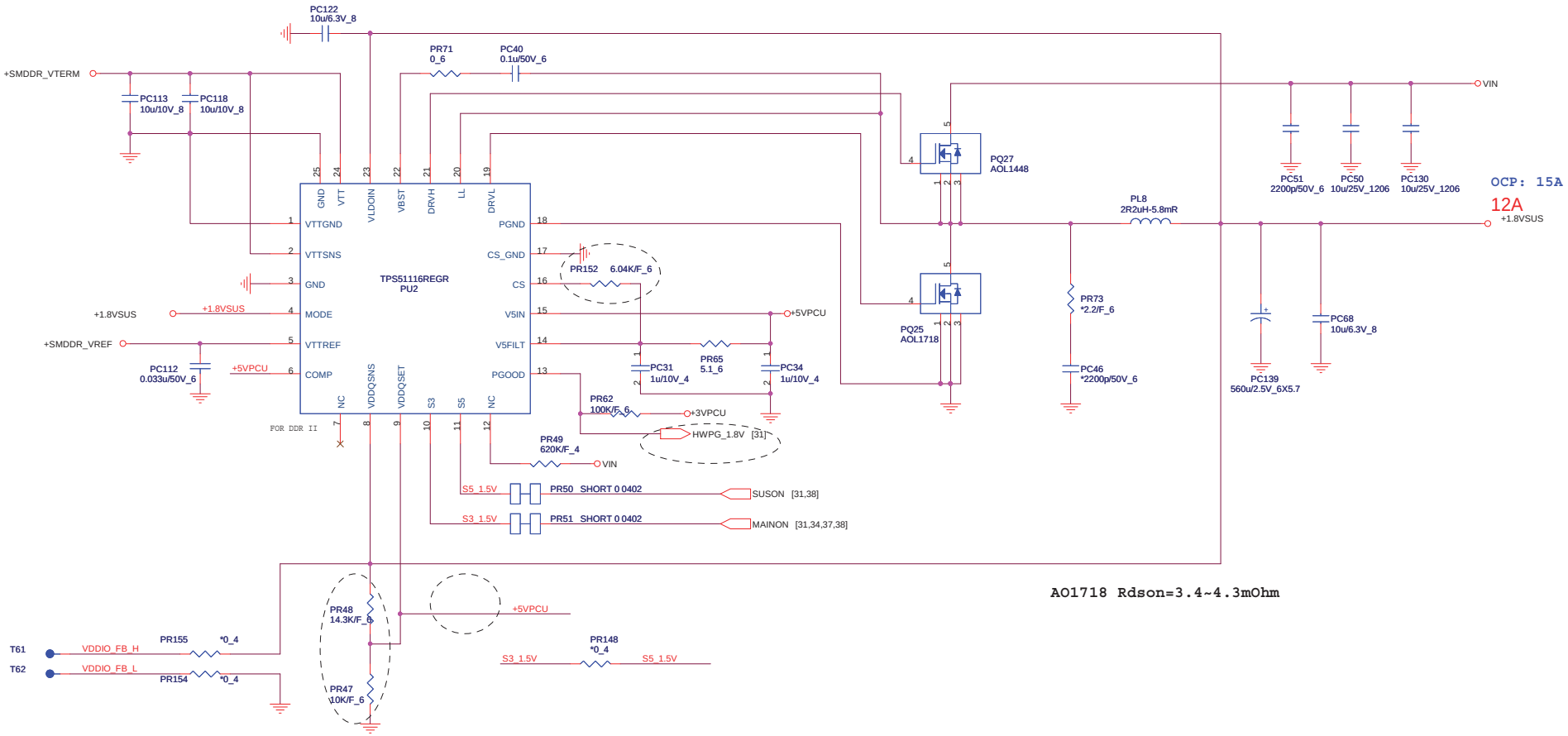
RILIM=2.76K--- 2.8K

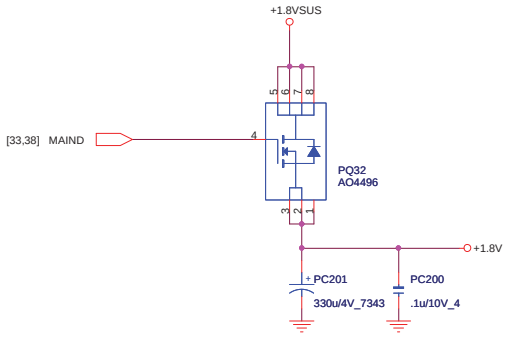


Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Tuesday, May 19, 2009	Sheet 33 of 39	



Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: CPU CORE(ISL6266A)	Rev: 1A
Date: Tuesday, May 19, 2009	Sheet 34 of 39	





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PROJECT : ZR6E

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Wednesday, May 20, 2009 Sheet 35 of 39

VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =	1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =	1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =	0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =	0.91 (G0=1, G1=1)

[31,34,36,38] MAINON — MAINON

[21] GPU_VID1 — [21] GPU_VID0

PU4 EV@OZ8111 — AGND VDDA TEST VREF VSET; OCT VIN ON/SKIP PGD; CSN CSP LX HDR; VDDP GNDP LDR BST

PU8 EV@G973 — VIN VIN1 EN VCNTL FB; POK GND VOUT VOUT

PQ7 EV@DMN601K-7 (G1) PQ6 EV@DMN601K-7 (G0) PQ28 EV@AOL1448 PQ30 EV@AOL1718

PD6 EV@RB500V-40

PL10 EV@1R5uH-3.9mR

OCP:18A
14A

+VGACORE

[31] 1V8_ON

[18] VGA_SENSE — PR79 *EV@100/F_4

M92LP

+VGA1.1V
2.435A

Vout =0.8(1+R1/R2)
=1.5V

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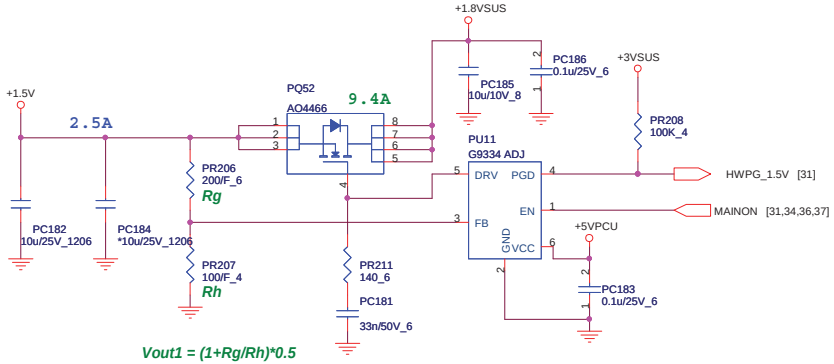
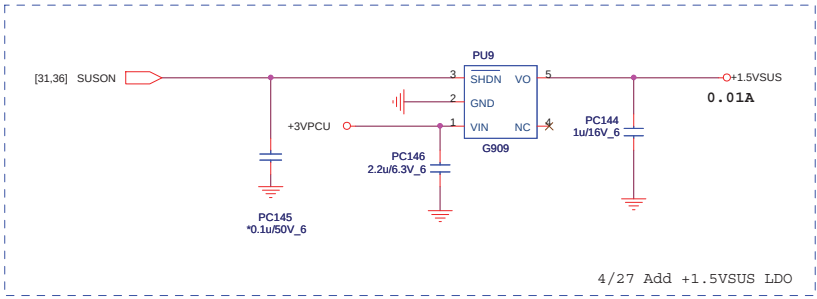
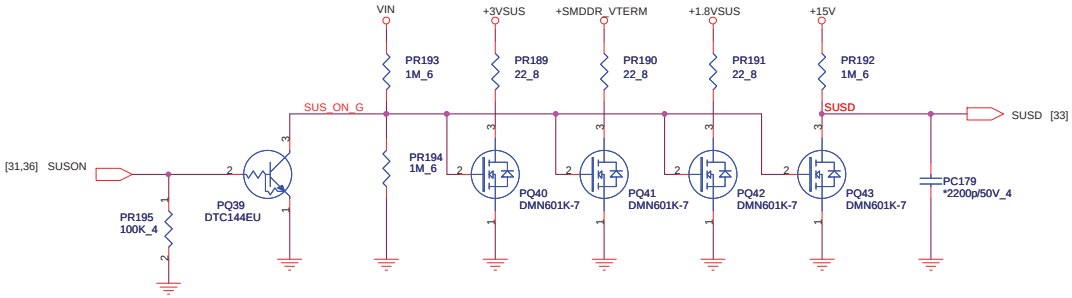
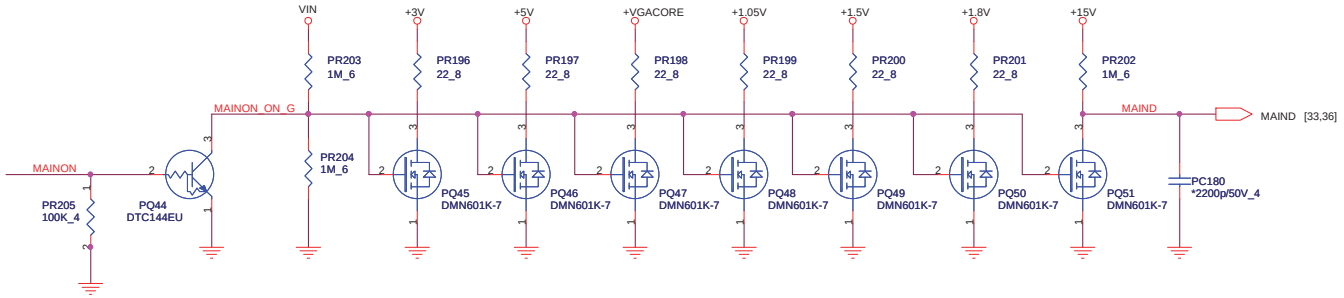
PROJECT : ZR6E

Size	Document Number	Rev
	VGA M92LP (OZ8118)	1A
Date: Wednesday, May 20, 2009	Sheet 36 of 39	









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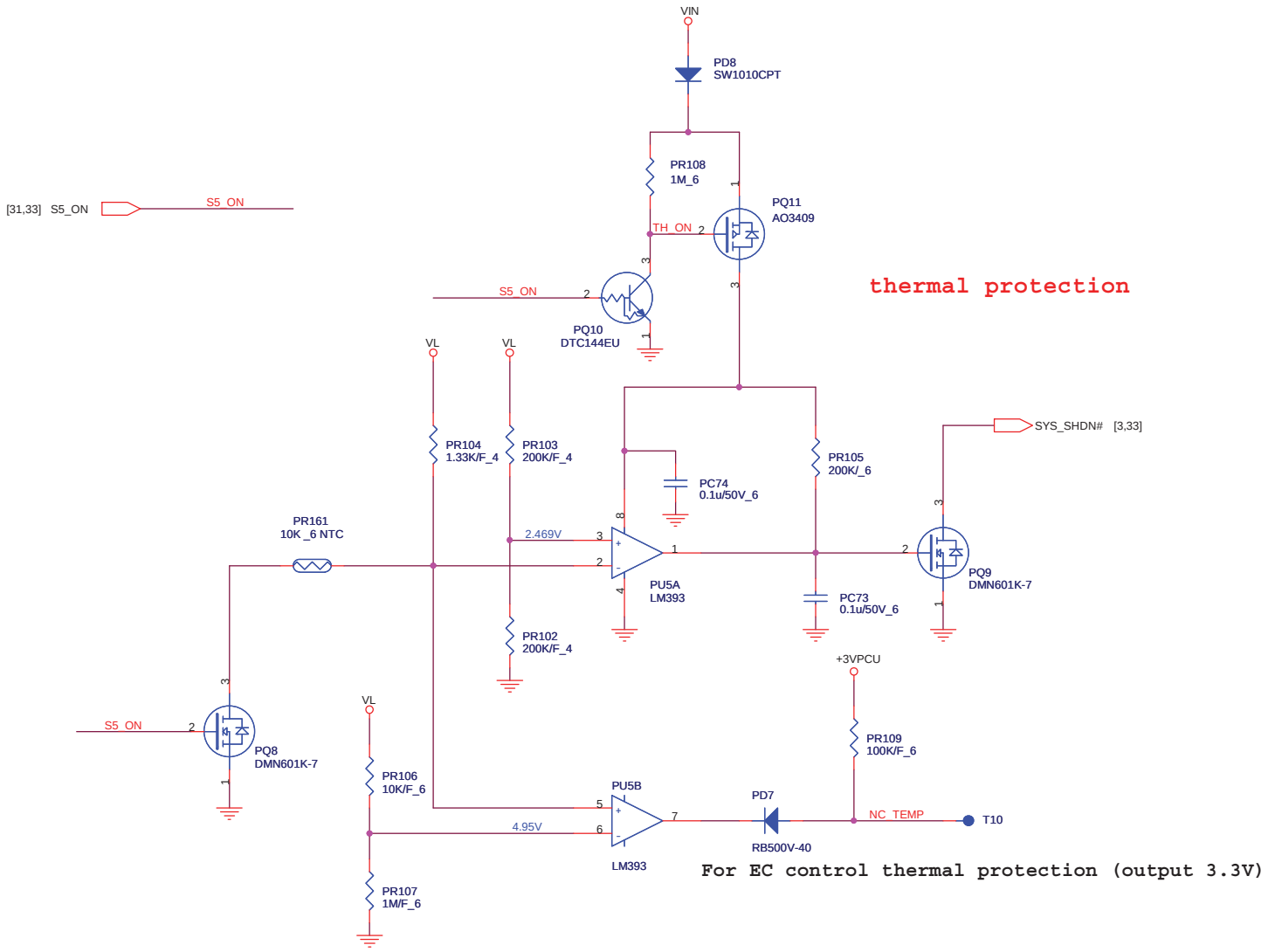
PROJECT : ZR6E

Size	Document Number	Rev
	Discharge	1A

Date: Tuesday, May 19, 2009 Sheet 37 of 39



Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: Thermal Protection	Rev 1A
Date: Tuesday, May 19, 2009	Sheet 38 of 39	

MODEL: REV

CHANGE LIST

ZR6 MB

PAGE \ MODEL	ZR6 MB FROM	ZR6 MB TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

MB Assy' P/N: 31ZR6MB00B0,C0,D0,E0,F0,G0

Project : ZR6E MB

Document No.:

Approved by :

Drawing by : James Chen

DATE:

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	Thermal Protection	1A

Date: Tuesday, May 19, 2009 Sheet 39 of 39