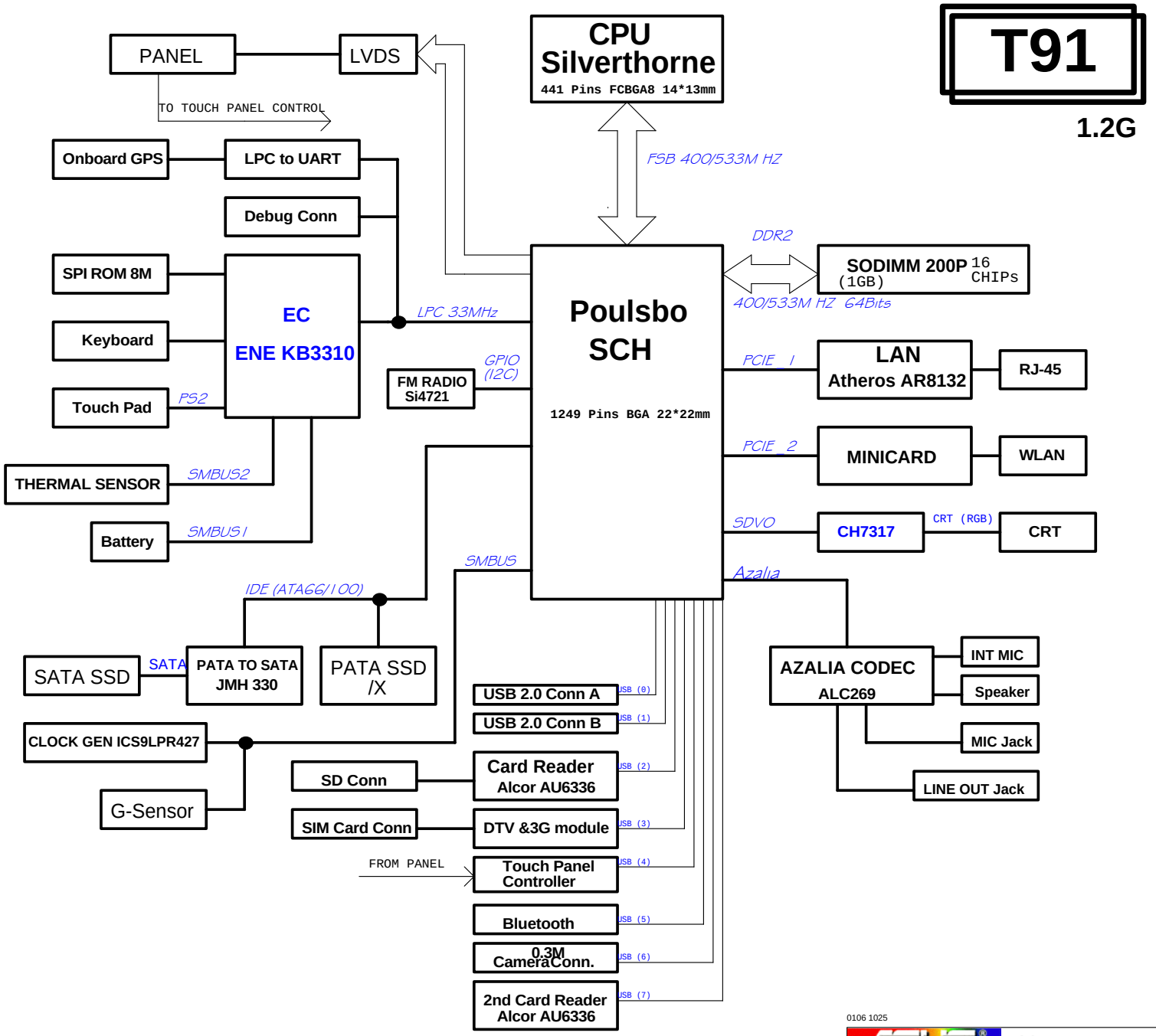

0106 1025

Title : Block Diagram

Engineer: Jerry Liu

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 1 of 57

SCH GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOSUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOSUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
N45	GPIOSUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOSUS3/ USBCC	Test Point	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	PCB ID	I/O CMOS3.3	Core	OFF	OFF	Input
F34	GPIO2	GPS_EN	I/O CMOS3.3	Core	OFF	OFF	Output
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

0106 1025

ASUSTek Computer INC.

Title : SCH GPIO Setting

Engineer: Jerry Liu

Size	Project Name	Rev
A3	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 2 of 57

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	BUF_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Battery over temperature
15	GPIO08	EXT_SMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	Reserved for GPIO extender
18	GPIO0C/ESB_DAT	NC	O	Reserved for GPIO extender
19	GPIO0D	LID_EC_R#	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A	I	
64	GPI39/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	Batt1 (Small/Internal): 1-present, 0-absent
76	GPI43	BAT2_IN	I	Batt2 (Small/Internal): 1-present, 0-absent
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	N.C.	O	
85	GPIO4C/PSCLK2	N.C.	O	
86	GPIO4D/PSDAT2	GS2_INT2	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	GS1_INT1	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPXOA06	CNT1_DIS#	O	batt1 discharging enabled
104	GPXOA07	CNT2_CHG#	O	batt2 (Small/Internal) charging enabled. Batt2 is charging priority in AC mode.
105	GPXOA08	CNT2_CHG#	O	batt2 discharging enabled
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#,100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#,100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

0106 1025

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Jerry Liu

Size	Project Name	Rev
A3	T91	1.2G

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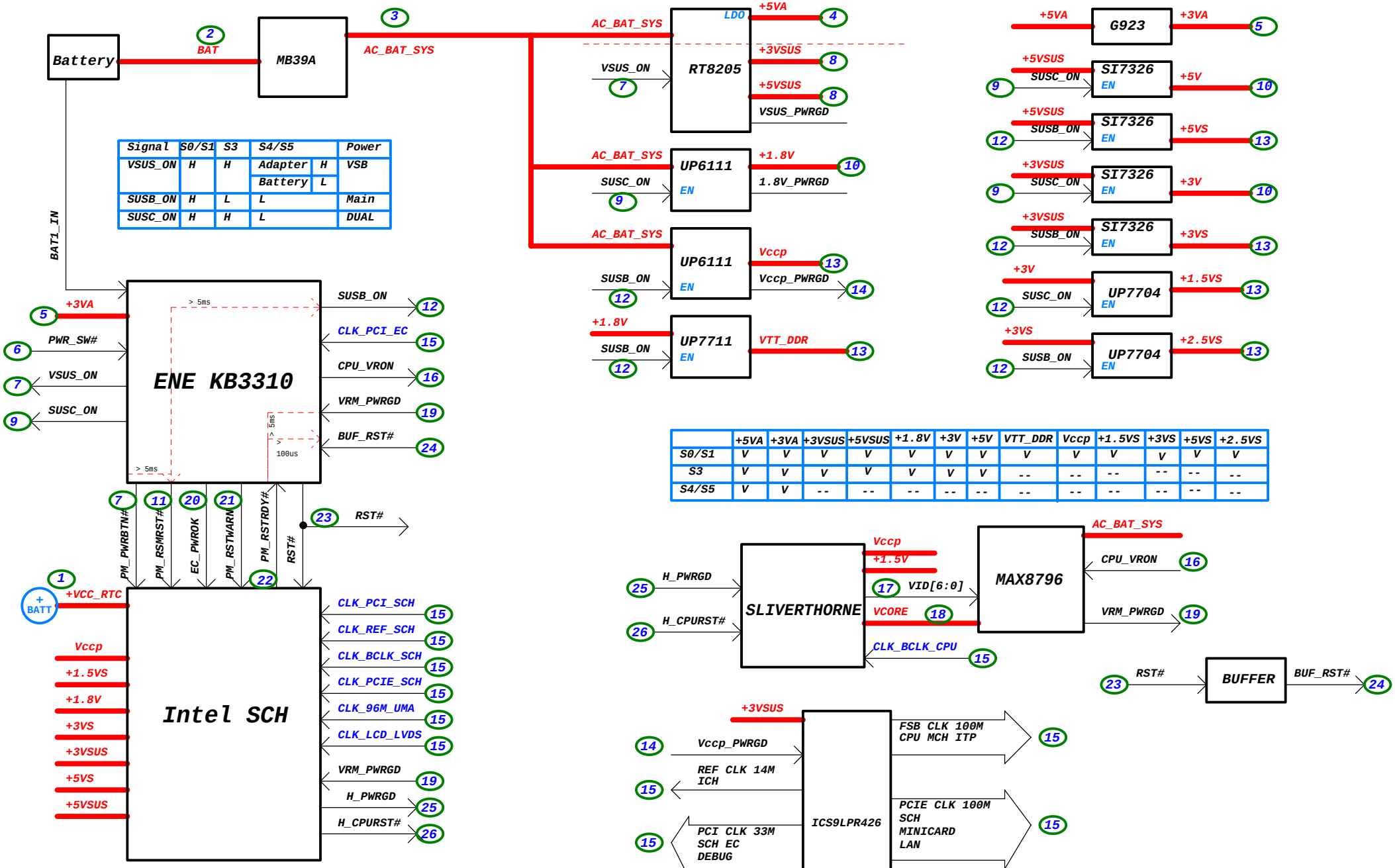


Signal	S0/S1	S3	S4/S5		Power
VSUS_ON	H	H	Adapter	H	VSB
			Battery	L	
SUSB_ON	H	L	L		Main
SUSC_ON	H	H	L		DUAL

	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	--	--	--	--	--	--	--	--	--	--	--

0106 1025

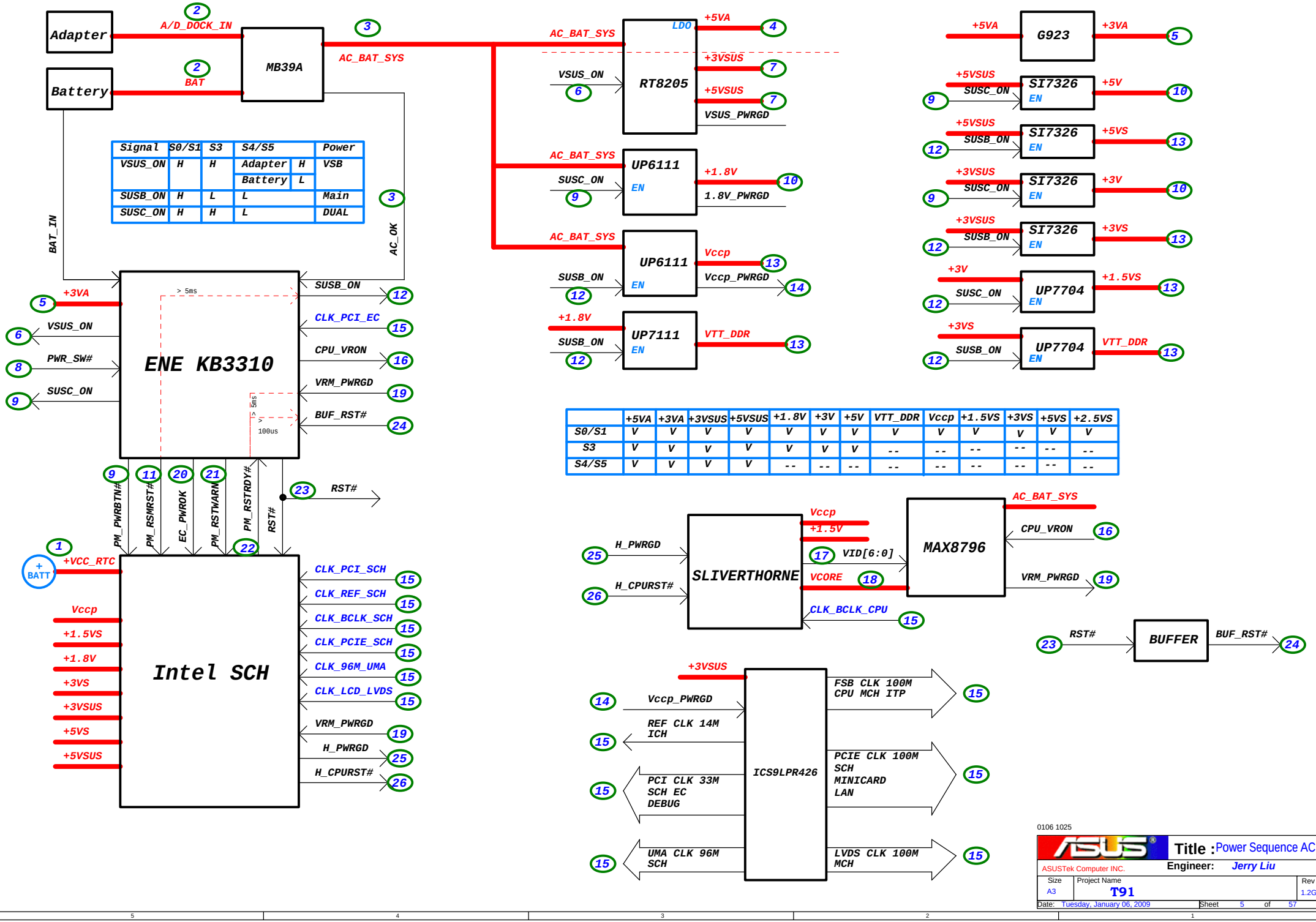
ASUSTek Computer INC.

Title : Power Sequence DC

Engineer: Jerry Liu

Size	Project Name	Rev
A3	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 4 of 57


Adapter
Battery
A/D_DOCK_IN
BAT
MB39A
AC_BAT_SYS
BAT_IN
AC_OK
Signal | S0/S1 | S3 | S4/S5 | Power
VSUS_ON | H | H | Adapter H | VSB
Battery L
SUSB_ON | H | L | L | Main
SUSC_ON | H | H | L | DUAL
ENE KB3310
> 5ms
> 5ms
100us
+3VA
VSUS_ON
PWR_SW#
SUSC_ON
SUSB_ON
CLK_PCI_EC
CPU_VRON
VRM_PWRGD
BUF_RST#
PM_PWRBTN#
PM_RSMRST#
EC_PWROK
PM_RSTWARN
PM_RSTRDY#
RST#
+VCC_RTC
BATT
Intel SCH
Vccp
+1.5VS
+1.8V
+3VS
+3VSUS
+5VS
+5VSUS
CLK_PCI_SCH
CLK_REF_SCH
CLK_BCLK_SCH
CLK_PCIE_SCH
CLK_96M_UMA
CLK_LCD_LVDS
VRM_PWRGD
H_PWRGD
H_CPURST#
AC_BAT_SYS
VSUS_ON
RT8205
LDO
+5VA
+3VSUS
+5VSUS
VSUS_PWRGD
SUSC_ON
UP6111
EN
+1.8V
1.8V_PWRGD
SUSB_ON
UP6111
EN
Vccp
Vccp_PWRGD
+1.8V
SUSB_ON
UP7111
EN
VTT_DDR
+5VA
G923
+3VA
+5VSUS
SUSC_ON
SI7326
EN
+5V
+5VSUS
SUSB_ON
SI7326
EN
+5VS
+3VSUS
SUSC_ON
SI7326
EN
+3V
+3VSUS
SUSB_ON
SI7326
EN
+3VS
+3V
SUSC_ON
UP7704
EN
+1.5VS
+3VS
SUSB_ON
UP7704
EN
VTT_DDR
+5VA | +3VA | +3VSUS | +5VSUS | +1.8V | +3V | +5V | VTT_DDR | Vccp | +1.5VS | +3VS | +5VS | +2.5VS
S0/S1 | V | V | V | V | V | V | V | V | V | V | V | V | V
S3 | V | V | V | V | V | V | V | -- | -- | -- | -- | -- | -- | --
S4/S5 | V | V | V | V | -- | -- | -- | -- | -- | -- | -- | -- | -- | --
H_PWRGD
H_CPURST#
SLIVERTHORNE
Vccp
+1.5V
VID[6:0]
VCORE
CLK_BCLK_CPU
MAX8796
AC_BAT_SYS
CPU_VRON
VRM_PWRGD
RST#
BUFFER
BUF_RST#
+3VSUS
Vccp_PWRGD
REF CLK 14M
ICH
PCI CLK 33M
SCH EC
DEBUG
UMA CLK 96M
SCH
ICS9LPR426
FSB CLK 100M
CPU MCH ITP
PCIE CLK 100M
SCH
MINICARD
LAN
LVDS CLK 100M
MCH
0106 1025
Title : Power Sequence AC
ASUSTek Computer INC.
Engineer: Jerry Liu
Size A3
Project Name T91
Rev 1.2G
Date: Tuesday, January 06, 2009
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S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for AC_OK until adaptor power is good, then

2.At least 5mS after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.

3.At least 20mS after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)

4.EC asserts RSTWARN.

5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

6.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

7.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

8.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

10.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

11.Waiting for RSTRDY# until deasserted by SCH.

12.RESET# can be deasserted at lease 100uS after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for BAT_IN until battery power is good, then

2.Waiting for PWR_SW# until user is pressed.

3.EC asserts VSUS_ON to enable VSUS power.

4.At least 20mS after VSUS power is stable.

5.EC asserts RSTWARN.

6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.

10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

12.Waiting for RSTRDY# until deasserted by SCH.

13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).

2.At least 20mS after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.

3.Waiting for SLPRDY# until has been asserted.

4.EC asserts RSTWARN to SCH to begin internal sequence.

5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.

6.EC asserts RESET# after detecting RSTRDY# asserted.

7.EC deasserts ICH_PWROK.

8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

9.EC asserts PM_RSMRST#.

10.EC deasserts SUSC_ON to turn off the other power planes.

11.EC deasserts VSUS_ON if in battery mode.

12.EC deasserts RSTWARN to save more power.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.

2.For external wake event (PWR_SW#, keyboard wake up), then

3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.

4.EC asserts SUSB_ON to enable SUSB power.

5.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

7.At least 5mS after receiving CPUPWR_GD, ICH_PWROK is asserted.

8.Deasserts RSTWARN after ICH_PWROK is asserted.

9.RESET# can be deasserted 100uS after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.

2.EC asserts RSTWARN to SCH.

3.EC asserts RESET# for 1200mS to SCH after asserts RSTWARN.

4.EC deasserts RSTWARN.

5.EC deasserts RESET# after at least 100uS delay from RSTWARN.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.

2.EC asserts RSTWARN to SCH.

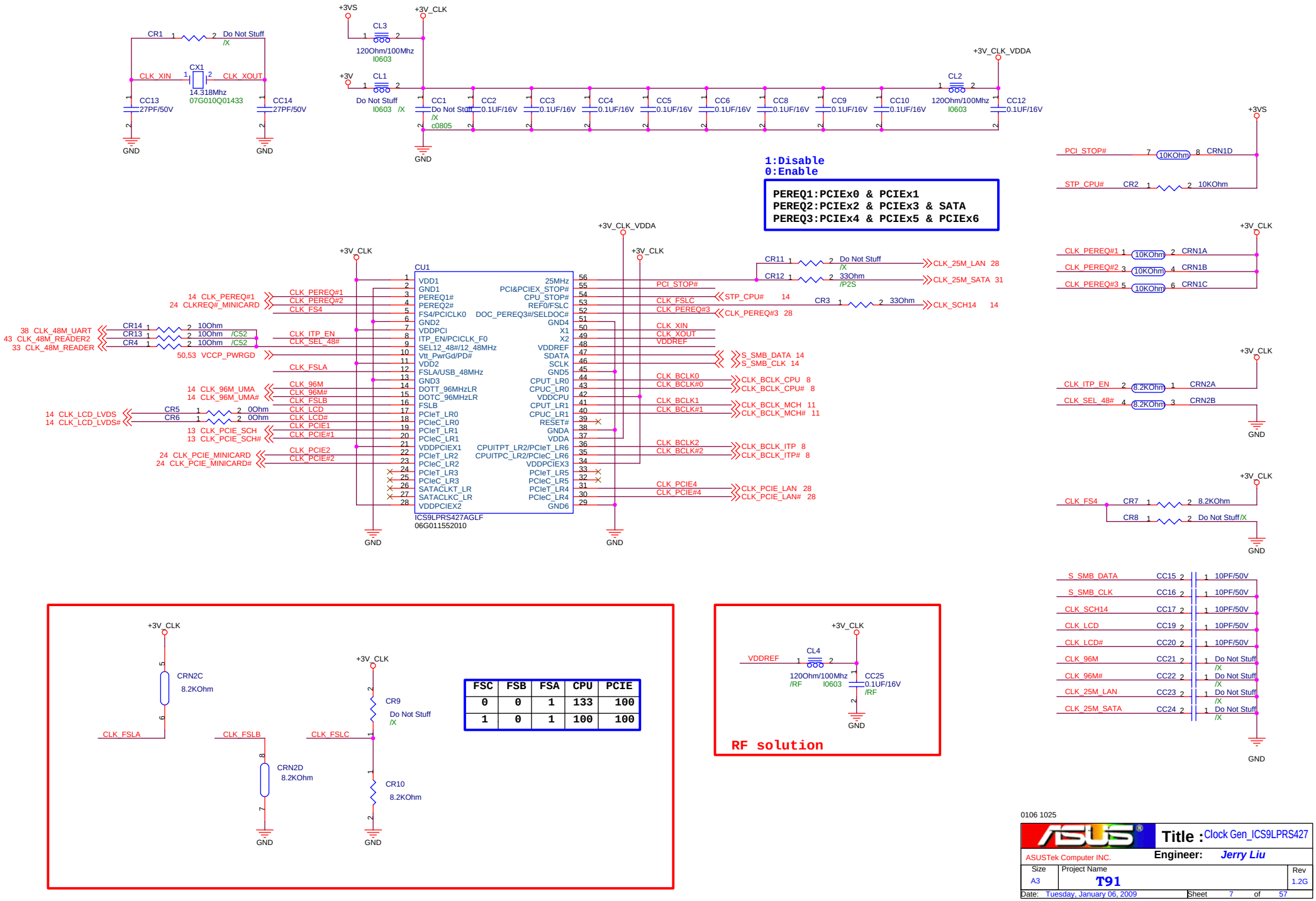
3.EC asserts RESET# to SCH after asserts RSTWARN.

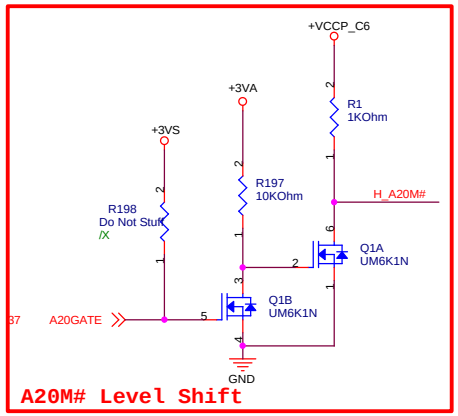
4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.

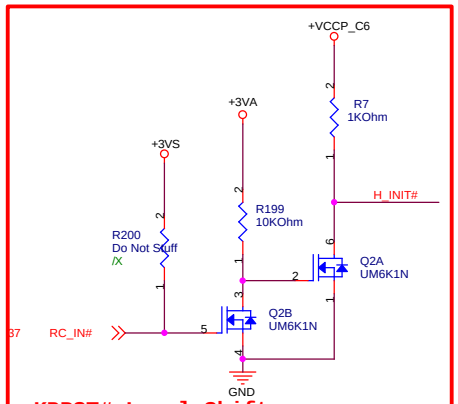
5.EC asserts PM_RSMRST# after CPU_VRON power is off.

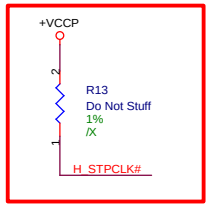
6.EC disables SUSC_ON power for 3~5 seconds.

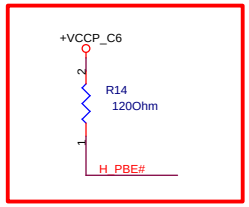
7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.

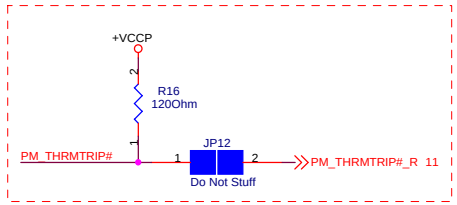

CR1 Do Not Stuff /X
CX1 14.318Mhz 07G010Q01433
CLK_XIN
CLK_XOUT
CC13 27PF/50V
CC14 27PF/50V
GND
+3VS
+3V_CLK
CL3 120Ohm/100Mhz l0603
+3V
CL1 Do Not Stuff l0603 /X
CC1 Do Not Stuff /X c0805
CC2 0.1UF/16V
CC3 0.1UF/16V
CC4 0.1UF/16V
CC5 0.1UF/16V
CC6 0.1UF/16V
CC8 0.1UF/16V
CC9 0.1UF/16V
CC10 0.1UF/16V
+3V_CLK_VDDA
CL2 120Ohm/100Mhz l0603
CC12 0.1UF/16V
1:Disable
0:Enable
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6
CU1
VDD1
GND1
PEREQ1#
PEREQ2#
FS4/PCICLK0
GND2
VDDPCI
ITP_EN/PCICLK_F0
SEL12_48#/12_48MHz
Vtt_PwrGd/PD#
VDD2
FSLA/USB_48MHz
GND3
DOTT_96MHzLR
DOTC_96MHzLR
FSLB
PCIeT_LR0
PCIeC_LR0
PCIeT_LR1
PCIeC_LR1
VDDPCIEX1
PCIeT_LR2
PCIeC_LR2
PCIeT_LR3
PCIeC_LR3
SATACLKT_LR
SATACLKC_LR
VDDPCIEX2
25MHz
PCI&PCIEX_STOP#
CPU_STOP#
REF0/FSLC
DOC_PEREQ3#/SELDOC#
GND4
X1
X2
VDDREF
SDATA
SCLK
GND5
CPUT_LR0
CPUC_LR0
VDDCPU
CPUT_LR1
CPUC_LR1
RESET#
GNDA
VDDA
CPUITPT_LR2/PCIeT_LR6
CPUITPC_LR2/PCIeC_LR6
VDDPCIEX3
PCIeT_LR5
PCIeC_LR5
PCIeT_LR4
PCIeC_LR4
GND6
ICS9LPRS427AGLF
06G011552010
14 CLK_PEREQ#1
24 CLKREQ#_MINICARD
CLK_PEREQ#1
CLK_PEREQ#2
CLK_FS4
38 CLK_48M_UART
43 CLK_48M_READER2
33 CLK_48M_READER
CR14 10Ohm
CR13 10Ohm /C52
CR4 10Ohm /C52
CLK_ITP_EN
CLK_SEL_48#
50,53 VCCP_PWRGD
CLK_FSLA
14 CLK_96M_UMA
14 CLK_96M_UMA#
CLK_96M
CLK_96M#
CLK_FSLB
14 CLK_LCD_LVDS
14 CLK_LCD_LVDS#
CR5 0Ohm
CR6 0Ohm
CLK_LCD
CLK_LCD#
13 CLK_PCIE_SCH
13 CLK_PCIE_SCH#
CLK_PCIE1
CLK_PCIE#1
24 CLK_PCIE_MINICARD
24 CLK_PCIE_MINICARD#
CLK_PCIE2
CLK_PCIE#2
PCI_STOP#
STP_CPU# 14
CLK_FSLC
CLK_PEREQ#3
CLK_PEREQ#3 28
CLK_XIN
CLK_XOUT
VDDREF
S_SMB_DATA 14
S_SMB_CLK 14
CLK_BCLK0
CLK_BCLK#0
CLK_BCLK_CPU 8
CLK_BCLK_CPU# 8
CLK_BCLK1
CLK_BCLK#1
CLK_BCLK_MCH 11
CLK_BCLK_MCH# 11
CLK_BCLK2
CLK_BCLK#2
CLK_BCLK_ITP 8
CLK_BCLK_ITP# 8
CLK_PCIE4
CLK_PCIE#4
CLK_PCIE_LAN 28
CLK_PCIE_LAN# 28
CR11 Do Not Stuff /X
CR12 33Ohm /P2S
CLK_25M_LAN 28
CLK_25M_SATA 31
CR3 33Ohm
CLK_SCH14 14
PCI_STOP# 10KOhm CRN1D
STP_CPU# CR2 10KOhm
CLK_PEREQ#1 10KOhm CRN1A
CLK_PEREQ#2 10KOhm CRN1B
CLK_PEREQ#3 10KOhm CRN1C
CLK_ITP_EN 8.2KOhm CRN2A
CLK_SEL_48# 8.2KOhm CRN2B
CLK_FS4 CR7 8.2KOhm
CR8 Do Not Stuff /X
S_SMB_DATA CC15 10PF/50V
S_SMB_CLK CC16 10PF/50V
CLK_SCH14 CC17 10PF/50V
CLK_LCD CC19 10PF/50V
CLK_LCD# CC20 10PF/50V
CLK_96M CC21 Do Not Stuff /X
CLK_96M# CC22 Do Not Stuff /X
CLK_25M_LAN CC23 Do Not Stuff /X
CLK_25M_SATA CC24 Do Not Stuff /X
CRN2C 8.2KOhm
CRN2D 8.2KOhm
CR9 Do Not Stuff /X
CR10 8.2KOhm
FSC FSB FSA CPU PCIE
0 0 1 133 100
1 0 1 100 100
VDDREF CL4 120Ohm/100Mhz /RF l0603
CC25 0.1UF/16V /RF
RF solution
0106 1025
Title : Clock Gen_ICS9LPRS427
ASUSTek Computer INC.
Engineer: Jerry Liu
Size A3
Project Name T91
Rev 1.2G
Date: Tuesday, January 06, 2009
Sheet 7 of 57

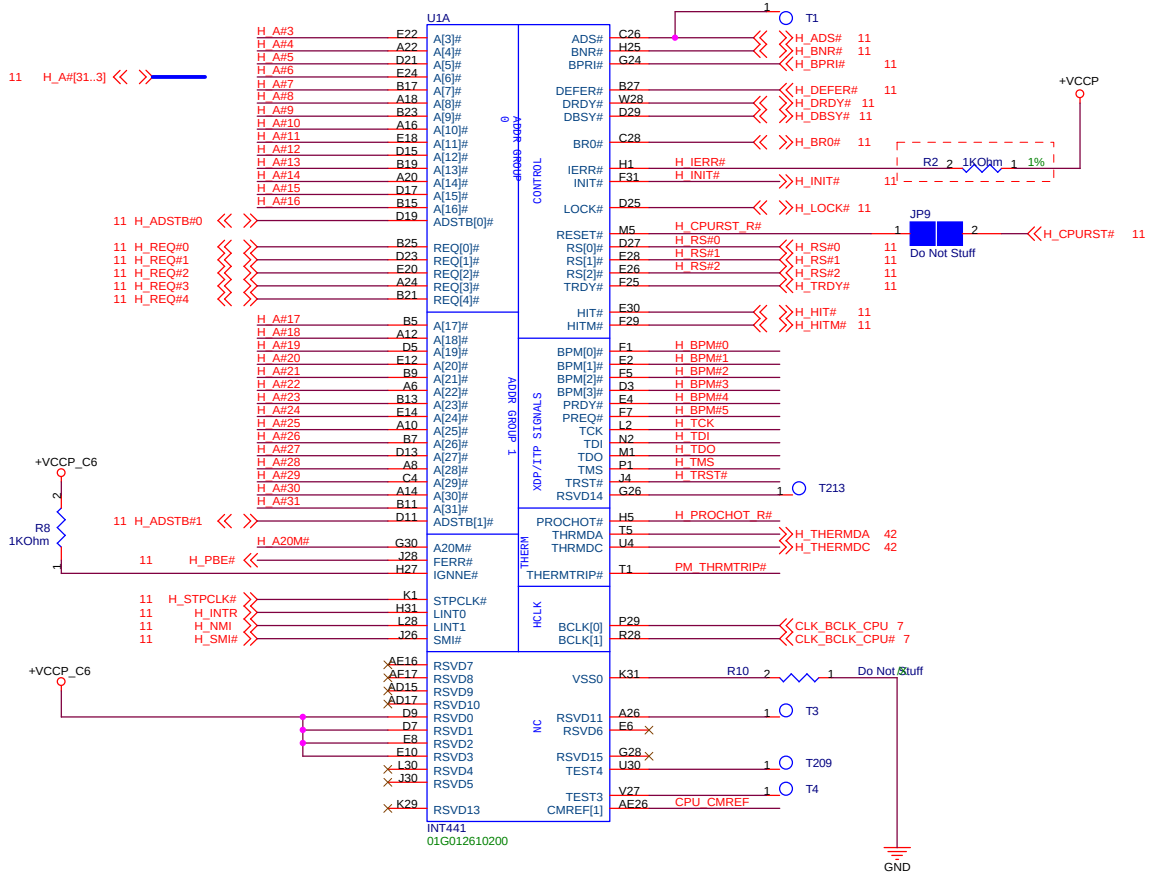




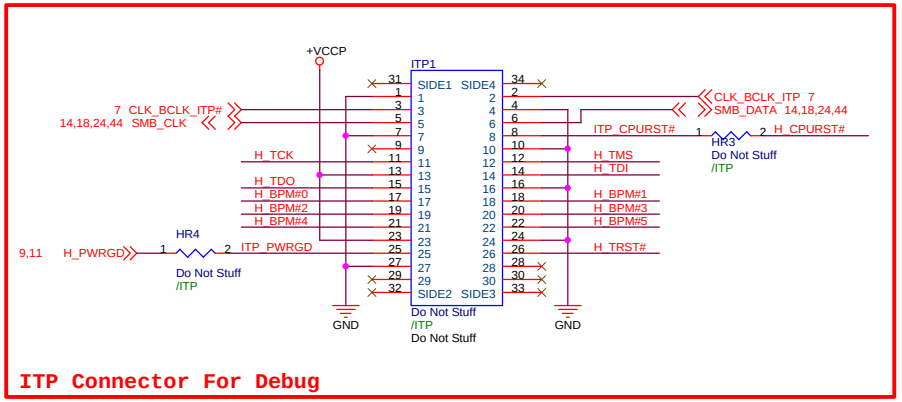


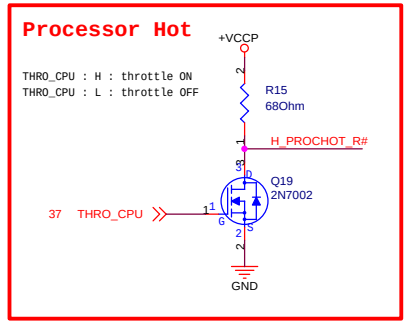


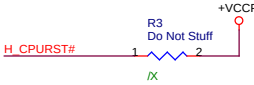


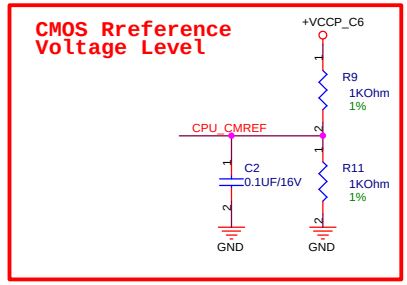


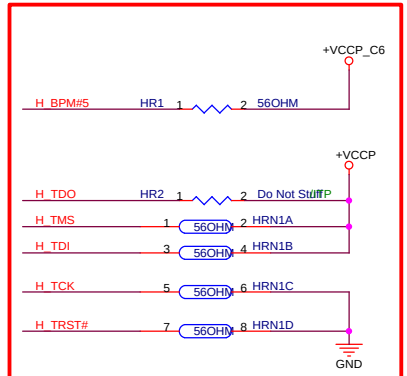
Z530 : 01G011980000
Z520 C0 stage : 01G012610200

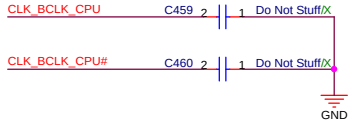






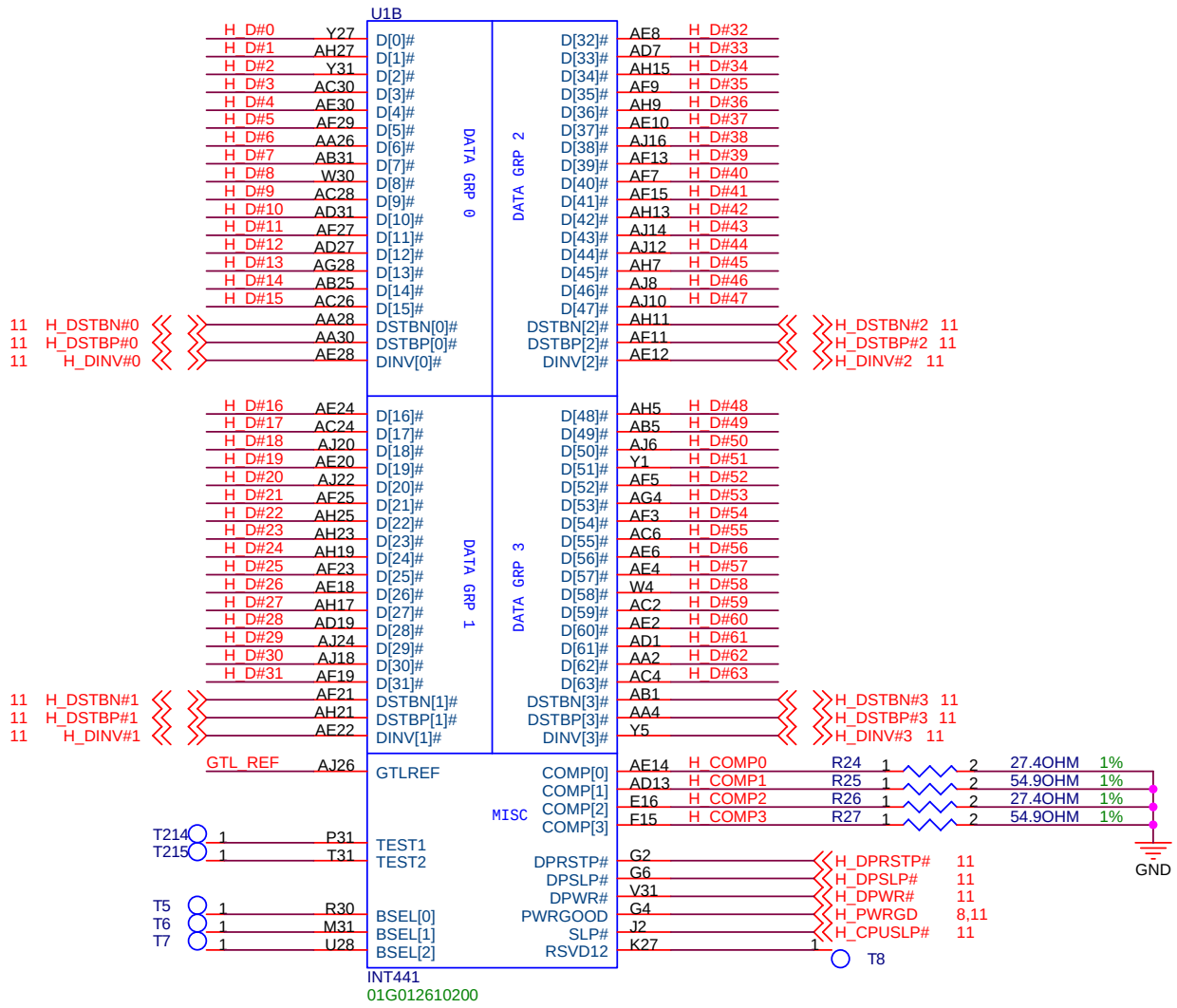




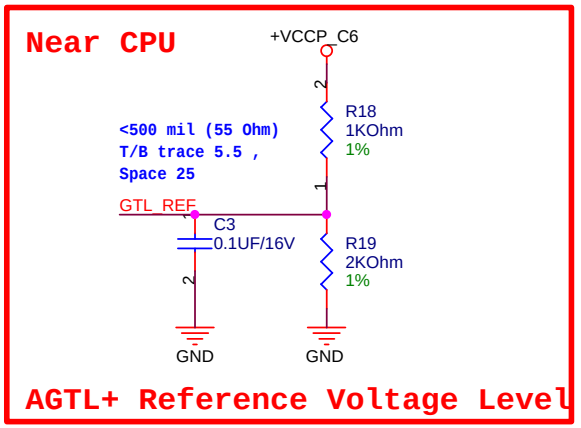


0106 1025

ASUSTeK COMPUTER INC	Title : CPU-SLIVERTHORNE(1)	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 8 of 57	



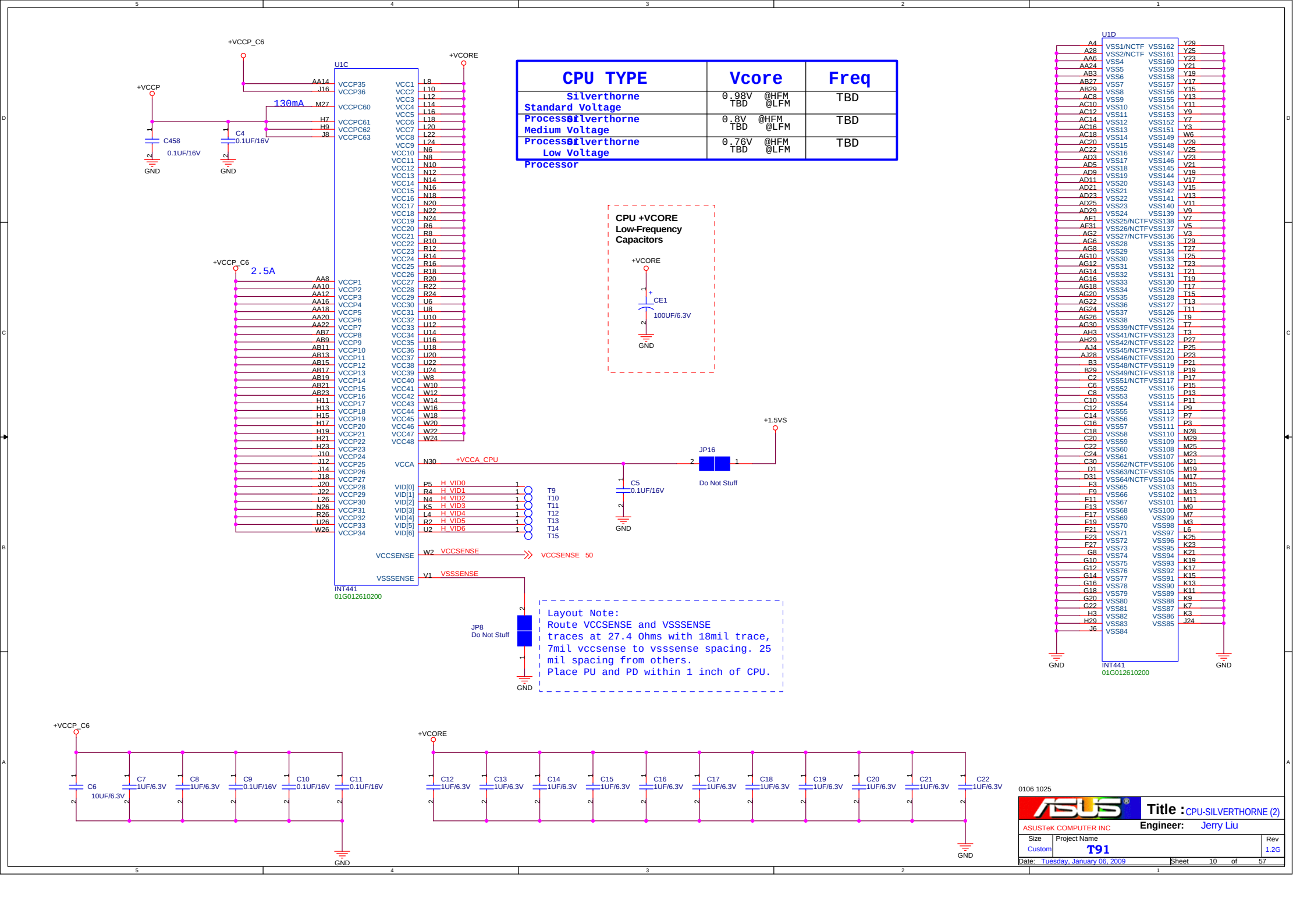
H_D#[63:0] H_D#[63:0] 11



Layout Note
COMP 0 2 connect with Z0=27.4 ohm,L<0.5"
COMP 1 3 connect with Z0=55 ohm,L<0.5"

0106 1025

ASUSTeK COMPUTER INC	Title : CPU-SLIVERTHORNE(1)	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 9 of 57	



CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage Processor	0.98V @HFM TBD @LFM	TBD
Silverthorne Medium Voltage Processor	0.8V @HFM TBD @LFM	TBD
Silverthorne Low Voltage Processor	0.76V @HFM TBD @LFM	TBD

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 18mil trace, 7mil vccsense to vsssense spacing. 25 mil spacing from others.
Place PU and PD within 1 inch of CPU.

0106 1025

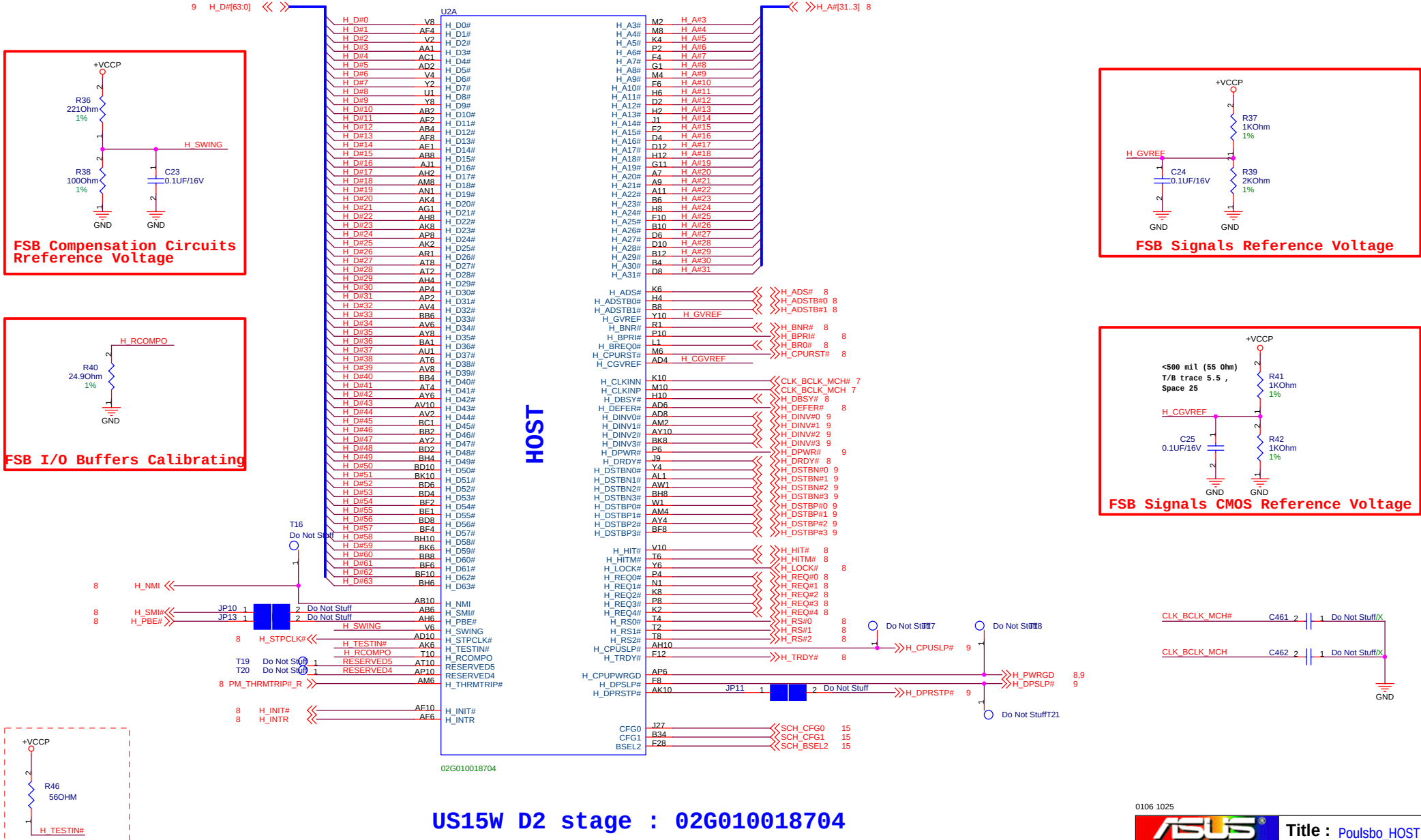
ASUSTeK COMPUTER INC

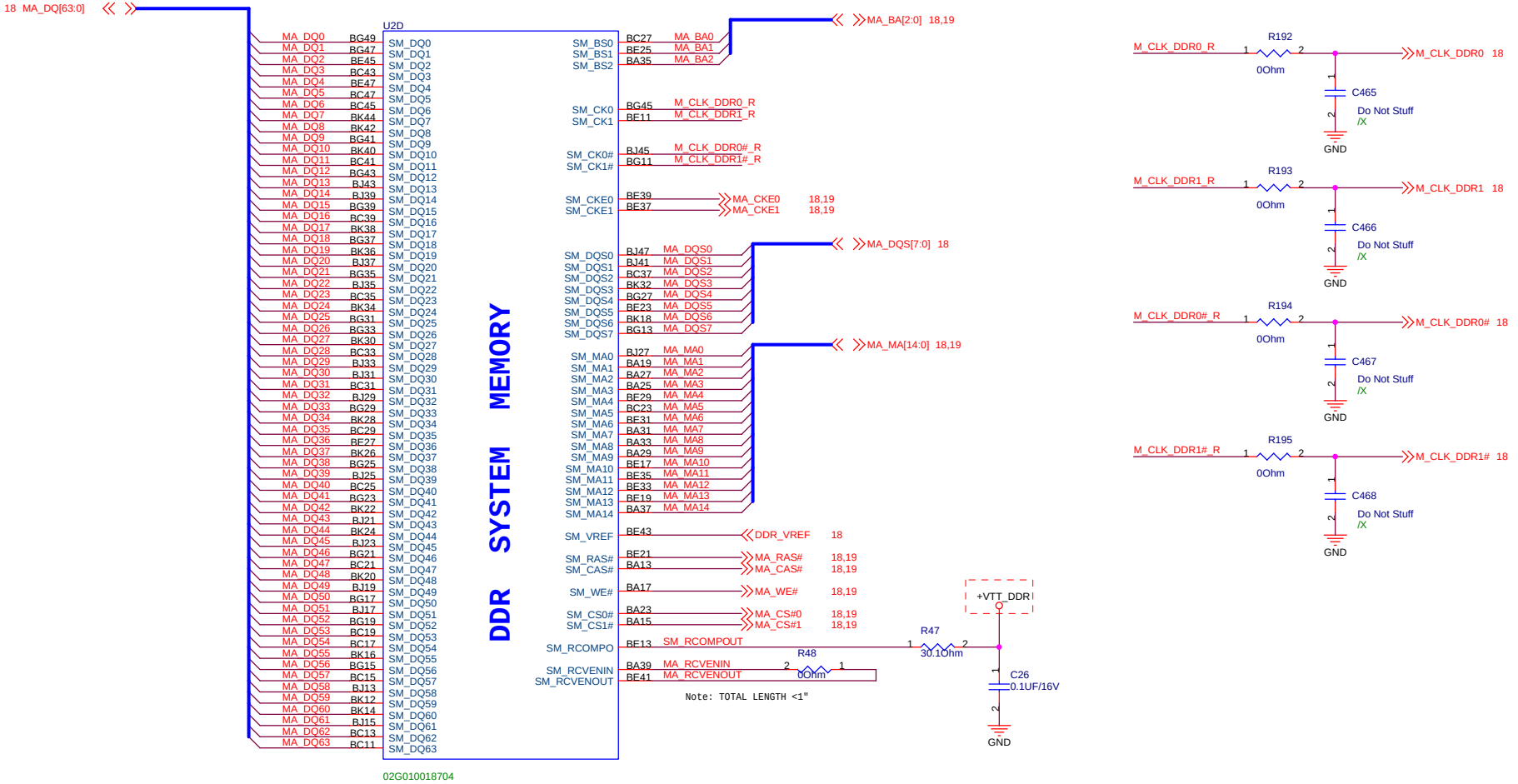
Title : CPU-SILVERTHORNE (2)

Engineer: Jerry Liu

Size	Project Name	Rev
Custom	T91	1.2G

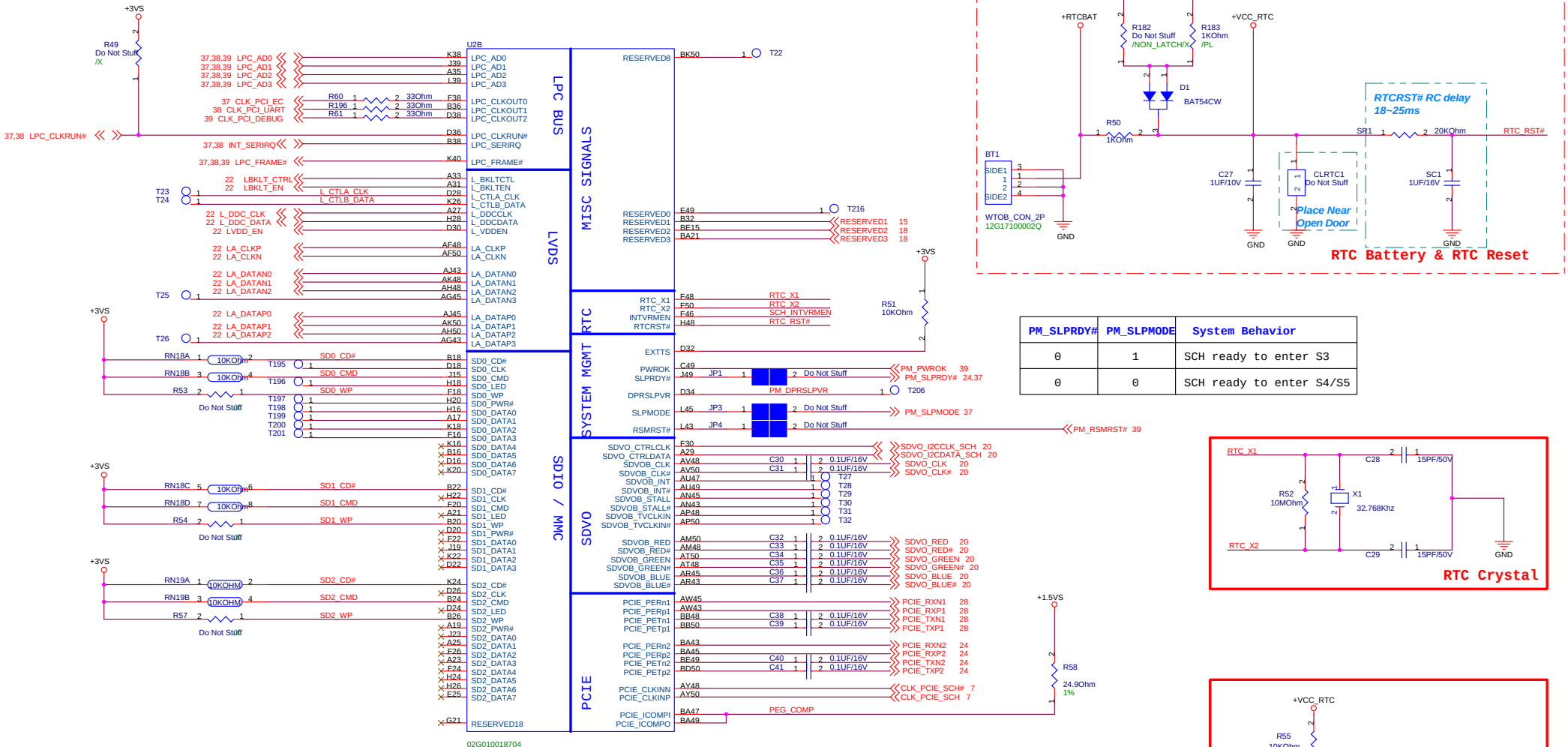
Date: Tuesday, January 06, 2009 Sheet 10 of 57


FSB Compensation Circuits
Rreference Voltage
FSB I/O Buffers Calibrating
FSB Signals Reference Voltage
FSB Signals CMOS Reference Voltage
HOST
U2A
02G010018704
US15W D2 stage : 02G010018704
Title : Poulsbo_HOST (1)
ASUSTeK COMPUTER INC
Engineer: Jerry Liu
Project Name
T91
Rev
1.2G
Date: Tuesday, January 06, 2009
Sheet 11 of 57



0106 1025

ASUSTek Computer INC.	Title : Poulsbo_DDR2 (2)	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 12 of 57	



PM_SLPRDY#	PM_SLPMODE	System Behavior
0	1	SCH ready to enter S3
0	0	SCH ready to enter S4/S5

0106 1025

ASUSTeK COMPUTER INC	Title : Poulsbo_LVDS/SDVO	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 13 of 57	

USB 0	USB PORT
USB 1	USB PORT
USB 2	Card Reader
USB 3	3.5G
USB 4	Touch Panel
USB 5	Bluetooth
USB 6	Camera
USB 7	2'nd Card Reader

U2C

USB I/F

32 USB_PN0 — AE47 USB_DN0
32 USB_PP0 — AE49 USB_DP0
32 USB_PN1 — AD48 USB_DN1
32 USB_PP1 — AD50 USB_DP1
33 USB_PN2 — AB50 USB_DN2
33 USB_PP2 — AB48 USB_DP2
23 USB_PN3 — AA49 USB_DN3
23 USB_PP3 — AA47 USB_DP3
43 USB_PN4 — Y48 USB_DN4
43 USB_PP4 — Y50 USB_DP4
25 USB_PN5 — V50 USB_DN5
25 USB_PP5 — V48 USB_DP5
34 USB_PN6 — U47 USB_DN6
34 USB_PP6 — U49 USB_DP6
43 USB_PN7 — T50 USB_DN7
43 USB_PP7 — T48 USB_DP7

32 USB_OC#0 — R43 USB_OC#0 — USB_OC0#
32 USB_OC#1 — W45 USB_OC#1 — USB_OC1#
R45 USB_OC#2 — USB_OC2#
U43 USB_OC#3 — USB_OC3#
AA45 USB_OC#4 — USB_OC4#
AA43 USB_OC#5 — USB_OC5#
W43 USB_OC#6 — USB_OC6#
U45 USB_OC#7 — USB_OC7#

+3V — R66 10KOhm

AC45 USB_RBIASN
USBRBIAS_PN — AC43 USB_RBIASP

Termination Voltage

<583mA

+VCCP

VTT_1 AW13
VTT_2 AV12
VTT_3 AU13
VTT_4 AT12
VTT_5 AR13
VTT_6 AP12
VTT_7 AN13
VTT_8 AM12
VTT_9 AL13
VTT_10 AK12
VTT_11 AJ13
VTT_12 AH12
VTT_13 AG13
VTT_14 AE12
VTT_15 AE13
VTT_16 AC13
VTT_17 AB12
VTT_18 AA13
VTT_19 Y12
VTT_20 W13
VTT_21 V12
VTT_22 U13
VTT_23 T12
VTT_24 R13
VTT_25 P12
VTT_26 N13
VTT_27 M14
VTT_28 M12
VTT_29 AD12

+VCCP — C42 10UF/6.3V — C43 1UF/6.3V — C44 1UF/6.3V — C45 0.1UF/16V — C46 0.1UF/16V — GND

PATA/IDE

30,31 IDE_DDREQ — J43 PATA_DDREQ
30,31 IDE_IORDY — D46 PATA_IORDY
30,31 IDE_IRQ — G45 PATA_IDEIRQ
30,31 IDE_DDACK# — B46 PATA_DDACK#
30,31 IDE_DIOW# — A37 PATA_DIOW#
30,31 IDE_DIOR# — F44 PATA_DIOR#
30,31 IDE_DCS#3 — C47 PATA_DCS3#
30,31 IDE_DCS#1 — E47 PATA_DCS1#

IDE_DA2 — K42 PATA_DA2
IDE_DA1 — J45 PATA_DA1
IDE_DA0 — H40 PATA_DA0

IDE_DD15 — B40 PATA_DD15
IDE_DD14 — E43 PATA_DD14
IDE_DD13 — H42 PATA_DD13
IDE_DD12 — D42 PATA_DD12
IDE_DD11 — F40 PATA_DD11
IDE_DD10 — A43 PATA_DD10
IDE_DD9 — A41 PATA_DD9
IDE_DD8 — J41 PATA_DD8
IDE_DD7 — A39 PATA_DD7
IDE_DD6 — B42 PATA_DD6
IDE_DD5 — F42 PATA_DD5
IDE_DD4 — D44 PATA_DD4
IDE_DD3 — L41 PATA_DD3
IDE_DD2 — B44 PATA_DD2
IDE_DD1 — G43 PATA_DD1
IDE_DD0 — D40 PATA_DD0

30,31 IDE_DD[15:0] — IDE_DD[15:0]
30,31 IDE_DA[2:0] — IDE_DA[2:0]

JTAG

TRST# N49 — SCH_TRST# — R67 2 1 10KOhM — +VCCP
TMS M50 — SCH_TMS — 1 T36
TDI K48 — XDP_TDI_SCH — 1 T37
TDO M48 — XDP_TDO — 1 T38
TCK N47 — XDP_TCK_1 — 1 T39

SYSTEM GPIOs

STPCPU# H30 — STP_CPU# 7
RSTRDY# H50 — PM_RSTRDY# 37
RESET# BA41 — RST# 37,40
RSTWARN K50 — PM_RSTWARN 37
GPIOSUS0 U41 — PM_LEVELDOWN# 51,52,53,54
GPIOSUS1 N43 — CPU_LEVELDOWN# 50
GPIOSUS2 N45 — PM_PWRBTN# 37
GPIOSUS3 R41 — CARD_READER_EN# 33,43

WAKE# N41 — PCIE_WAKE# 24,28
SMI# B30 — EXTSMI# 37
THRM# F22 — PM_THRM#
GPE# P50 — KBC_SCI# 37
BT_DIS# 25
R175 1 2 0Ohm
GPIO0 G29 — SCH_GPIO_0 15 — PCB_ID0
GPIO1 K30
GPIO2 F34 — GPS_EN 27
GPIO3 G33 — SCH_GPIO_3 15
GPIO4 K36 — 3GLAN_OFF 23
GPIO5 H36 — MINICARD_EN# 24
GPIO6 F36 — DDR_MEM_CONFIG 15
GPIO7 J31 — SLPIOVR# 56
GPIO8 H34 — CAMERA_EN 34
GPIO9 K28 — WLAN_LED 43

HD AUDIO

SPKR J35 — SB_SPKR 35
HDA_CLK K14 — 33OHM — RN15A — A_Z_BITCLK 35
HDA_SYNC E13 — 33OHM — RN15B — A_Z_SYNC 35
HDA_RST# A13 — 33OHM — RN15C — A_Z_RST# 35
HDA_SDI0 F14 — A_Z_SDIN0 35
HDA_SDI1 B14 — T40
HDA_SDO D14 — 33OHM — RN15D — A_Z_SDOUT 35
HDA_DOCKEN# E15 — T41
HDA_DOCKRST# H14 — T42

CLOCK I/F

RESERVED6 AU43 — T210
RESERVED7 AU45 — T211
DA_REFCLKINN AL45 — CLK_96M_UMA# 7
DA_REFCLKINP AL43 — CLK_96M_UMA 7
DB_REFCLKINNSSC AE45 — CLK_LCD_LVDS# 7
DB_REFCLKINPSSC AE43 — CLK_LCD_LVDS 7
CLKREQ# B28 — R82 Do Not Stuff — CLK_PEREQ#1 7
CLK14 H32 — CLK_SCH14 7
USB_CLK48 W41
SUSCLK J47 — SUSCLK — T43

SMB

SMB_ALERT# K32 — SMB_ALERT#
SMB_DATA G37 — S_SMB_DATA — S_SMB_DATA 7
SMB_CLK H38 — S_SMB_CLK — S_SMB_CLK 7

JP14 Do Not Stuff /X — GND

NO-Connect

02G010018704

USBRBIAS_PN — R73 22.6Ohm 1% — GND

+3V — R66 10KOhm

+3VS — R212 10KOhm

PM_THRM# — R69 Do Not Stuff — THRM_ALERT# 42

+3VS — SMB_ALERT# — R213 10KOhm

+3VS — EXTSMI# — R214 10KOhm

+3V — KBC_SCI# — R215 10KOhm

+3V — PCIE_WAKE# — R72 1KOhm

SCH_GPIO_3 — R189 0Ohm — FM_DATA 26

DDR_MEM_CONFIG — R190 0Ohm — FM_CLK 26

+3V — RN7A 10KOHM — RN7B 10KOHM — IDE_IORDY — IDE_IRQ

+3VS — R75 Do Not Stuff /X — PCB_ID0 — R80 8.2KOhm — GND

PCB_VID SR 0

PCB ID

+3V — RN26A Do Not Stuff /X — RN26B Do Not Stuff /X

+3VS — RN27A 4.7KOHM — RN27B 4.7KOHM

7 S_SMB_CLK — Q3A Do Not Stuff /X — SMB_CLK 8,18,24,44

+5VS

7 S_SMB_DATA — Q3B Do Not Stuff/X — SMB_DATA 8,18,24,44

7 S_SMB_CLK — R216 0Ohm — SMB_CLK 8,18,24,44

7 S_SMB_DATA — R217 0Ohm — SMB_DATA 8,18,24,44

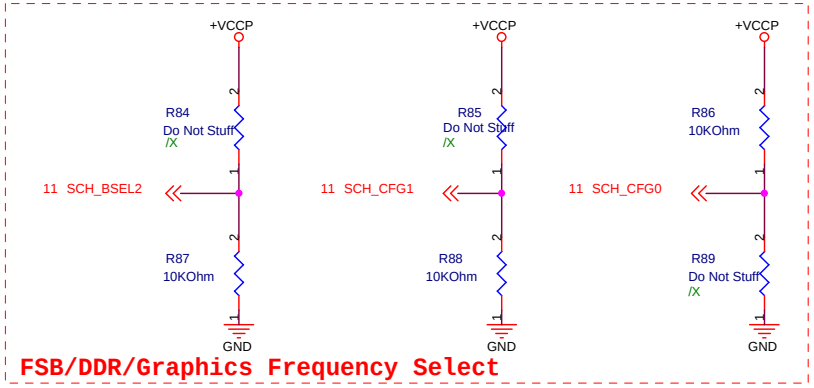
0106 1025

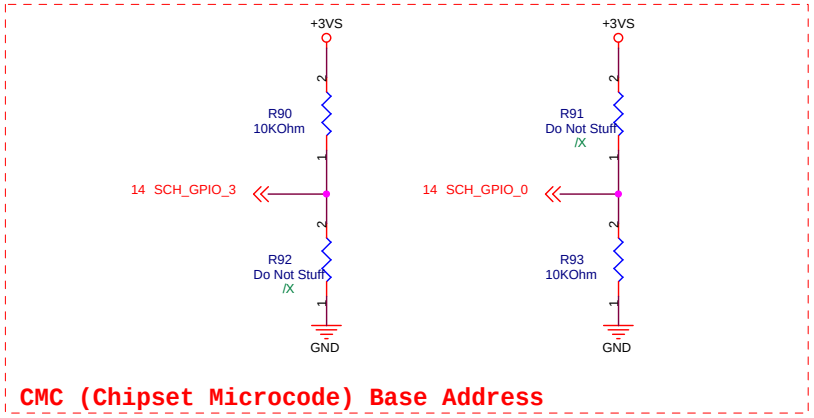
Title : SCH_Poulsbo_PMUSB/IDE/AZ(4)

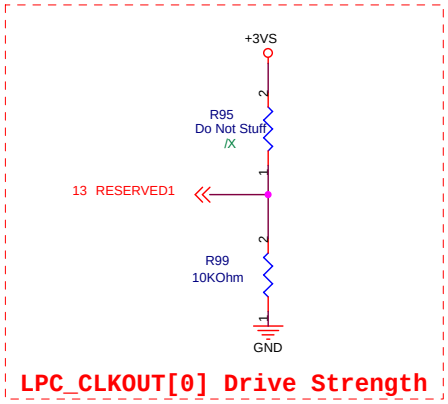
ASUSTeK COMPUTER INC Engineer: Jerry Liu

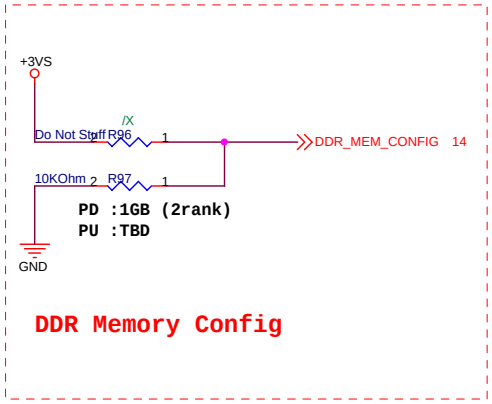
Size	Project Name	Rev
Custom	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 14 of 57









Strap Function	Singal Name			Strap		Comment
FSB/DDR Frequency Select Graphics Frequency Select	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed
	0	0	0	200	400	
	0	0	1	200	533	
CMC (Chipset Microcode) Base Address	GPIO3	GPIO0		Address		Selects the starting address that the CMC will use to start fetching code. (GPIO3 is the most significant)
	0	0		0xFFFB0000		
	0	1		0xFFFC0000		
	1	0		0xFFFD0000 (default)		
	1	1		0xFFFE0000		
LPC_CLKOUT[0] Buffer Strength	RESERVED1			Value		Selects the drive strength of the LPC_CLKOUT[0] clock.
	0			Reserved		
	0			1 Load (Default)		
	1			Reserved		
	1			2 Loads		

0106 1025

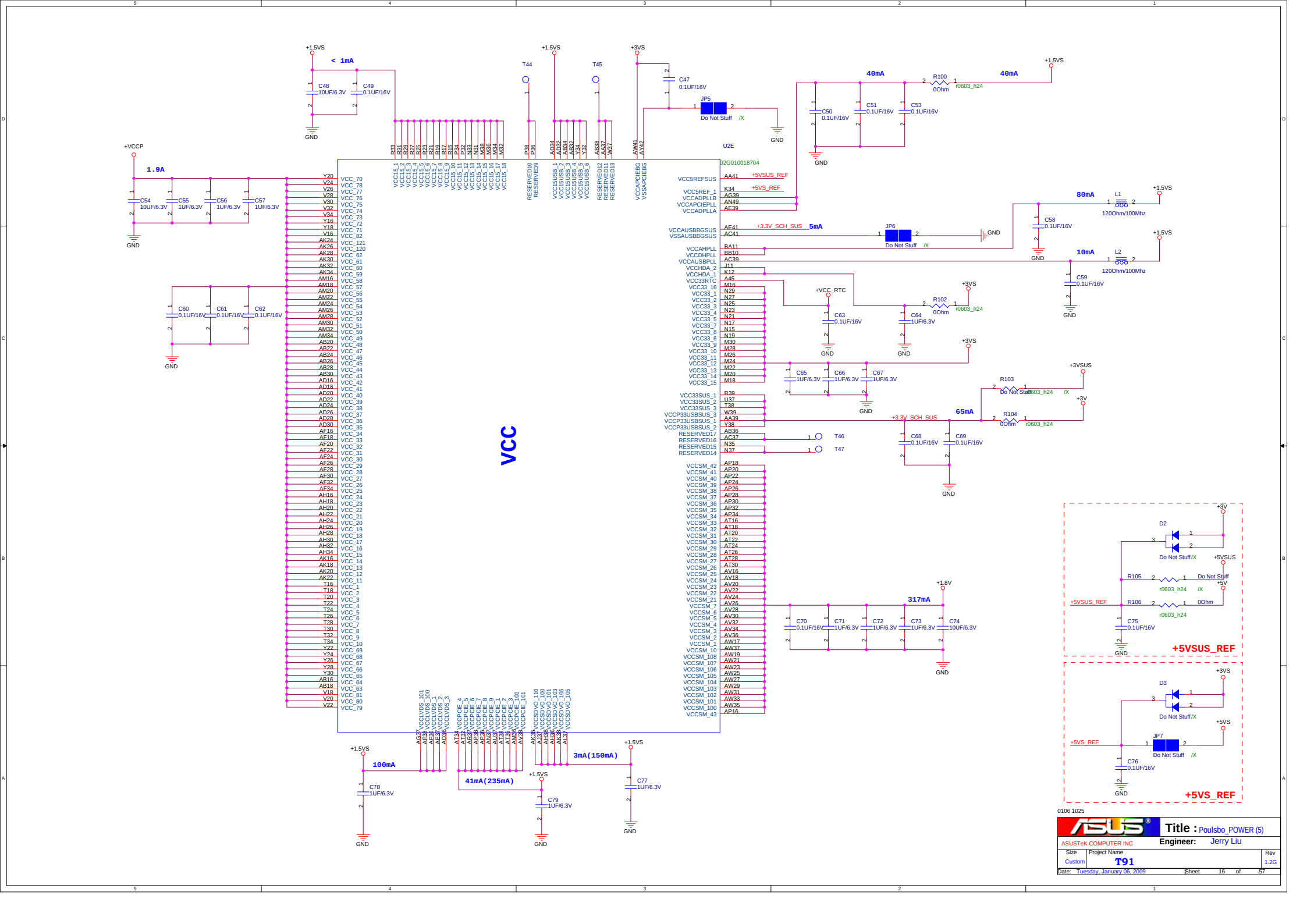
ASUSTek Computer INC.

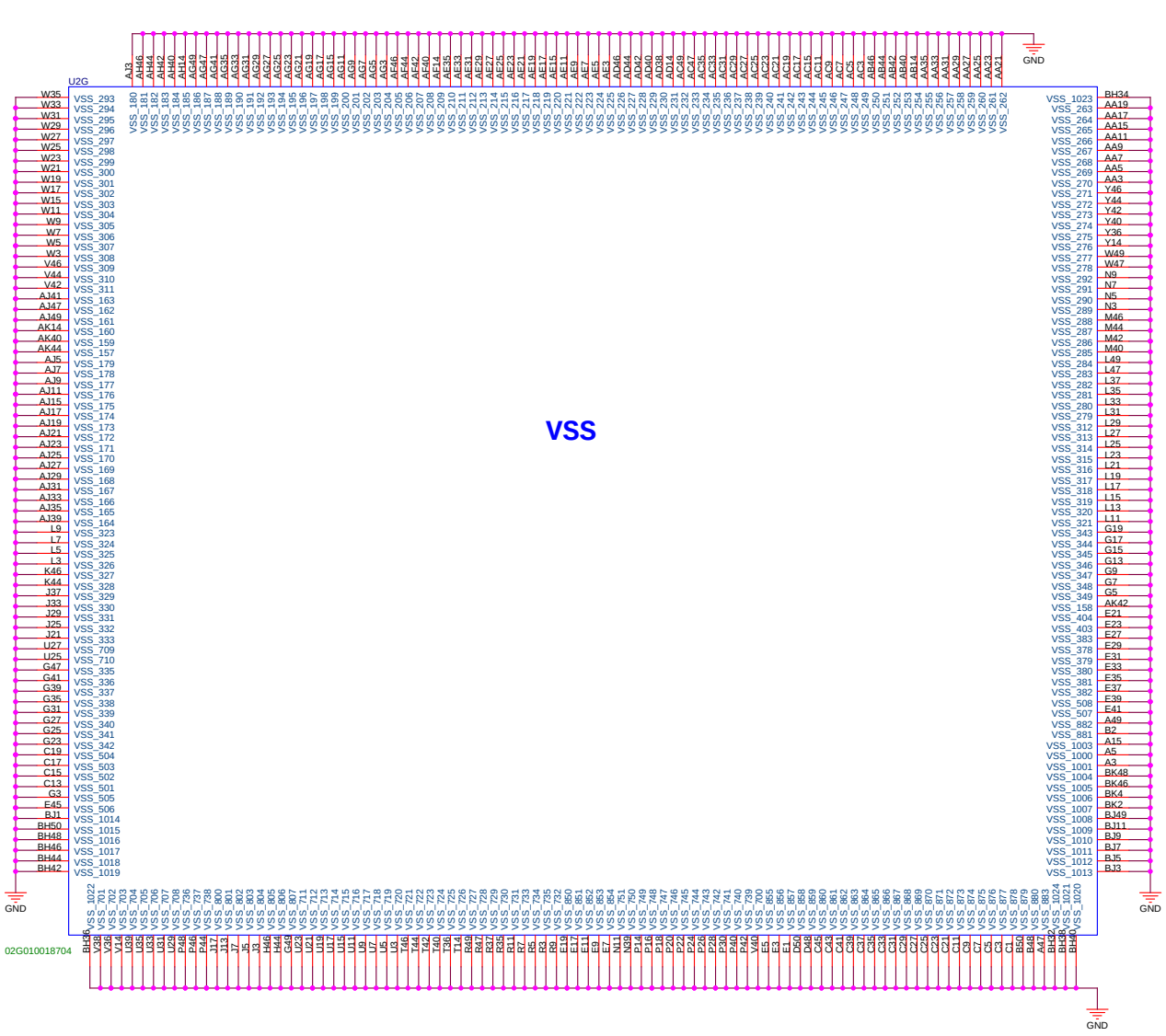
Title : POULSBO_STRAP(5)

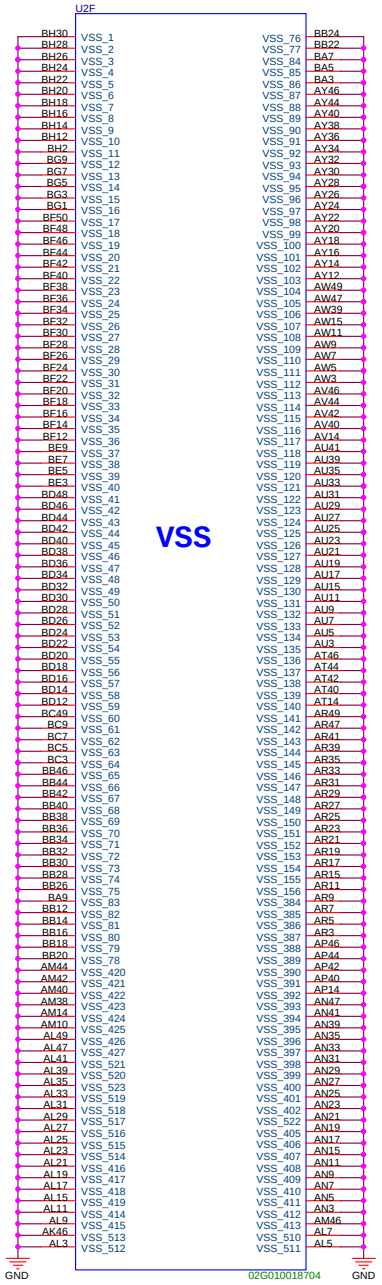
Engineer: Jerry Liu

Size	Project Name	Rev
B	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 15 of 57

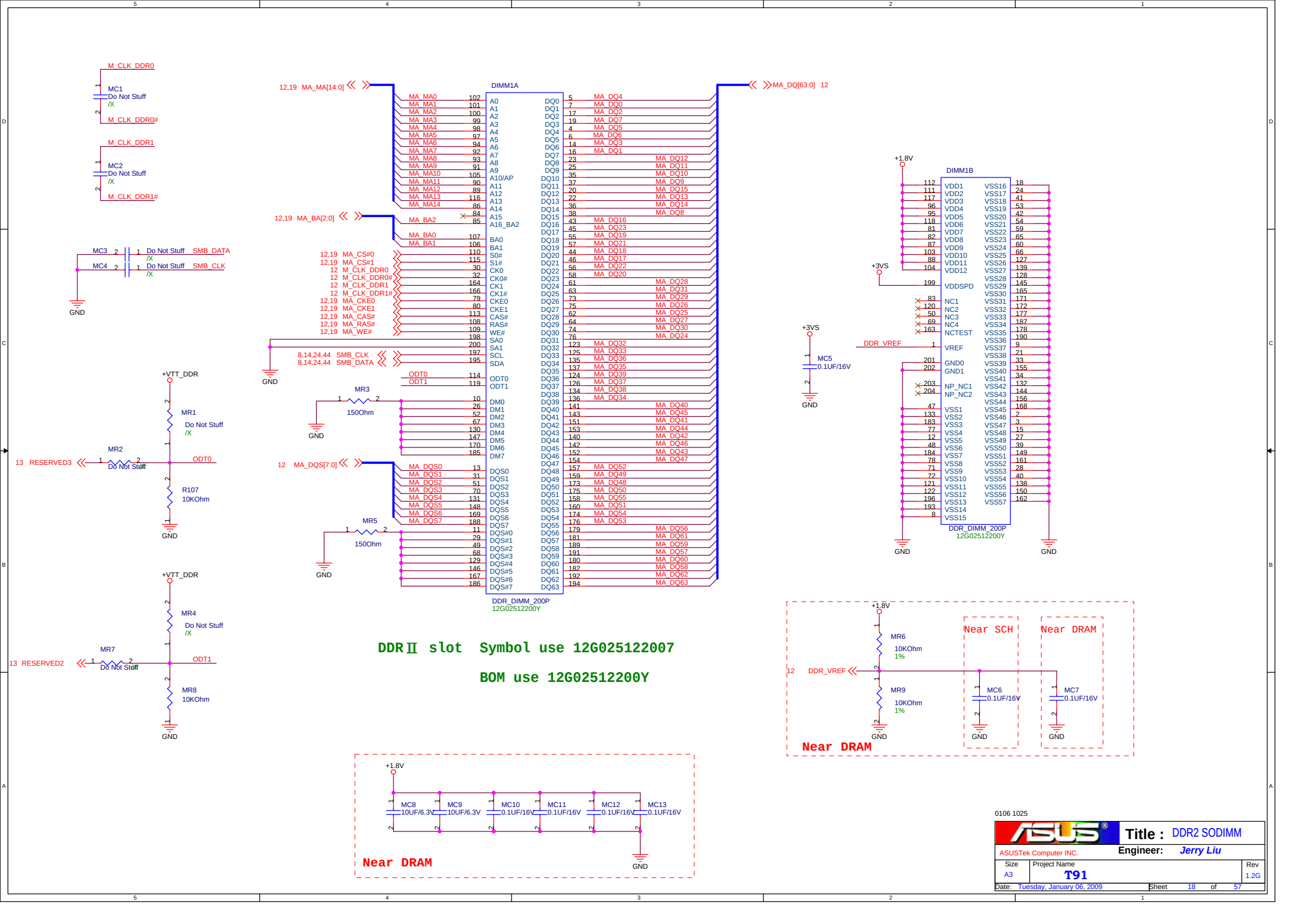

VCC
U2E
02G010018704
+1.5VS
< 1mA
C48 10UF/6.3V
C49 0.1UF/16V
GND
T44
T45
+3VS
C47 0.1UF/16V
JP5
Do Not Stuff /X
40mA
R100 0Ohm r0603_h24
C50 0.1UF/16V
C51 0.1UF/16V
C53 0.1UF/16V
+VCCP
1.9A
C54 10UF/6.3V
C55 1UF/6.3V
C56 1UF/6.3V
C57 1UF/6.3V
C60 0.1UF/16V
C61 0.1UF/16V
C62 0.1UF/16V
VCC5REFSUS
+5VSUS_REF
VCC5REF_1
+5VS_REF
VCCADPLLB
VCCAPCIEPLL
VCCADPLLA
VCCAUSBBGSUS
VSSAUSBBGSUS
+3.3V_SCH_SUS
5mA
JP6
Do Not Stuff /X
80mA
L1 120Ohm/100Mhz
C58 0.1UF/16V
10mA
L2 120Ohm/100Mhz
C59 0.1UF/16V
VCCAHPLL
VCCDHPLL
VCCAUSBPLL
VCCHDA_2
VCCHDA_1
VCC33RTC
+VCC_RTC
C63 0.1UF/16V
R102 0Ohm r0603_h24
C64 1UF/6.3V
VCC33_16
VCC33_1
VCC33_2
VCC33_3
VCC33_4
VCC33_5
VCC33_7
VCC33_8
VCC33_6
VCC33_9
VCC33_10
VCC33_11
VCC33_12
VCC33_13
VCC33_14
VCC33_15
C65 1UF/6.3V
C66 1UF/6.3V
C67 1UF/6.3V
VCC33SUS_1
VCC33SUS_2
VCC33SUS_3
VCCP33USBSUS_3
VCCP33USBSUS_1
VCCP33USBSUS_2
RESERVED17
RESERVED16
RESERVED15
RESERVED14
T46
T47
+3.3V_SCH_SUS
65mA
R103 Do Not Stuff r0603_h24 /X
R104 0Ohm r0603_h24
+3VSUS
+3V
C68 0.1UF/16V
C69 0.1UF/16V
VCCSM_42
VCCSM_41
VCCSM_40
VCCSM_39
VCCSM_38
VCCSM_37
VCCSM_36
VCCSM_35
VCCSM_34
VCCSM_33
VCCSM_32
VCCSM_31
VCCSM_30
VCCSM_29
VCCSM_28
VCCSM_27
VCCSM_26
VCCSM_25
VCCSM_24
VCCSM_23
VCCSM_22
VCCSM_21
VCCSM_7
VCCSM_6
VCCSM_5
VCCSM_4
VCCSM_3
VCCSM_2
VCCSM_1
VCCSM_10
VCCSM_108
VCCSM_107
VCCSM_106
VCCSM_105
VCCSM_104
VCCSM_103
VCCSM_102
VCCSM_101
VCCSM_100
VCCSM_43
+1.8V
317mA
C70 0.1UF/16V
C71 1UF/6.3V
C72 1UF/6.3V
C73 1UF/6.3V
C74 10UF/6.3V
D2
Do Not Stuff /X
+5VSUS
R105 Do Not Stuff r0603_h24 /X
+5V
+5VSUS_REF
R106 0Ohm r0603_h24
C75 0.1UF/16V
+5VSUS_REF
D3
Do Not Stuff /X
+5VS
+5VS_REF
JP7
Do Not Stuff /X
C76 0.1UF/16V
+5VS_REF
100mA
C78 1UF/6.3V
41mA(235mA)
C79 1UF/6.3V
3mA(150mA)
C77 1UF/6.3V
0106 1025
Title : Poulsbo_POWER (5)
ASUSTeK COMPUTER INC
Engineer: Jerry Liu
Size Custom
Project Name T91
Rev 1.2G
Date: Tuesday, January 06, 2009
Sheet 16 of 57





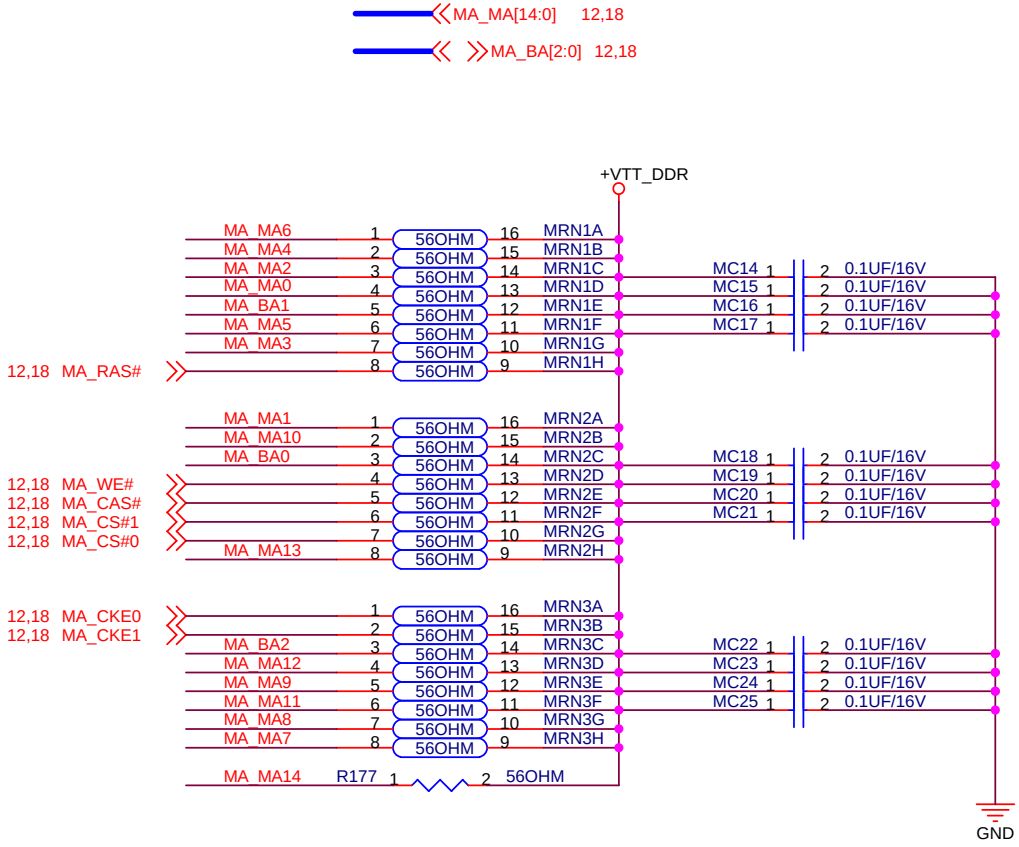
0106 1025

ASUSTeK COMPUTER INC	Title : POULSBO_GND (6)	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 17 of 57	



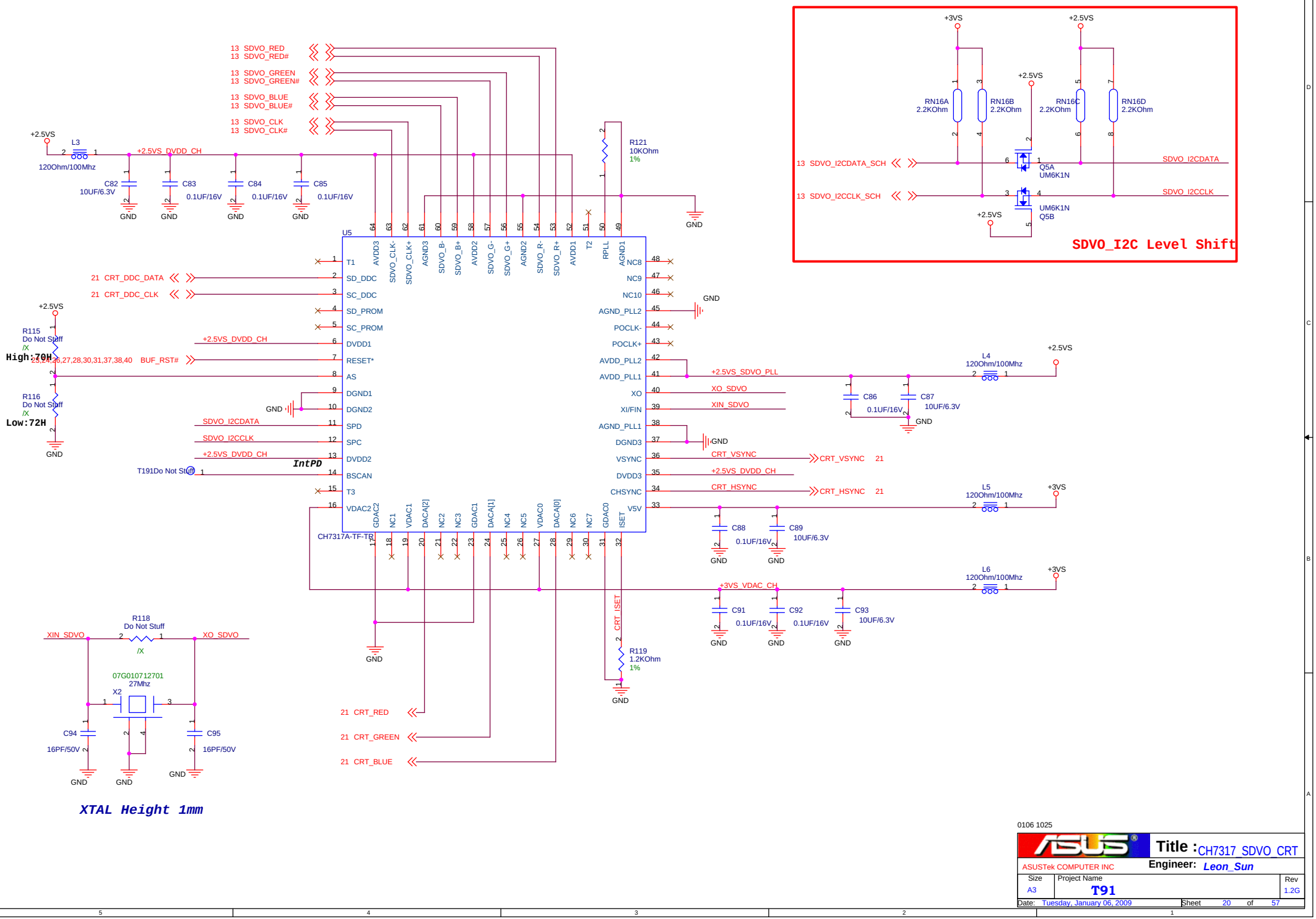
0106 1025

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 18 of 57	



0106 1025

ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 19 of 57	



0106 1025

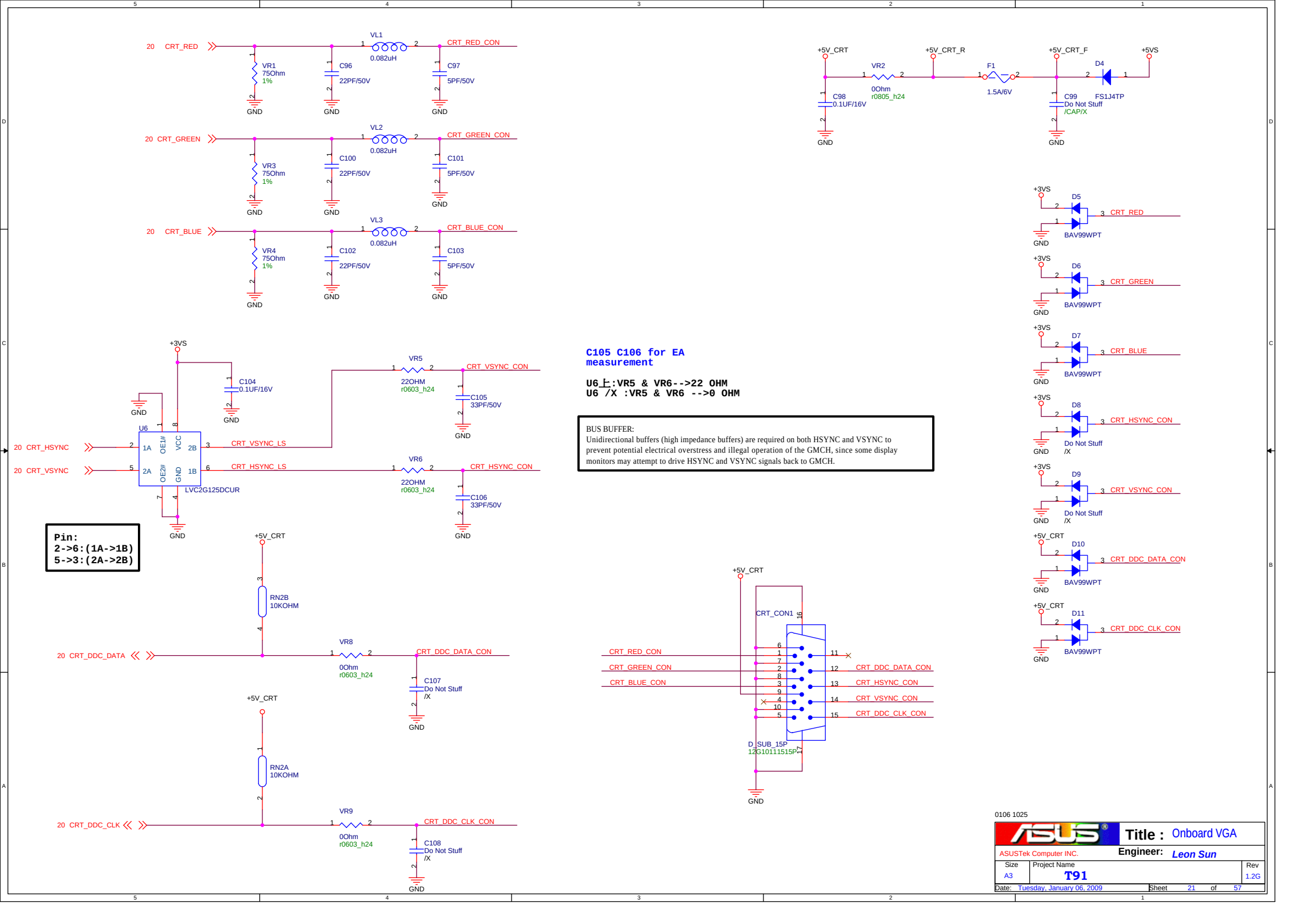
ASUSTek COMPUTER INC

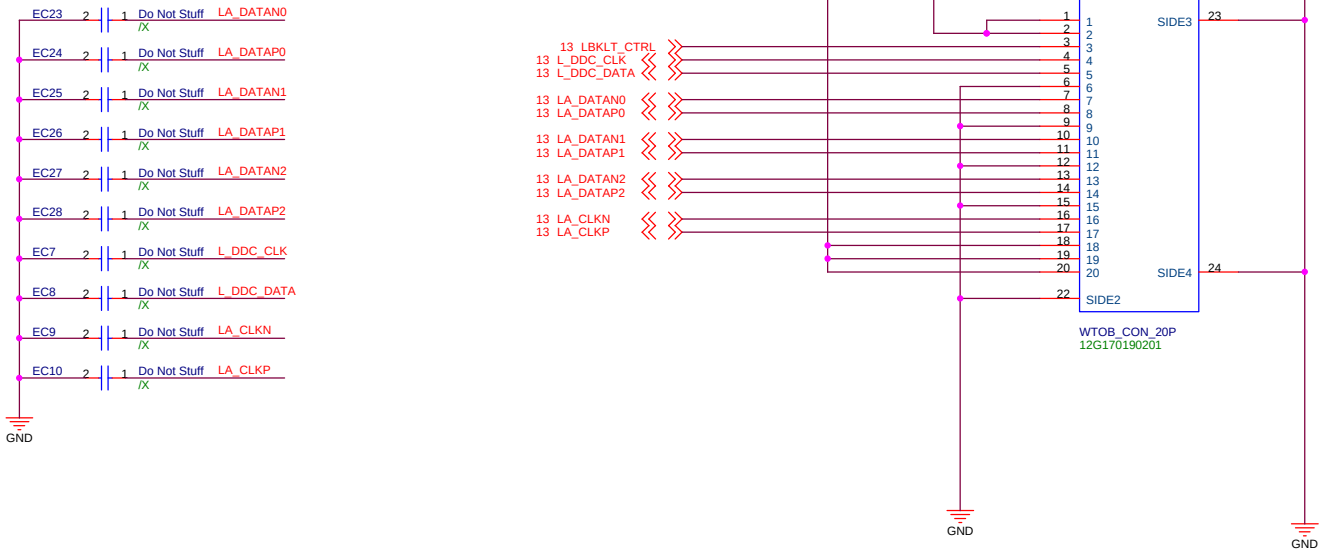
Title : CH7317_SDVO_CRT

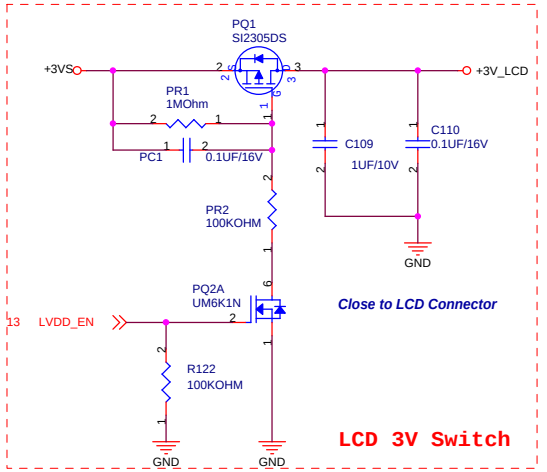
Engineer: Leon_Sun

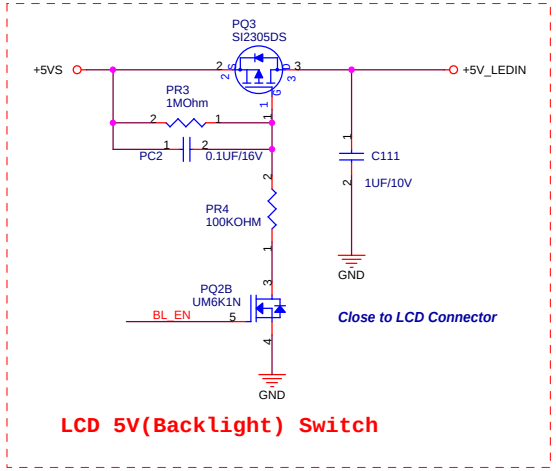
Size	Project Name	Rev
A3	T91	1.2G

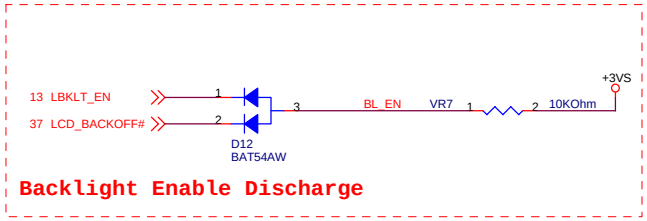
Date: Tuesday, January 06, 2009 Sheet 20 of 57


20 CRT_RED
VL1
0.082uH
CRT_RED_CON
VR1
75Ohm
1%
C96
22PF/50V
C97
5PF/50V
GND
20 CRT_GREEN
VL2
0.082uH
CRT_GREEN_CON
VR3
75Ohm
1%
C100
22PF/50V
C101
5PF/50V
20 CRT_BLUE
VL3
0.082uH
CRT_BLUE_CON
VR4
75Ohm
1%
C102
22PF/50V
C103
5PF/50V
+5V_CRT
VR2
0Ohm
r0805_h24
+5V_CRT_R
F1
1.5A/6V
+5V_CRT_F
D4
+5VS
C98
0.1UF/16V
C99
Do Not Stuff
/CAP/X
FS1J4TP
+3VS
D5
CRT_RED
BAV99WPT
D6
CRT_GREEN
D7
CRT_BLUE
D8
CRT_HSYNC_CON
Do Not Stuff
/X
D9
CRT_VSYNC_CON
D10
CRT_DDC_DATA_CON
D11
CRT_DDC_CLK_CON
+3VS
C104
0.1UF/16V
VR5
22OHM
r0603_h24
CRT_VSYNC_CON
C105
33PF/50V
U6
20 CRT_HSYNC
20 CRT_VSYNC
1A
2A
OE1#
OE2#
VCC
GND
2B
1B
CRT_VSYNC_LS
CRT_HSYNC_LS
LVC2G125DCUR
VR6
22OHM
r0603_h24
CRT_HSYNC_CON
C106
33PF/50V
Pin:
2->6:(1A->1B)
5->3:(2A->2B)
+5V_CRT
RN2B
10KOHM
20 CRT_DDC_DATA
VR8
0Ohm
r0603_h24
CRT_DDC_DATA_CON
C107
Do Not Stuff
/X
RN2A
10KOHM
20 CRT_DDC_CLK
VR9
0Ohm
r0603_h24
CRT_DDC_CLK_CON
C108
Do Not Stuff
/X
C105 C106 for EA measurement
U6上:VR5 & VR6-->22 OHM
U6 /X :VR5 & VR6 -->0 OHM
BUS BUFFER:
Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.
+5V_CRT
CRT_CON1
CRT_RED_CON
CRT_GREEN_CON
CRT_BLUE_CON
CRT_DDC_DATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDC_CLK_CON
D_SUB_15P
12G10111515P
0106 1025
Title : Onboard VGA
ASUSTek Computer INC.
Engineer: Leon Sun
Size
A3
Project Name
T91
Rev
1.2G
Date: Tuesday, January 06, 2009
Sheet 21 of 57



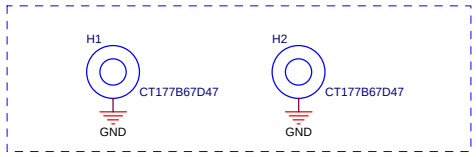




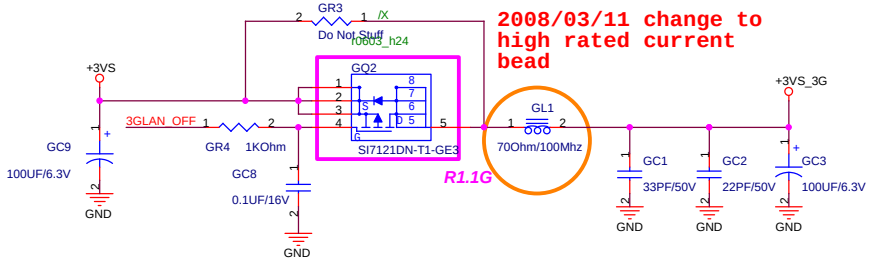


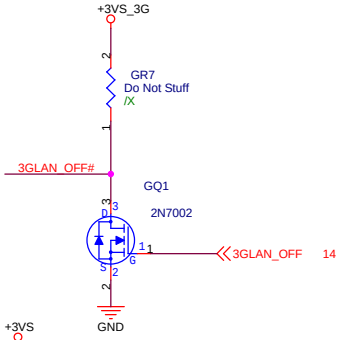
0106 1025

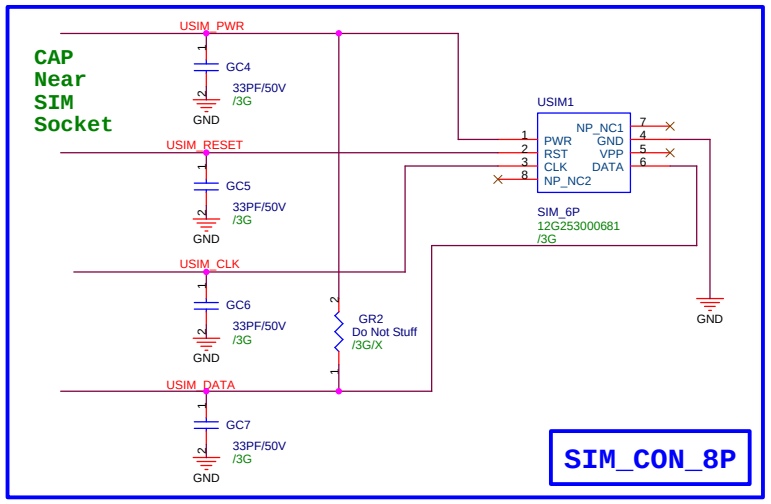
ASUSTek Computer INC.	Title : LVDS Conn	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 22 of 57	

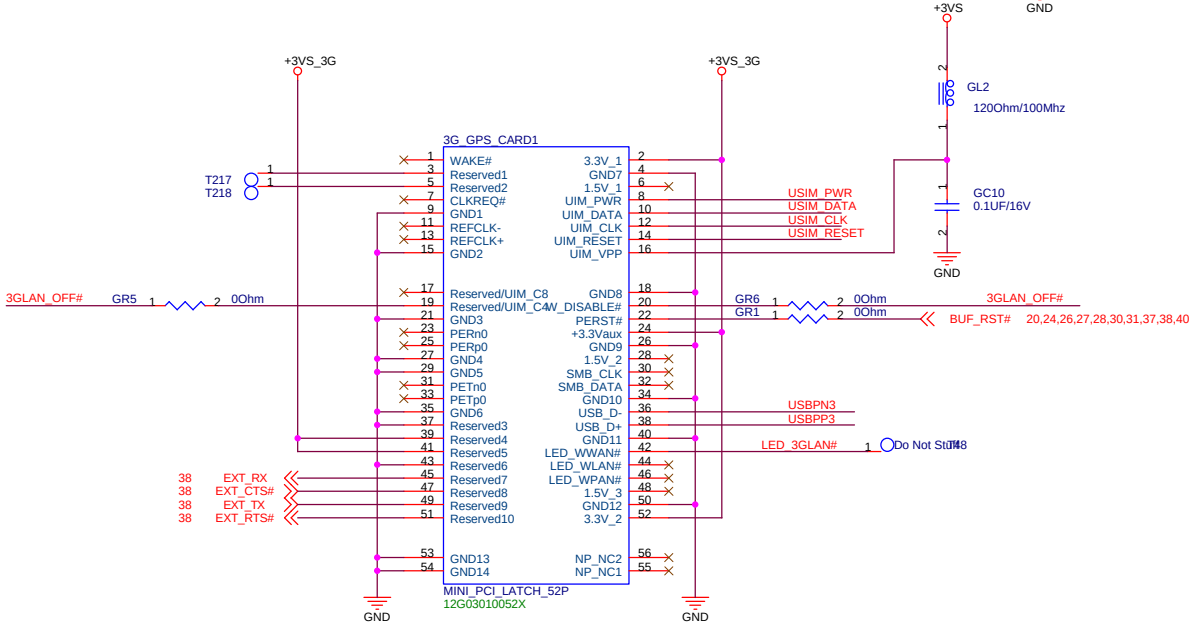


MINI CARD NUT(2.8mm) *2

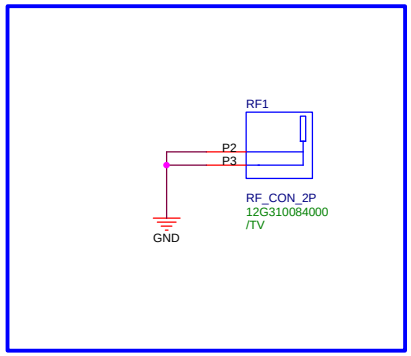


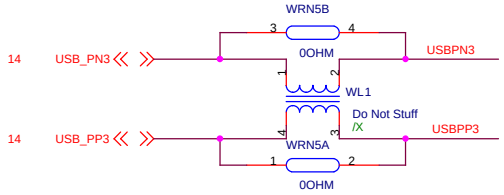






GPS/DTV Antenna





0106 1025

3.5G Module & External Antenna

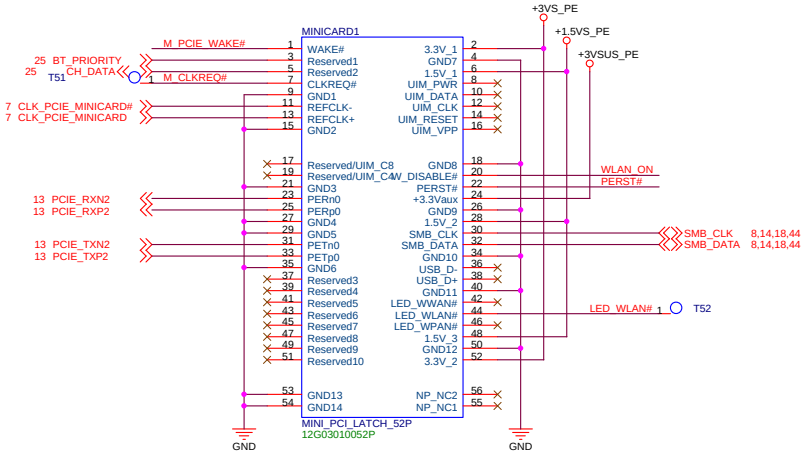
ASUSTek Computer INC.

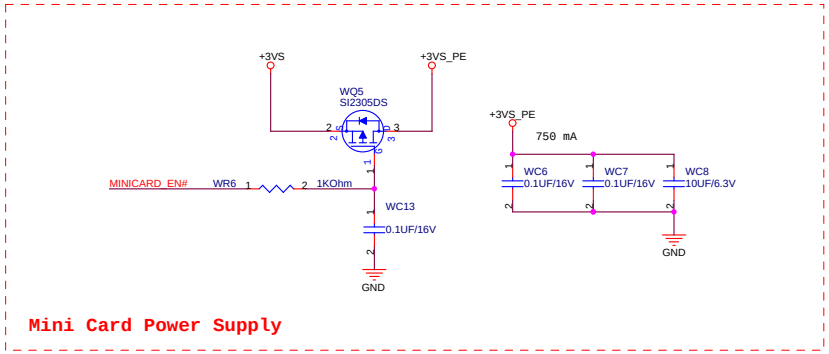
Title :

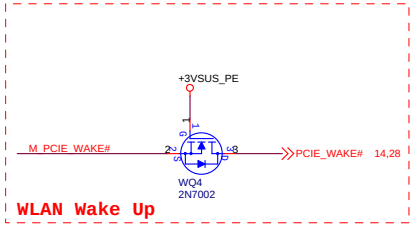
Engineer: Leon Sun

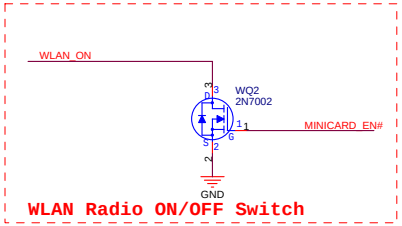
Size	Project Name	Rev
A3	T91	1.2G

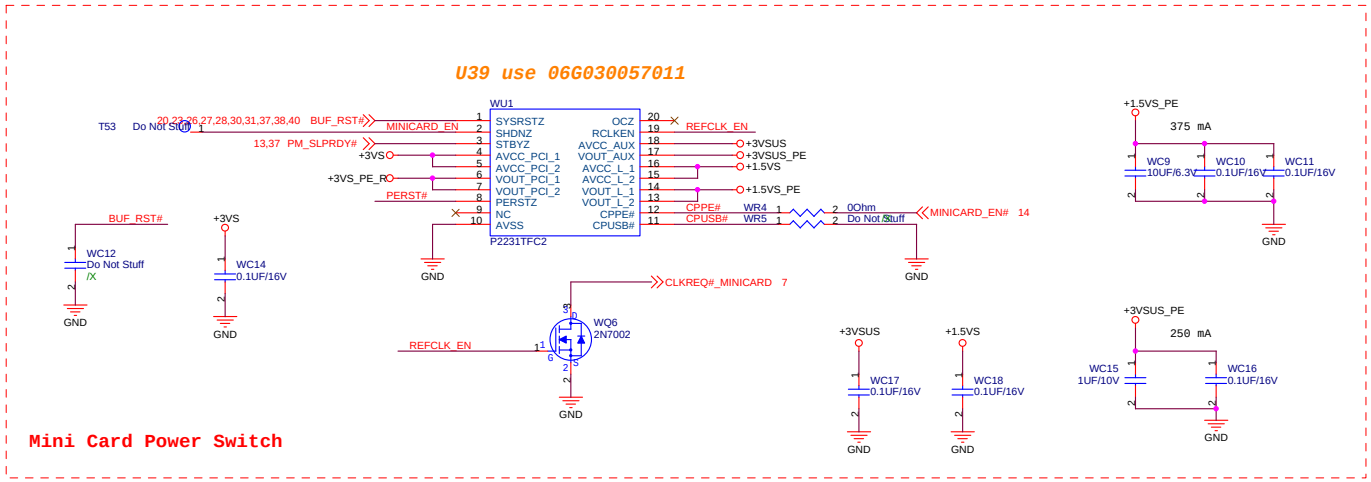
Date: Tuesday, January 06, 2009 Sheet 23 of 57

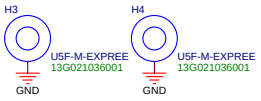






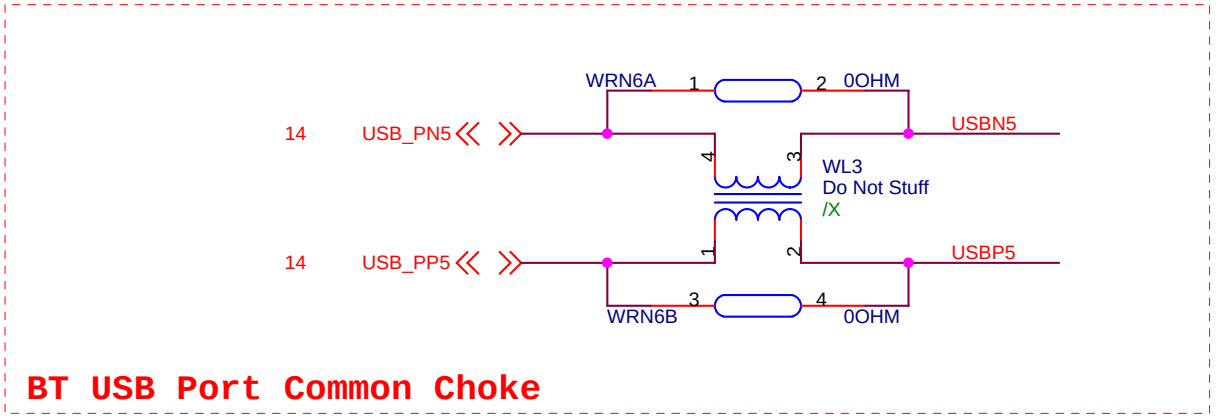




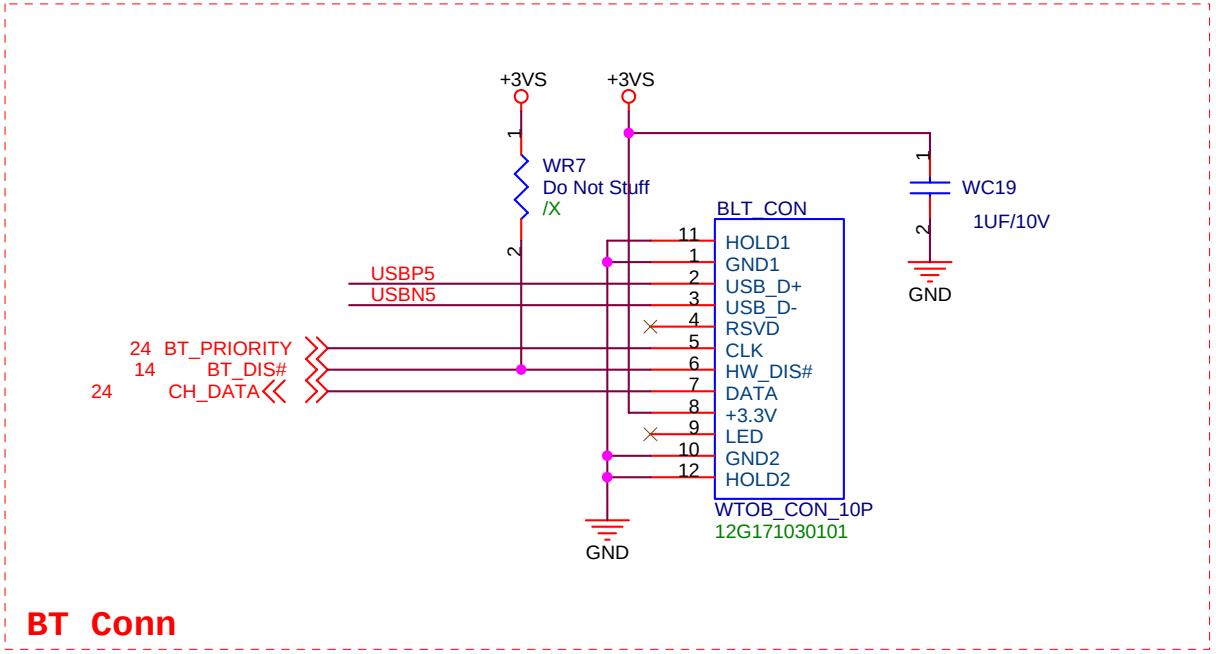


0106 1025

ASUSTek Computer INC.	Title : Mini WIFI	
	Engineer: Jerry Liu	
Size: Custom	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 24 of 57	



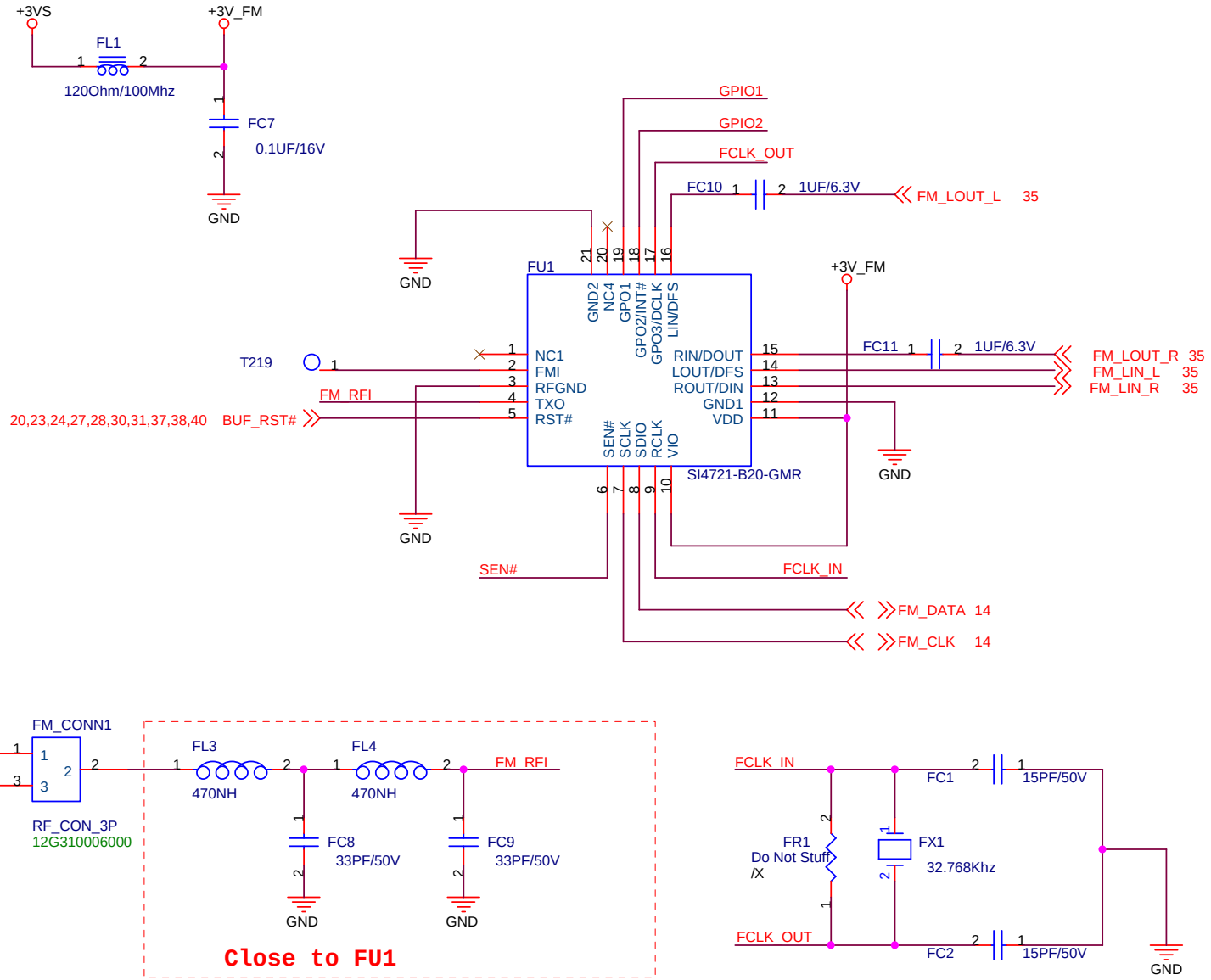
BT USB Port Common Choke

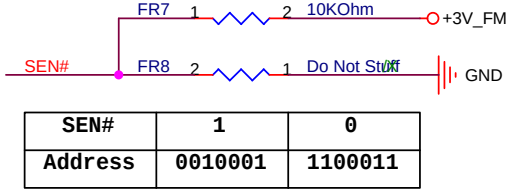


BT Conn

0106 1025

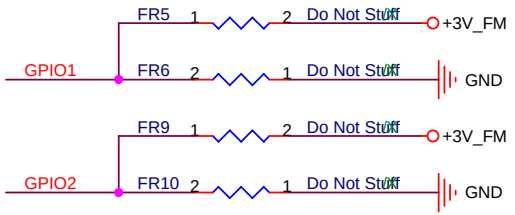
ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: Jerry Liu	
Size: A	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 25 of 57	





SEN#	1	0
Address	0010001	1100011

seven-bit device address Selection



BUS Mode	GPIO1	GPIO2/INT
2-Wire	1	0
SPI	1	1(Must Drive)
3-Wire	0(Must Drive)	0

Bus Mode Selection

0106 1025

ASUSTek Computer INC.

Title : FM RADIO

Engineer: *Jerry Liu*

Size	Project Name	Rev
A4	T91	1.2G

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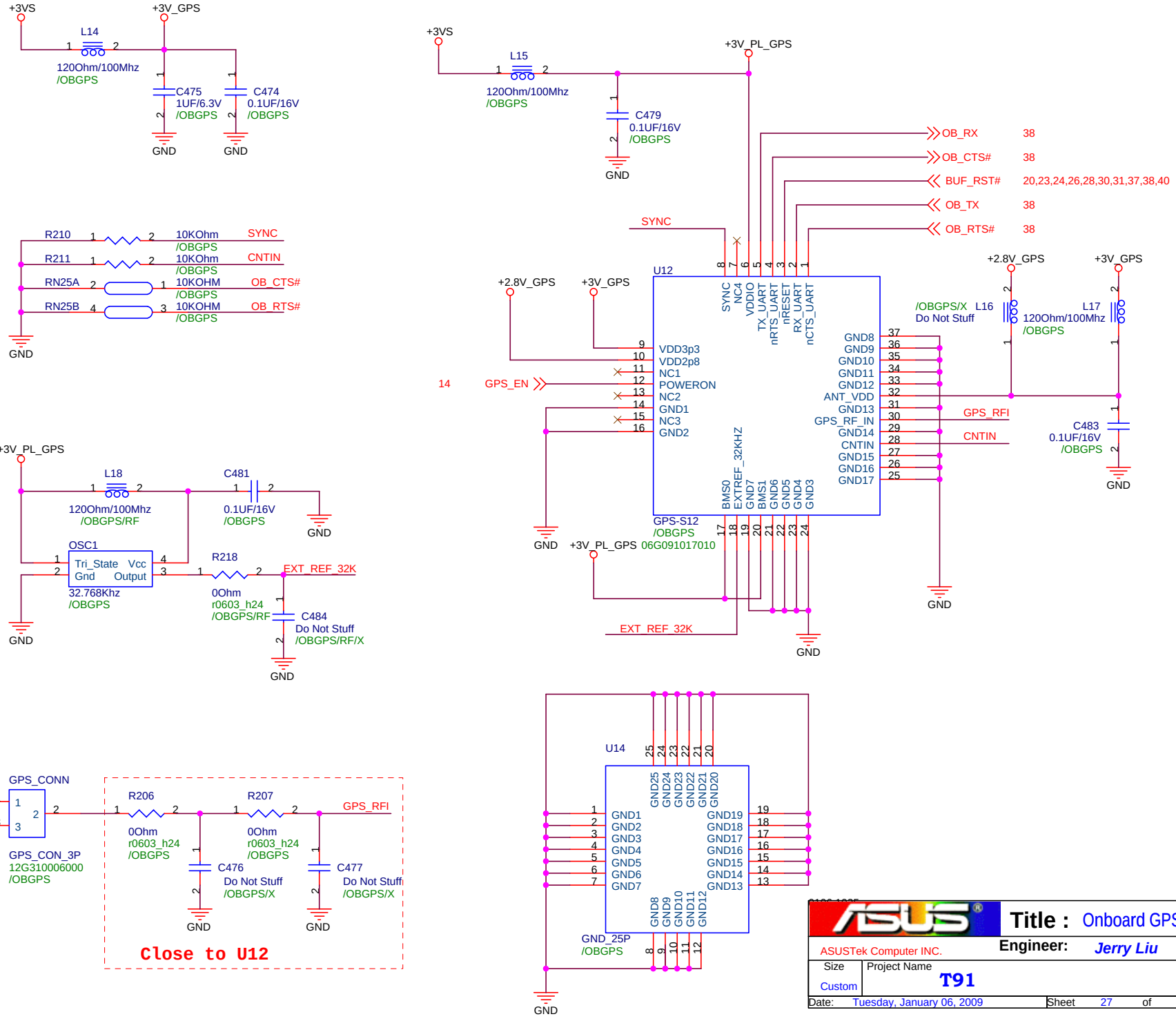


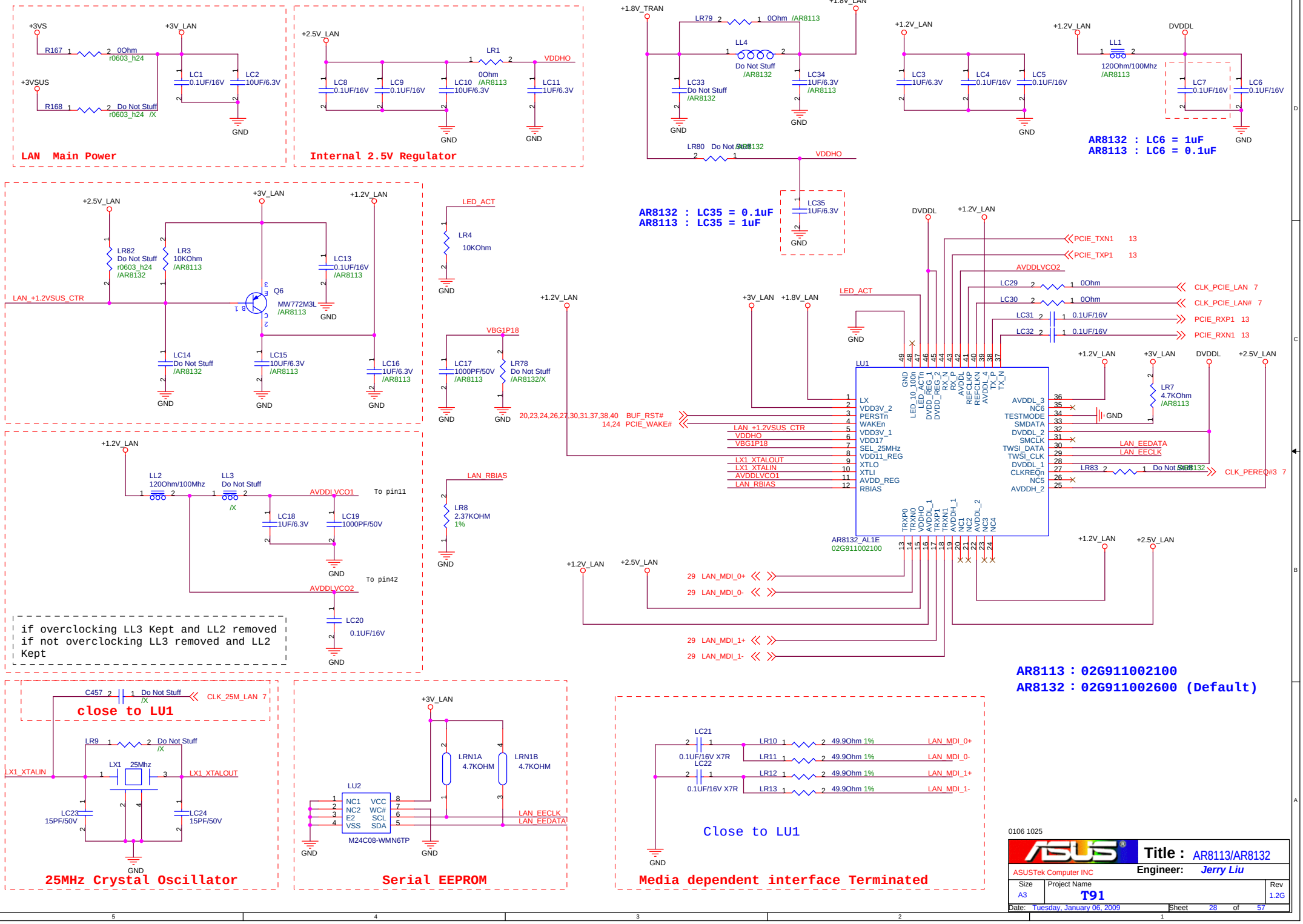
ASUSTek Computer INC.

Title : Onboard GPS

Engineer: *Jerry Liu*

Size	Project Name	Rev
Custom	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 27 of 57


LAN Main Power
Internal 2.5V Regulator
AR8132 : LC6 = 1uF
AR8113 : LC6 = 0.1uF
AR8132 : LC35 = 0.1uF
AR8113 : LC35 = 1uF
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept
close to LU1
25MHz Crystal Oscillator
Serial EEPROM
Close to LU1
Media dependent interface Terminated
AR8113 : 02G911002100
AR8132 : 02G911002600 (Default)
Title : AR8113/AR8132
ASUSTek Computer INC
Engineer: Jerry Liu
Project Name T91
Size A3
Rev 1.2G
Date: Tuesday, January 06, 2009
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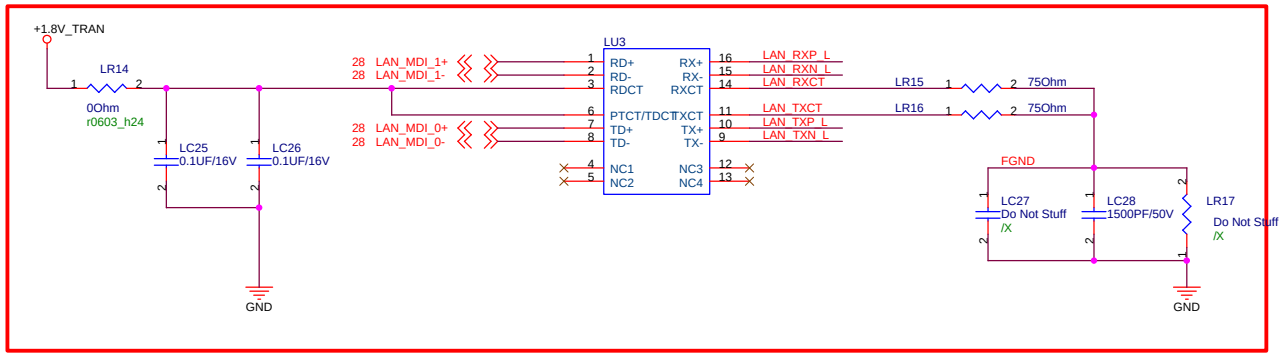
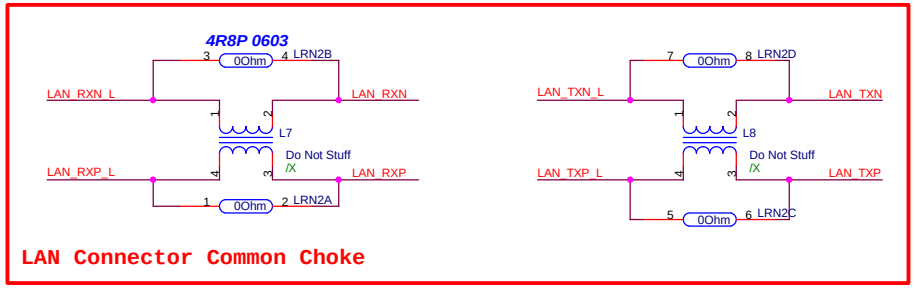
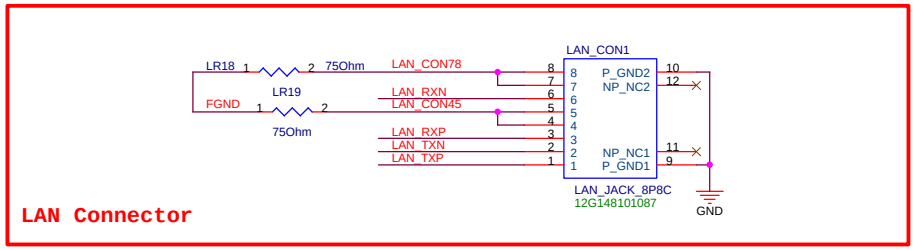
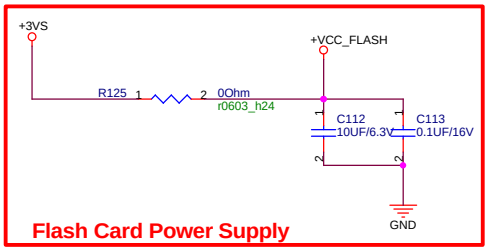


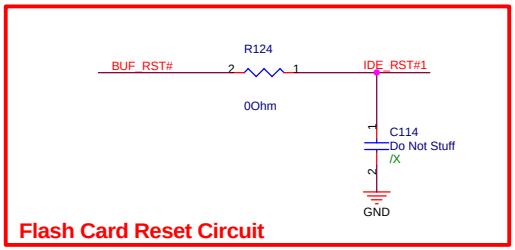


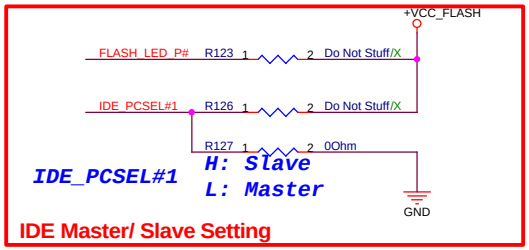


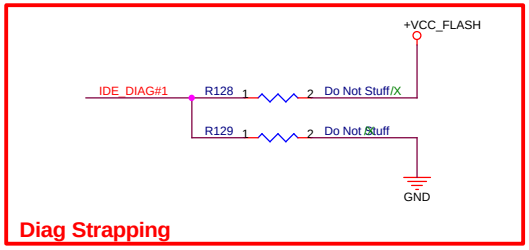
0106 1025

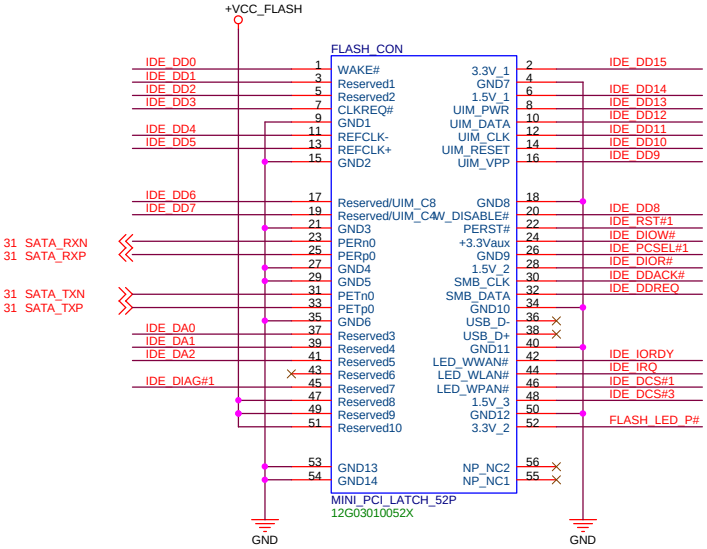
ASUSTek Computer INC.	Title : RJ45	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 29 of 57	



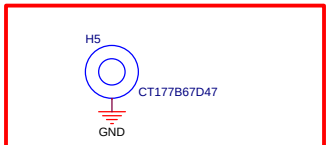






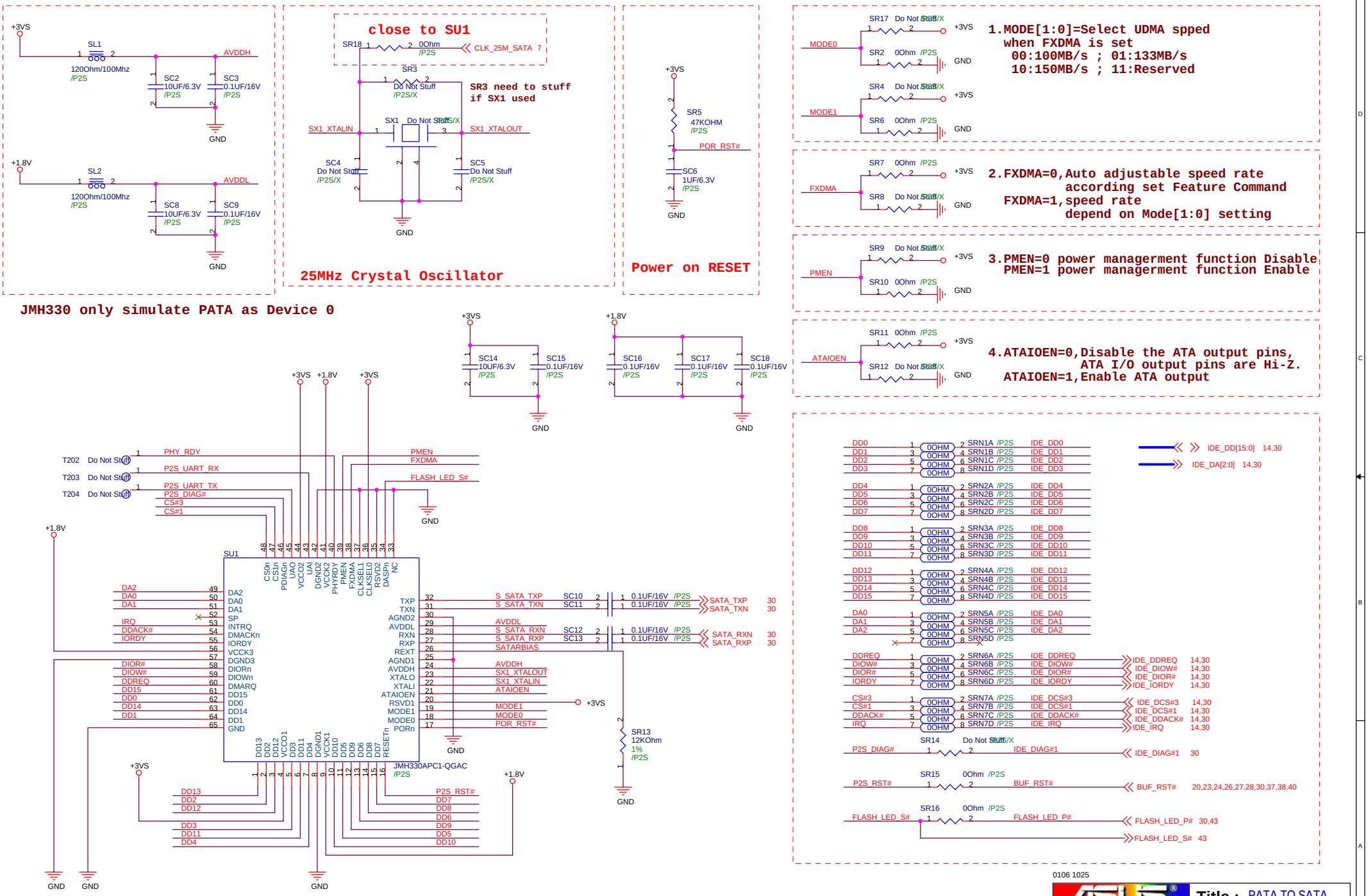


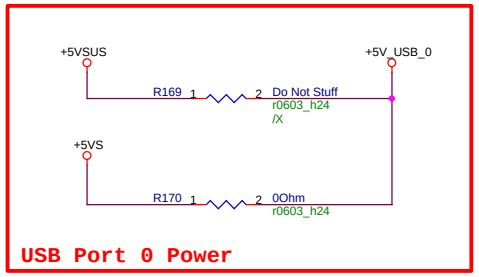
IDE_DD[15:0] 14,31
IDE_DA[2:0] 14,31
IDE_DDACK# 14,31
IDE_DDREQ 14,31
IDE_DIOR# 14,31
IDE_DIOW# 14,31
IDE_IORDY 14,31
IDE_DCS#1 14,31
IDE_DCS#3 14,31
IDE_IRQ 14,31
BUF_RST# 20,23,24,26,27,28,31,37,38,40
FLASH_LED_P# 31,43
IDE_DIAG#1 31



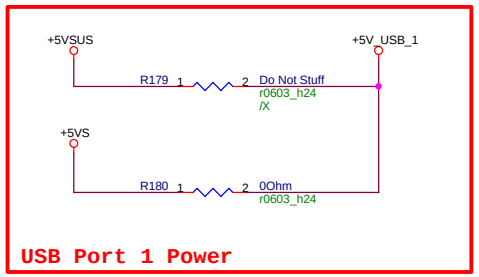
0106 1025

ASUSTek Computer INC.	Title : Flash Conn	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 30 of 57	

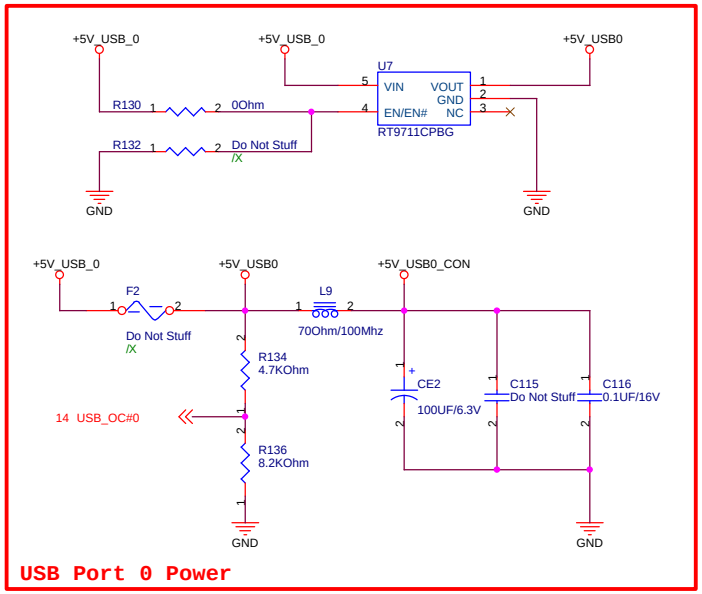

close to SU1
SR3 need to stuff if SX1 used
25MHz Crystal Oscillator
Power on RESET
JMH330 only simulate PATA as Device 0
1.MODE[1:0]=Select UDMA spped when FXDMA is set
00:100MB/s ; 01:133MB/s
10:150MB/s ; 11:Reserved
2.FXDMA=0,Auto adjustable speed rate according set Feature Command
FXDMA=1,speed rate depend on Mode[1:0] setting
3.PMEN=0 power managerment function Disable
PMEN=1 power managerment function Enable
4.ATAIOEN=0,Disable the ATA output pins, ATA I/O output pins are Hi-Z.
ATAIOEN=1,Enable ATA output
JMH330APC1-QGAC /P2S
0106 1025
Title : PATA TO SATA
ASUSTek Computer INC.
Engineer: Jerry Liu
Size A3
Project Name T91
Rev 1.2G
Date: Tuesday, January 06, 2009
Sheet 31 of 57



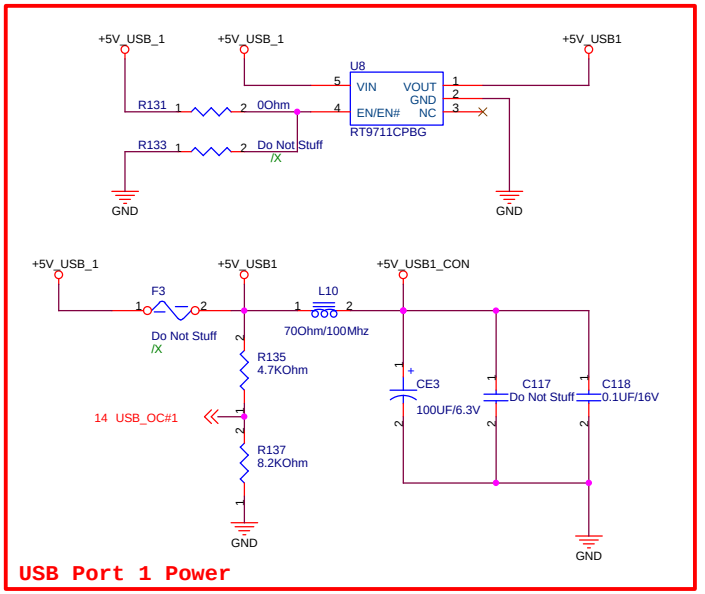
USB Port 0 Power



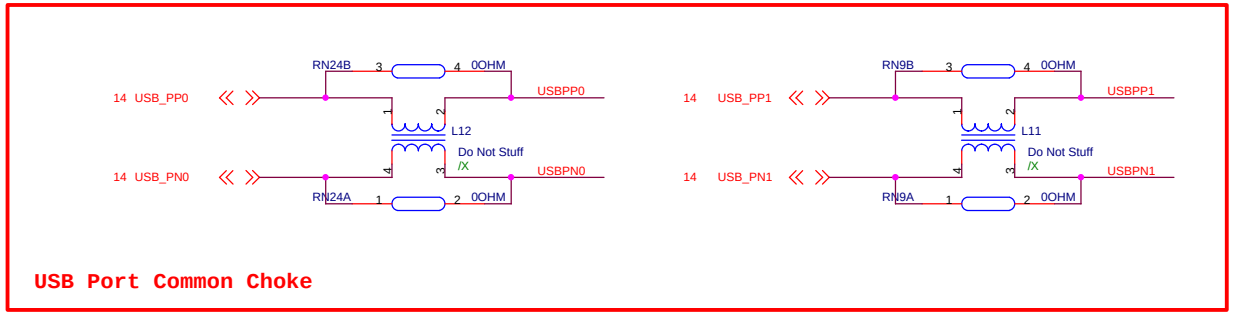
USB Port 1 Power



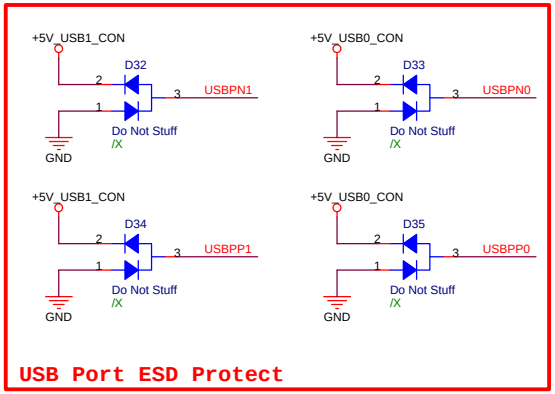
USB Port 0 Power



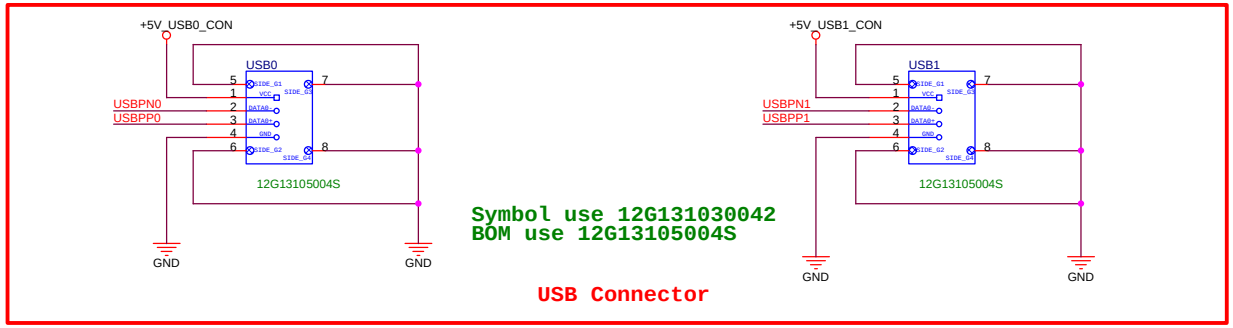
USB Port 1 Power



USB Port Common Choke



USB Port ESD Protect

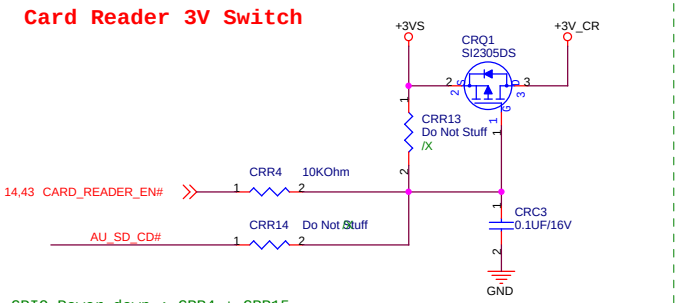


USB Connector

0106 1025

ASUSTek Computer INC.	Title : USB Port	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 32 of 57	

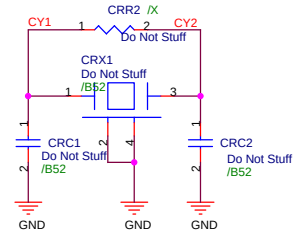
Card Reader 3V Switch



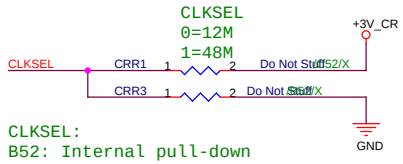
GPIO Power down : CRR4 + CRR15
(remove CRR13 + CRR14 + CRR16)

SD card Power down : CRR13 + CRR14 + CRR16
(remove CRR4 + CRR15)

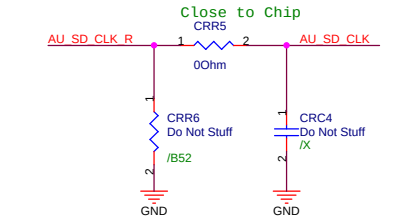
12MHz Crystal Oscillator

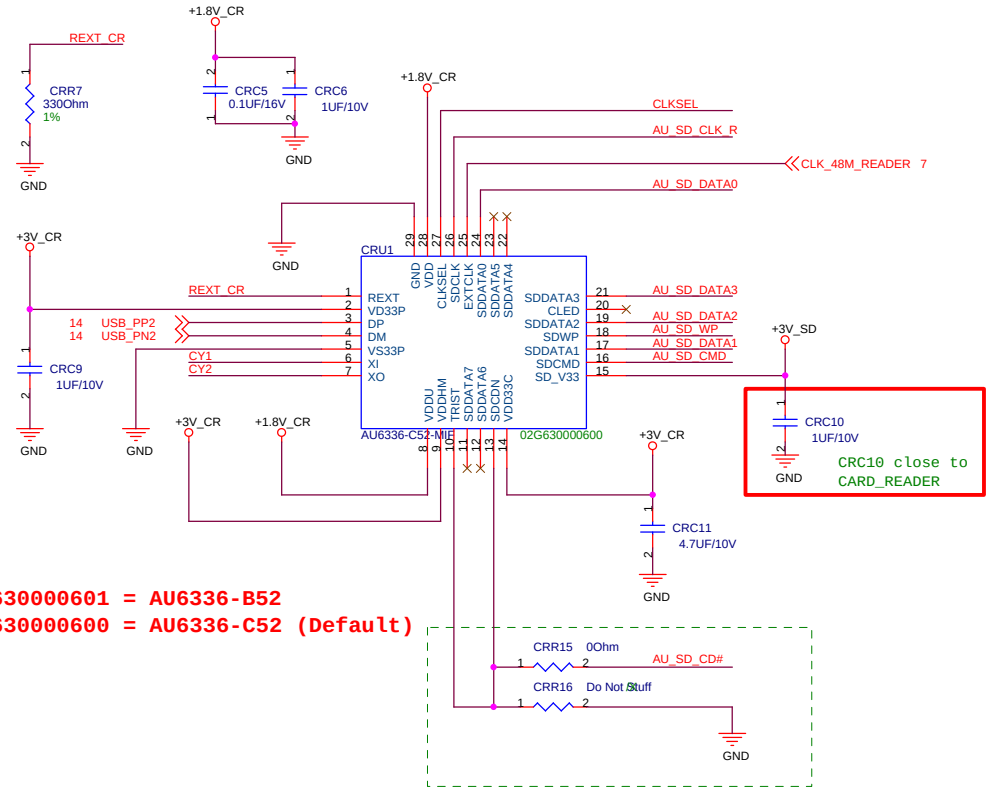


Clock Setting



CLKSEL:
B52: Internal pull-down
C52: Internal pull-up





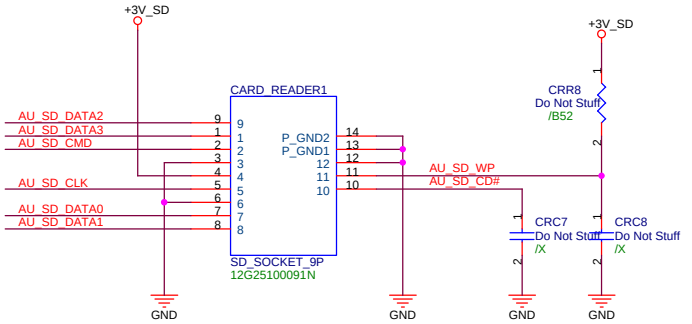
02G630000601 = AU6336-B52
02G630000600 = AU6336-C52 (Default)

Card Reader Connector

SDWP: Internal Pull-up

SDCDN: Internal Pull-up

SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card inserted

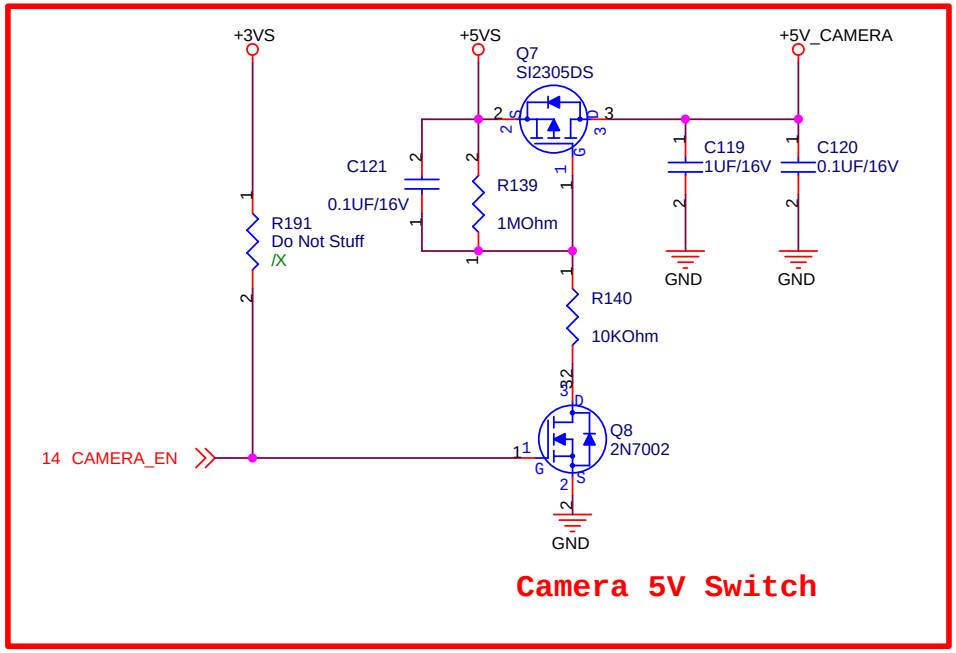


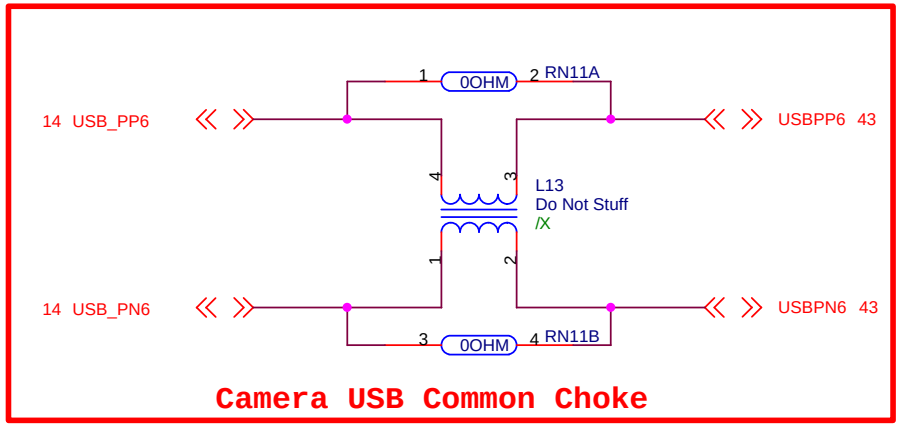
Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.

Card Reader Connector

0106 1025

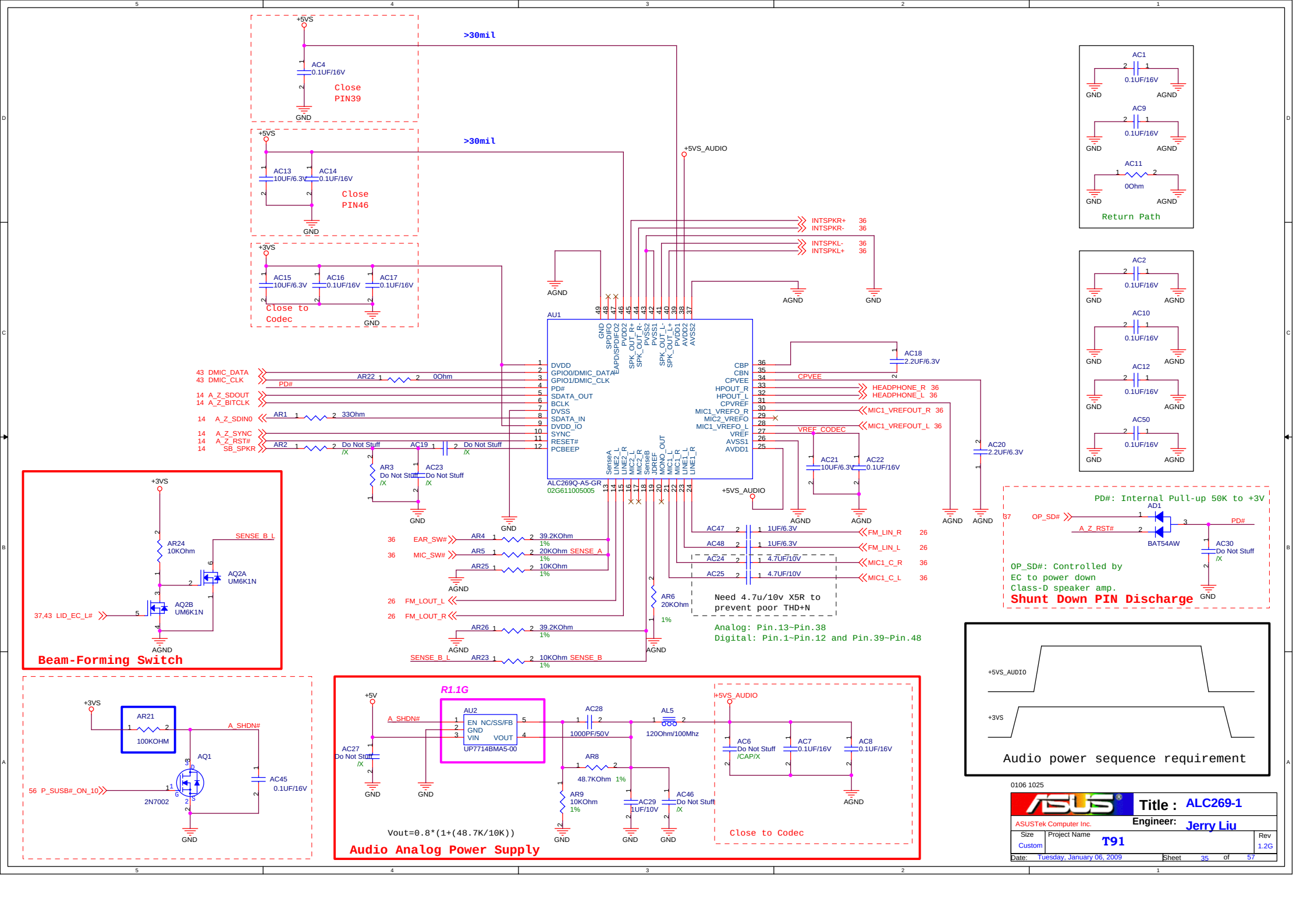
ASUSTek Computer Inc.	Title : AU6336-C52	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 33 of 57	

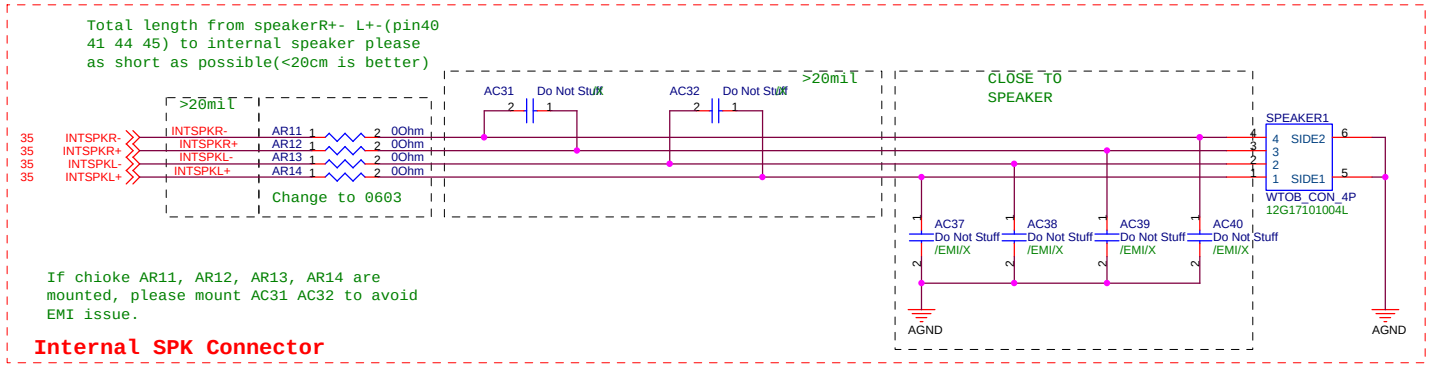


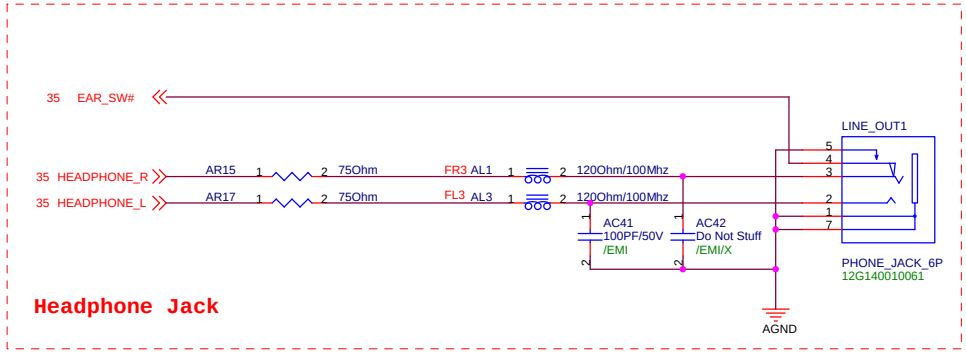


0106 1025

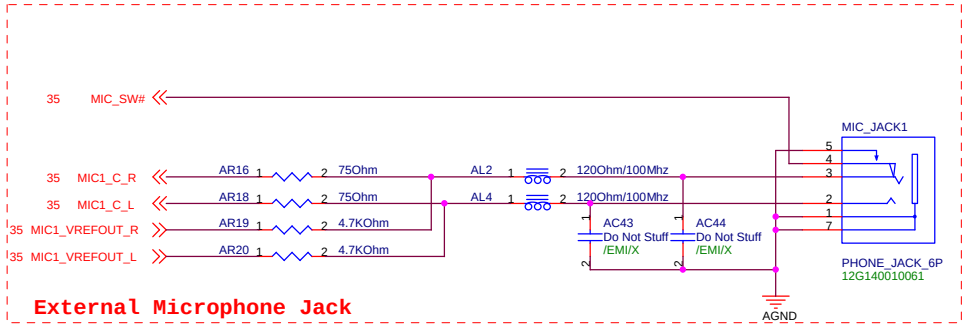
ASUSTek Computer INC.	Title : Camera Conn	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 34 of 57	


>30mil
Close PIN39
Close PIN46
Close to Codec
Return Path
ALC269Q-A5-GR
02G611005005
Need 4.7u/10v X5R to prevent poor THD+N
Analog: Pin.13~Pin.38
Digital: Pin.1~Pin.12 and Pin.39~Pin.48
PD#: Internal Pull-up 50K to +3V
OP_SD#: Controlled by EC to power down Class-D speaker amp.
Shunt Down PIN Discharge
Beam-Forming Switch
R1.1G
Vout=0.8*(1+(48.7K/10K))
Audio Analog Power Supply
Close to Codec
Audio power sequence requirement
Title : ALC269-1
ASUSTek Computer Inc.
Engineer: Jerry Liu
Project Name T91
Rev 1.2G
Date: Tuesday, January 06, 2009
Sheet 35 of 57



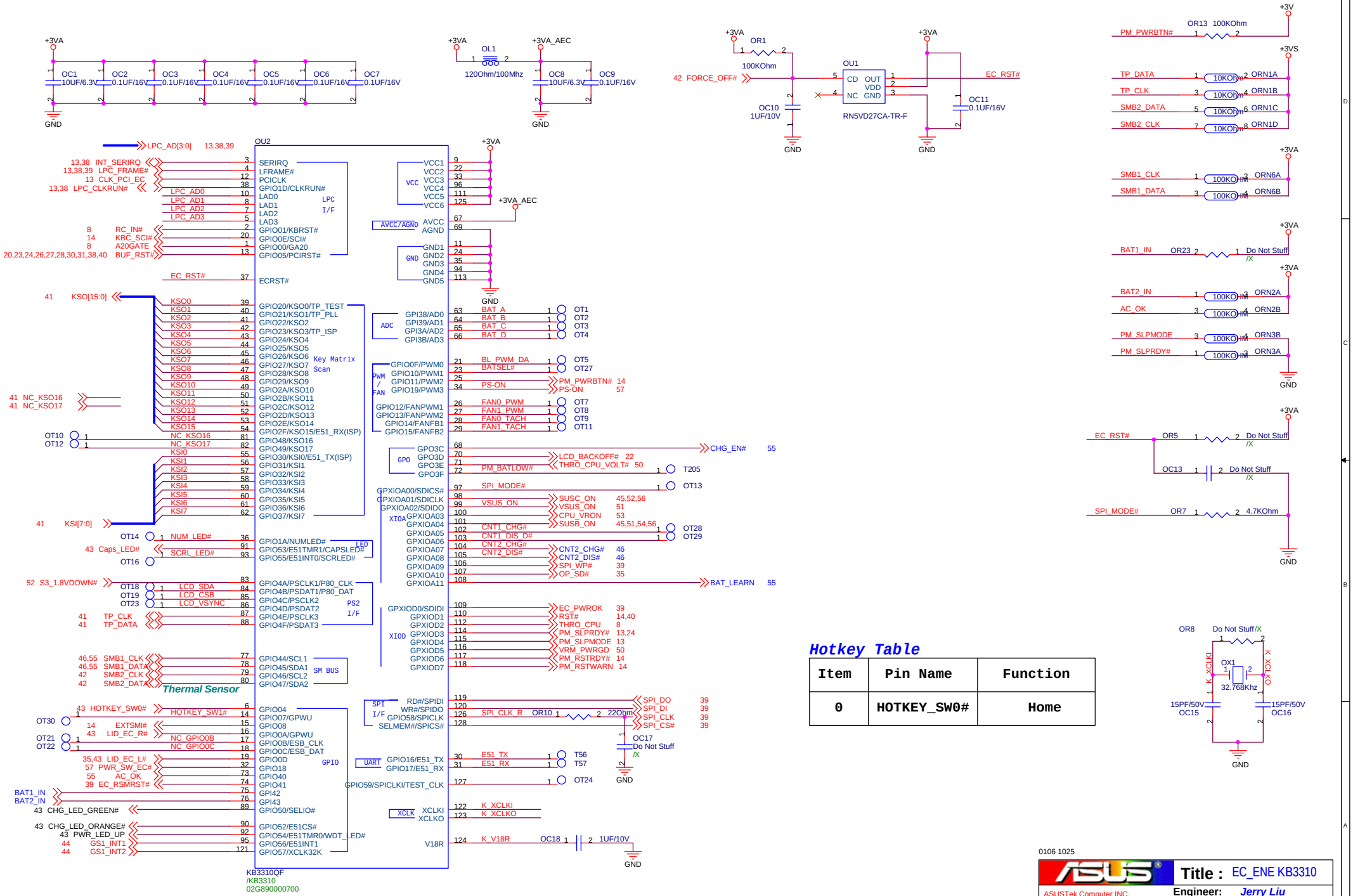


Symbol use 12G140010060
BOM use 12G140010061



0106 1025

ASUSTek Computer Inc.	Title : ALC269-2	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 36 of 57	



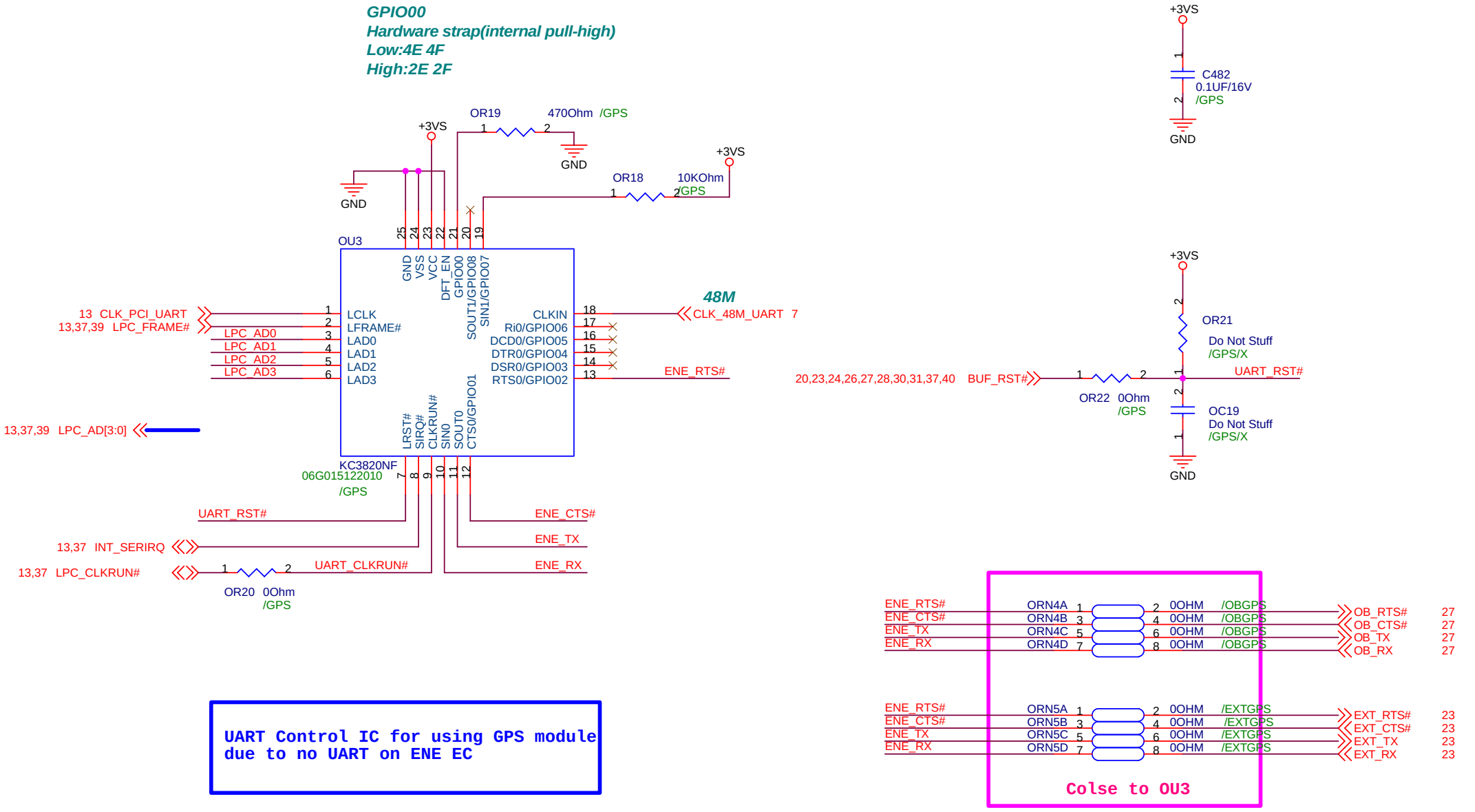
Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home

HOTKEY_SW0# - HOTKEY_SW3# internal PU

0106 1025

ASUSTek Computer INC.	Title : EC_ENE KB3310	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 37 of 57	

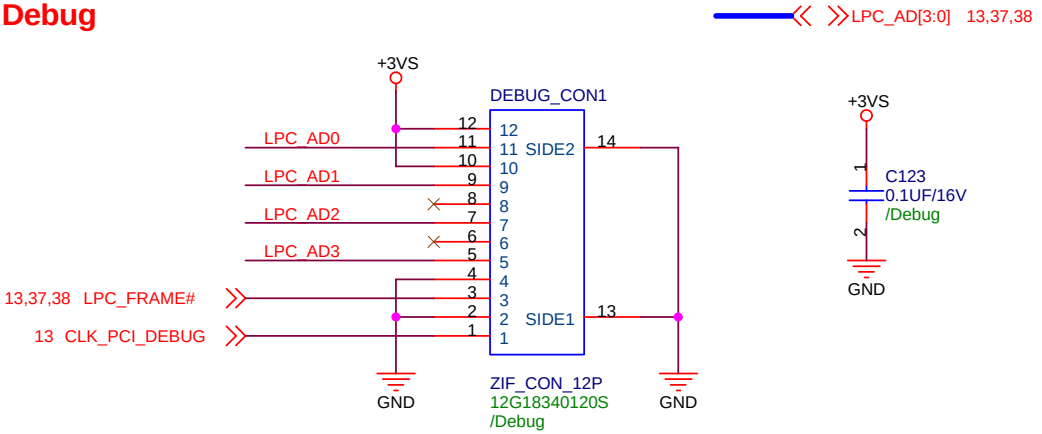


UART Control IC for using GPS module due to no UART on ENE EC

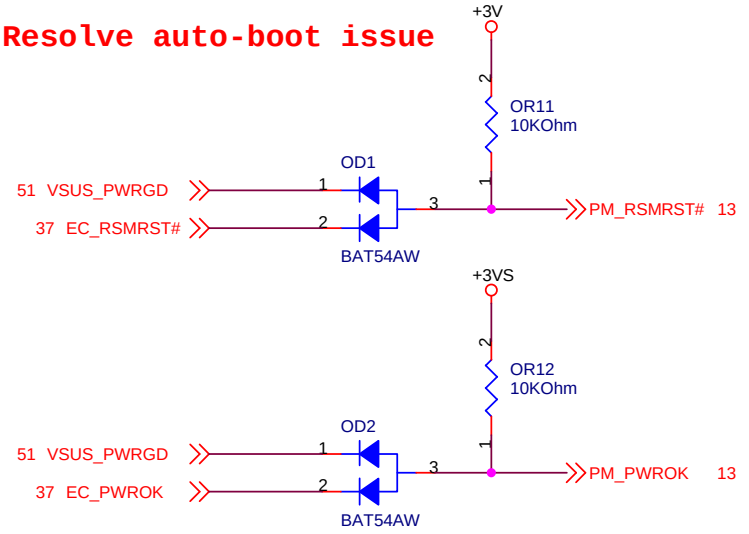
0106 1025

ASUSTek Computer INC.	Title : EC_UART_KC3820	
	Engineer: Jerry_Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 38 of 57	

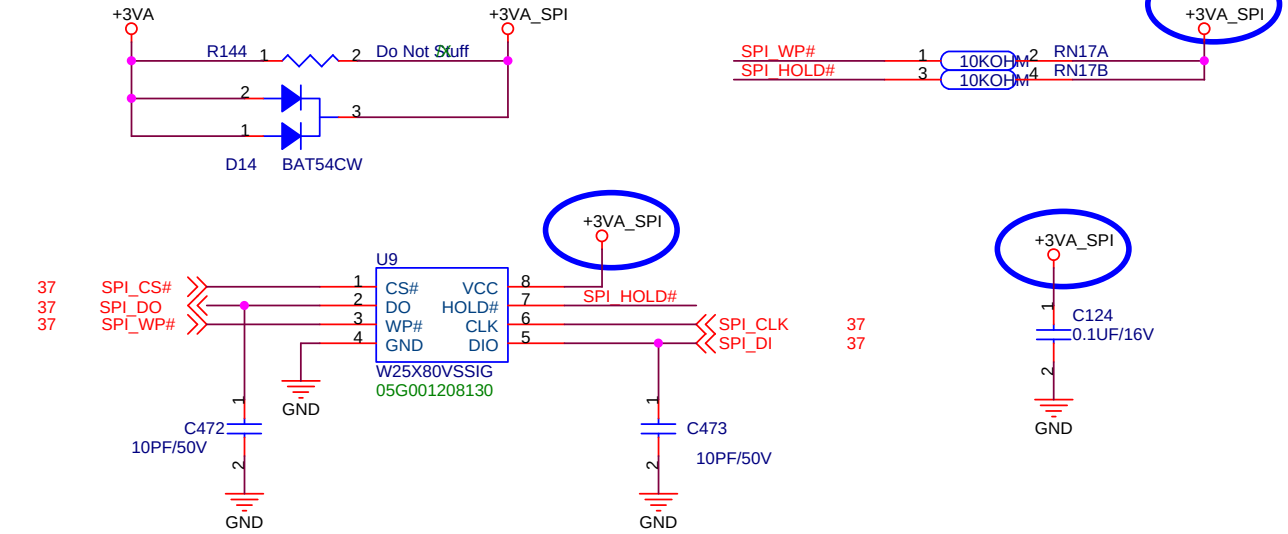
For Debug



Resolve auto-boot issue

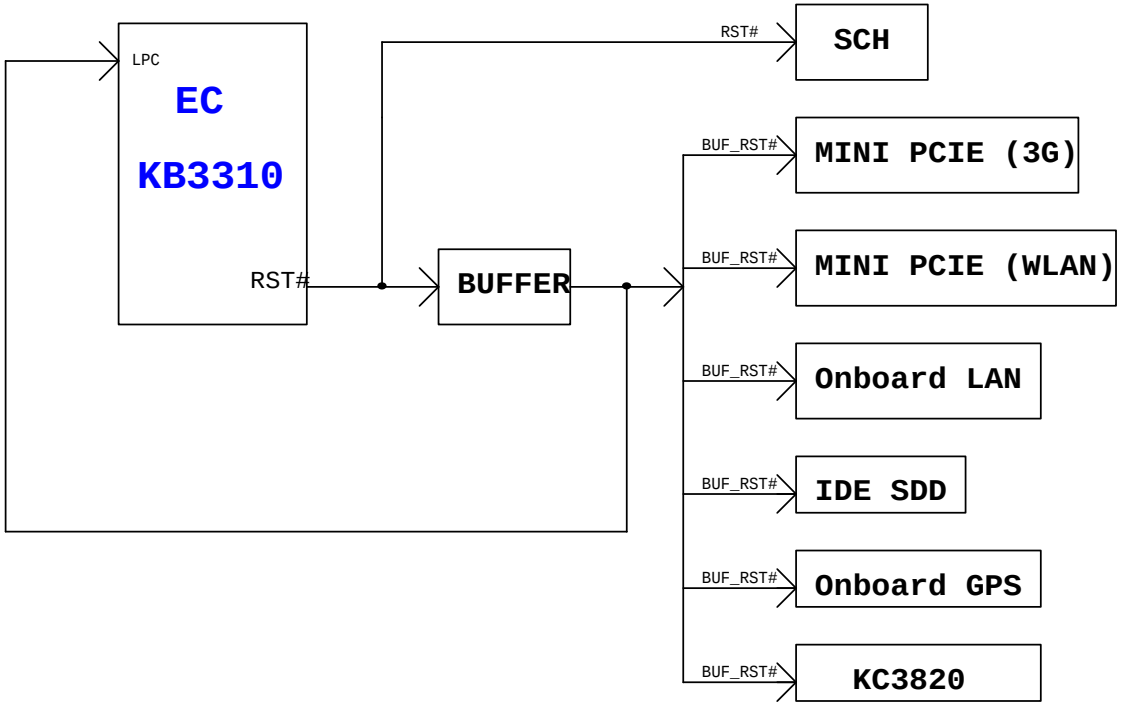


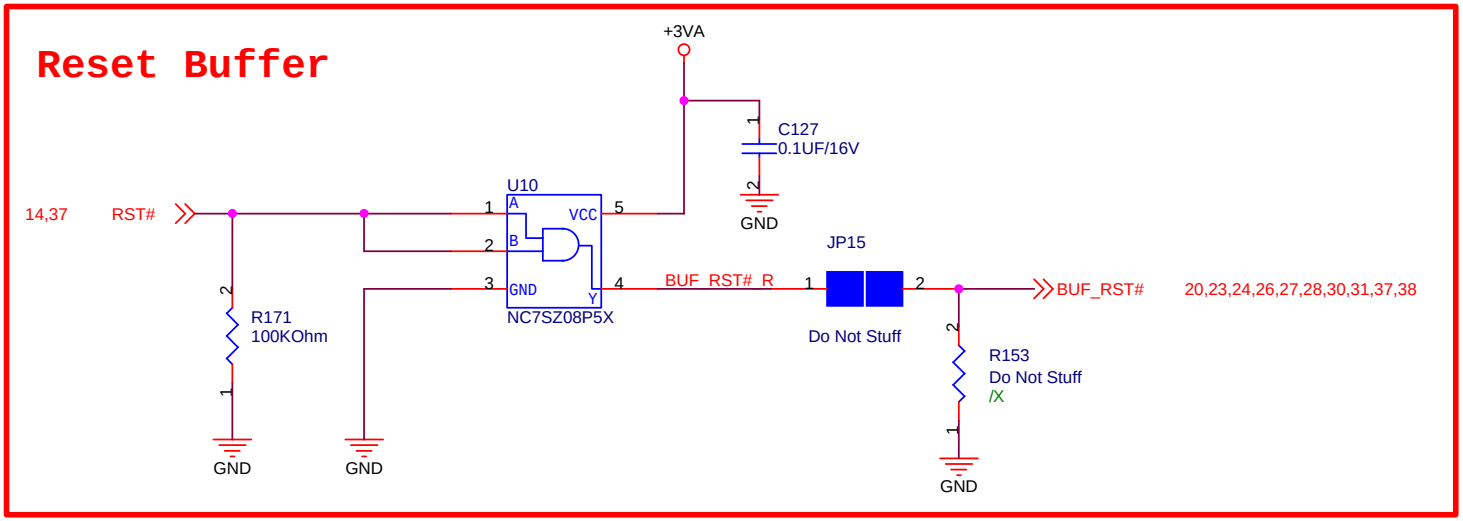
SPI ROM



0106 1025

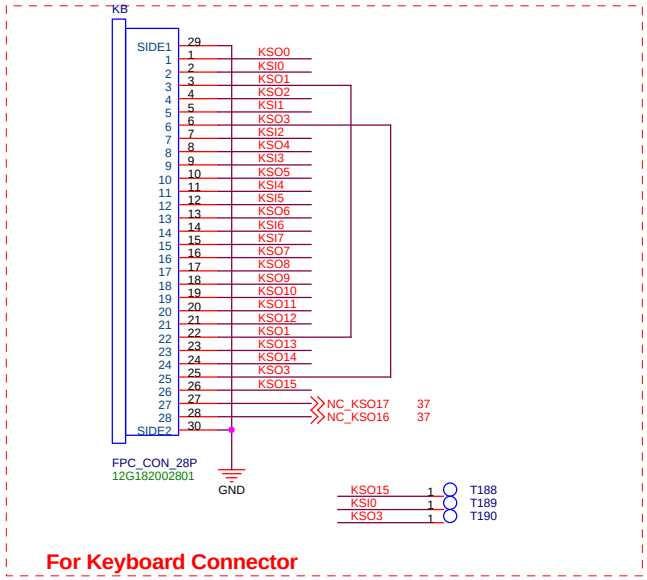
ASUSTek Computer INC.	Title : SPI ROM/ Debug	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 39 of 57	

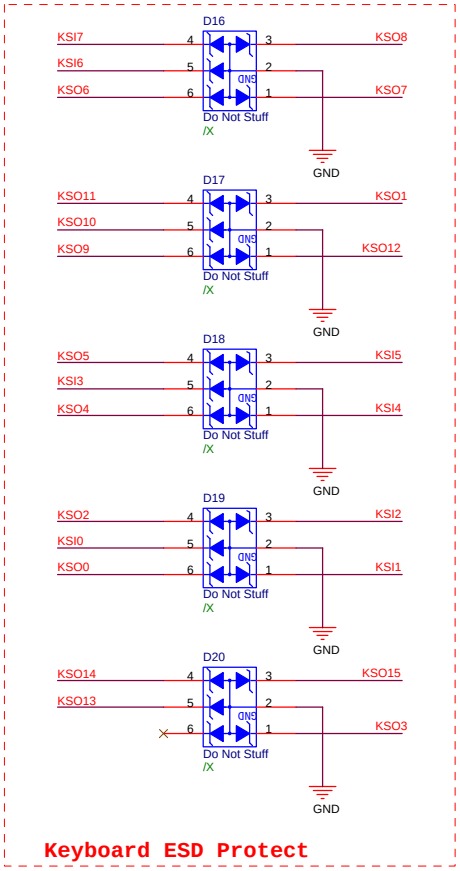


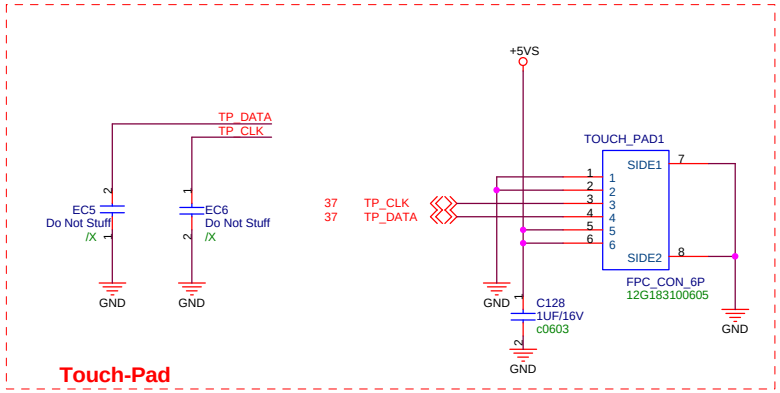


0106 1025

ASUSTeK COMPUTER INC	Title : Reset Map	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 40 of 57	

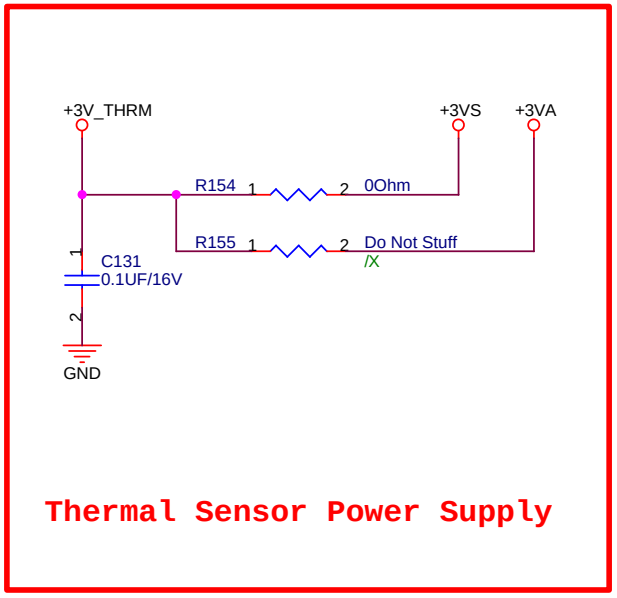


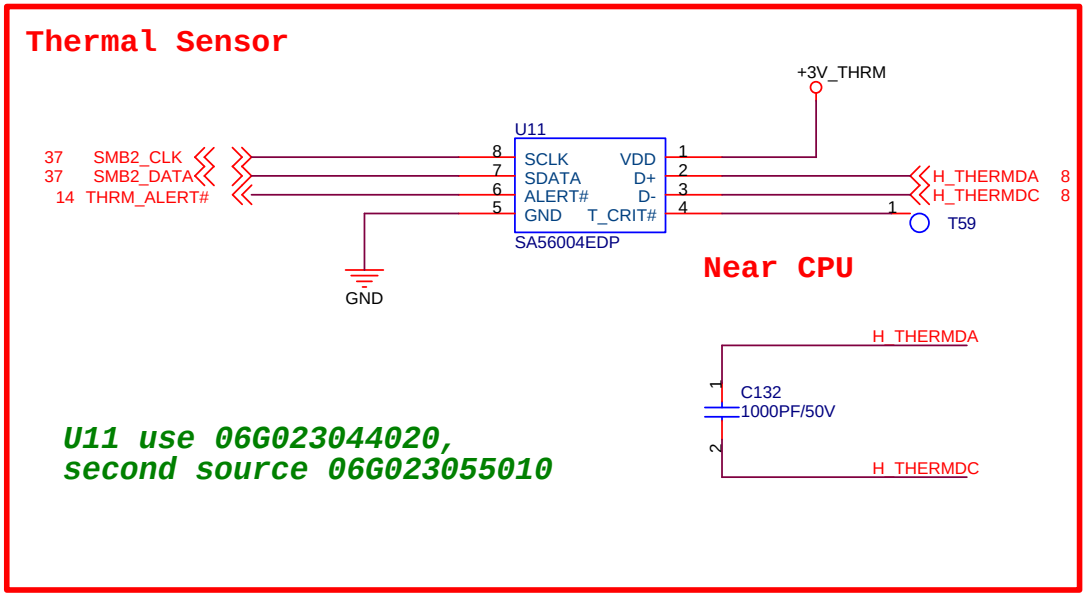


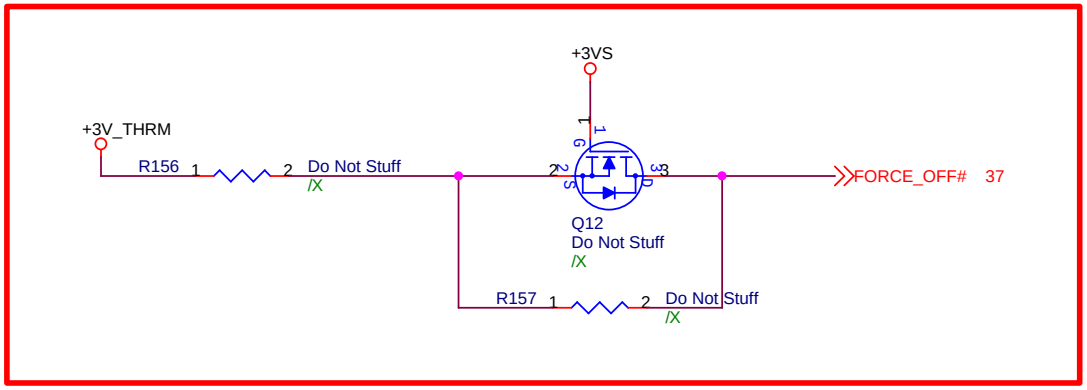


0106 1025

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 41 of 57	

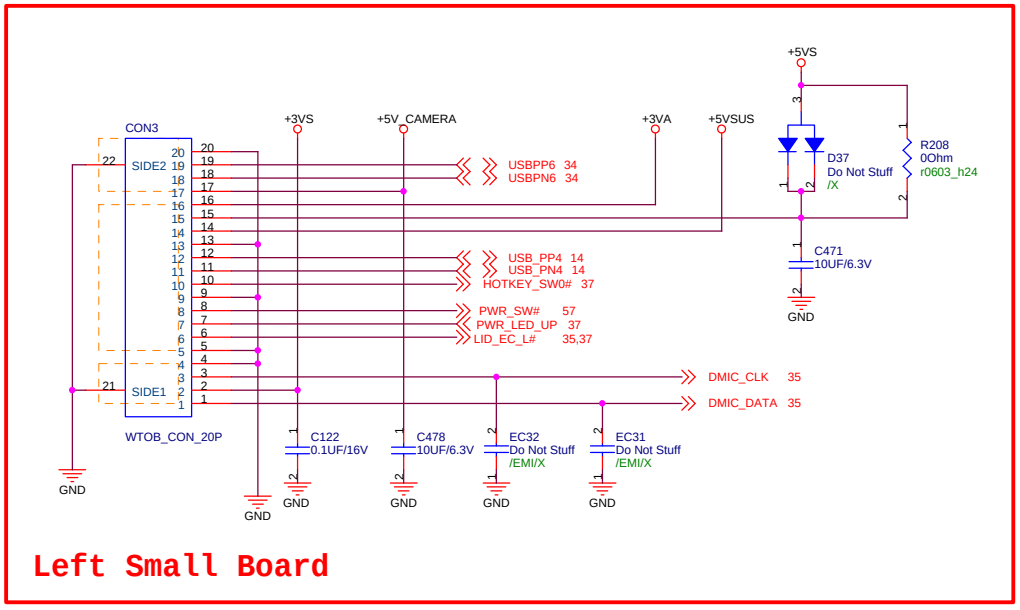




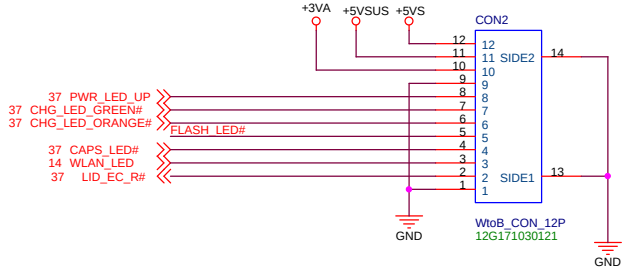


0106 1025

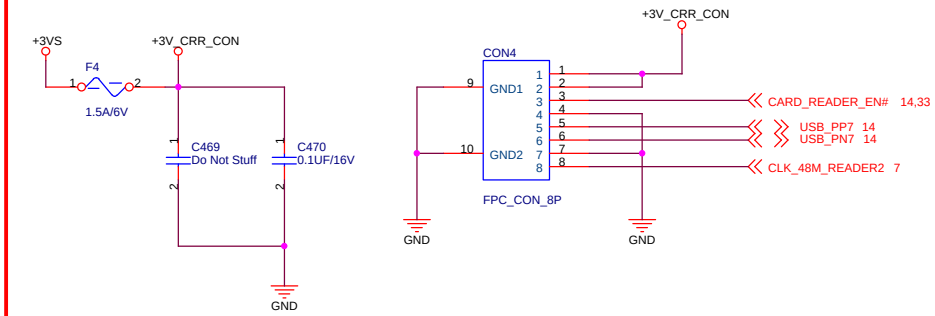
ASUSTek Computer INC.	Title : Thermal Sensor	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 42 of 57	



Left Small Board

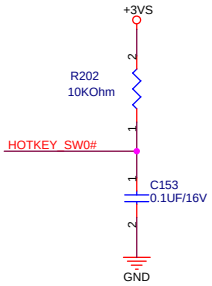


Right Small Board



2nd SD Card Reader

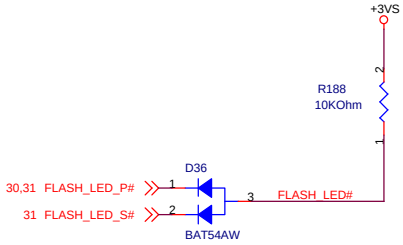
Home Key



Hotkey Table

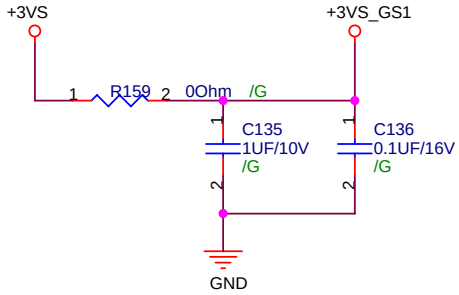
Item	Pin Name	Function
0	HOTKEY_SW0#	HOME

Flash LED

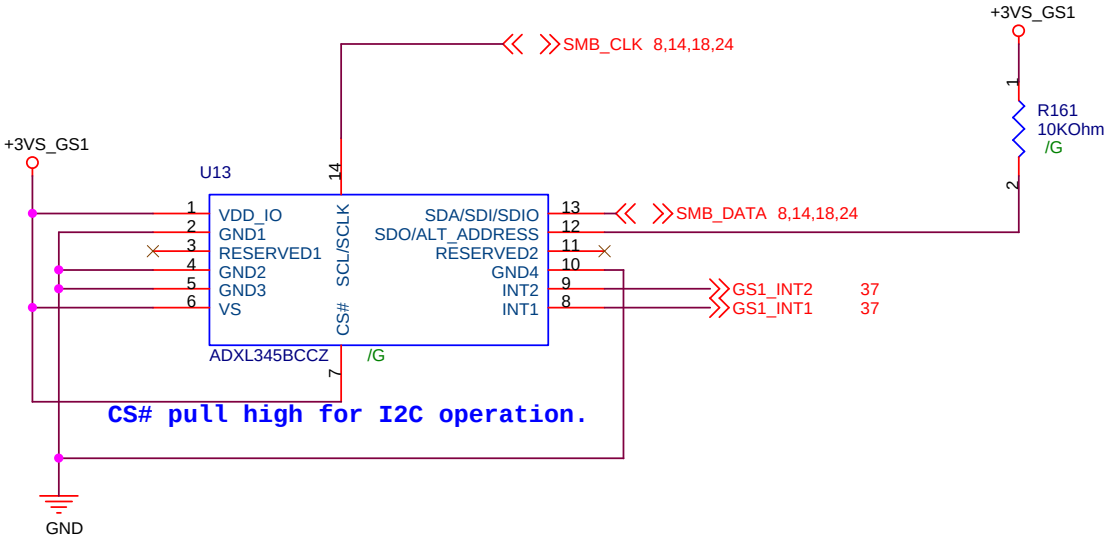


0106 1025

ASUSTek Computer INC.	Title : Small Board Conn	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 43 of 57	

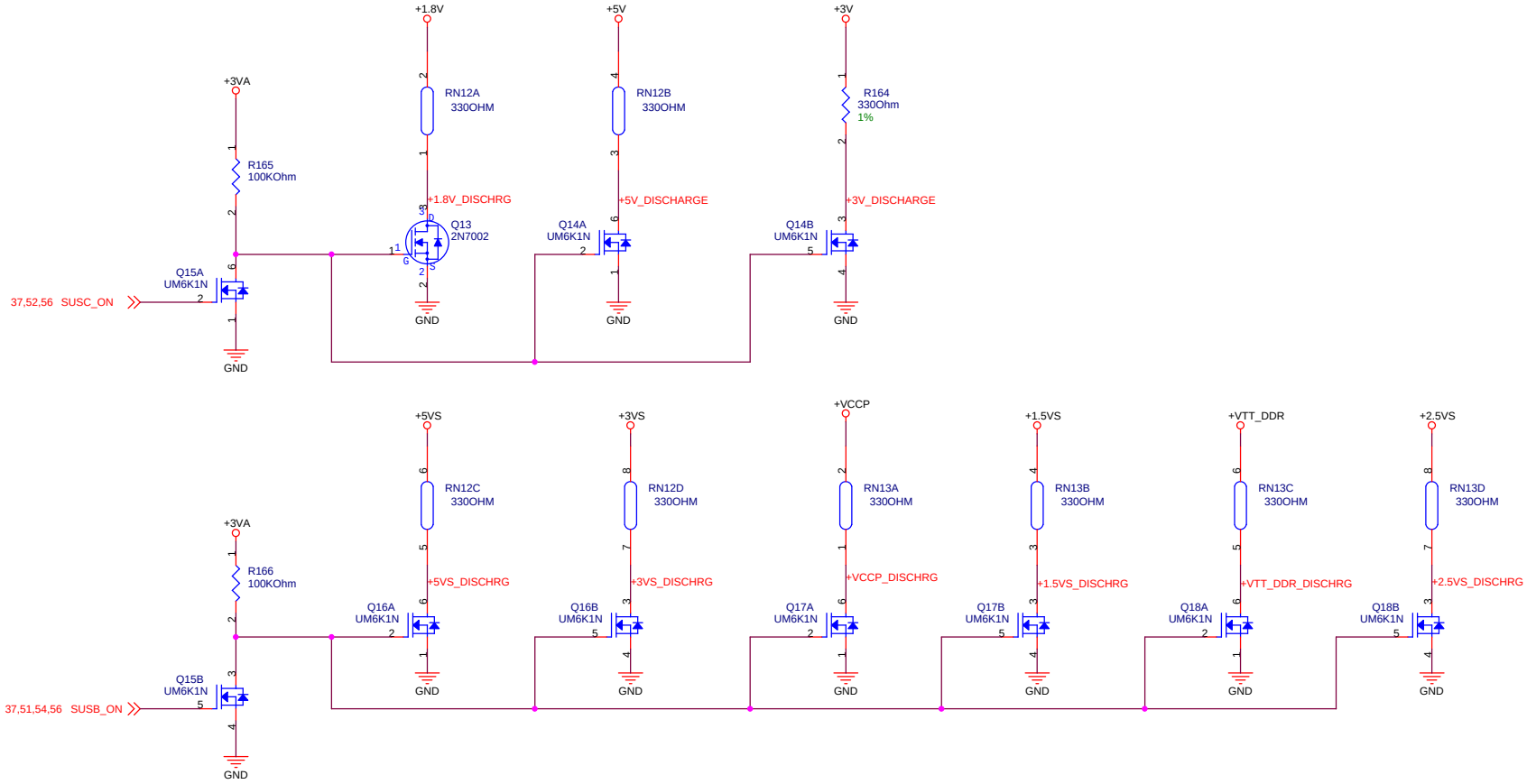


SMBUS Address: 0X1D



0106 1025

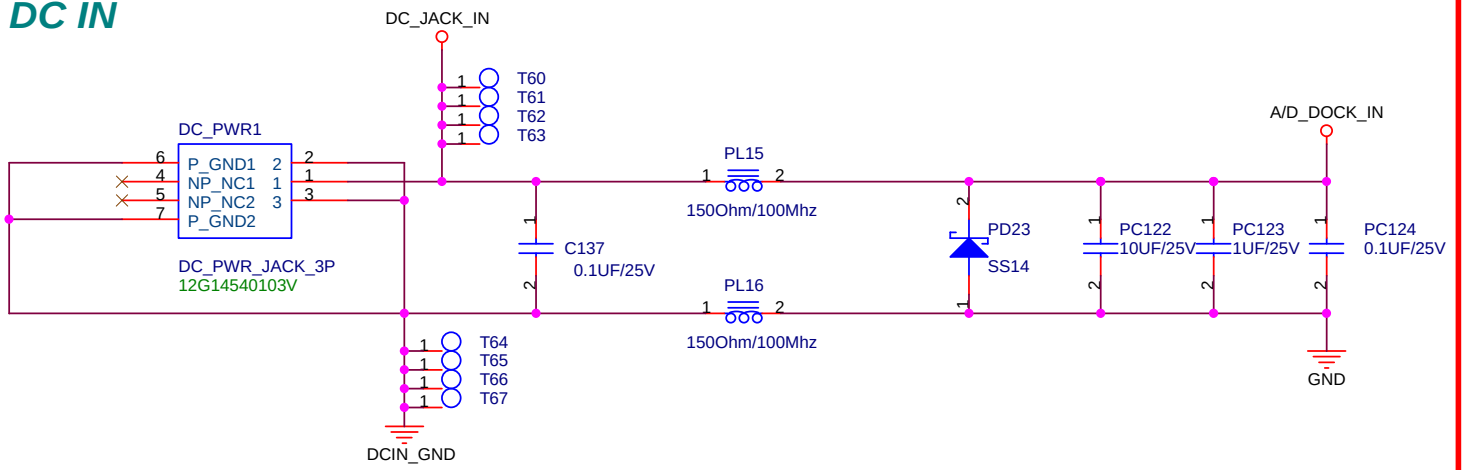
ASUSTek Computer INC.	Title : G-Sensor	
	Engineer: *Jerry Liu*	
Size: A4	Project Name: **T91**	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 44 of 57	



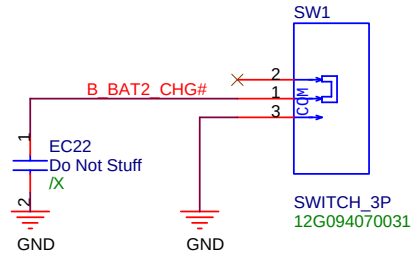
0106 1025

ASUSTek Computer INC.	Title : Discharge	
	Engineer: *Jerry Liu*	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 45 of 57	

DC IN

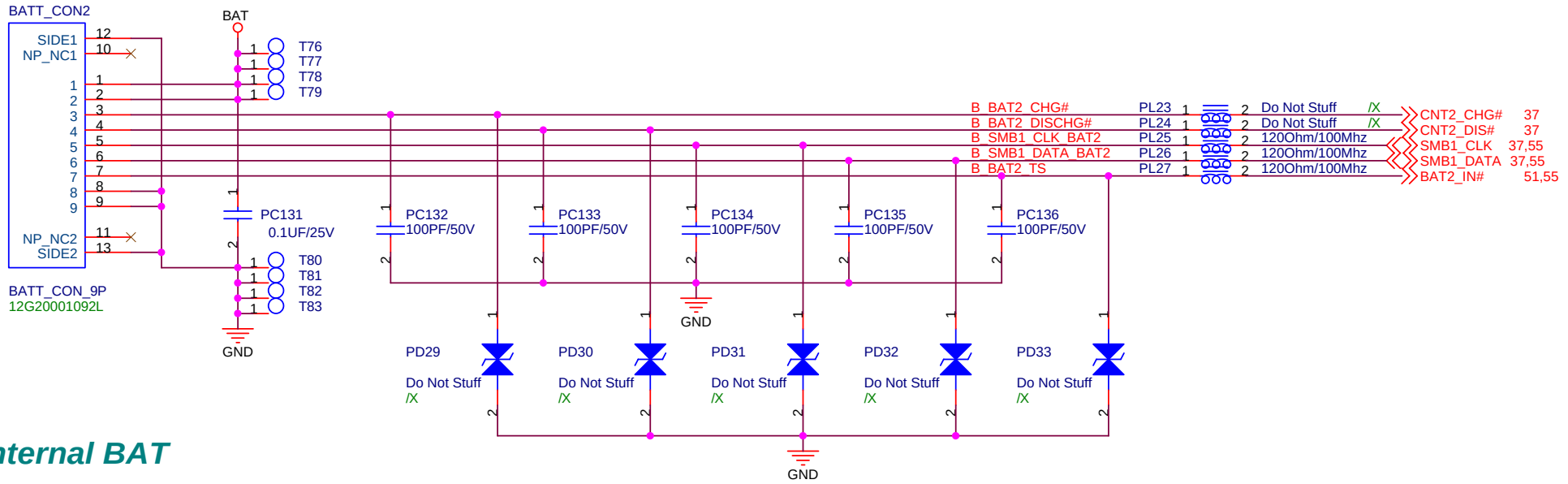


Battery Switch



CNT2_CHG# : Low : Battery ON

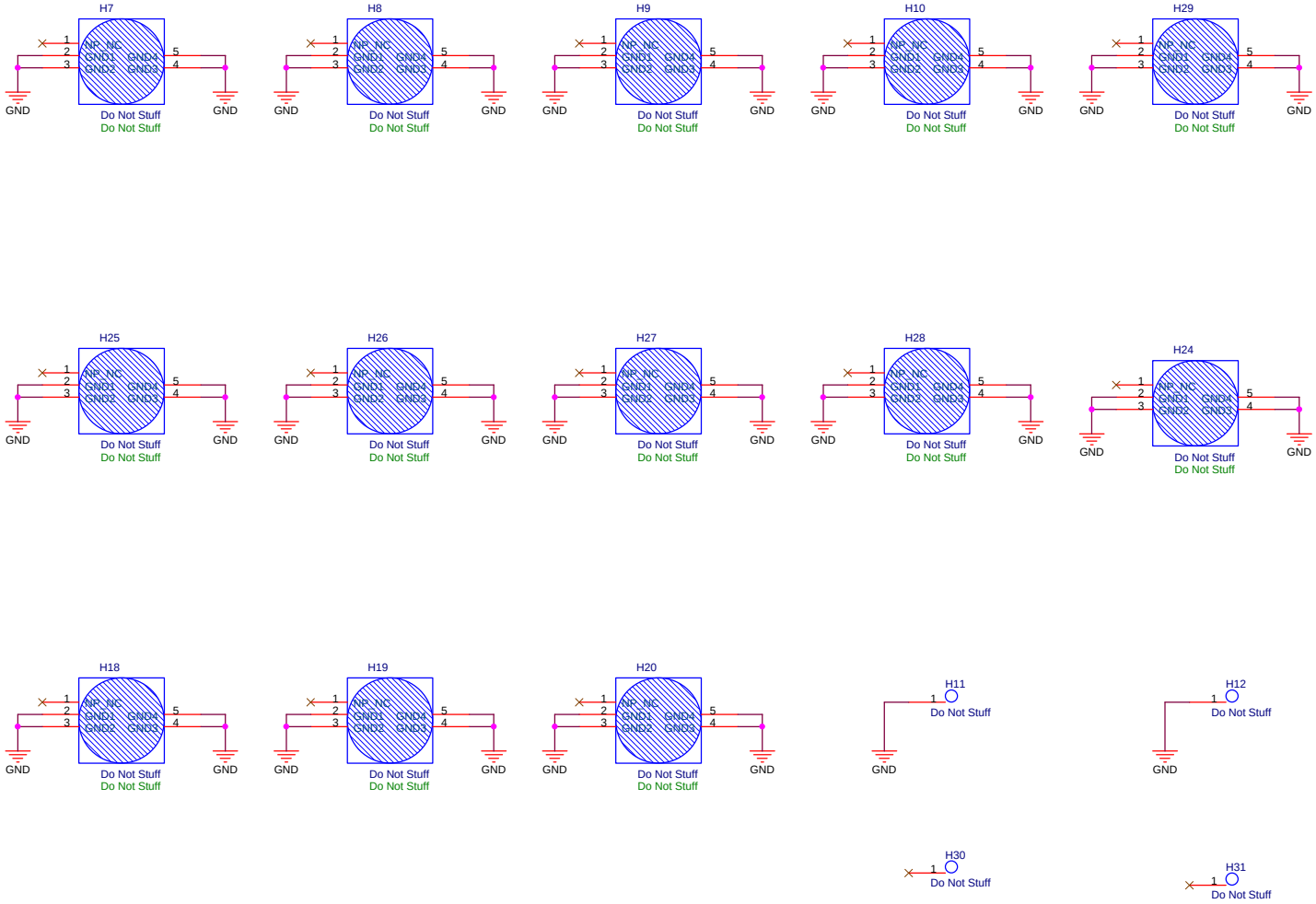
CNT2_CHG# : open : Battery OFF



Internal BAT

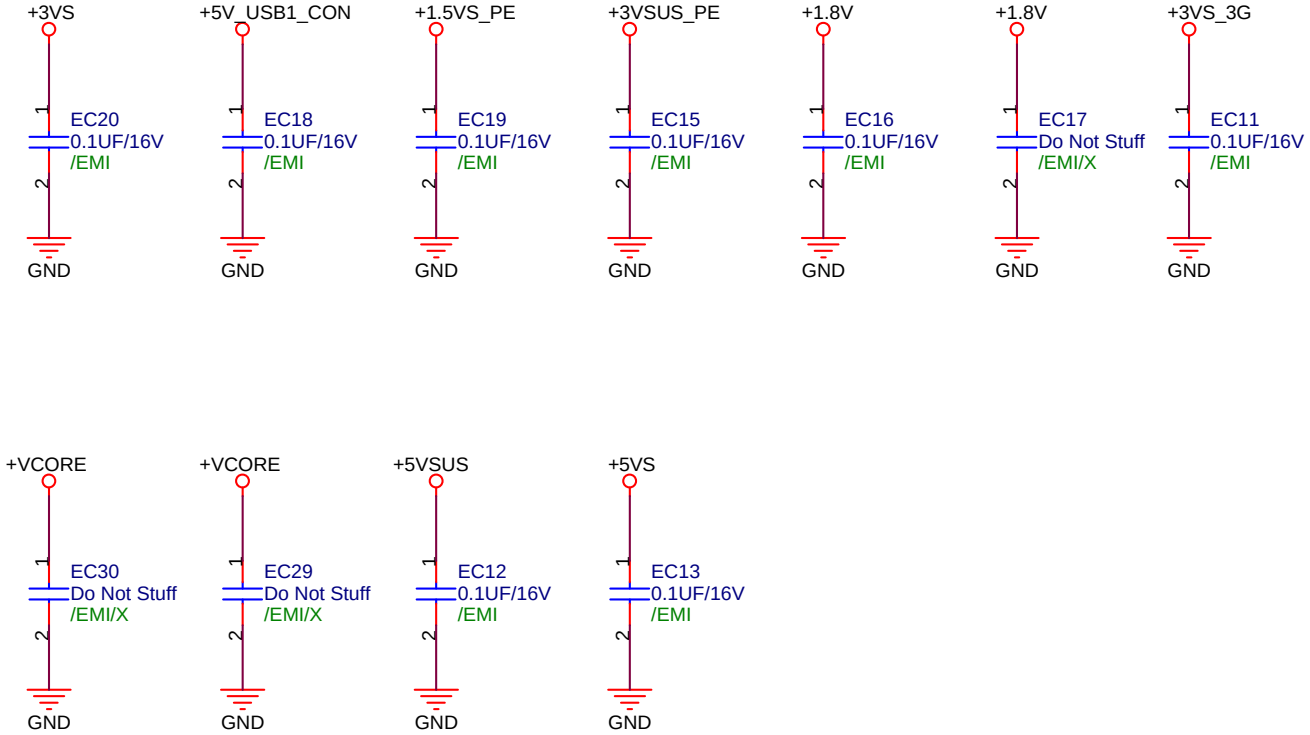
0106 1025

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 46 of 57	



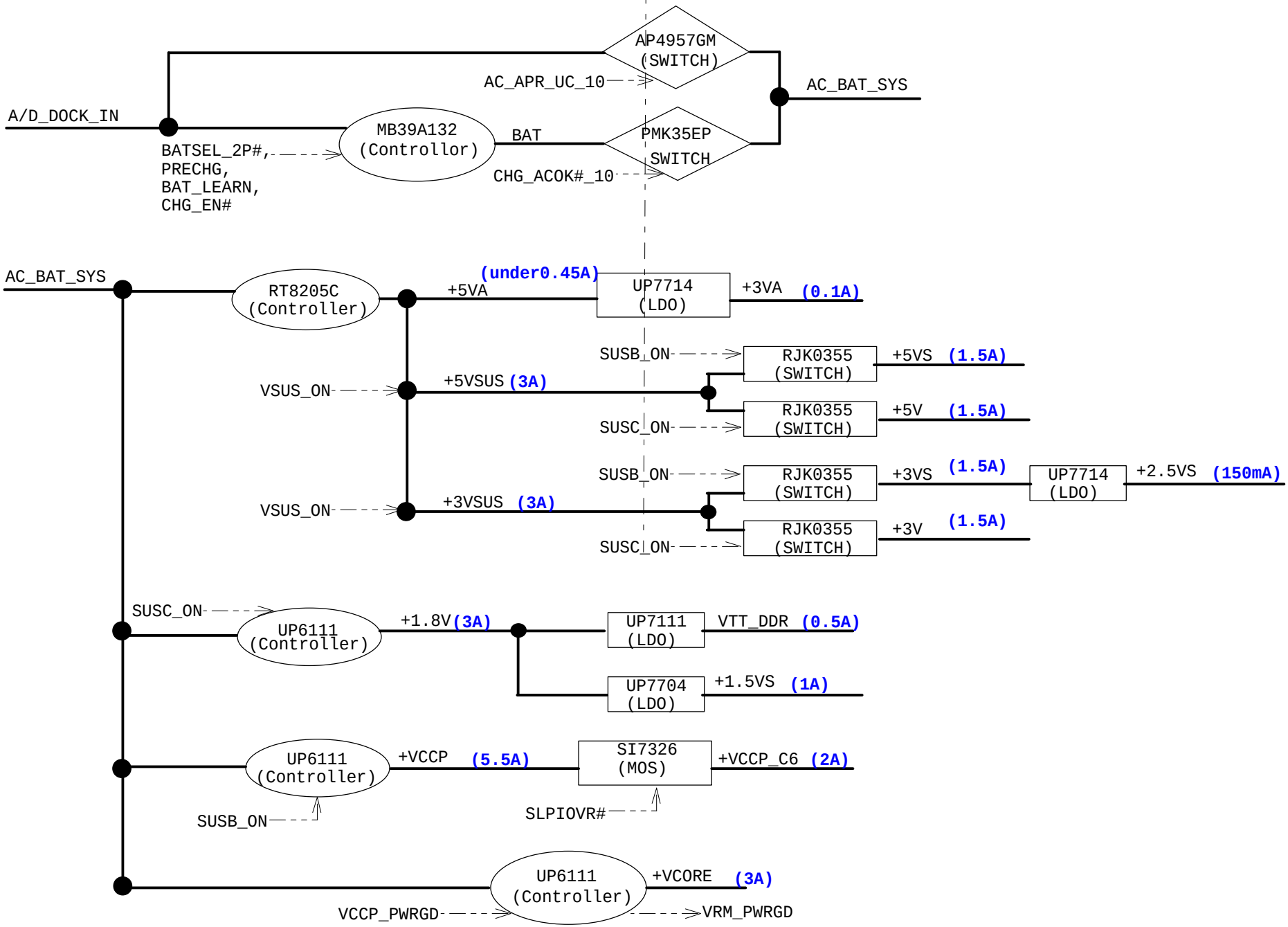
0106 1025

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 47 of 57	



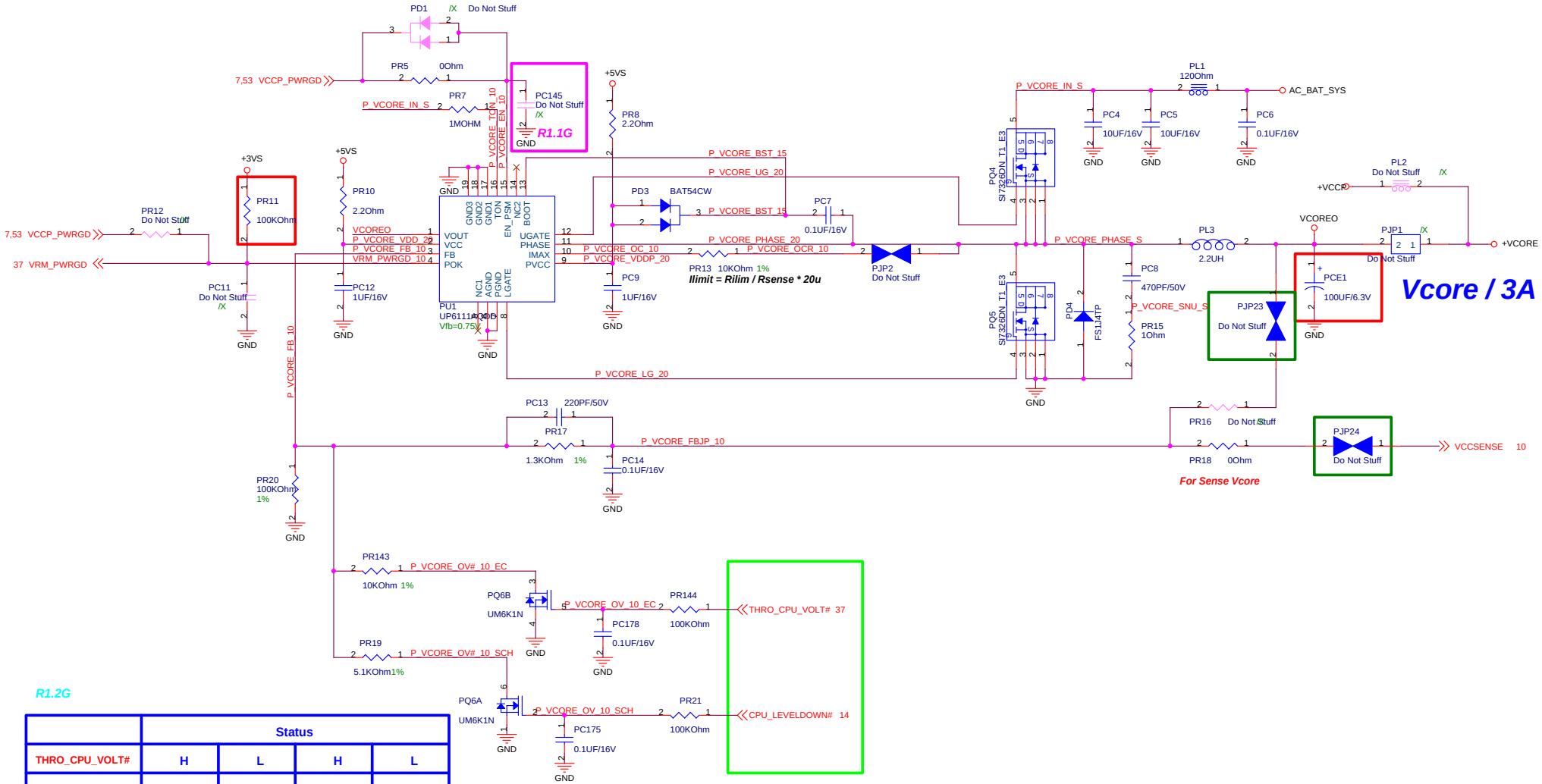
0106 1025

ASUSTek Computer INC.	Title : EMI	
	Engineer: Jerry Liu	
Size: A	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 48 of 57	



0106 1025

ASUSTek Computer INC.	Title : Power Flow	
	Engineer: Jerry Liu	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 49 of 57	



R1.2G

	Status			
THRO_CPU_VOLT#	H	L	H	L
CPU_LEVELDOWN#	H	H	L	L
Voltage	1.0484V	0.9509V	0.8573V	0.7598V
	Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

0106 1025

ASUSTek Computer INC.

Title : Vcore

Engineer: Joy_Zhou

Size	Project Name	Rev
Custom	T91	1.2G

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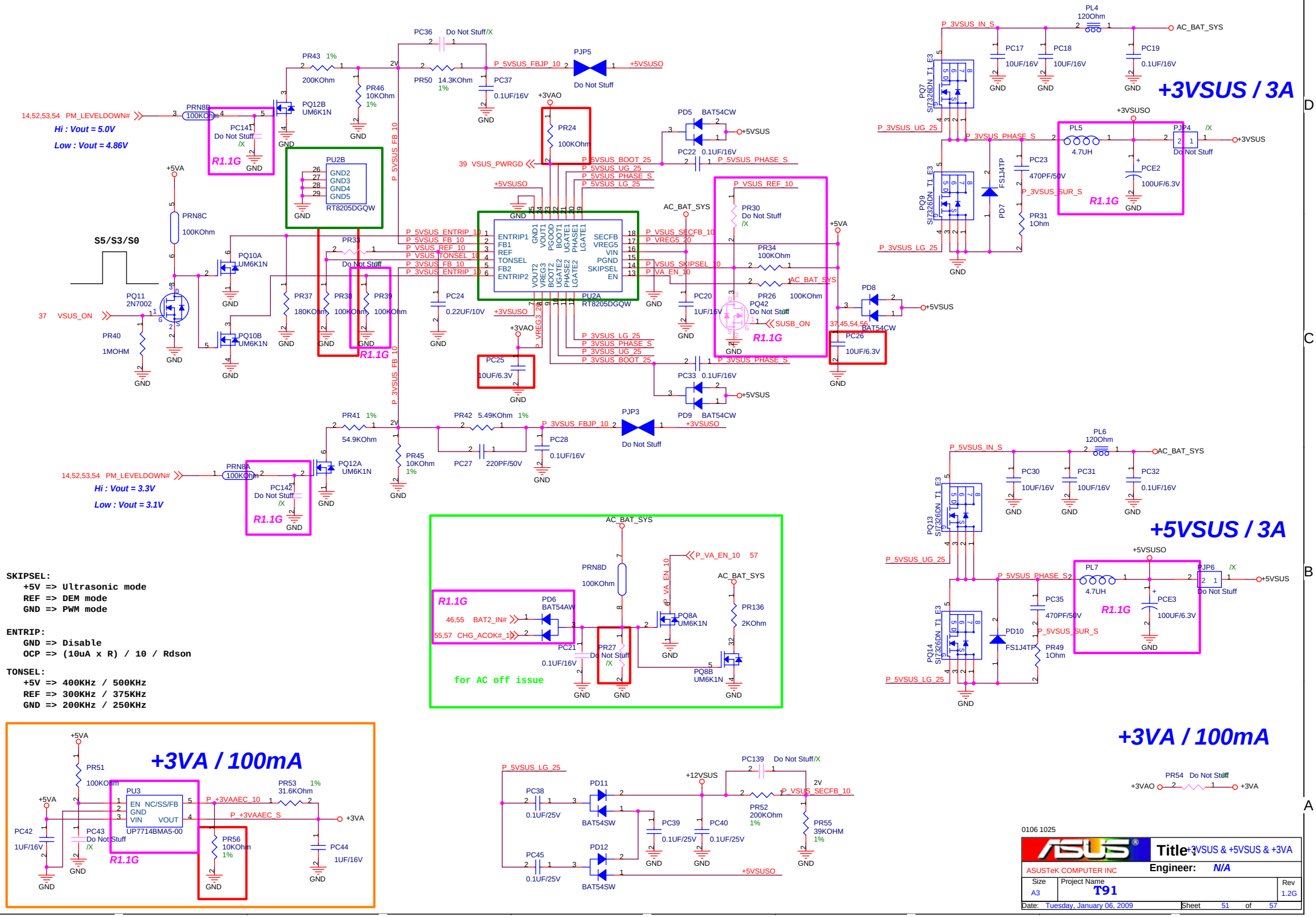
+3VSUS / 3A
+5VSUS / 3A
+3VA / 100mA
+3VA / 100mA
S5/S3/S0
Hi : Vout = 5.0V
Low : Vout = 4.86V
Hi : Vout = 3.3V
Low : Vout = 3.1V
SKIPSEL:
+5V => Ultrasonic mode
REF => DEM mode
GND => PWM mode
ENTRIP:
GND => Disable
OCP => (10uA x R) / 10 / Rdson
TONSEL:
+5V => 400KHz / 500KHz
REF => 300KHz / 375KHz
GND => 200KHz / 250KHz
for AC off issue
R1.1G
Title: +3VSUS & +5VSUS & +3VA
ASUSTeK COMPUTER INC
Engineer: N/A
Project Name T91
Size A3
Rev 1.2G
Date: Tuesday, January 06, 2009
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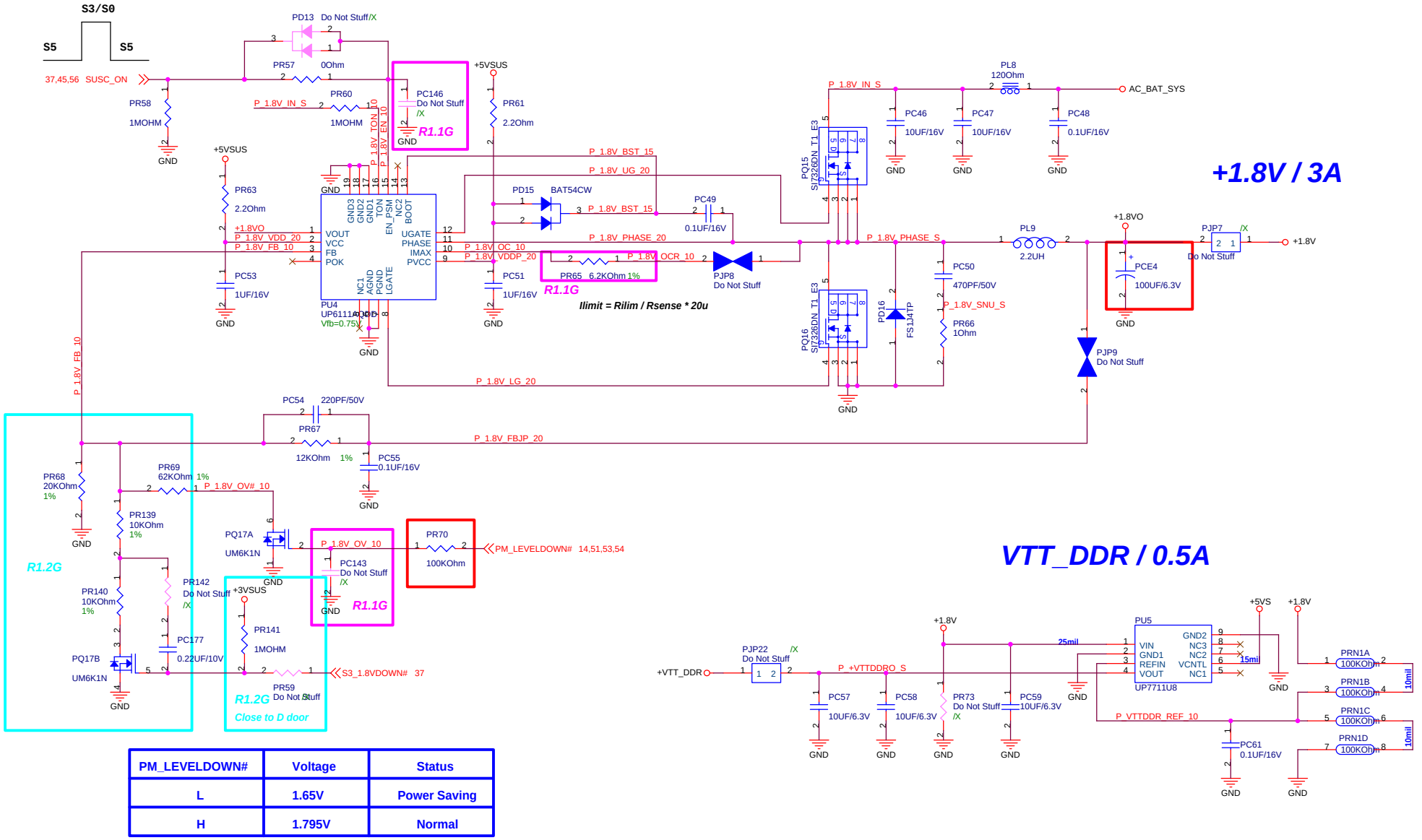
0106 1025



PM_LEVELDOWN#	Voltage	Status
L	1.65V	Power Saving
H	1.795V	Normal

0106 1025

ASUSTek Computer INC.	Title : +1.8V & VTTDDR	
	Engineer: Joy_Zhou	
Size: A3	Project Name: T91	Rev: 1.2G
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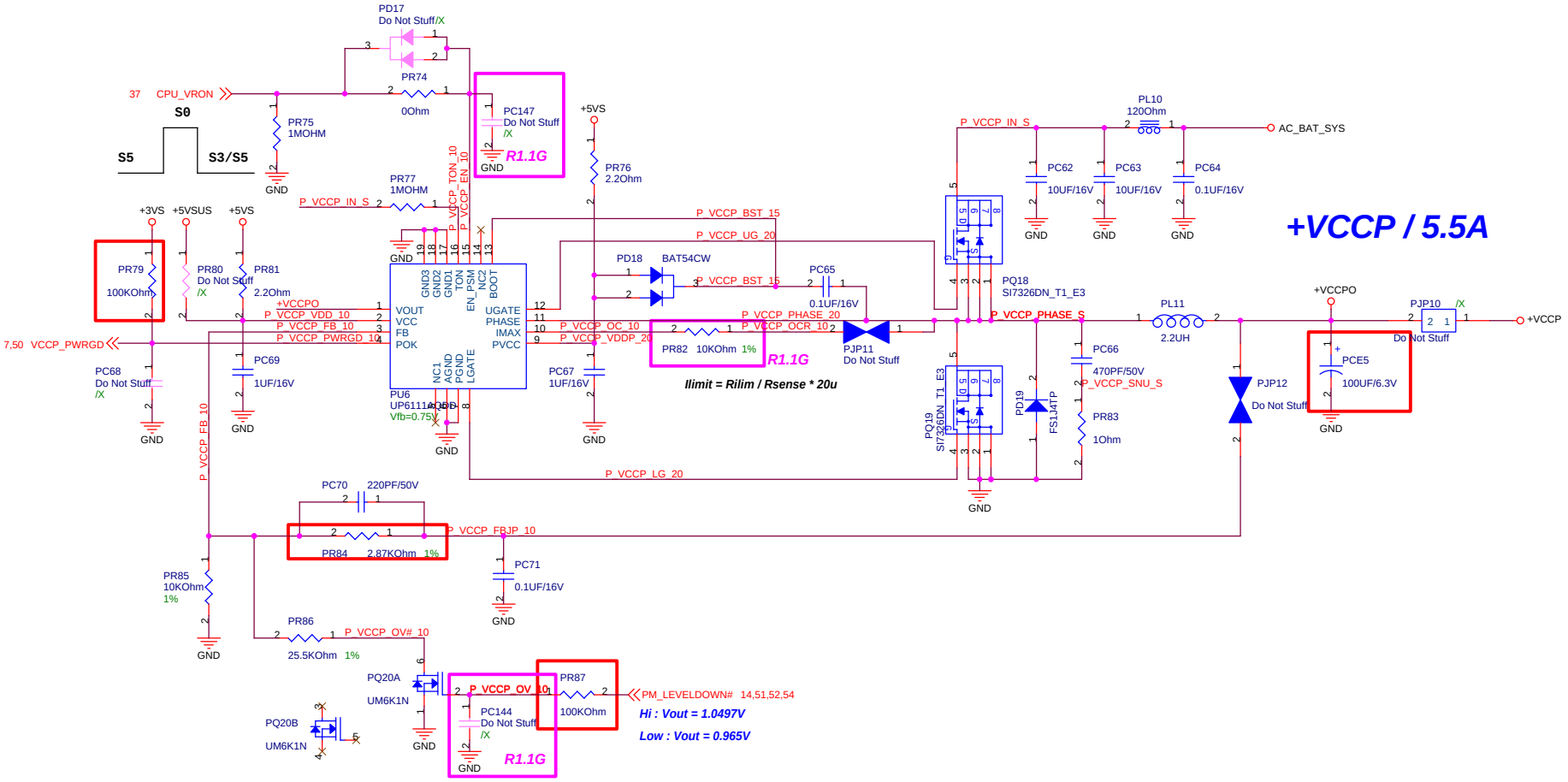

PM_LEVELDOWN#	Voltage	Status
L	0.965V	Power Saving
H	1.0497V	Normal

0106 1025

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A3	Project Name: T91	Rev: 1.2G
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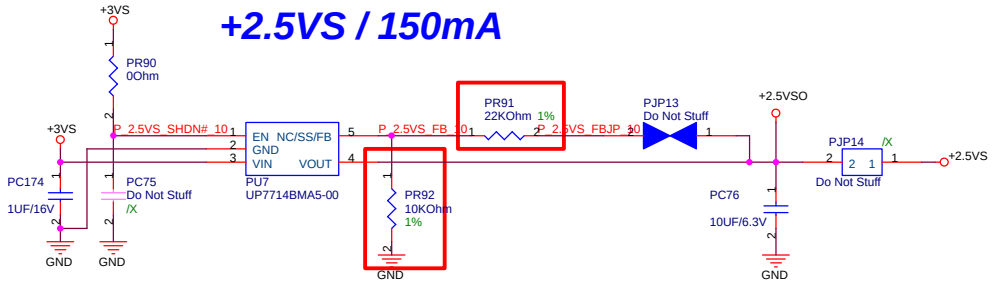
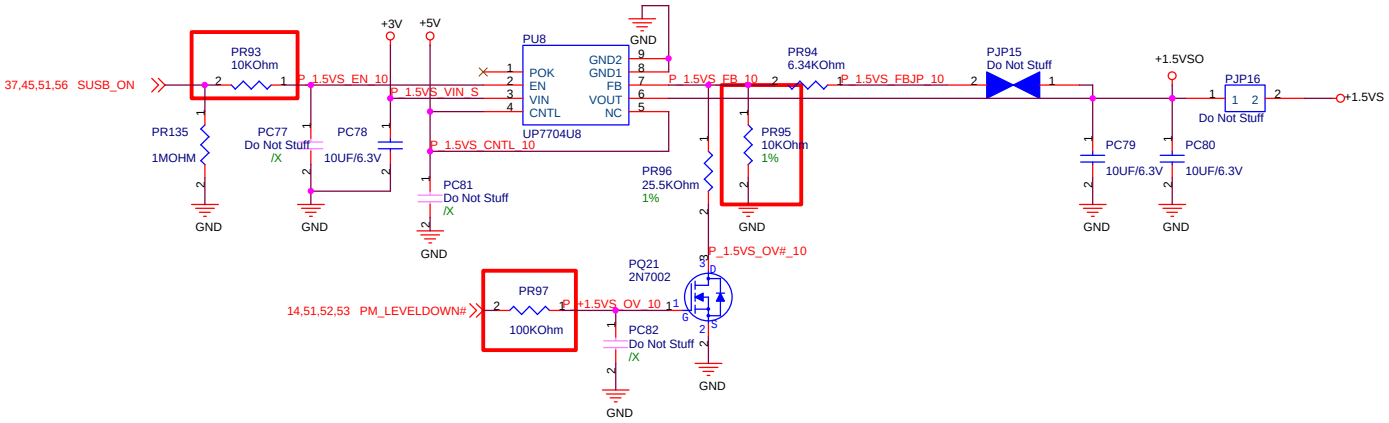
+2.5VS / 150mA

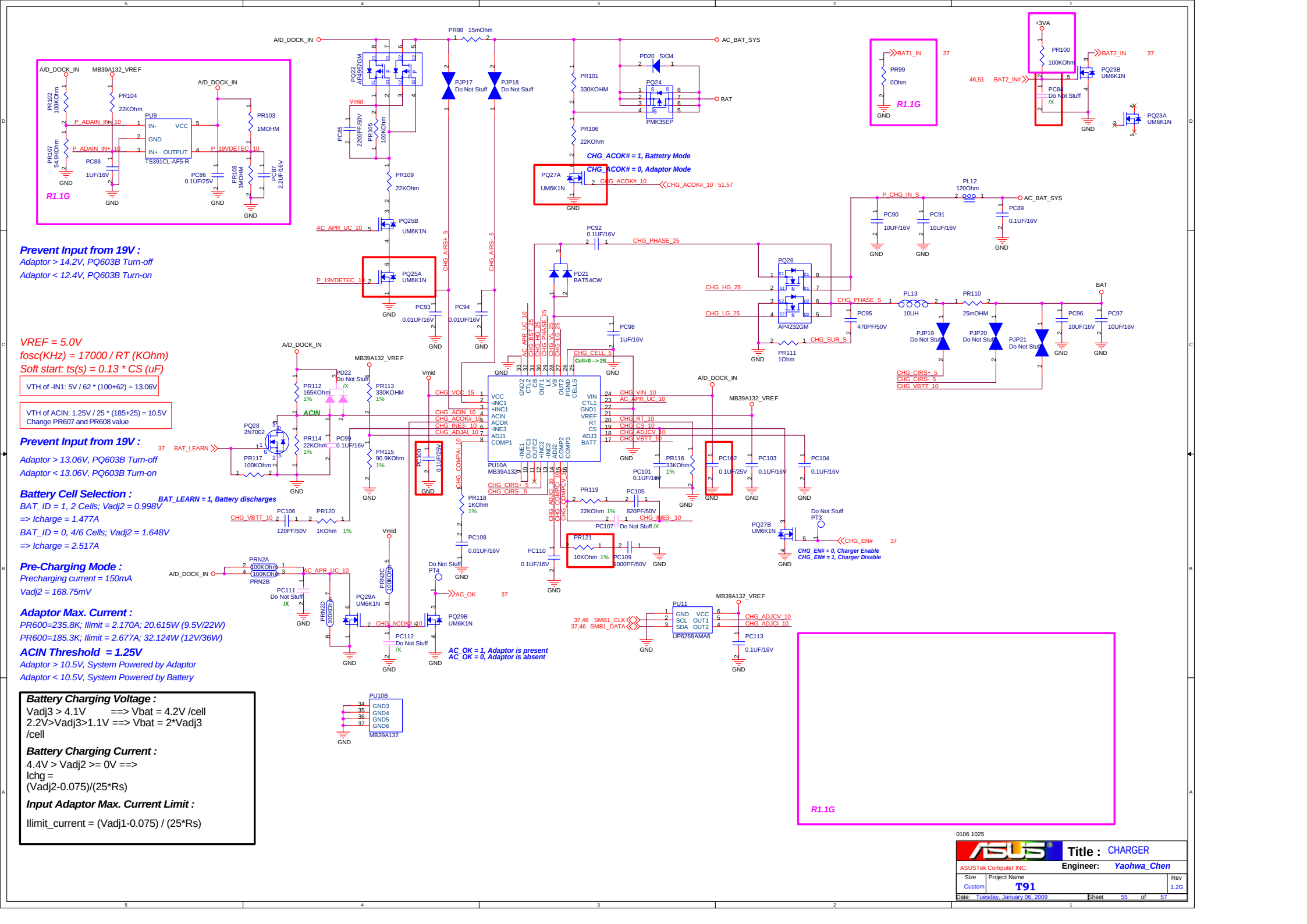


+1.5VS / 1A



0106 1025

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: T91	Rev: 1.2G
Date: Tuesday, January 06, 2009	Sheet 54 of 57	



Prevent Input from 19V :

Adaptor > 14.2V, PQ603B Turn-off

Adaptor < 12.4V, PQ603B Turn-on

VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.13 * CS (uF)*

VTH of -IN1: 5V / 62 * (100+62) = 13.06V

VTH of ACIN: 1.25V / 25 * (185+25) = 10.5V
Change PR607 and PR608 value

Prevent Input from 19V :

Adaptor > 13.06V, PQ603B Turn-off

Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :

BAT_LEARN = 1, Battery discharges

BAT_ID = 1, 2 Cells; Vadj2 = 0.998V

=> Icharge = 1.477A

BAT_ID = 0, 4/6 Cells; Vadj2 = 1.648V

=> Icharge = 2.517A

Pre-Charging Mode :

Precharging current = 150mA

Vadj2 = 168.75mV

Adaptor Max. Current :

PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)

PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)

ACIN Threshold = 1.25V

Adaptor > 10.5V, System Powered by Adaptor

Adaptor < 10.5V, System Powered by Battery

Battery Charging Voltage :

Vadj3 > 4.1V ==> Vbat = 4.2V /cell

2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Charging Current :

4.4V > Vadj2 >= 0V ==>

Ichg =

(Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)

0106 1025

ASUSTek Computer INC.

Title : CHARGER

Engineer: Yaohwa_Chen

Size	Project Name	Rev
Custom	T91	1.2G

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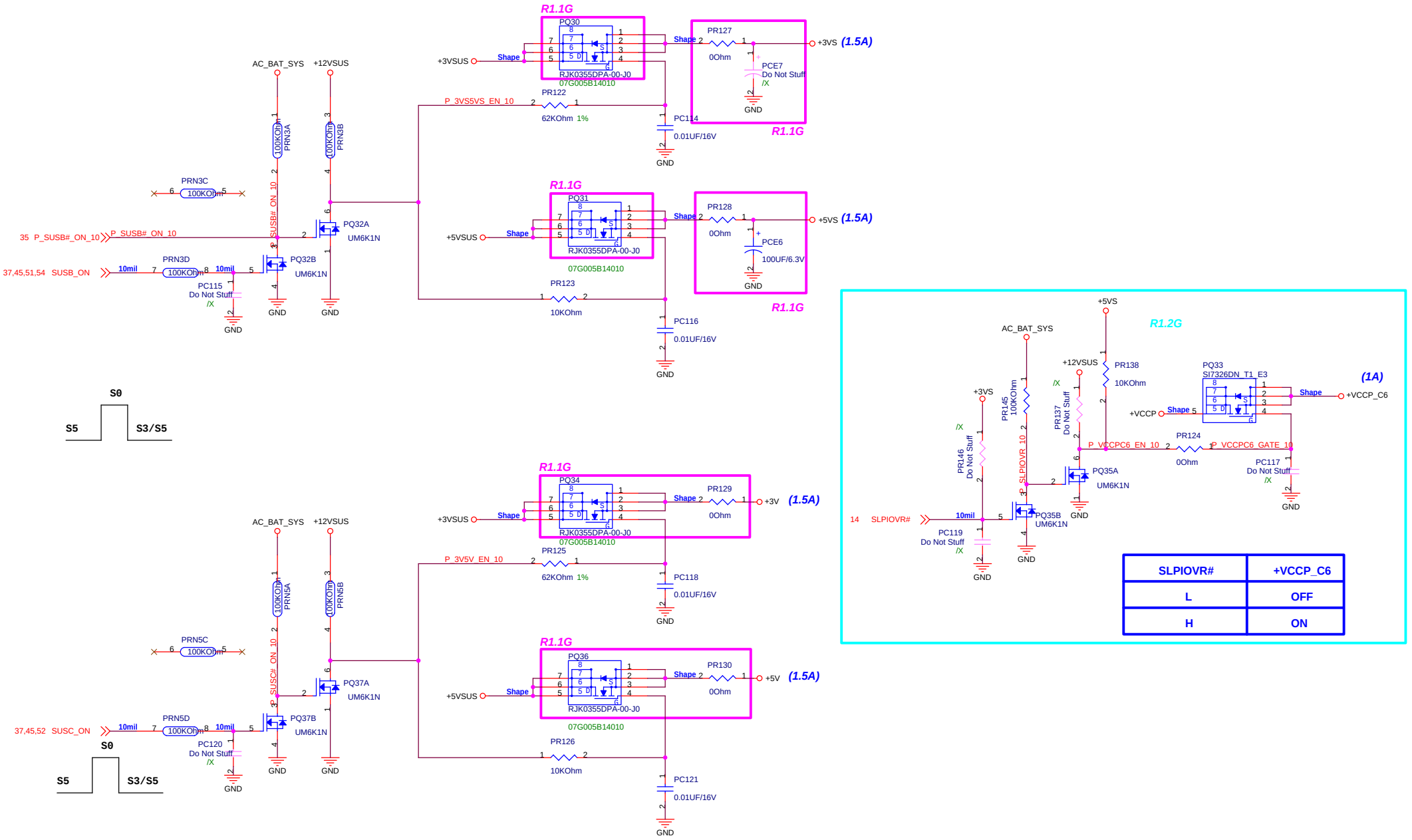

0106 1025

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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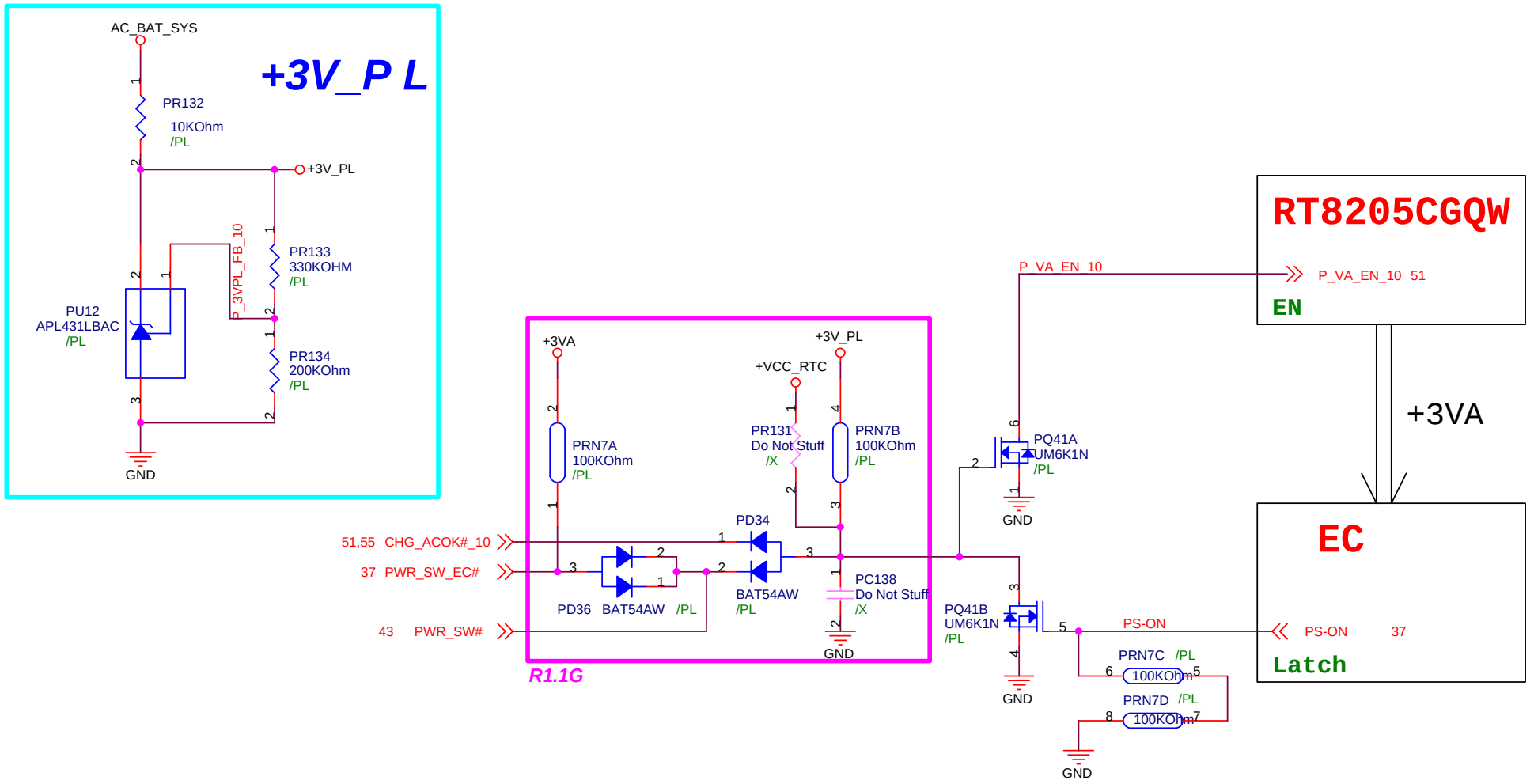

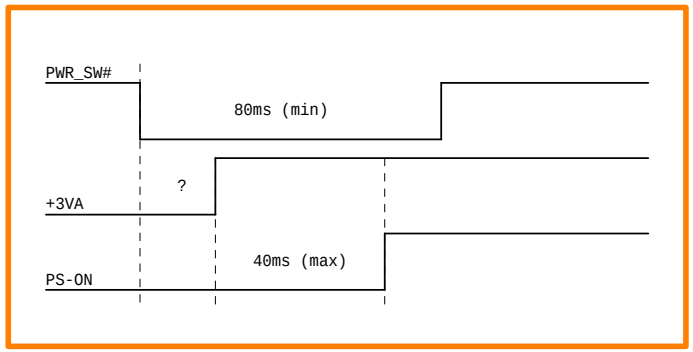

0106 1025

ASUSTek Computer INC.	Title : Power Latch	
	Engineer: Jerry Liu	
Size: A4	Project Name: T91	Rev: 1.2G
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