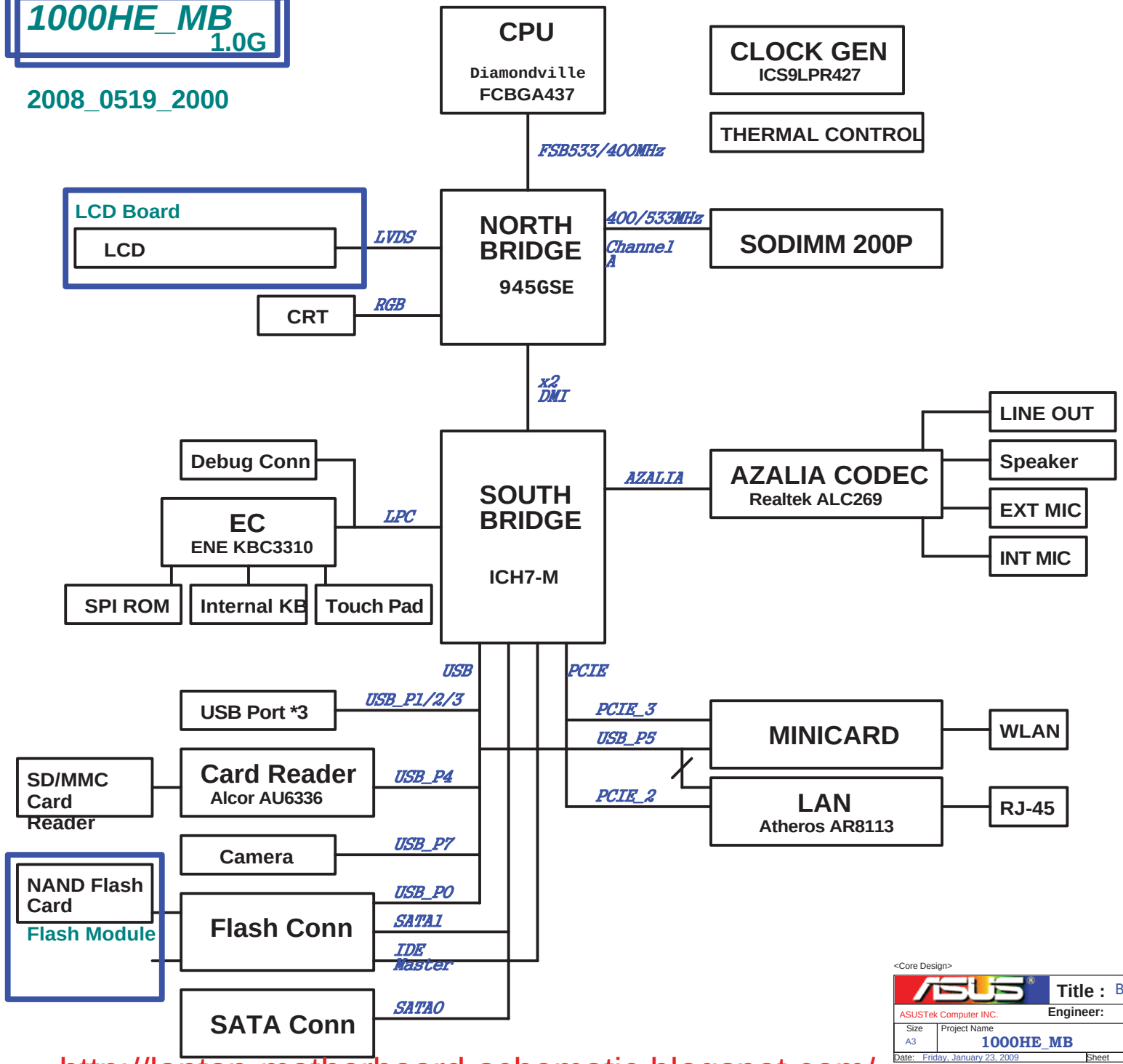
1000HE_MB 1.0G

2008_0519_2000

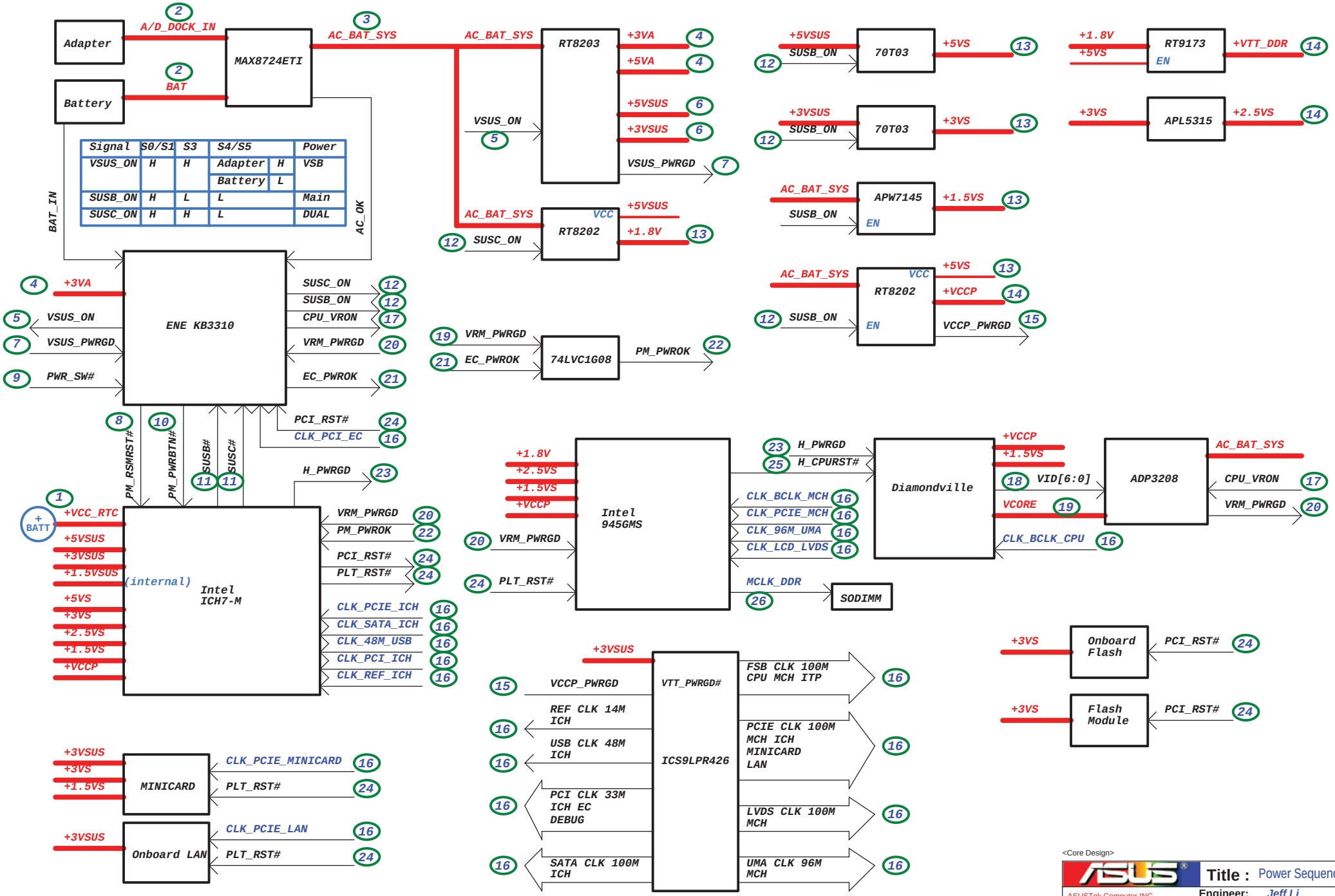


<Core Design>

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Echo_Huang	
Size: A3	Project Name: 1000HE_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 1 of 47	

<Core Design>

ASUSTek Computer INC.	Title : History	
	Engineer: KingCa_Jin	
Size: A3	Project Name: 1000HE_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 2 of 47	



<Core Design>

Title : Power Sequence

ASUSTek Computer INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 3 of 47

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SCI#	EXT_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configureation
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSAVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Core Design>

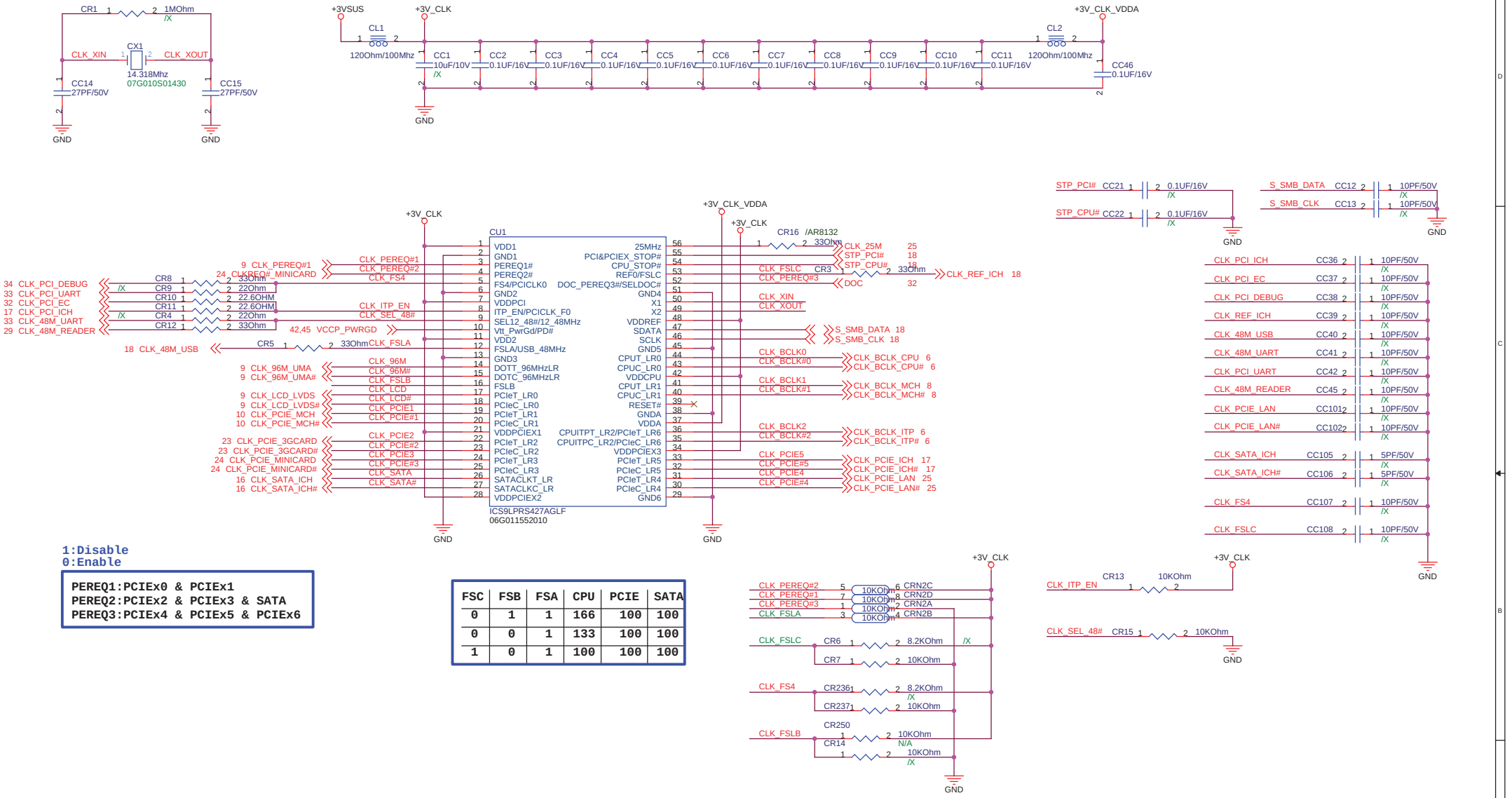
ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 4 of 47



1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	1	1	166	100	100
0	0	1	133	100	100
1	0	1	100	100	100

<Core Design>

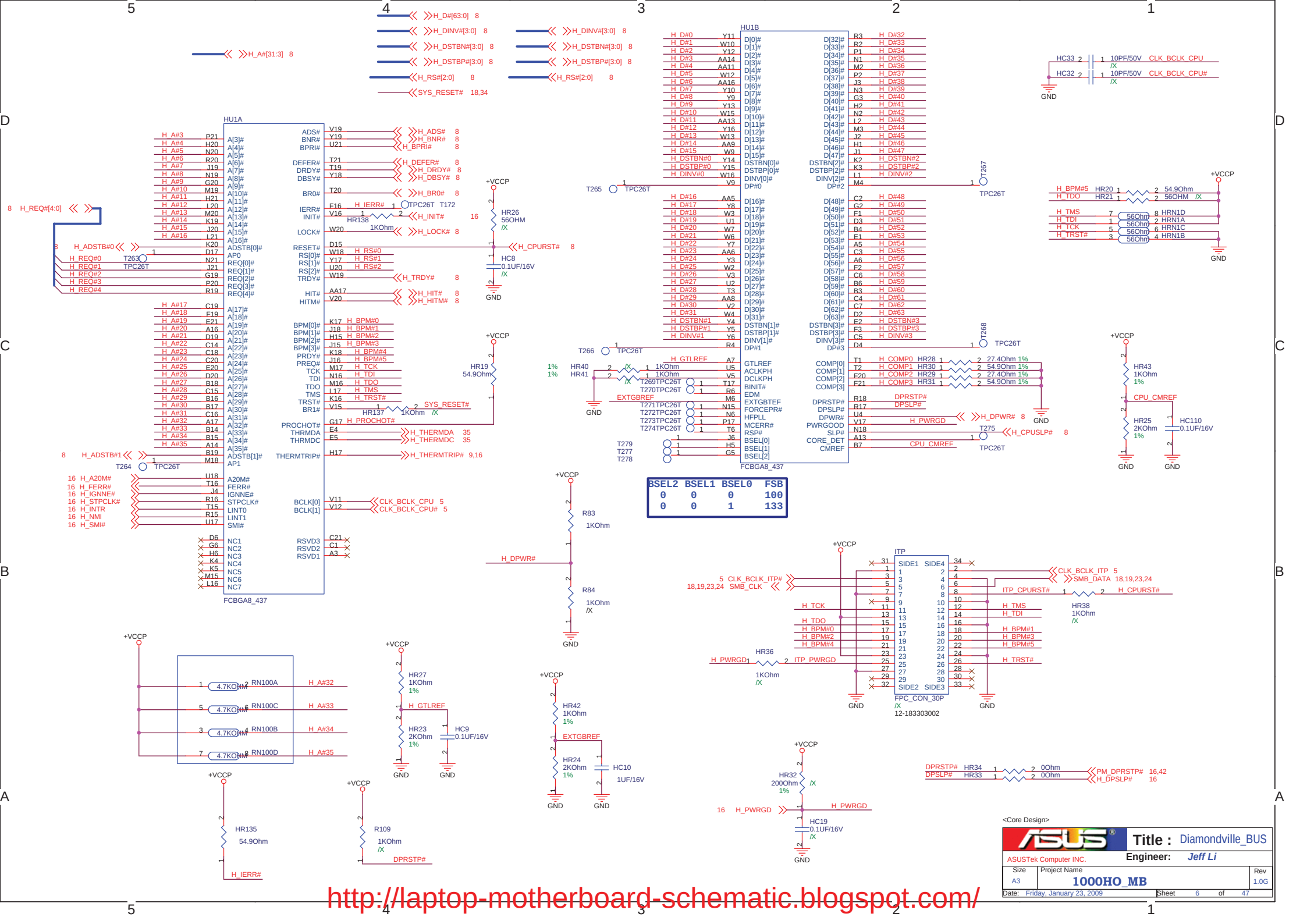
ASUSTek Computer INC.

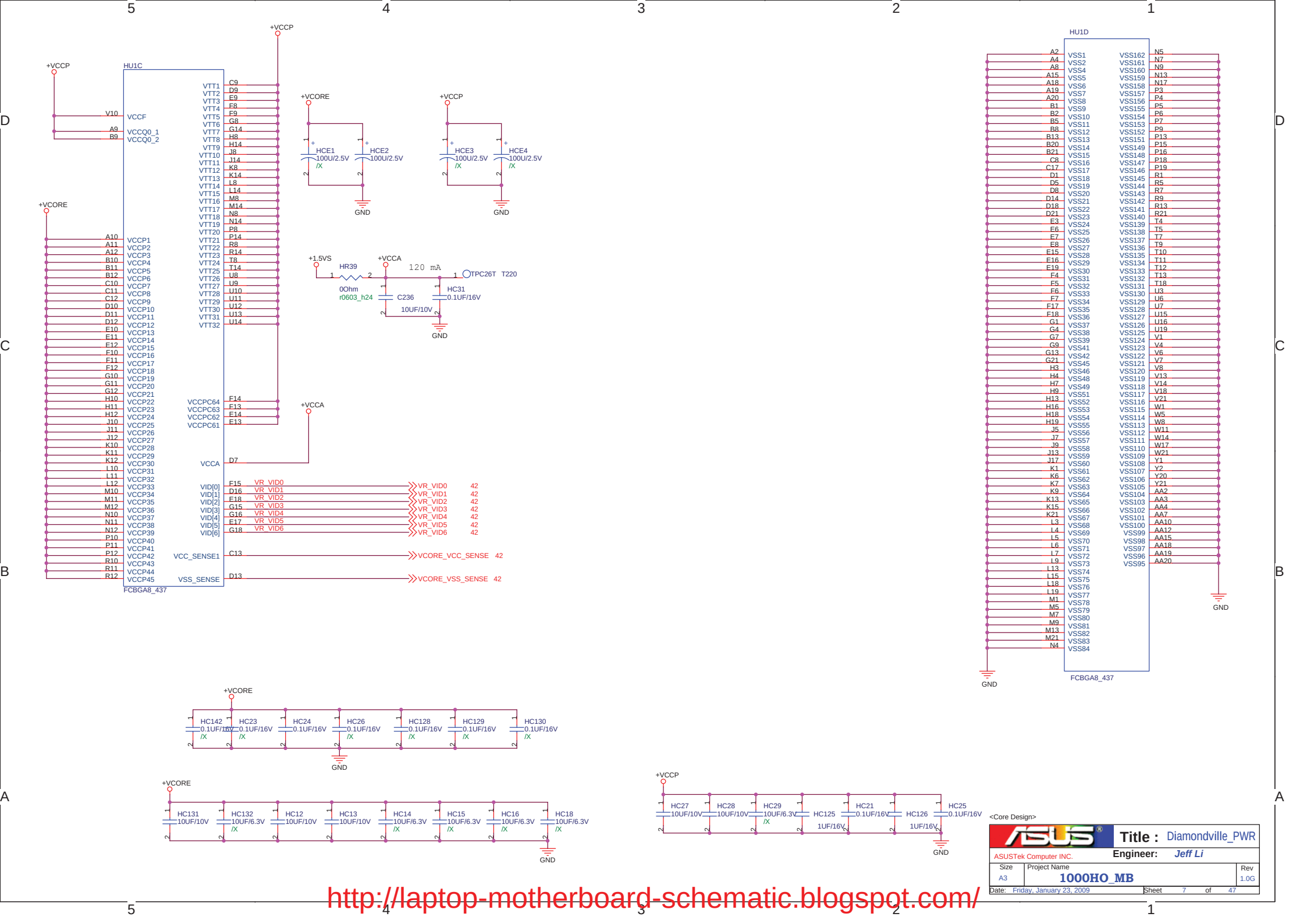
Title : Clock Gen_ICS9LPRS427

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 5 of 47





<Core Design>

ASUSTek Computer INC.

Title : Diamondville_PWR

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 7 of 47

Power : +VCCP

RCOMP

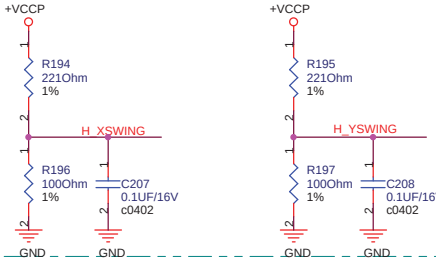
For Calibrating the FSB I/O Buffer

SCOMP

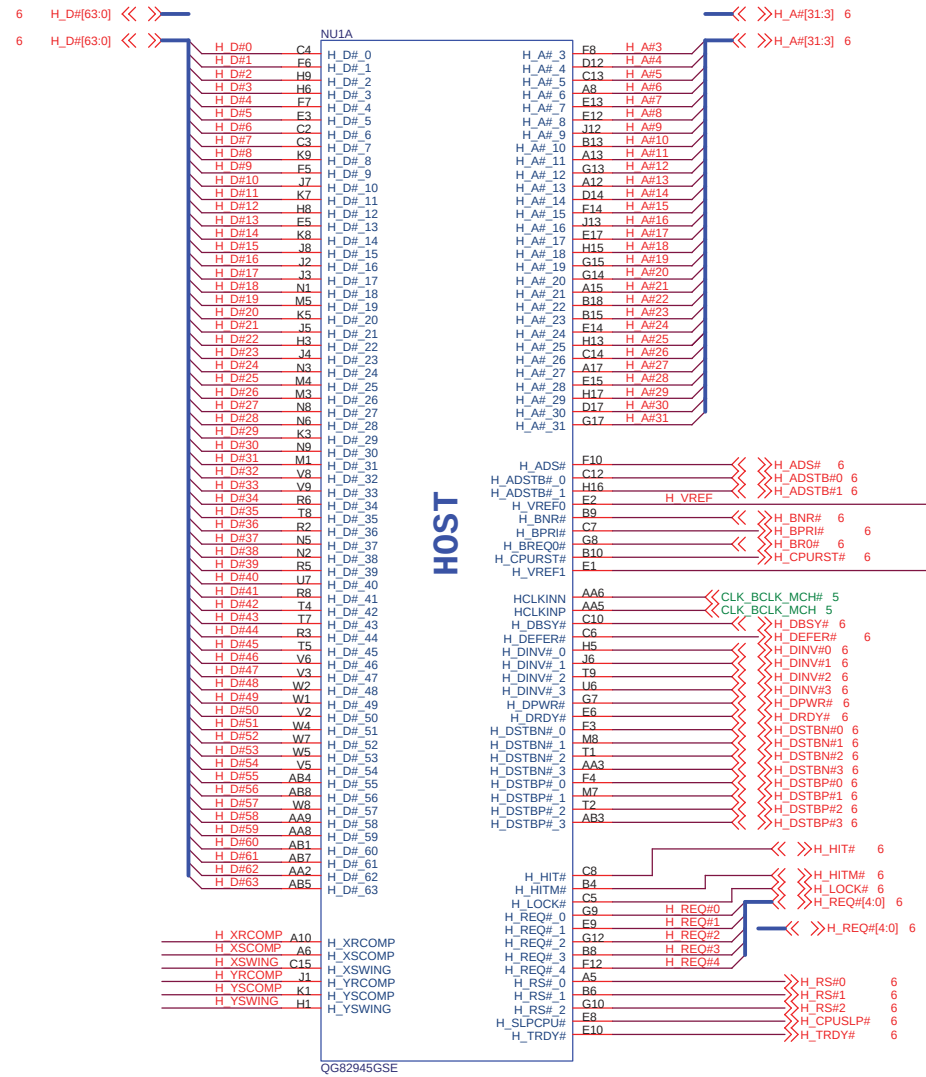
For Slew Rate Compenssation on the FSB

Voltage Swing

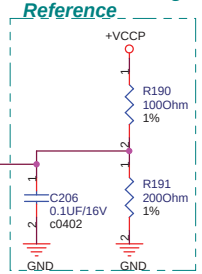
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing



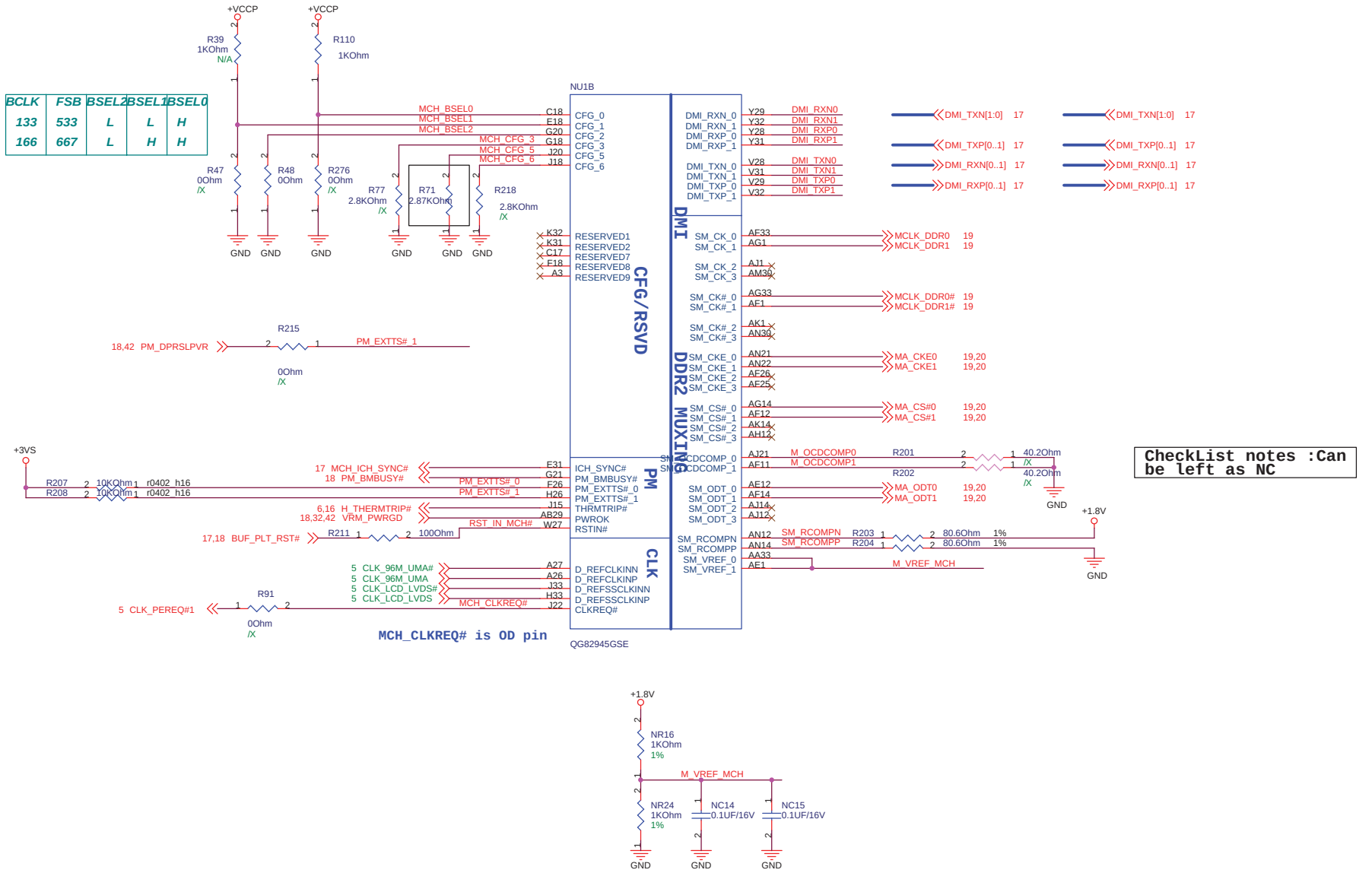
AGTL+ I/O Voltage Reference

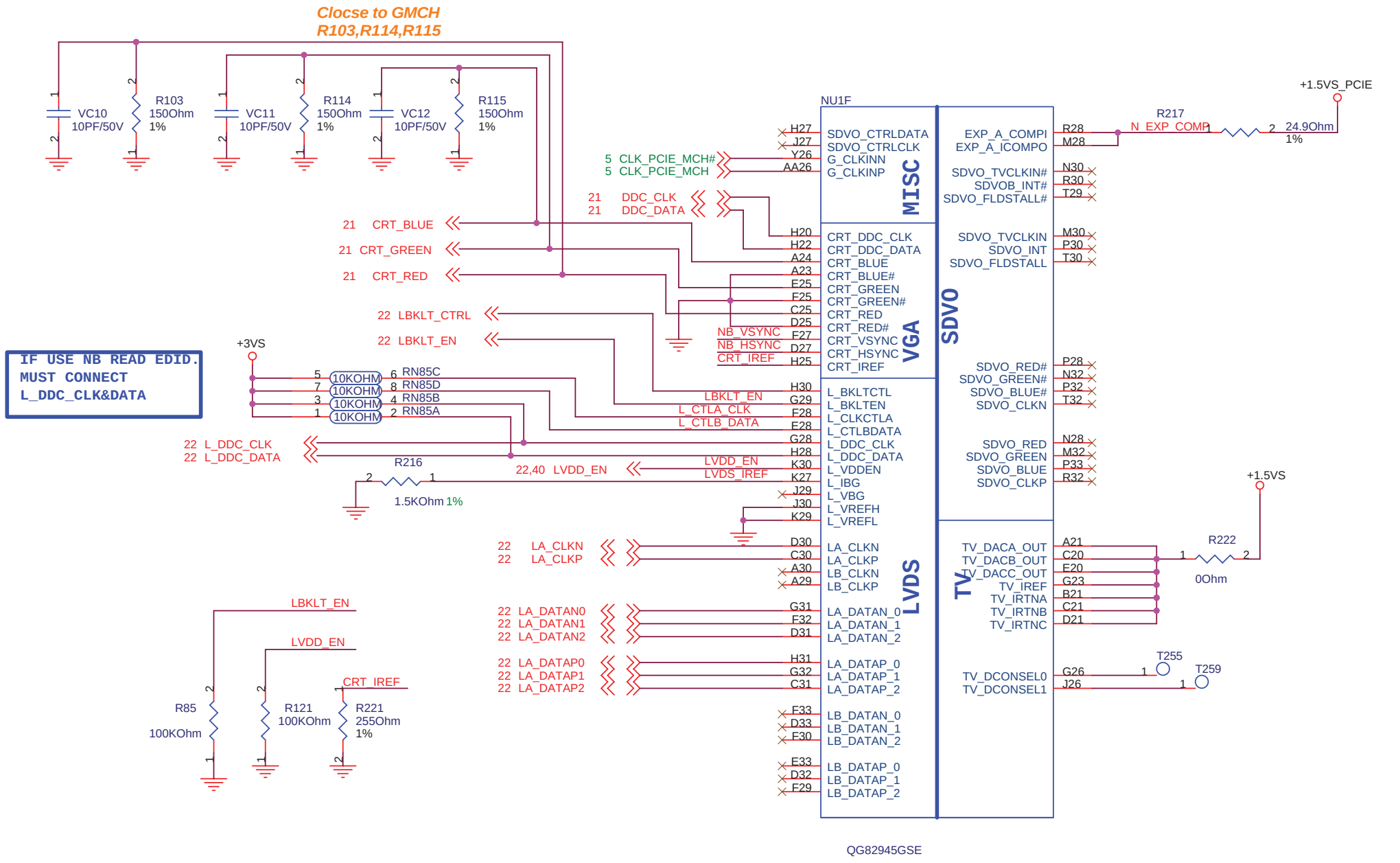


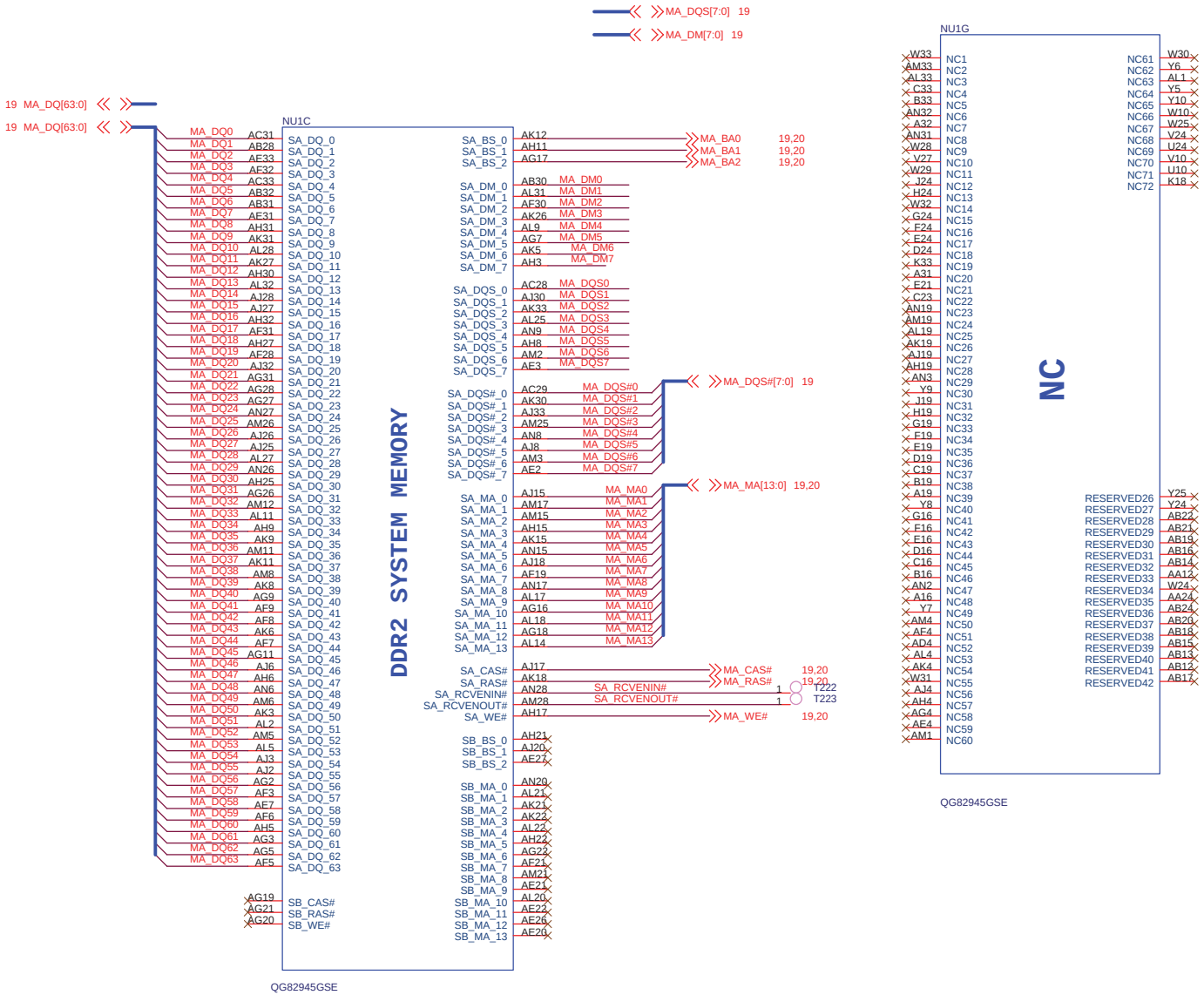
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(HOST)	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 8 of 47	







<Core Design>

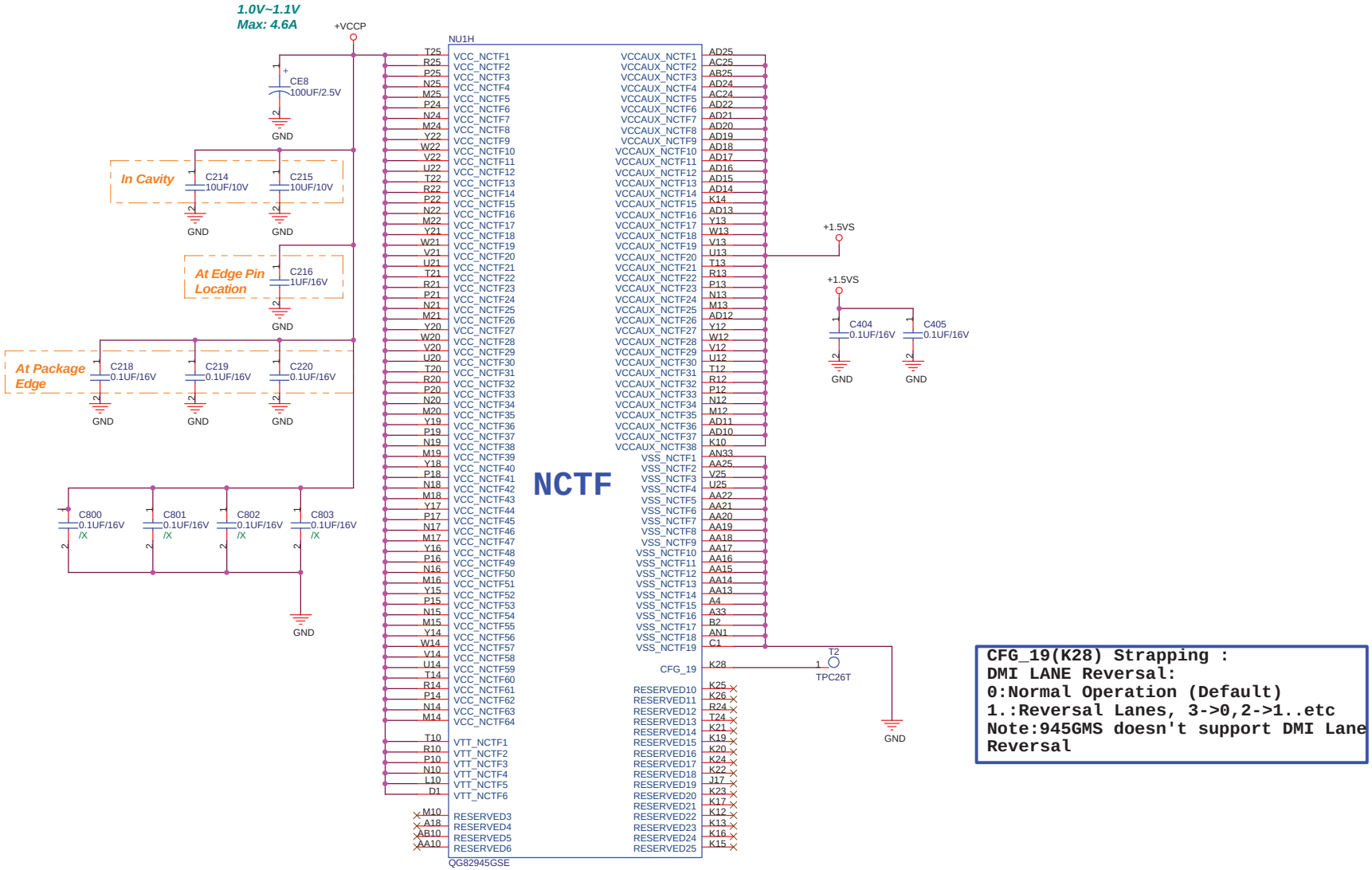
ASUSTeK COMPUTER INC.

Title : NB-945GMS(DDR2)

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 11 of 47



<Core Design>

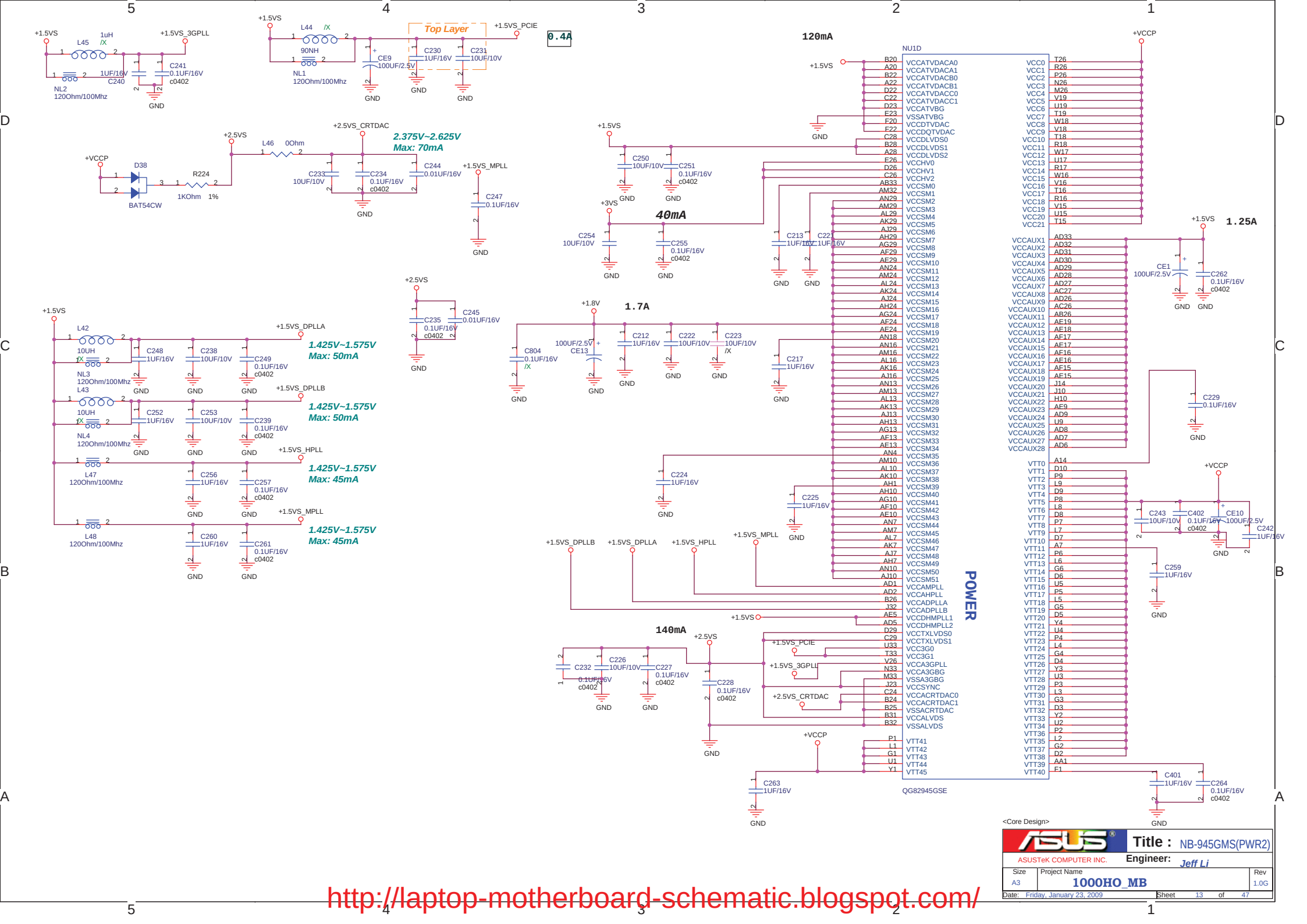
ASUSTeK COMPUTER INC.

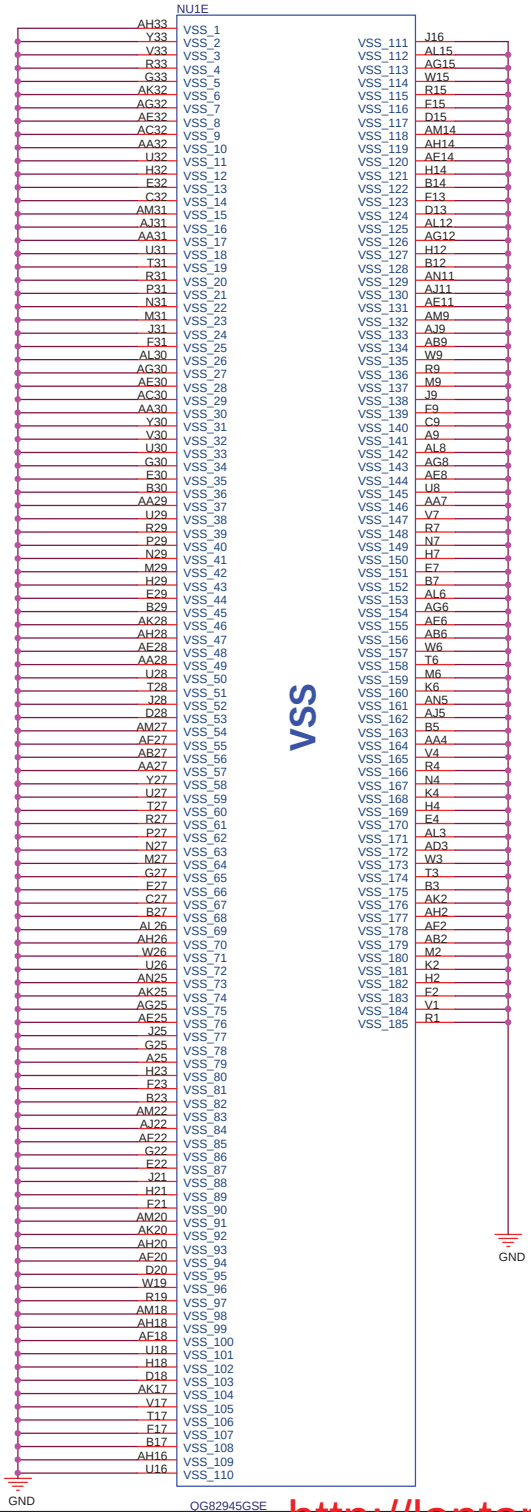
Title : NB-945GMs(PWR)

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 12 of 47





<Core Design>

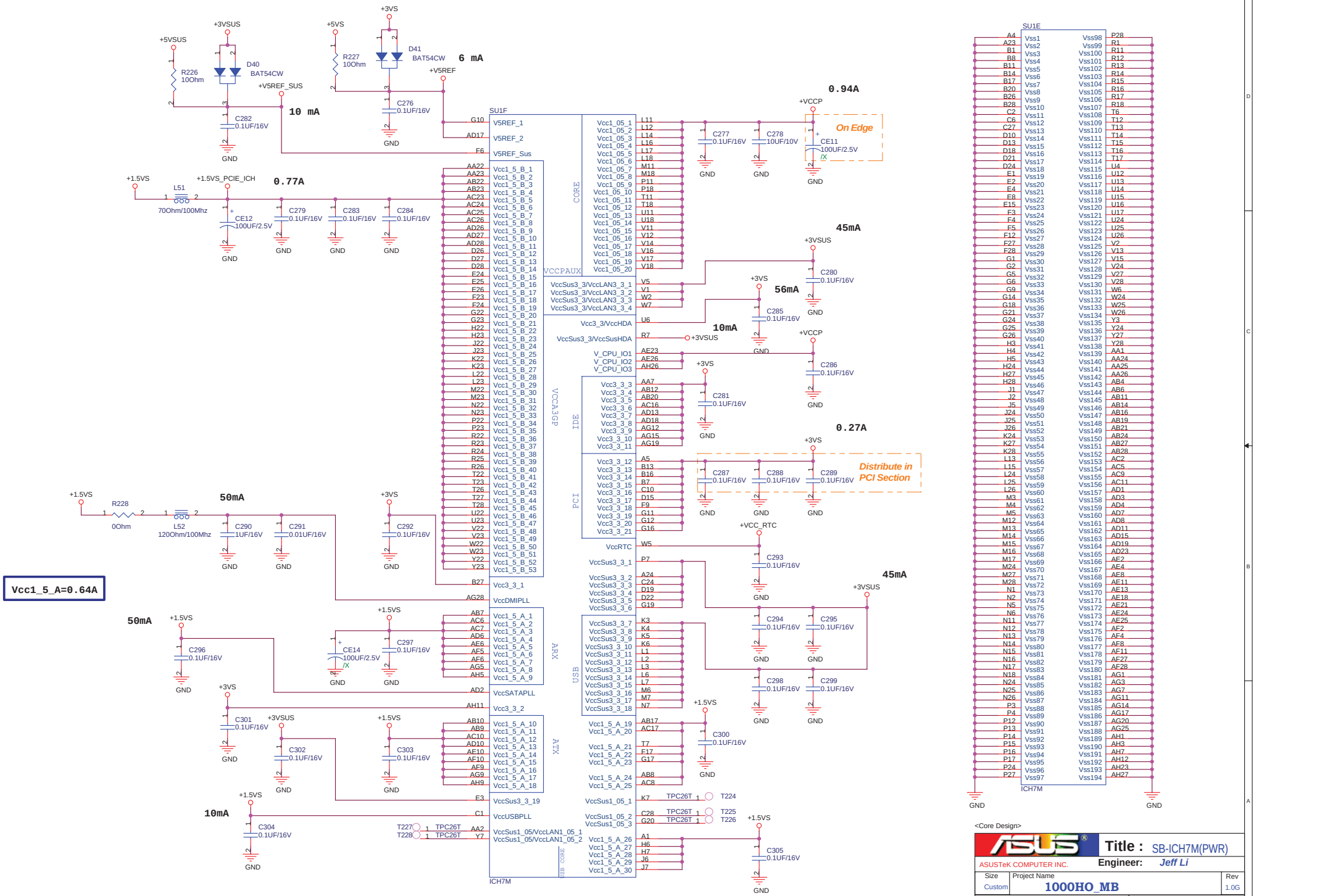
ASUSTeK COMPUTER INC.

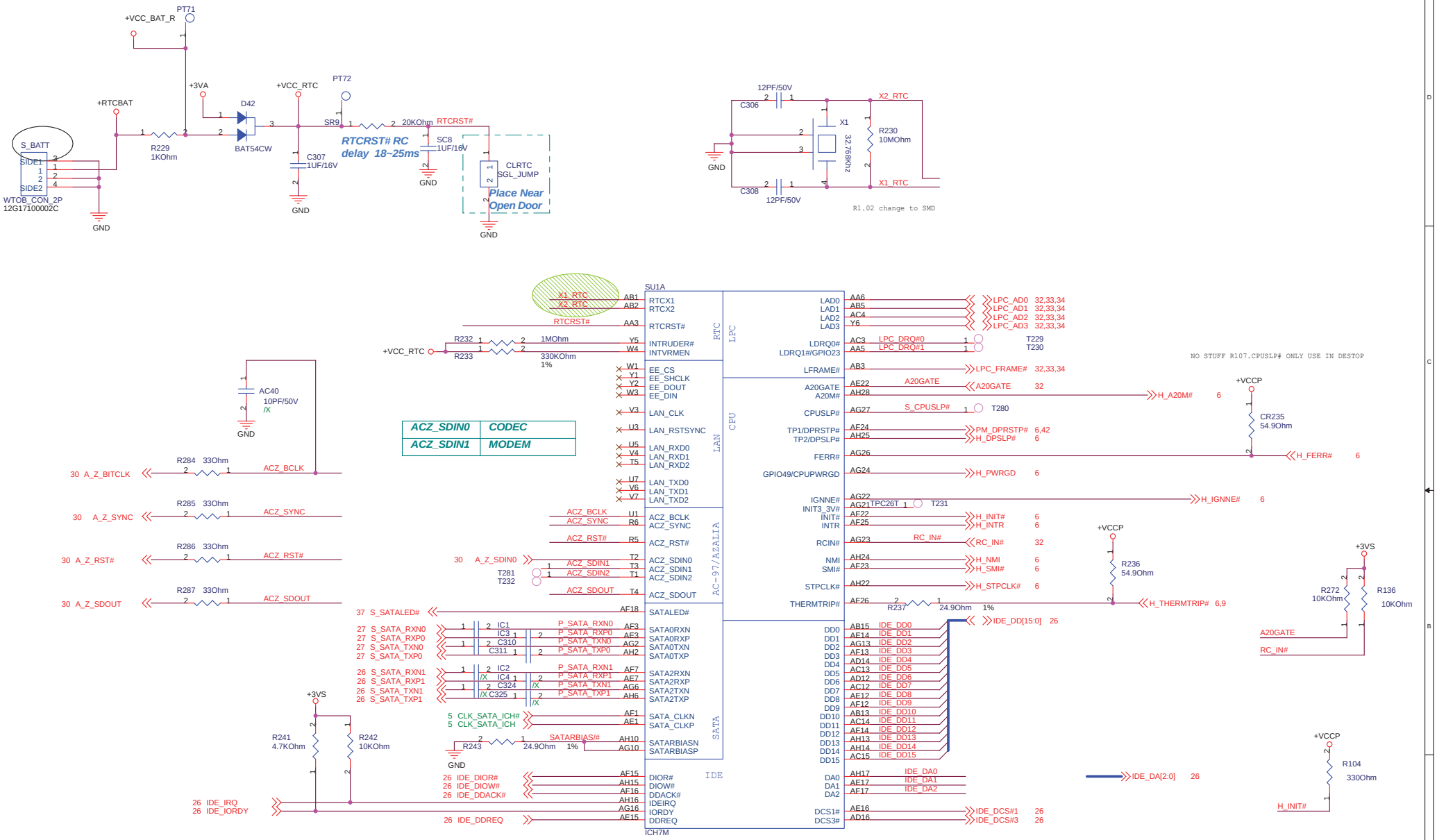
Title : NB-945PMS(GND)

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 14 of 47





<Core Design>

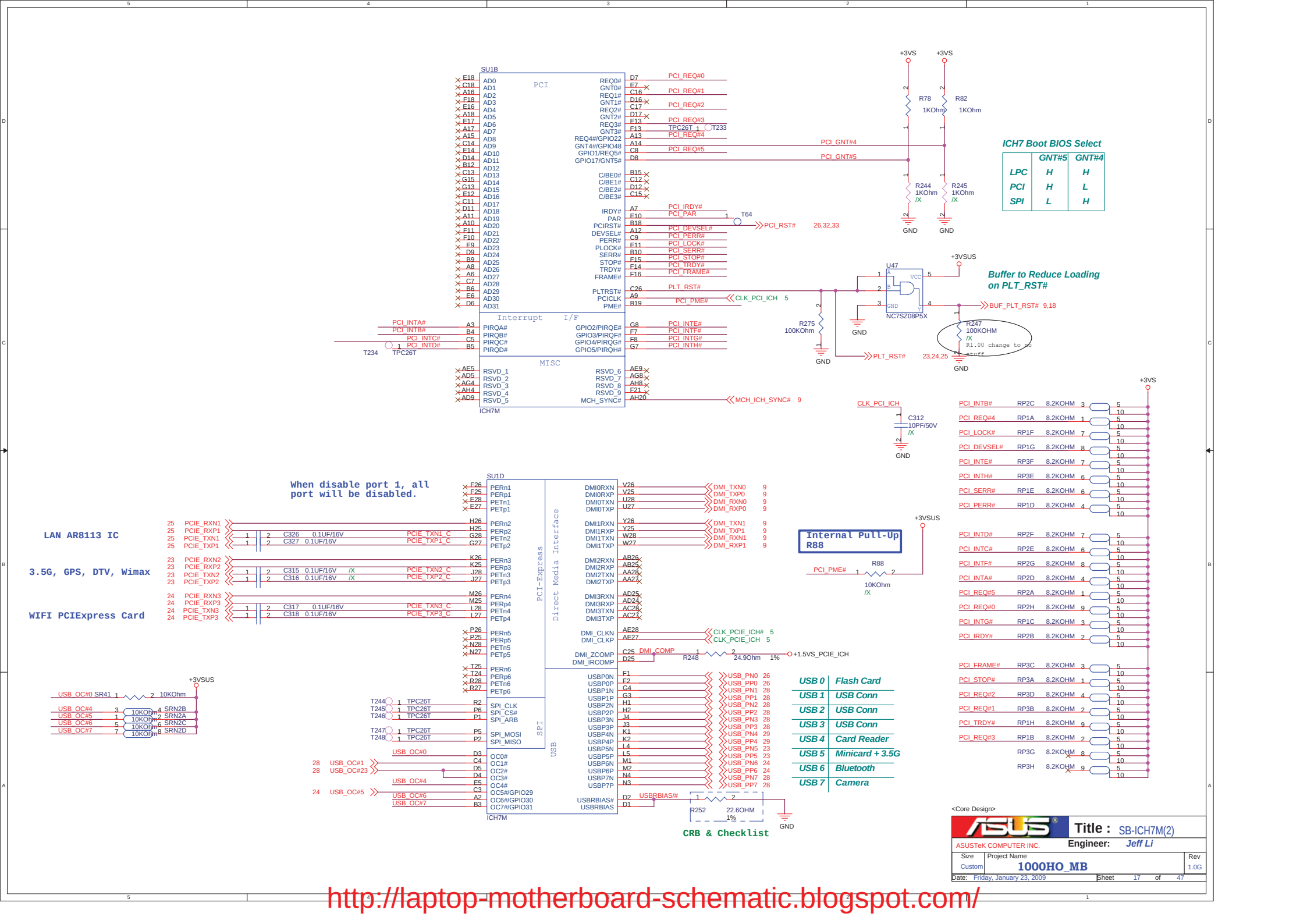
ASUSTeK COMPUTER INC.

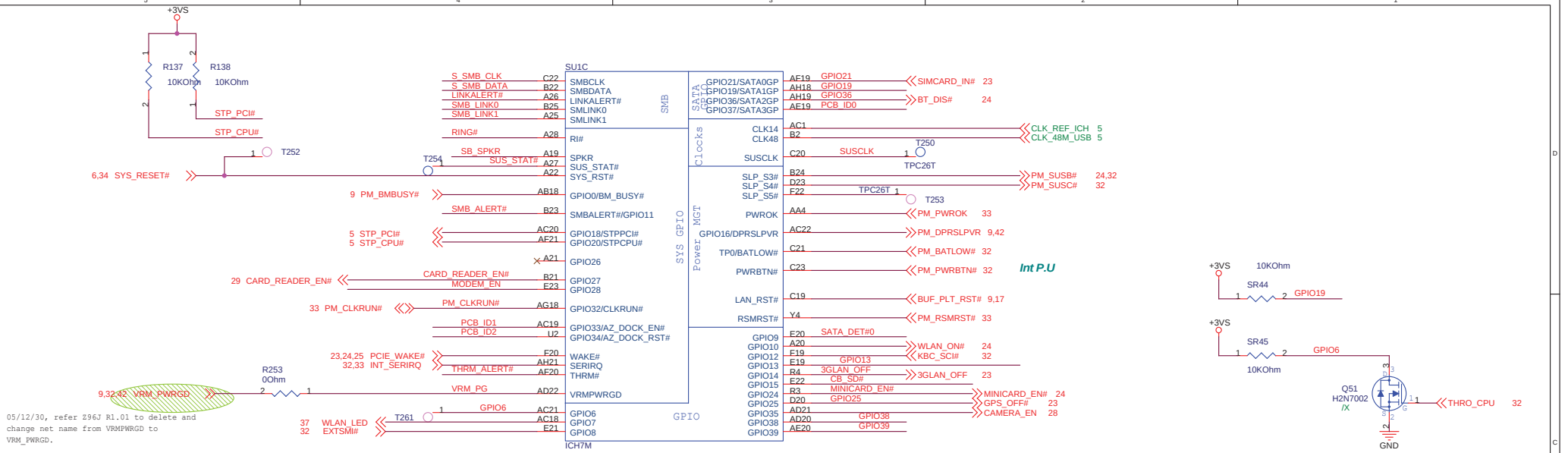
Title : SB-ICH7-M(1)

Engineer: Jeff Li

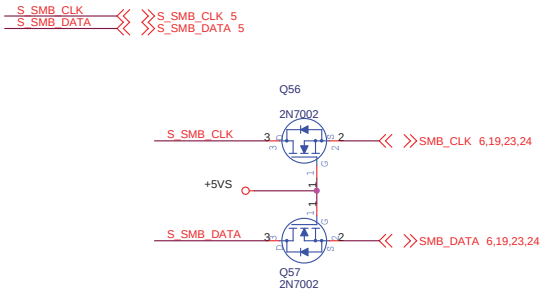
Size	Project Name	Rev
Custom	1000HO_MB	1.0G

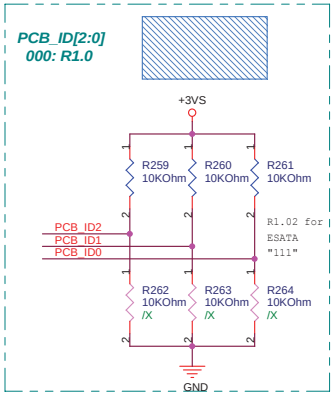
Date: Friday, January 23, 2009 Sheet 16 of 47





WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x





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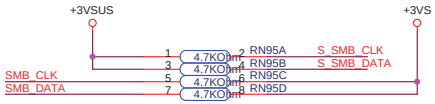
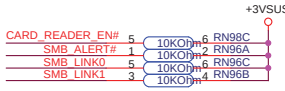
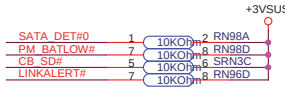
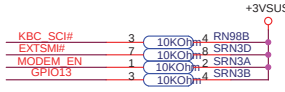
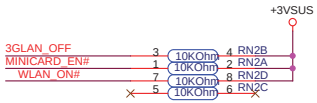
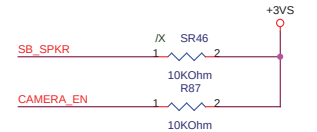


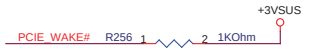


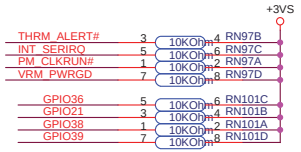












<Core Design>

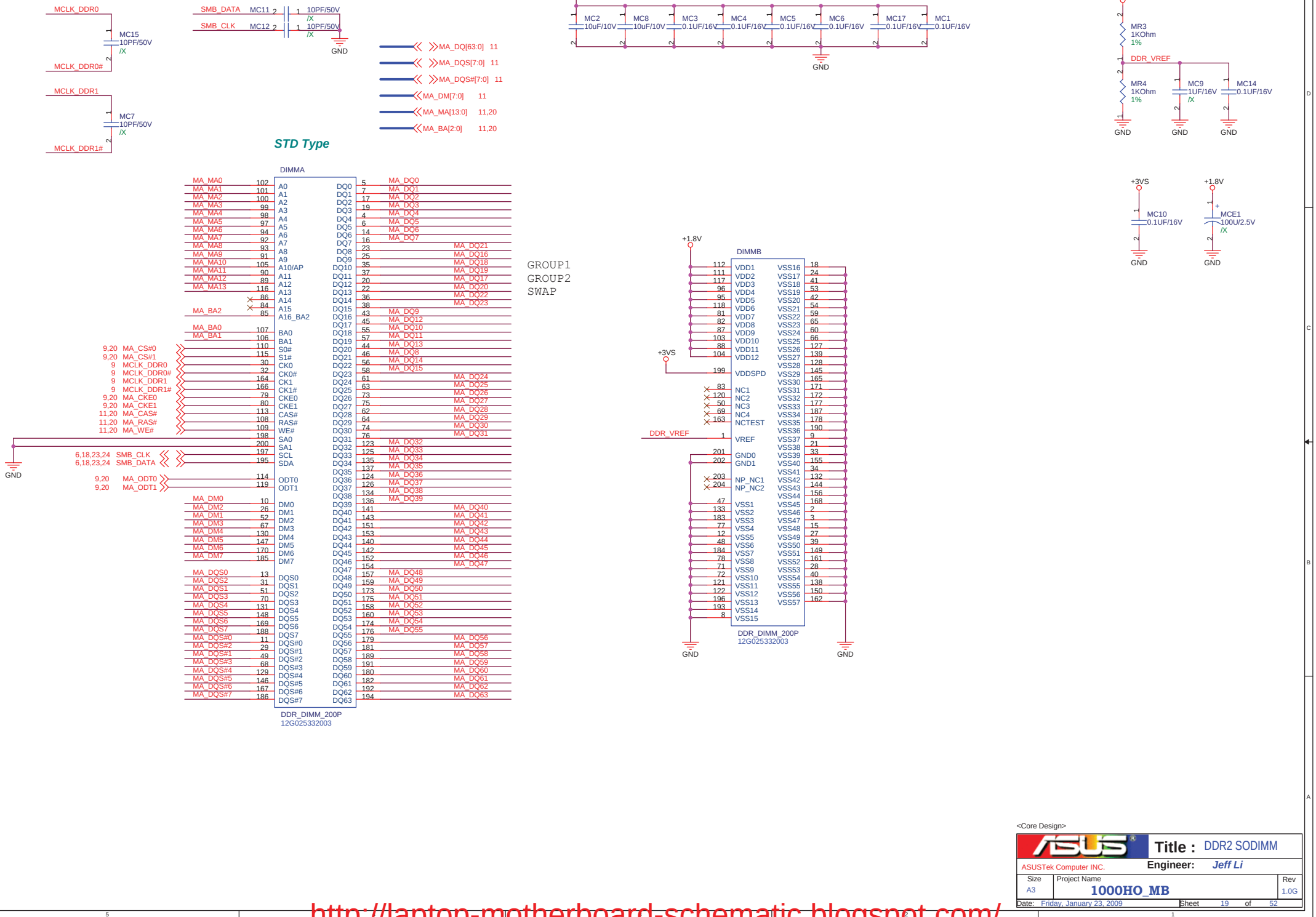
ASUSTeK COMPUTER INC

Title : SB-ICH7M(3)

Engineer: Jeff Li

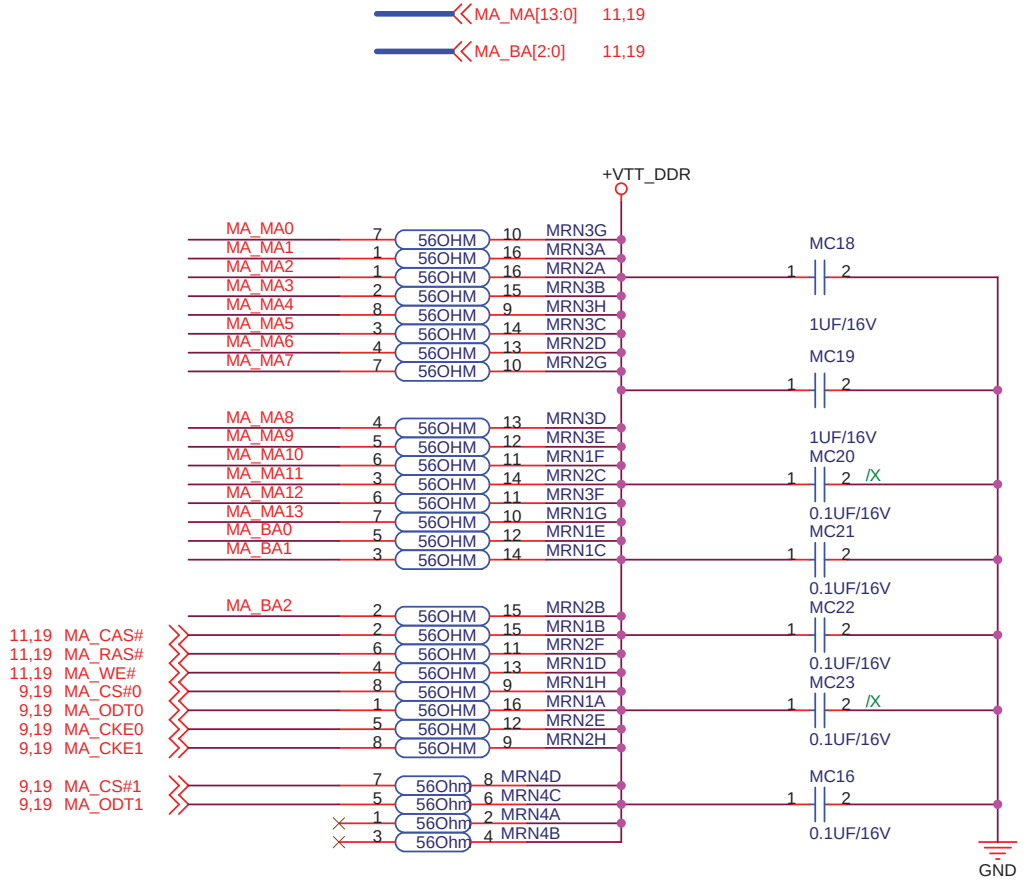
Size	Project Name	Rev
Custom	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 18 of 47



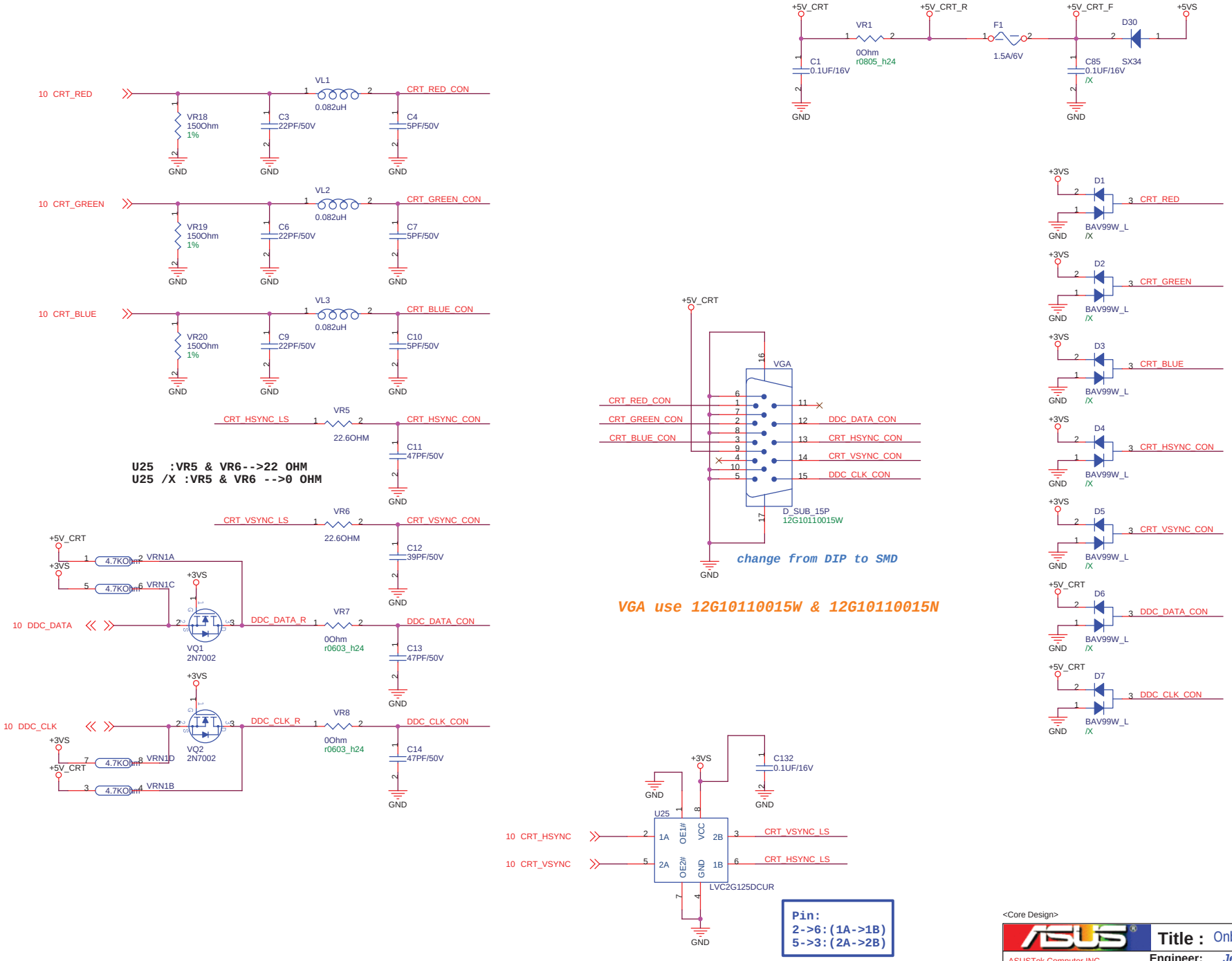
<Core Design>

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 19 of 52	



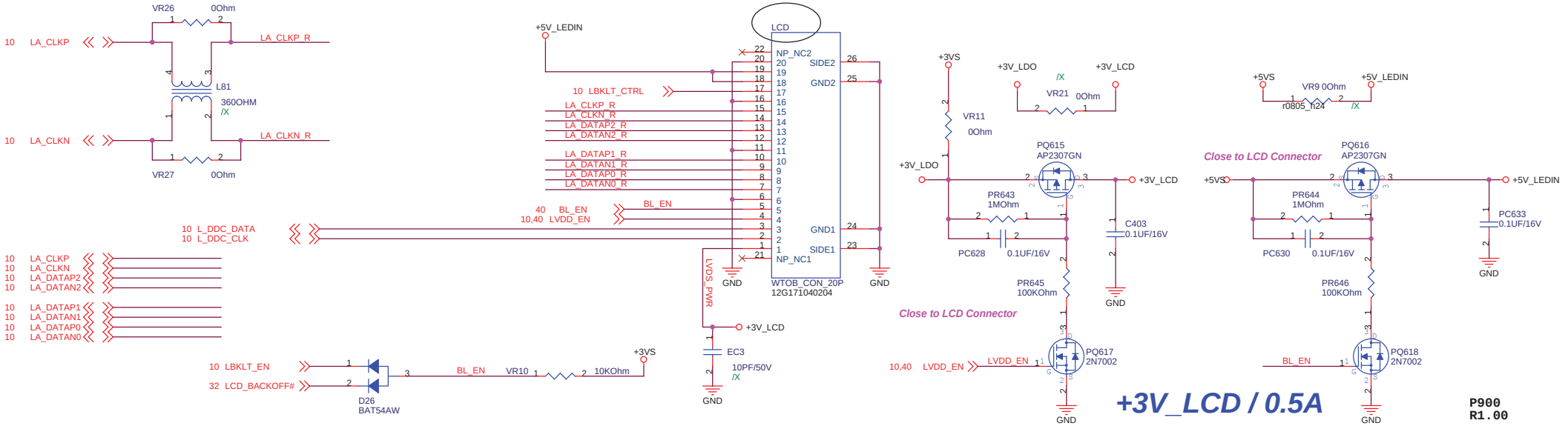
<Core Design>

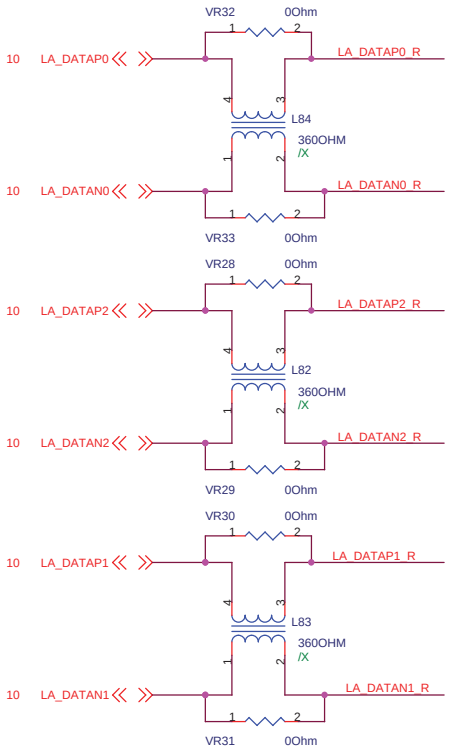
ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: Jeff Li	
Size: A4	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 20 of 52	

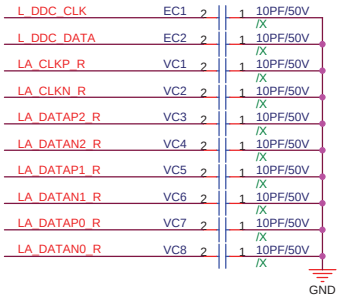


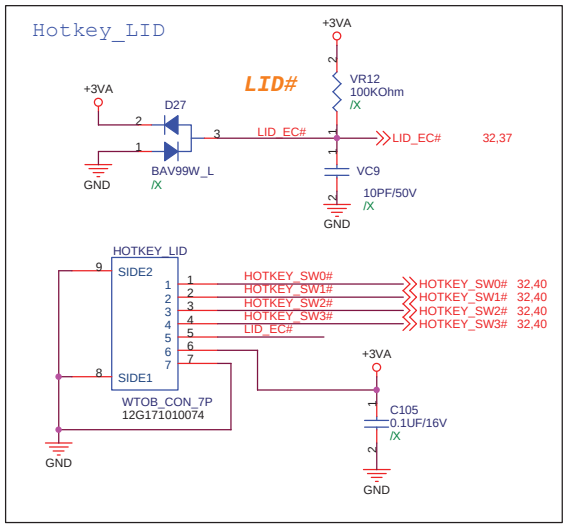
<Core Design>

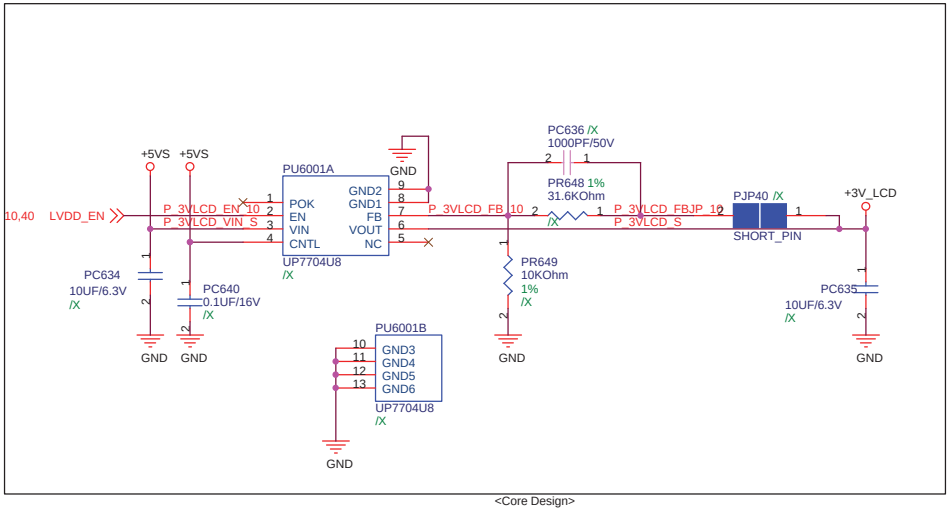
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 21 of 52	





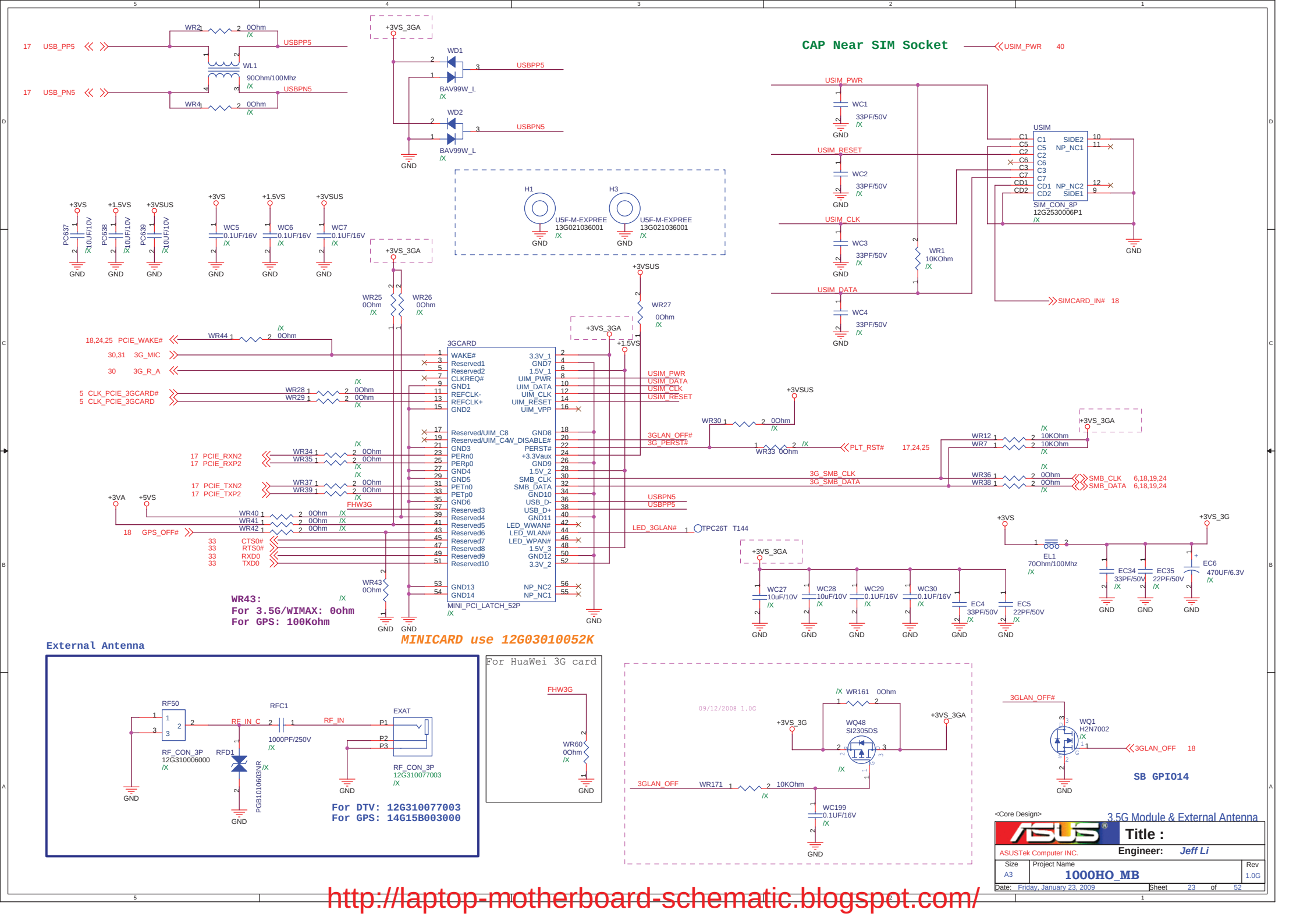


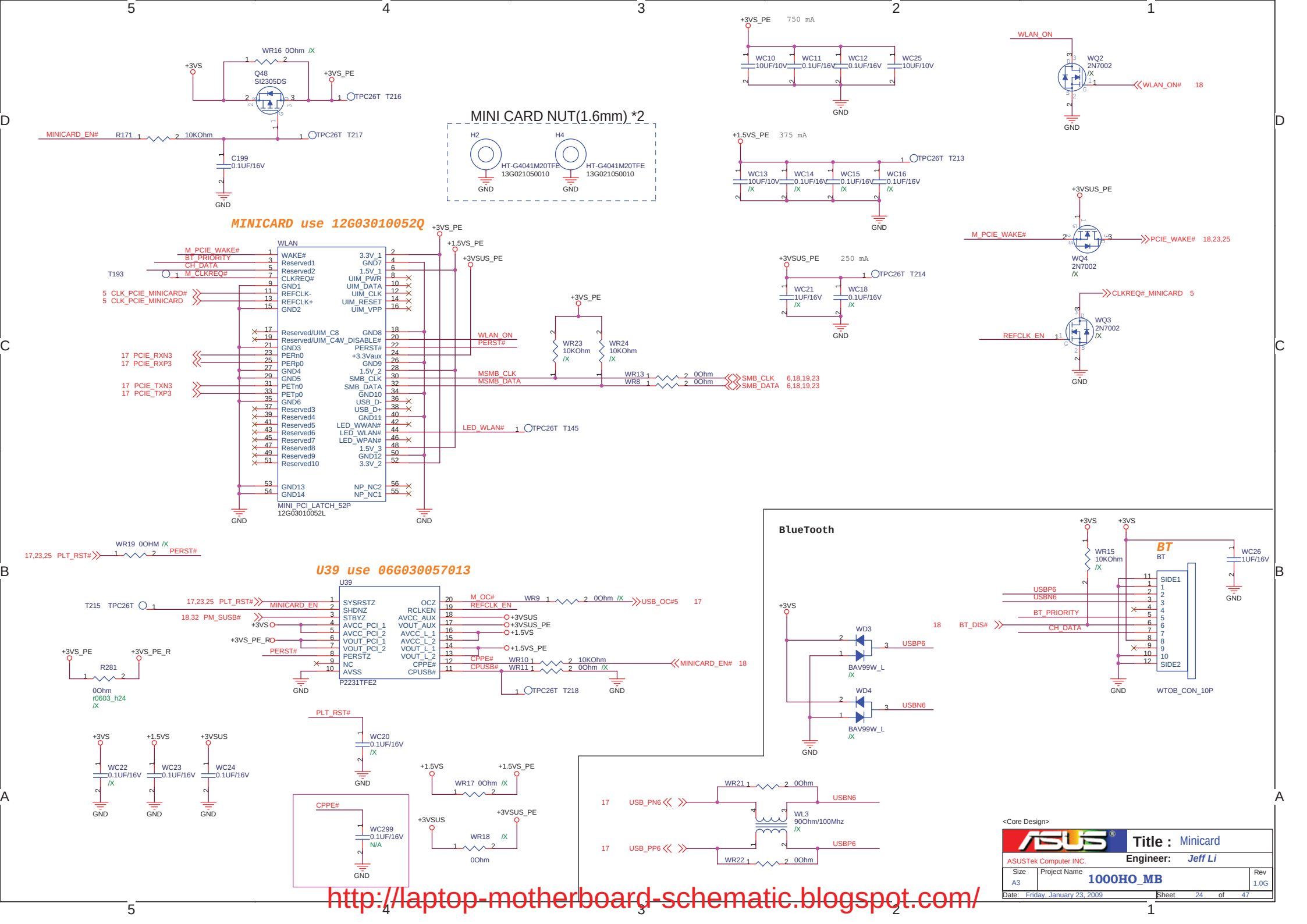


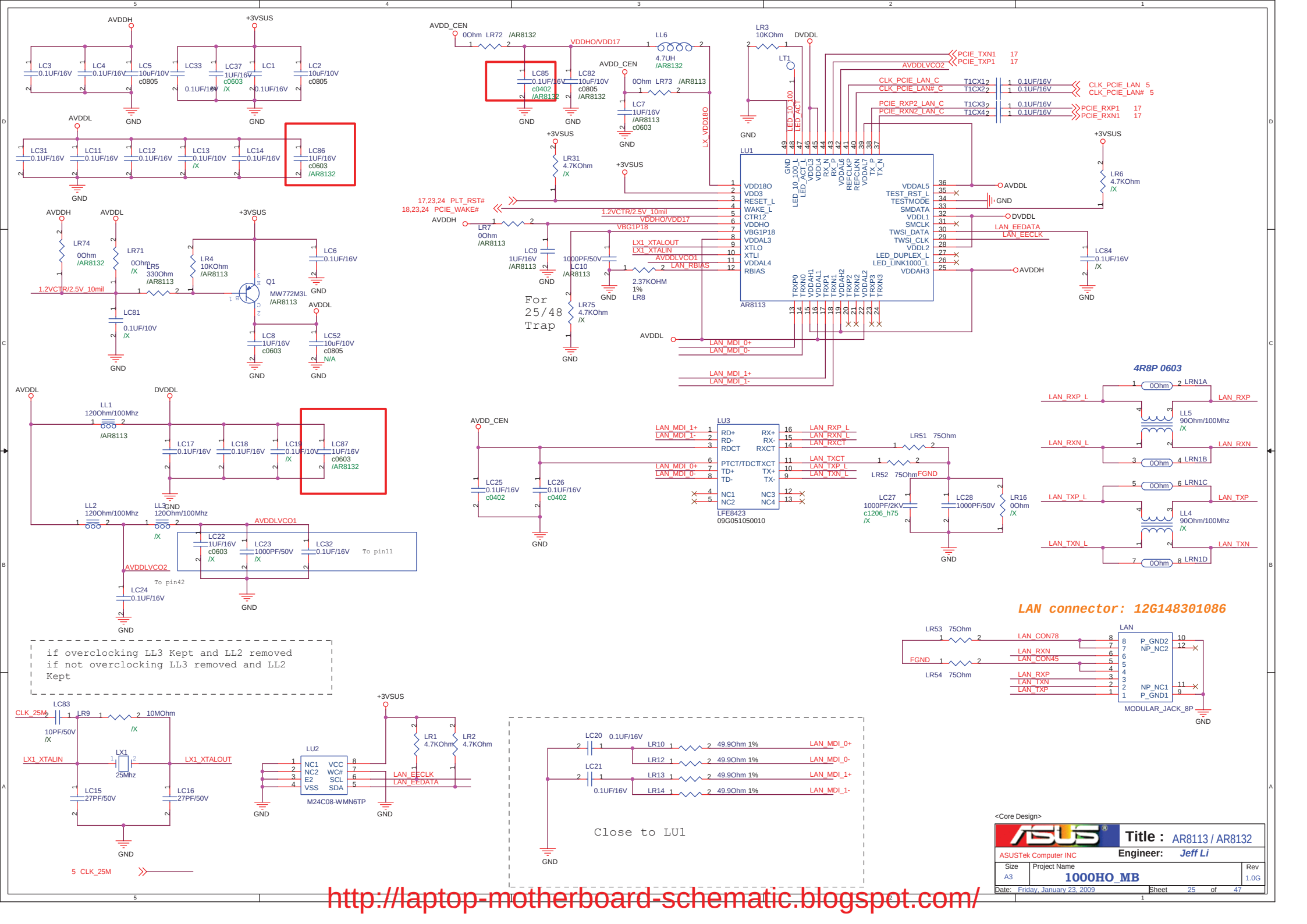


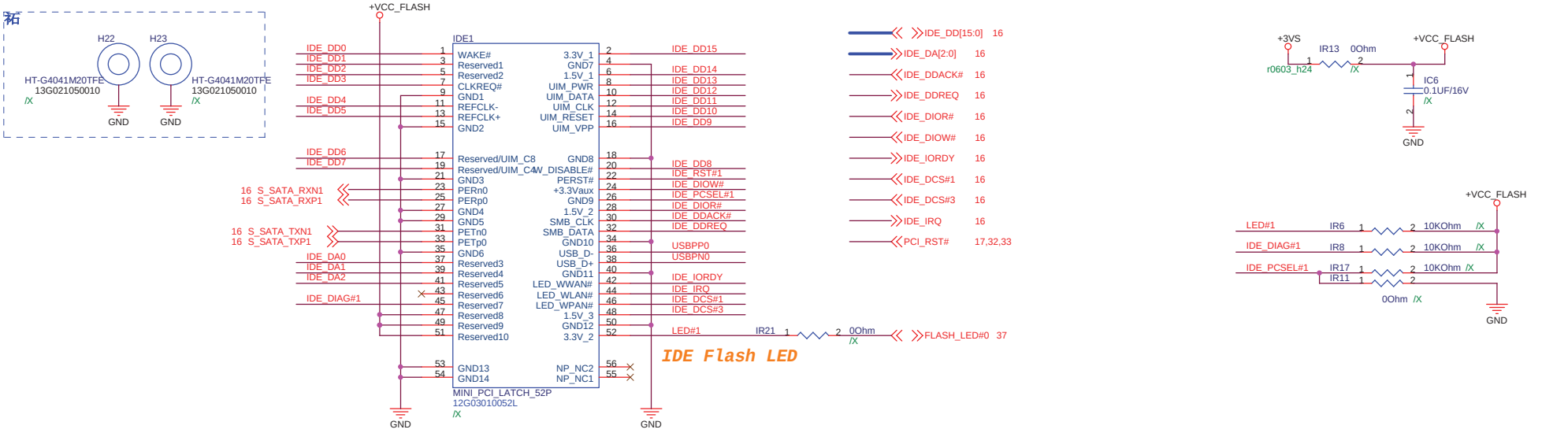
<Core Design>

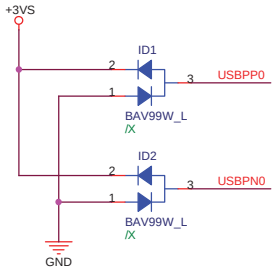
ASUSTek Computer INC.	Title : LVDS Conn_LID	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 22 of 52	

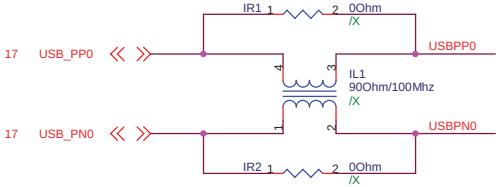


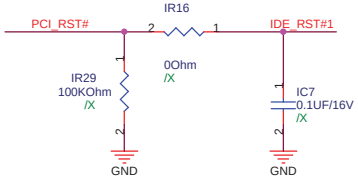

MINI CARD NUT(1.6mm) *2
MINICARD use 12G03010052Q
U39 use 06G030057013
BlueTooth
WLAN
MINI_PCI_LATCH_52P
12G03010052L
P2231TFE2
WTOB_CON_10P
<Core Design>
Title : Minicard
ASUSTek Computer INC.
Engineer: Jeff Li
1000HO_MB
Date: Friday, January 23, 2009
Sheet 24 of 47
http://laptop-motherboard-schematic.blogspot.com/









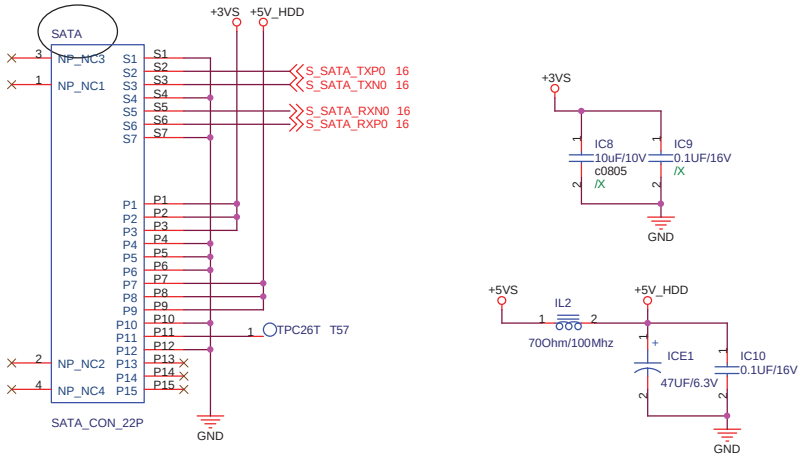


Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?

<Core Design>

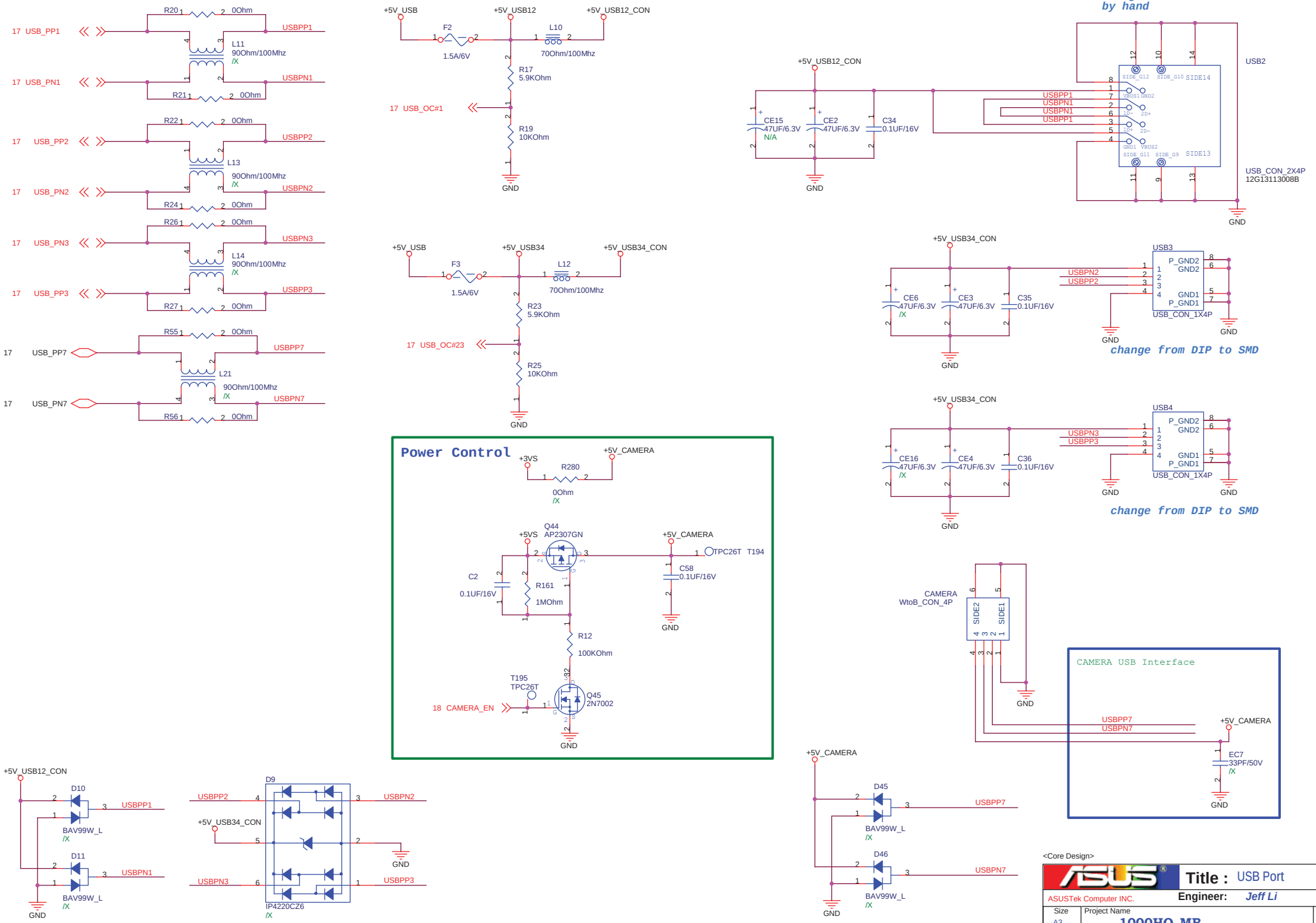
ASUSTek Computer INC.	Title : HD + Flash Conn	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 26 of 47	

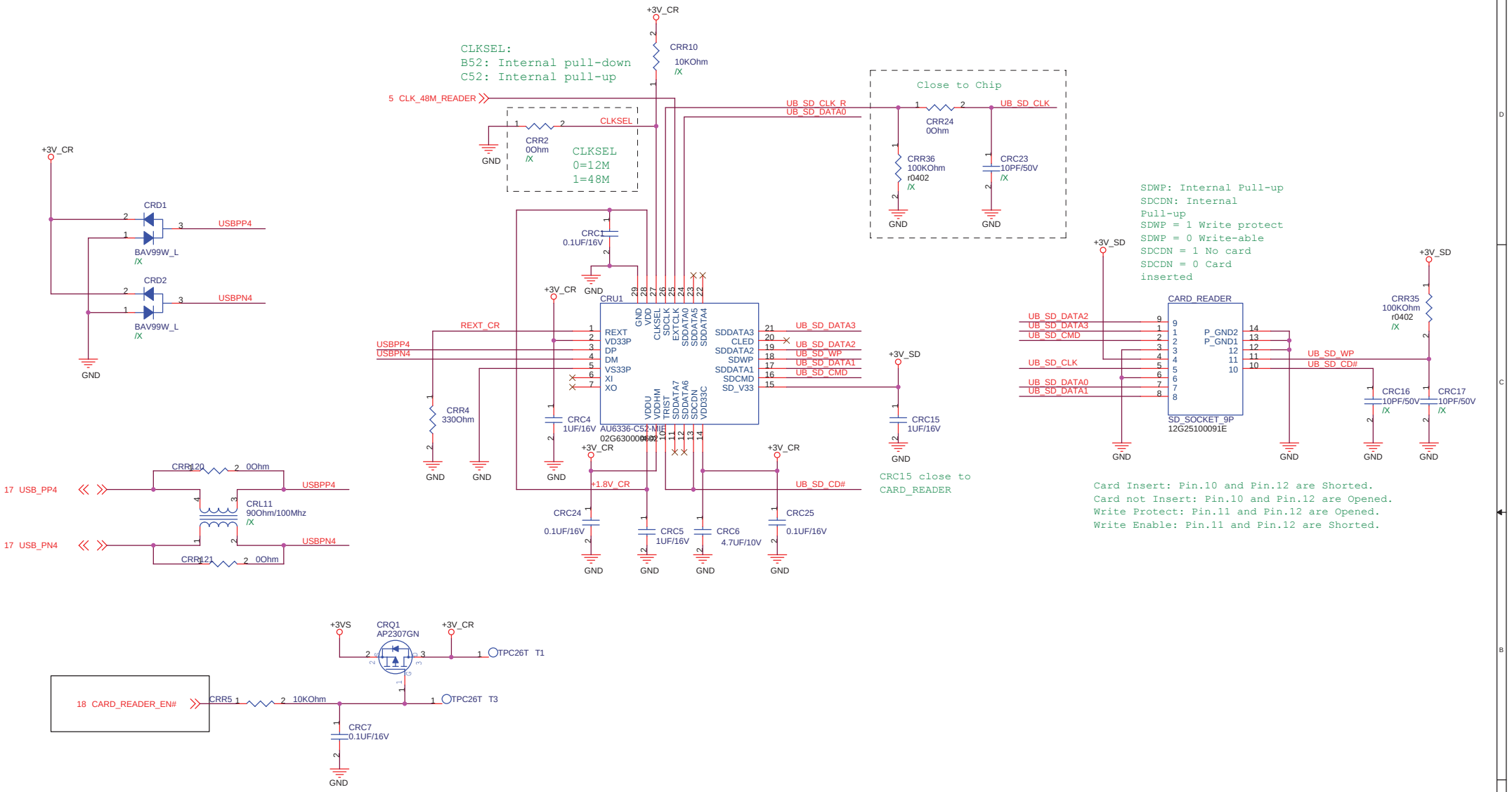
SATA HDD Connector



<Core Design>

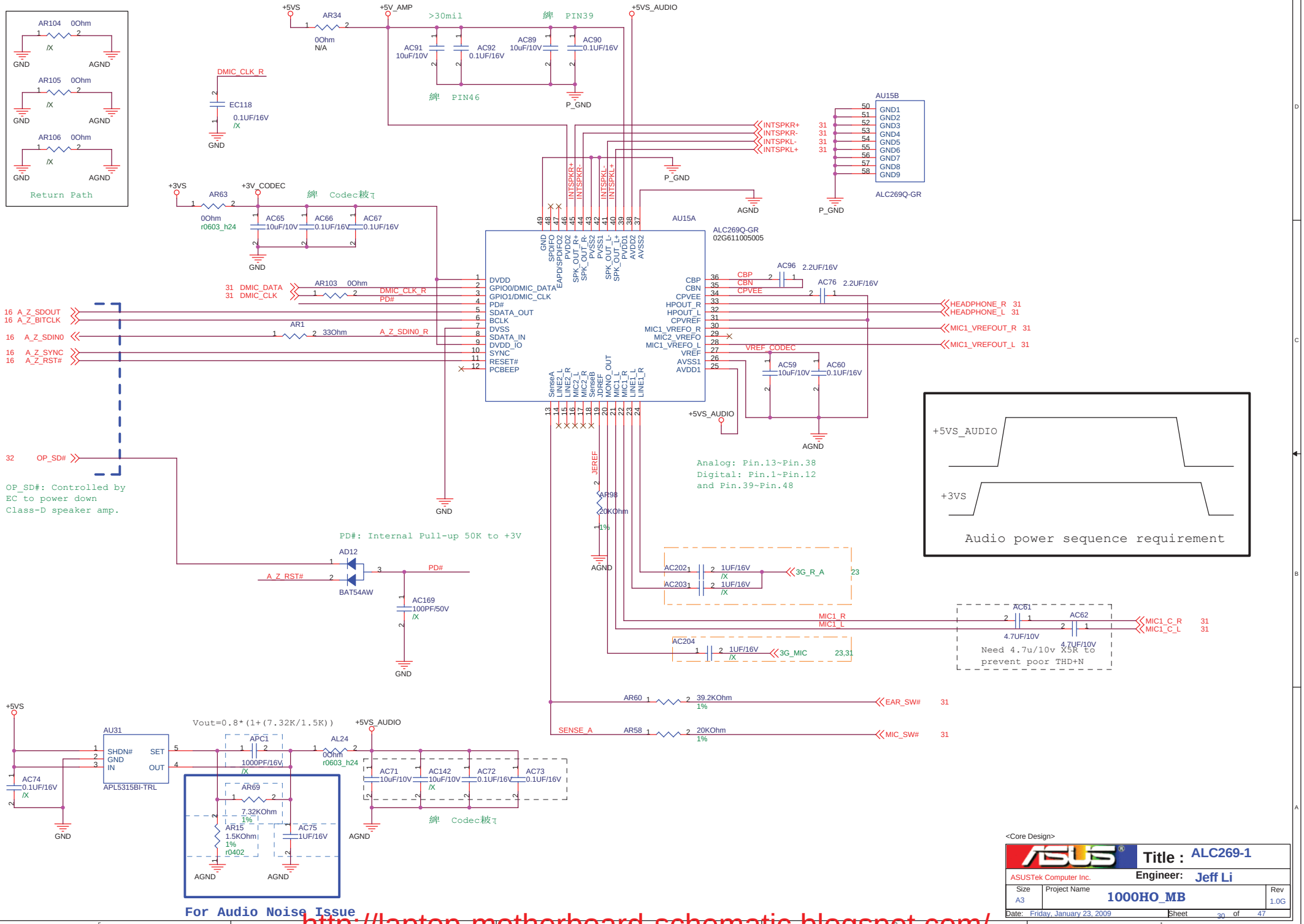
ASUSTek Computer INC.	Title : HDD	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 27 of 47	

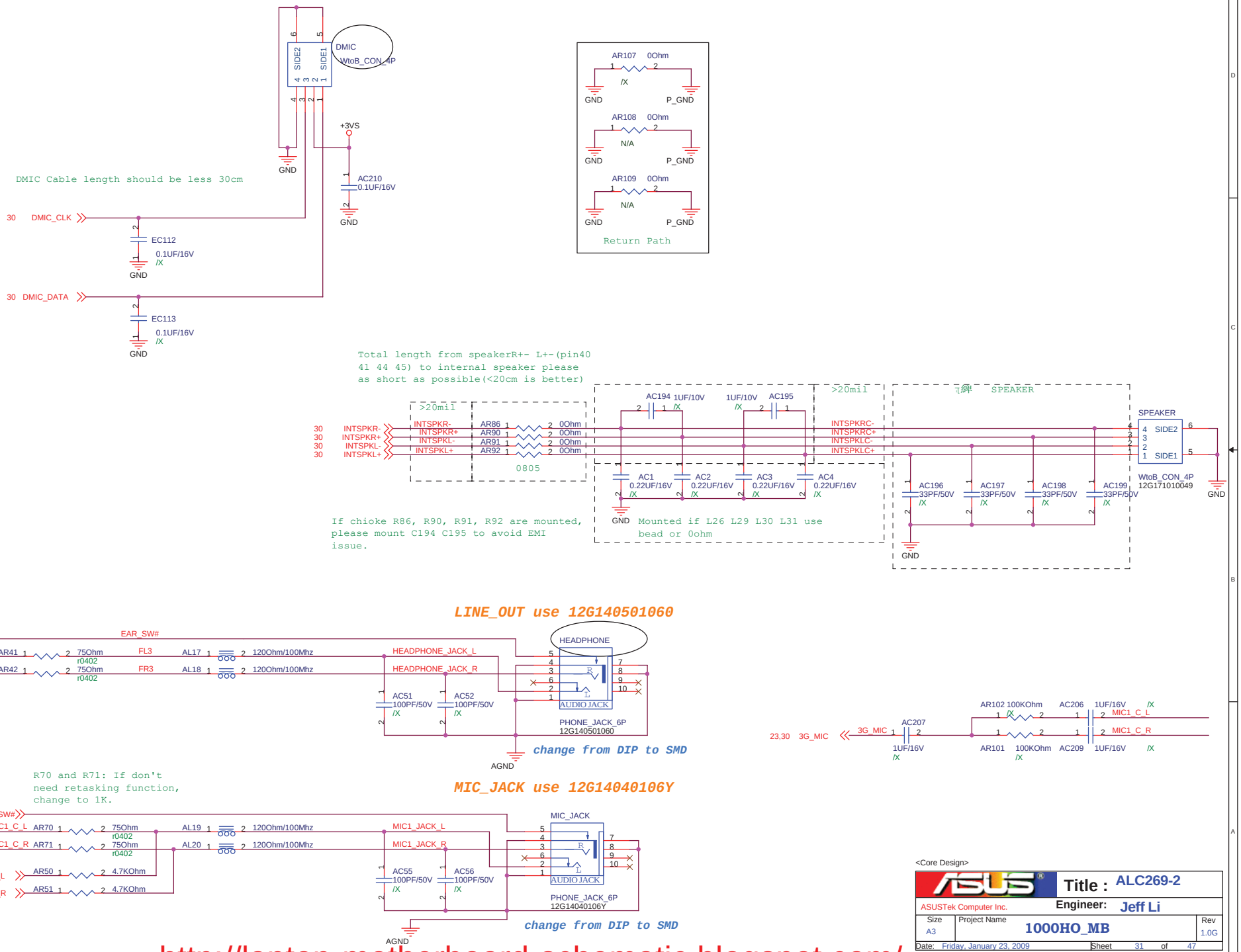




<Core Design>

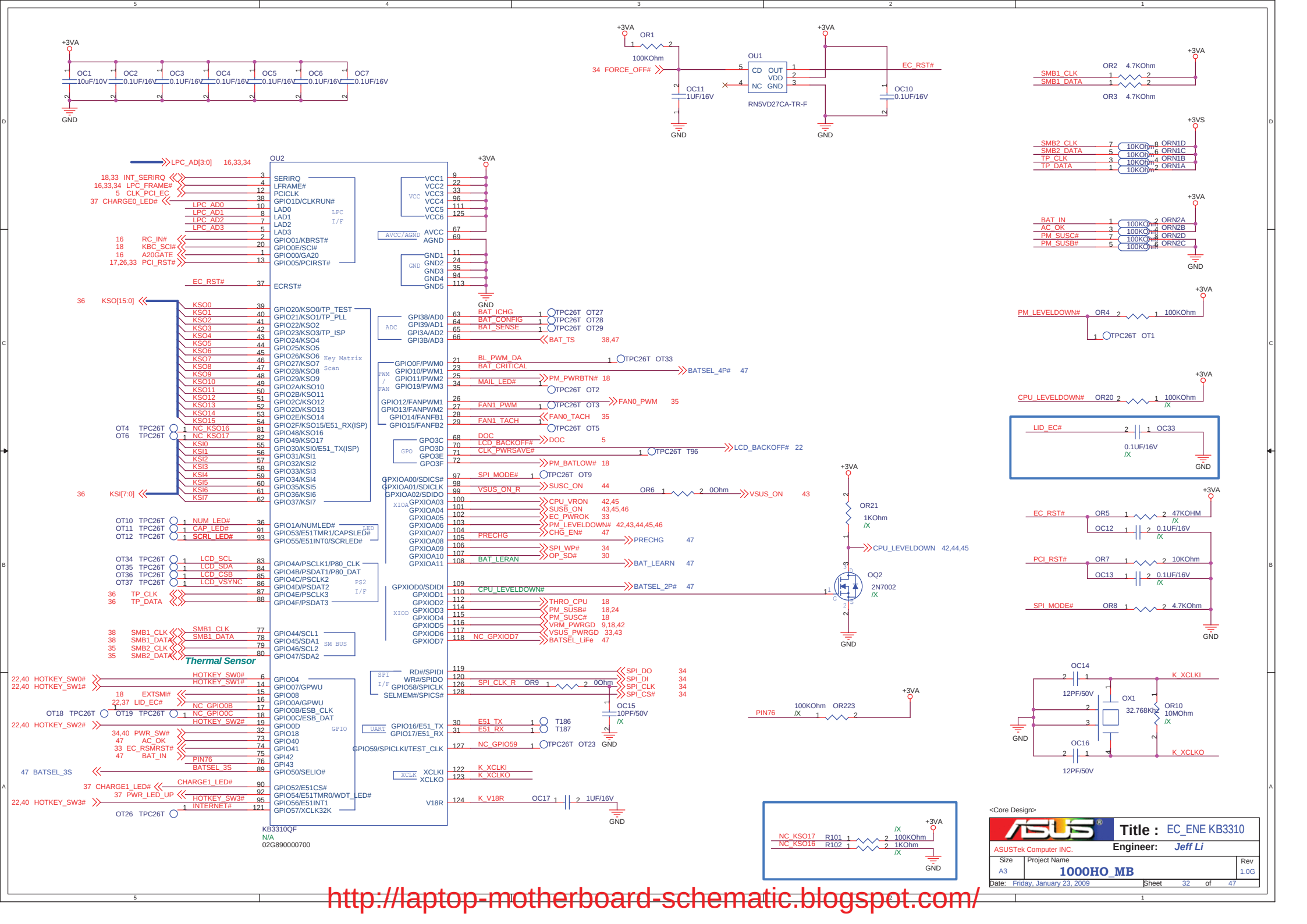
ASUSTek Computer Inc.	Title : AU6336-C52	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 29 of 47	

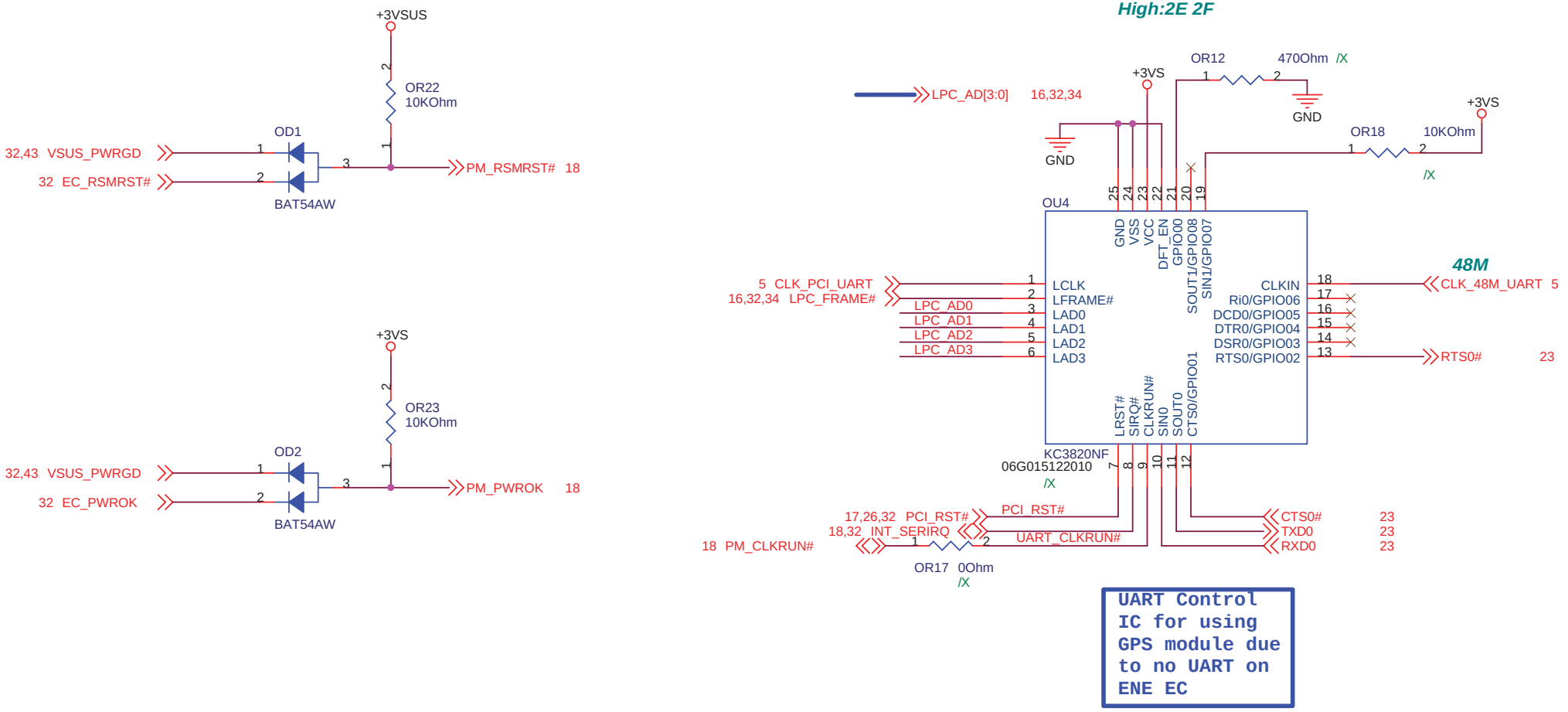




<Core Design>

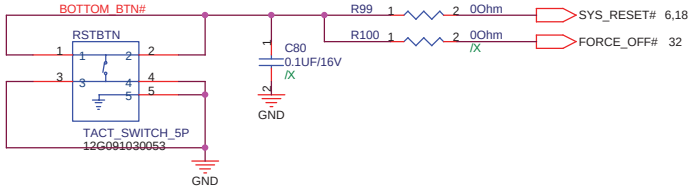
ASUSTek Computer Inc.	Title : ALC269-2	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 31 of 47	

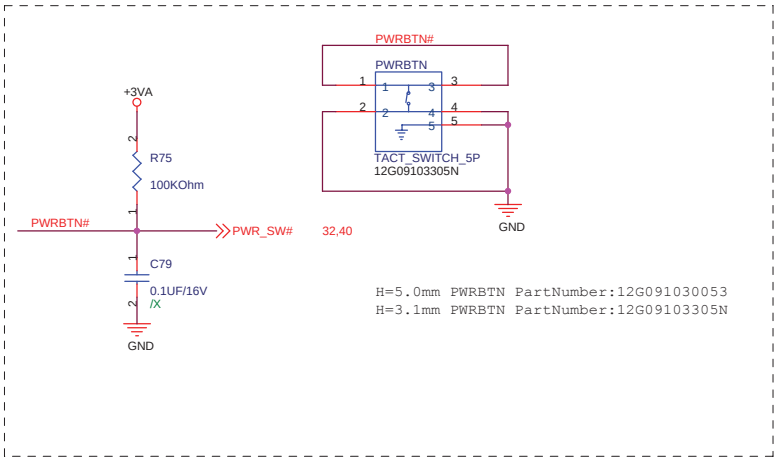


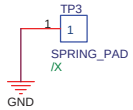


<Core Design>

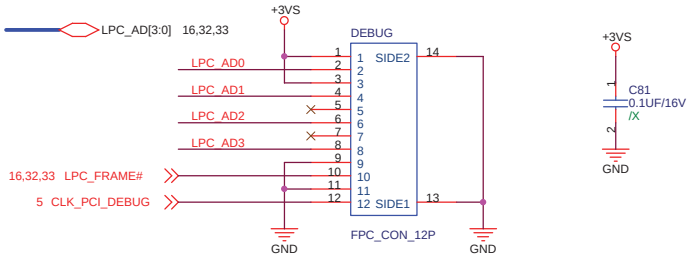
ASUSTek Computer INC.	Title : EC_UART_KC3820	
	Engineer: Jeff Li	
Size: A4	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 33 of 47	



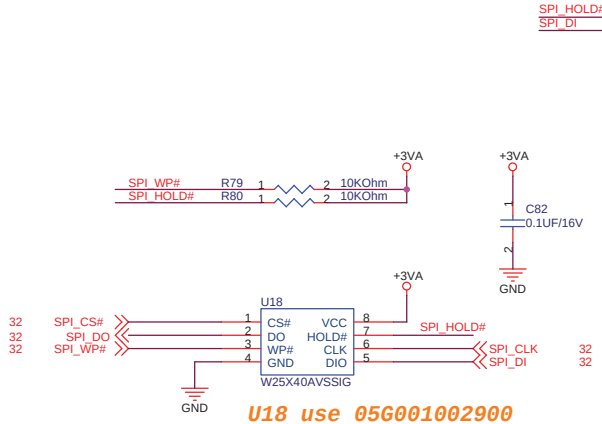




For Debug



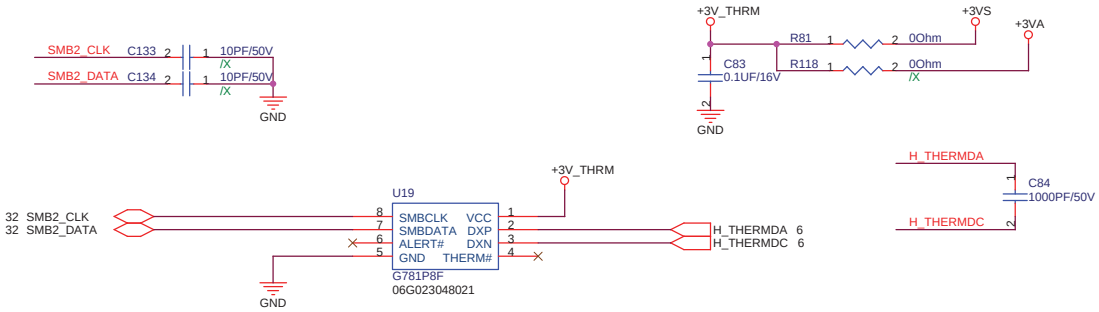
Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125



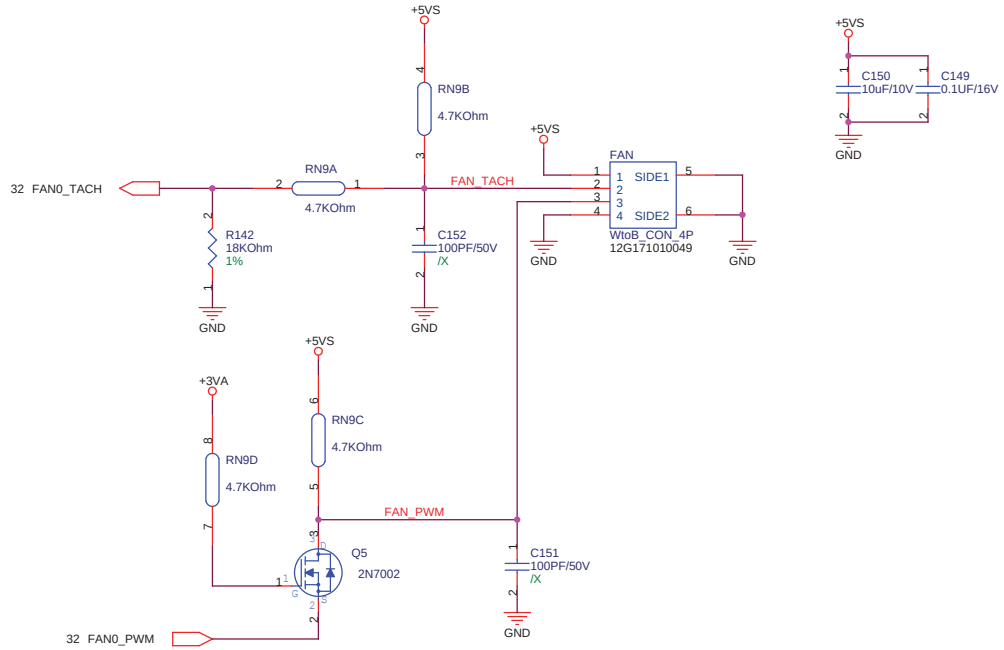
U18 use 05G001002900 & 05G00100F130

<Core Design>

ASUSTek Computer INC.	Title : Switch_SPI ROM_Debug	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 34 of 52	



U19 use 06G023048021

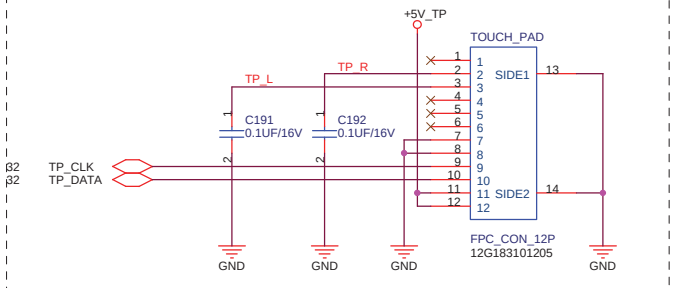


<Core Design>

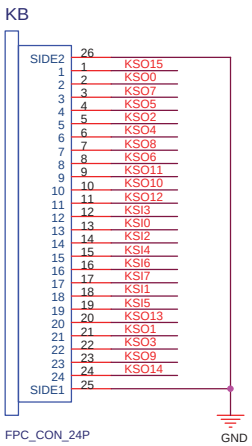
ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 35 of 52	

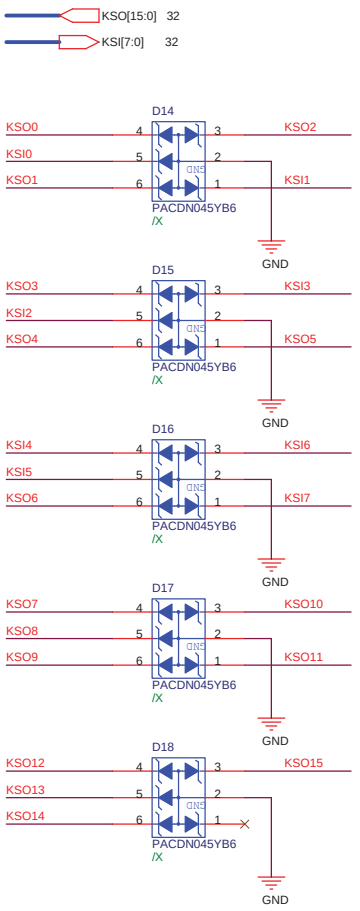
For Touch-Pad

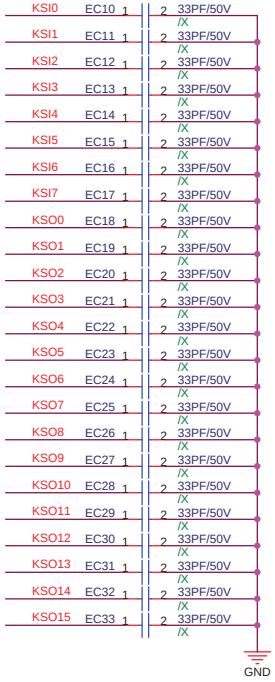
P900 R1.0G



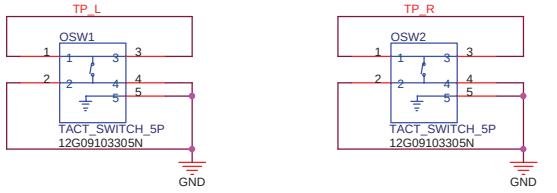
For Keyboard Connector

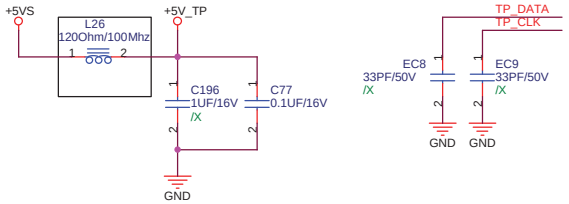


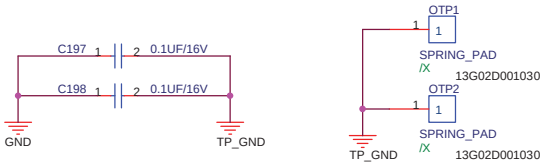




SW2, SW3 use 12G09103305N



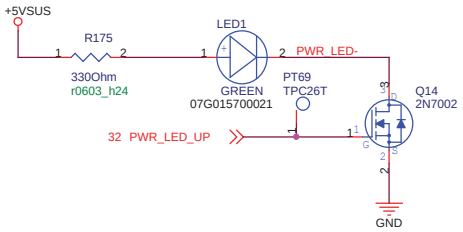




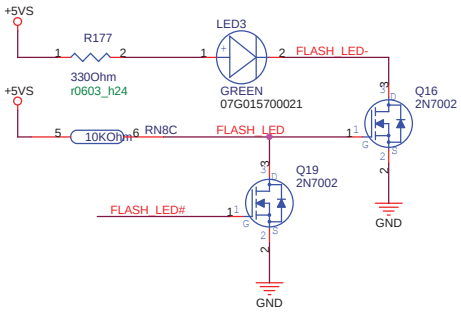
<Core Design>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 36 of 52	

for POWER LED

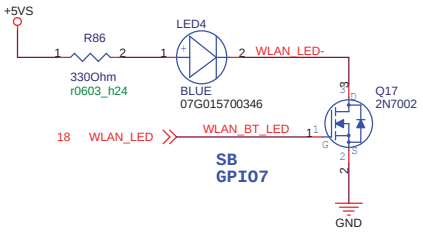


for FLASH LED

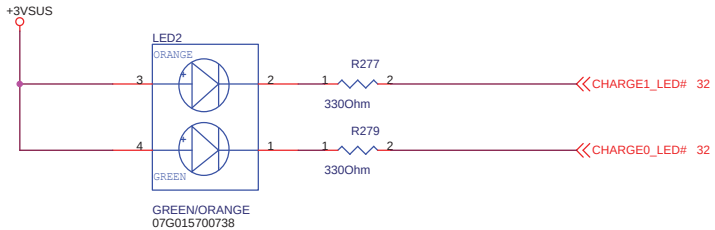


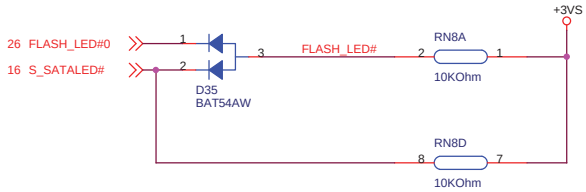
for WLAN/BlueTooth LED

R86 use 4.7K OHm 10G213472003030

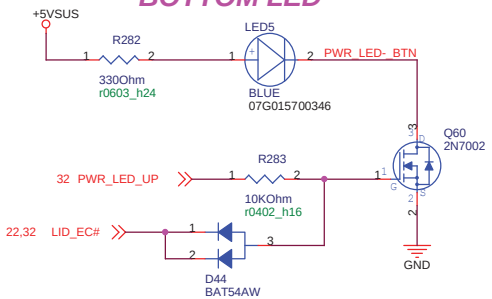


for CHARGE LED





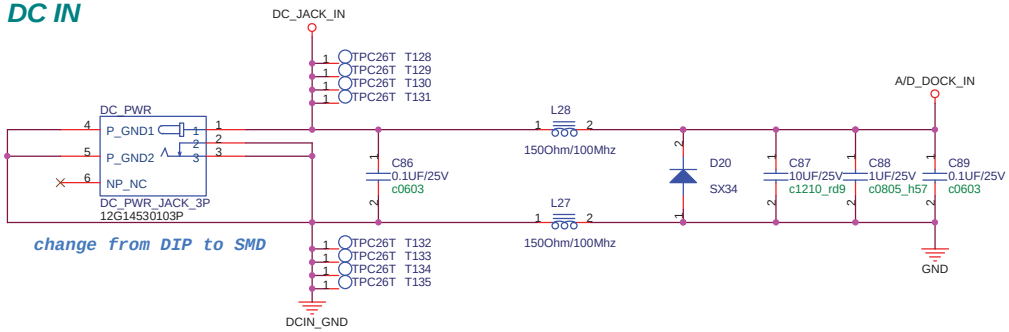
for POWER BOTTOM LED



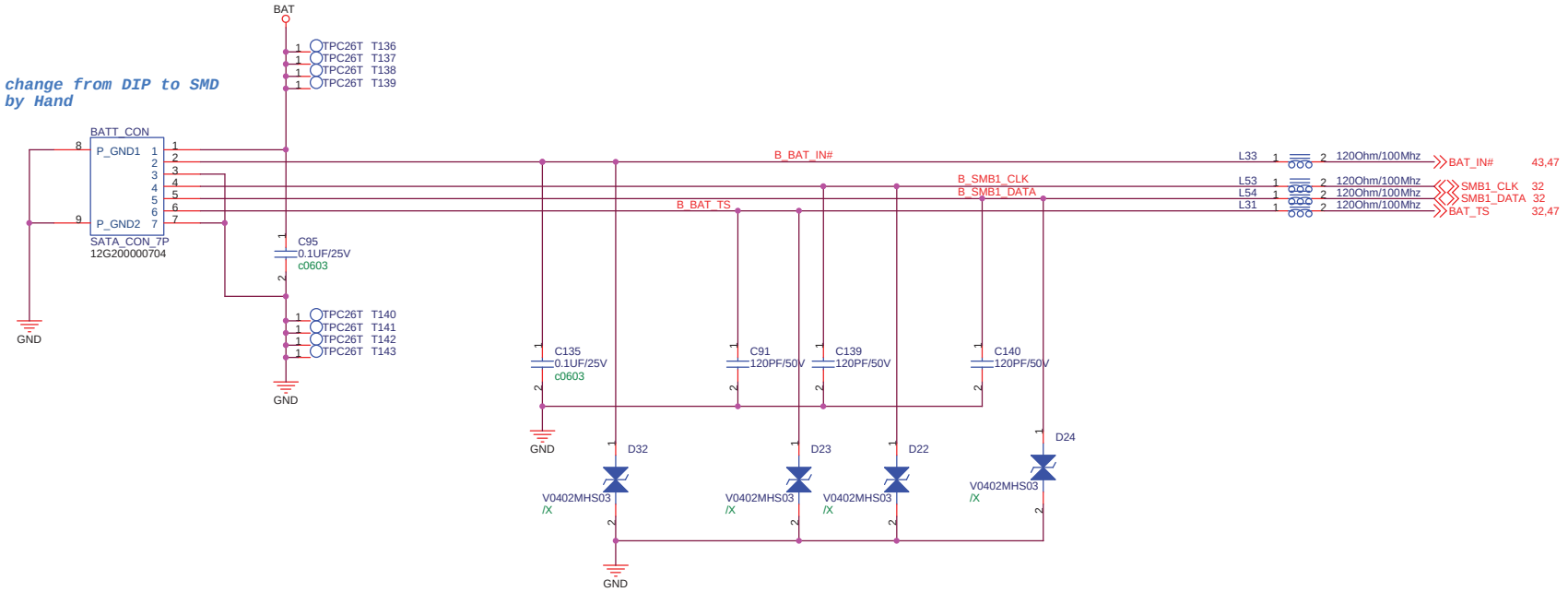
<Core Design>

ASUSTek Computer INC.	Title : LED	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 37 of 47	

DC IN

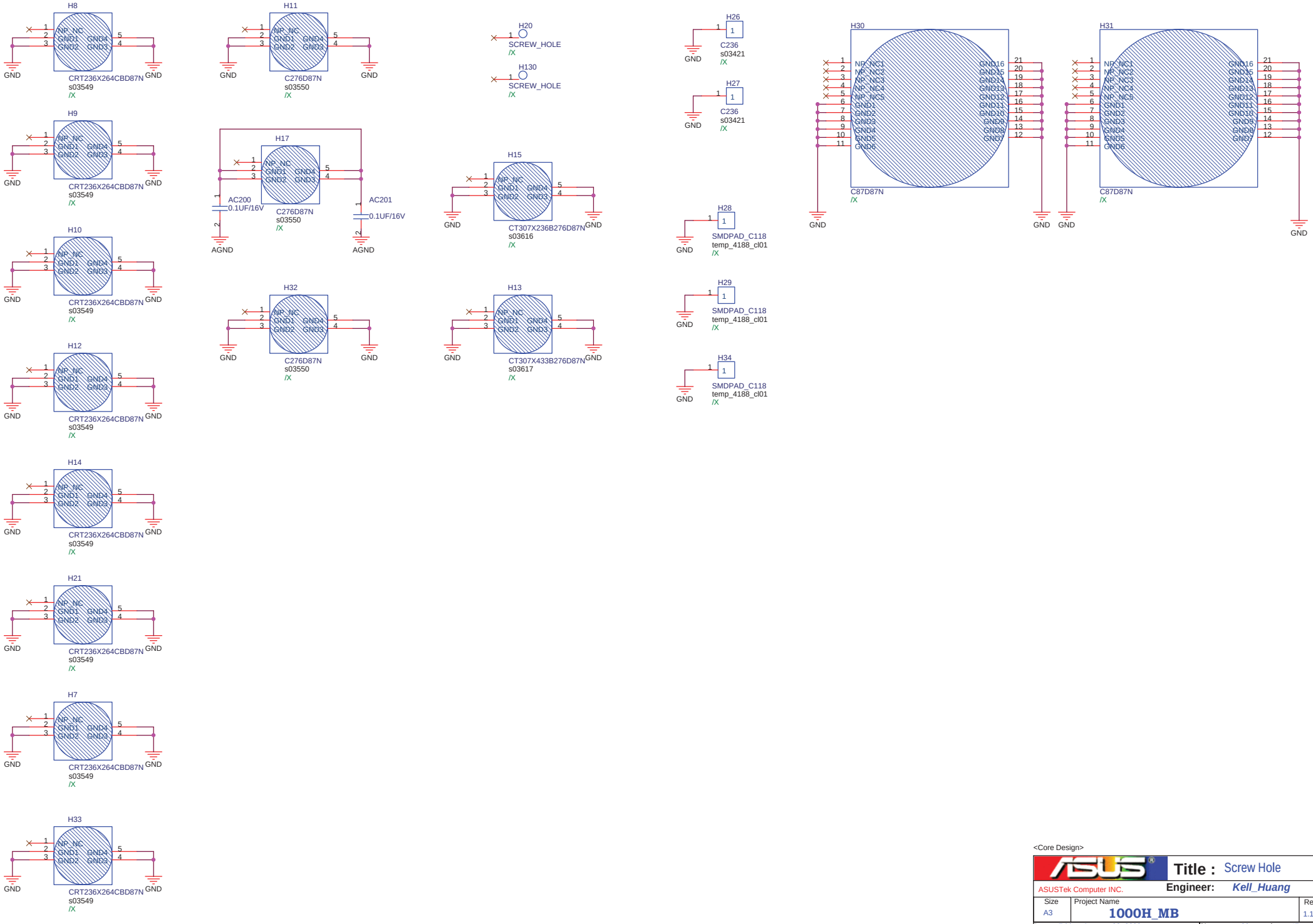


BAT IN



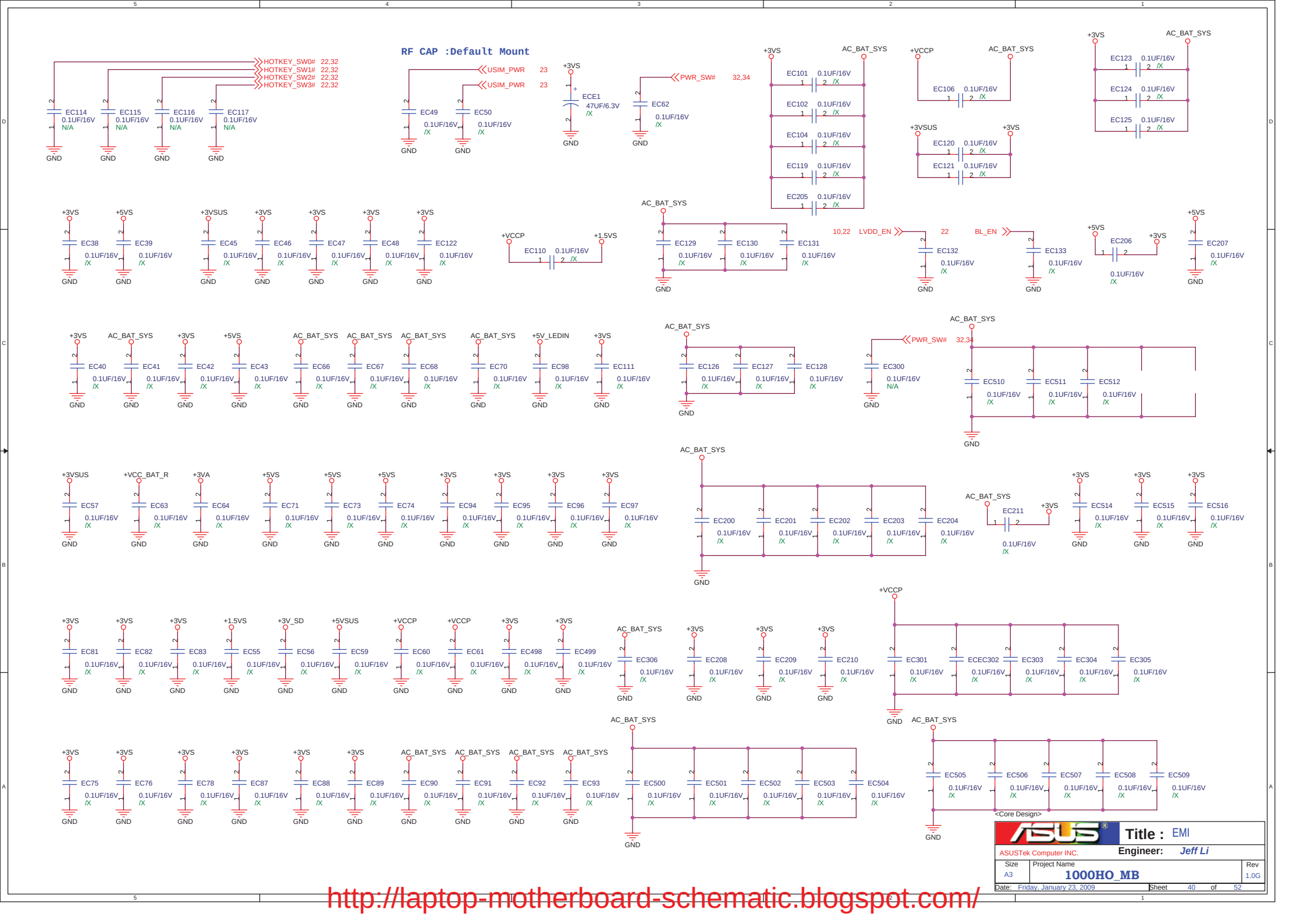
<Core Design>

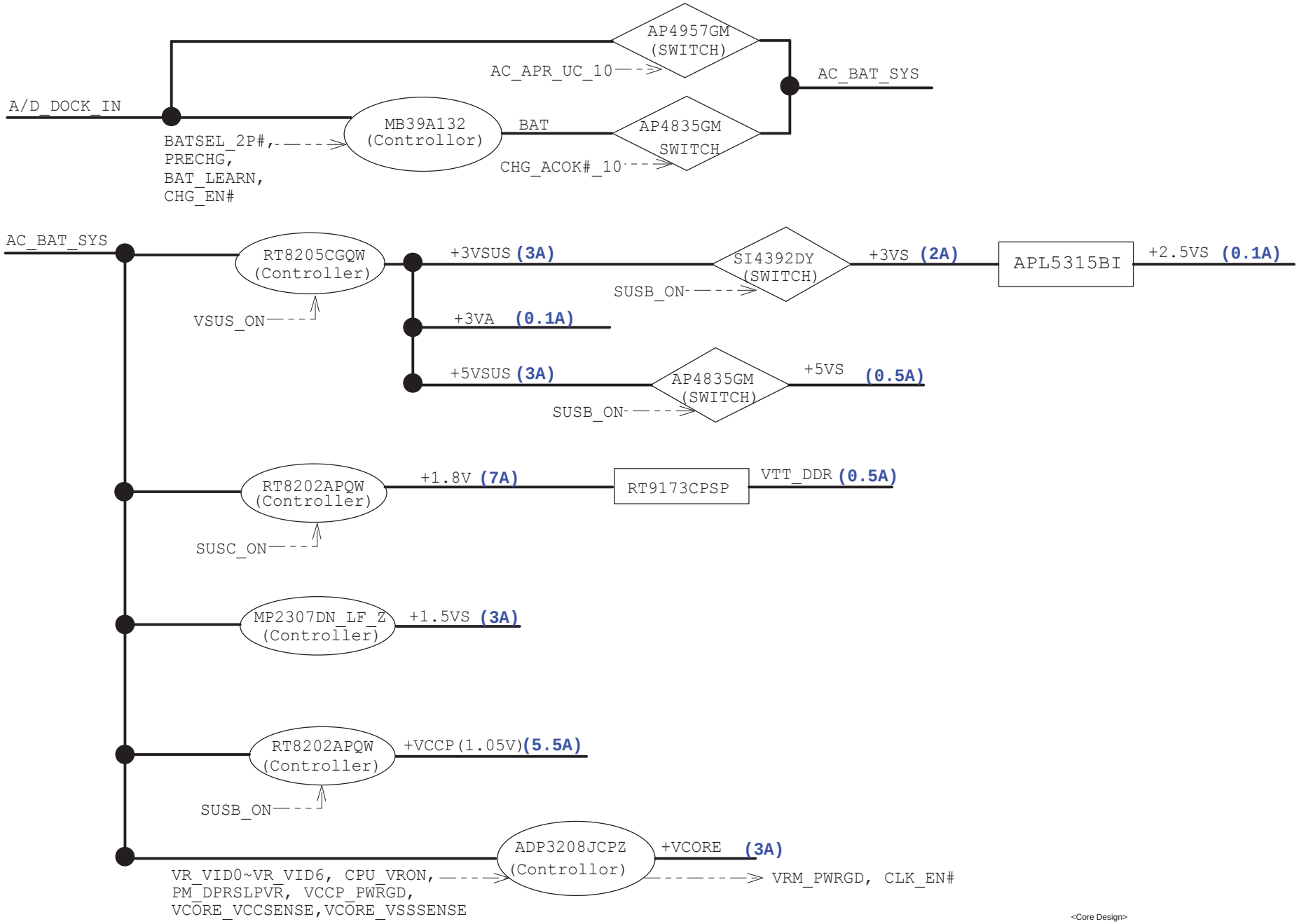
ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 38 of 52	



<Core Design>

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 39 of 47	





<Core Design>

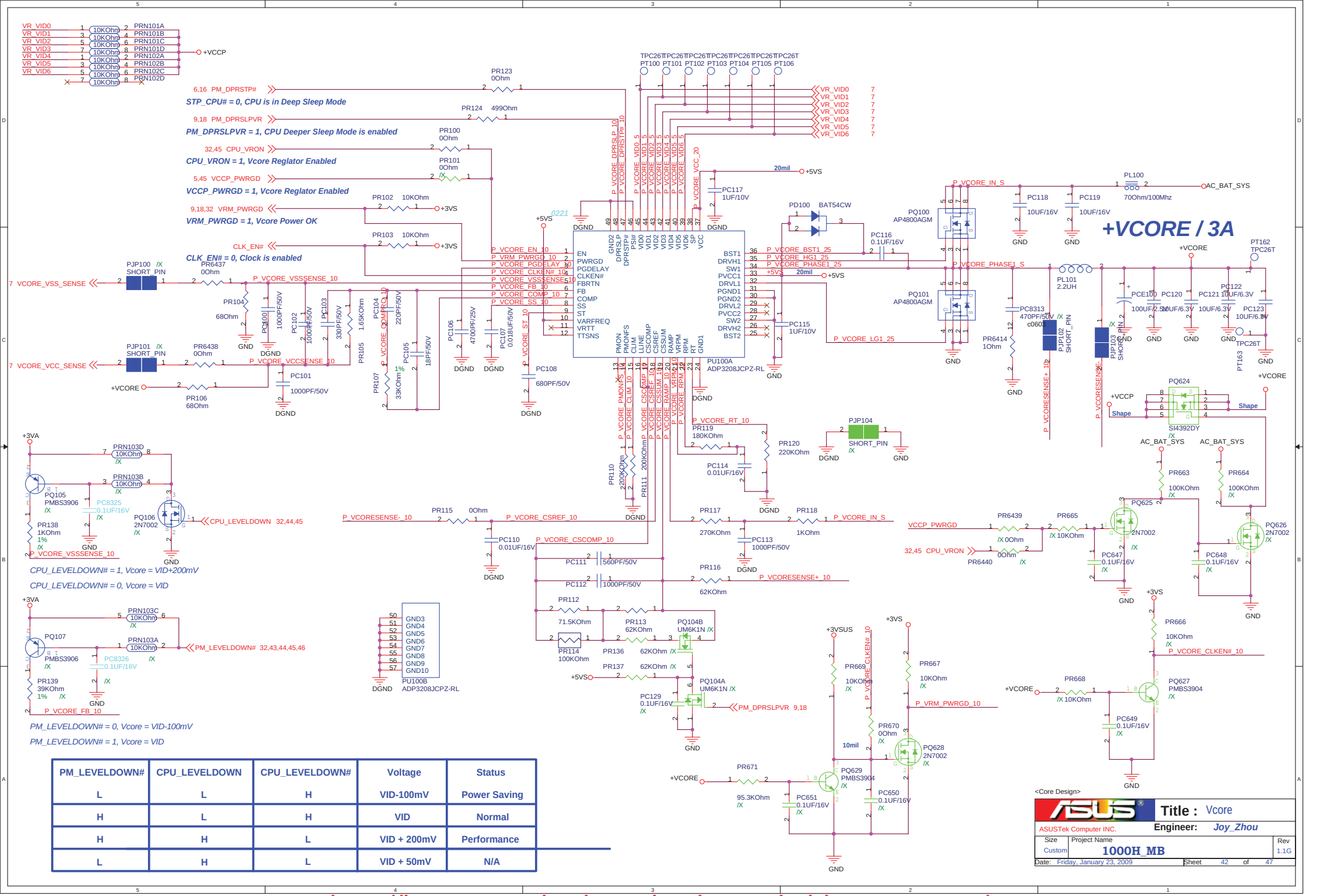
ASUSTek Computer INC.

Title : Power Flow

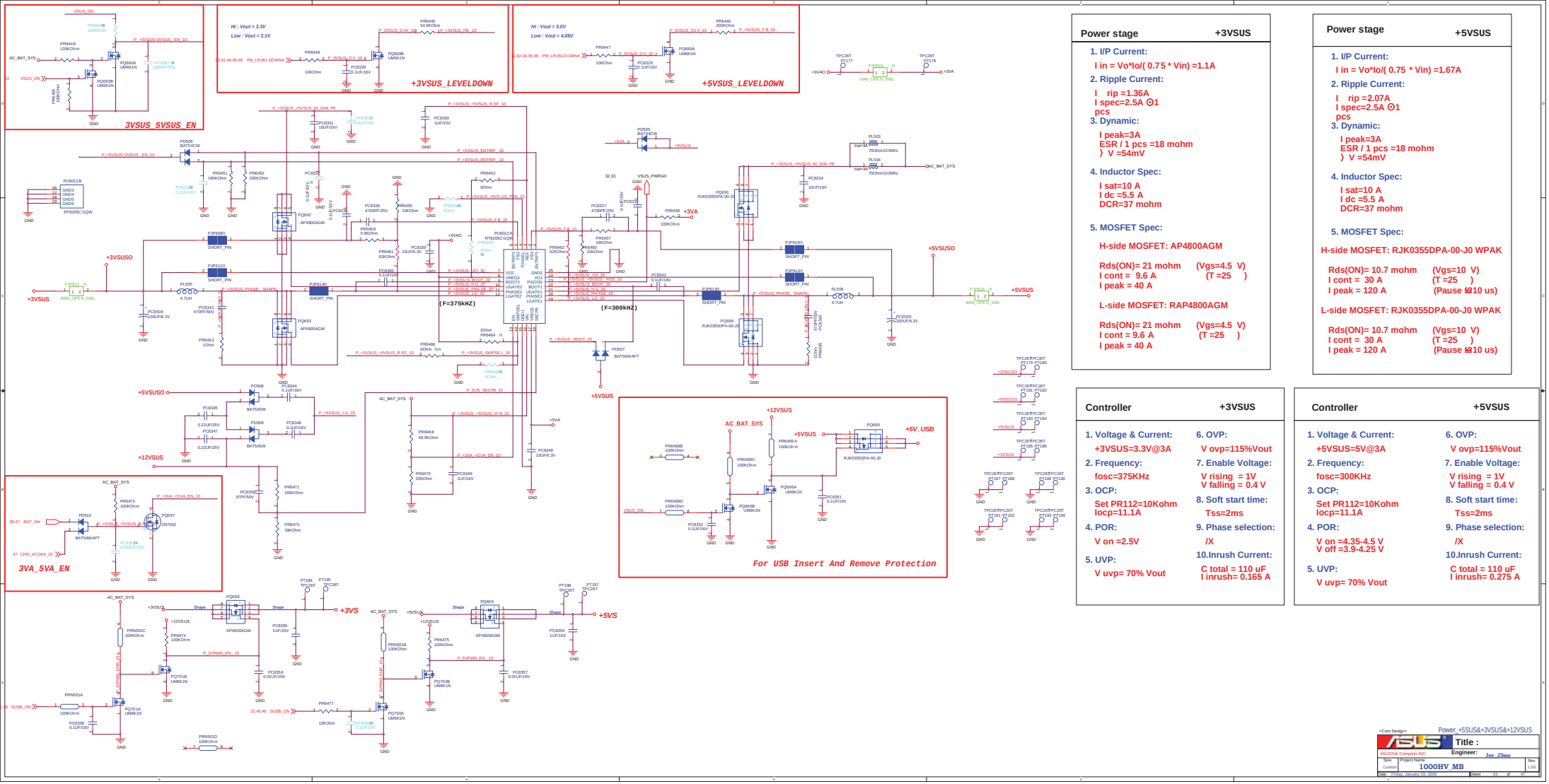
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 41 of 47



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A



Power stage +3VSUS

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.1A
2. Ripple Current:
   I rip =1.36A
   I spec=2.5A ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   〉V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:
   H-side MOSFET: AP4800AGM
   Rds(ON)= 21 mohm (Vgs=4.5 V)
   I cont = 9.6 A (T =25)
   I peak = 40 A
   L-side MOSFET: RAP4800AGM
   Rds(ON)= 21 mohm (Vgs=4.5 V)
   I cont = 9.6 A (T =25)
   I peak = 40 A

Power stage +5VSUS

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.67A
2. Ripple Current:
   I rip =2.07A
   I spec=2.5A ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   〉V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA-00-J0 WPAK
   Rds(ON)= 10.7 mohm (Vgs=10 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)
   L-side MOSFET: RJK0355DPA-00-J0 WPAK
   Rds(ON)= 10.7 mohm (Vgs=10 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

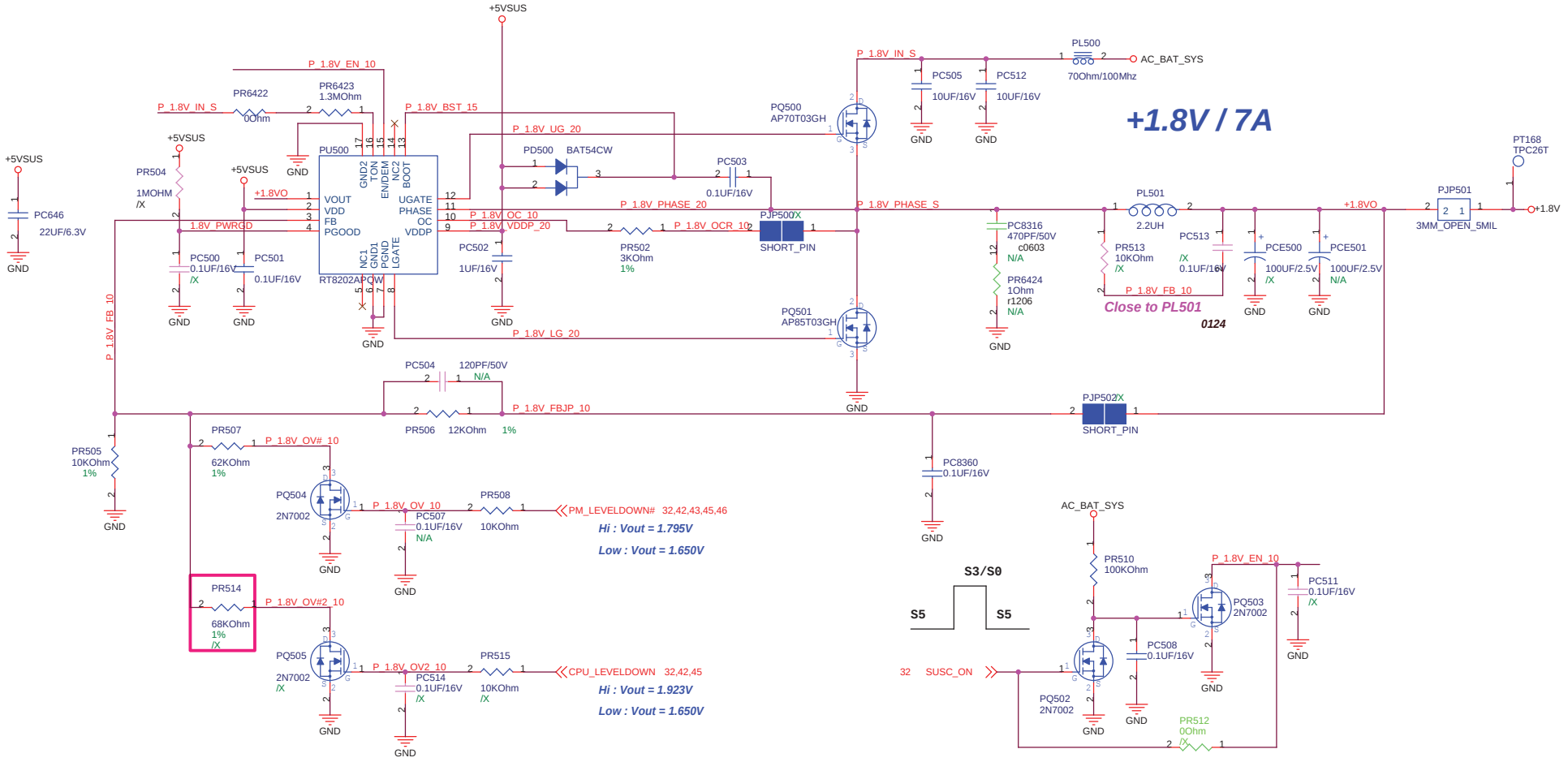
Controller +3VSUS

1. Voltage & Current:
   +3VSUS=3.3V@3A
2. Frequency:
   fosc=375KHz
3. OCP:
   Set PR112=10Kohm
   Iocp=11.1A
4. POR:
   V on =2.5V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 110 uF
    I inrush= 0.165 A

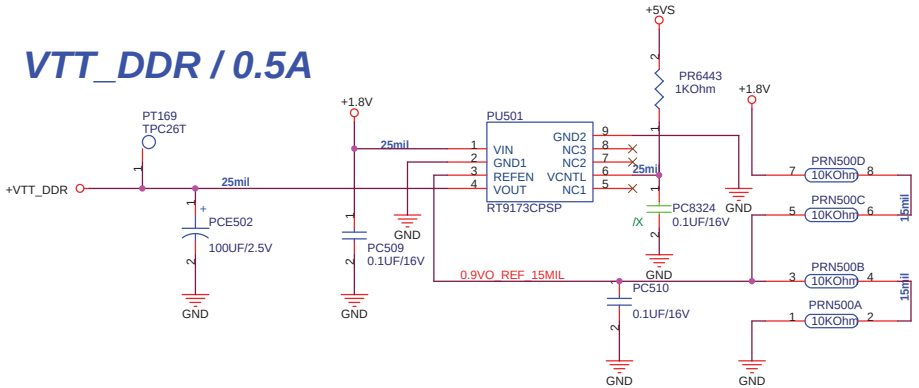
Controller +5VSUS

1. Voltage & Current:
   +5VSUS=5V@3A
2. Frequency:
   fosc=300KHz
3. OCP:
   Set PR112=10Kohm
   Iocp=11.1A
4. POR:
   V on =4.35-4.5 V
   V off =3.9-4.25 V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 110 uF
    I inrush= 0.275 A

<Core Design> Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTeK Computer INC
Engineer: Jay_Zhou
Size: Custom | Project Name: 1000HV_MB | Rev: 1.00
Date: Friday, January 22, 2010 | Sheet 43 of 47



VTT_DDR / 0.5A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

<Core Design>

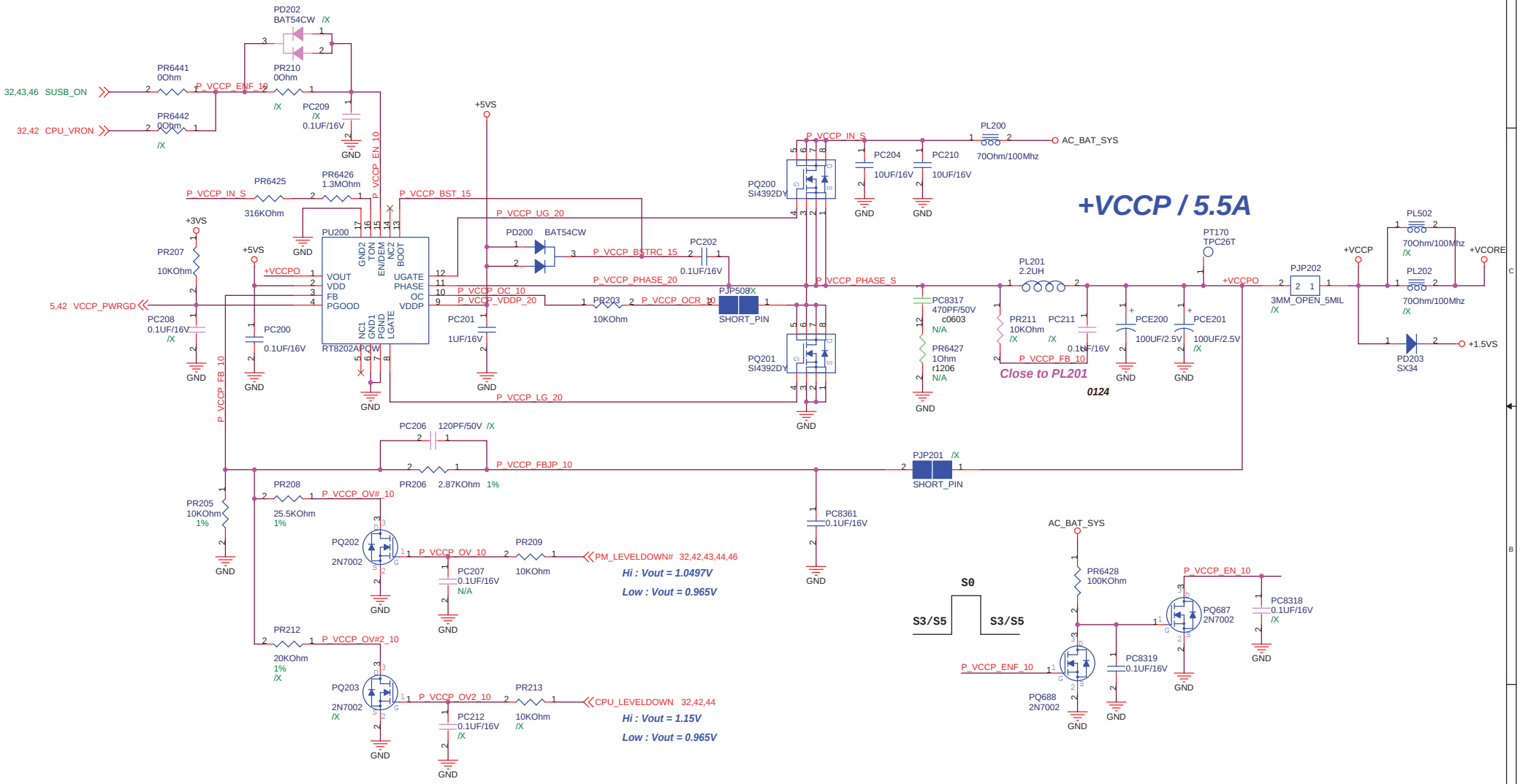
ASUSTek Computer INC.

Title : +1.8V & VTTDDR

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 44 of 47



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<Core Design>

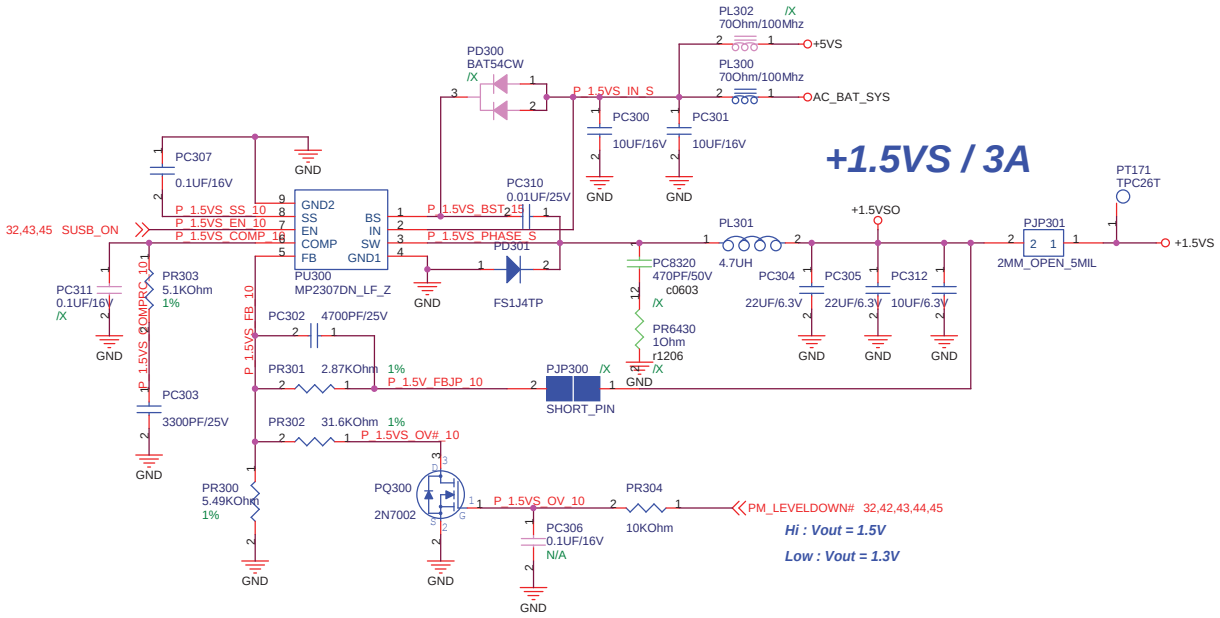
ASUSTek Computer INC.

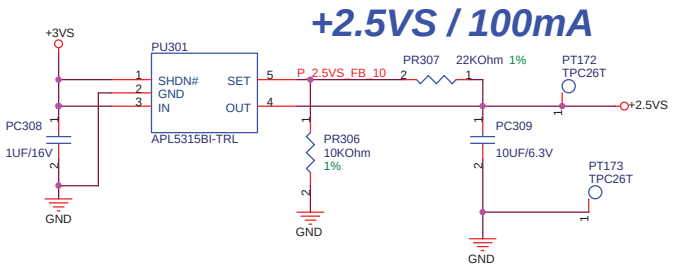
Title : VCCP

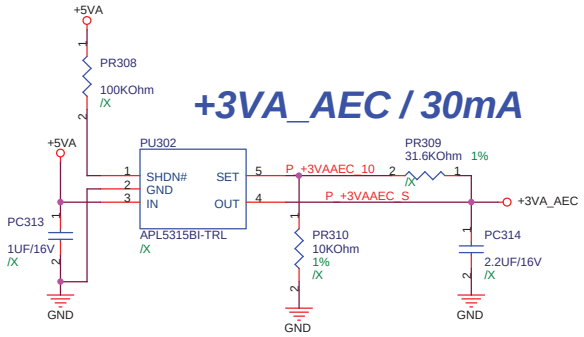
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 45 of 47

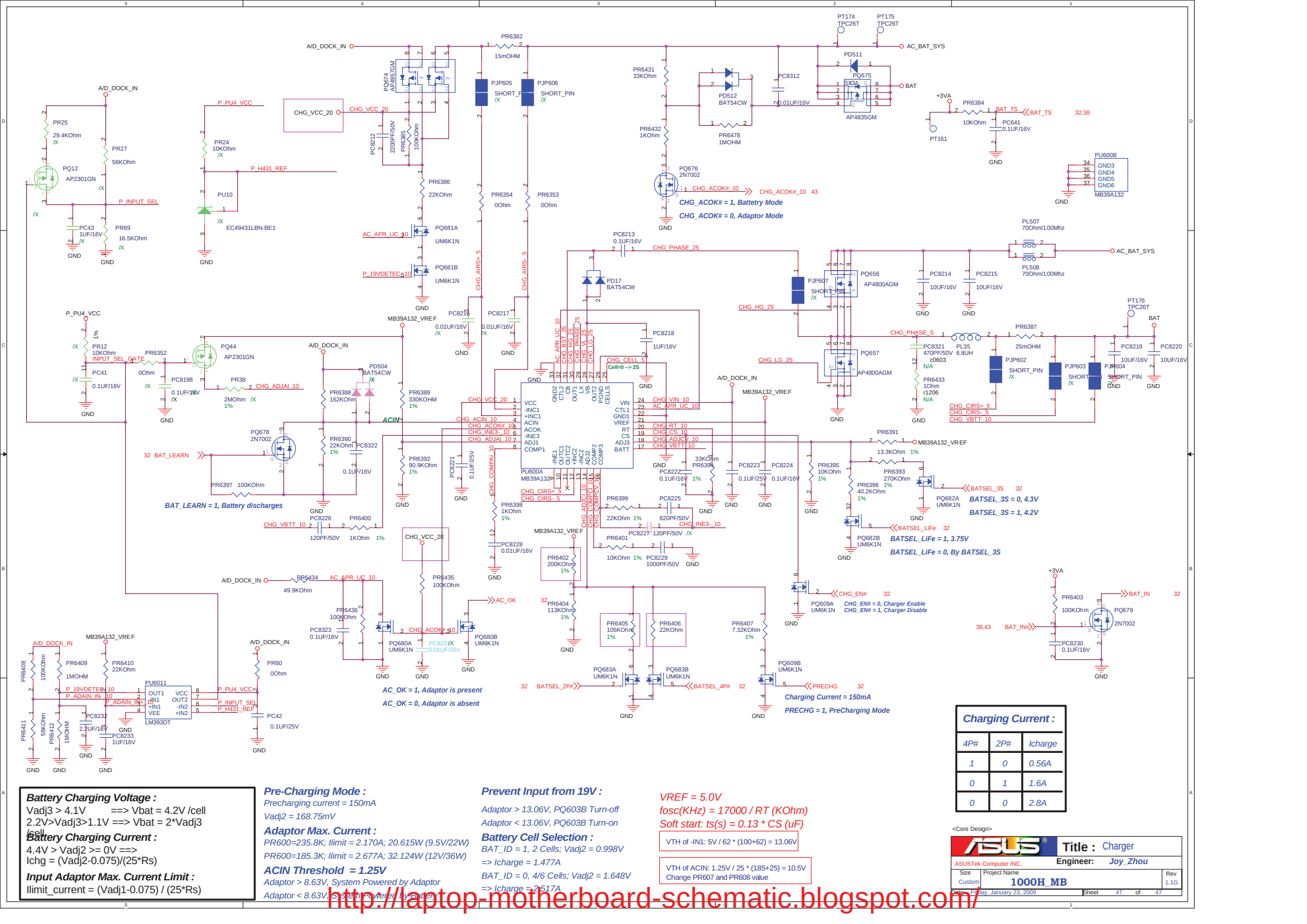






<Core Design>

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 46 of 47	



<Core Design>

ASUSTek Computer INC.	Title : Note	
	Engineer: KingCa_Jin	
Size: A3	Project Name: 1000HE_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 48 of 47	