Compal Confidential

Schematics Document

P4 uFCBGA/uFCPGA Northwood with SIS Core Logic

2001-5-30

REV:1.0A

Compal Electronics, Inc.			
Title	Cover Sheet		
Size	Document Number ACT10		Rev 1.0A
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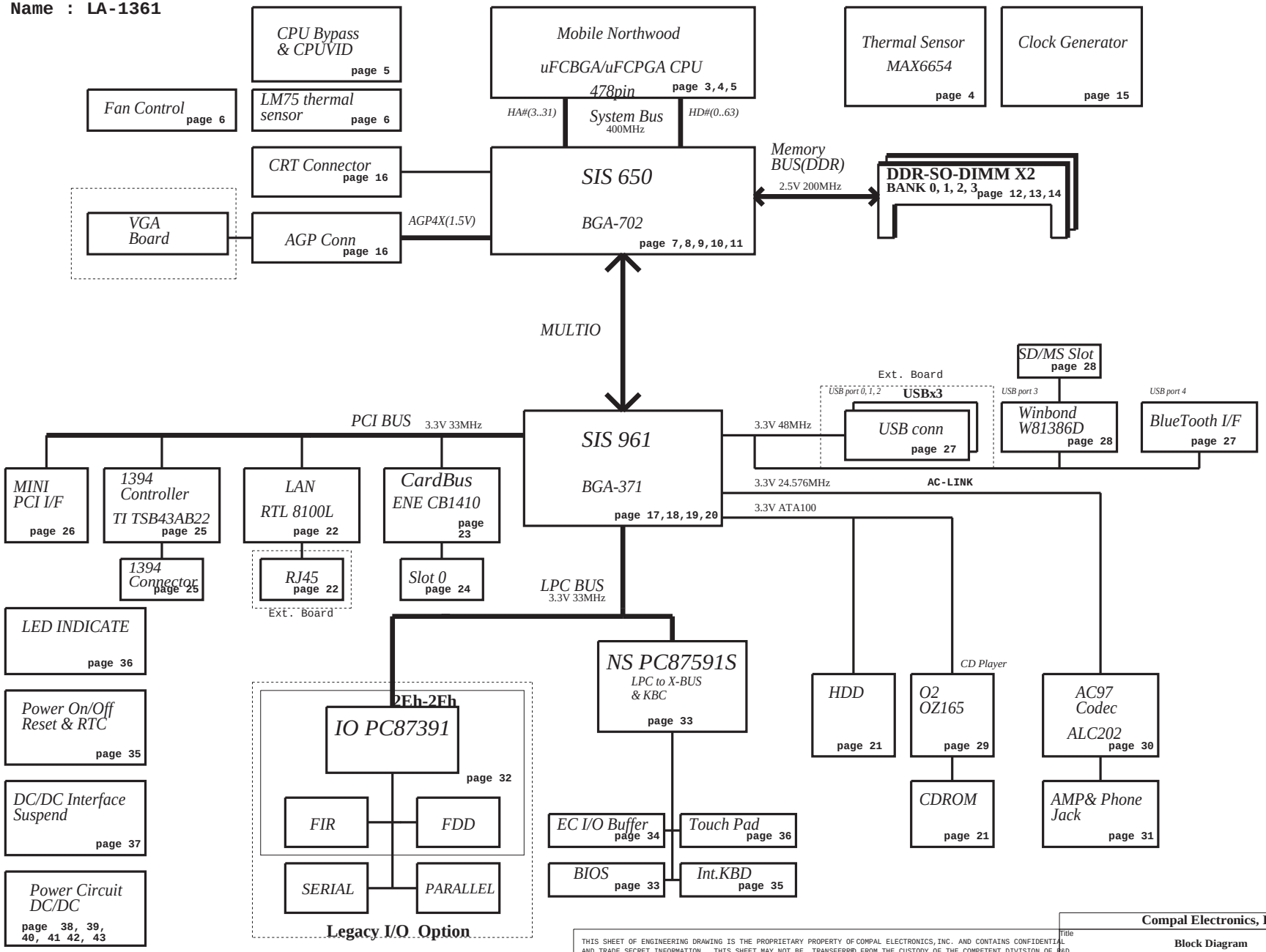
Model Name :CT10

File Name : LA-1361



Compal Electronics, Inc.

Title: Block Diagram

Size: | Document Number: ACT10 | Rev: 1.0A

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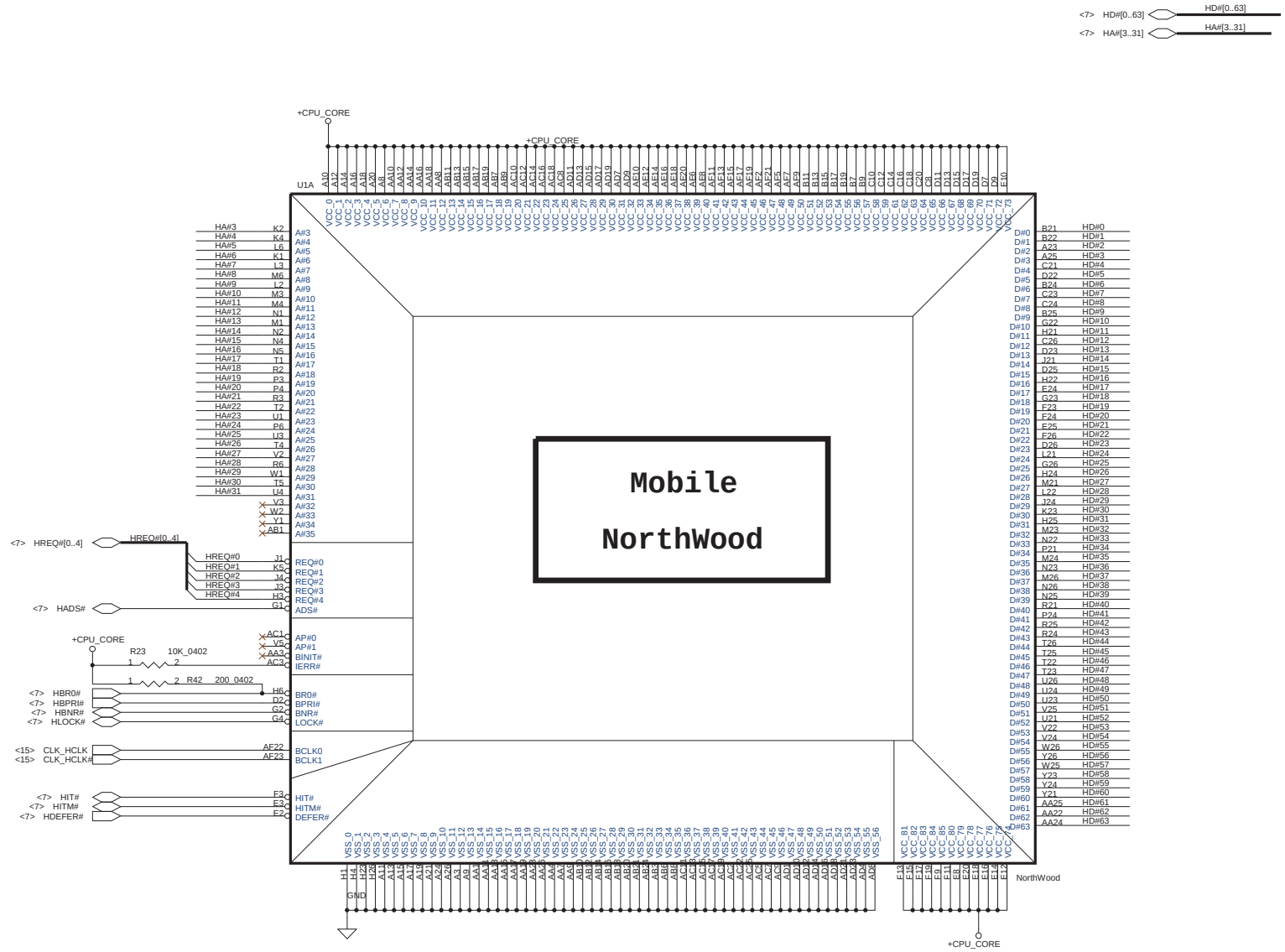

Compal Electronics, Inc.	
Title: Mobile Northwood uFCPGA	
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Mobile NorthWood

U1B

Place resistor <100mils from CPU pin

If used ITP port must depop

Thermal Sensor MAX6654MEE

GTL Reference Voltage

Layout note :
1. Place R_A and R_B near CPU.
2. Place decoupling cap 220PF near CPU.(Within 500mils)

All of these pin connected inside

BSEL0	BSEL1	
0	0	100
0	1	Resvd
1	0	Resvd
1	1	Resvd

Address:1001_110X

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Title	Mobile Northwood uFCPGA & Thermal sensor	
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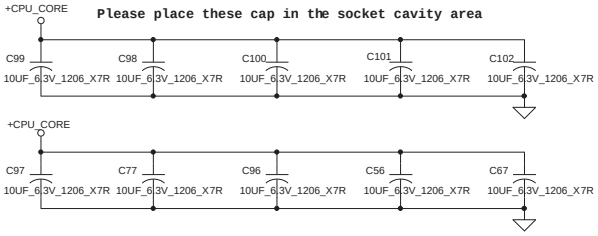
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

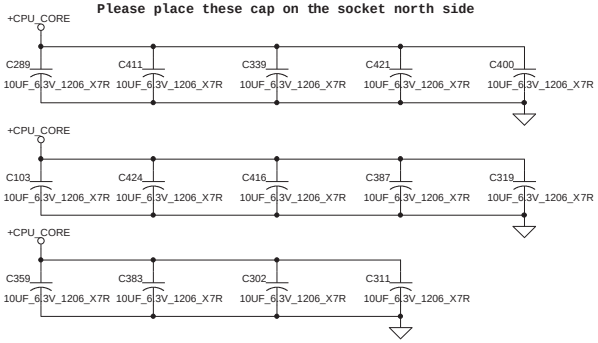
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

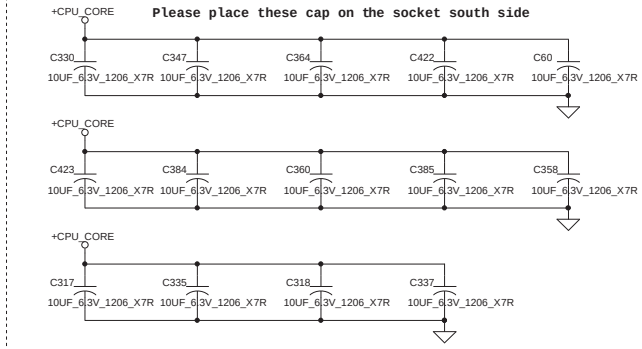
Please place these cap in the socket cavity area



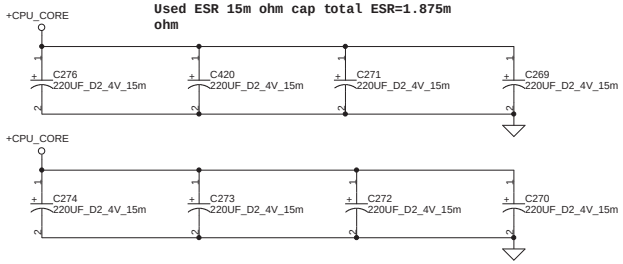
Please place these cap on the socket north side

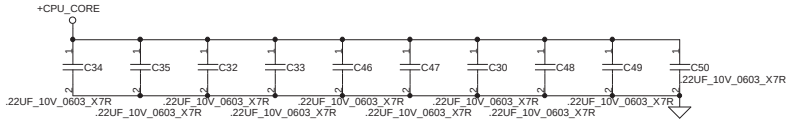


Please place these cap on the socket south side

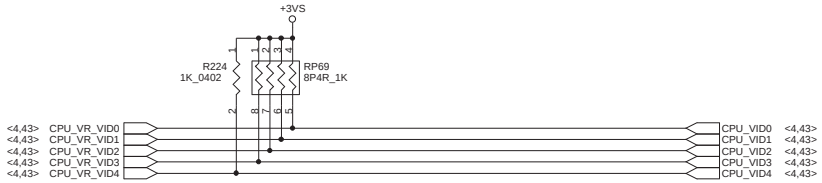


Used ESR 15m ohm cap total ESR=1.875m ohm

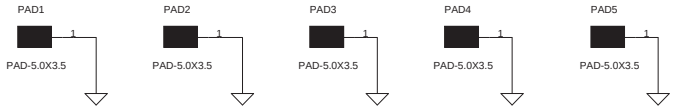




CPU Voltage ID



EMI Clip PAD for CPU



Compal Electronics, Inc.

Title	CPU Bypass & CPU VID	
Size	Document Number ACT10	Rev 1.0A
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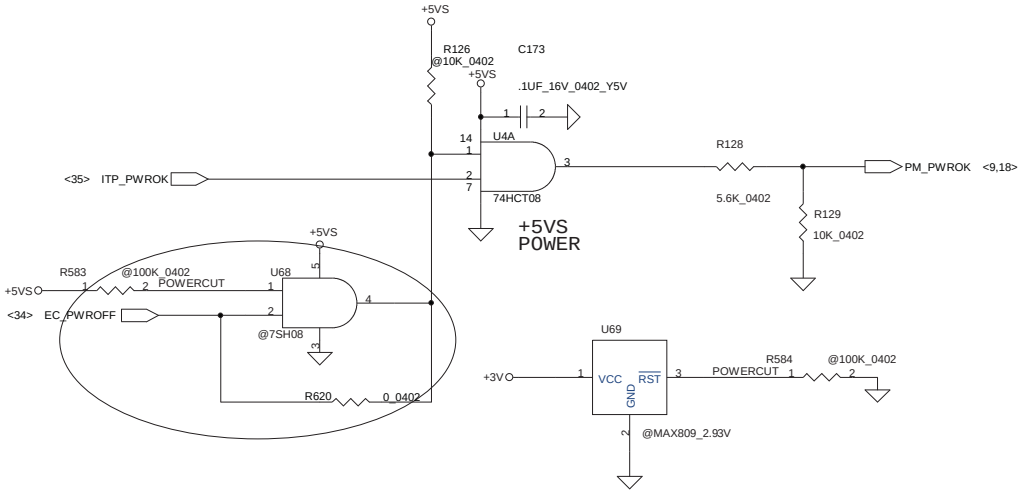
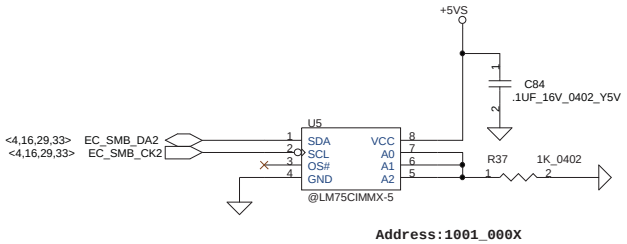
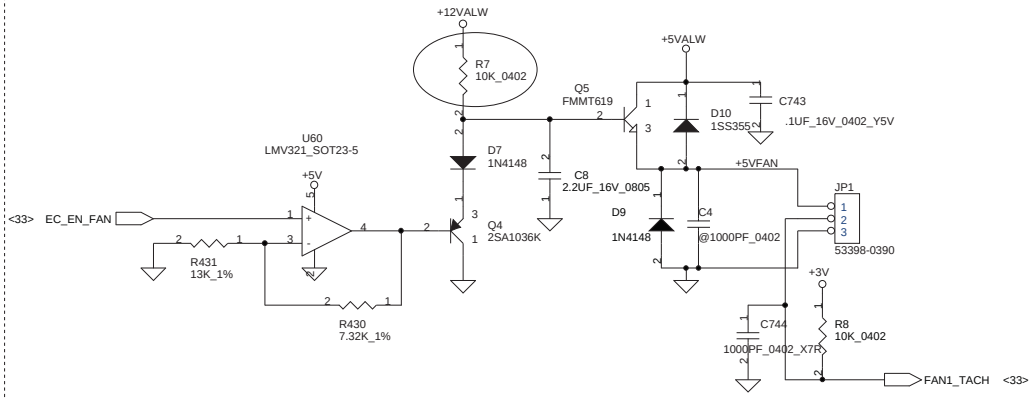




Dectect PCB Thermal

Fan1 Control circuit



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Title: LM75 Thermal sensor & Fan control		
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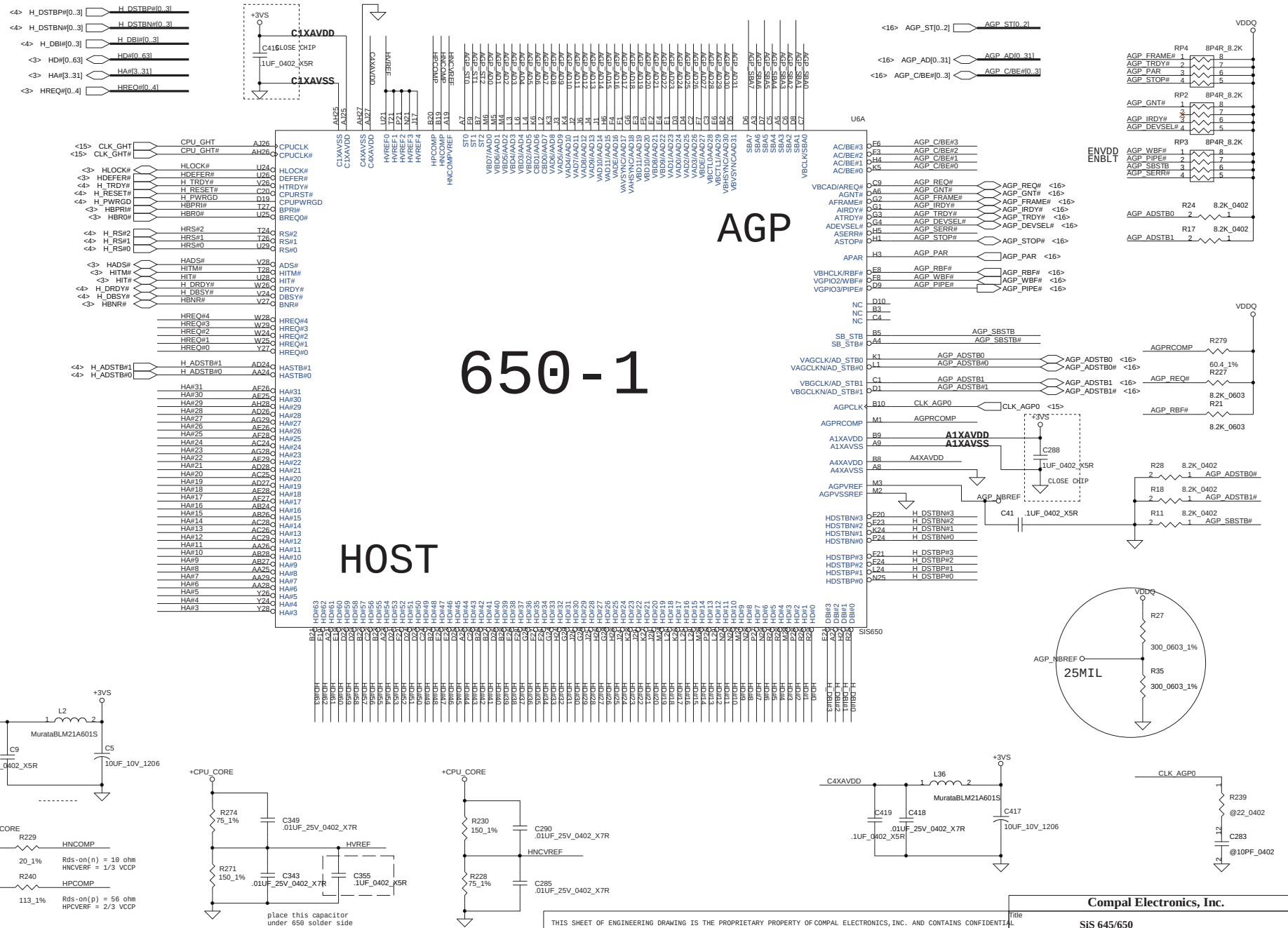

Compal Electronics, Inc.

Title: SiS 645/650

Size: Document Number: ACT10 Rev: 1.0A

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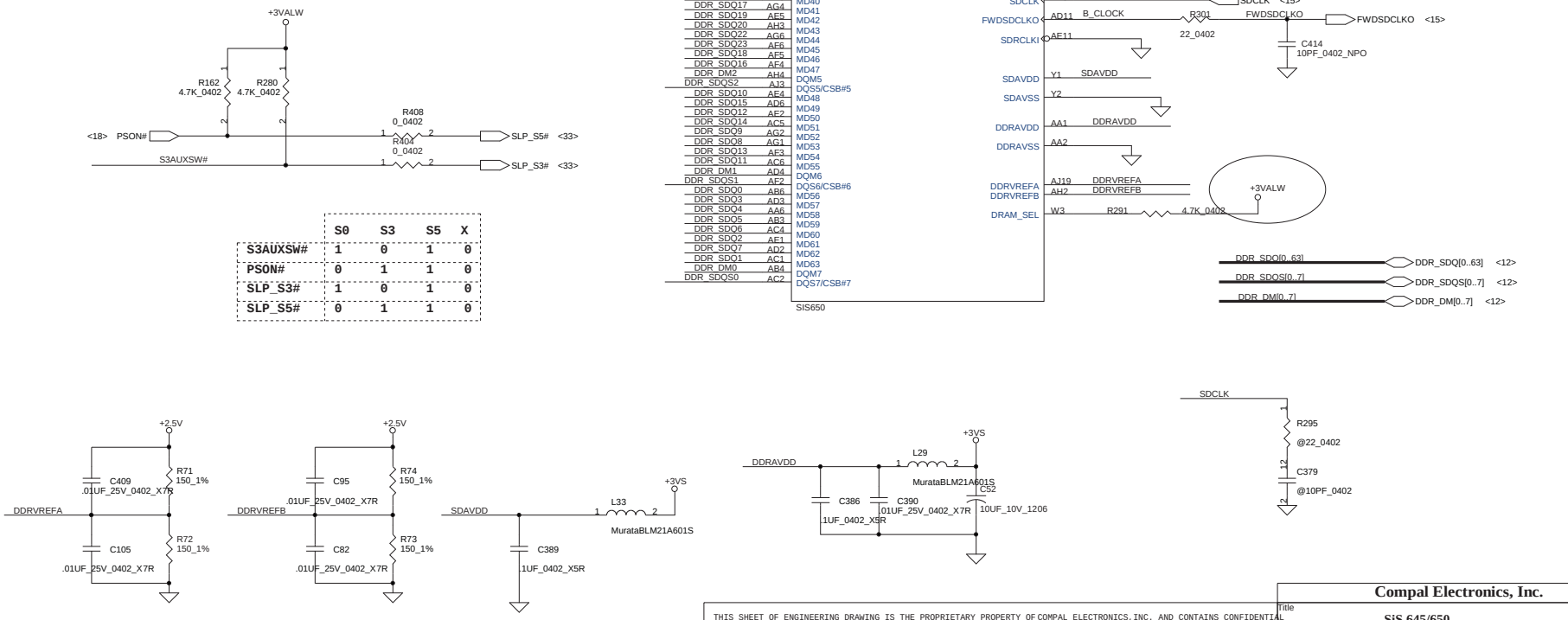

	S0	S3	S5	X
S3AUXSW#	1	0	1	0
PSON#	0	1	1	0
SLP_S3#	1	0	1	0
SLP_S5#	0	1	1	0

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Title	SiS 645/650	
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NB Hardware Trap Table(For Mobil Only)

	0	1	Default	
DLLEN#	enable PLL	disable PLL	0	embedded pull-low (30~50K Ohm)
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	Panel ID0		X	yes
CSYNC	Panel ID1		X	
RSYNC	enable VGA interface		1	
LSYNC	Panel ID2		X	

CLK_NB14M — R248 @22_0402 — C299 @10PF_0402
ZCLK0 — R285 @22_0402 — C361 @10PF_0402

+1.8VS — R39 150_1% — C353 .1UF_0402_X5R — ZVREF — R38 150_1% — C357 .1UF_0402_X5R

<17> ZAD[0..15] — ZAD[0..15]

U6C
SIS650

<15> ZCLK0	ZCLK0	V3	ZCLK
<17> ZUREQ	ZUREQ	U6	ZUREQ
<17> ZDREQ	ZDREQ	U1	ZDREQ
<17> ZSTB0	ZSTB0	T3	ZSTB0
<17> ZSTB#0	ZSTB#0	T1	ZSTB#0
<17> ZSTB1	ZSTB1	P1	ZSTB1
<17> ZSTB#1	ZSTB#1	P3	ZSTB#1
	ZAD0	T4	ZAD0
	ZAD1	R3	ZAD1
	ZAD2	T5	ZAD2
	ZAD3	T6	ZAD3
	ZAD4	R2	ZAD4
	ZAD5	R6	ZAD5
	ZAD6	R1	ZAD6
	ZAD7	R4	ZAD7
	ZAD8	P4	ZAD8
	ZAD9	N3	ZAD9
	ZAD10	P5	ZAD10
	ZAD11	P6	ZAD11
	ZAD12	N1	ZAD12
	ZAD13	N6	ZAD13
	ZAD14	N2	ZAD14
	ZAD15	N4	ZAD15
	ZVREF	U3	ZVREF
	VDDZCMP	V5	VDDZCMP
	ZCMP_N	U4	ZCMP_N
	ZCMP_P	U2	ZCMP_P
		V6	VSSZCMP
	Z4XAVDD	W1	Z1XAVDD
		W2	Z1XAVSS
	Z4XAVDD	V2	Z4XAVDD
		V1	Z4XAVSS
<17> 961_PCIRST#		Y3	PCIRST#
<6,18> PM_PWROK	PWRGD	W4	PWROK
<18,33,35> RSMRST#	AUXOK	W6	AUXOK
PID0_OLD — R257 1K_0402	TRAP0	D11	TRAP1
		E10	TRAP0

VOSCI	C15	CLK_NB14M	CLK_NB14M <15>
ROUT	A12	ROUT — R13 0_0402	CRT_R_SIS <16>
GOUT	B13	GOUT — R12 0_0402	CRT_G_SIS <16>
BOUT	A13	BOUT — R14 0_0402	CRT_B_SIS <16>
HSYNC	F13	R263 33_0402	HSYNC_SIS <16>
VSYNC	E13	R253 33_0402	VSYNC_SIS <16>
		RP68 4P2R_100	
VGPIO0	D13	DDCCL_SIS	DDCCL_SIS <16>
VGPIO1	D12	DDCDA_SIS	DDCDA_SIS <16>
INT#A	B11		SIS_PIRQA# <16>
CSYNC	E12	PID1_OLD	
RSYNC	A11	RSYNC	
LSYNC	F12	PID2_OLD	
VCOMP	E14	VCOMP	
VRSET	D14	VRSET — R250 130_1%	
VVBWN	F14	VVBWN	
DACAVDD1	B12	DACAVDD2	
DACAVSS1	C12		
DACAVDD2	C13	DACAVDD2	
DACAVSS2	C14		
DCLKAVDD	B15	DCLKAVDD	
DCLKAVSS	A15		
ECLKAVDD	B14	ECLKAVDD	
ECLKAVSS	A14		
ENTEST	F10	ENTEST	
DLLEN#	E11	DLLEN#	
TESTMODE0	C11		
TESTMODE1	F11		
TESTMODE2	A10	R259 1K_0402	

for 650 only — +3VS
RSYNC — R234 4.7K_0402
PID0_OLD — R254 @10K_0402
PID1_OLD — R265 @10K_0402
PID2_OLD — R264 @10K_0402

+3VS — L28 MurataBLM21A601S — Z4XAVDD
C45 10UF_10V_1206 — C372 .01UF_25V_0402_X7R

C382 .01UF_25V_0402_X7R — Z4XAVDD

Ap Note:
DACAVDD1 & DACAVDD2 connect together
DACAVSS1 & DACAVSS2 connect together

ENTEST — R266 4.7K_0402
PWRGD — C388 .1UF_0402_X5R
AUXOK — C374 @.1UF_0402_X5R

+1.8VS — R277 0_0603 — C366 .1UF_0402_X5R — C348 .01UF_25V_0402_X7R
VDDZCMP
R286 56_0402 — ZCMP_N
R290 56_0402 — ZCMP_P

L13 MurataBLM21A601S — +3VS
DCLKAVDD — C292 .01UF_25V_0402_X7R — C291 .1UF_0402_X5R — C275 10UF_10V_1206

L14 MurataBLM21A601S — +3VS
ECLKAVDD — C294 .01UF_25V_0402_X7R — C293 .1UF_0402_X5R — C268 10UF_10V_1206

VVBWN — C300 .1UF_0402_X5R
VCOMP — C301 .1UF_0402_X5R
DACAVDD2 — L17 MurataBLM21A601S — +1.8VS
C297 1UF_0402_X5R — C286 1UF_10V_0603_X5R — C341 10UF_10V_1206

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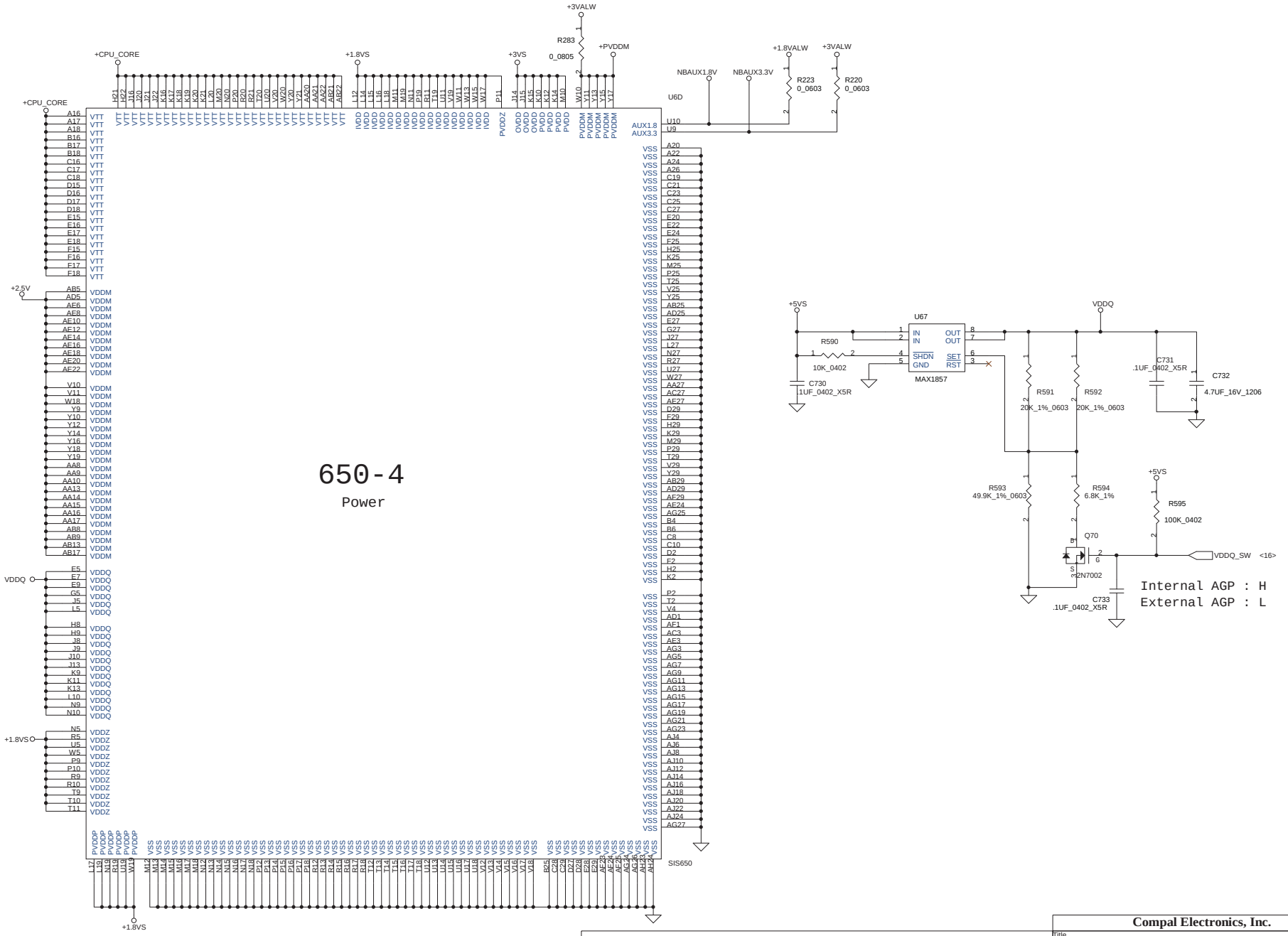

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Title	SiS 645/650	
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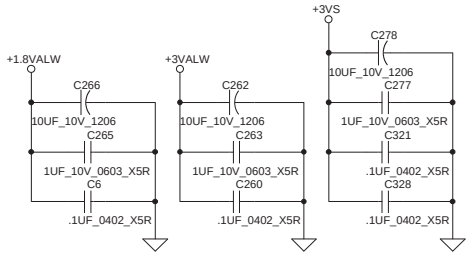
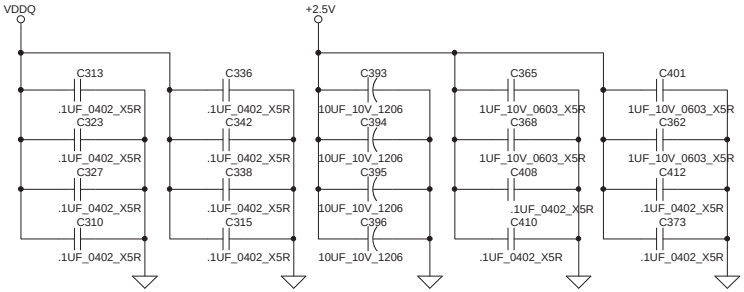
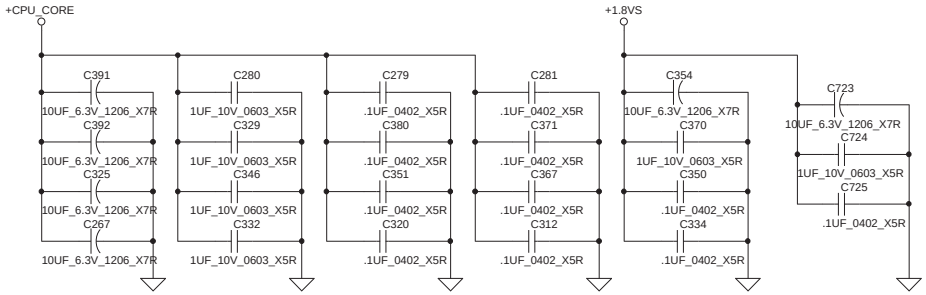
Layout note : Processor system bus

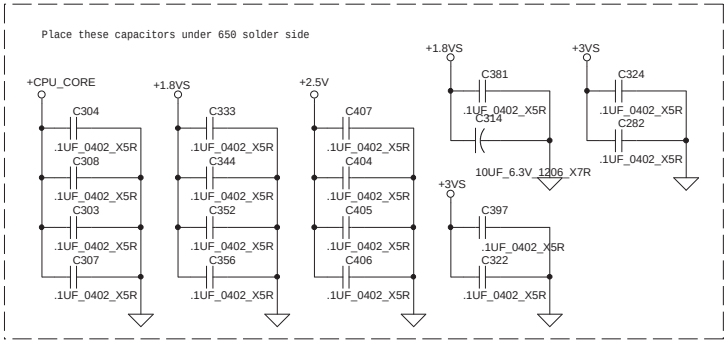
Distribute as close as possible
to Processor Quadrant.(between VTTFSB and VSS pin)

CHECK SiS 650 CAP.
IT NEED HOW MANY ESR









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Title	SiS 645/650 Decoupling	
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DDR SWAP NOW, SO DATA NOT CORRECT

Layout note

Place these resistor closely DIMM0, all trace length<750mil

RP5 4P2R_10: DDR_SDQ1 / DDR_SDQ5 — DDR_DQ1 / DDR_DQ5
RP30 4P2R_10: DDR_SDQ2 / DDR_SDQ7 — DDR_DQ2 / DDR_DQ7
RP6 4P2R_10: DDR_DM0 / DDR_SDQS0 — DDR_F_DM0 / DDR_DQS0
RP31 4P2R_10: DDR_SDQ4 / DDR_SDQ3 — DDR_DQ4 / DDR_DQ3
RP7 4P2R_10: DDR_SDQ0 / DDR_SDQ6 — DDR_DQ0 / DDR_DQ6
RP32 4P2R_10: DDR_SDQ14 / DDR_SDQ11 — DDR_DQ14 / DDR_DQ11
RP8 4P2R_10: DDR_SDQ12 / DDR_SDQ15 — DDR_DQ12 / DDR_DQ15
RP33 4P2R_10: DDR_DM1 / DDR_SDQS1 — DDR_F_DM1 / DDR_DQS1
RP9 4P2R_10: DDR_SDQ9 / DDR_SDQ8 — DDR_DQ9 / DDR_DQ8
RP34 4P2R_10: DDR_SDQ10 / DDR_SDQ13 — DDR_DQ10 / DDR_DQ13
RP10 4P2R_10: DDR_SDQ20 / DDR_SDQ19 — DDR_DQ20 / DDR_DQ19
RP35 4P2R_10: DDR_SDQ17 / DDR_SDQ16 — DDR_DQ17 / DDR_DQ16
RP11 4P2R_10: DDR_SDQS2 / DDR_DM2 — DDR_DQS2 / DDR_F_DM2
RP36 4P2R_10: DDR_SDQ18 / DDR_SDQ21 — DDR_DQ18 / DDR_DQ21
RP12 4P2R_10: DDR_SDQ23 / DDR_SDQ22 — DDR_DQ23 / DDR_DQ22
RP37 4P2R_10: DDR_SDQ31 / DDR_SDQ25 — DDR_DQ31 / DDR_DQ25
RP13 4P2R_10: DDR_SDQ28 / DDR_SDQ29 — DDR_DQ28 / DDR_DQ29
RP38 4P2R_10: DDR_SDQS3 / DDR_DM3 — DDR_DQS3 / DDR_F_DM3
RP14 4P2R_10: DDR_SDQ26 / DDR_SDQ24 — DDR_DQ26 / DDR_DQ24
RP39 4P2R_10: DDR_SDQ30 / DDR_SDQ27 — DDR_DQ30 / DDR_DQ27

RP43 4P2R_10: DDR_SDQ36 / DDR_SDQ38 — DDR_DQ36 / DDR_DQ38
RP20 4P2R_10: DDR_SDQ37 / DDR_SDQ32 — DDR_DQ37 / DDR_DQ32
RP44 4P2R_10: DDR_SDQS4 / DDR_DM4 — DDR_DQS4 / DDR_F_DM4
RP21 4P2R_10: DDR_SDQ39 / DDR_SDQ33 — DDR_DQ39 / DDR_DQ33
RP45 4P2R_10: DDR_SDQ34 / DDR_SDQ35 — DDR_DQ34 / DDR_DQ35
RP22 4P2R_10: DDR_SDQ43 / DDR_SDQ44 — DDR_DQ43 / DDR_DQ44
RP46 4P2R_10: DDR_SDQ41 / DDR_SDQ45 — DDR_DQ41 / DDR_DQ45
RP23 4P2R_10: DDR_DM5 / DDR_SDQS5 — DDR_F_DM5 / DDR_DQS5
RP47 4P2R_10: DDR_SDQ40 / DDR_SDQ42 — DDR_DQ40 / DDR_DQ42
RP24 4P2R_10: DDR_SDQ47 / DDR_SDQ46 — DDR_DQ47 / DDR_DQ46
RP48 4P2R_10: DDR_SDQ49 / DDR_SDQ48 — DDR_DQ49 / DDR_DQ48
RP25 4P2R_10: DDR_SDQ53 / DDR_SDQ50 — DDR_DQ53 / DDR_DQ50
RP49 4P2R_10: DDR_SDQS6 / DDR_DM6 — DDR_DQS6 / DDR_F_DM6
RP26 4P2R_10: DDR_SDQ51 / DDR_SDQ52 — DDR_DQ51 / DDR_DQ52
RP50 4P2R_10: DDR_SDQ55 / DDR_SDQ54 — DDR_DQ55 / DDR_DQ54
RP27 4P2R_10: DDR_SDQ58 / DDR_SDQ60 — DDR_DQ58 / DDR_DQ60
RP51 4P2R_10: DDR_SDQ57 / DDR_SDQ56 — DDR_DQ57 / DDR_DQ56
RP28 4P2R_10: DDR_DM7 / DDR_SDQS7 — DDR_F_DM7 / DDR_DQS7
RP52 4P2R_10: DDR_SDQ62 / DDR_SDQ61 — DDR_DQ62 / DDR_DQ61
RP71 4P2R_10: DDR_SDQ63 / DDR_SDQ59 — DDR_DQ63 / DDR_DQ59

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

<8> DDR_SDQ[0..63] → DDR_SDQ[0..63]
<8> DDR_DM[0..7] → DDR_DM[0..7]
<8> DDR_SDQS[0..7] → DDR_SDQS[0..7]

JP2 — MOLEX 67589-2003 200P STD

VREF	1	2	VREF
VSS	3	4	VSS
DDR_DQ1 DQ0	5	6	DQ4 DDR_DQ5
DDR_DQ2 DQ1	7	8	DQ5 DDR_DQ7
VDD	9	10	VDD
DDR_DQS0 DQS0	11	12	DM0 DDR_F_DM0
DDR_DQ4 DQ2	13	14	DQ6 DDR_DQ3
VSS	15	16	VSS
DDR_DQ0 DQ3	17	18	DQ7 DDR_DQ6
DDR_DQ14 DQ8	19	20	DQ12 DDR_DQ11
VDD	21	22	VDD
DDR_DQ12 DQ9	23	24	DQ13 DDR_DQ15
DDR_DQS1 DQS1	25	26	DM1 DDR_F_DM1
VSS	27	28	VSS
DDR_DQ9 DQ10	29	30	DQ14 DDR_DQ8
DDR_DQ10 DQ11	31	32	DQ15 DDR_DQ13
<15> DDR_CLK1 VDD	33	34	VDD
<15> DDR_CLK1# CK0	35	36	VDD
CK0#	37	38	VSS
VSS	39	40	VSS
DDR_DQ20 DQ16	41	42	DQ20 DDR_DQ19
DDR_DQ17 DQ17	43	44	DQ21 DDR_DQ16
VDD	45	46	VDD
DDR_DQS2 DQS2	47	48	DM2 DDR_F_DM2
DDR_DQ18 DQ18	49	50	DQ22 DDR_DQ21
VSS	51	52	VSS
DDR_DQ23 DQ19	53	54	DQ23 DDR_DQ22
DDR_DQ31 DQ24	55	56	DQ28 DDR_DQ25
VDD	57	58	VDD
DDR_DQ28 DQ25	59	60	DQ29 DDR_DQ29
DDR_DQS3 DQS3	61	62	DM3 DDR_F_DM3
VSS	63	64	VSS
DDR_DQ26 DQ26	65	66	DQ30 DDR_DQ24
DDR_DQ30 DQ27	67	68	DQ31 DDR_DQ27
VDD	69	70	VDD
CB0	71	72	CB4
CB1	73	74	CB5
VSS	75	76	VSS
DQS8	77	78	DM8
CB2	79	80	CB6
VDD	81	82	VDD
CB3	83	84	CB7
DU	85	86	DU/RESET#
VSS	87	88	VSS
<15> DDR_CLK0 CK2	89	90	VSS
<15> DDR_CLK0# CK2#	91	92	VDD
<8> DDR_CKE1 VDD	93	94	VDD
CKE1	95	96	CKE0 DDR_CKE0 <8>
DDR_SMA12 DU/A13	97	98	DU/BA2
DDR_SMA9 A12	99	100	A11 DDR_SMA11
A9	101	102	A8 DDR_SMA8
DDR_SMA7 VSS	103	104	VSS
DDR_SMA5 A7	105	106	A6 DDR_SMA6
DDR_SMA3 A5	107	108	A4 DDR_SMA4
DDR_SMA1 A3	109	110	A2 DDR_SMA2
A1	111	112	A0 DDR_SMA0
DDR_SMA10 VDD	113	114	VDD
DDR_F_SBS0 A10/AP	115	116	BA1 DDR_F_SBS1
<8,13> DDR_SWE# BA0	117	118	RAS# DDR_SRAS# <8,13>
<8,13> DDR_SCS#0 WE#	119	120	CAS# DDR_SCAS# <8,13>
S0#	121	122	S1# DDR_SCS#1 <8>
DU	123	124	DU
VSS	125	126	VSS
DDR_DQ36 DQ32	127	128	DQ36 DDR_DQ38
DDR_DQ37 DQ33	129	130	DQ37 DDR_DQ32
VDD	131	132	VDD
DDR_DQS4 DQS4	133	134	DM4 DDR_F_DM4
DDR_DQ39 DQ34	135	136	DQ38 DDR_DQ33
VSS	137	138	VSS
DDR_DQ34 DQ35	139	140	DQ39 DDR_DQ35
DDR_DQ43 DQ40	141	142	DQ44 DDR_DQ44
VDD	143	144	VDD
DDR_DQ41 DQ41	145	146	DQ45 DDR_DQ45
DDR_DQS5 DQS5	147	148	DM5 DDR_F_DM5
VSS	149	150	VSS
DDR_DQ40 DQ42	151	152	DQ46 DDR_DQ42
DDR_DQ47 DQ43	153	154	DQ47 DDR_DQ46
VDD	155	156	VDD
VDD	157	158	CK1# DDR_CLK2# <15>
VSS	159	160	CK1 DDR_CLK2 <15>
VSS	161	162	VSS
DDR_DQ49 DQ48	163	164	DQ52 DDR_DQ48
DDR_DQ53 DQ49	165	166	DQ53 DDR_DQ50 <13> DDR_F_SBS1
VDD	167	168	VDD
DDR_DQS6 DQS6	169	170	DM6 DDR_F_DM6
DDR_DQ51 DQ50	171	172	DQ54 DDR_DQ52
VSS	173	174	VSS
DDR_DQ55 DQ51	175	176	DQ55 DDR_DQ54 <13> DDR_F_SBS0
DDR_DQ58 DQ56	177	178	DQ60 DDR_DQ60
VDD	179	180	VDD
DDR_DQ57 DQ57	181	182	DQ61 DDR_DQ56
DDR_DQS7 DQS7	183	184	DM7 DDR_F_DM7
VSS	185	186	VSS
DDR_DQ62 DQ58	187	188	DQ62 DDR_DQ61
DDR_DQ63 DQ59	189	190	DQ63 DDR_DQ59
VDD	191	192	VDD
<13,15,18,20> SMB_DATA SDA	193	194	SA0
<13,15,18,20> SMB_CLK SCL	195	196	SA1
+3VS VDD_SPD	197	198	SA2
VDD_ID	199	200	DU

+2.5V → VREF
SDREF_R → L54 MurataBLM21A601S → SDREF
C451 .1UF_16V_0402_Y5V

DDR_DQ[0..63] <13>
DDR_F_DM[0..7] <13>
DDR_DQS[0..7] <13>
DDR_SMA[0..12] <8,13>

Layout note
Place these resistor closely DIMM0, all trace length Max=1.3"

+2.5V
RP58 4P2R_470: DDR_CKE0, DDR_CKE1
+1.25VS
R132 33_0402: DDR_SCS#1
PULL_UP AT PAGE 13

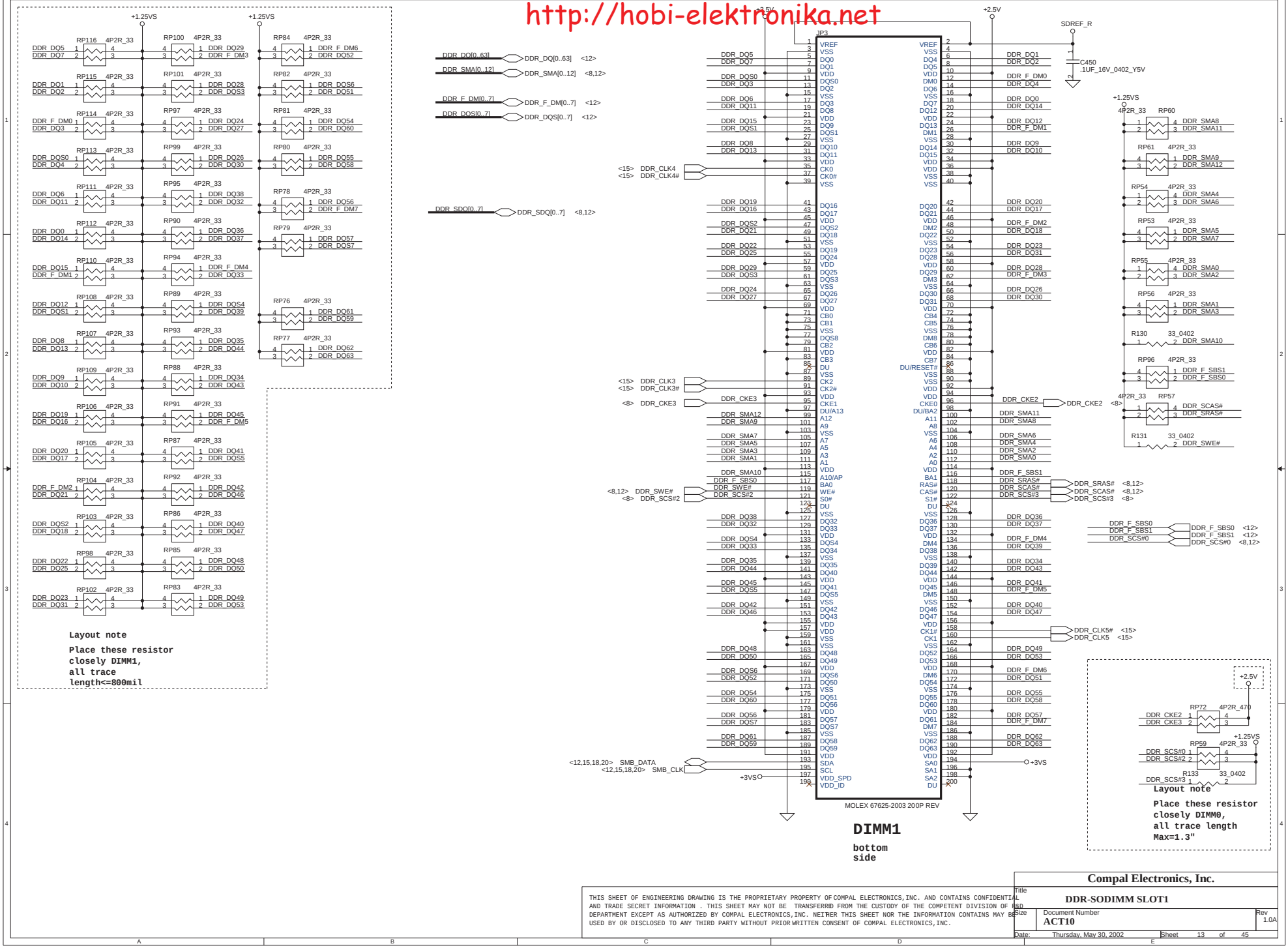
4P2R_10 RP19: DDR_F_SBS1 → DDR_SBS1 <8>, DDR_SBS0 <8>; DDR_F_SBS0

DIMM0

top side

Compal Electronics, Inc.

Title: DDR-SODIMM SLOT1
Size: Document Number: ACT10 Rev: 1.0A
Date: Thursday, May 30, 2002 Sheet 12 of 45

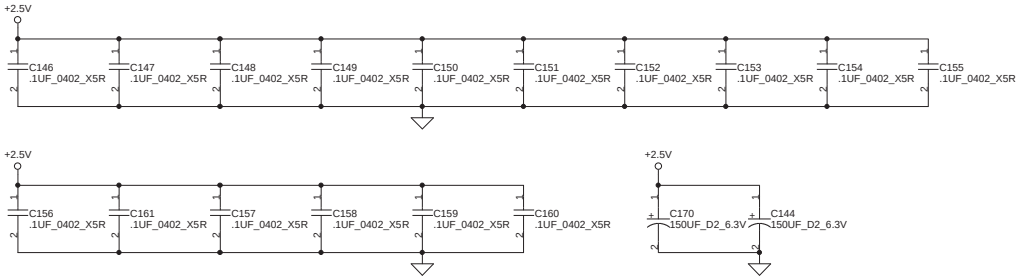


Compal Electronics, Inc.

Title	DDR-SODIMM SLOT1	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 13 of 45	

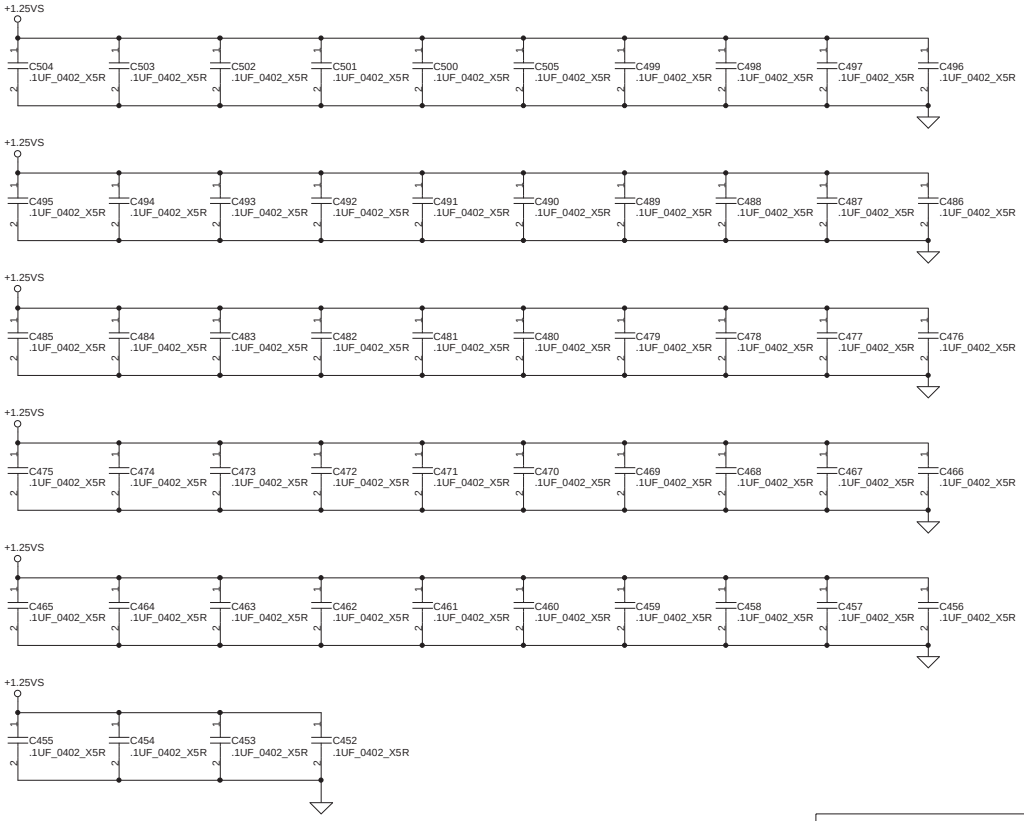
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



Compal Electronics, Inc.

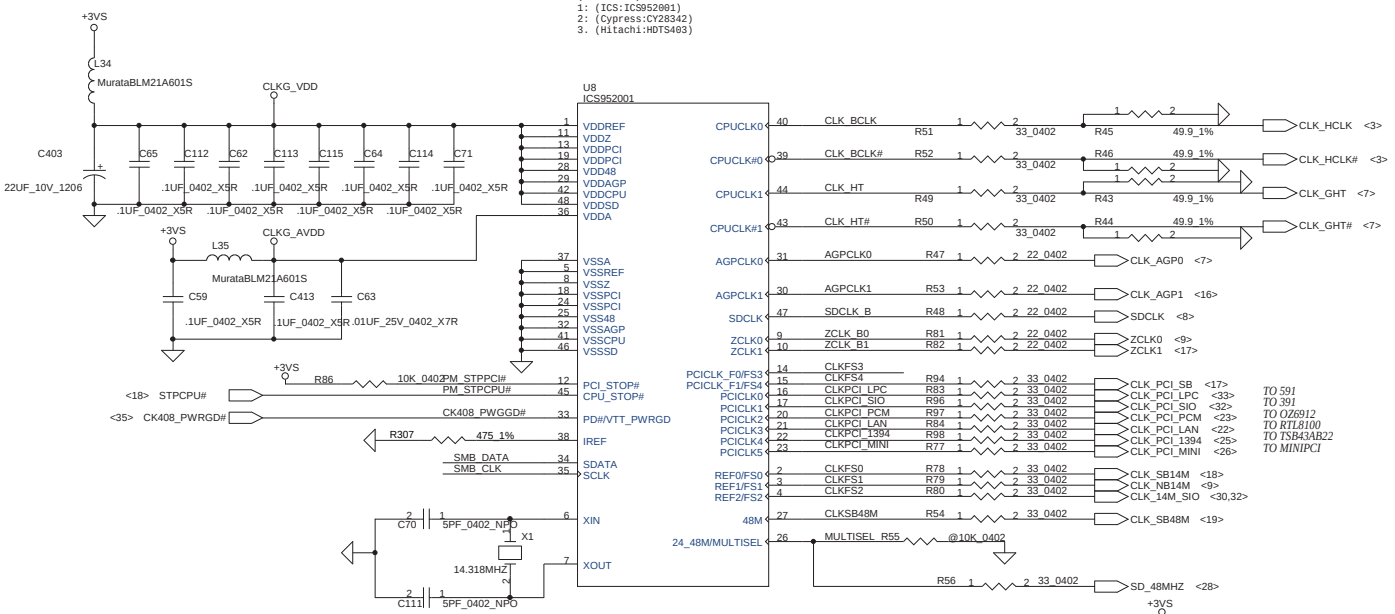
Title: **DDR SODIMM Decoupling**

Size: | Document Number: **ACT10** | Rev: 1.0A

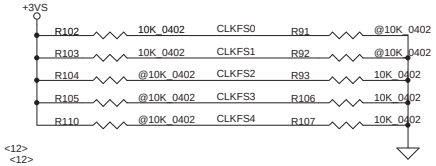
Date: Thursday, May 30, 2002 | Sheet 14 of 45

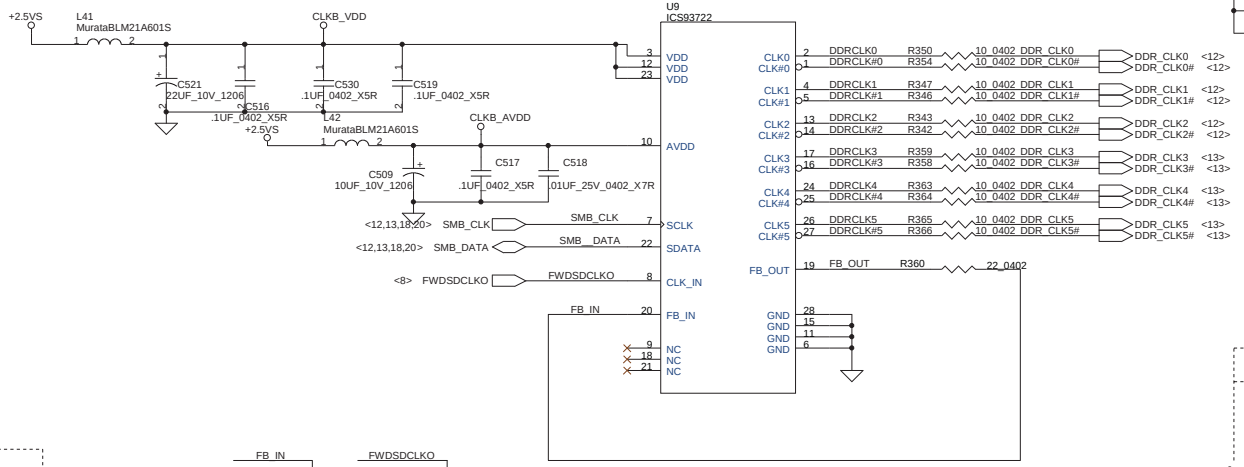
Main Clock Generator

(3 OPTIONS)
1: (ICS:ICS952001)
2: (Cypress:CY28342)
3. (Hitachi:HDTS403)

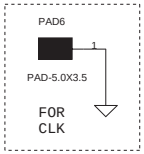


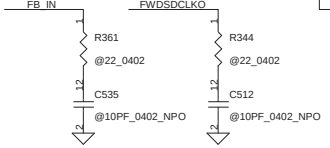
ICS suggestion 14.318MHz > 36pF, C273, C274 4pF





FS4	FS3	FS2	FS1	FS0	CPU	DDR	ZCLK	AGP	PCI
1	1	0	0	0	100.0	133.0	80.0	66.7	33.3
1	1	0	0	1	100.0	100.0	80.0	66.7	33.3
0	0	1	1	1	100.0	133.3	80.0	66.7	33.3
* 0	0	0	1	1	100.0	133.3	66.7	66.7	33.3





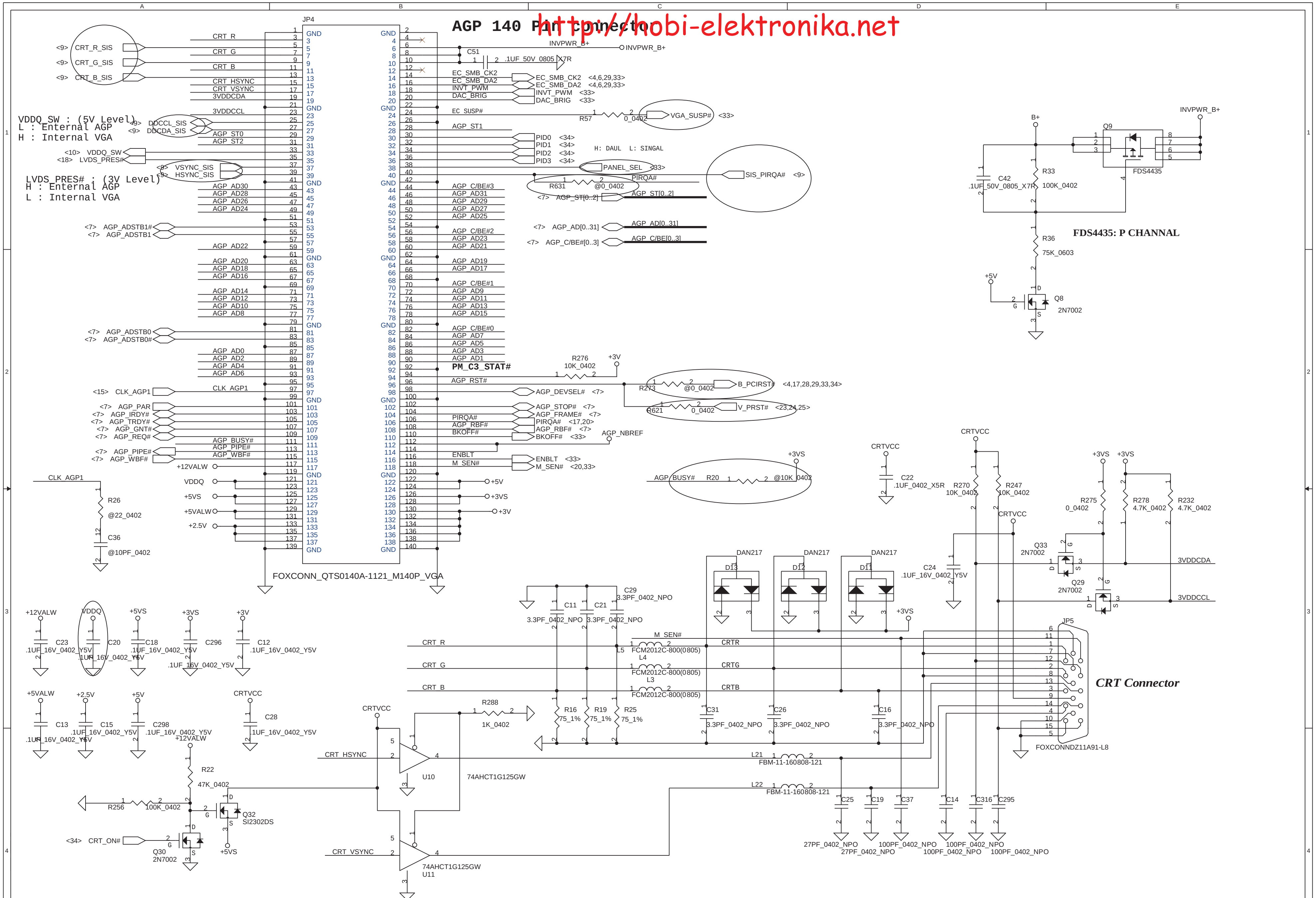
Compal Electronics, Inc.

Title: Clock Generator

Size: | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 15 of 45

AGP 140 Pin connector



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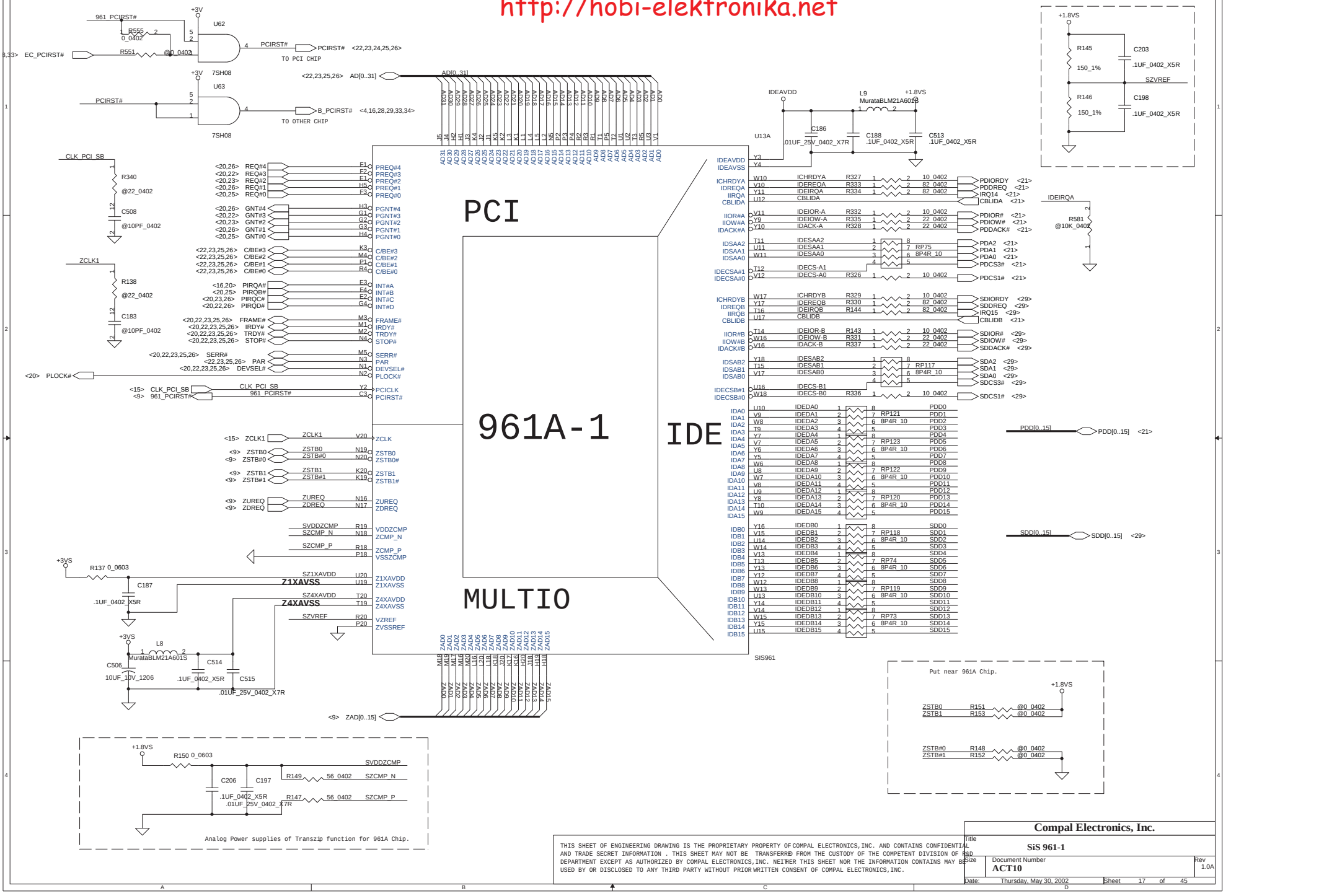
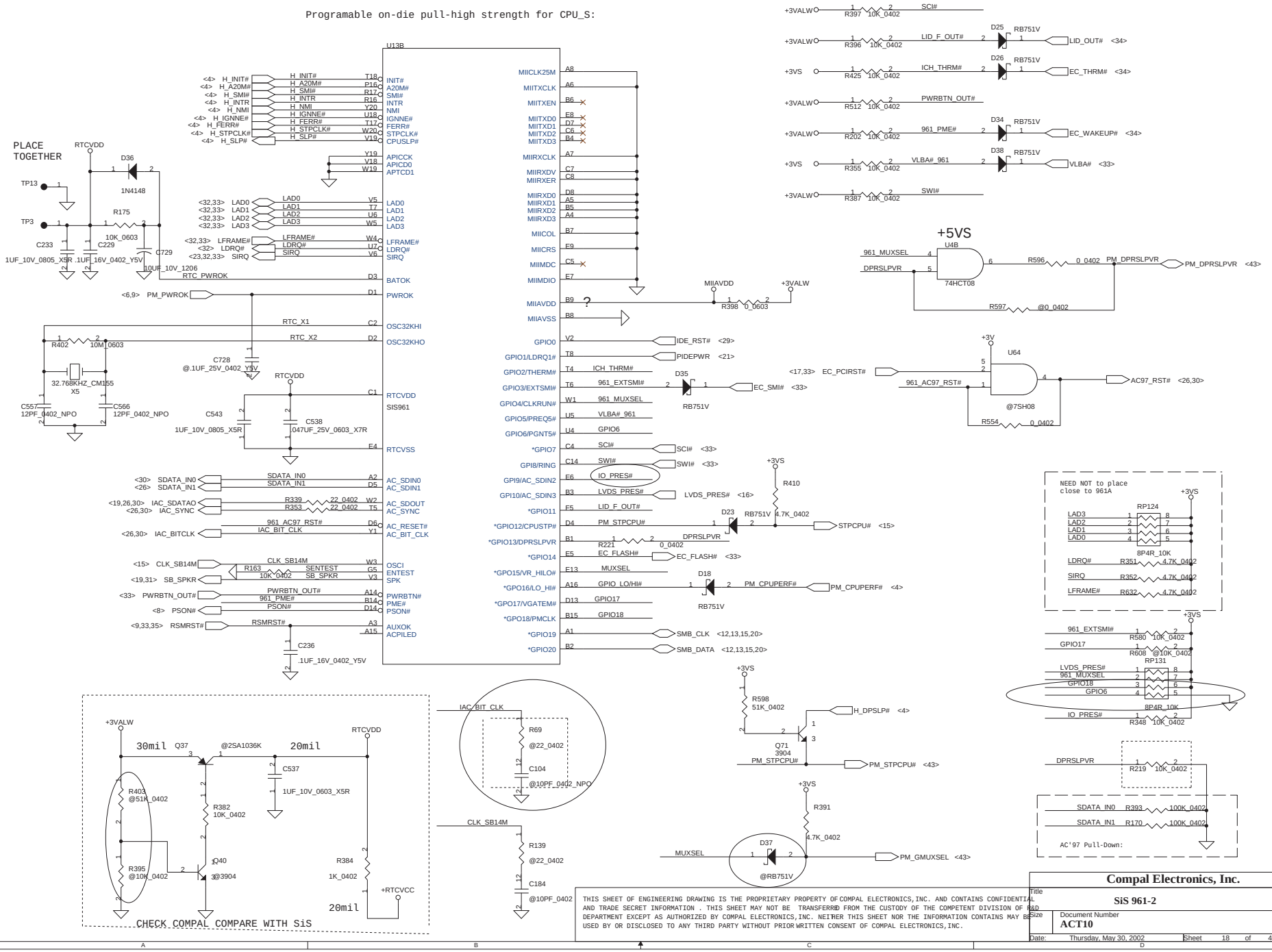
Compal Electronics, Inc.	
Title	AGPConn. & CRT
Size / Document Number	ACT10
Rev	1.0A
Date:	Thursday, May 30, 2002
Sheet	16 of 45



Compal Electronics, Inc.

Title	SiS 961-1		
Size	Document Number ACT10		Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 17	of	45



Compal Electronics, Inc.

Title	SiS 961-2	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 18 of 45	

FOR 961 USB PIN DEFINITION

Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
Control 0 : port 1 UV1+ E14 UV1- D15 OC1# J16
Control 0 : port 2 UV2+ E16 UV2- E15 OC2# H17
HW TRIP PULL LOW 1K SOUTH BIRDGE DEBUG MODE

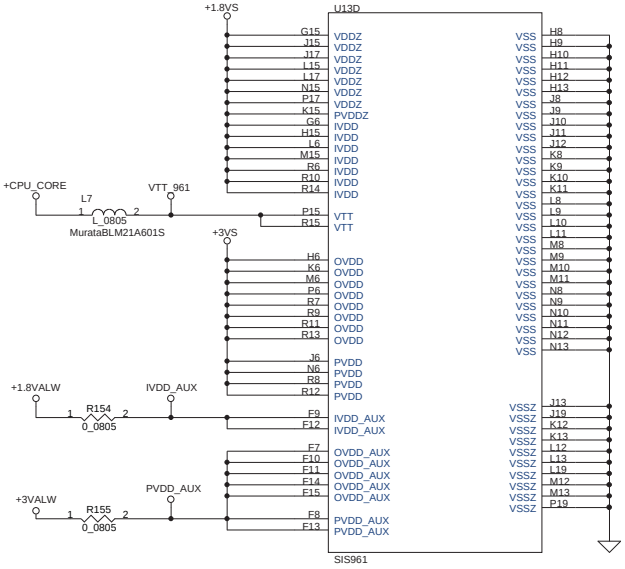
Control 1 : port 3 UV3+ D18 UV3- D19 OC3# G17
Control 1 : port 4 UV4+ E18 UV4- F18 OC4# H16
Control 1 : port 5 UV5+ G18 UV5- G19 OC5# G16
HW TRIP PULL LOW 1K TRIP FROM PCI AD0..31
PULL HIGH TRIP FROM FLASH ROM

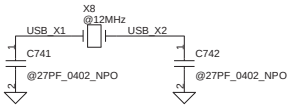
FOR 962 USB PIN DEFINITION

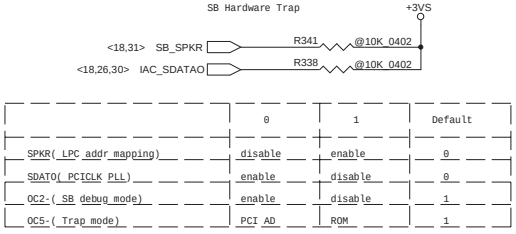
Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
Control 0 : port 3 UV3+ E18 UV3- F18 OC3# H16

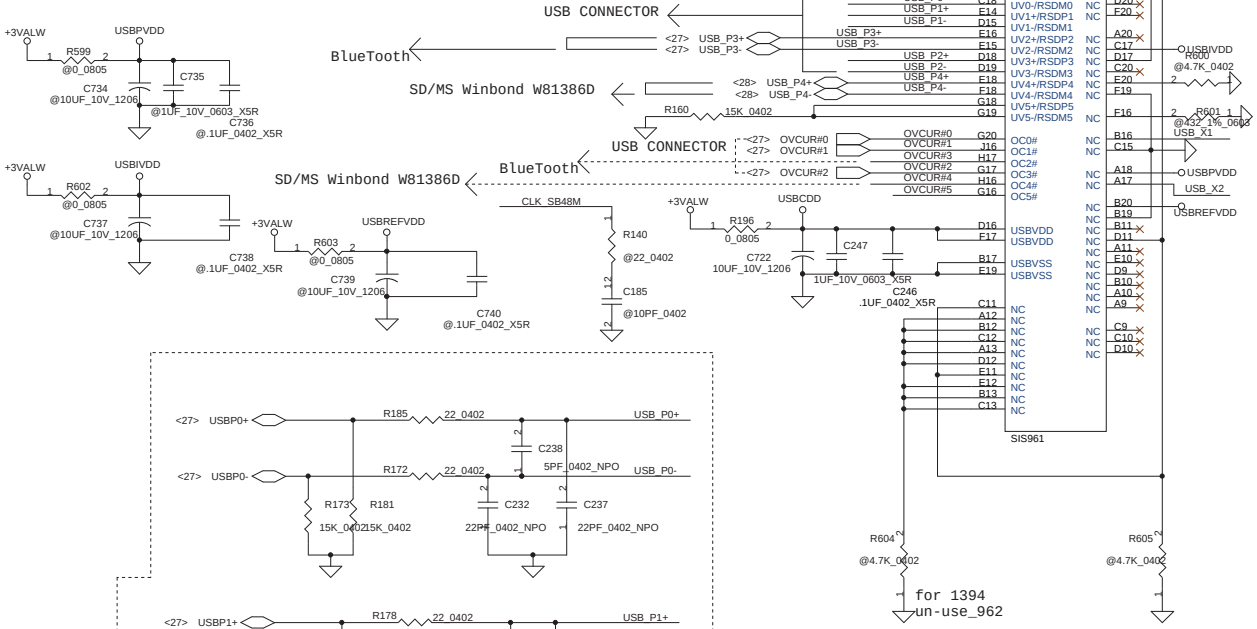
Control 1 : port 1 UV1+ D18 UV1- D19 OC1# G17
Control 1 : port 4 UV4+ E16 UV4- E15 OC4# H17

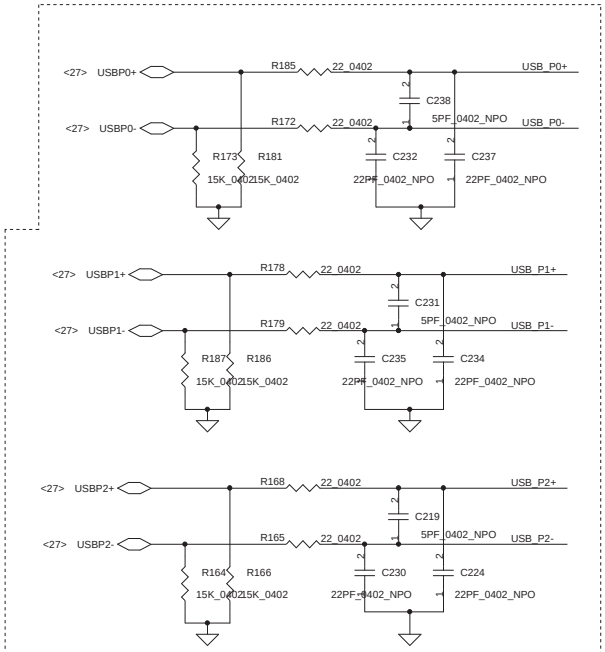
Control 2 : port 2 UV2+ E14 UV2- D15 OC2# J16
Control 2 : port 5 UV5+ G18 UV5- G19 OC5# G16

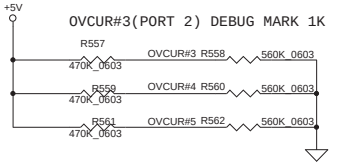








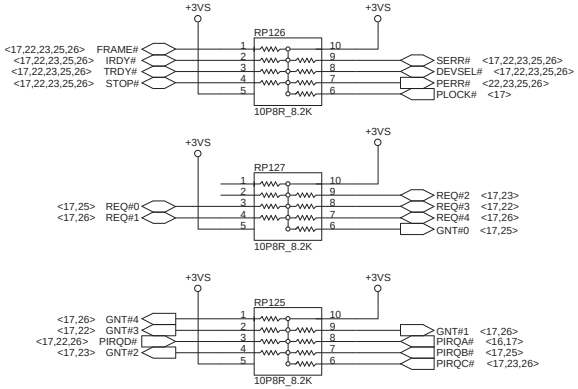


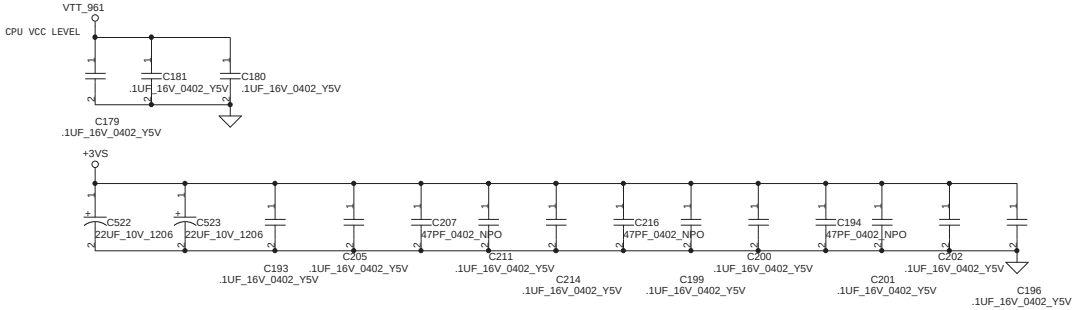


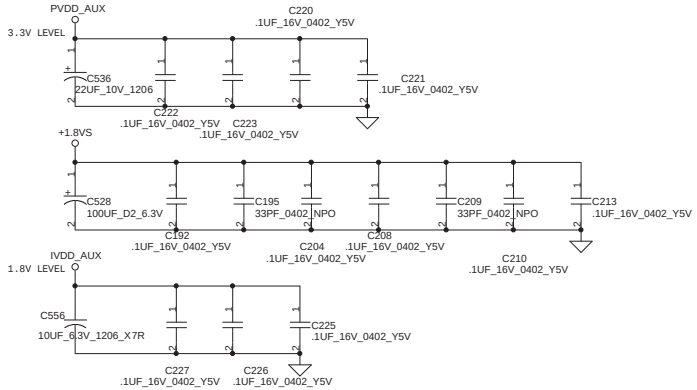
OVCUR#5 : PULL UP TRAP FROM SYSTEM FLASH ROM
PULL DOWN 1K TRAP FROM PCI AD31..0

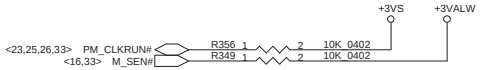
Compal Electronics, Inc.

Title: SiS 961(3) USB
Size: Document Number: ACT10 Rev: 1.0A
Date: Thursday, May 30, 2002 Sheet 19 of 45









Compal Electronics, Inc.

Title: SiS961 Decoupling & Pull-Up

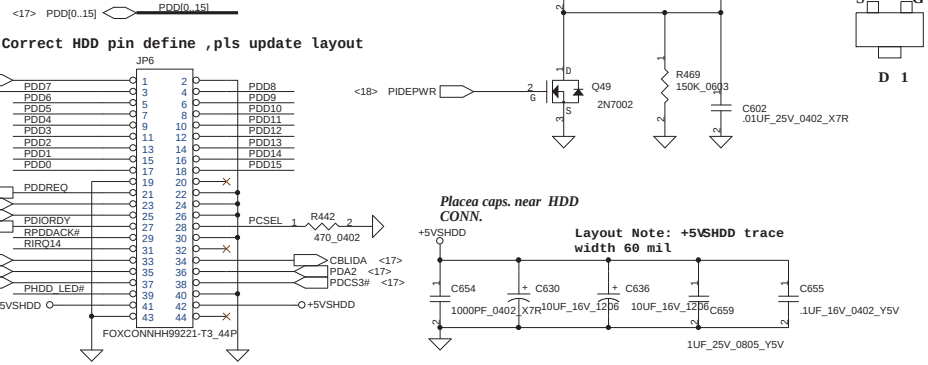
Size: | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 20 of 45

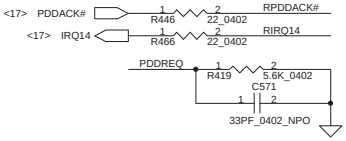
SI2301DS: 1 CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

S 3 2 G
D 1

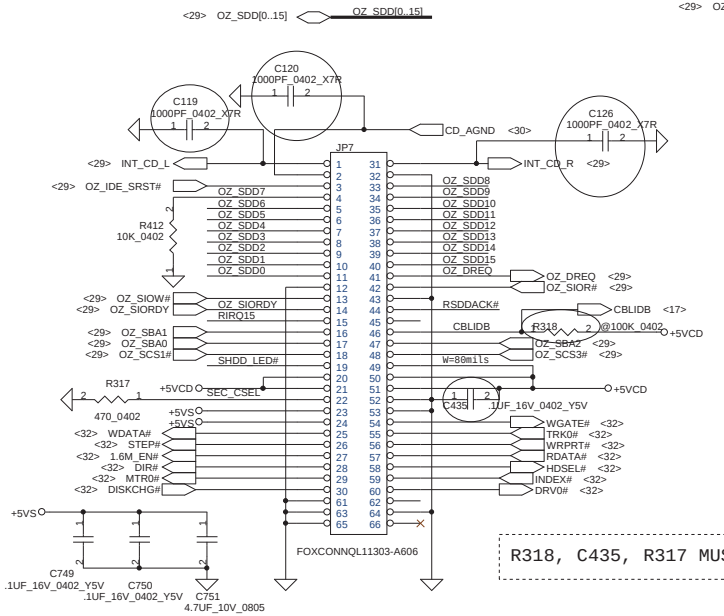
HDD Connector

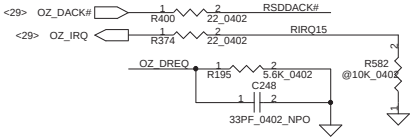


Placea caps. near HDD CONN.

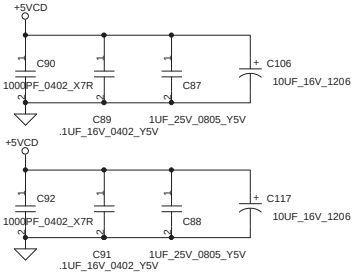


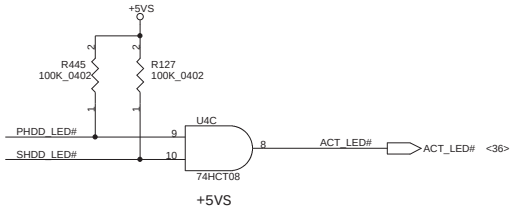
CD-ROM Connector





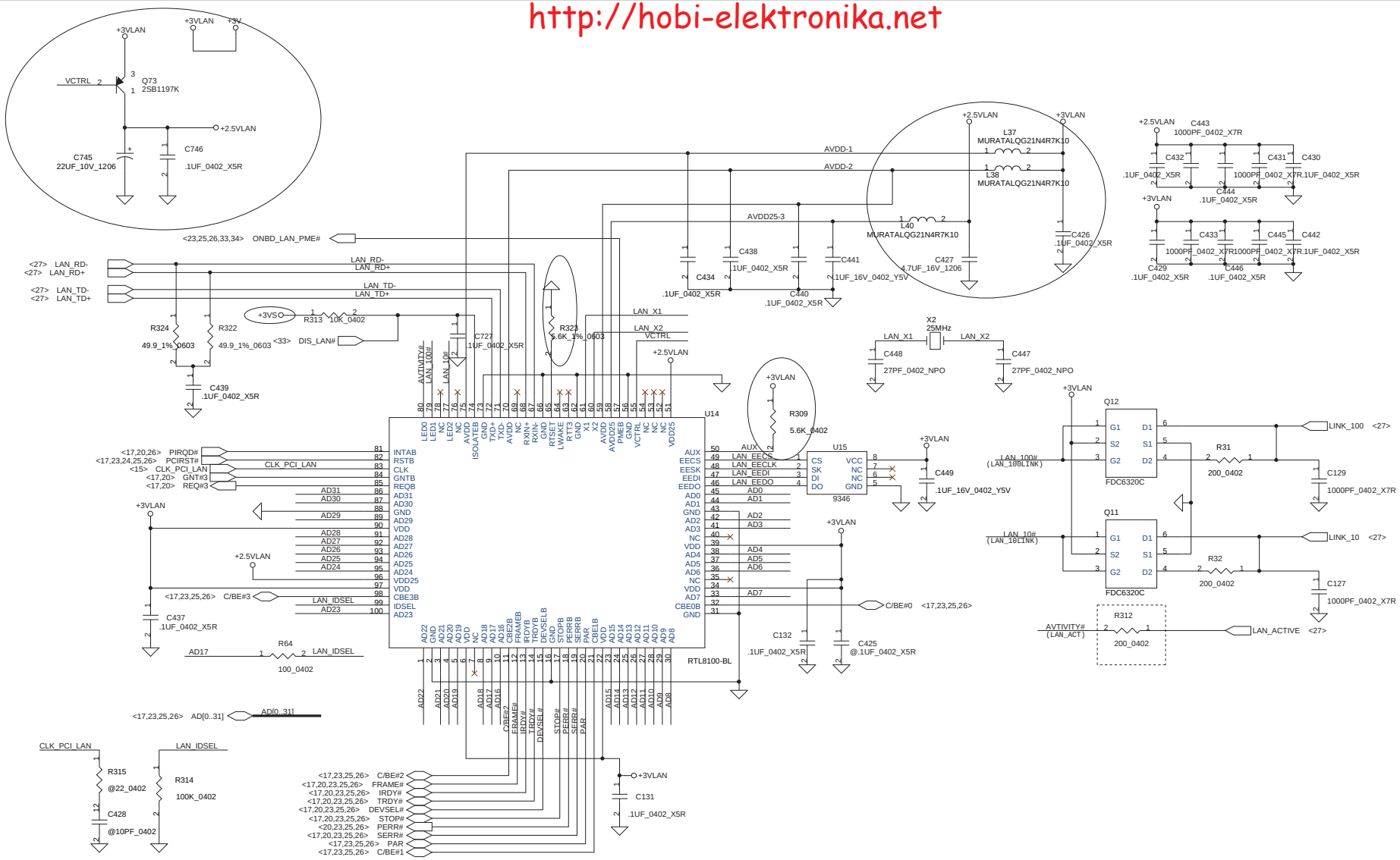
Placea caps. near CDROM CONN.





R318, C435, R317 MUST MOVE

Compal Electronics, Inc.	
Title	IDE/CD-ROM Module
Size	Document Number: ACT10 — Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 21 of 45



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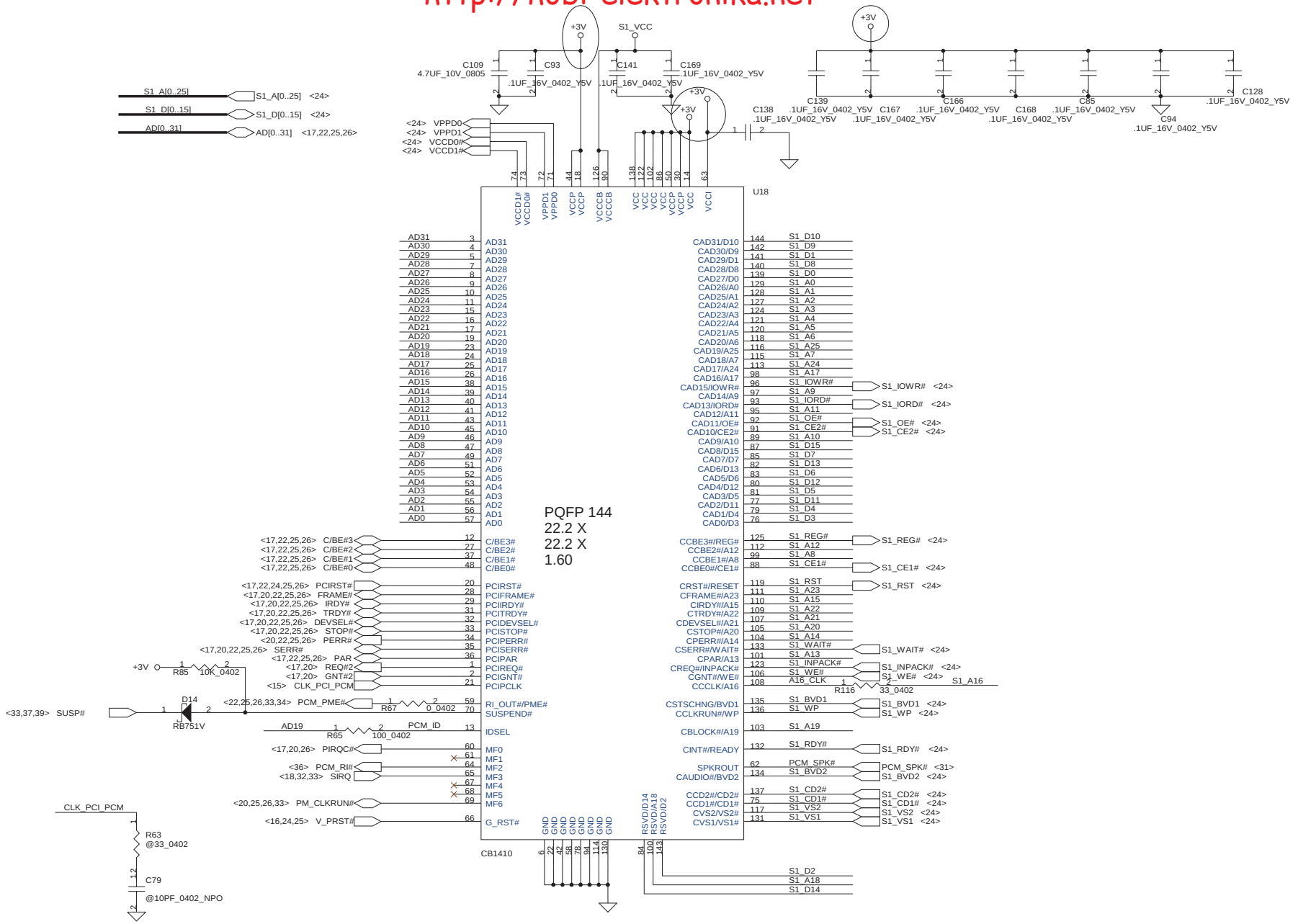
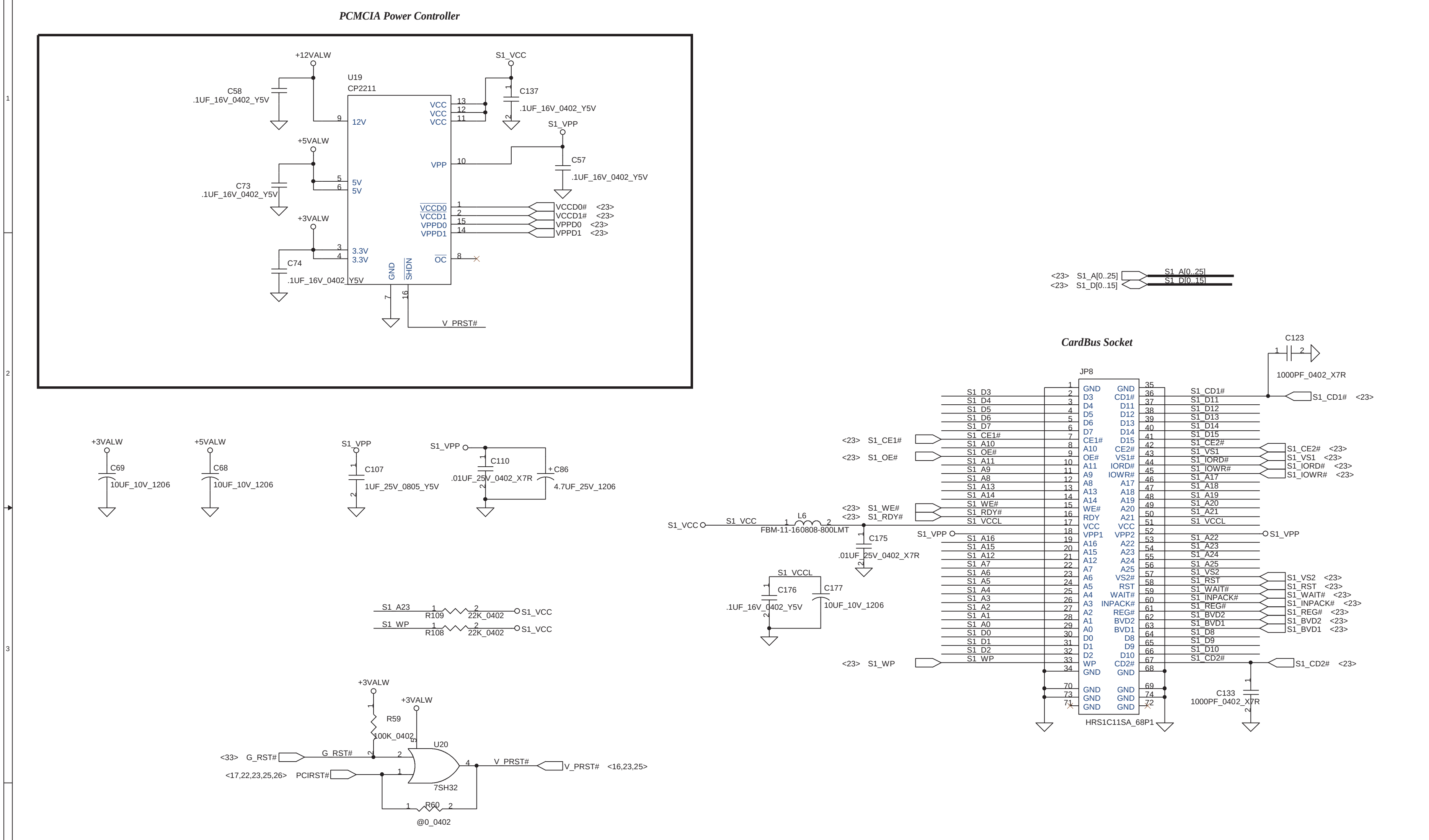
Compal Electronics, Inc.

Title	Realtek RTL8100BL	
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 22 of 45	



Compal Electronics, Ltd.

Title	PCMCIA controller ENE CB1410		
Size	Document Number ACT10		Rev 1.0A
Date:	Thursday, May 30, 2002	Sheet 23 of 45	



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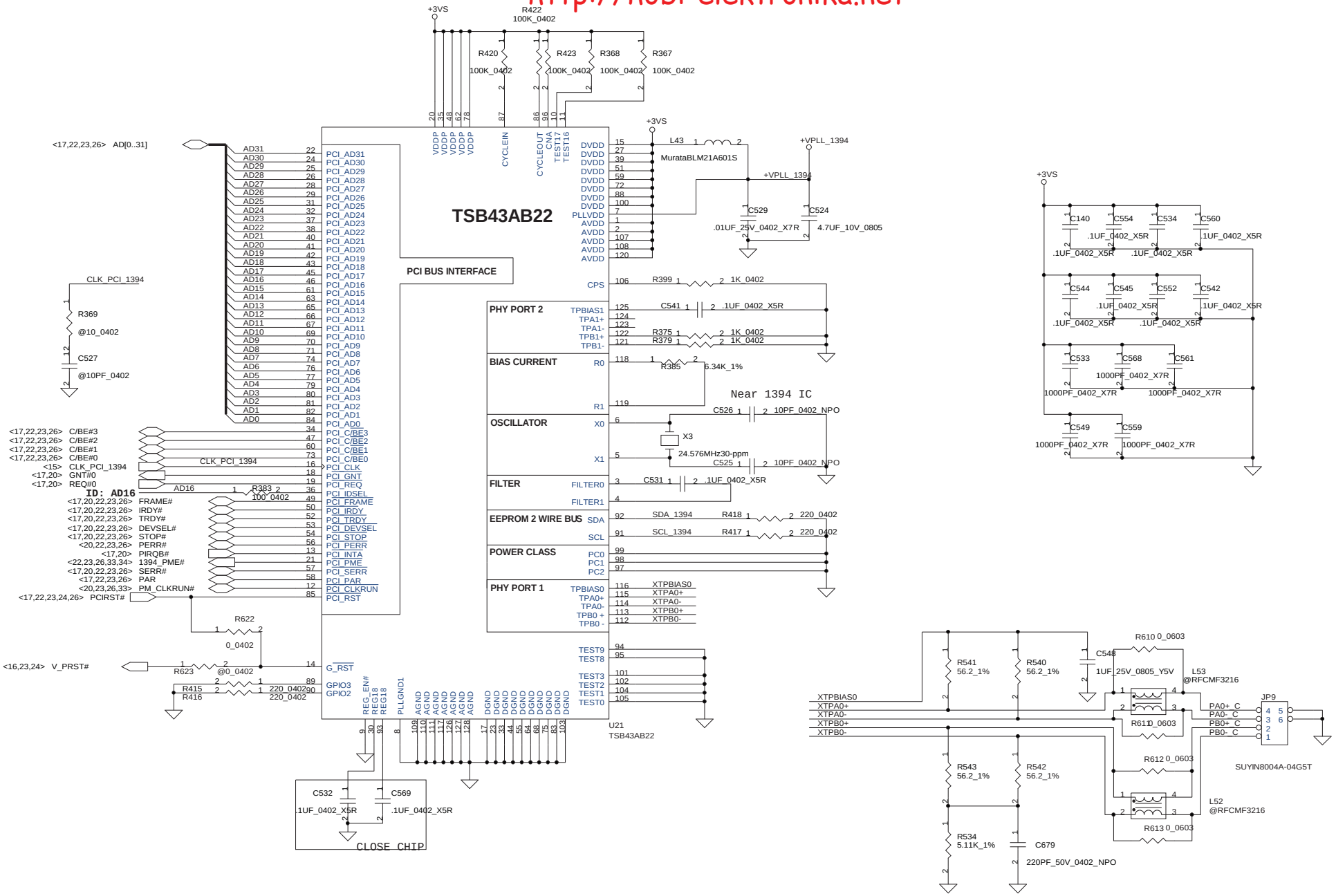
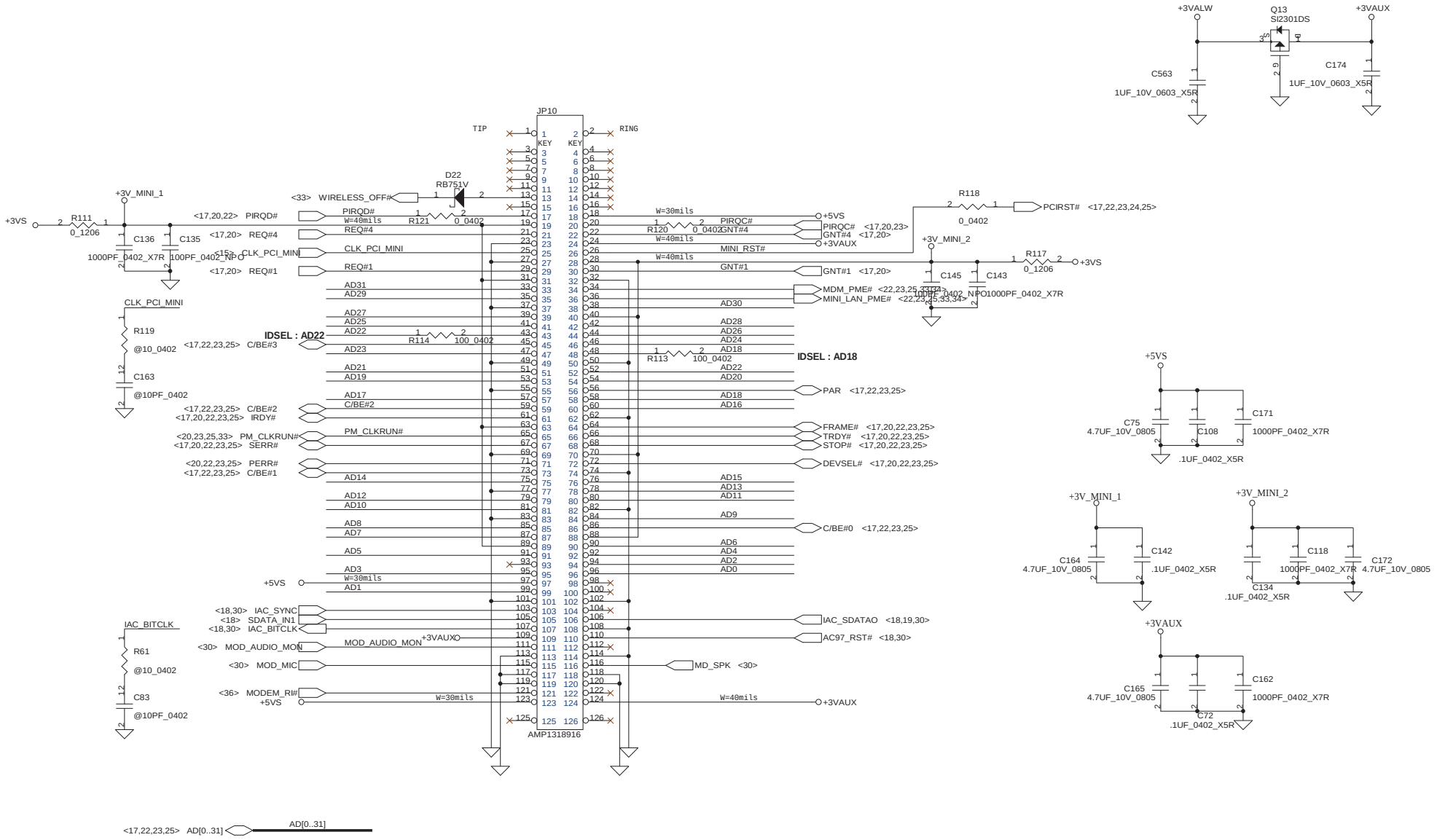
Compal Electronics, Inc.	
Title	CardBus Socket
Size / Document Number	ACT10
Rev	1.0A
Date:	Thursday, May 30, 2002
Sheet	24 of 45

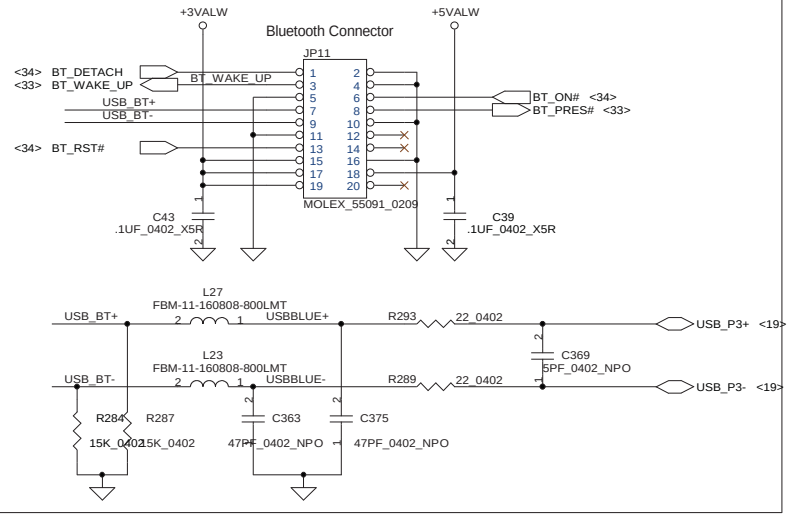


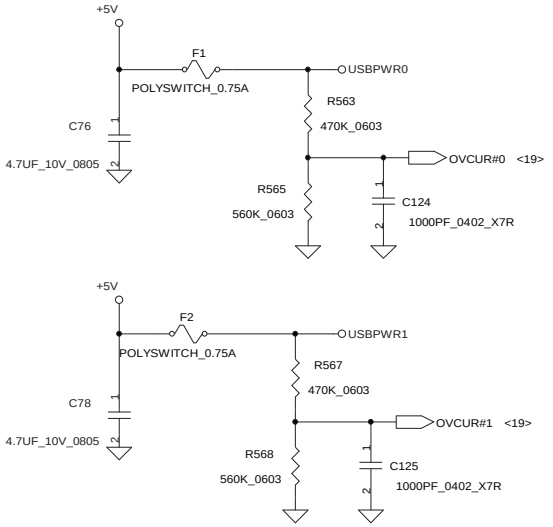


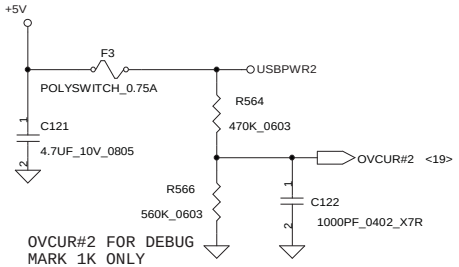
Compal Electronics, Ltd.

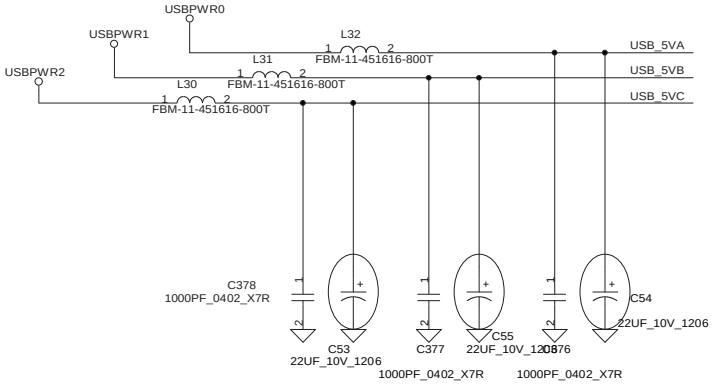
Title	Mini PCI Slot	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 26 of 45	

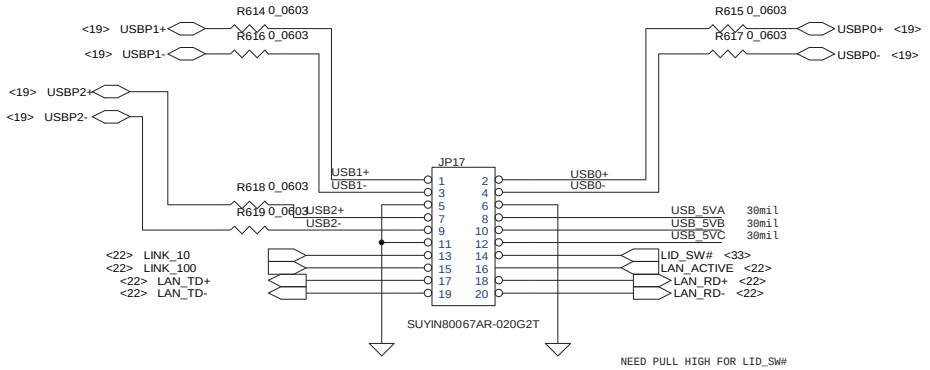
BlueTooth Interface





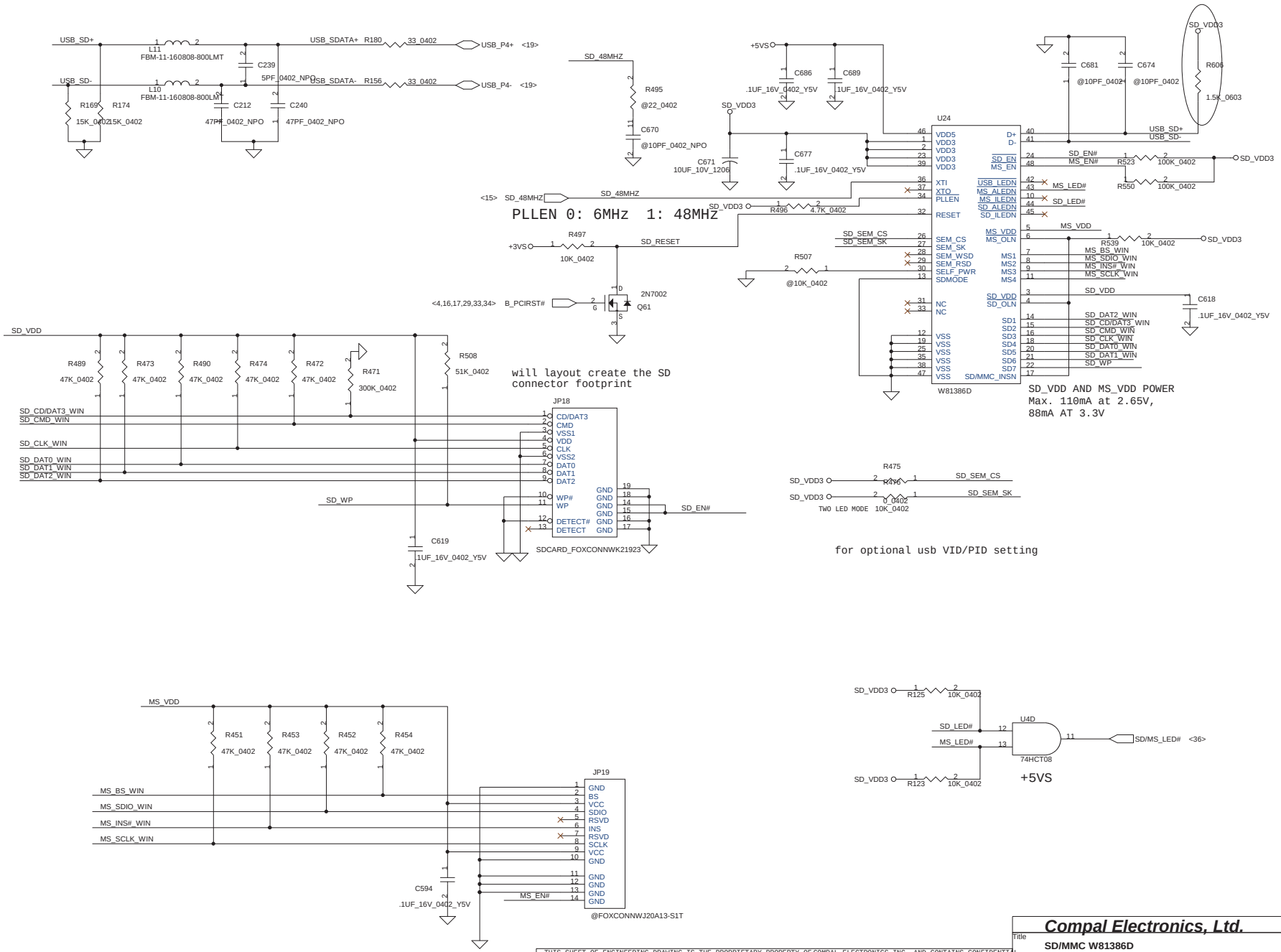






Compal Electronics, Ltd.

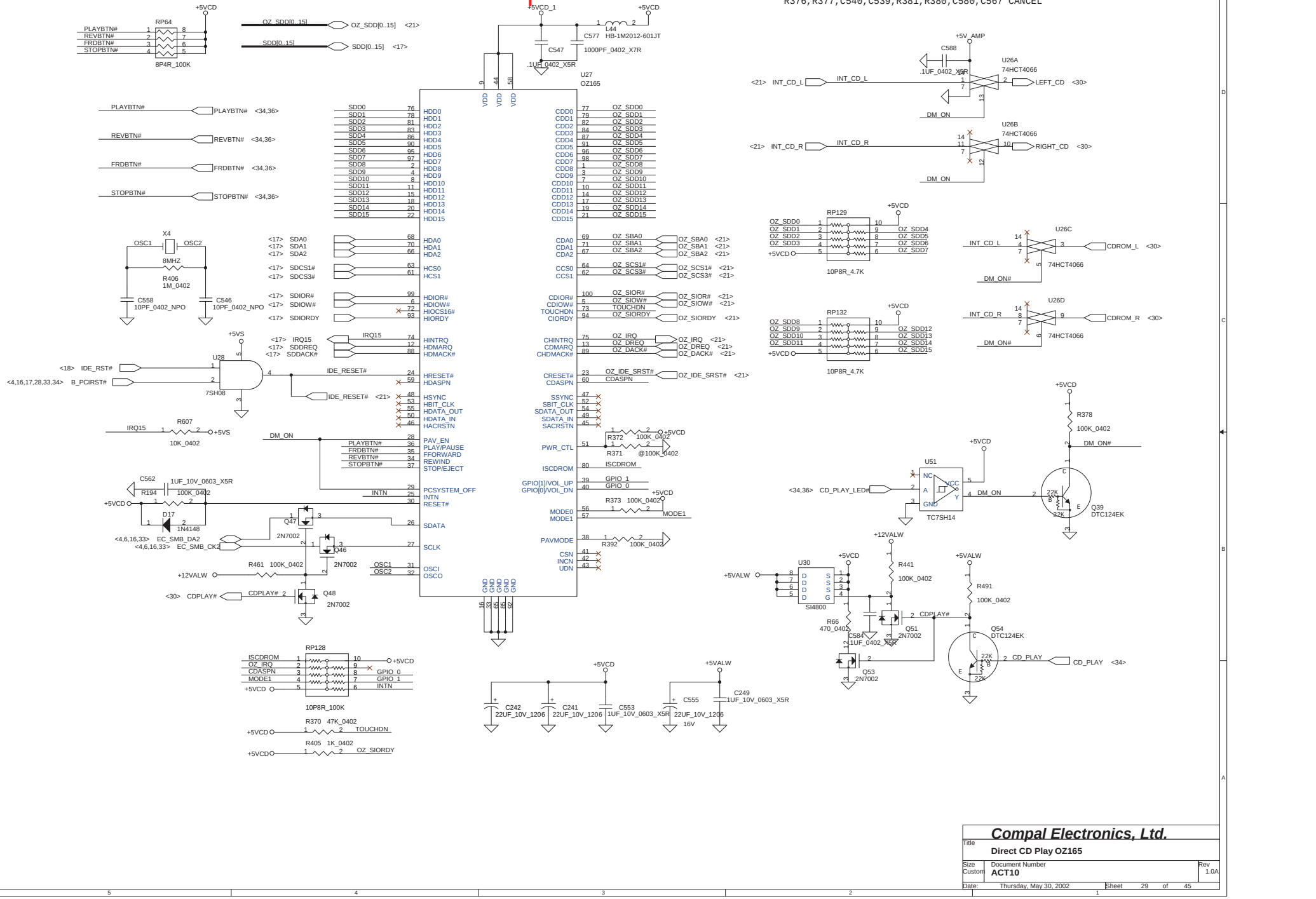
Title	USB & BlueTooth Connector	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 27 of 45	



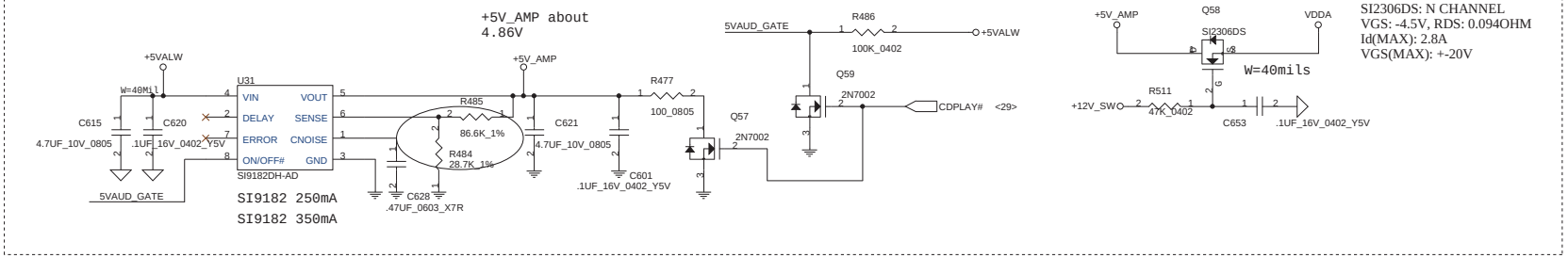
Compal Electronics, Ltd.

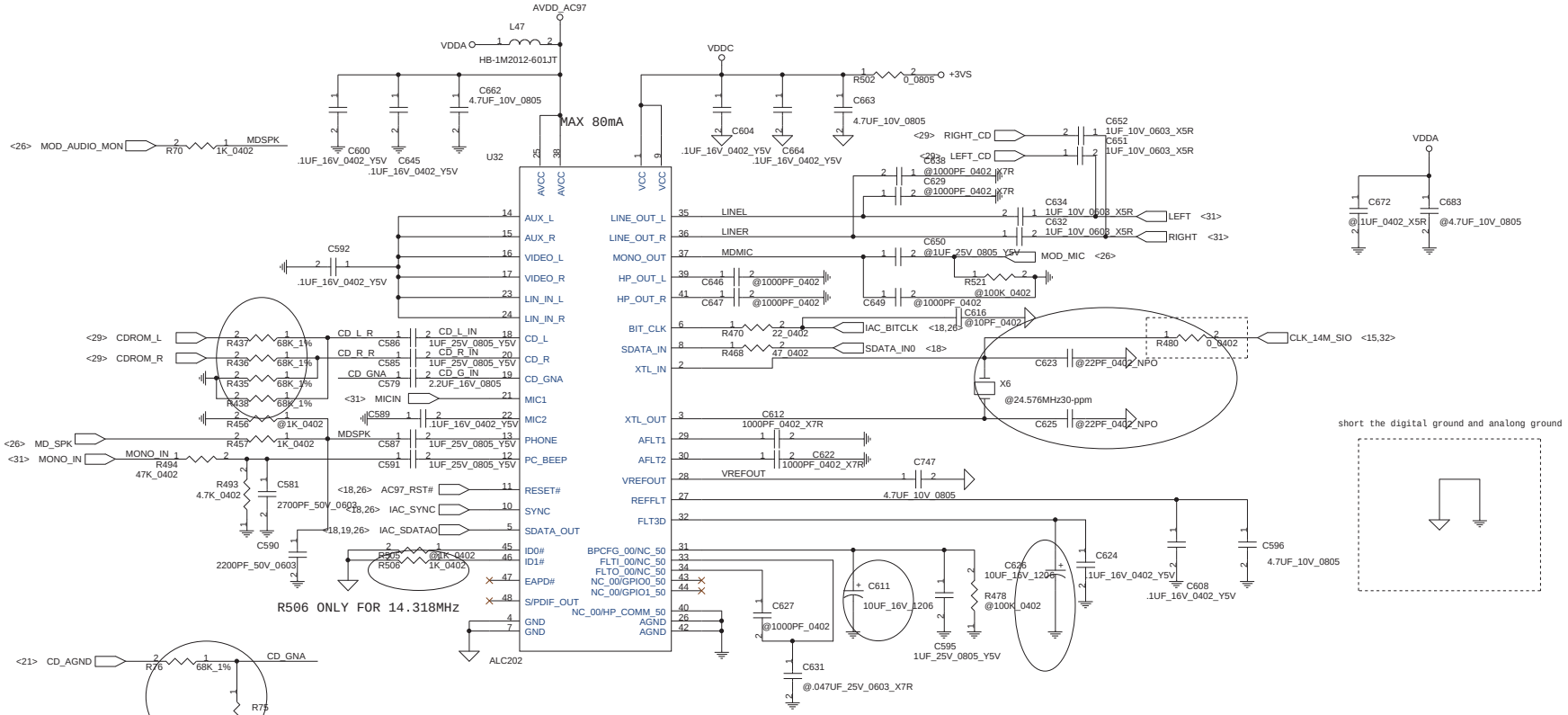
Title	SD/MMC W81386D	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 28 of 45	

R376,R377,C540,C539,R381,R380,C580,C567 CANCEL



Compal Electronics, Ltd.	
Title	Direct CD Play OZ165
Size: Custom	Document Number: ACT10
Rev	1.0A
Date: Thursday, May 30, 2002	Sheet 29 of 45

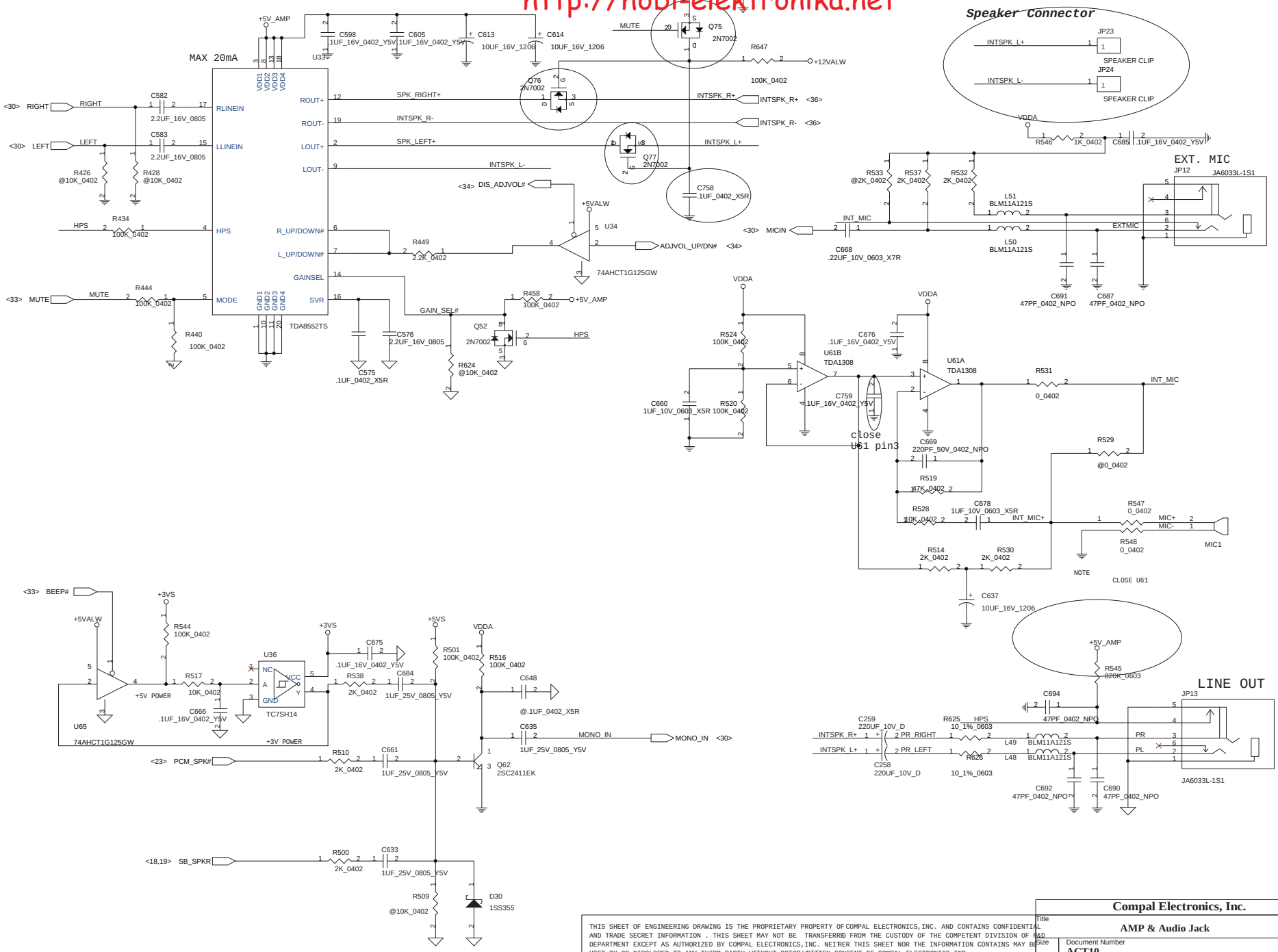




ID0#	ID1#	
1	1	14.318 OPEN
1	0	27MHZ
0	1	48MHZ
0	0	24.576MHZ

Compal Electronics, Inc.

Title	AC97 CODEC		
Size	Document Number ACT10		Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 30	of	45



Compal Electronics, Inc.

Title: AMP & Audio Jack

Size: | Document Number: ACT10 | Rev: 1.0A

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Fiduial Mark

FD1 FIDUCIALMARK FD3 FIDUCIALMARK FD2 FIDUCIALMARK FD4 FIDUCIALMARK
FD6 FIDUCIALMARK FD5 FIDUCIALMARK

Screw Hole

H20 O188X72D148X32 H21 O188X72D148X32 H26 O188X72D148X32 H27 O188X72D148X32
For HDD Case

H1 S354D118 H2 S354D118 H8 S354D118 H12 S354D118 H17 S354D118 H31 S354D118

H5 S315D118 H4 S315D118 H22 S315D118 H23 S315D118 H14 S315D118 H29 S315D118
H13 S315D118 H25 S315D118

H11 S315D173 H7 S315D173 H9 S315D173 H6 S315D173
4.4 Skew

H24 S354D173 H16 S276D142X173
H19 S335D118 H28 S354D122
H30 S217X146D197X126 H10 S217X146D197X126
H3 S354D169

CF2 CF4 CF5 CF6 CF9 CF12 CF13 CF17 CF10 CF14 CF11 CF15 CF1 CF3 CF7 CF8 CF18 CF16 CF20 CF19
SMDC40M80

+3VALW
R388 2.15K_1%_0603
TEMP_650 <33>
R389 0_0402
R40 Thermistor_0805_10K
SL210020F00

The temperature sensing for SIS650

CLK_PCI_SIO R157 @10_0402 C218 @10PF_0402
CLK_14M_SIO R158 @10_0402 C217 @10PF_0402
+3VS R633 10K_0402 R634 10K_0402

U70 PC87391 PC87391_TQFP_100P

<18,33> LAD0 LAD1 LAD2 LAD3
<15> CLK_PCI_SIO
<34> LPC_RST#
<18,33> LFRAME#
<18> LDRQ#
IO_PD# IO_CLKRUN#
<18,23,33> SIRQ
<15,30> CLK_14M_SIO
<21> DISKCHG# HDSEL# RDATA# WRPRT# TRK0# WGATE# WDATA# STEP# DIR# DRV0# MTR0# INDEX# 1.6M_EN#

LAD0 LAD1 LAD2 LAD3 LCLK LRESET# LFRAME# LDRQ# LPCPD# CLKRUN# SERIRQ SMI# CLKIN DSKCHG# HDSEL# RDATA# WP# TRK0# WGATE# WDATA# STEP# DIR# DR0# MTR0# INDEX# DENSEL DRATE0/IRSL2 NC NC NC NC NC NC/XCNF2 NC NC NC NC NC MTR1# NC NC RI2# DTR2#_BOUT2 CTS2# SOUT2 RTS2# SIN2 DSR2# DCD2#

PD0/INDEX# PD1/TRK0# PD2/WP# PD3/RDATA# PD4/DSKCHG# PD5/MSEN0 PD6/DRATE0 PD7/MSEN1
PNF/XRDY SLCT/WGATE# PE/WDATA# BUSY_WAIT#/MTR1# ACK#/DR1# SLIN#_ASTRB#/STEP# INIT#/DIR# ERR#/HDSEL# AFD#_DSTRB#/DENSEL STB#_WRITE#
DCD1# DSR1# SIN1 RTS1#/TEST SOUT1/XCNF0 CTS1# DTR1#_BOUT1/BADDR RI1#
IRTX IRRX1 IRRX2_IRSL0 IRSL1 IRSL3/PWUREQ#
NC/XCNF1 WDO# MTR1#/DRATE0 IRSL2/DR1# DR1#

LPD0 LPD1 LPD2 LPD3 LPD4 LPD5 LPD6 LPD7
LPTSLCT LPTPE LPTBUSY LPTACK# LPTSLCTIN# LPTINIT# LPTERR# LPTAFD# LPTSTB#
DCDA# DSRA# RXDA RTSA# TXDA DTRA# RIA#
IRTXOUT IRRX IRMODE XCNF1

C752 10UF_10V_1206 C753 .1UF_10V_0402_Y5V C190 .1UF_0402_X5R
R635 100K_0402 +3VS
IRTXOUT <36> IRRX <36> IRMODE <36>

RP135 1K_1206_10P8R
WDATA# WGATE# HDSEL# DIR# +5VS
STEP# MTR0# DRV0# RDATA# XCNF2

RP136 8P4R_1K
DISKCHG# INDEX# WRPRT# TRK0# +5VS

R636 100K_0402 +3VS
RP137 8P4R_100K

JP26 ACES 87153-2601
LPD0 LPD1 LPD2 LPD3 LPD4 LPD5 LPD6 LPD7 +5VS TXDA CTSA# DTRA# RIA#
LPTSLCT LPTPE LPTBUSY LPTACK# LPTSLCTIN# LPTINIT# LPTERR# LPTAFD# LPTSTB# DCDA# DSRA# RXDA RTSA#

R637 R638 R639 R640 R641 R642 R643 R644 @10K_0402
TXDA XCNF1 XCNF2 DTRA#

C189 .1UF_0402_X5R +5VS
C191 .1UF_0402_X5R +5VS

Signal	Pin #	Description
BADDR: DTRA#	61	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F

Compal Electronics, Inc.
Title: Skew Hole/SUPER IO
Size: Document Number: ACT10 Rev: 1.0A
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I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

	ENV0	ENV1	TRIS
IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

BOARD ID 000 --> 001
VERSION 0.2

Compal Electronics, Ltd.	
Title	EC PC87591/BIOS
Size: Custom	Document Number: ACT10
Rev	1.0A
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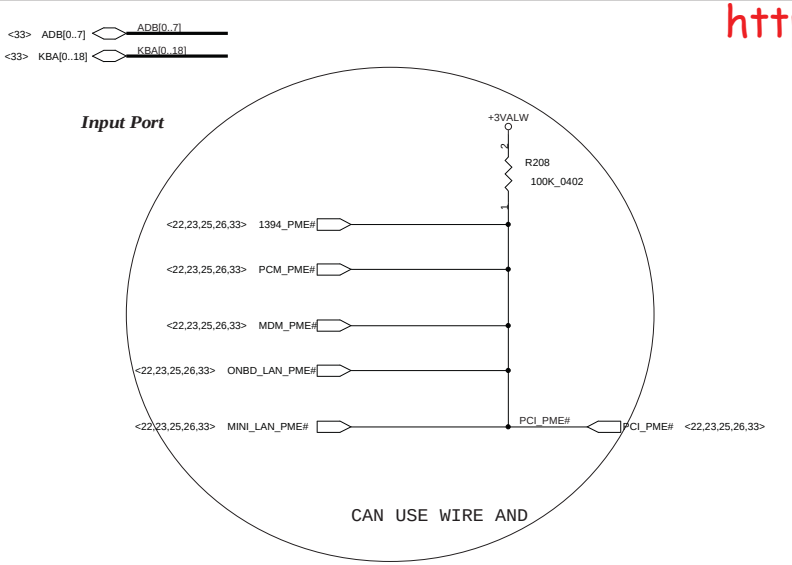
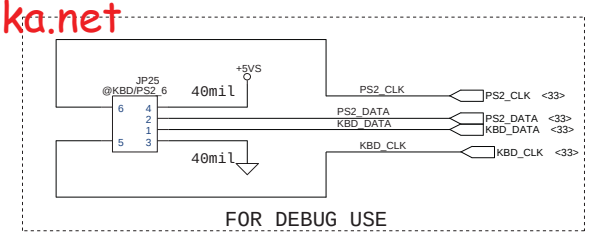
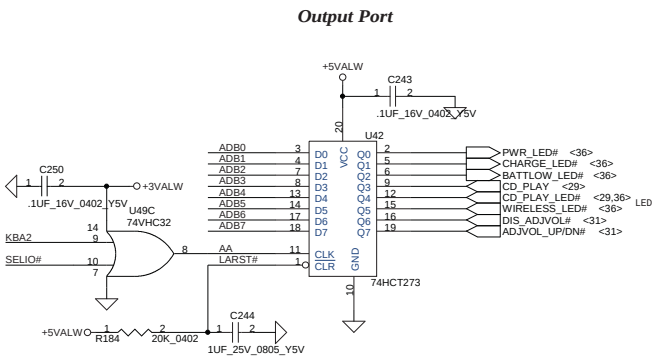
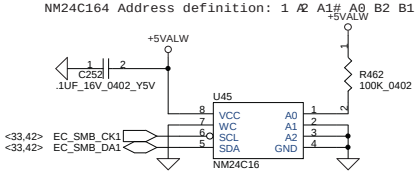




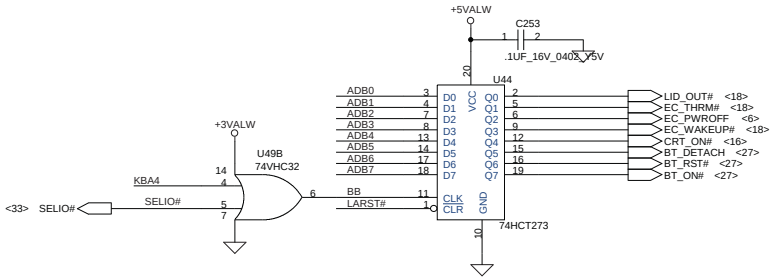


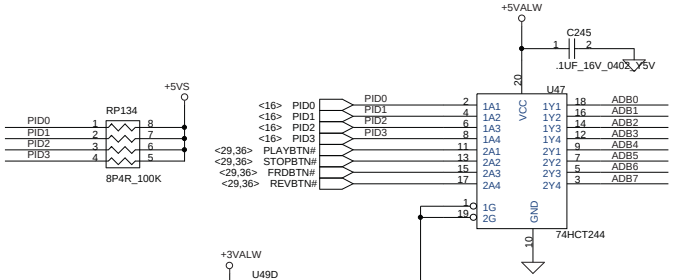
NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#

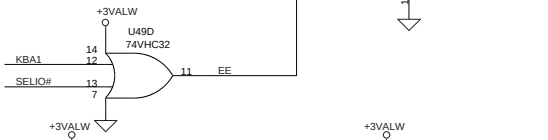


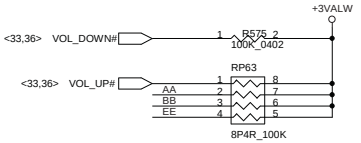
EC I2C Bus Address:

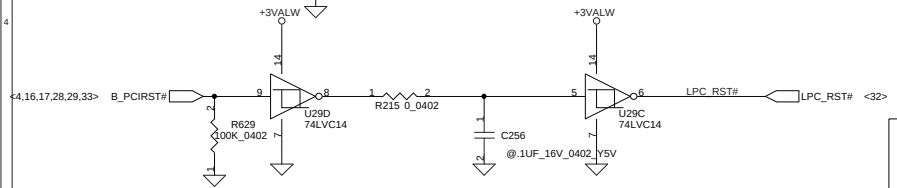
24C164: 1011xxx R/W#
24C16: 1010xxx R/W#











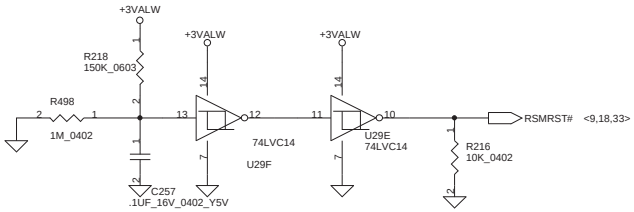
Compal Electronics, Inc.

Title: EC Extend I/O KB Conn. & BIOS

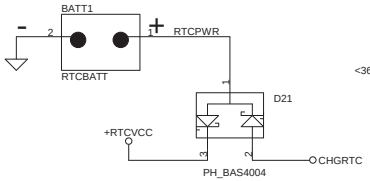
Size: | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 34 of 45

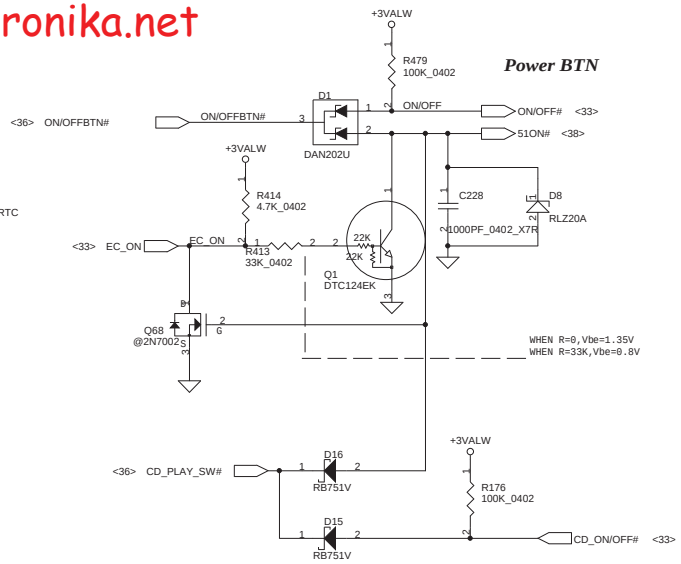
Power ON Circuit

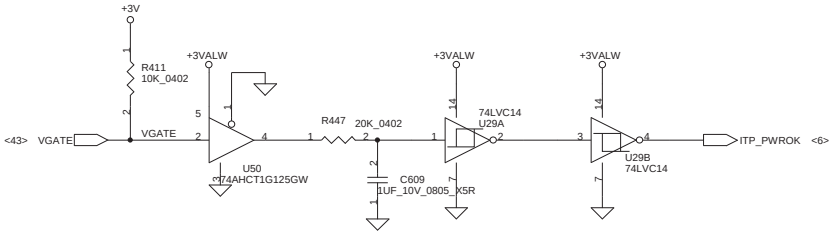


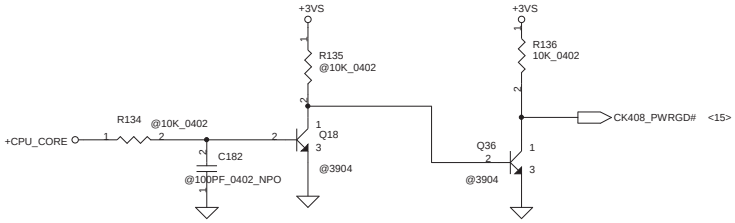
RTC Battery

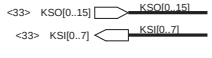


Power BTN

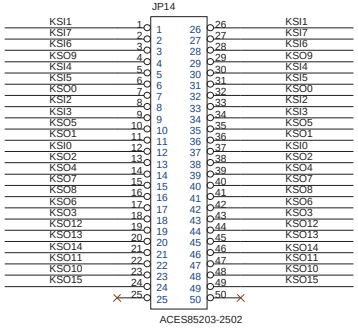


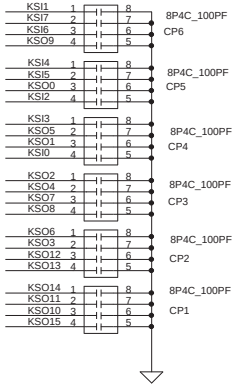


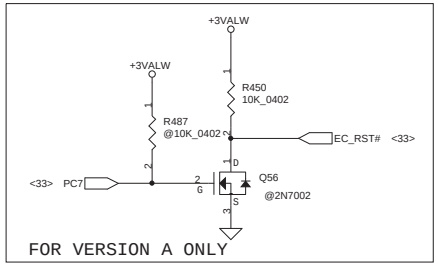




INT_KBD CONN.







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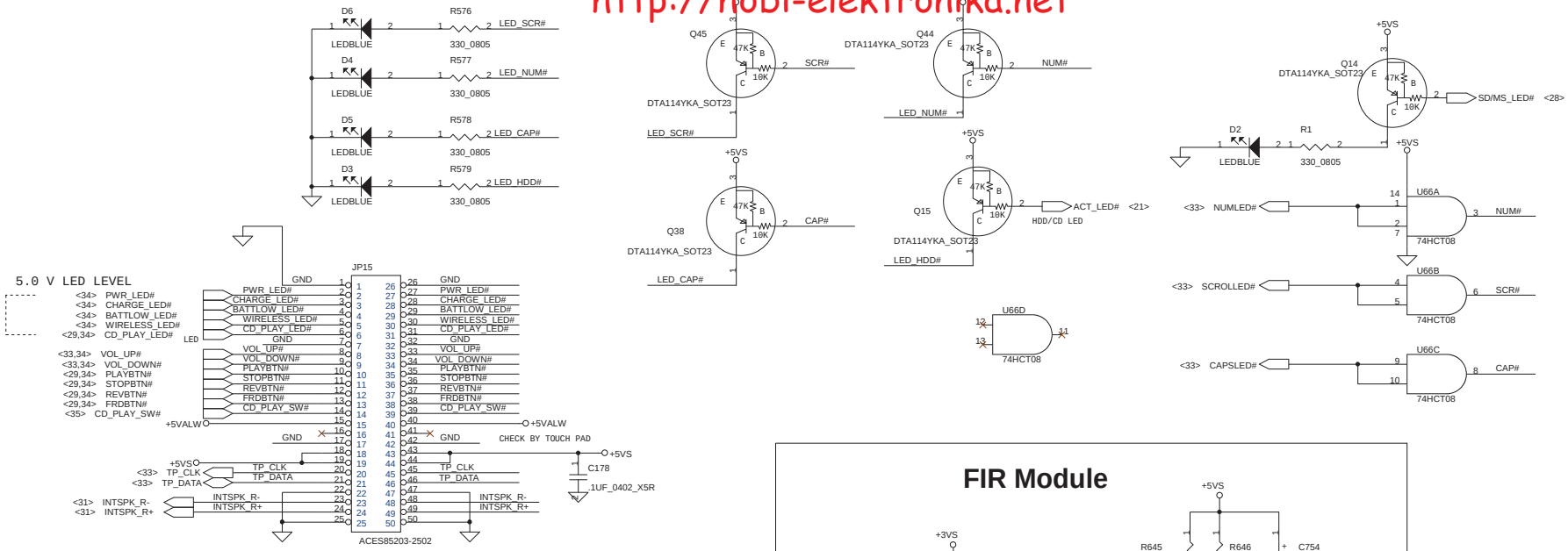
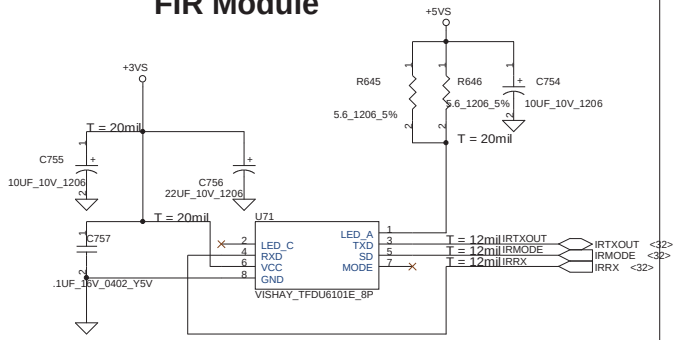
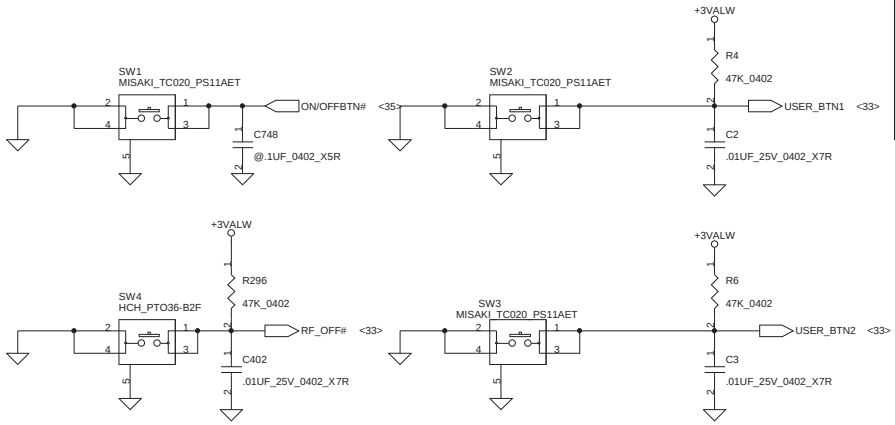
Title	Power OK/Reset/RTC battery/Lid Switch/Int. KB	
Size	Document Number ACT10	Rev 1.0A
Date: Thursday, May 30, 2002	Sheet 35 of 45	

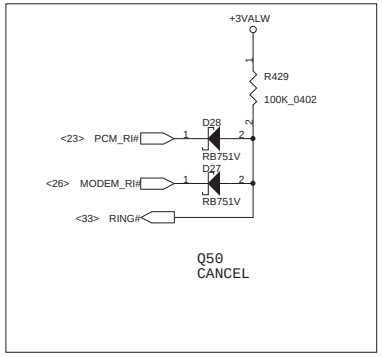


will change the pin definition after FPC finish by the M_E

FIR Module



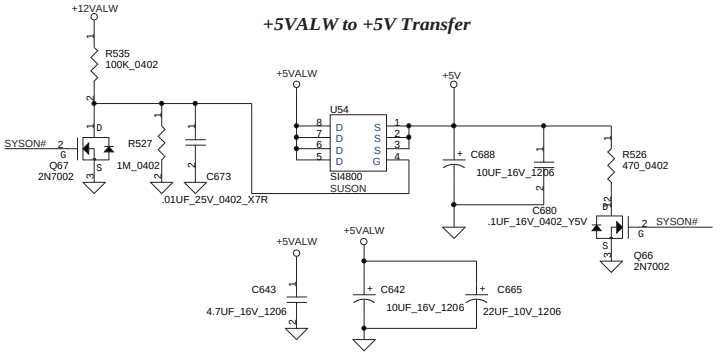




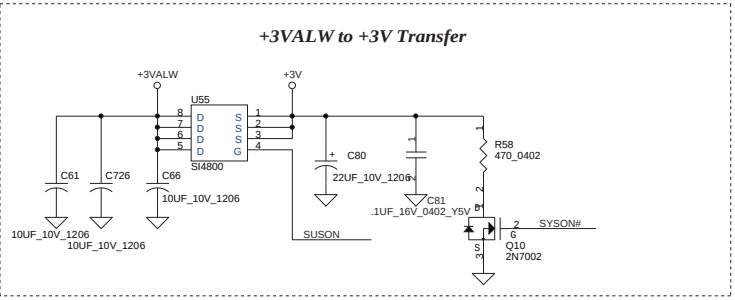
Compal Electronics, Ltd.

Title	SW/LED/RI#/IR/CD BUTTOM	
Size: Custom	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 36 of 45	

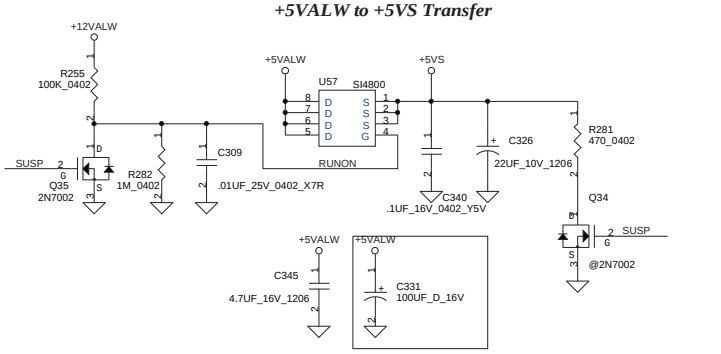
+5VALW to +5V Transfer



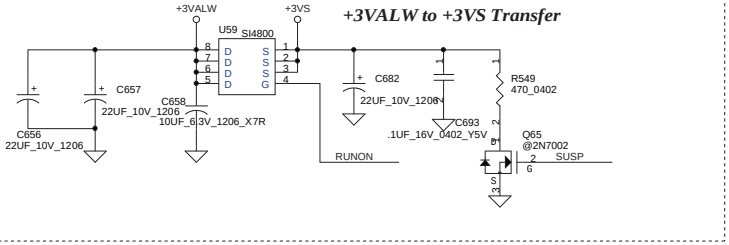
+3VALW to +3V Transfer



+5VALW to +5VS Transfer

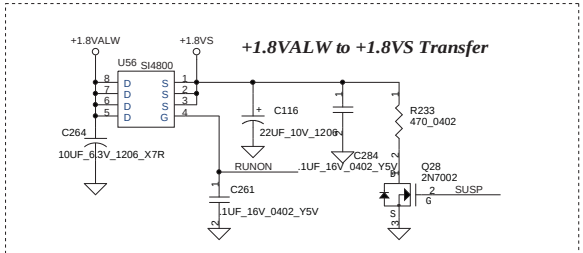


+3VALW to +3VS Transfer

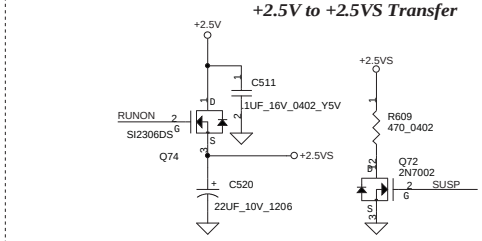


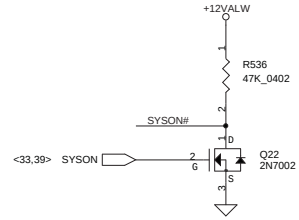
1.8VALW/+1.5VS Power direct provide

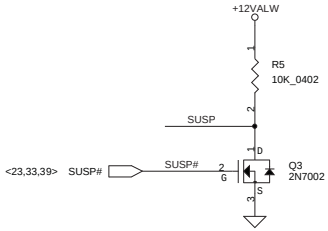
+1.8VALW to +1.8VS Transfer



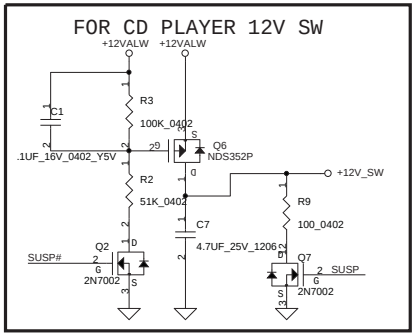
+2.5V to +2.5VS Transfer



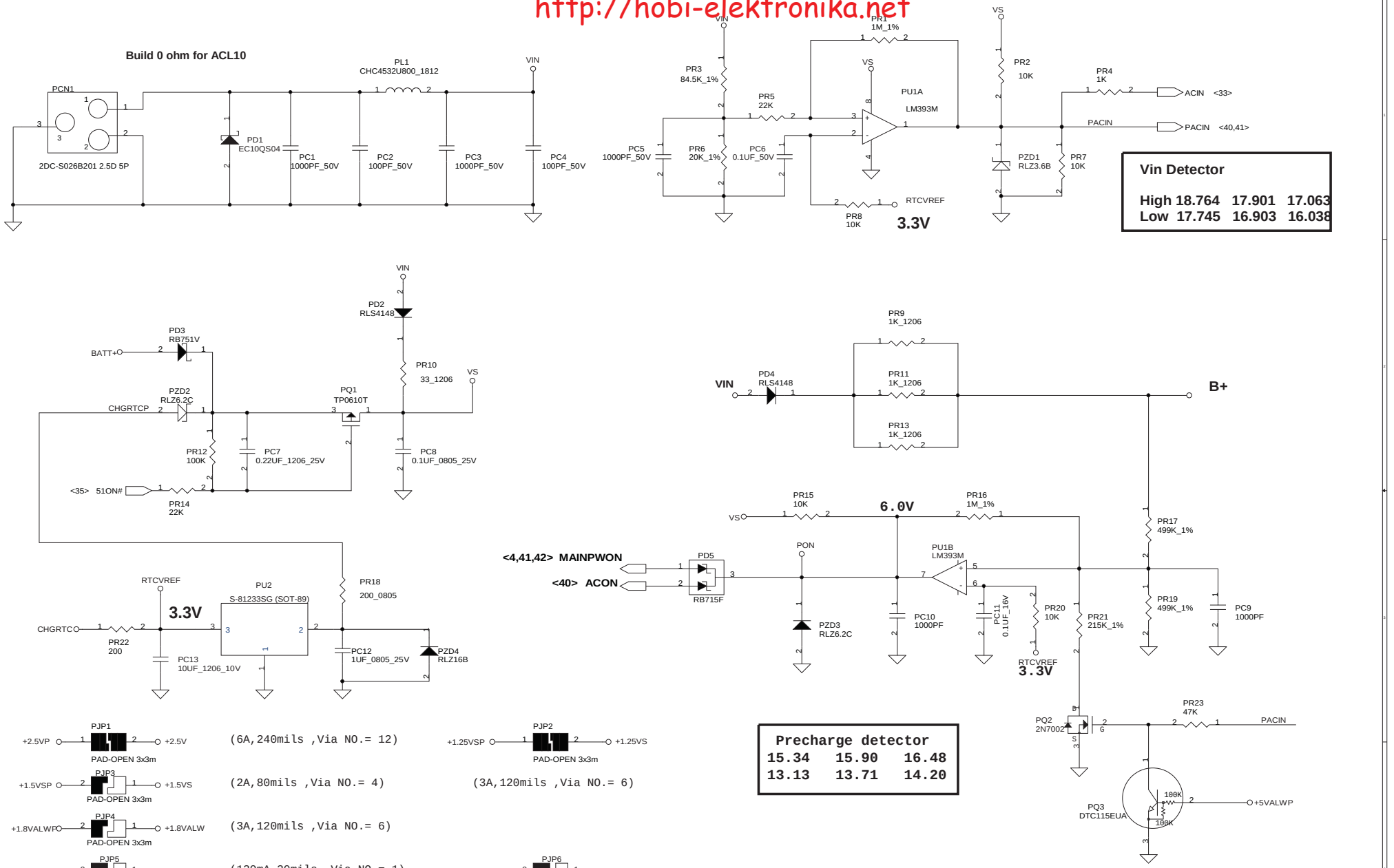




FOR CD PLAYER 12V SW



Compal Electronics, Inc.		
Title: DC/DC Circuit Interface		
Size	Document Number: ACT10	Rev: 1.0A
Date: Thursday, May 30, 2002	Sheet 37 of 45	



COMPAL ELECTRONICS, INC

Title: DCIN & DETECTOR

Size	Document Number	Rev
B	ACT10	1.0A

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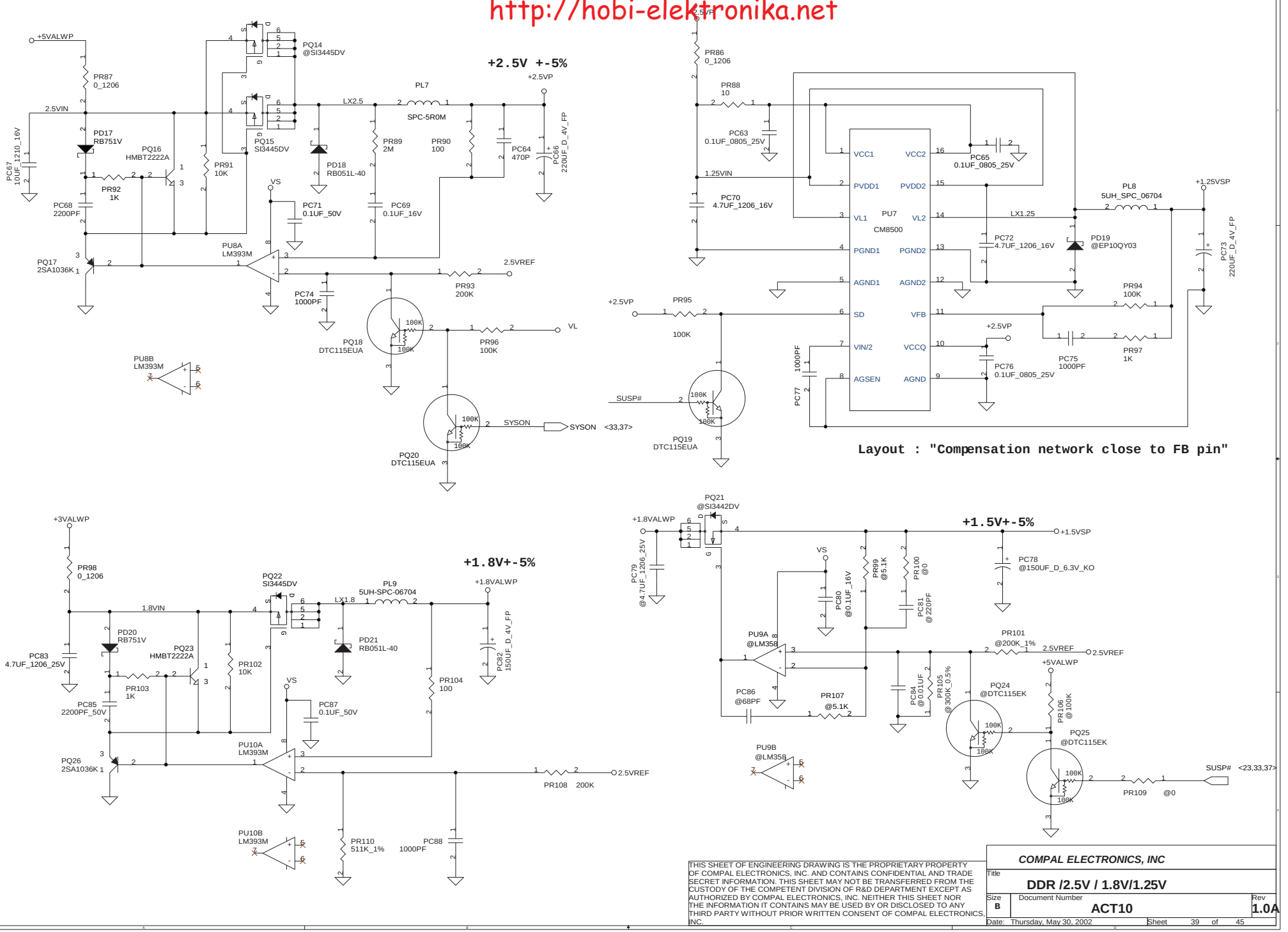

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COMPAL ELECTRONICS, INC

Title: **DDR /2.5V / 1.8V/1.25V**

Size	Document Number	Rev
B	ACT10	1.0A

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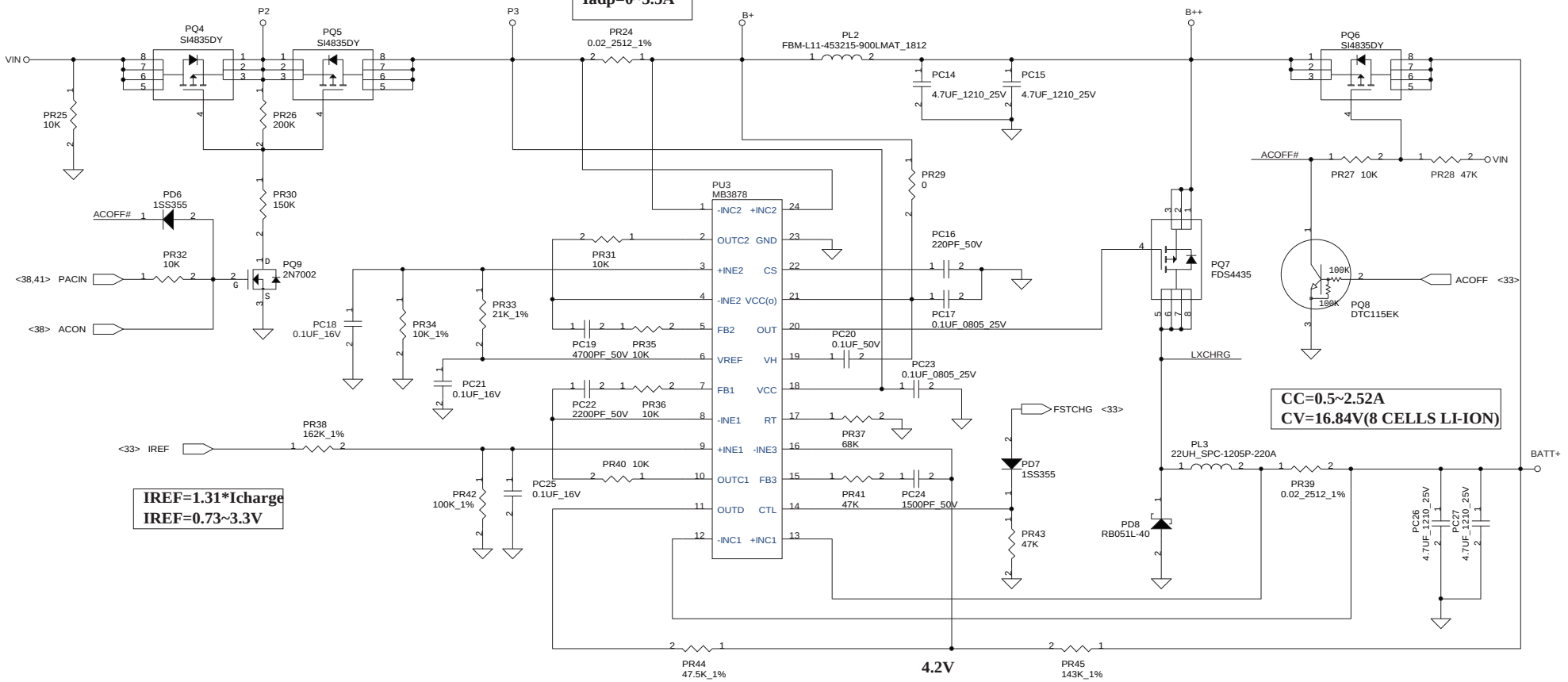
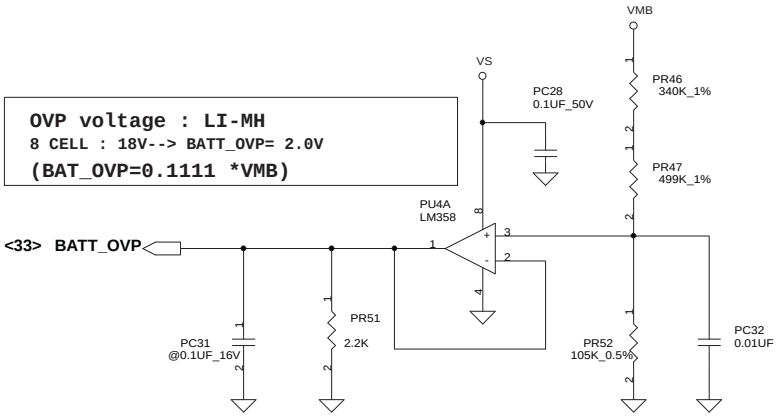
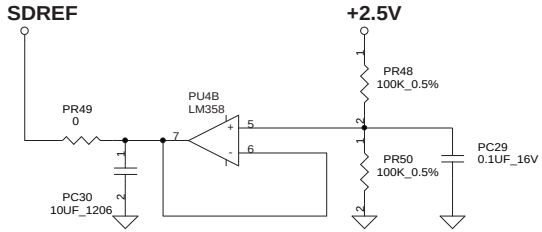




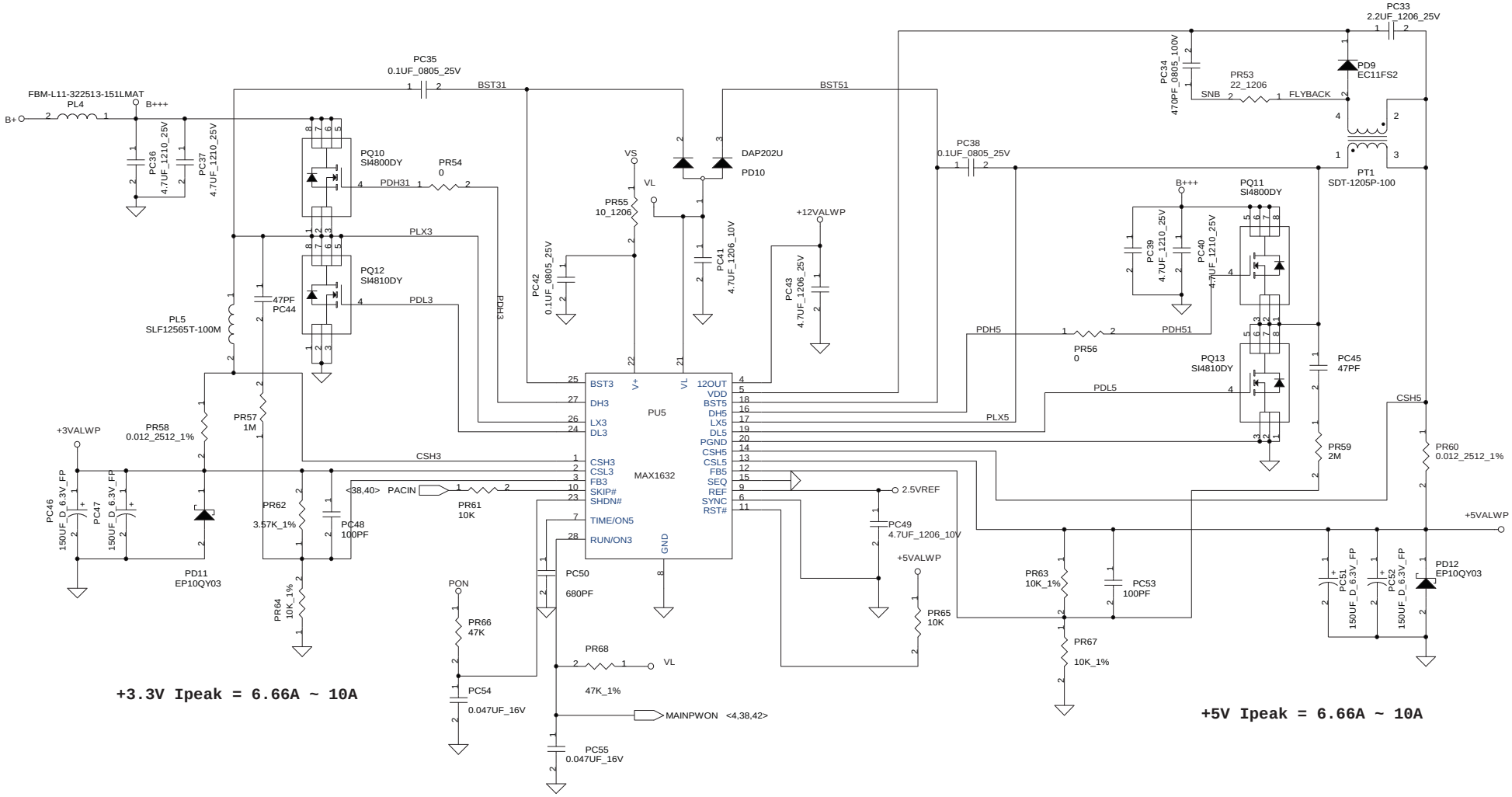


COMPAL ELECTRONICS, INC

Title: CHARGER

Size: B | Document Number: ACT10 | Rev: 1.0A

Date: Thursday, May 30, 2002 | Sheet 40 of 45



COMPAL ELECTRONICS, INC

Title: 5V/3.3V/12V

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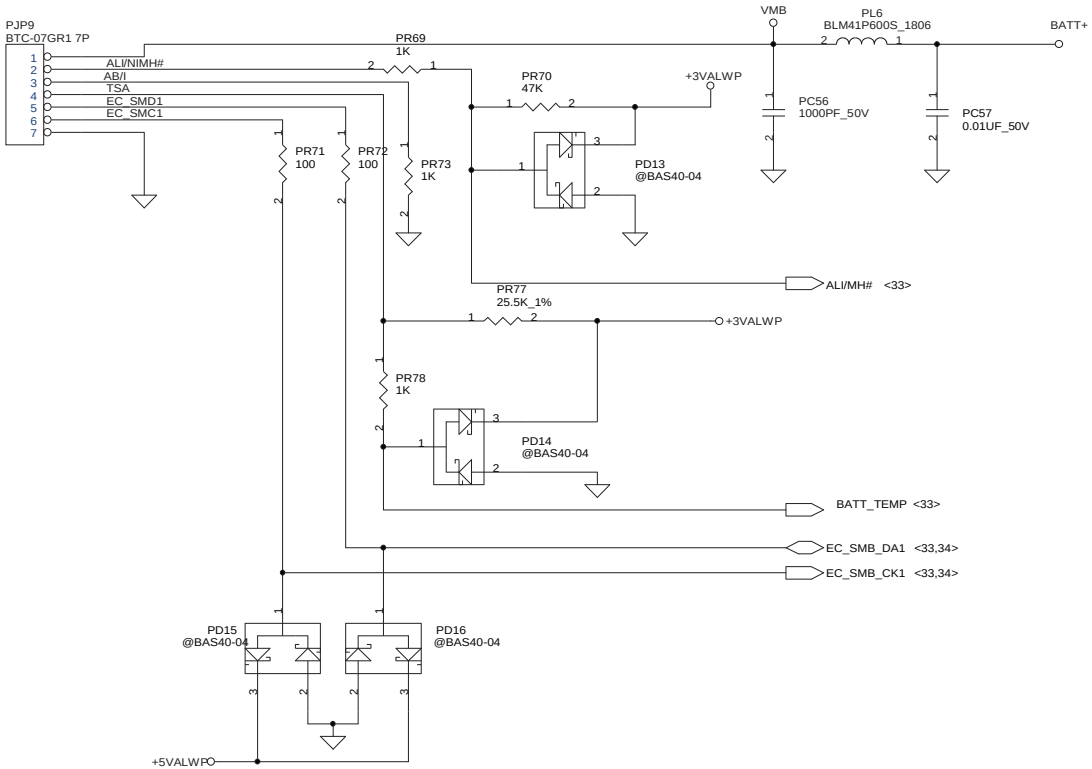
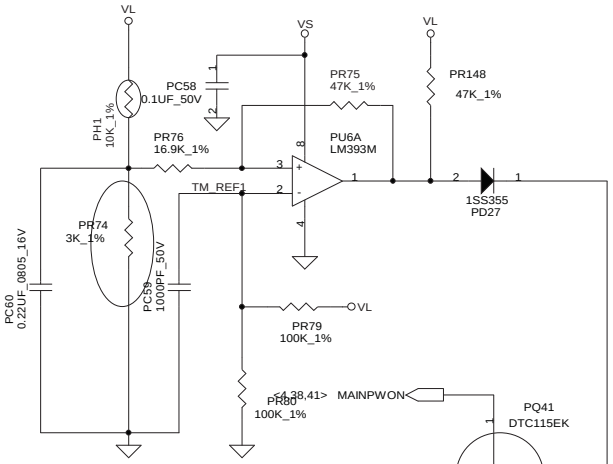
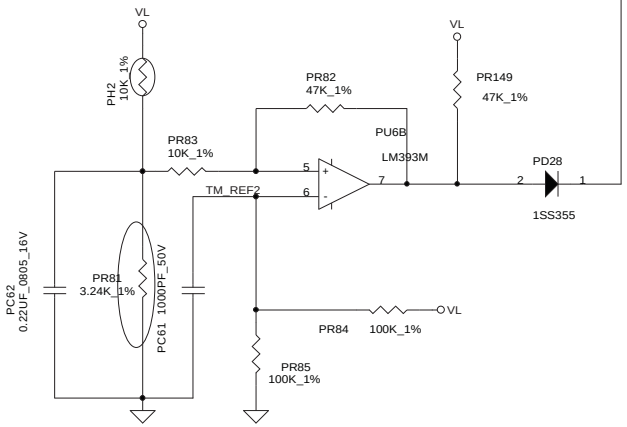


PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C



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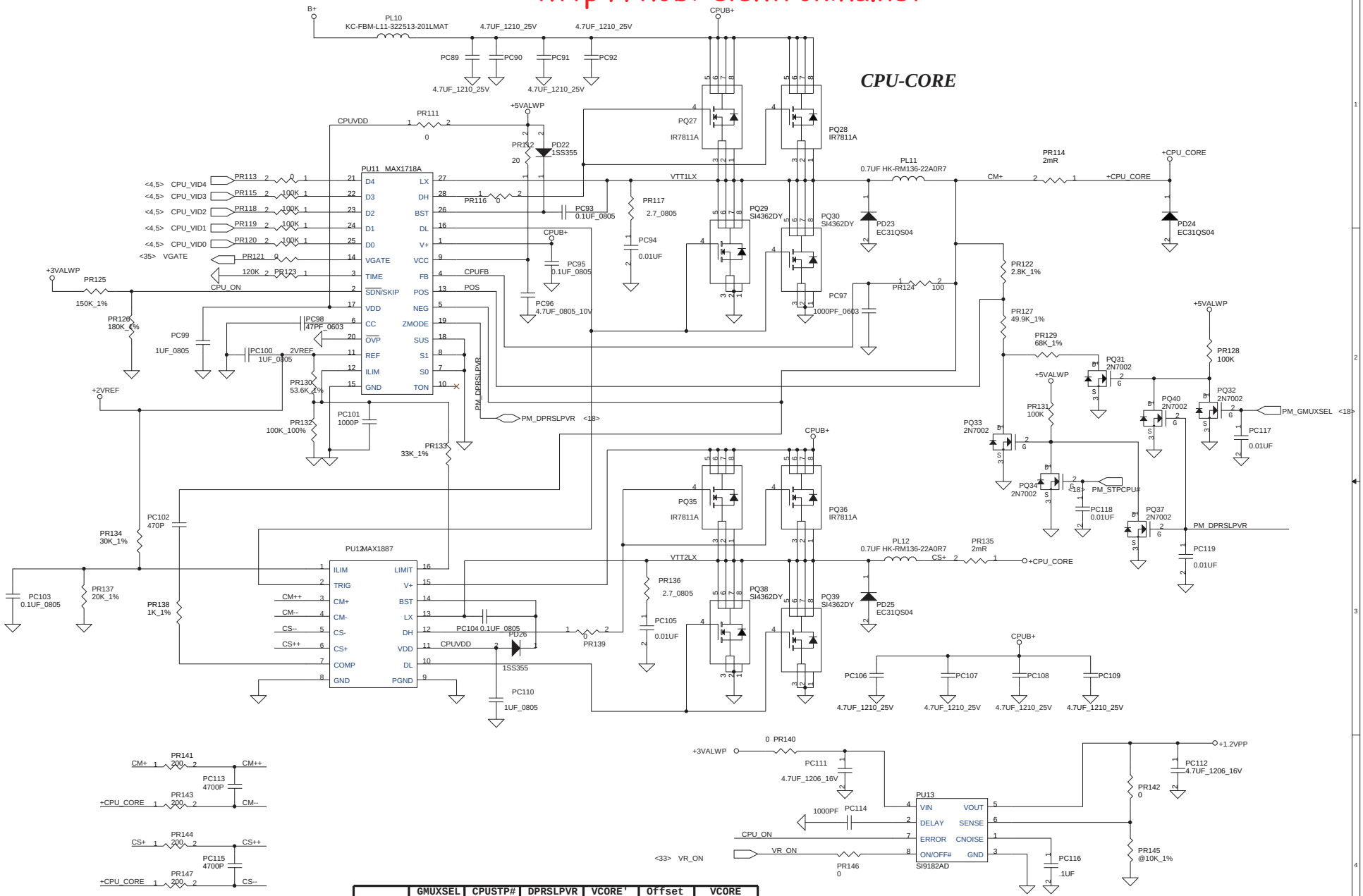
CPU-CORE



	GMUXSEL	CPUSTP#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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AGP Multiplexed Channel B List **Power Managment table**

AGP D0 : VBD7
AGP D1 : VBD6
AGP D2 : VBD5
AGP D3 : VBD4
AGP D4 : VBD3
AGP D5 : VBD2
AGP D6 : VBD1
AGP D7 : VBD0
AGP D19 : VBD11
AGP D20 : VBD10
AGP D21 : VBD8
AGP D22 : VBD9
AGP D27 : VBDE
AGP D28 : VBCTL0
AGP D29 : VBCTL1
AGP D30 : VBHSYNC
AGP D31 : VBVSYNC
AGP AREQ# : VBCD
AGP RBF# : VBHCLK
AGP SBA0 : VBCLK
AGP STB1 : VBGCLK
AGP STB1# : VBGCLK#

AGP D24 : VAD0
AGP D23 : VAD1
AGP D25 : VAD2
AGP D26 : VAD3
AGP D10 : VAD4
AGP D9 : VAD5
AGP D8 : VAD6
AGP D11 : VAD7
AGP D12 : VAD8
AGP D13 : VAD9
AGP D14 : VAD10
AGP D15 : VAD11
AGP D16 : VADE
AGP D18 : VAHSYNC
AGP D17 : VAVSYNC
AGP STB0 : VAGCLK
AGP STB0# : VAGCLK#

Signal / State	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

IDSEL :
1394 : AD16
LAN : AD17
CARDBUS : AD19
MINI_PCI : AD18, AD22

PCI MASTER :
1394 : REQ0#, GNT0#
MINI-PCI(Wireless Lan) : REQ1#, GNT1#
CARDBUS : REQ2#, GNT2#
LAN : REQ3#, GNT3#
MINI-PCI : REQ4#, GNT4#

PCI IRQ ROUTING :
VGA : INTA#
1394 : INTB#
CARDBUS/MINI-PCI : INTC#
LAN/MINI-PCI : INTD#

History list

Item	Description	Page	Note	Date
1	Layout Ver. 0.0		Power not Include	01/11/22
2	Layout Ver. 0.0 add power		Power Include	01/11/23
3	Add Part Number			01/12/25
4	Change some parts suggest from SiS		Add Jumpper	01/1/3

Compal Electronics, Inc.

Title: Note & Revision

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