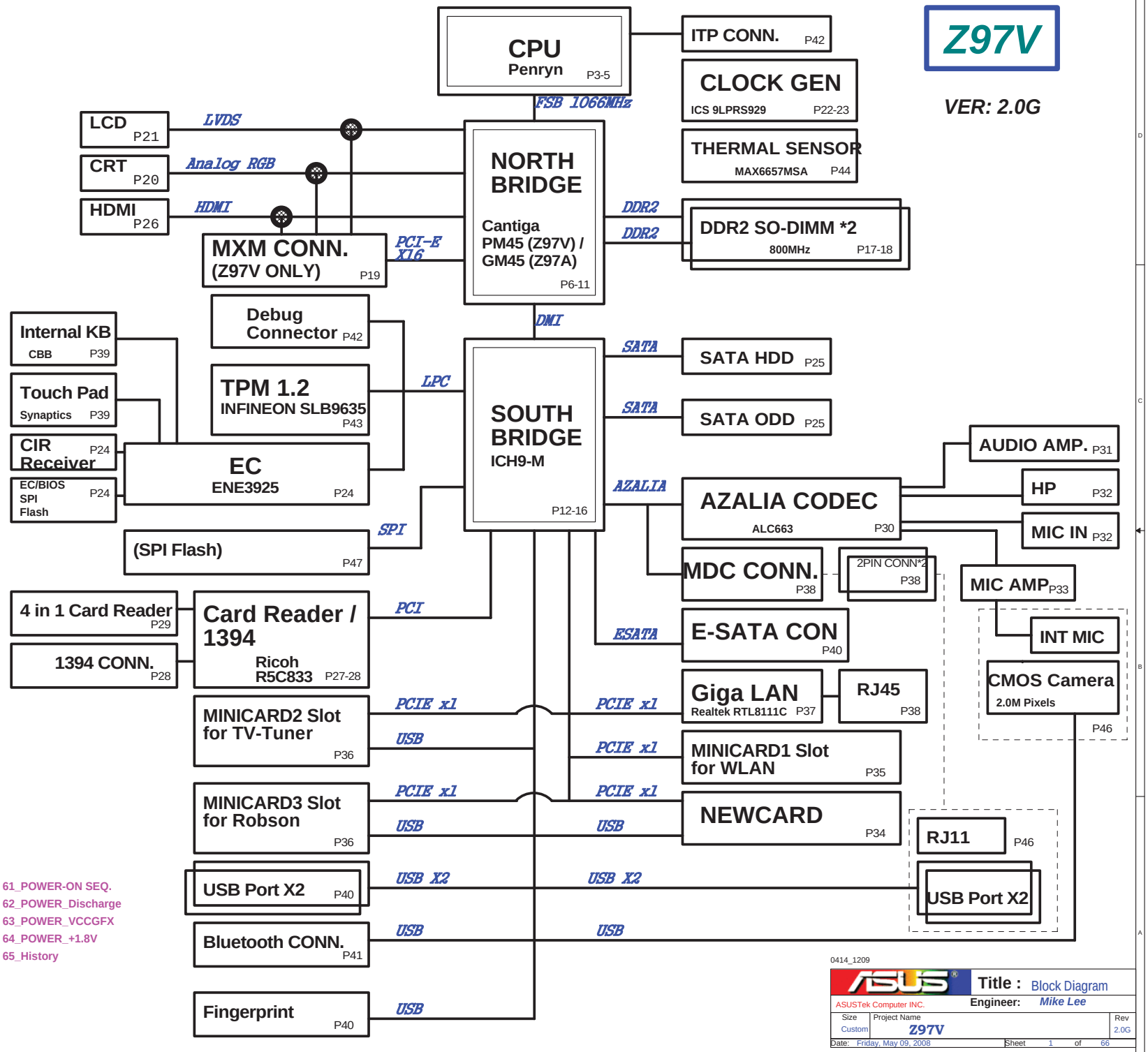
01_Block Diagram
02_System Setting
03_CPU-PENRYN(1)
04_CPU-PENRYN(2)
05_CPU-Capacitor
06_NB_-CANTIGA--CPU (1)
07_NB_-CANTIGA--DDR2/PEG (2)
08_NB_-CANTIGA--DDR2 bus (3)
09_NB_-CANTIGA--POWER (4)
10_NB_-CANTIGA--POWER (5)
11_NB_-CANTIGA--GND/Strap(6)
12_SB_-ICH9M(1)
13_SB_-ICH9M(2)
14_SB_-ICH9M(3)
15_SB_-ICH9M(PWR)
16_SB_-ICH9M--OTHER
17_DDRII_1-DIMMs
18_DDRII_2-Termination
19_MXM_Interface
20_CRT Connector
21_LVDS & Inverter Connector
22_Main Clock-1
23_Main Clock-2
24_EC ENE3925
25_SATA HDD & ODD Connector
26_HDMI Conn.
27_Ricoh R5C833_PCI
28_Ricoh R5C833_1394/SD
29_4 in 1 Card Reader
30_Audio_1-Realtek ALC888
31_Audio_2-Speaker / MicA
32_Audio_3-Phone Jack
33_MIC PreAmp.
34_NEWCARD
35_MINICARD for Wireless
36_MINICARD for TV & Robson
37_LAN RTL8111C
38_MDC / RJ45
39_Fingerprint&Touch Pad & KB
40_USB/ESATA Connector
41_Bluetooth Connector
42_ITP & Debug Connector
43_TPM Connector & I2C GPIO
44_Thermal Sensor & Fan
45_DC IN & BAT IN
46_50PIN (Inv/Launch/USB)
47_SPI Flash
48_RST SW / LED
49_Screw Hole
50_EMI CAP
51_POWER_FLOWCHART
52_POWER_CHARGER
53_POWER_SYSTEM
54_POWER_VCORE
55_ DDR POWER(1.8V)
56_POWER_I/O_+3VA
57_POWER_GOOD_DETECTER
58_POWER_LOAD SWITCH
59_POWER_1.5VS & 2.5VS
60_POWER_CHIP (1.05VS)*



ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	Native	PM_SYNC#	+3VS
GPIO 01	GPI	GP_INT#	+3VS
GPIO [2:5]	GPO	Hybrid Graphic Ctrl.	+3VS
GPIO 06	GPI	HDMI_HPD	+3VS
GPIO 07	GPO	Hybrid Graphic Ctrl.	+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	(PD GND)	+3VSUS
GPIO 10	Native	--	+3VSUS
GPIO 11	GPI	SMBALERT# (PU +3VSUS)	+3VSUS
GPIO 12	GPI	EXT_SCI#	+3VSUS
GPIO 13	GPO	--	+3VSUS
GPIO 14	Native	AC_OK	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPO	--	+3VS
GPIO 18	GPO	--	+3VS
GPIO 19	GPO	BT_LED	+3VS
GPIO 20	GPI	--	+3VS
GPIO 21	GPO	WLAN_LED	+3VS
GPIO 22	GPI	(PU +3VS)	+3VS
GPIO 23	Native	LPC_DRQ1#	+3VS
GPIO 24	GPO	MXMPWR_ON#	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	--	+3VSUS
GPIO 28	GPO	--	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	Native	PM_CLKRUN#	+3VS
GPIO 33	GPO	--	+3VS
GPIO 34	Native	--	+3VS
GPIO 35	Native	--	+3VS
GPIO 36	GPO	WLAN_ON	+3VS
GPIO 37	GPO	BT_ON	+3VS
GPIO 38	GPI	--	+3VS
GPIO 39	GPI	--	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	+3VSUS
GPIO 45	Native	USB_OC9#	+3VSUS
GPIO 46	Native	USB_OC10#	+3VSUS
GPIO 47	Native	USB_OC11#	+3VSUS
GPIO 48	GPO	--	+3VS
GPIO 49	GPO	--	+3VS
GPIO 50	Native	PCI_REQ#1 (PU +3VS)	+3VS
GPIO 51	Native	PCI_GNT#1	+3VS
GPIO 52	Native	PCI_REQ#2 (PU +3VS)	+3VS
GPIO 53	Native	PCI_GNT#2	+3VS
GPIO 54	Native	PCI_REQ#3 (PU +3VS)	+3VS
GPIO 55	Native	PCI_GNT#3	+3VS
GPIO 56	GPI	(PU +3VSUS)	+3VSUS
GPIO 57	GPI	(PU +3VSUS)	+3VSUS
GPIO 58	Native	SPI_CS#1	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	LINKALERT# (PU +3VSUS)	+3VSUS

GPIO 02	GPO	MXMPWR_ON# (RESERVED)	
GPIO 24	GPO	MXMPWR_ON#	
GPIO 03	GPO	MXMRST#	
GPIO 04	GPO	dGPU_DDC_SEL#	For LCD/CRT Signal Switch
GPIO 05	GPO	dGPU_IMG_SEL#	
GPIO 06	GPI	HDMI_HPD	For HDMI DDC Signal Switch, HDMI Hot Plug Detection
GPIO 07	GPO	dGPU_DDC_ALT_SEL#	

2008/02/28

PCI Device	IDSEL#	REQ/GNT#	Interrupts
1394	AD17	0	INTA
CARD READER	AD17	0	INTB

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor	1001110x (98)
MXM Thermal Sensor	(0x9A or 0x9E)
GPIO Extender (for OV)	0100110x (48)
HDMI DDC	

2008/01/14

GM45 QS(B2) 02G010021410

PM45 QS(B2) 02G010022500

ICH9M-B(A3) 02G010015340

0414_1209

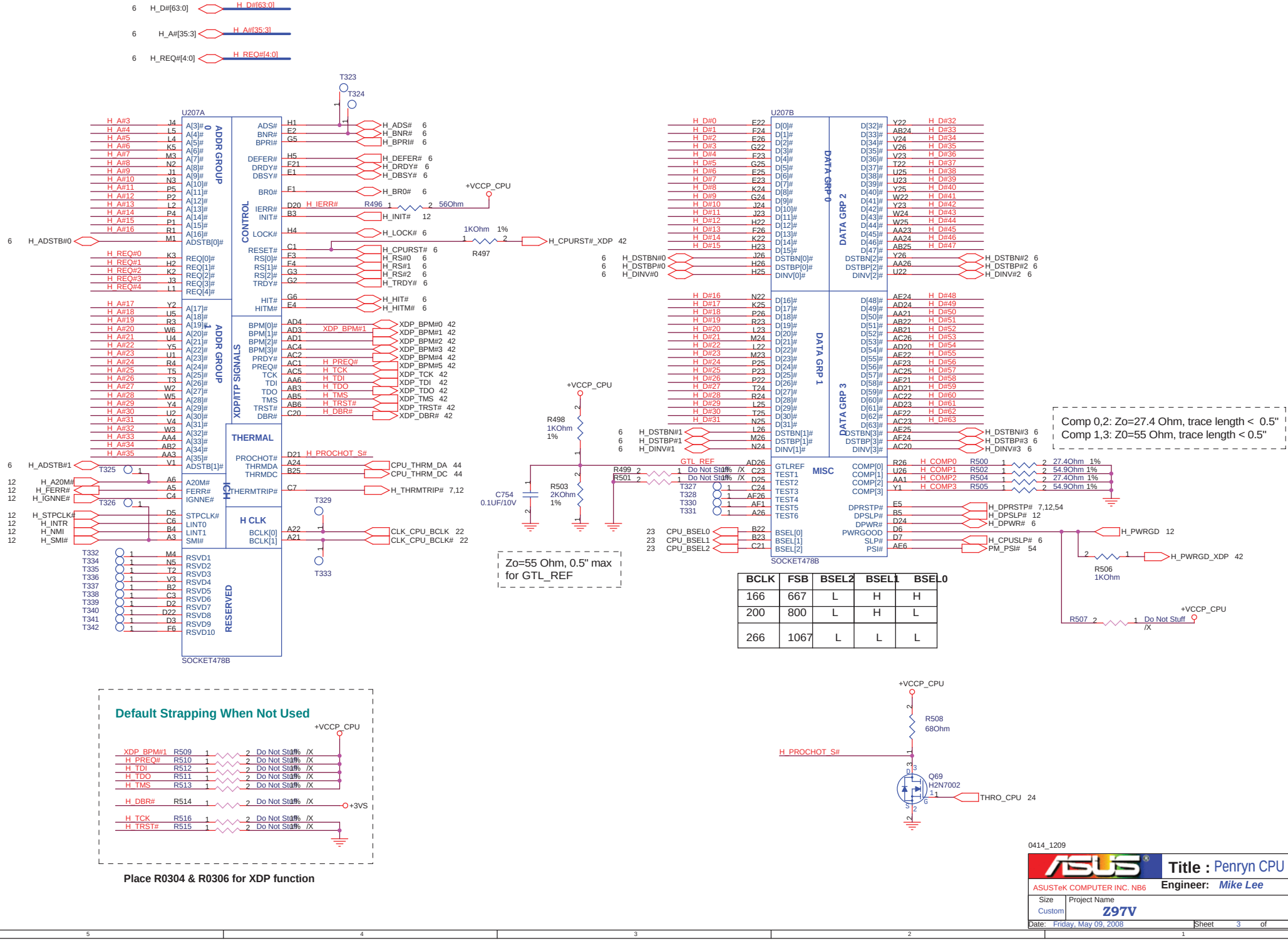
ASUSTek Computer INC.

Title : System Setting

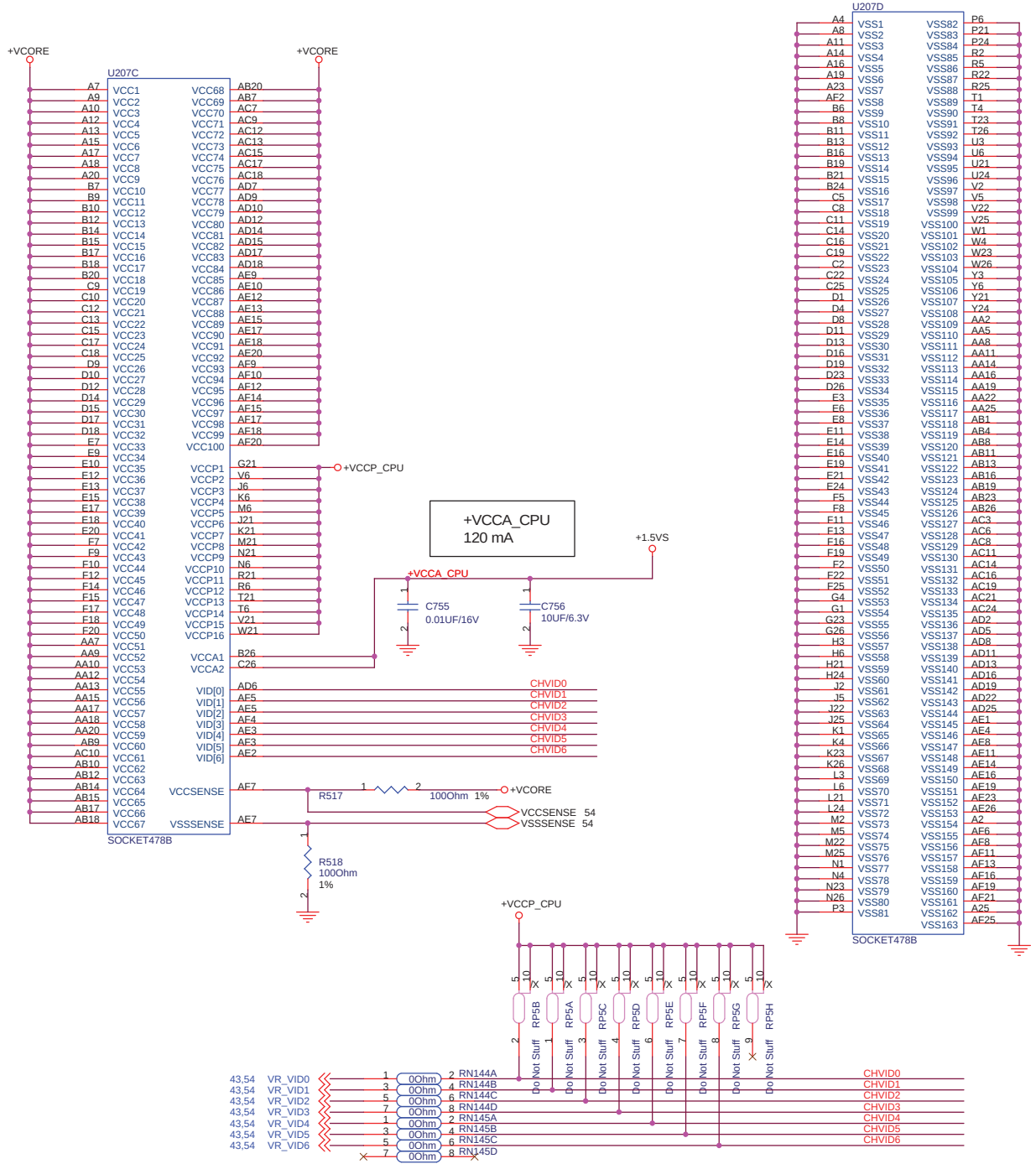
Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 2 of 66



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L



0414_1209

Title : Penryn CPU (2)

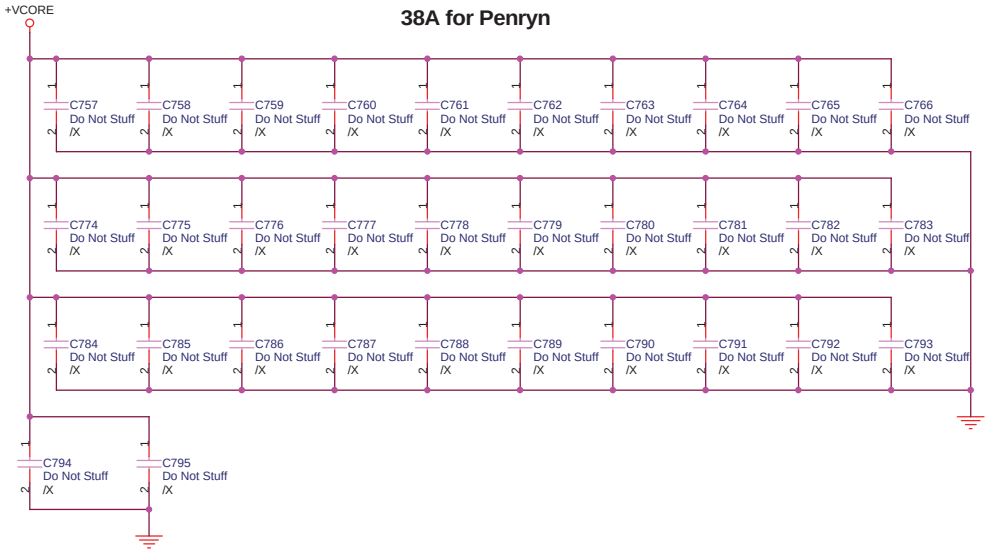
ASUSTeK COMPUTER INC. NB6

Engineer: *Mike Lee*

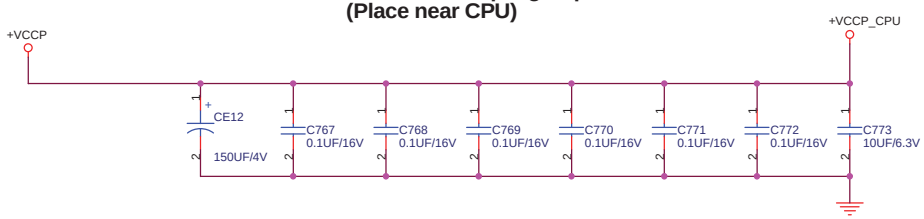
Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 4 of 66

38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?

0414_1209

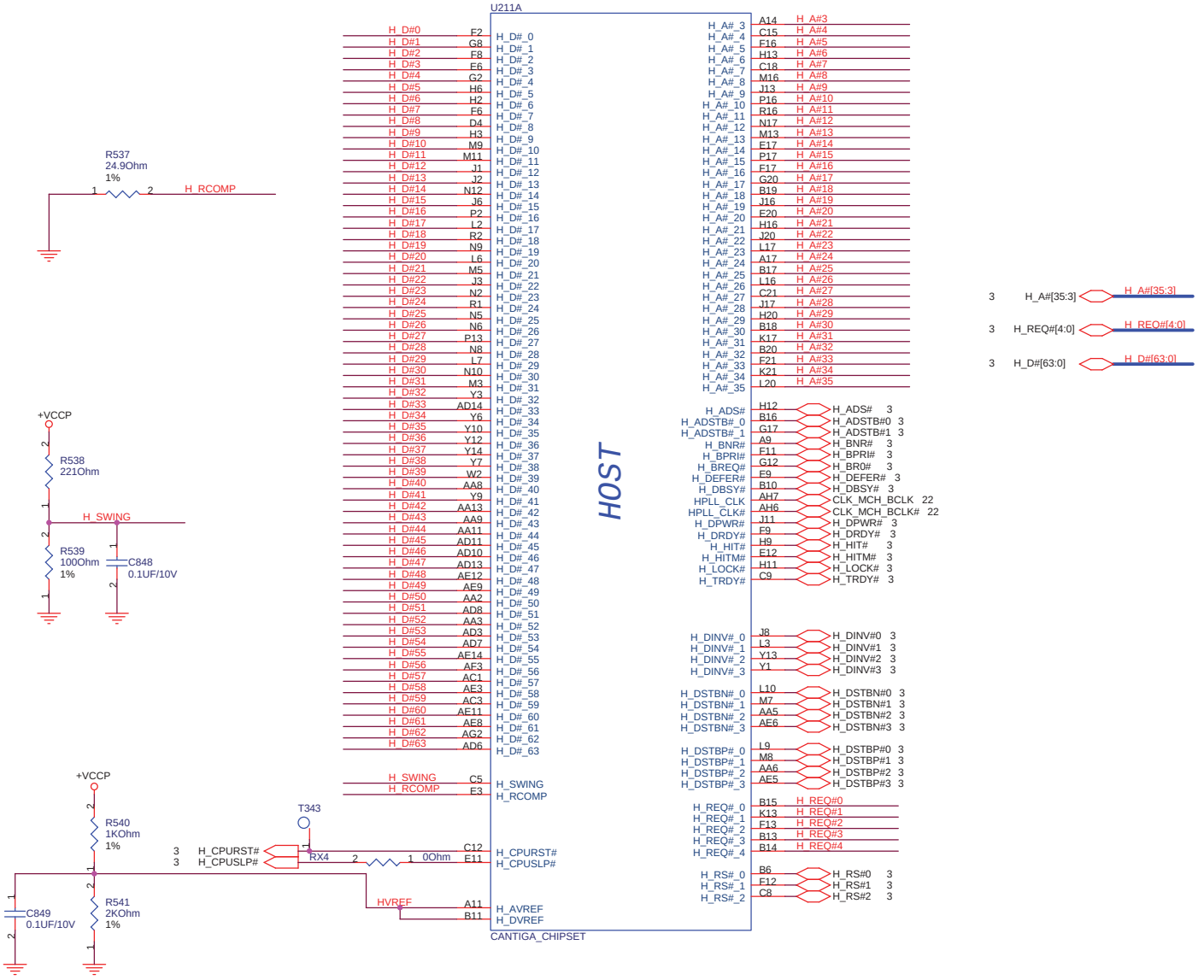
ASUSTeK COMPUTER INC. NB6

Title : CPU CAPS

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.00

Date: Friday, May 09, 2008 Sheet 5 of 66



Cap 0.1uF within 100 mils from GMCH

0414_1209

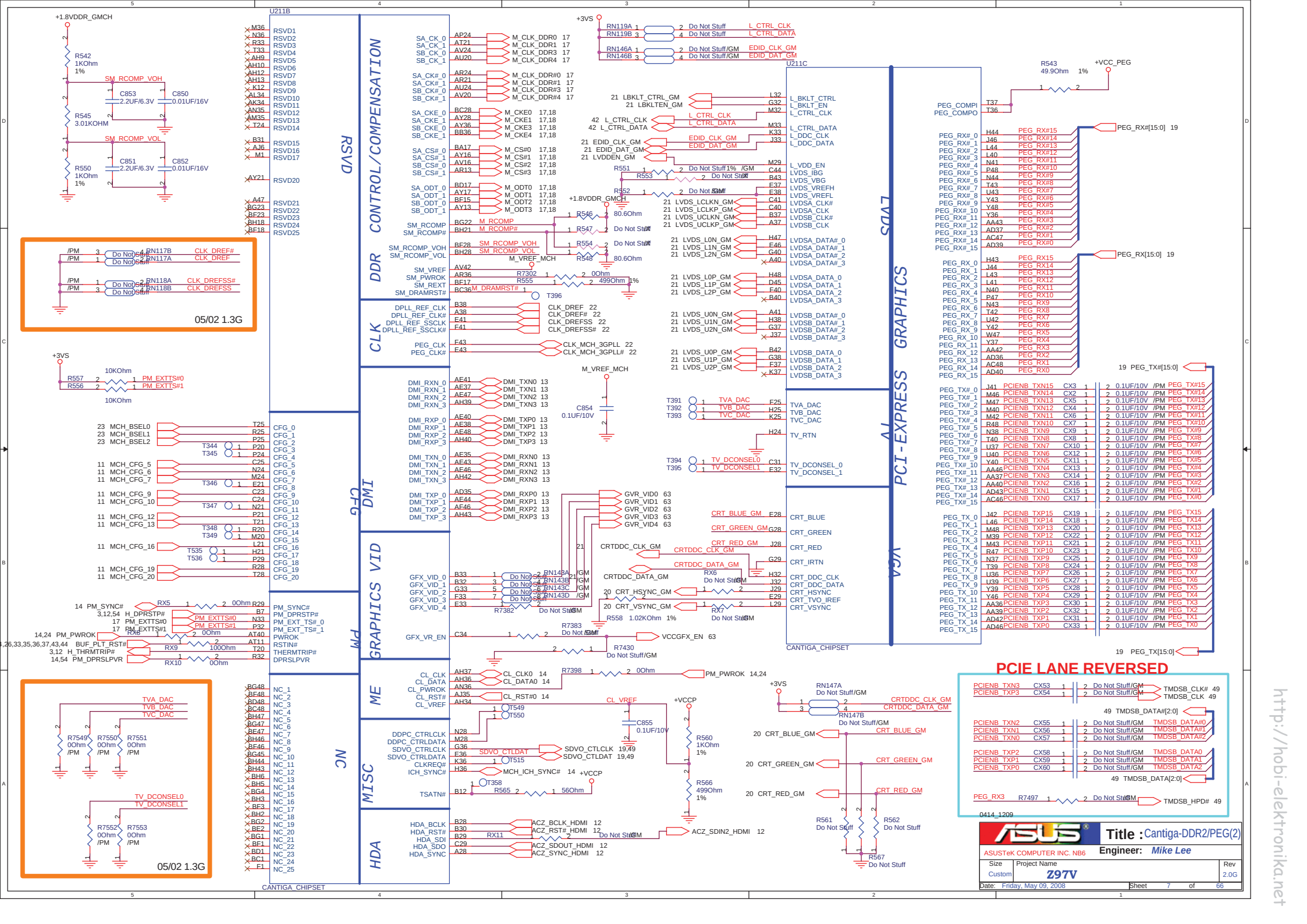
ASUSTeK COMPUTER INC. NB6

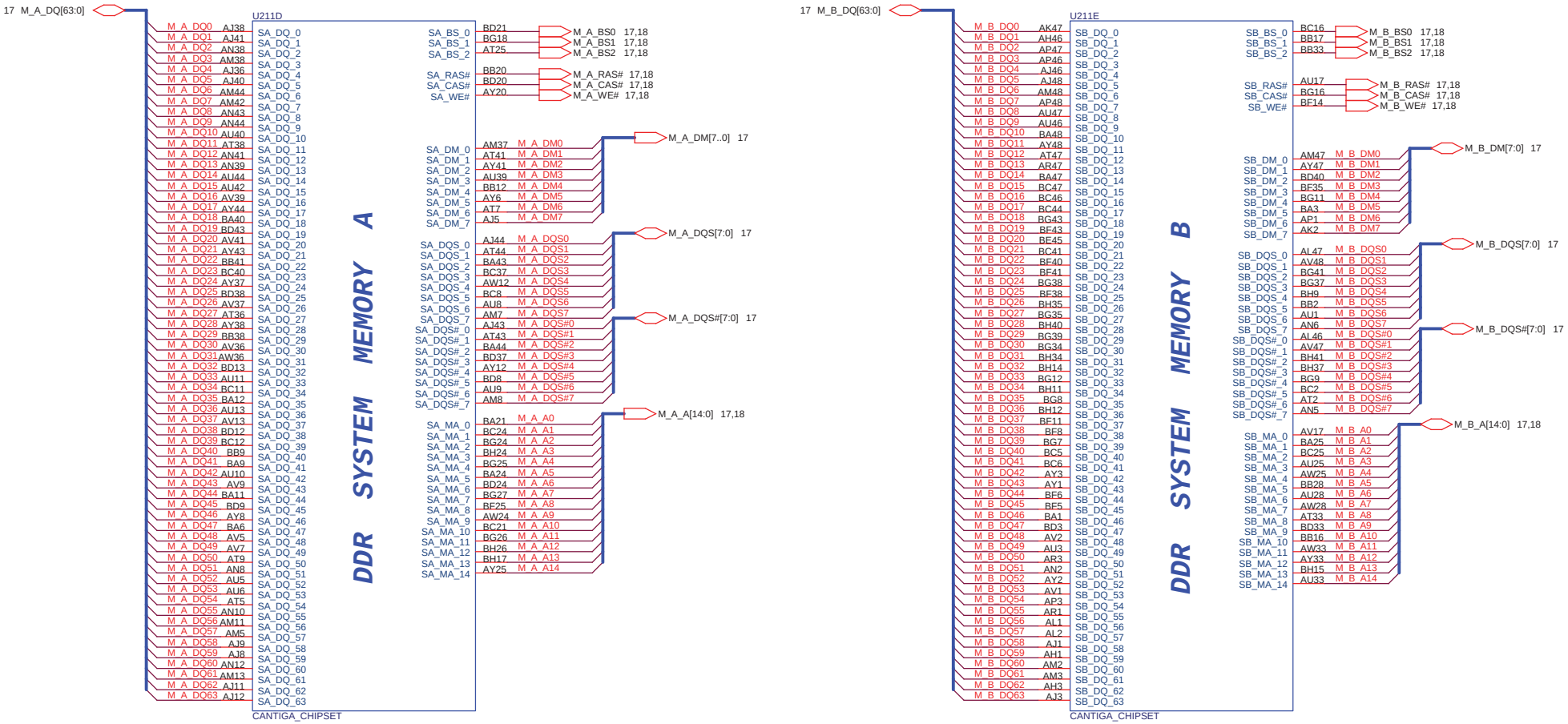
Title : Cantiga -- CPU (1)

Engineer: *Mike Lee*

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 6 of 66


U211B
U211C
RSVD
DDR CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
HDA
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA_CHIPSET
PCIE LANE REVERSED
05/02 1.3G
05/02 1.3G
ASUSTeK COMPUTER INC. NB6
Engineer: Mike Lee
Title : Cantiga-DDR2/PEG(2)
Size Custom
Project Name Z97V
Rev 2.0G
Date: Friday, May 09, 2008
Sheet 7 of 66
0414_1209
http://hobi-elektronika.net



0414_1209

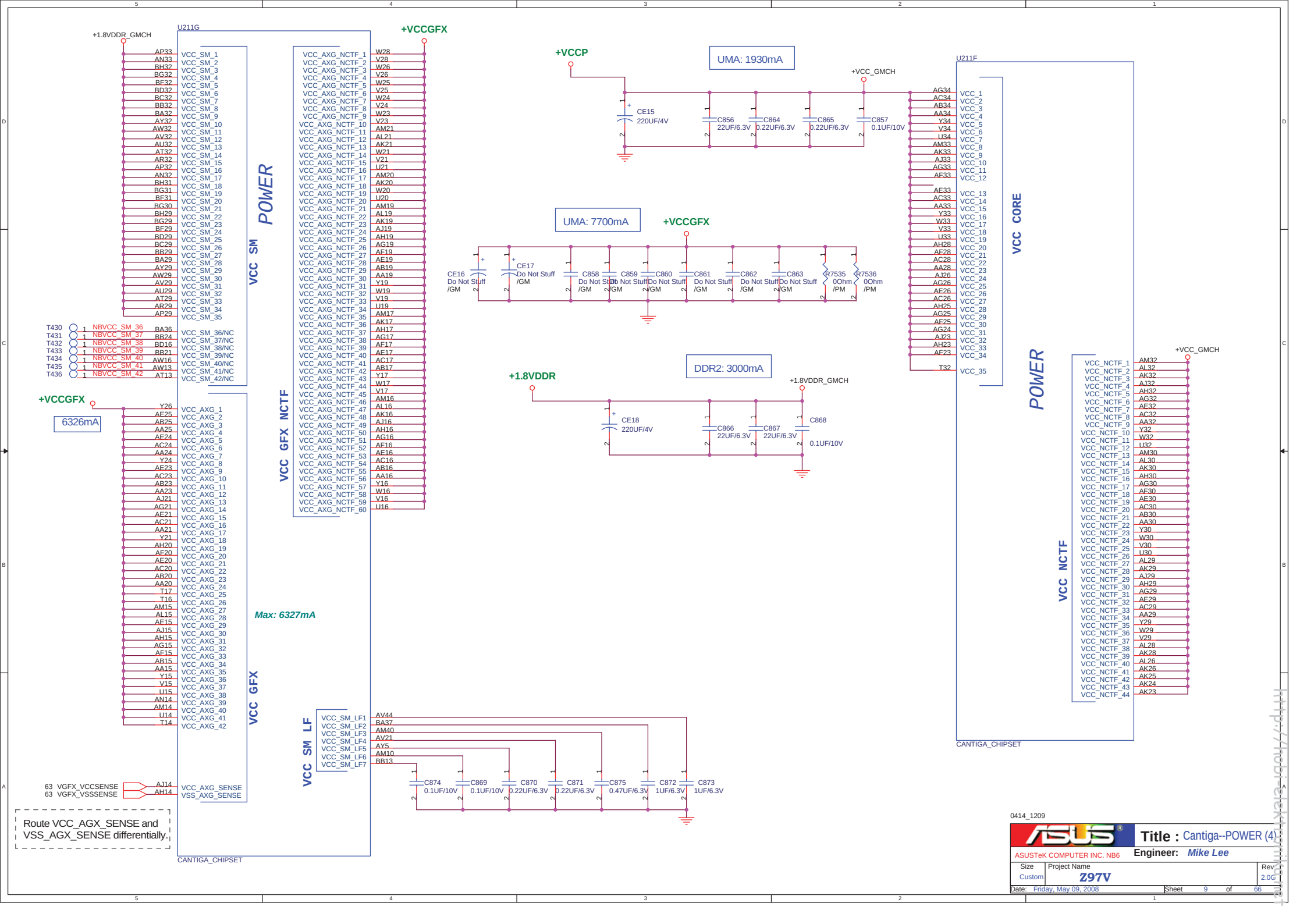
ASUSTeK COMPUTER INC. NB6

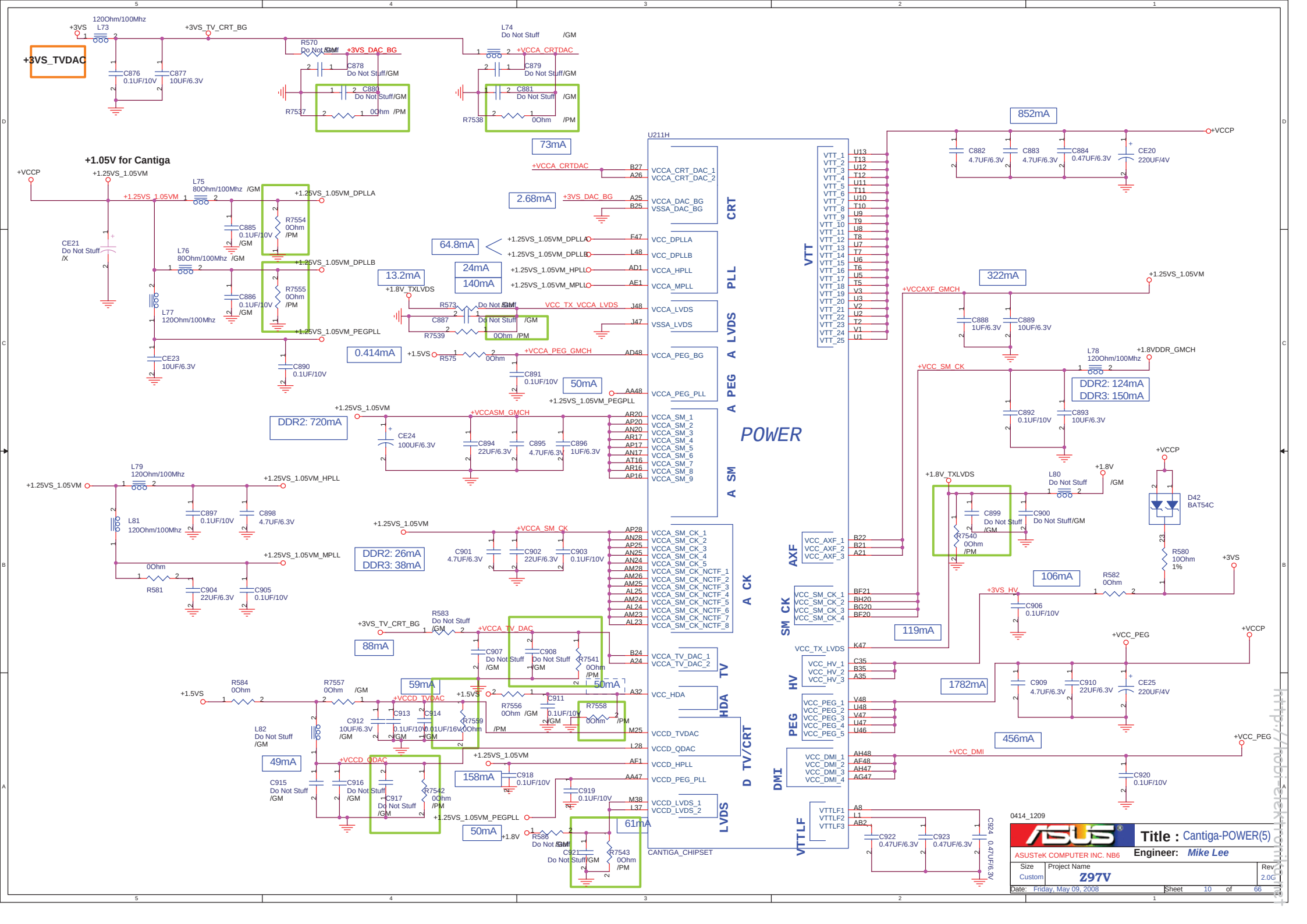
Title : Cantiga--DDR2 bus (2)

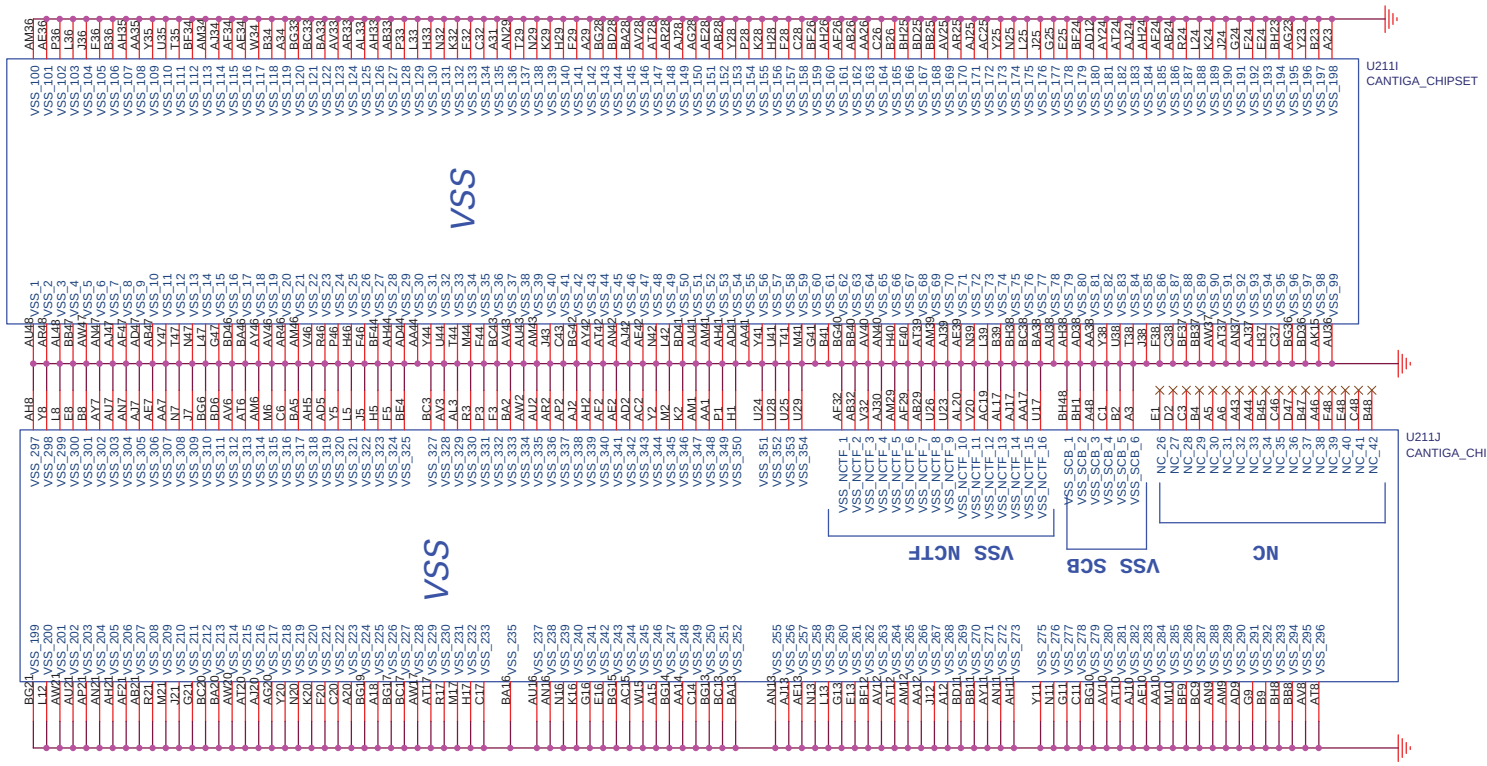
Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 8 of 66


U211G
+1.8VDDR_GMCH
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC SM
POWER
T430 NBVCC_SM_36
T431 NBVCC_SM_37
T432 NBVCC_SM_38
T433 NBVCC_SM_39
T434 NBVCC_SM_40
T435 NBVCC_SM_41
T436 NBVCC_SM_42
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
+VCCGFX
6326mA
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC GFX
Max: 6327mA
63 VGFX_VCCSENSE
63 VGFX_VSSSENSE
VCC_AXG_SENSE
VSS_AXG_SENSE
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.
CANTIGA_CHIPSET
+VCCGFX
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C874 0.1UF/10V
C869 0.1UF/10V
C870 0.22UF/6.3V
C871 0.22UF/6.3V
C875 0.47UF/6.3V
C872 1UF/6.3V
C873 1UF/6.3V
+VCCP
UMA: 1930mA
+VCC_GMCH
CE15 220UF/4V
C856 22UF/6.3V
C864 0.22UF/6.3V
C865 0.22UF/6.3V
C857 0.1UF/10V
UMA: 7700mA
+VCCGFX
CE16 Do Not Stuff /GM
CE17 Do Not Stuff /GM
C858 Do Not Stuff /GM
C859 Do Not Stuff /GM
C860 Do Not Stuff /GM
C861 Do Not Stuff /GM
C862 Do Not Stuff /GM
C863 Do Not Stuff /GM
R7535 0Ohm /PM
R7536 0Ohm /PM
+1.8VDDR
DDR2: 3000mA
+1.8VDDR_GMCH
CE18 220UF/4V
C866 22UF/6.3V
C867 22UF/6.3V
C868 0.1UF/10V
U211F
AG34 VCC_1
AC34 VCC_2
AB34 VCC_3
AA34 VCC_4
Y34 VCC_5
V34 VCC_6
U34 VCC_7
AM33 VCC_8
AK33 VCC_9
AJ33 VCC_10
AG33 VCC_11
AF33 VCC_12
AE33 VCC_13
AC33 VCC_14
AA33 VCC_15
Y33 VCC_16
W33 VCC_17
V33 VCC_18
U33 VCC_19
AH28 VCC_20
AF28 VCC_21
AC28 VCC_22
AA28 VCC_23
AJ26 VCC_24
AG26 VCC_25
AE26 VCC_26
AC26 VCC_27
AH25 VCC_28
AG25 VCC_29
AF25 VCC_30
AG24 VCC_31
AJ23 VCC_32
AH23 VCC_33
AF23 VCC_34
T32 VCC_35
VCC CORE
POWER
+VCC_GMCH
VCC_NCTF_1 AM32
VCC_NCTF_2 AL32
VCC_NCTF_3 AK32
VCC_NCTF_4 AJ32
VCC_NCTF_5 AH32
VCC_NCTF_6 AG32
VCC_NCTF_7 AE32
VCC_NCTF_8 AC32
VCC_NCTF_9 AA32
VCC_NCTF_10 Y32
VCC_NCTF_11 W32
VCC_NCTF_12 U32
VCC_NCTF_13 AM30
VCC_NCTF_14 AL30
VCC_NCTF_15 AK30
VCC_NCTF_16 AH30
VCC_NCTF_17 AG30
VCC_NCTF_18 AF30
VCC_NCTF_19 AE30
VCC_NCTF_20 AC30
VCC_NCTF_21 AB30
VCC_NCTF_22 AA30
VCC_NCTF_23 Y30
VCC_NCTF_24 W30
VCC_NCTF_25 V30
VCC_NCTF_26 U30
VCC_NCTF_27 AL29
VCC_NCTF_28 AK29
VCC_NCTF_29 AJ29
VCC_NCTF_30 AH29
VCC_NCTF_31 AG29
VCC_NCTF_32 AE29
VCC_NCTF_33 AC29
VCC_NCTF_34 AA29
VCC_NCTF_35 Y29
VCC_NCTF_36 W29
VCC_NCTF_37 V29
VCC_NCTF_38 AL28
VCC_NCTF_39 AK28
VCC_NCTF_40 AL26
VCC_NCTF_41 AK26
VCC_NCTF_42 AK25
VCC_NCTF_43 AK24
VCC_NCTF_44 AK23
VCC NCTF
CANTIGA_CHIPSET
0414_1209
Title : Cantiga--POWER (4)
ASUSTeK COMPUTER INC. NB6
Engineer: Mike Lee
Size Custom
Project Name Z97V
Rev 2.0G
Date: Friday, May 09, 2008
Sheet 9 of 66


+3VS_TVDAC
+1.05V for Cantiga
POWER
U211H
CANTIGA_CHIPSET
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
73mA
2.68mA
64.8mA
24mA
140mA
13.2mA
0.414mA
50mA
DDR2: 720mA
DDR2: 26mA
DDR3: 38mA
88mA
59mA
49mA
158mA
50mA
61mA
852mA
322mA
DDR2: 124mA
DDR3: 150mA
106mA
119mA
1782mA
456mA
0414_1209
Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB6
Engineer: Mike Lee
Size: Custom
Project Name: Z97V
Rev: 2.0G
Date: Friday, May 09, 2008
Sheet 10 of 66



7 MCH_CFG_5

R587 Do Not Stuff /X

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

7 MCH_CFG_6

R590 Do Not Stuff /X

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

7 MCH_CFG_7

R592 Do Not Stuff /X

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

7 MCH_CFG_9

R595 2.21KOhm

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

PCIE LANE REVERSED

7 MCH_CFG_16

R596 Do Not Stuff /X

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

7 MCH_CFG_10

R589 Do Not Stuff /X

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

7 MCH_CFG_12

R591 Do Not Stuff /X

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

7 MCH_CFG_13

R594 Do Not Stuff /X

+3VS

R588 Do Not Stuff /X

7 MCH_CFG_19

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

+3VS

R593 Do Not Stuff /X

7 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

0414_1209

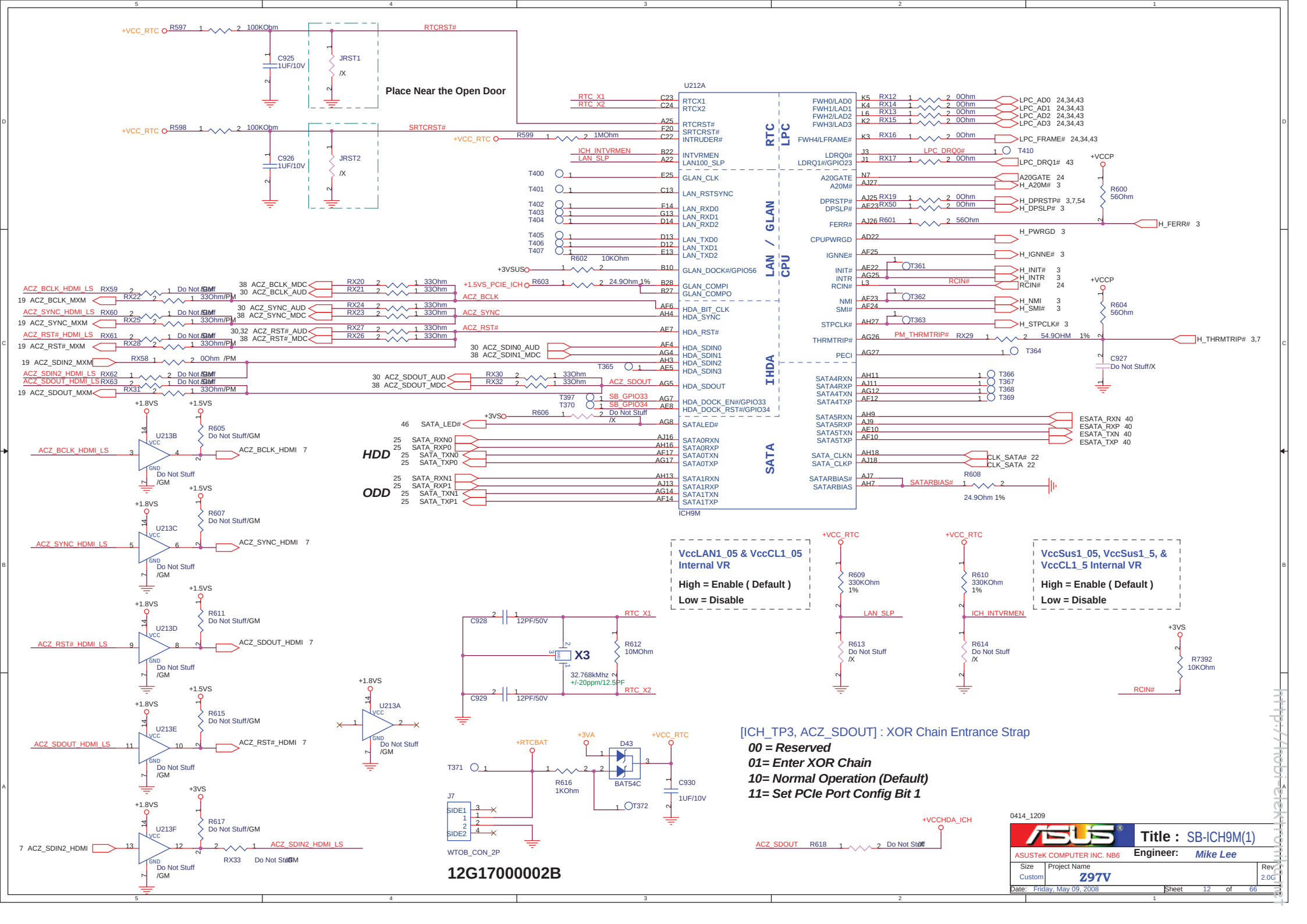
ASUSTeK COMPUTER INC. NB6

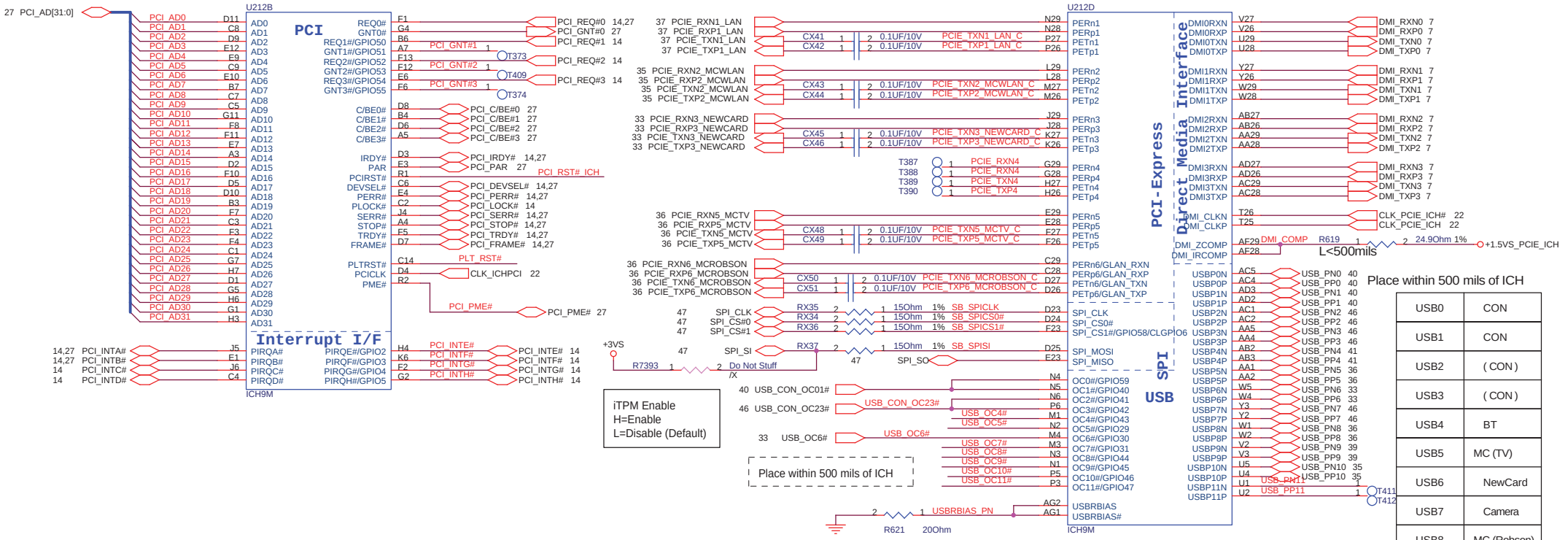
Title : Cantiga-GND

Engineer: *Mike Lee*

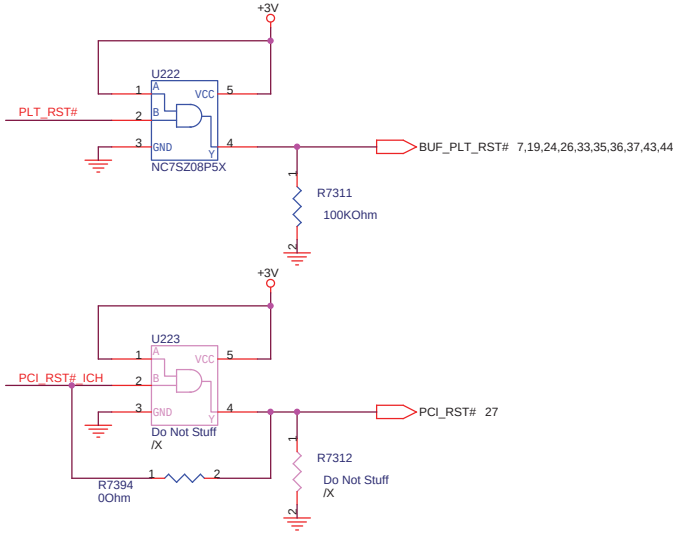
Size	Project Name	Rev
Custom	Z97V	2.0G

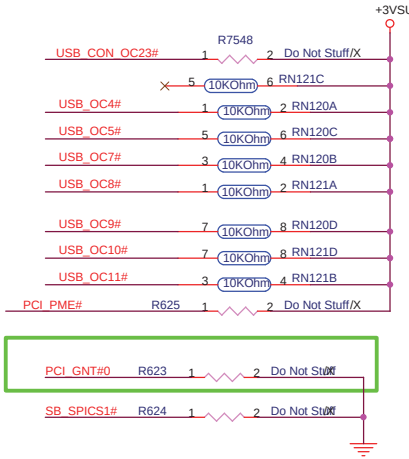
Date: Friday, May 09, 2008 Sheet 11 of 66


Place Near the Open Door
U212A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
HDD
ODD
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable
X3
32.768kMhz
+/-20ppm/12.5PF
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
WTOB_CON_2P
12G17000002B
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB6
Engineer: Mike Lee
Project Name Z97V
Rev 2.0G
Date: Friday, May 09, 2008
Sheet 12 of 66
0414_1209



USB0	CON
USB1	CON
USB2	(CON)
USB3	(CON)
USB4	BT
USB5	MC (TV)
USB6	NewCard
USB7	Camera
USB8	MC (Robson)
USB9	FingerPrint
USB10	MC (WLAN)
USB11	





ICH9 Boot BIOS select

		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

0414_1209

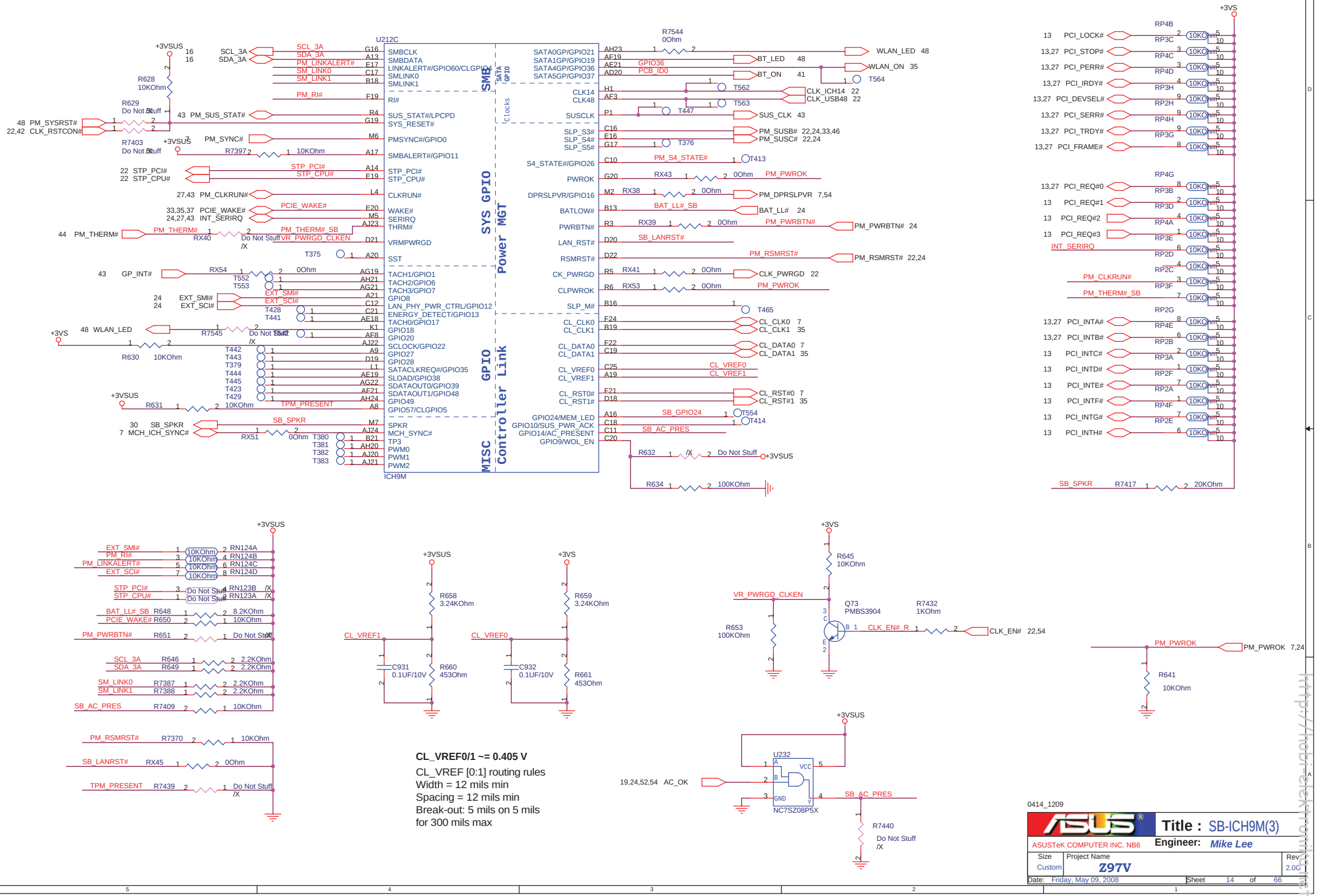
Title : SB-ICH9M(2)

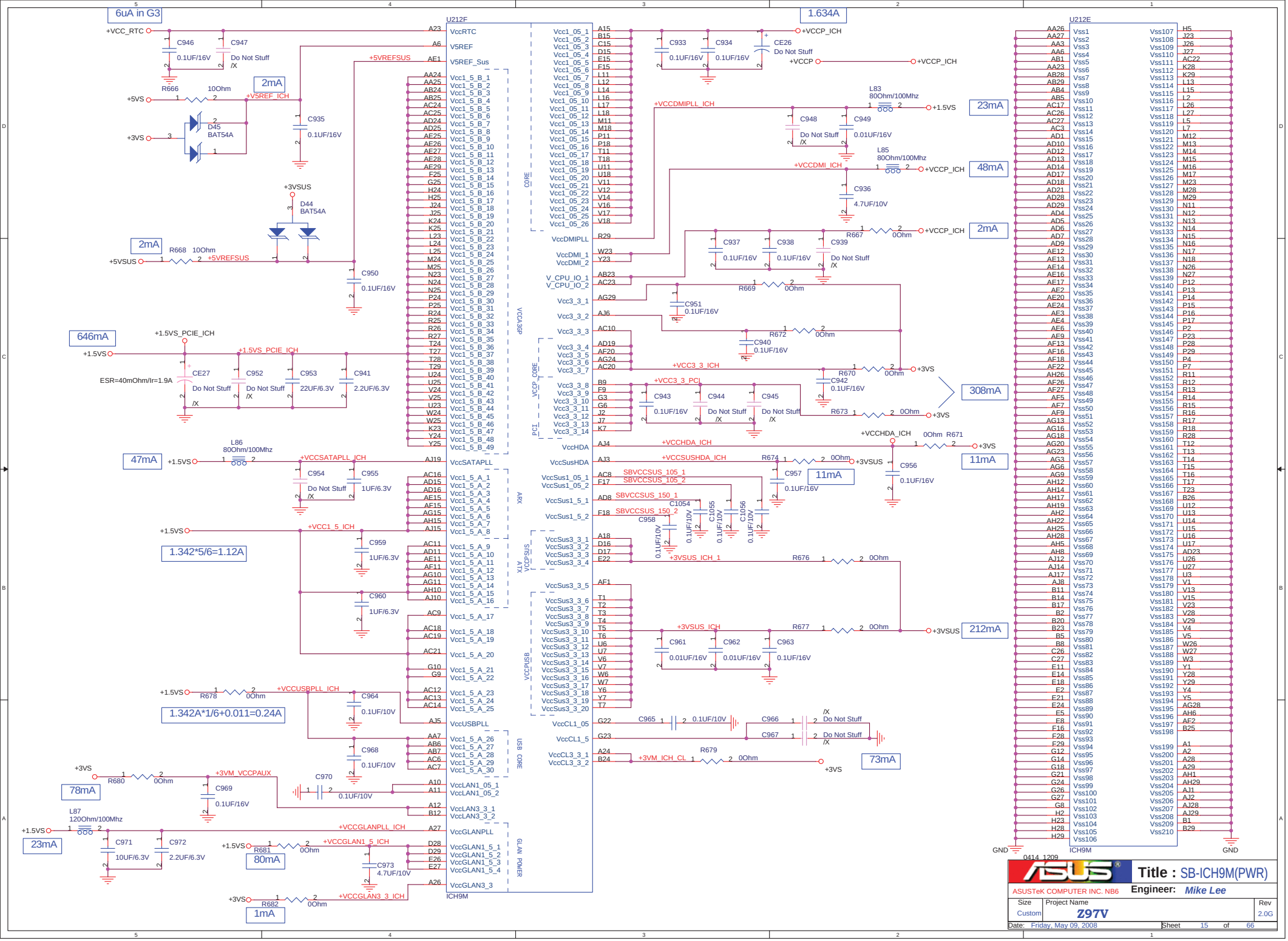
ASUSTeK COMPUTER INC. NB6

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 13 of 66


U212C
ICH9M
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO5
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SMB
SATA GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
+3VSUS
+3VS
SCL_3A
SDA_3A
PM_LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
PM_SUS_STAT#
PM_SYNC#
STP_PCI#
STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THERM#
PM_THERM#_SB
VR_PWRGD_CLKEN
GP_INT#
EXT_SMI#
EXT_SCI#
WLAN_LED
TPM_PRESENT
SB_SPKR
MCH_ICH_SYNC#
R628 10KOhm
R629 Do Not Stuff /X
R7403 Do Not Stuff /X
R7397 10KOhm
RX40 Do Not Stuff /X
RX54 0Ohm
R7545 Do Not Stuff /X
R630 10KOhm
R631 10KOhm
RX51 0Ohm
R7544 0Ohm
WLAN_LED 48
BT_LED 48
WLAN_ON 35
BT_ON 41
GPIO36
PCB_ID0
T562
T563
T564
T447
CLK_ICH14 22
CLK_USB48 22
SUS_CLK 43
T376
PM_SUSB# 22,24,33,46
PM_SUSC# 22,24
PM_S4_STATE#
T413
RX43 0Ohm
PM_PWROK
RX38 0Ohm
PM_DPRSLPVR 7,54
BAT_LL#_SB
BAT_LL# 24
RX39 0Ohm
PM_PWRBTN#
PM_PWRBTN# 24
SB_LANRST#
PM_RSMRST#
PM_RSMRST# 22,24
RX41 0Ohm
CLK_PWRGD 22
RX53 0Ohm
T465
CL_CLK0 7
CL_CLK1 35
CL_DATA0 7
CL_DATA1 35
CL_VREF0
CL_VREF1
CL_RST#0 7
CL_RST#1 35
SB_GPIO24
T554
T414
SB_AC_PRES
R632 /X Do Not Stuff
R634 100KOhm
RP4B
RP3C
RP4C
RP4D
RP3H
RP2H
RP4H
RP3G
RP4G
RP3B
RP3D
RP4A
RP3E
RP2D
RP2C
RP3F
RP2G
RP4E
RP2B
RP3A
RP2F
RP2A
RP4F
RP2E
PCI_LOCK#
PCI_STOP#
PCI_PERR#
PCI_IRDY#
PCI_DEVSEL#
PCI_SERR#
PCI_TRDY#
PCI_FRAME#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_INTE#
PCI_INTF#
PCI_INTG#
PCI_INTH#
R7417 20KOhm
RN124A
RN124B
RN124C
RN124D
RN123B /X
RN123A /X
R648 8.2KOhm
R650 10KOhm
R651 Do Not Stuff /X
R646 2.2KOhm
R649 2.2KOhm
R7387 2.2KOhm
R7388 2.2KOhm
R7409 10KOhm
R7370 10KOhm
RX45 0Ohm
R7439 Do Not Stuff /X
R658 3.24KOhm
R659 3.24KOhm
C931 0.1UF/10V
C932 0.1UF/10V
R660 453Ohm
R661 453Ohm
R645 10KOhm
R653 100KOhm
Q73 PMBS3904
R7432 1KOhm
CLK_EN# 22,54
R641 10KOhm
U232
NC7SZ08P5X
AC_OK 19,24,52,54
R7440 Do Not Stuff /X
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils
for 300 mils max
0414_1209
Title : SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB6
Engineer: Mike Lee
Size Custom
Project Name Z97V
Rev 2.0G
Date: Friday, May 09, 2008
Sheet 14 of 66


6uA in G3
1.634A
U212F
U212E
+VCC_RTC
+5VREFSUS
+5VREF_ICH
+3VSUS
+1.5VS_PCIE_ICH
+VCCSATAPLL_ICH
+VCC1_5_ICH
+VCCUSBPLL_ICH
+3VM_VCCPAUX
+VCCGLANPLL_ICH
+VCCGLAN1_5_ICH
+VCCGLAN3_3_ICH
+VCCP_ICH
+VCCDMIPLL_ICH
+VCCDMI_ICH
+VCC3_3_ICH
+VCC3_3_PCI
+VCCHDA_ICH
+VCCSUSHDA_ICH
+3VSUS_ICH_1
+3VSUS_ICH
+3VM_ICH_CL
2mA
646mA
47mA
1.342*5/6=1.12A
1.342A*1/6+0.011=0.24A
78mA
23mA
80mA
1mA
11mA
308mA
48mA
212mA
73mA
ICH9M
0414_1209
Title : SB-ICH9M(PWR)
ASUSTeK COMPUTER INC. NB6
Engineer: Mike Lee
Project Name Z97V
Date: Friday, May 09, 2008
Sheet 15 of 66
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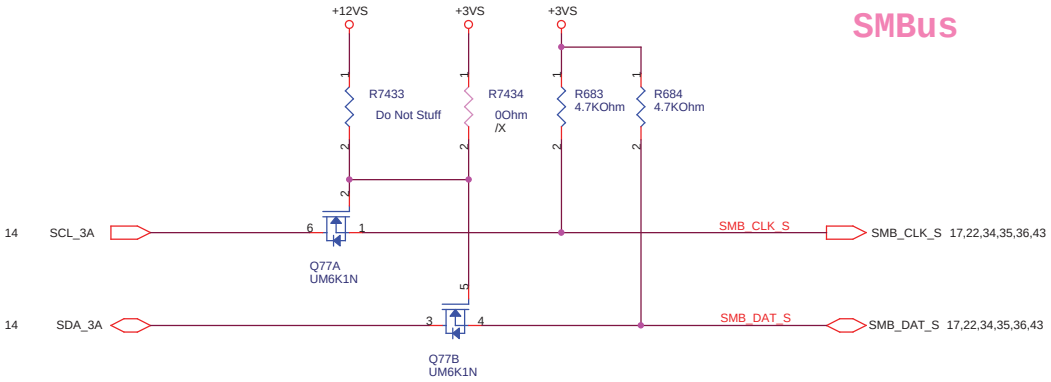
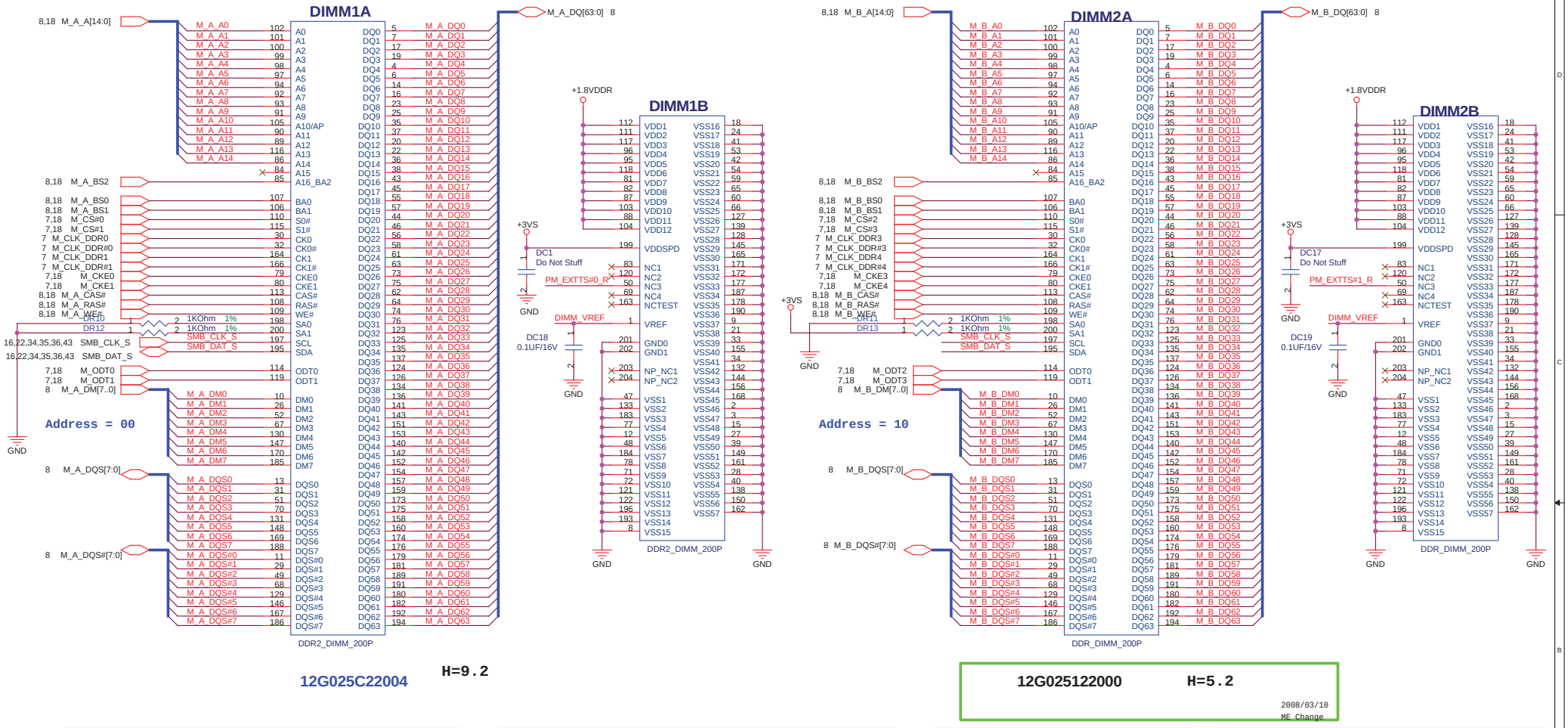
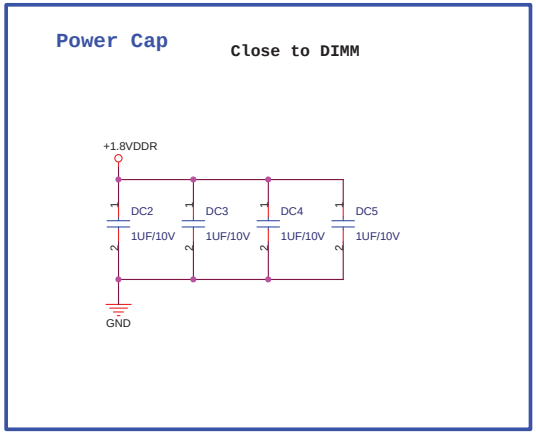
SMBus

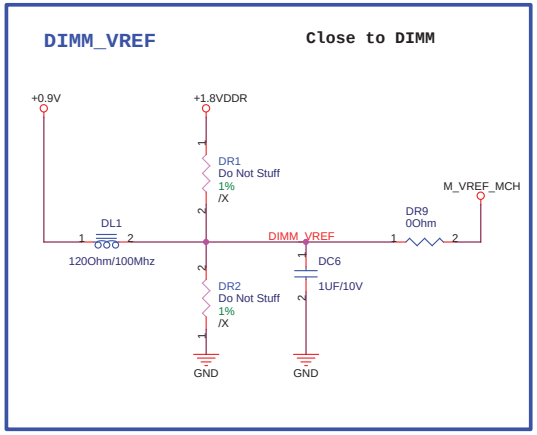


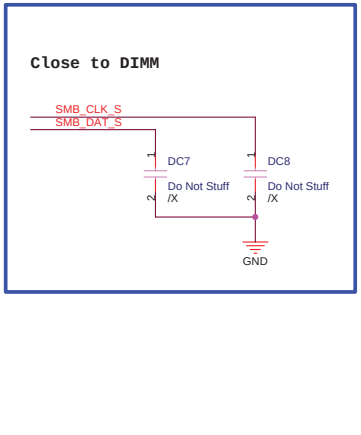
0414_1209

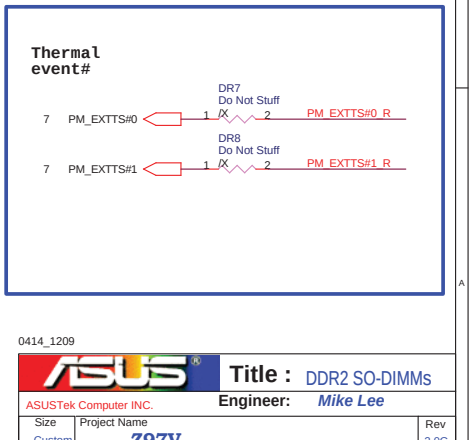
ASUSTeK COMPUTER INC. NB6	Title : ICH9M-Other	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 16 of 66	











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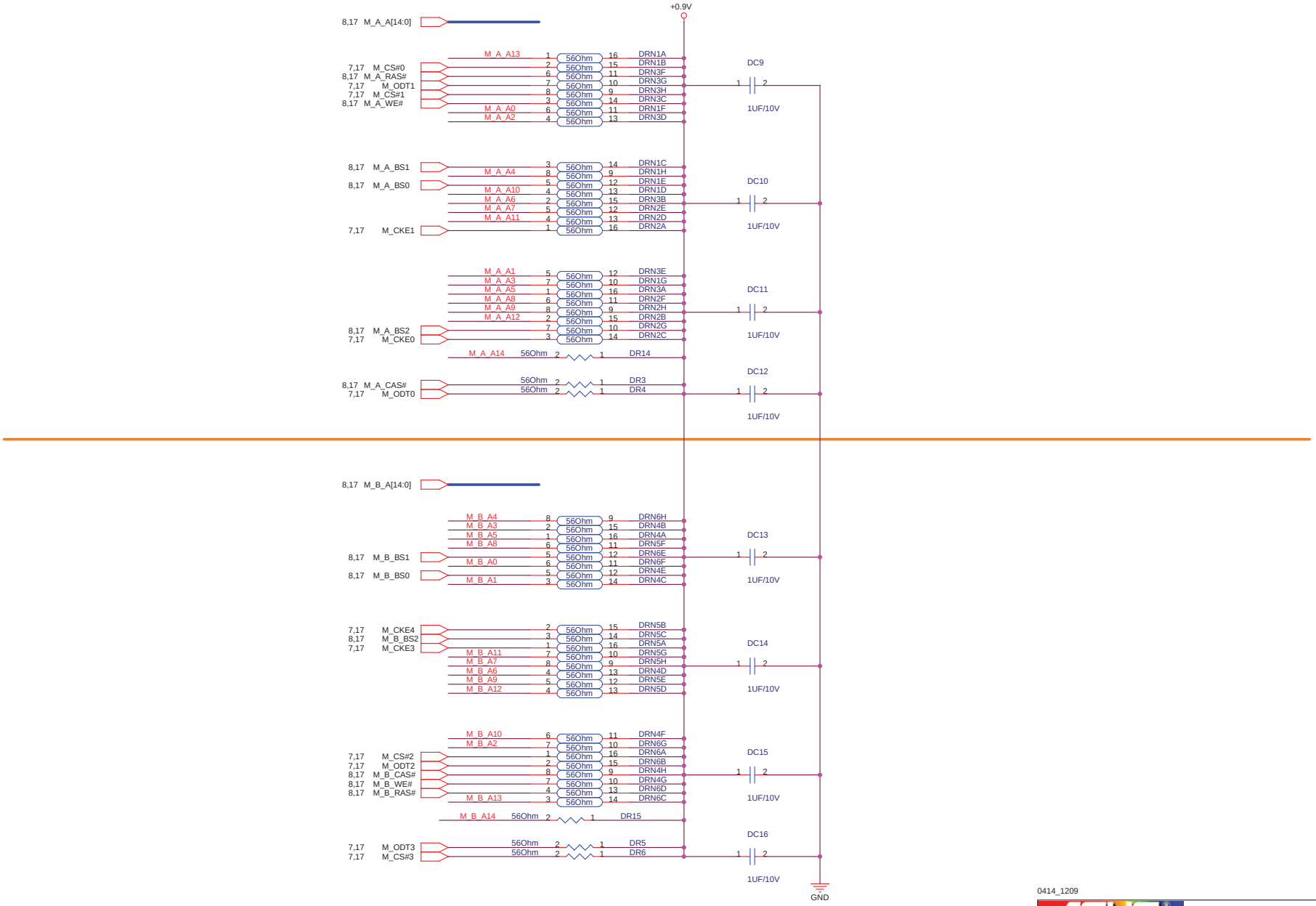
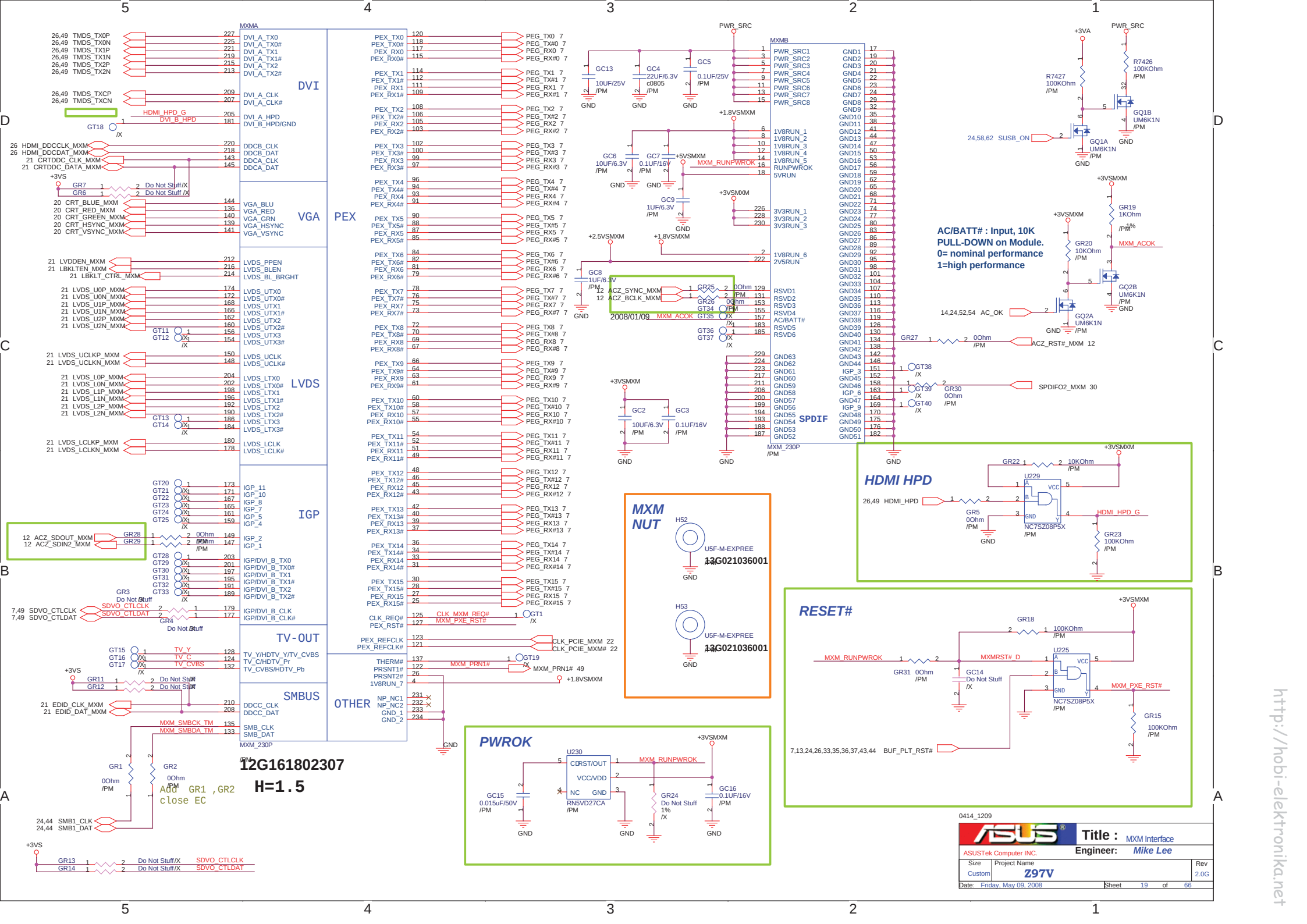
ASUSTek Computer INC.	Title : DDR2 SO-DIMMs	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 17 of 66	



0414_1209

ASUSTek Computer INC.	Title : DDR2 TERMINATION	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 18 of 66	


MXMA
DVI
VGA
PEX
LVDS
IGP
TV-OUT
SMBUS
OTHER
MXM_230P
12G161802307
H=1.5
Add GR1 ,GR2 close EC
MXMB
SPDIF
MXM_230P
AC/BATT# : Input, 10K PULL-DOWN on Module.
0= nominal performance
1=high performance
HDMI HPD
MXM NUT
H52
H53
U5F-M-EXPREE
13G021036001
RESET#
PWROK
U230
U225
U229
Title : MXM Interface
ASUSTek Computer INC.
Engineer: Mike Lee
Size Custom
Project Name Z97V
Rev 2.0G
Date: Friday, May 09, 2008
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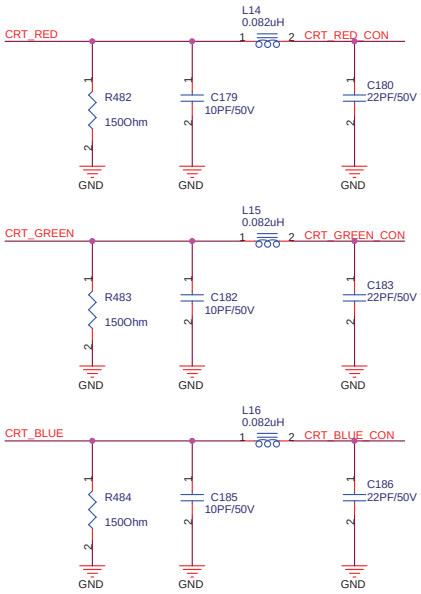
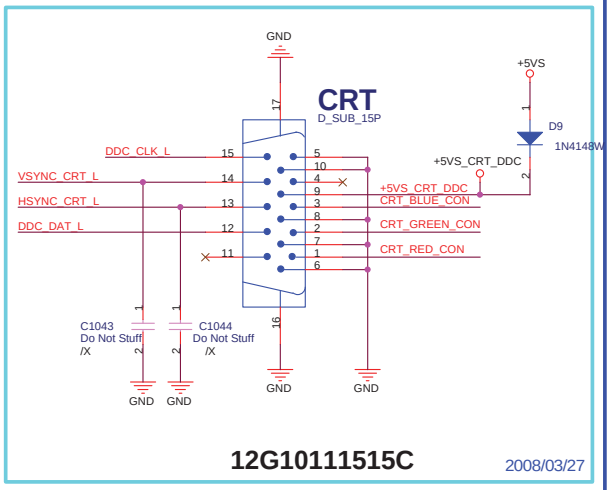
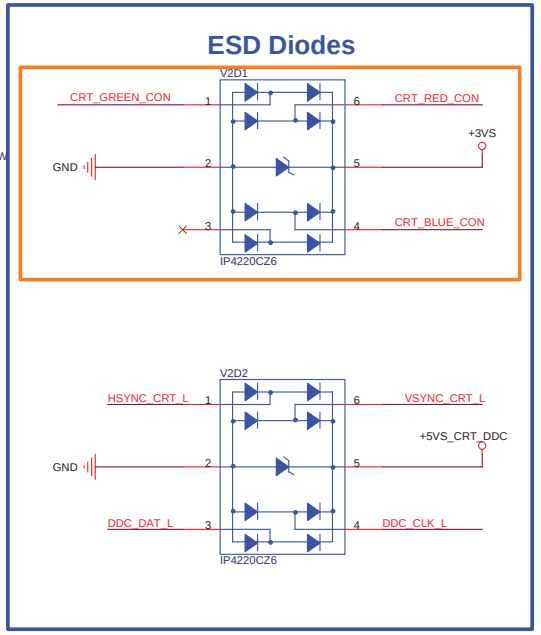
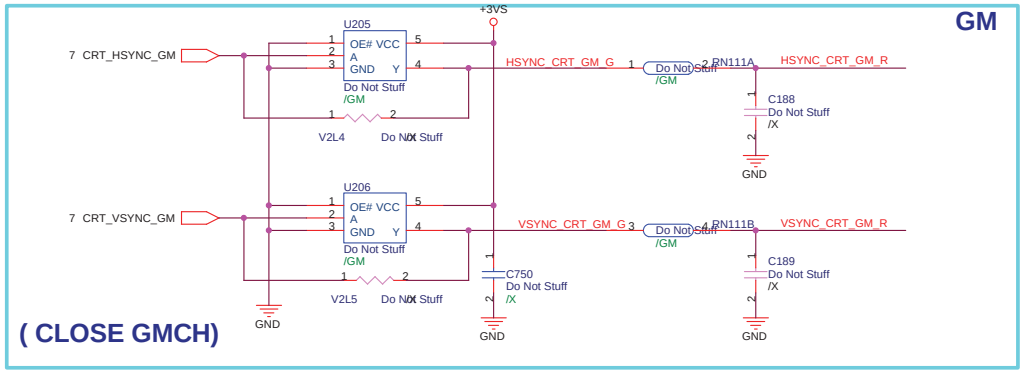
0414_1209
http://hobi-elektronika.net

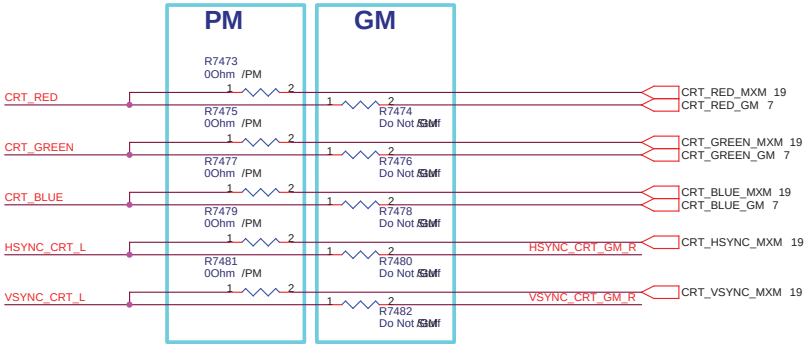


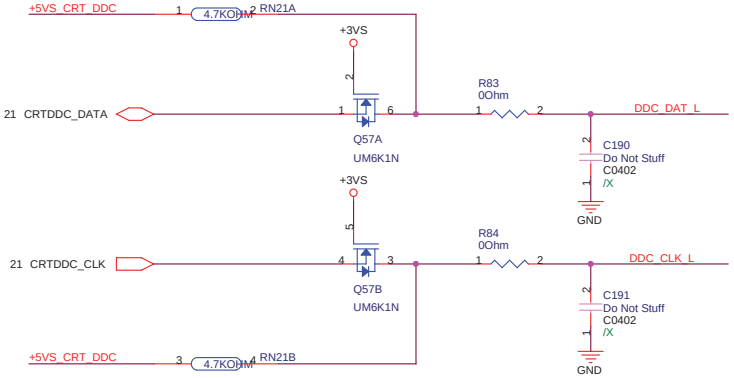


CRT Connector







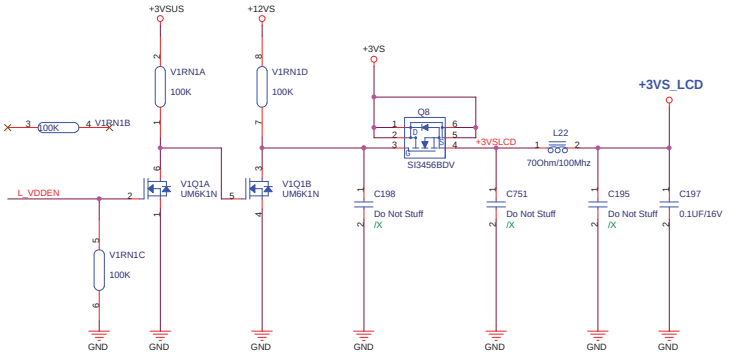


0414_1209

ASUSTek Computer INC.	Title : CRT Conn & MUX	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 20 of 66	

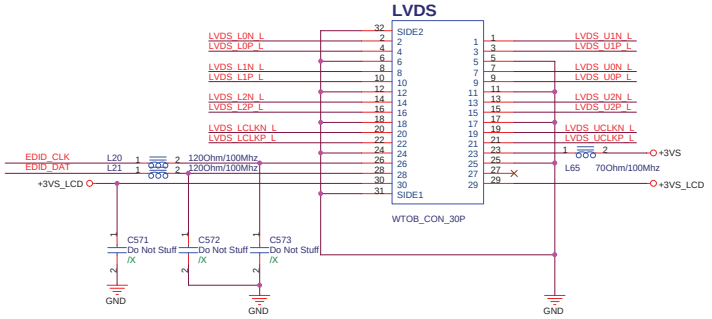
LCD Power

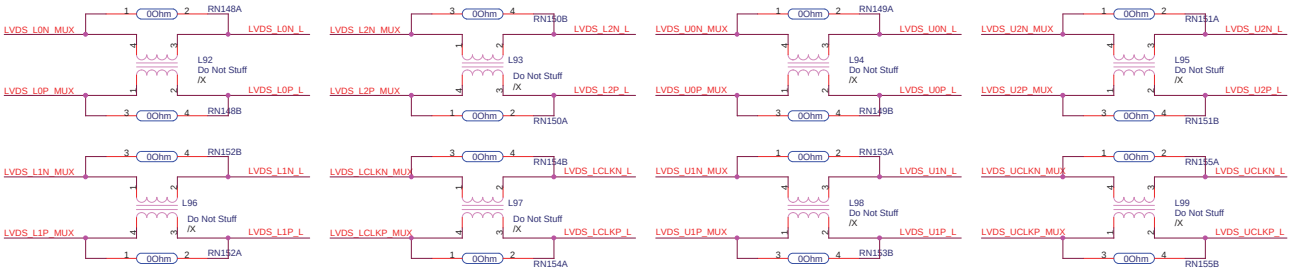
3-3.6V S0-S1M:410 mA(500 mA Max.)



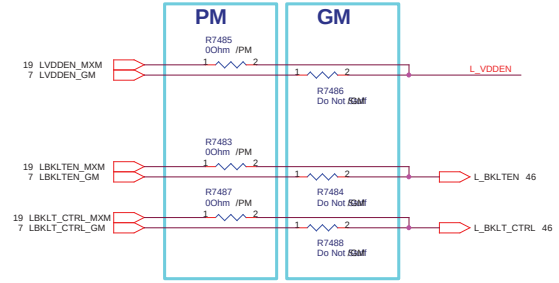
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Connector

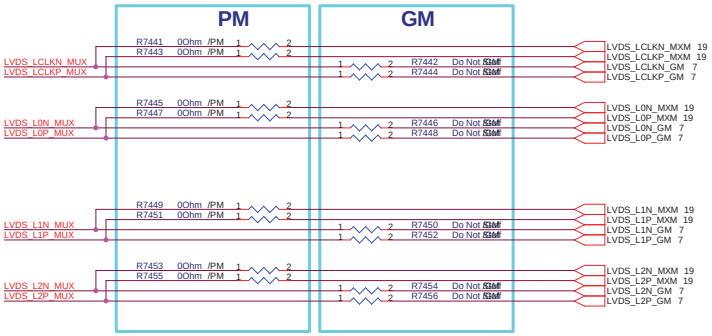


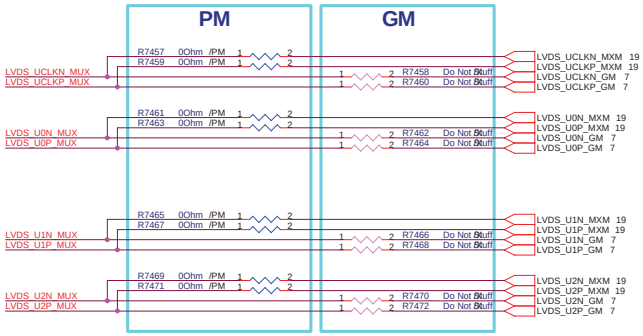


LCD VCC / BL SIGNAL

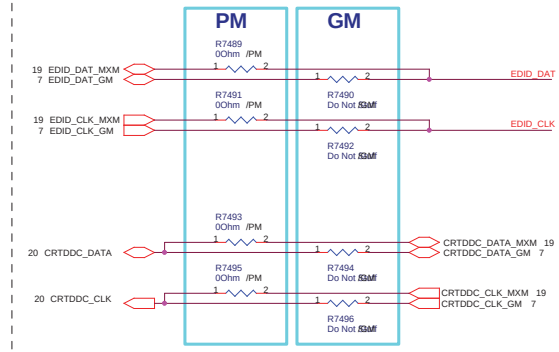


LCD IMAGE SIGNAL





LCD EDID / CRT DDC SIGNAL

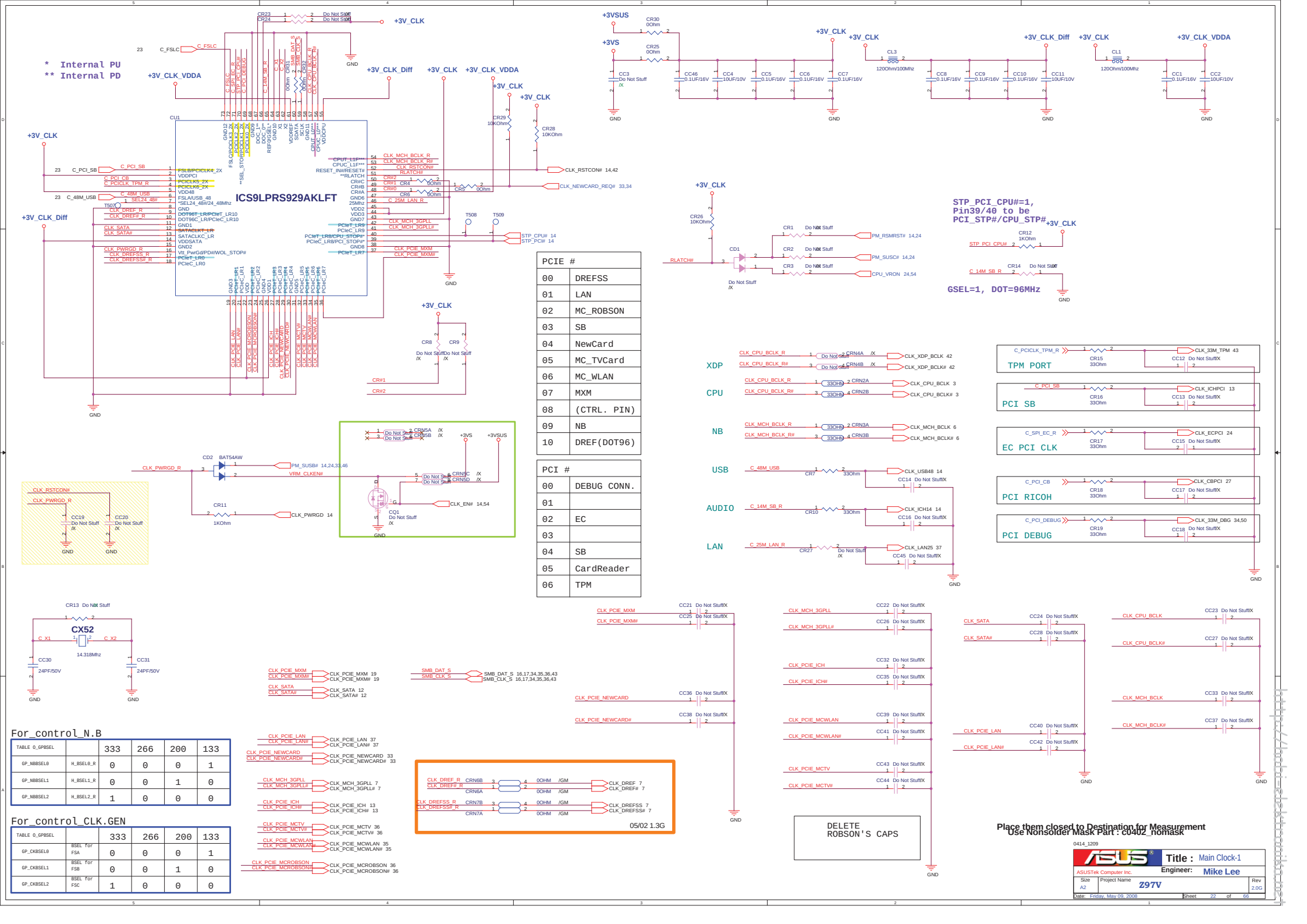


LOWER CHANNEL

UPPER CHANNEL

0414_1209

ASUSTek Computer INC.	Title : LVDS Conn & MUX.	
	Engineer: Mike Lee	
Size: C	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 21 of 66	



PCIE #	
00	DREFSS
01	LAN
02	MC_ROBSON
03	SB
04	NewCard
05	MC_TVCard
06	MC_WLAN
07	MXM
08	(CTRL. PIN)
09	NB
10	DREF(DOT96)

PCI #	
00	DEBUG CONN.
01	
02	EC
03	
04	SB
05	CardReader
06	TPM

For_control_N.B

TABLE 0_GPBSEL		333	266	200	133
GP_NBBSEL0	H_BSEL0_R	0	0	0	1
GP_NBBSEL1	H_BSEL1_R	0	0	1	0
GP_NBBSEL2	H_BSEL2_R	1	0	0	0

For_control_CLK.GEN

TABLE 0_GPBSEL		333	266	200	133
GP_CKBSEL0	BSEL for FSA	0	0	0	1
GP_CKBSEL1	BSEL for FSB	0	0	1	0
GP_CKBSEL2	BSEL for FSC	1	0	0	0

Title :	Main Clock-1
ASUSTek Computer Inc.	Engineer: Mike Lee
Size: A2	Project Name: Z97V
Rev: 2.0G	
Date: Friday, May 09, 2008	Sheet 22 of 66

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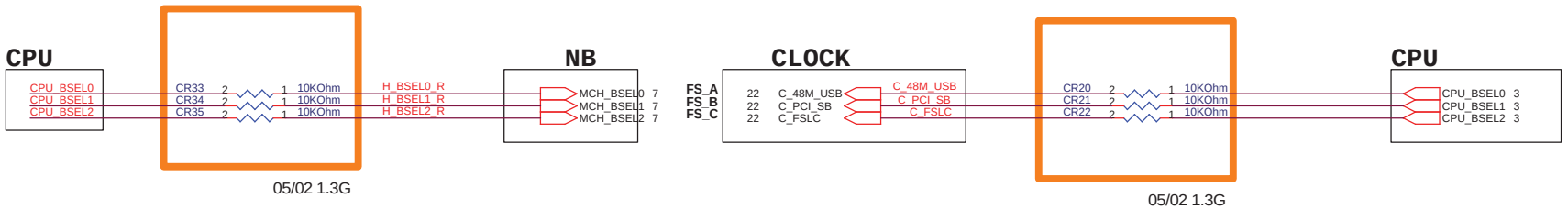


CLK Trapped by CPU's BSEL

HBSEL2	HBSEL1	HBSEL0	FSB
0	0	1	133MHz
0	1	0	200MHz
0	0	0	266MHz
1	0	0	333MHz

0414_1209

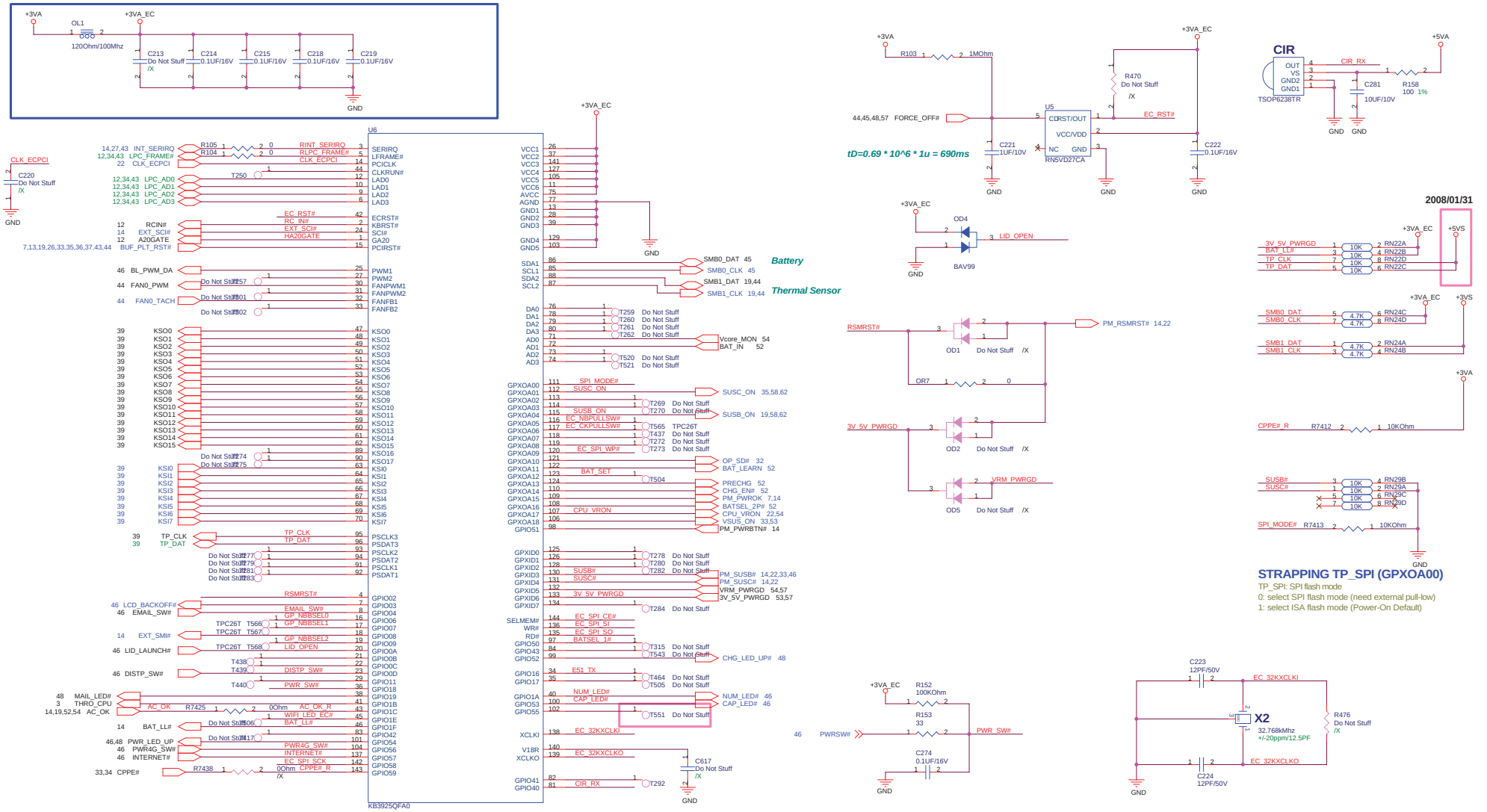
ASUSTek Computer Inc.

Title : Main Clock-2

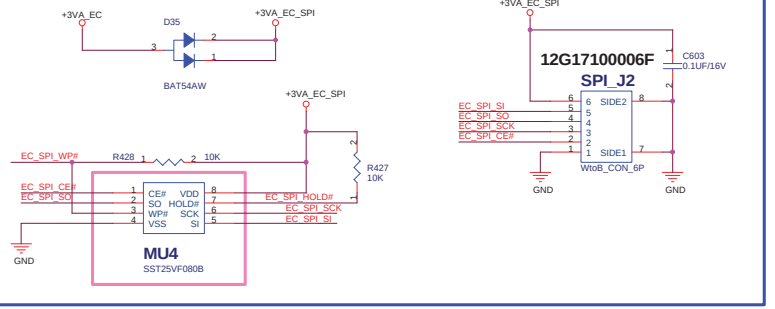
Engineer: Mike Lee

Size	Project Name	Rev
A3	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 23 of 66



SPI Flash ROM



0414_1209

ASUSTek Computer Inc.

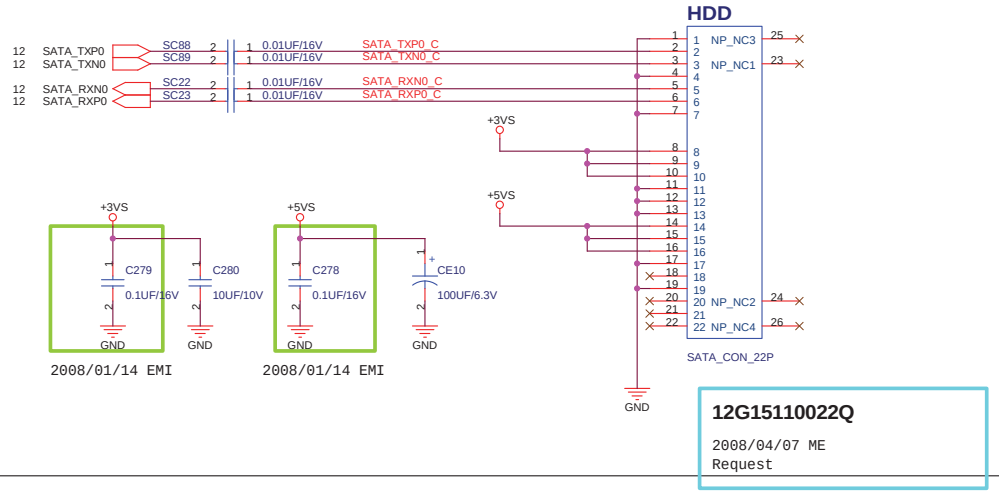
Title : EC-ENE3925

Engineer: Tony Kao

Size	Project Name	Rev
C	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 24 of 66

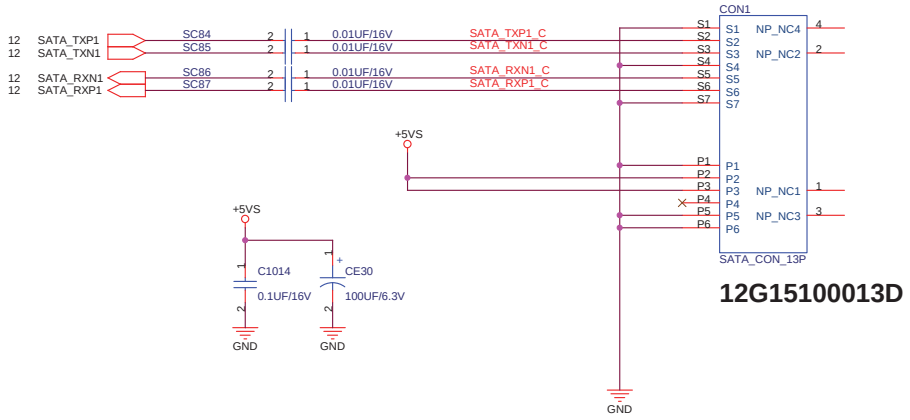
SATA HDD Connector



12G15110022Q

2008/04/07 ME
Request

SATA ODD Connector

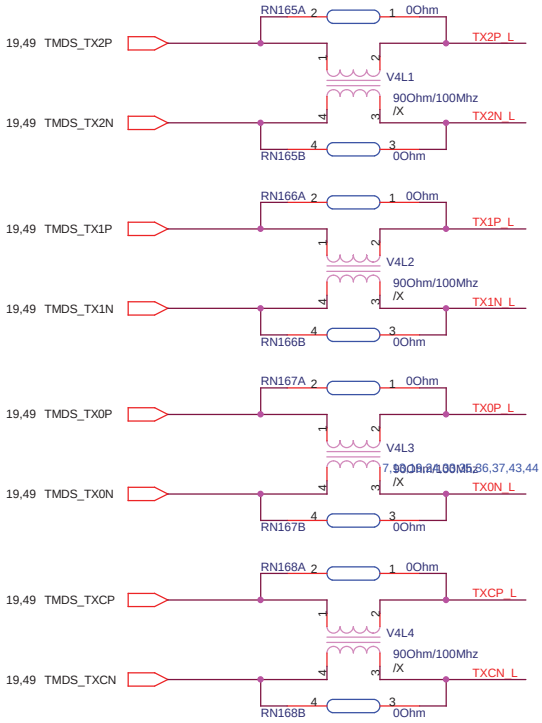


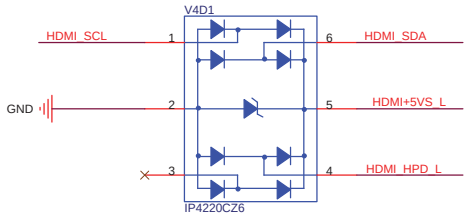
12G15100013D

0414_1209

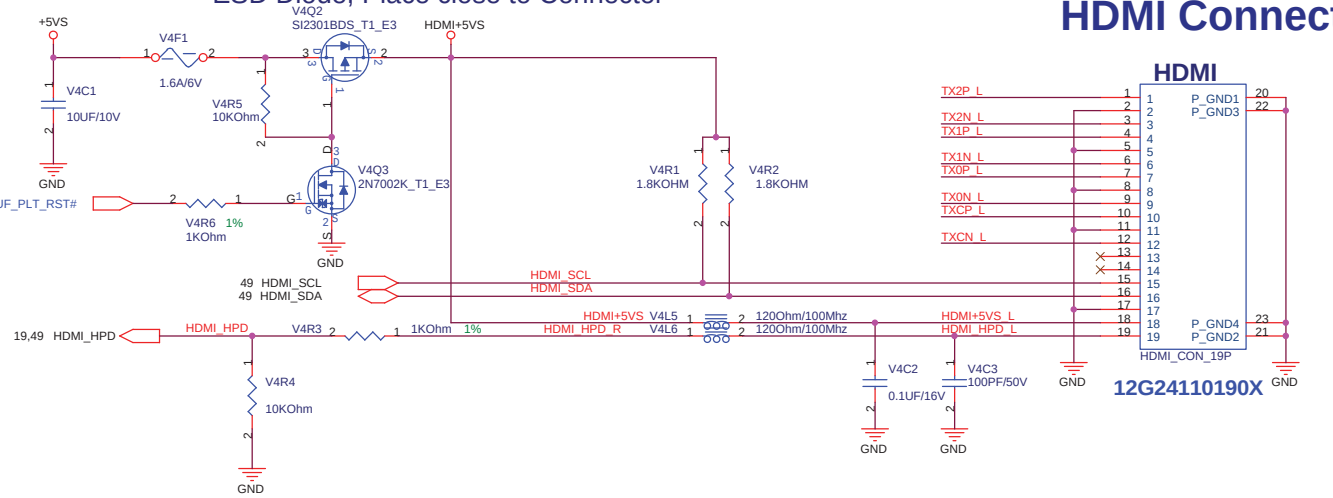
ASUSTek Computer INC.	Title : ODD Connector	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 25 of 66	

Choke : TDK ACM2012 prefered



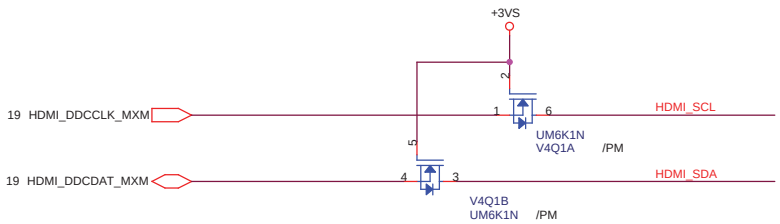


ESD Diode, Place close to Connector



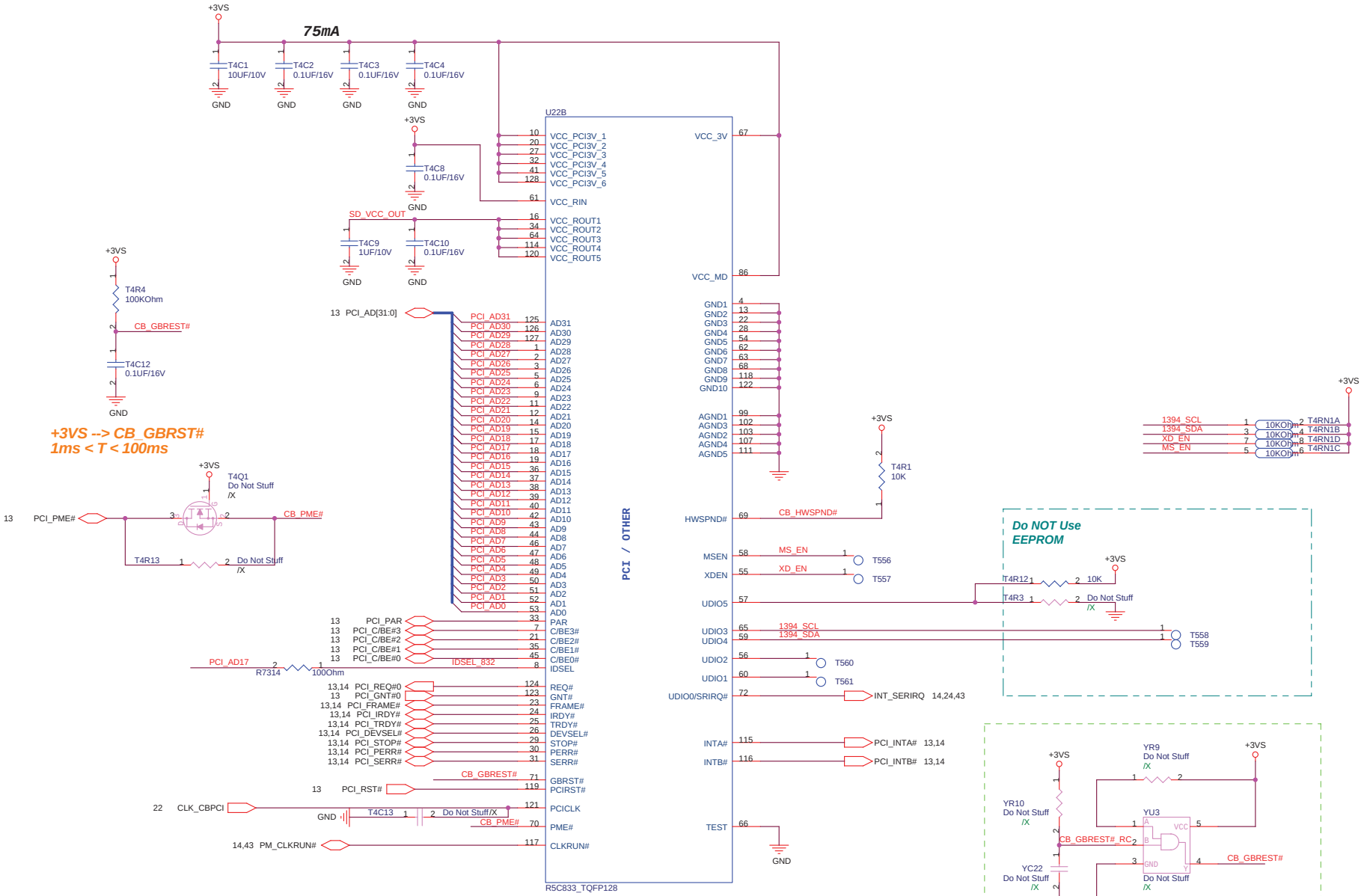
HDMI Connector

PM



0414_1209

ASUSTek Computer INC.	Title : HDMI Connector	
	Engineer: Mike Lee	
Size: A3	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 26 of 66	



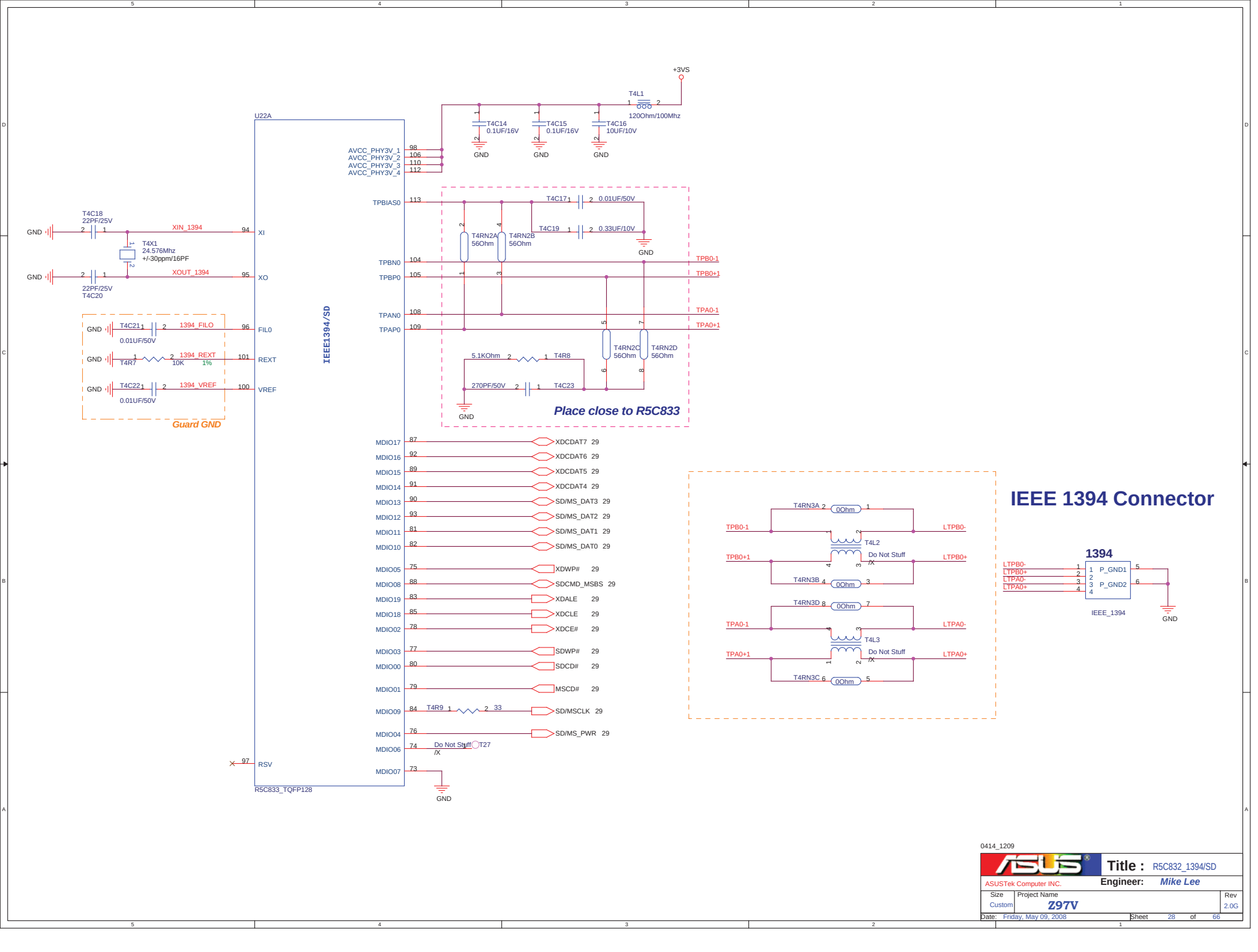
0414_1209

Title : R5C833_PCI

ASUSTek Computer INC. **Engineer:** *Mike Lee*

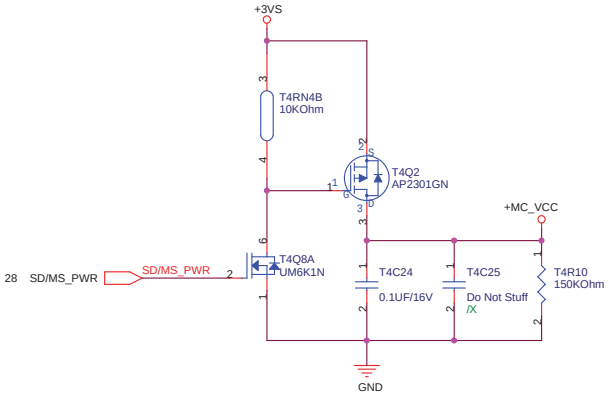
Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 27 of 66

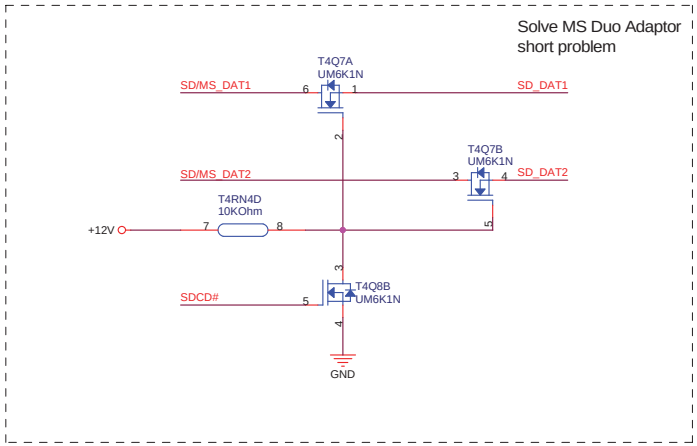


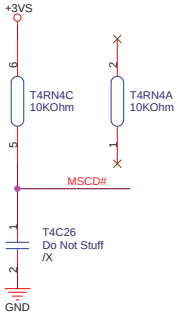
0414_1209

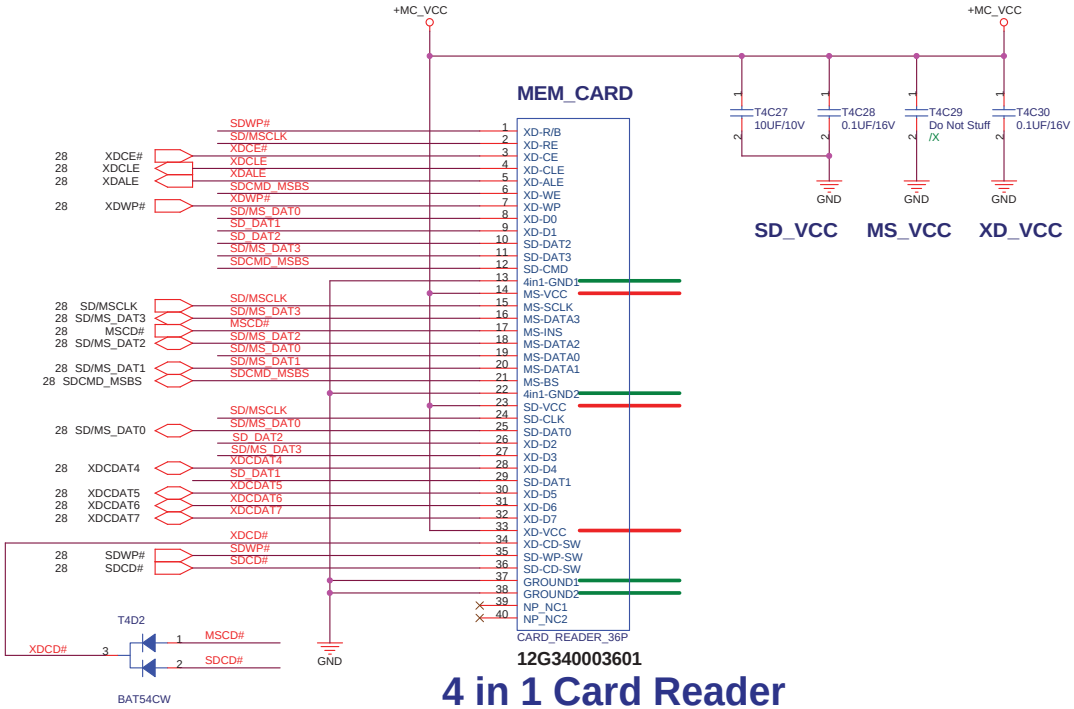
ASUSTek Computer INC.	Title : R5C832_1394/SD	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 28 of 66	



Card Reader Power Switcher





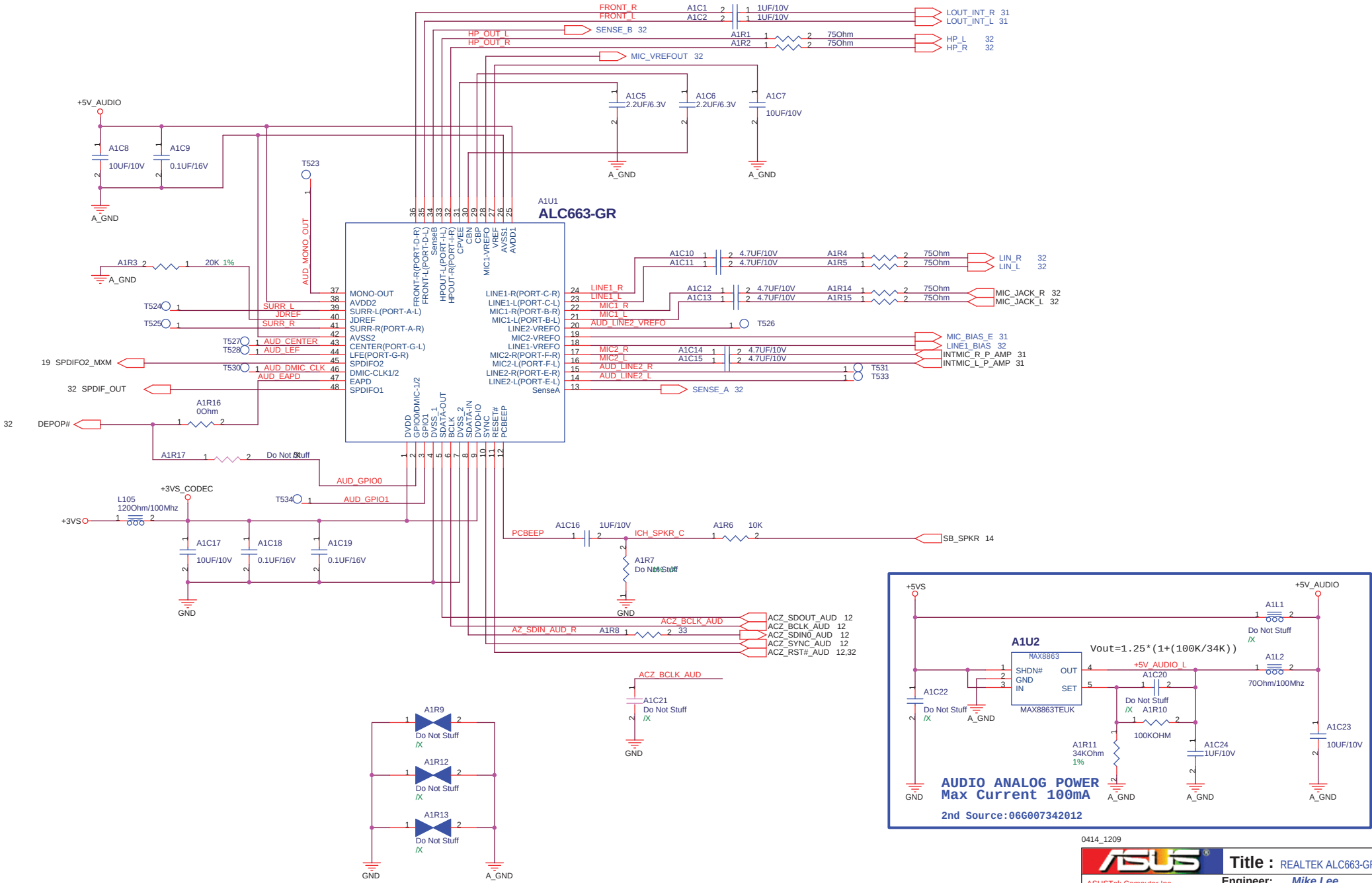


12G340003601

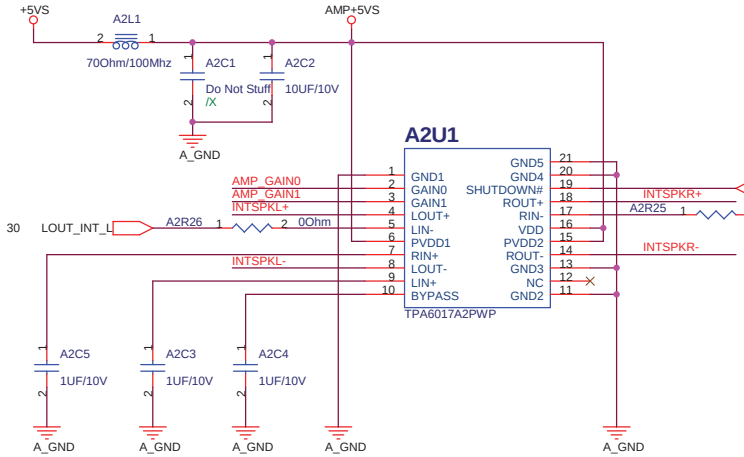
4 in 1 Card Reader

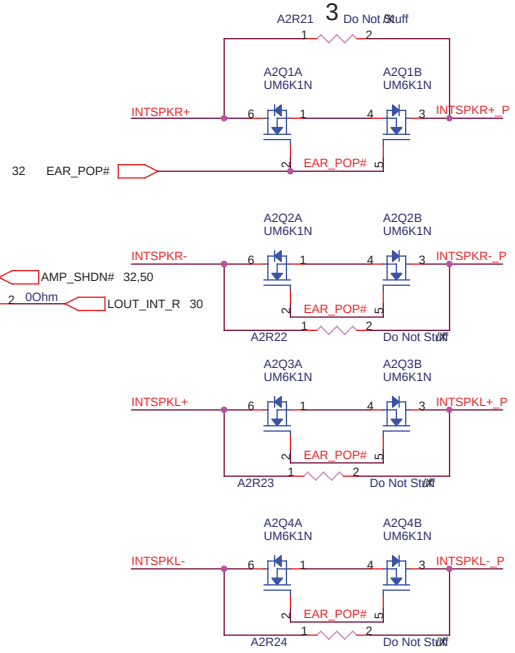
0414_1209

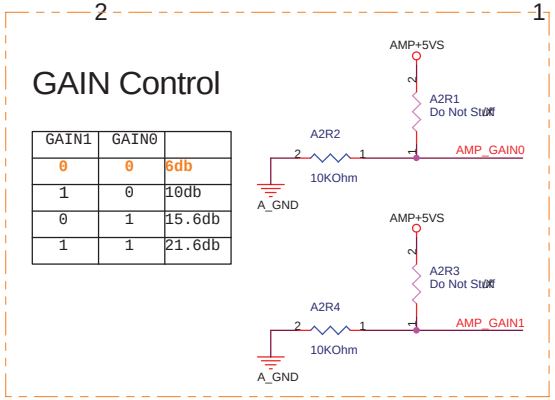
ASUSTek Computer INC.	Title : 4 in 1 Card Reader	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 29 of 66	

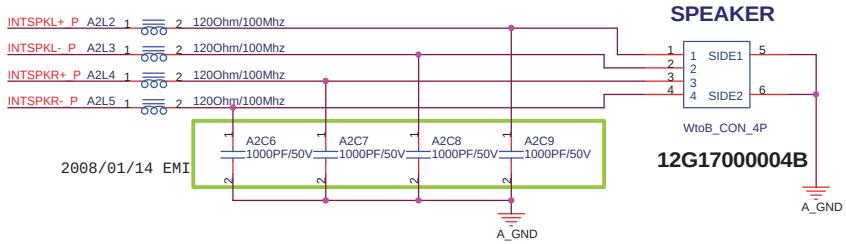


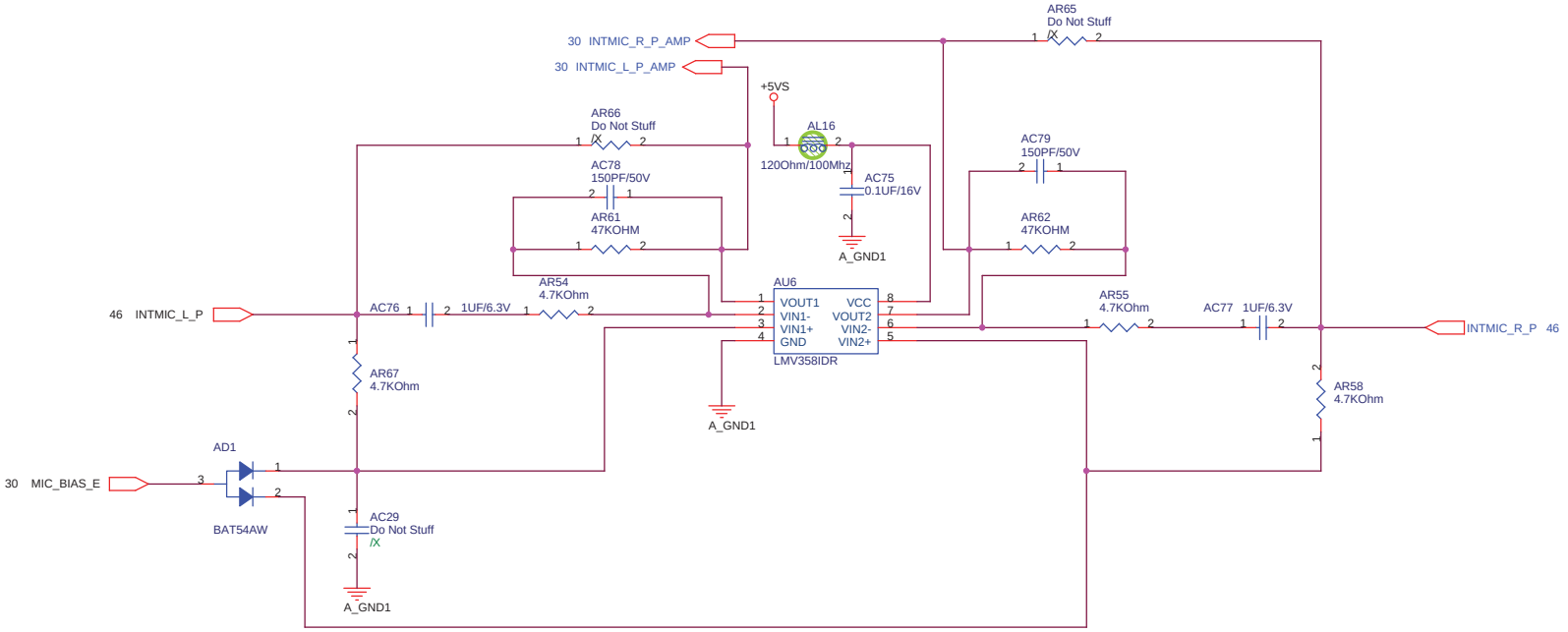
Audio Amp.

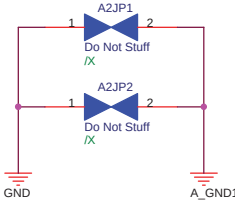












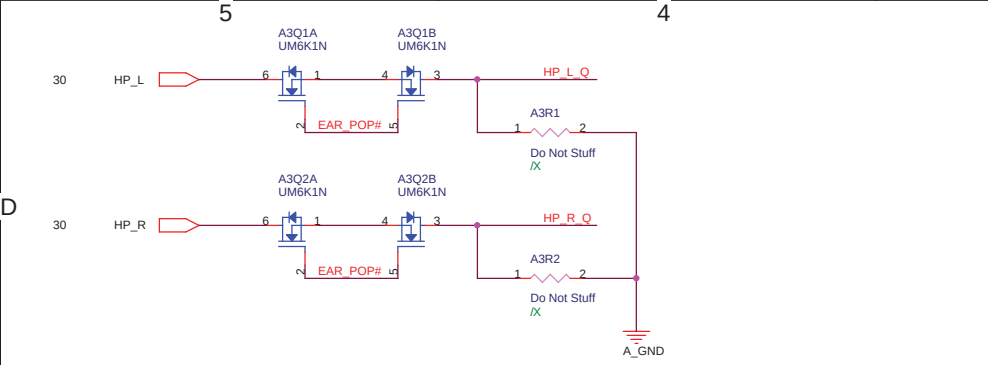
Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz

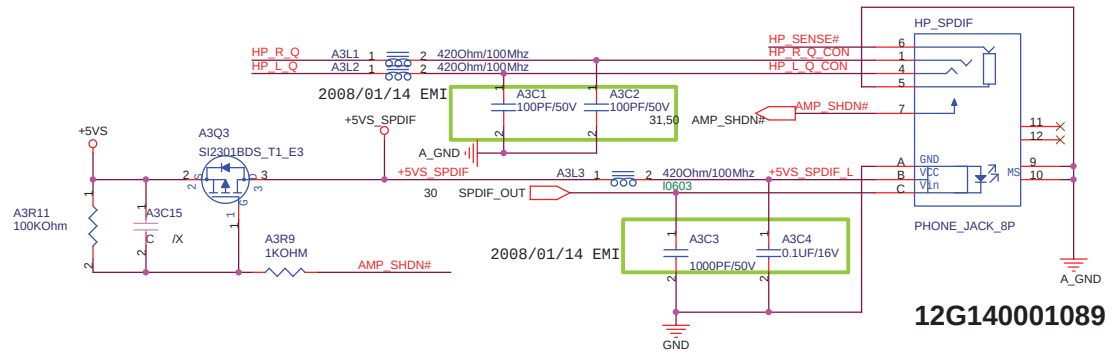
Place Near INTMIC Connector

0414_1209

ASUSTek Computer INC.	Title : Speaker / Mic PreAmp	
	Engineer: Mike Lee	
Size: A3	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 31 of 66	

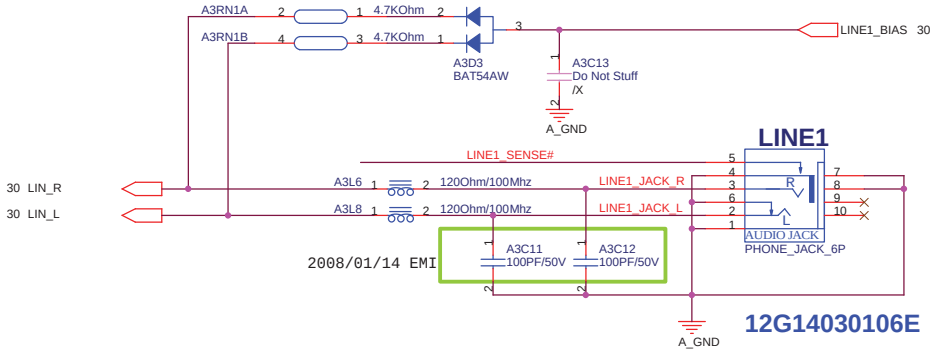


Headphone & S/PDIF Jack



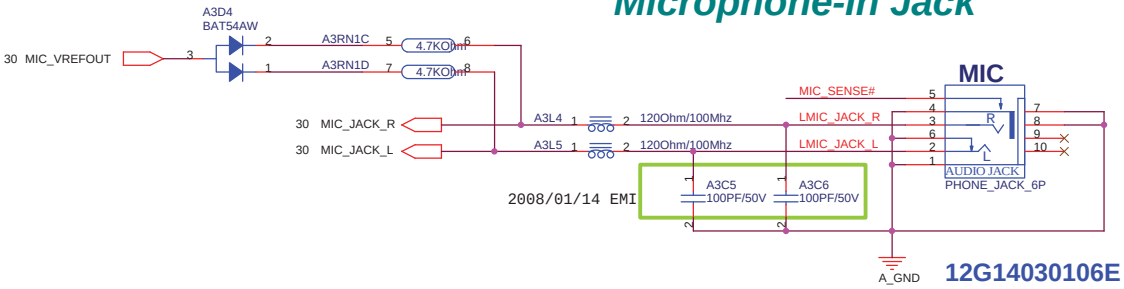
12G140001089

LINE1 Jack



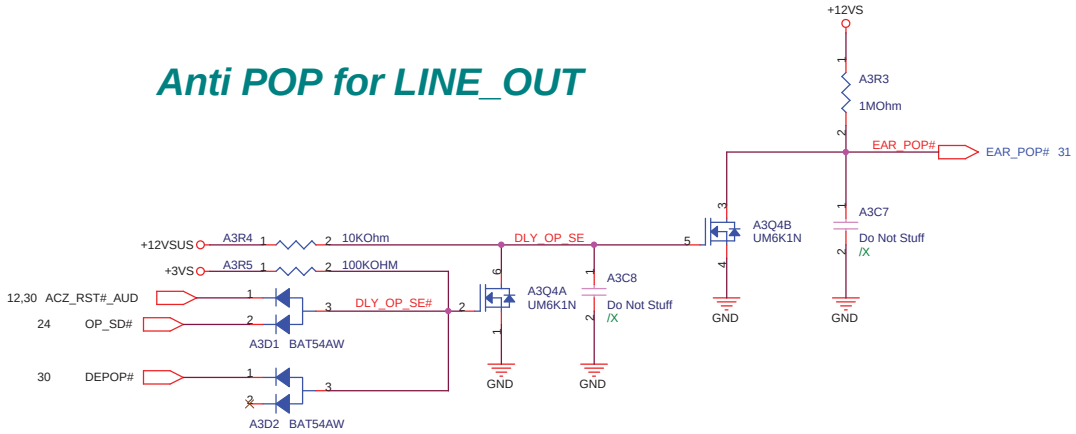
12G14030106E

Microphone-In Jack

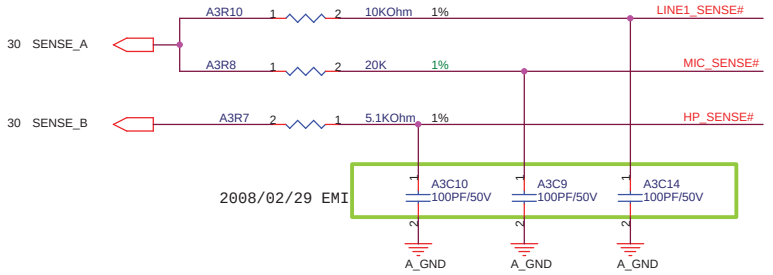


12G14030106E

Anti POP for LINE_OUT



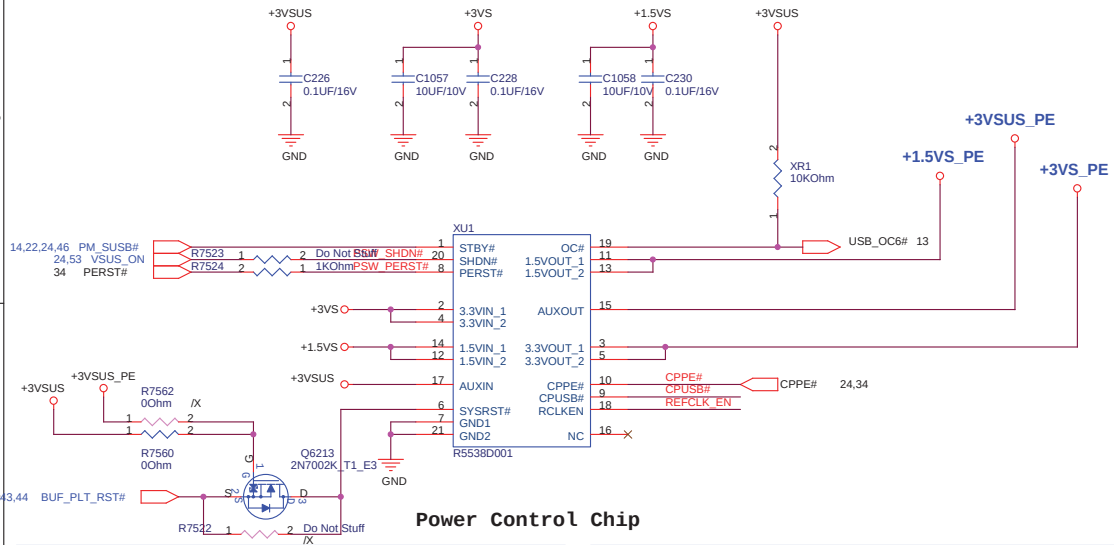
Jack Plug-in Detection



0414_1209

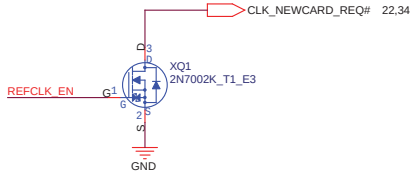
ASUSTek Computer INC.	Title : Phone Jack	
	Engineer: Mike Lee	
Size: A3	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 32 of 66	

Decouple Cap. (Near XU1)

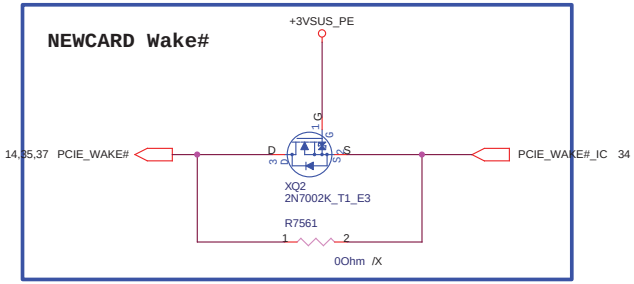


Power Control Chip

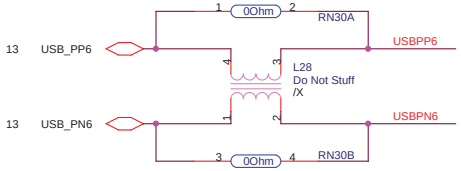
NEWCARD CLK Request



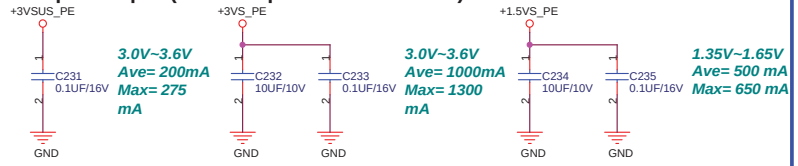
NEWCARD Wake#



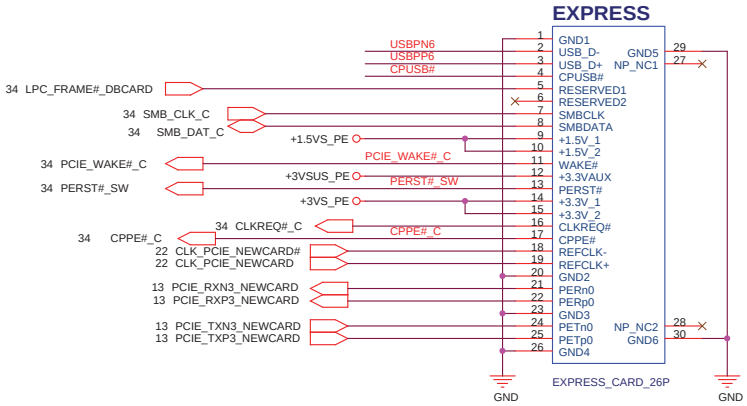
USB CHOKE FOR EMI



Decouple Cap. (Near Express connector)

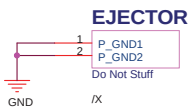


NewCard Header



!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector

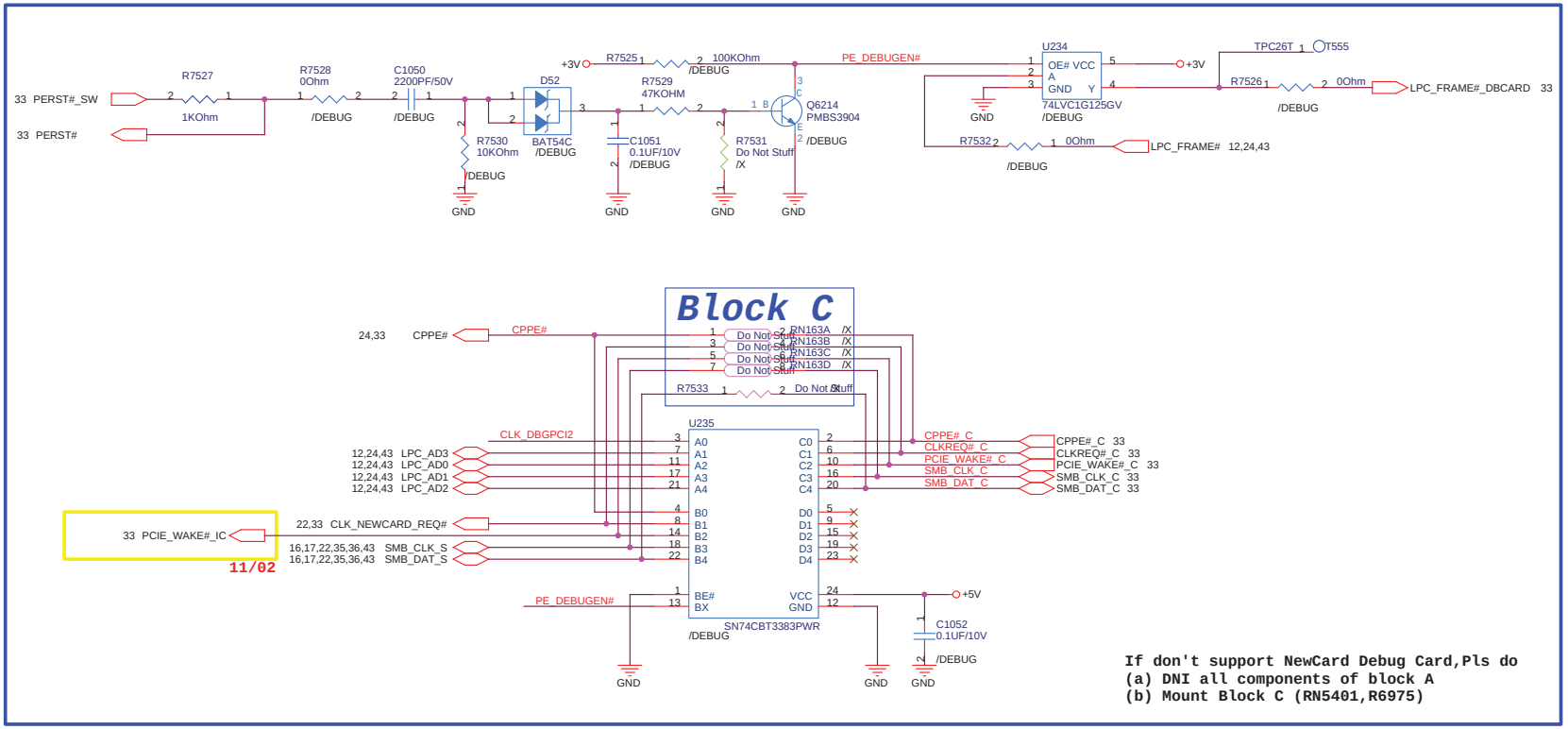


Do Not Stuff

0414_1209

ASUSTek Computer INC.	Title : EXPRESS CARD	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 33 of 66	

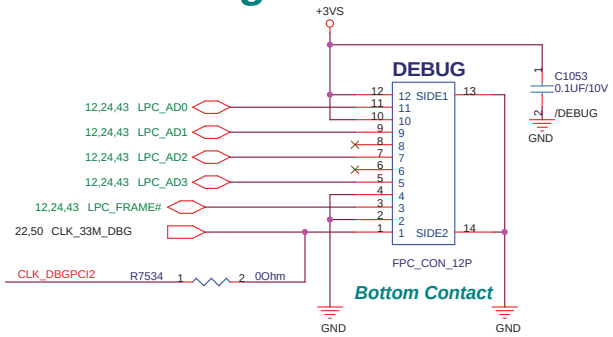
Block A

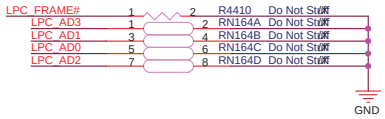


Debug Connector

For PCMCIA Debug Card

If support NewCard Debug Card, Pls don't mount all components.





0414_1209

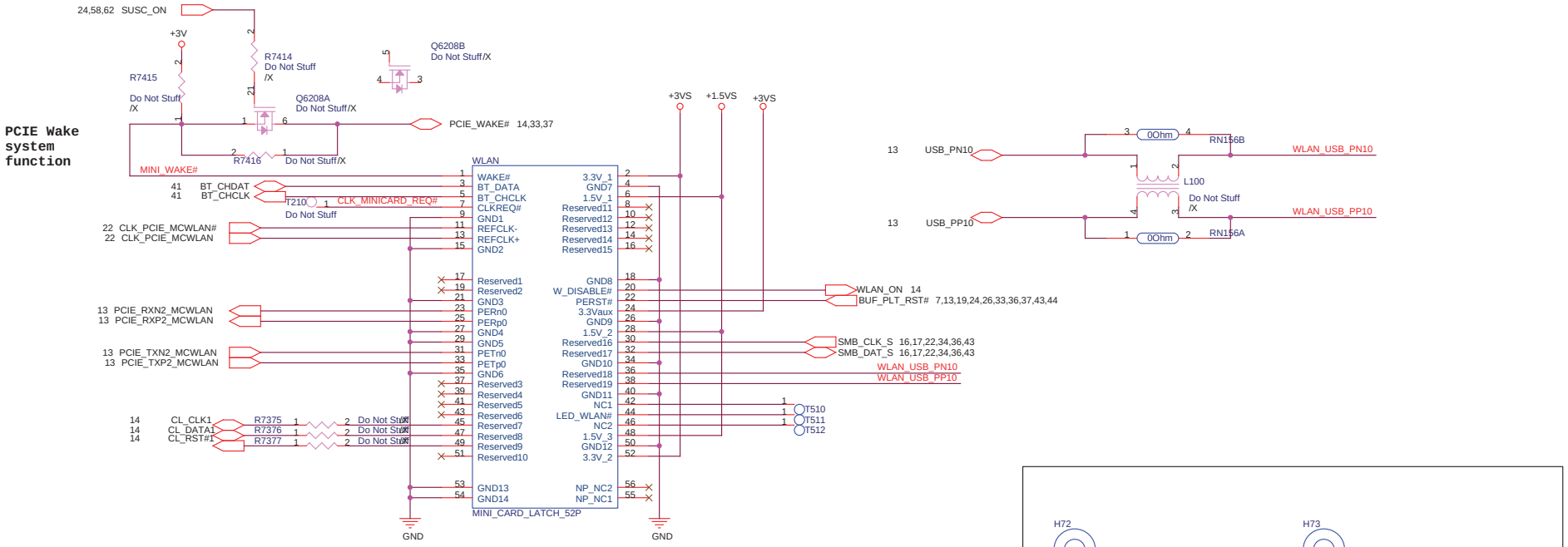
ASUSTek Computer INC.

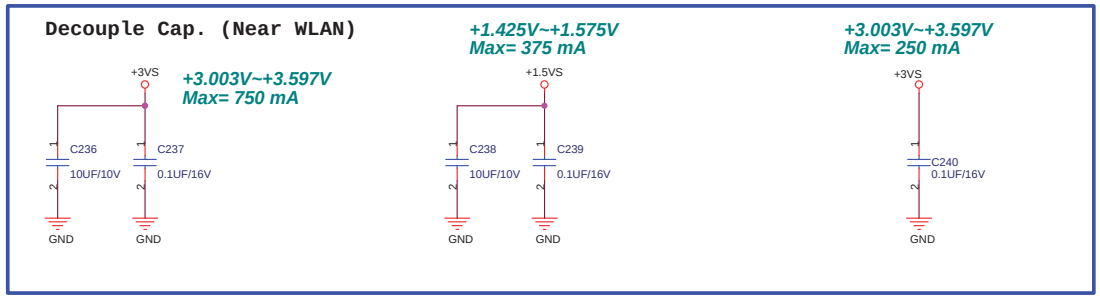
Title : New Card Debug

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 34 of 66





0414_1209

ASUSTek Computer INC.

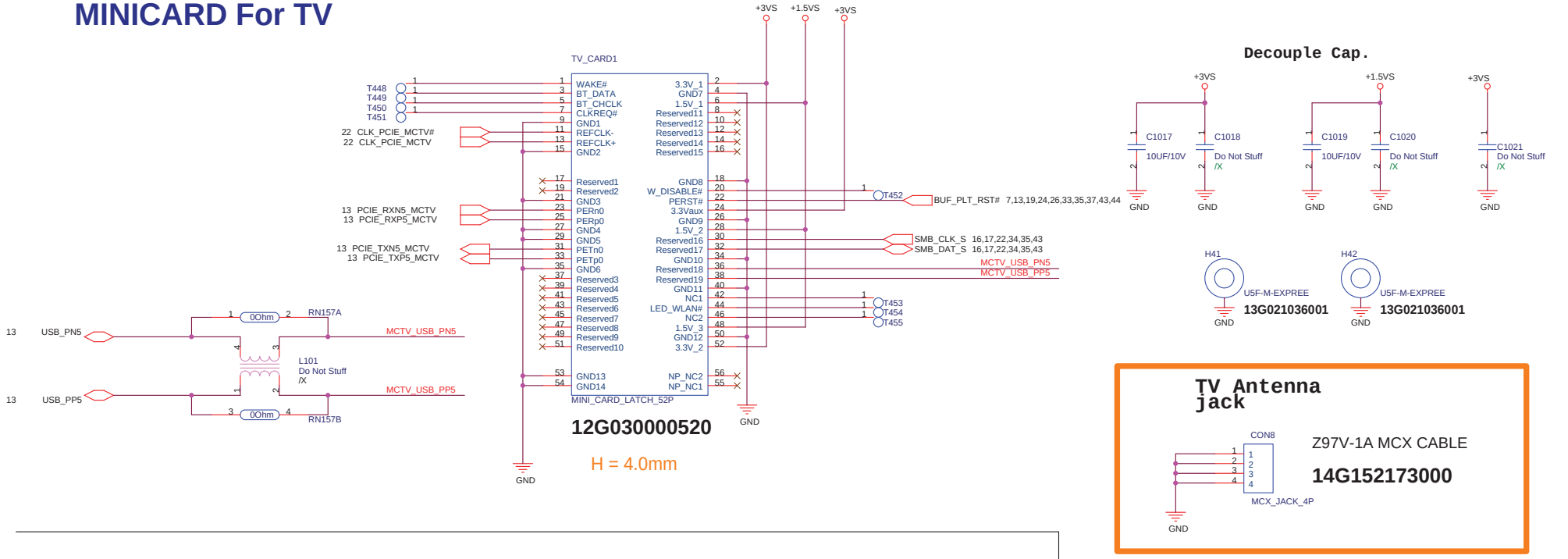
Title : MINICARD-1

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 35 of 66

MINICARD For TV



12G030000520

H = 4.0mm

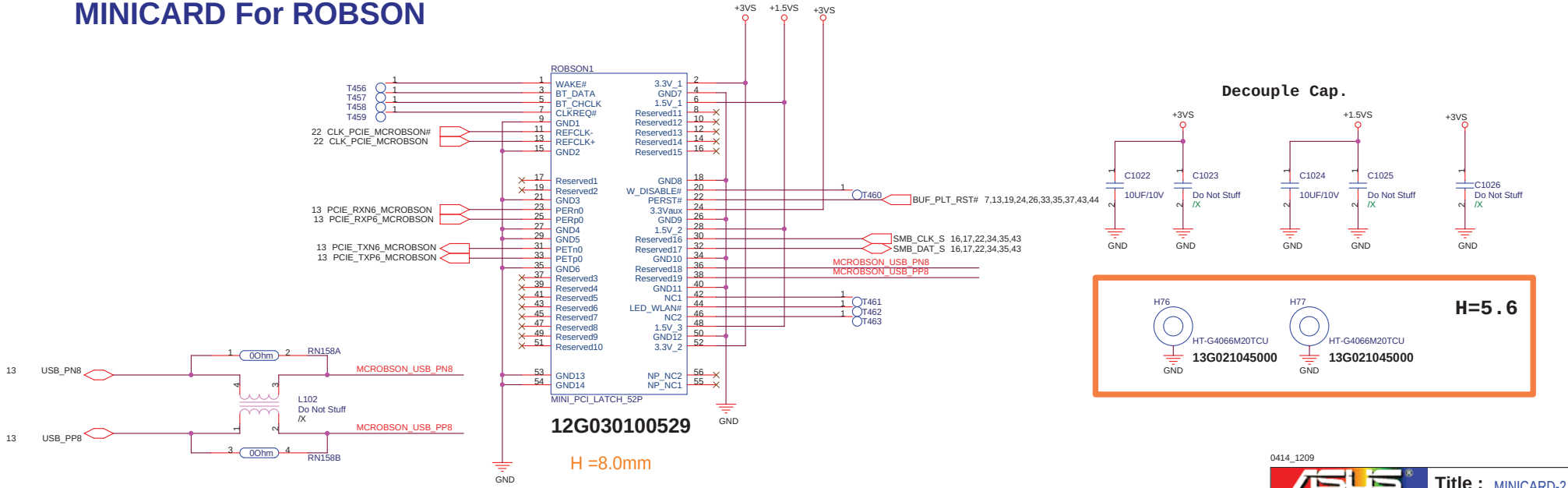
Decouple Cap.

TV Antenna jack

Z97V-1A MCX CABLE

14G152173000

MINICARD For ROBSON



12G030100529

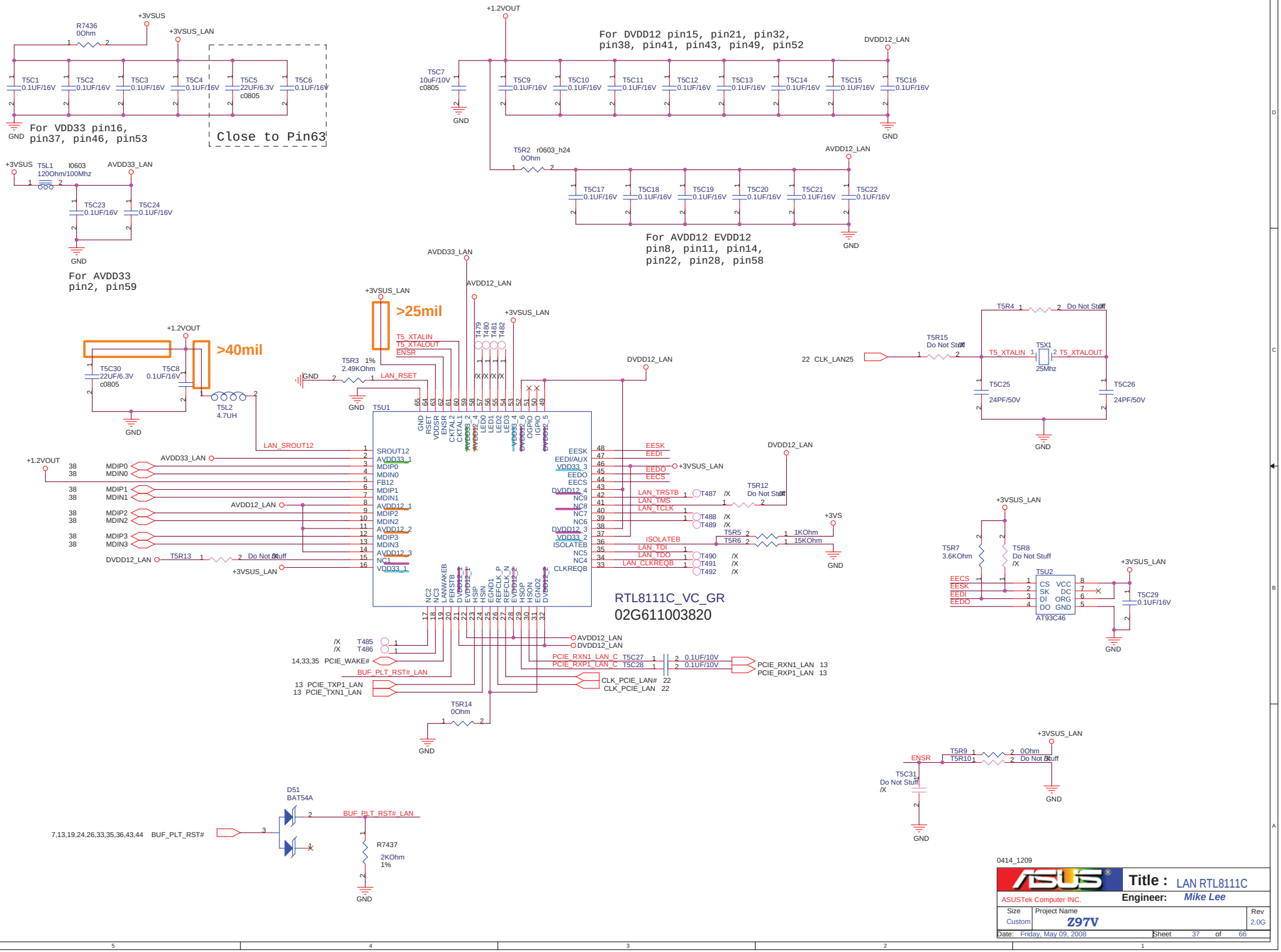
H =8.0mm

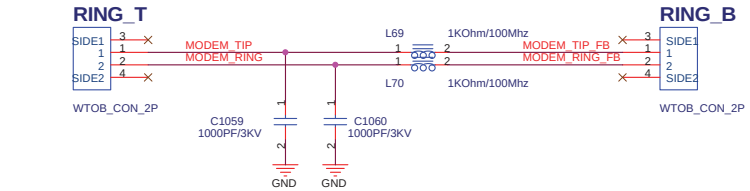
Decouple Cap.

H=5.6

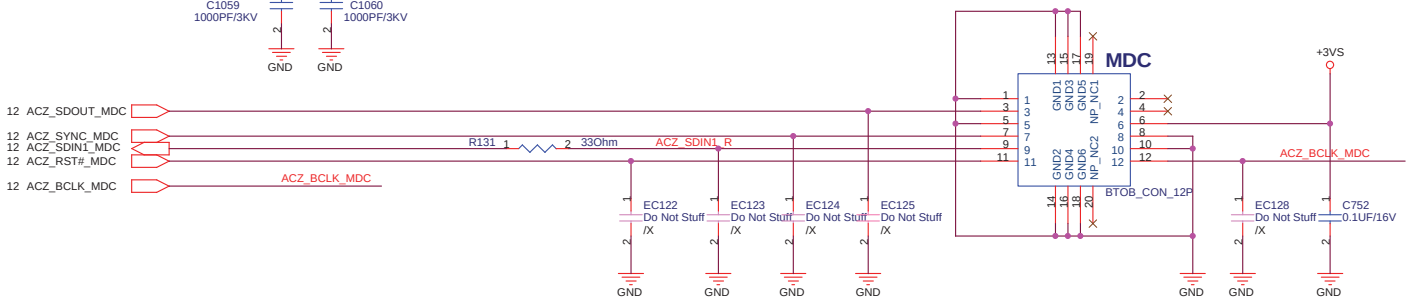
0414_1209

ASUSTek Computer INC.	Title : MINICARD-2	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 36 of 66	

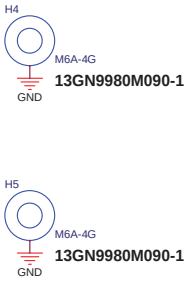


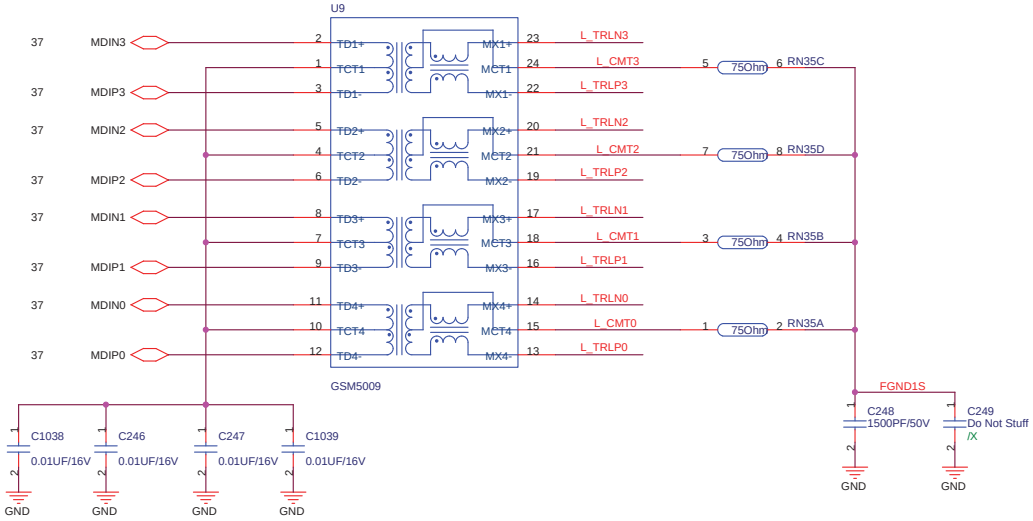


MDC Connector

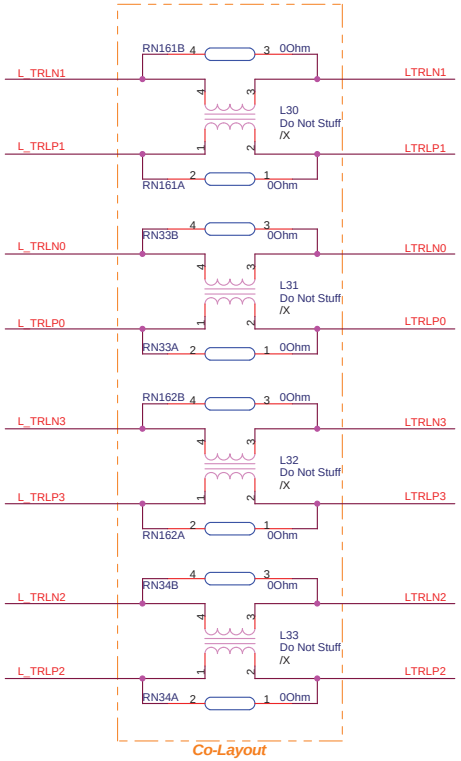


MDC Nut

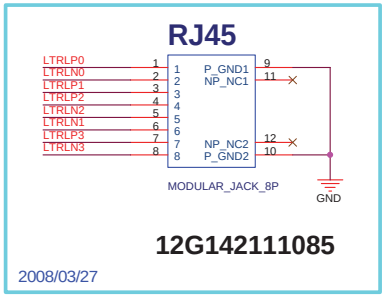




Giga LAN Transformer

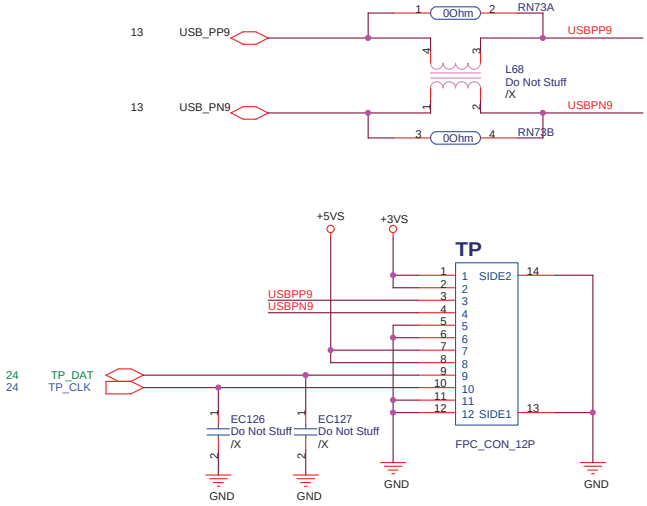


Co-Layout



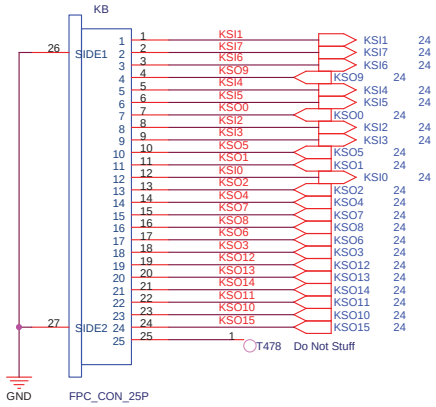
0414_1209

ASUSTek Computer INC.	Title : MDC / RJ45	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 38 of 66	



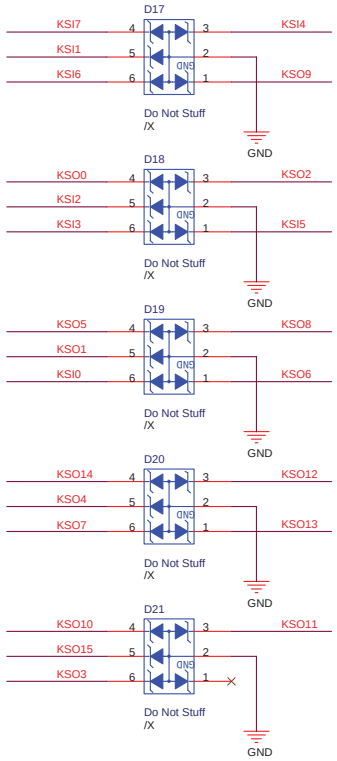
Fingerprint & TouchPad Connector

Keyboard Connector



12G182002502

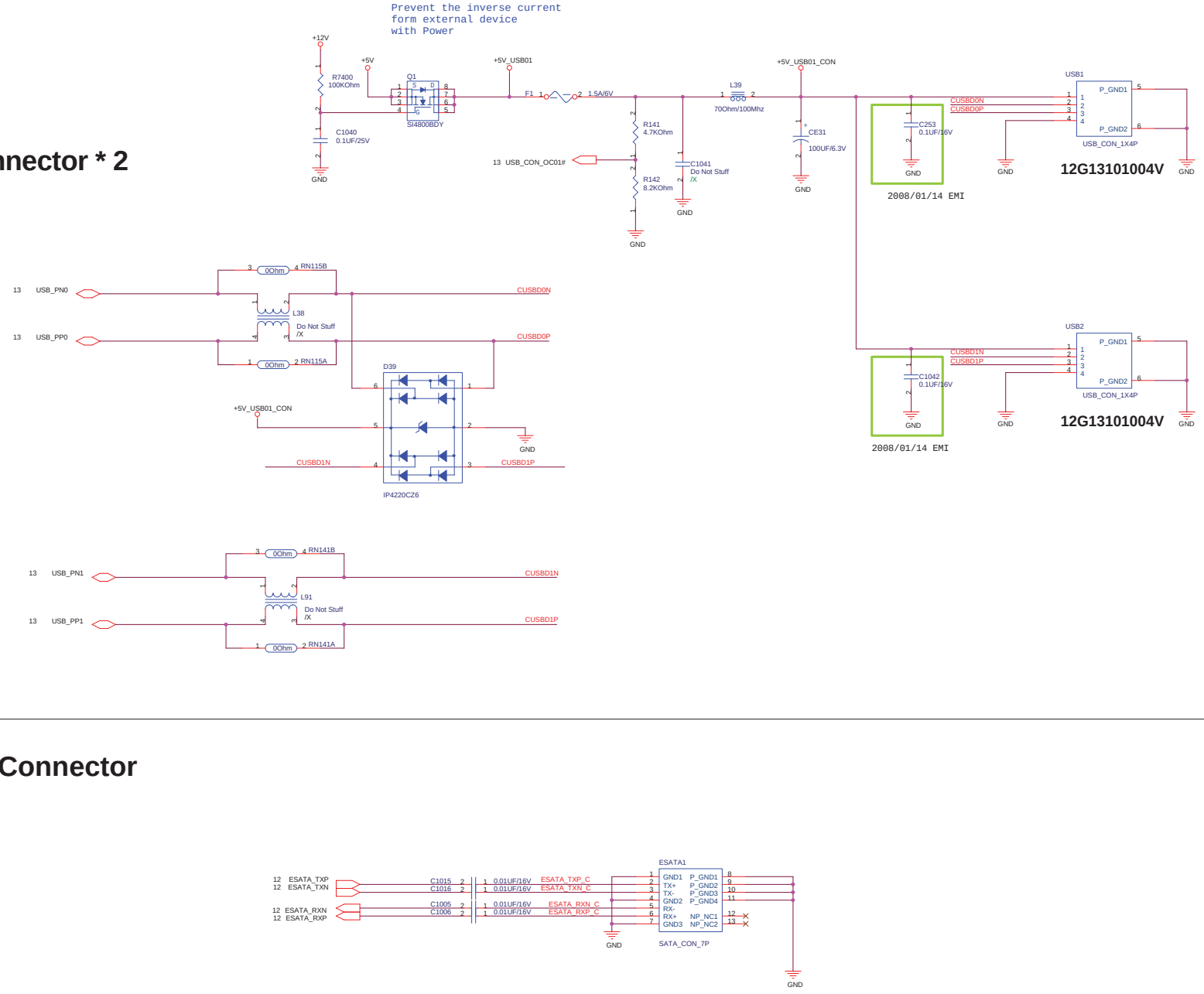
FOR EMI/ESD



0414_1209

ASUSTek Computer INC.	Title : Touch Pad & KB	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 39 of 66	

USB Connector * 2

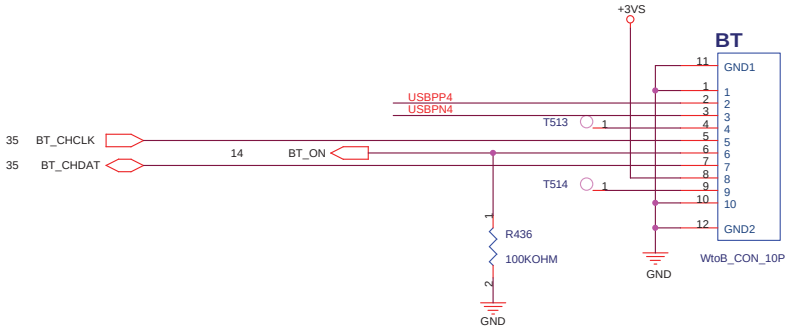


ESATA Connector

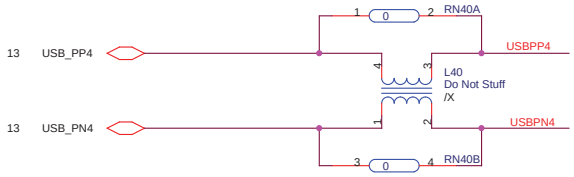
0414_1209

ASUSTek Computer INC.	Title:	USB / ESATA Connector
	Engineer:	Mike Lee
Size: C	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 40 of 66	

Bluetooth Connector



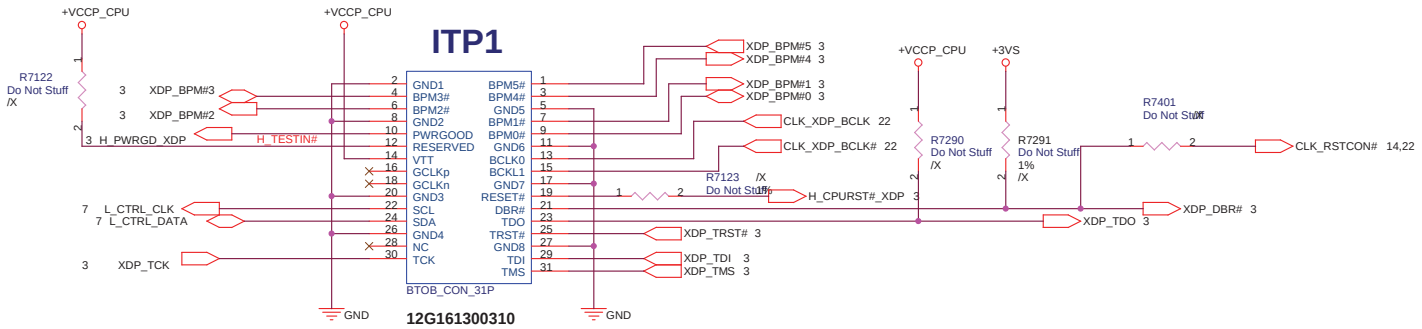
BT_OFF# : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled



0414_1209

ASUSTek Computer INC.	Title : Bluetooth Conn.	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 41 of 66	

ITP



0414_1209

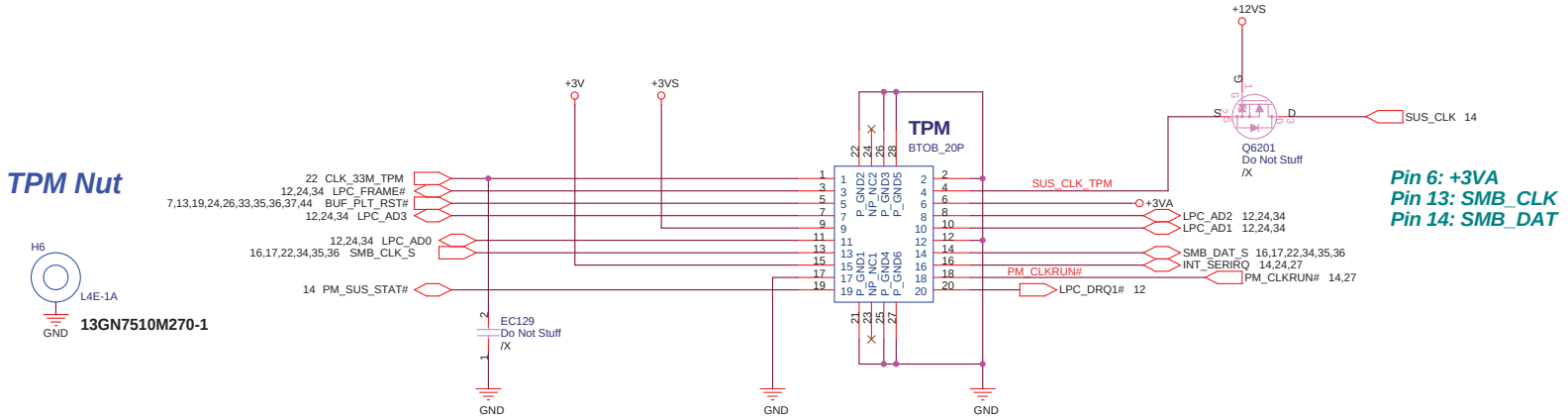
ASUSTek Computer INC.

Title : Debug Connector

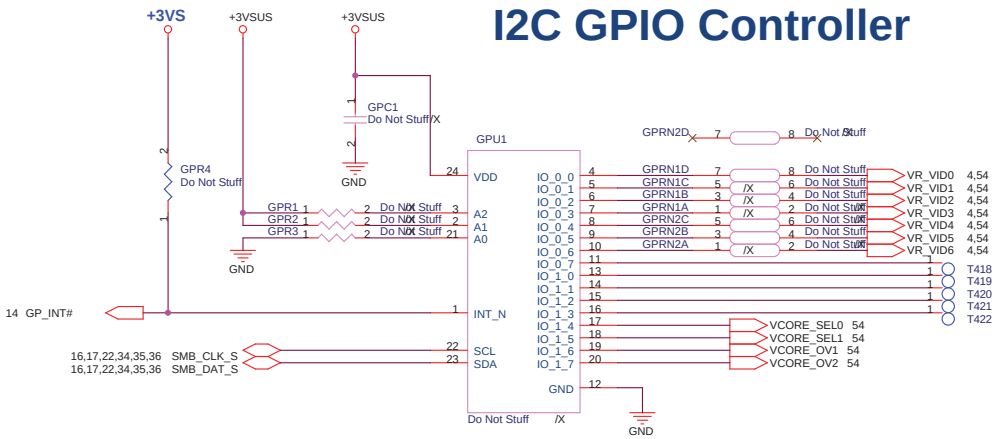
Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 42 of 66



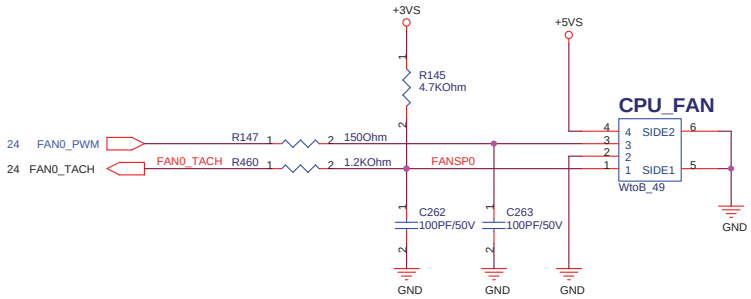
TPM Module Connector

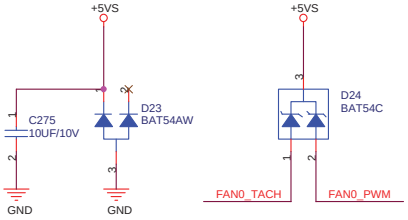


0414_1209

ASUSTek Computer INC.	Title : TPM Connector	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 43 of 66	

CPU Fan Connector

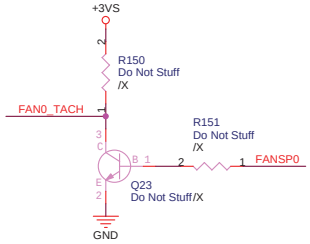




Route H_THERMDA and H_THERMDC in the same layer

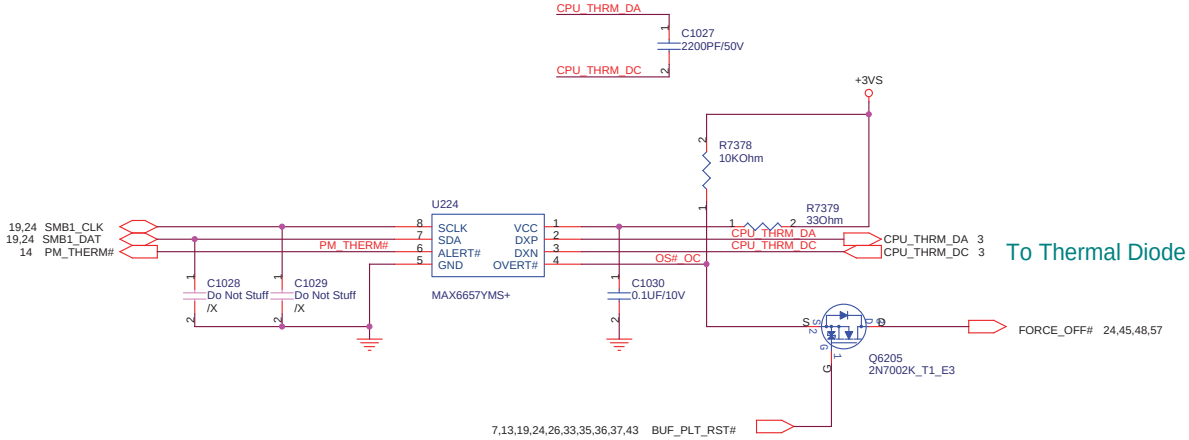
----------OTHER SIGNALS
15 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power



CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

CPU Thermal Sensor

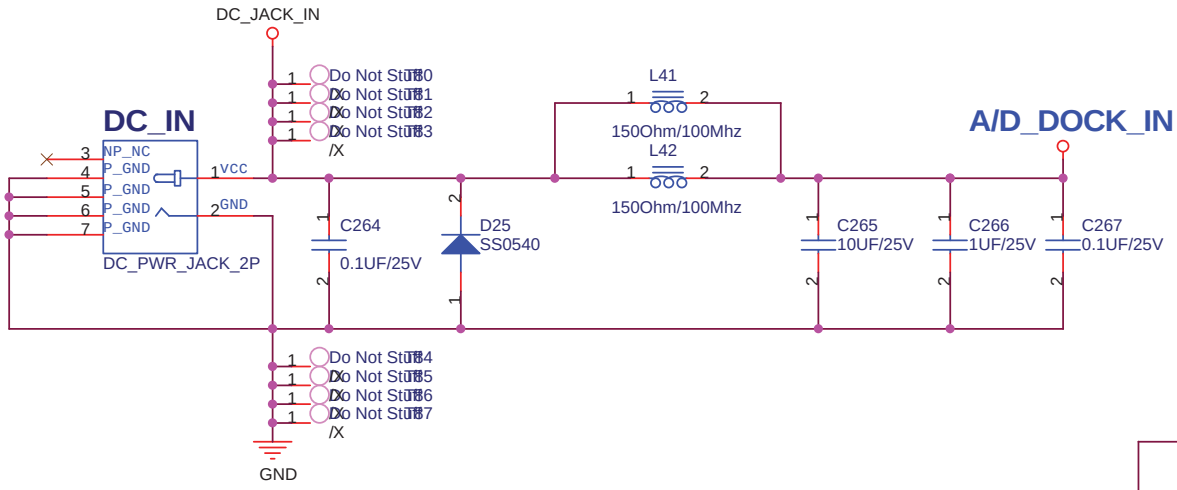


SM Bus Address fix at:
1001 100x (98), Resolution : +/- 1 degree

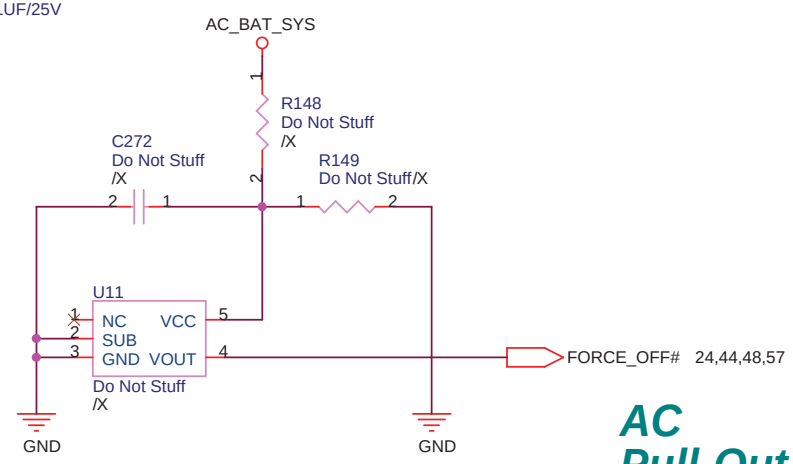
0414_1209

ASUSTek Computer INC.	Title : Thermal Sensor & Fan	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 44 of 66	

DC-IN Connector

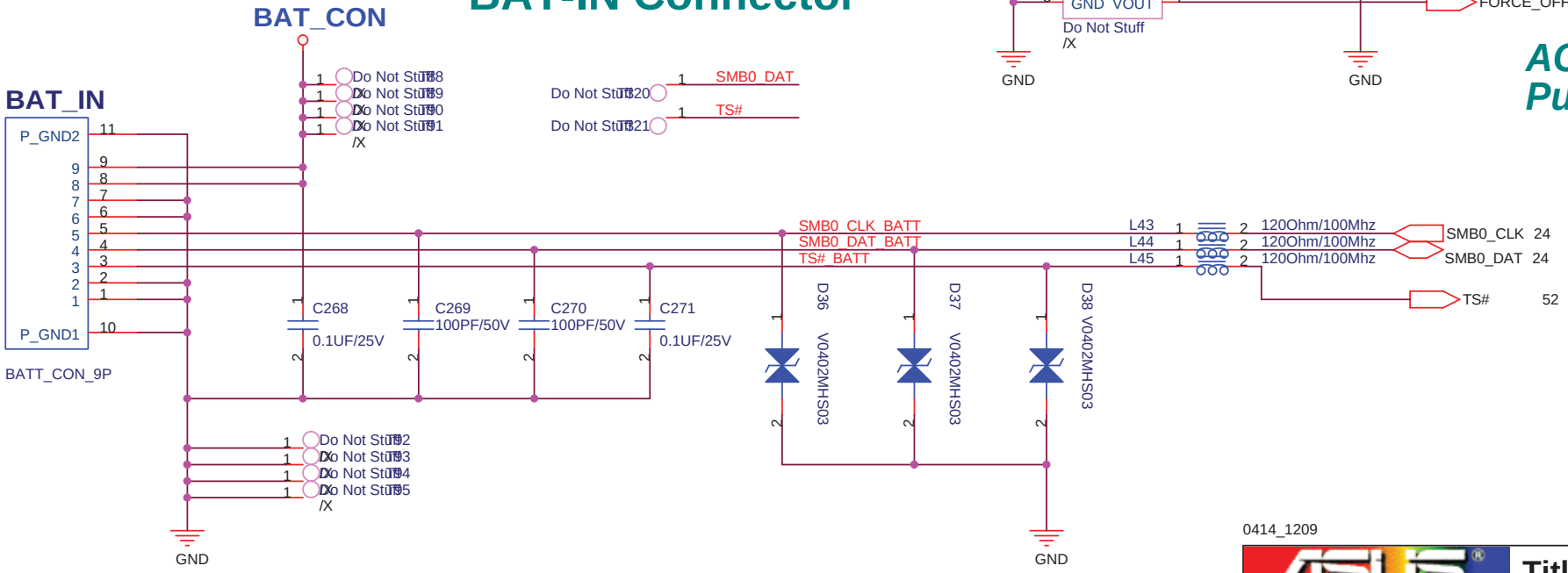


Without Battery & Pull out Adapter



AC Pull-Out

BAT-IN Connector

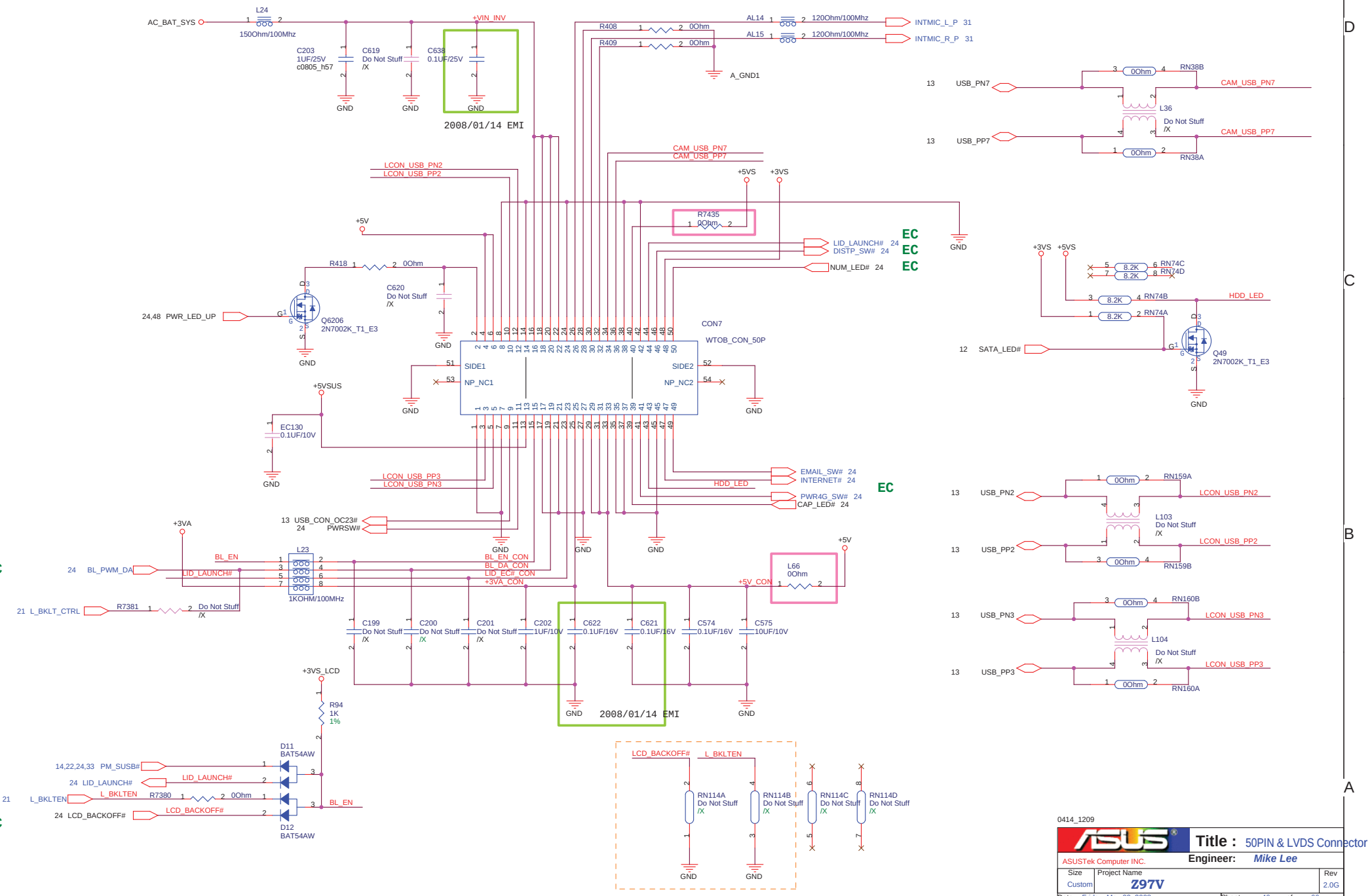


0414_1209

ASUSTek Computer INC.	Title : DC IN & BAT IN	
	Engineer: Tony Kao	
Size: A4	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 45 of 66	

LCD Backlight Control

INVERTER Connector



0414_1209

ASUSTek Computer INC.

Title : 50PIN & LVDS Connector

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 46 of 66

From SB

13 SPI_SI — Q50 2N7002K_T1_E3 — RSPI_MOSI
13 SPI_SO — Q51 2N7002K_T1_E3 — RSPI_MISO
13 SPI_CLK — Q52 2N7002K_T1_E3 — RSPI_CLK
13 SPI_CS#0 — Q6209 2N7002K_T1_E3 — RSPI_CS#0
13 SPI_CS#1 — Q6210 Do Not Stuff /X — RSPI_CS#1

PROGRAMMING SELECT	Stuff SW1 (R7428 NU)		Stuff R7428 (SW1 NU)
	P1	P2	
PROGRAM SPI 0	ON	OFF	V
PROGRAM SPI 1	OFF	ON	X

+3VSUS — D34 Do Not Stuff /X — +3VSUS_SPI
+3VS — D49 BAT54AW

R7428 0Ohm — RSPI_CS#1 / RSPI_CS#_CON / RSPI_CS#0 — SW1 (GND1, GND2, NP_NC1, NP_NC2) Do Not Stuff /X

12G17100006F SPI_J1 (WtoB_CON_6P) — C604 0.1UF/16V
RSPI_MOSI, RSPI_MISO, RSPI_CLK, RSPI_CS#_CON

SPI0 — U216 SST25VF080B (8Mb)
R689 3.3KOhm, R690 3.3KOhm, R692 15Ohm, R693 47Ohm, R694 47Ohm
+3VM_SPI0_WP#, +3VM_SPI0_HD#

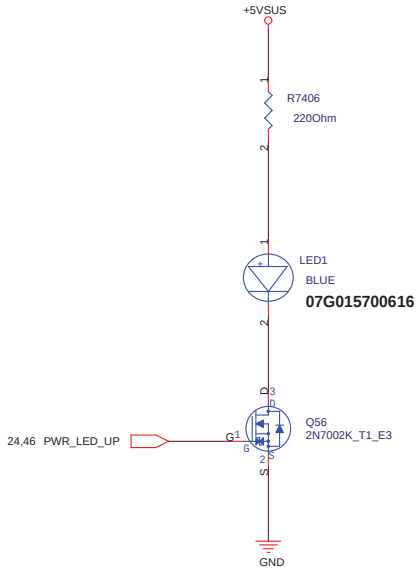
SPI1 — U217 (16Mb)
R695 Do Not Stuff /X, R696 Do Not Stuff /X, C975 Do Not Stuff /X
R697 Do Not Stuff /X, R698 Do Not Stuff /X, R699 Do Not Stuff /X
+3VM_SPI1_WP#, +3VM_SPI1_HD#

0414_1209

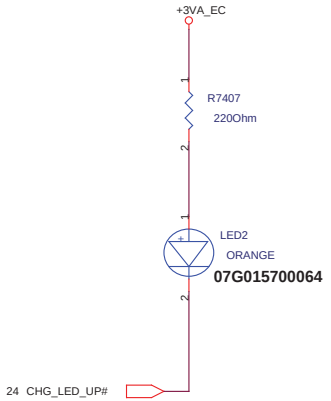
ASUSTek Computer INC.
Title : SPI Flash
Engineer: Mike Lee
Size: Custom | Project Name: Z97V | Rev: 2.0G
Date: Friday, May 09, 2008 | Sheet 47 of 66

LED

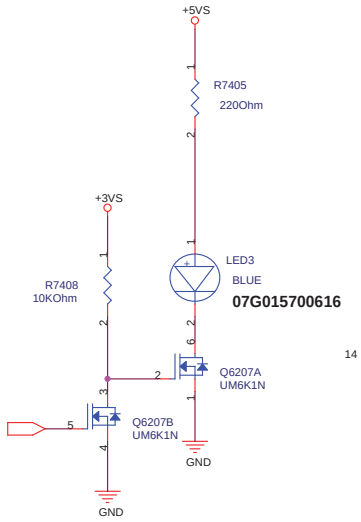
POWER LED



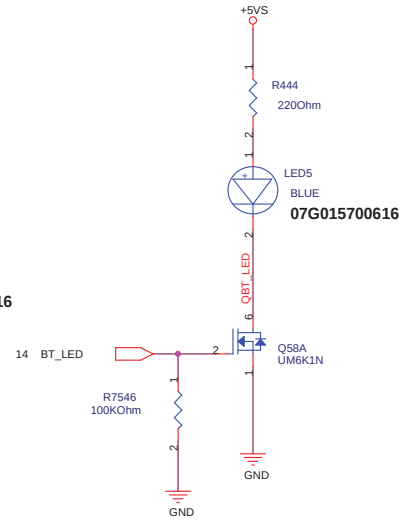
BATTERY LED



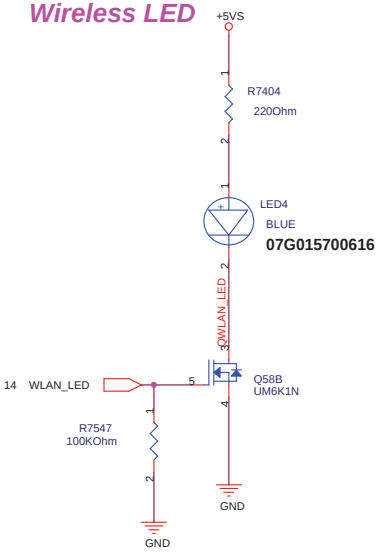
EMAIL LED



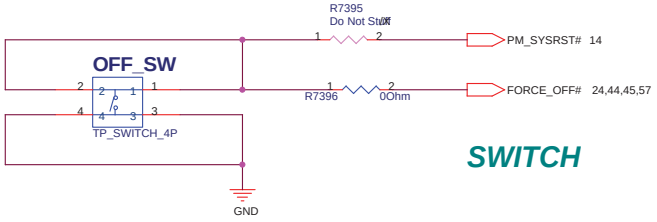
Bluetooth LED



Wireless LED



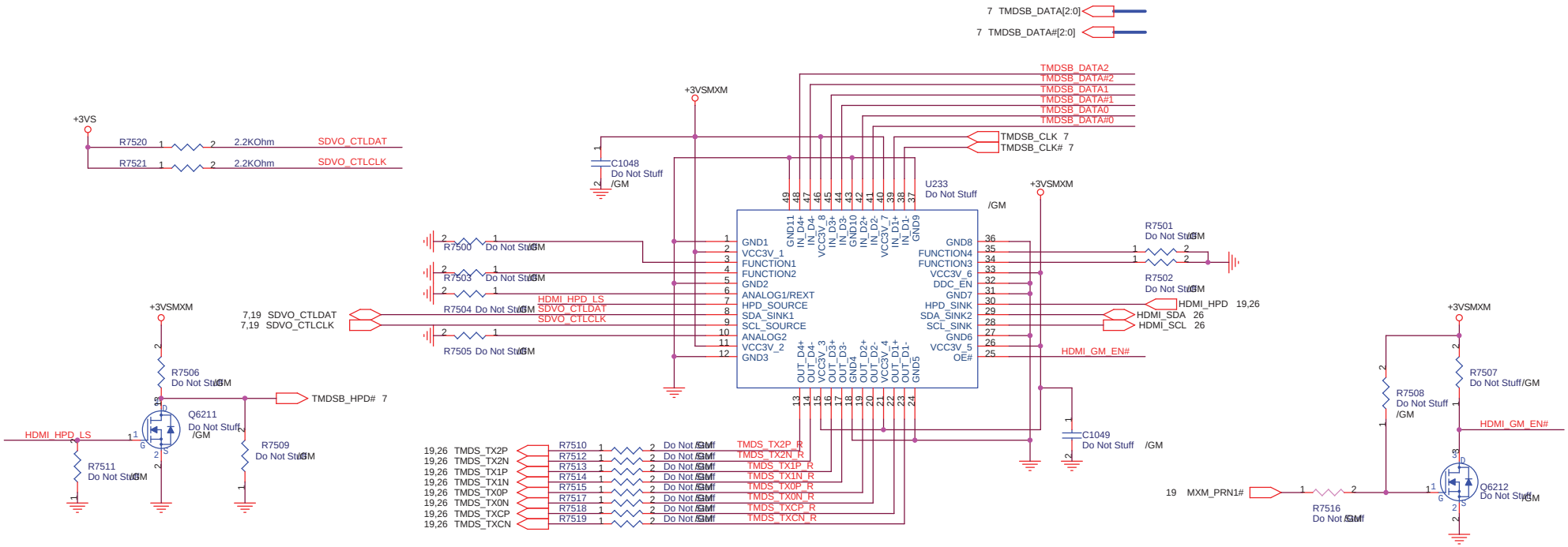
RESET SWITCH



SWITCH

0414_1209

ASUSTek Computer INC.	Title : RST SW / LED	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 48 of 66	



0414_1209

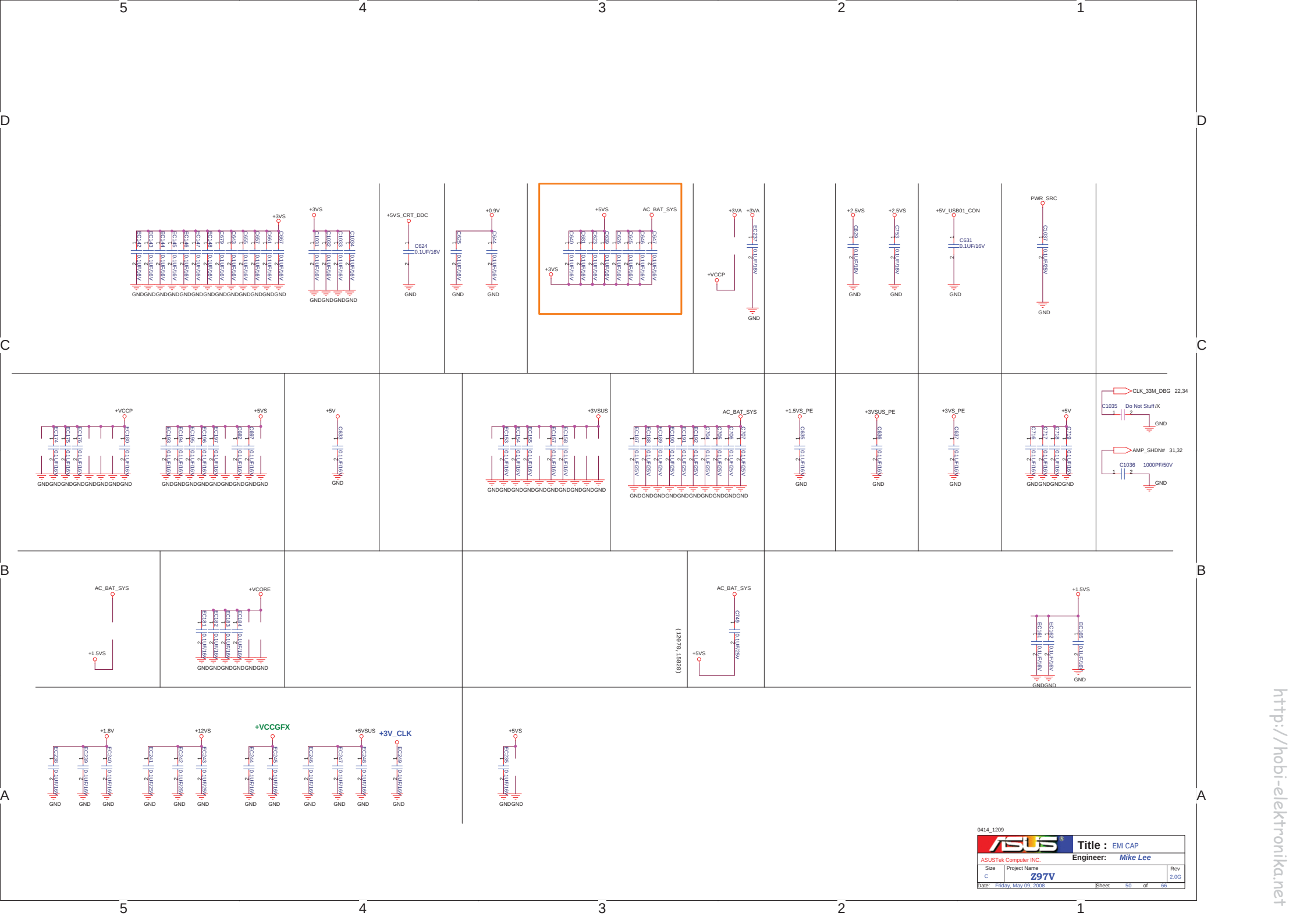
ASUSTeK COMPUTER INC. NB6

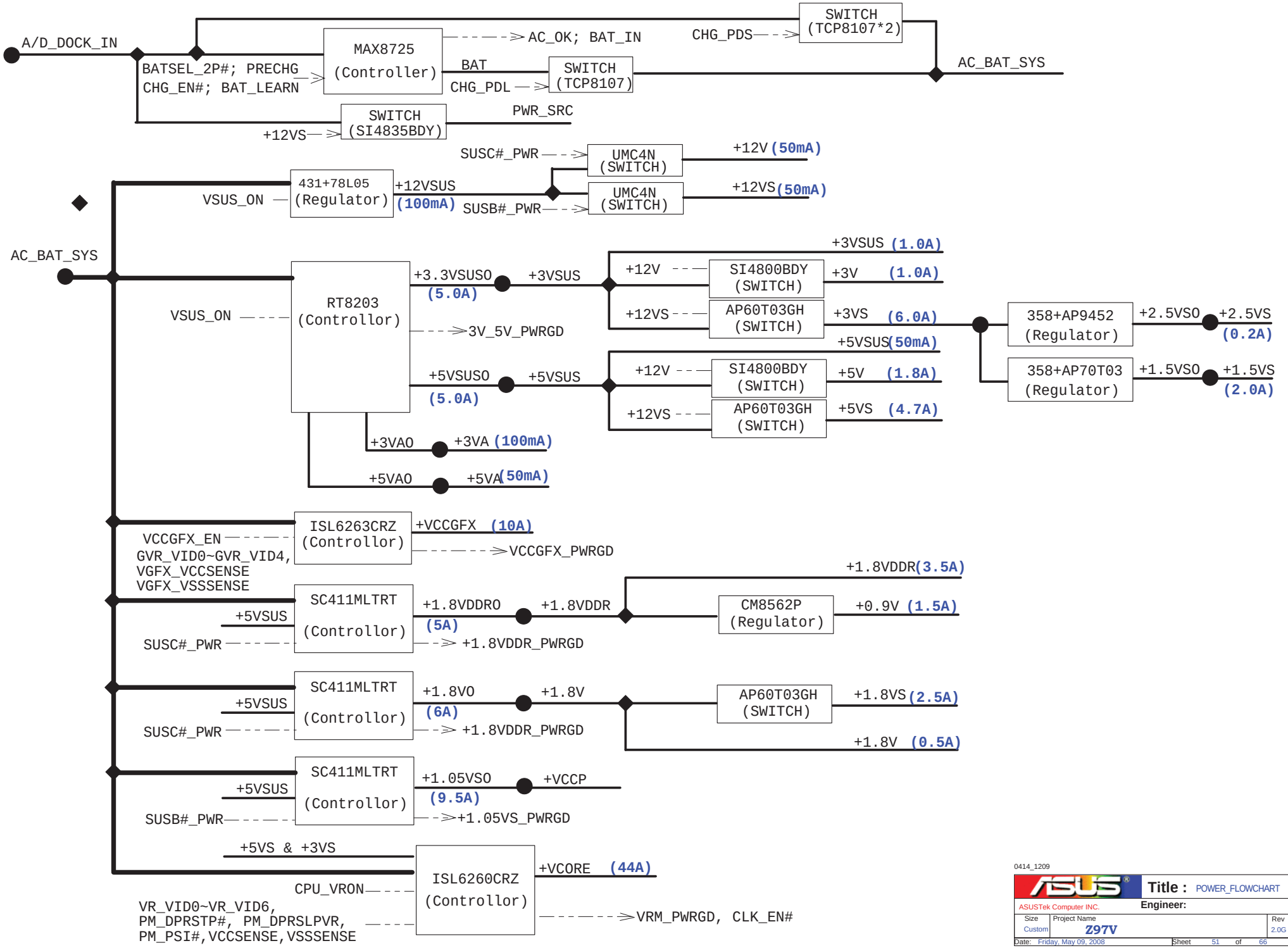
Title : HDMI LEVEL SHIFTERS

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 49 of 66





0414_1209

ASUSTek Computer INC.

Title : POWER_FLOWCHART

Engineer:

Size	Project Name	Rev
Custom	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 51 of 66

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 12.27V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V

Adaptor Max. Current :

PR807=20K PR812 = 178K; Ilimit = 4.5A; 90W
PR807=27K PR812 = 47K; Ilimit = 3.5A; 65W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 126mA
Victl = 0.0909V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Victl = 2.084V
=> Icharge = 1.6933A
BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V
=> Icharge = 2.9329A

PR814=120K PR813 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

For new EC did'nt need AC_APR_UC

AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent

BATSEL_2P# = 1, 3 Cells
BATSEL_2P# = 0, 6 or 9 Cells

PRECHG = 1, Pre-Charging Mode
Charging Current = 126mA

CHG_EN# = 1, Charger Disabled
CHG_EN# = 0, Charger Enabled

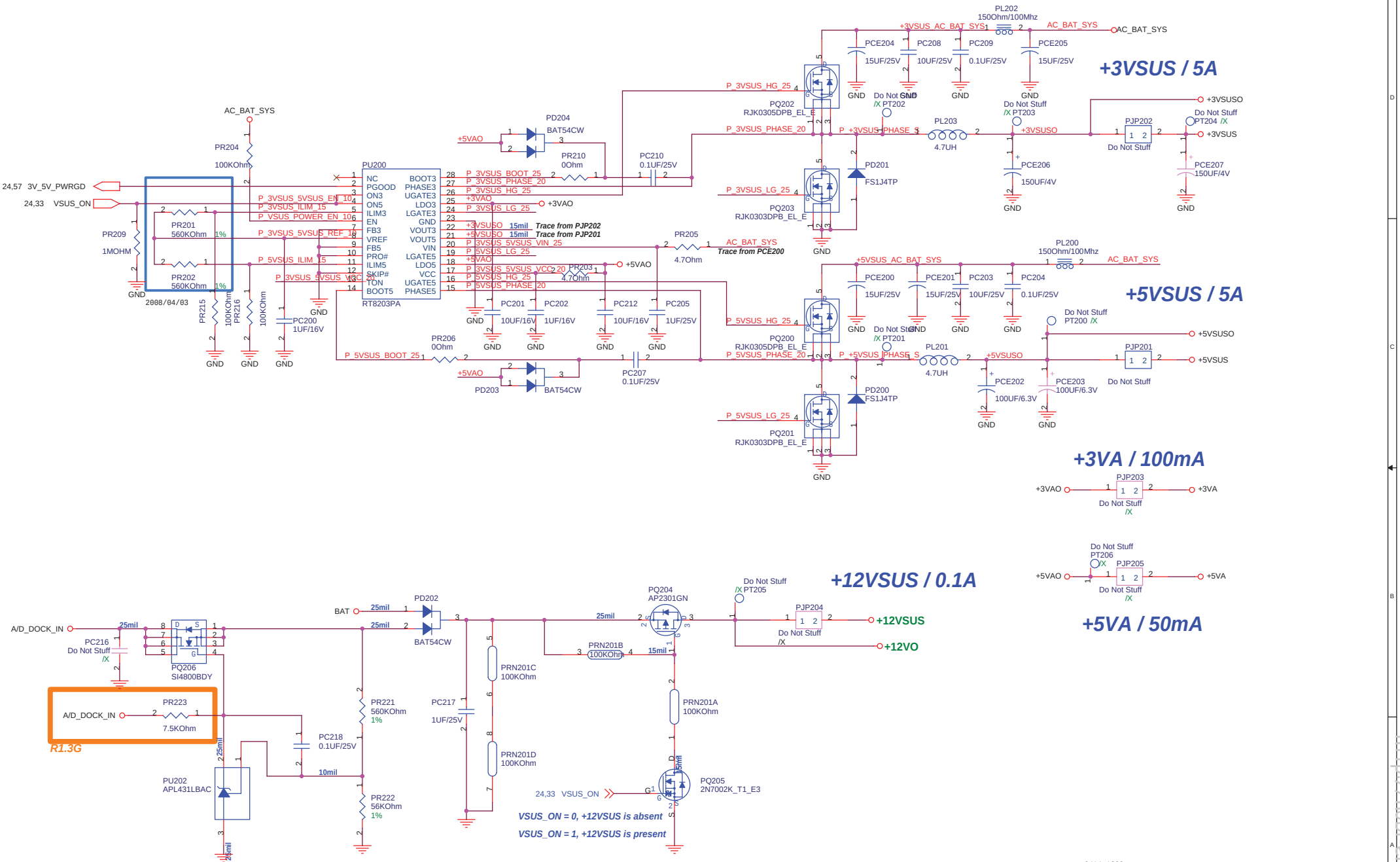
BAT_LEARN = 1, Battery discharges
BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

BAT_IN_OC# = 0; Battery Plug-in
BAT_IN_OC# = 1; Battery absence

TS# = 1; Battery absence
TS# = 0; Battery Plug-in

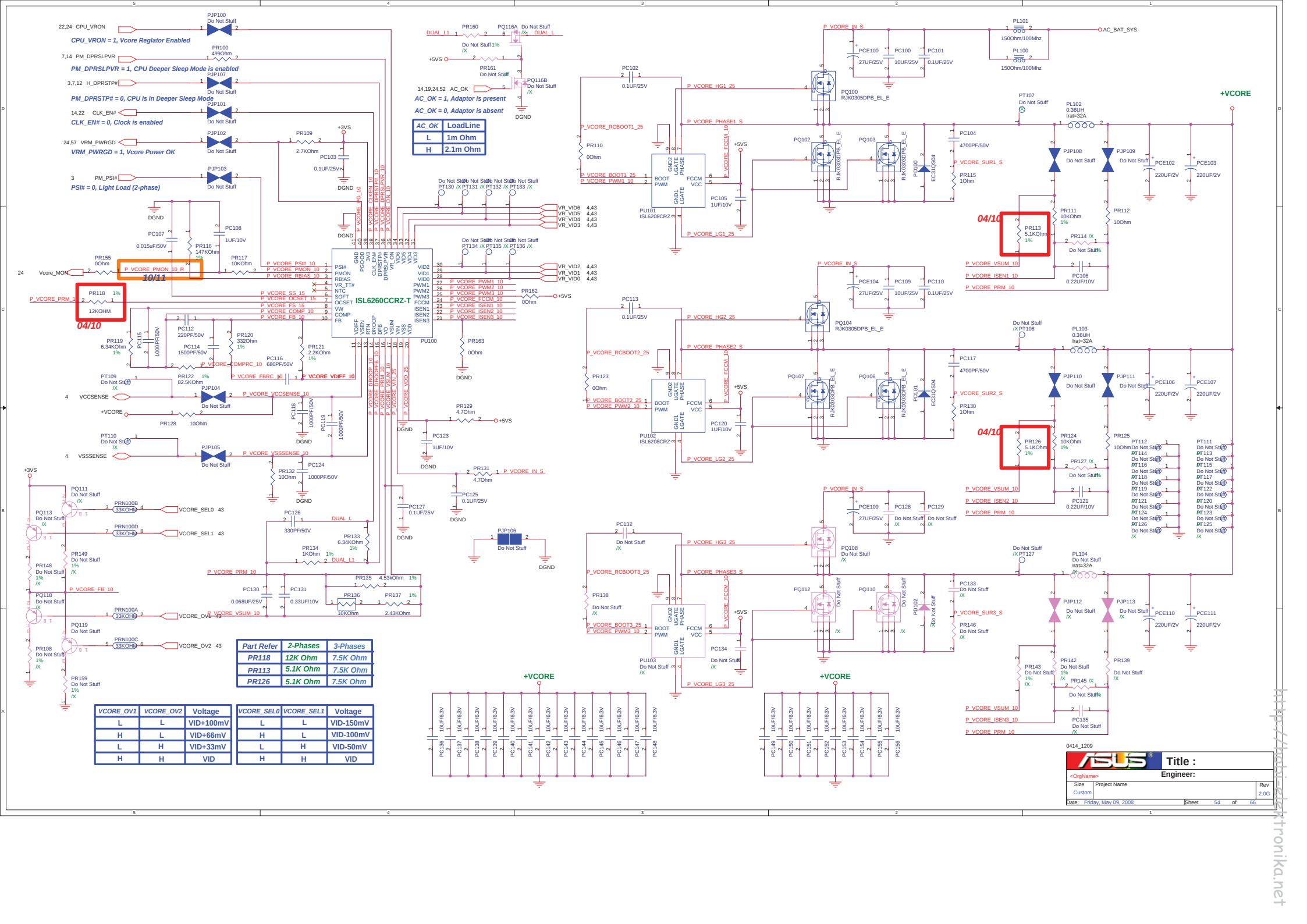
0414_1209

ASUSTek Computer INC.
Title : POWER_CHARGER
Engineer:
Size: C | Project Name: Z97V | Rev: 2.0G
Date: Friday, May 09, 2008 | Sheet 52 of 66

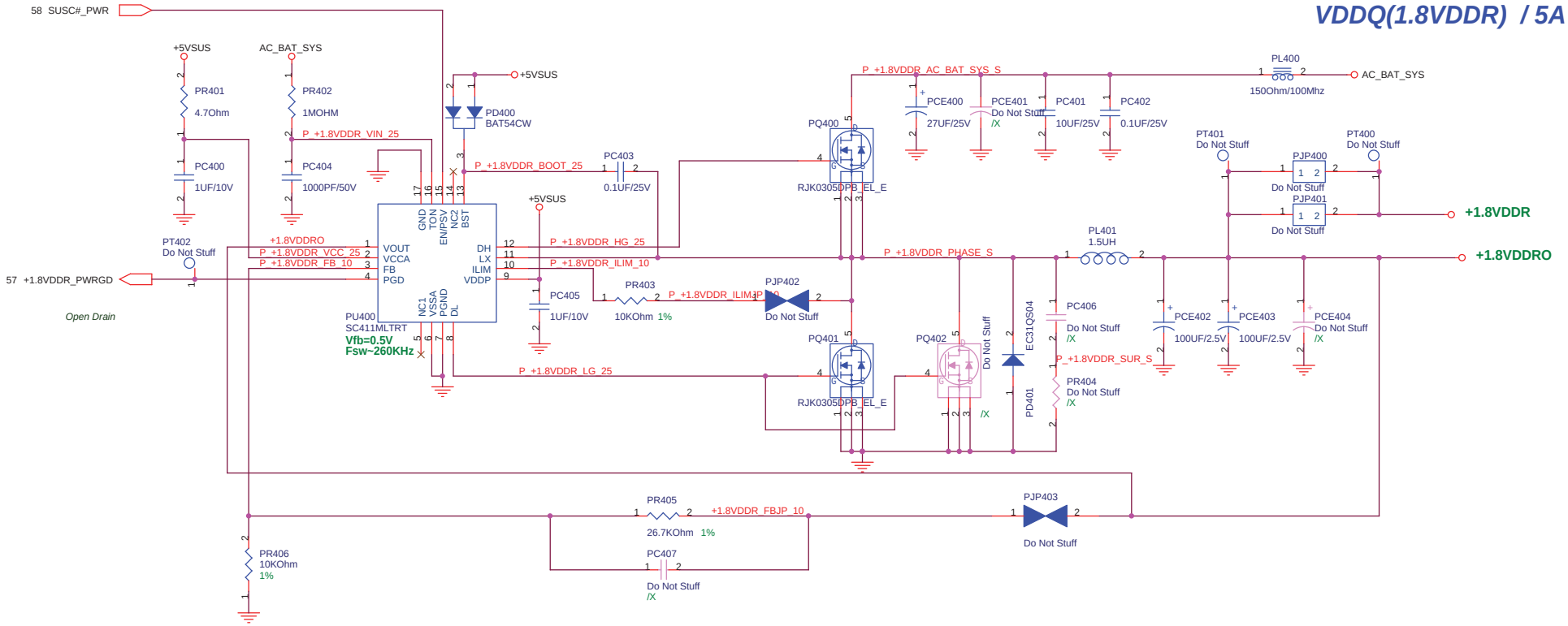


0414_1209

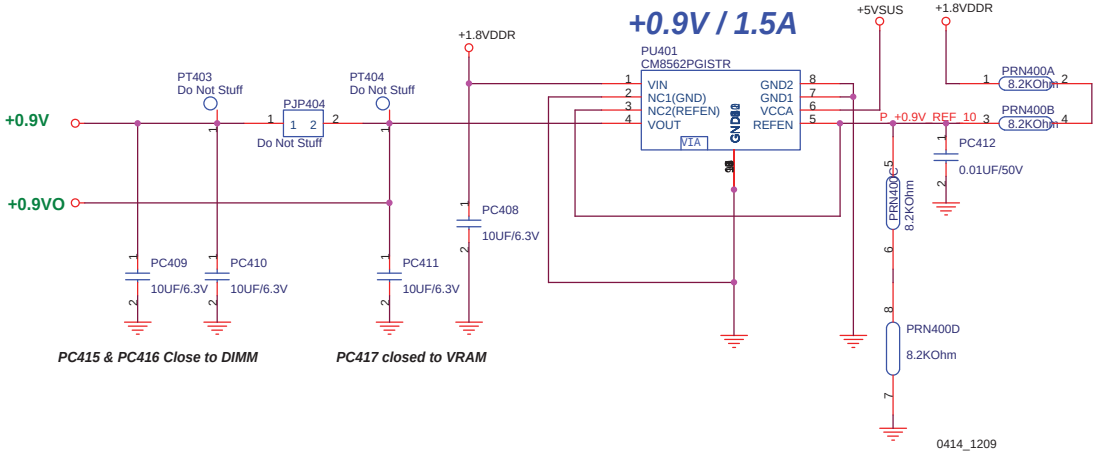
ASUSTek Computer INC.	Title : POWER_SYSTEM	
	Engineer:	
Size: A3	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 53 of 66	



VDDQ(1.8VDDR) / 5A



+0.9V / 1.5A



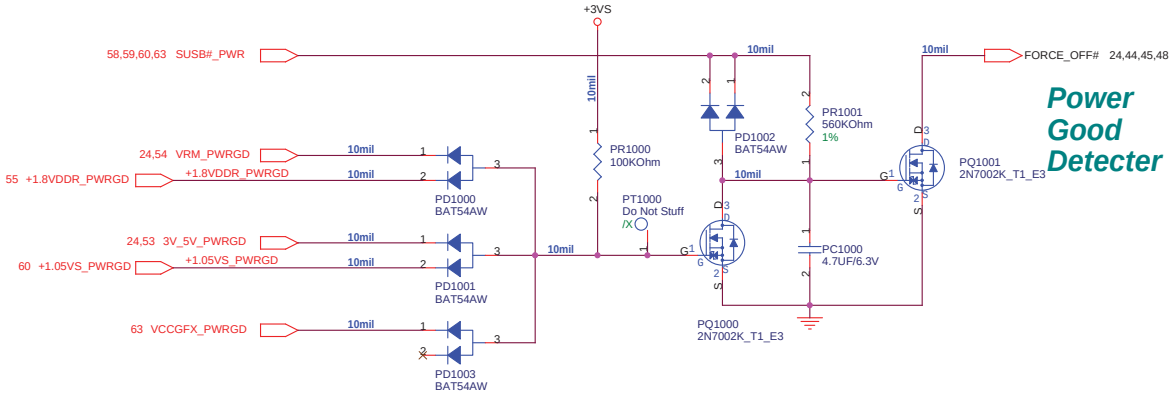
0414_1209

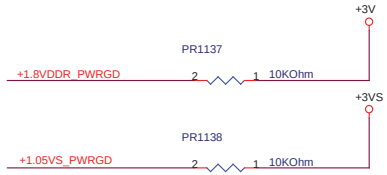
<OrgName>	Title :	
	Engineer:	
Size: A3	Project Name	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 55 of 66	

BLANK

0414_1209

ASUSTek Computer INC.	Title : POWER_I/O_+3VA & +2.5V
	Engineer:
Size: Custom	Project Name: Z97V
	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 56 of 66

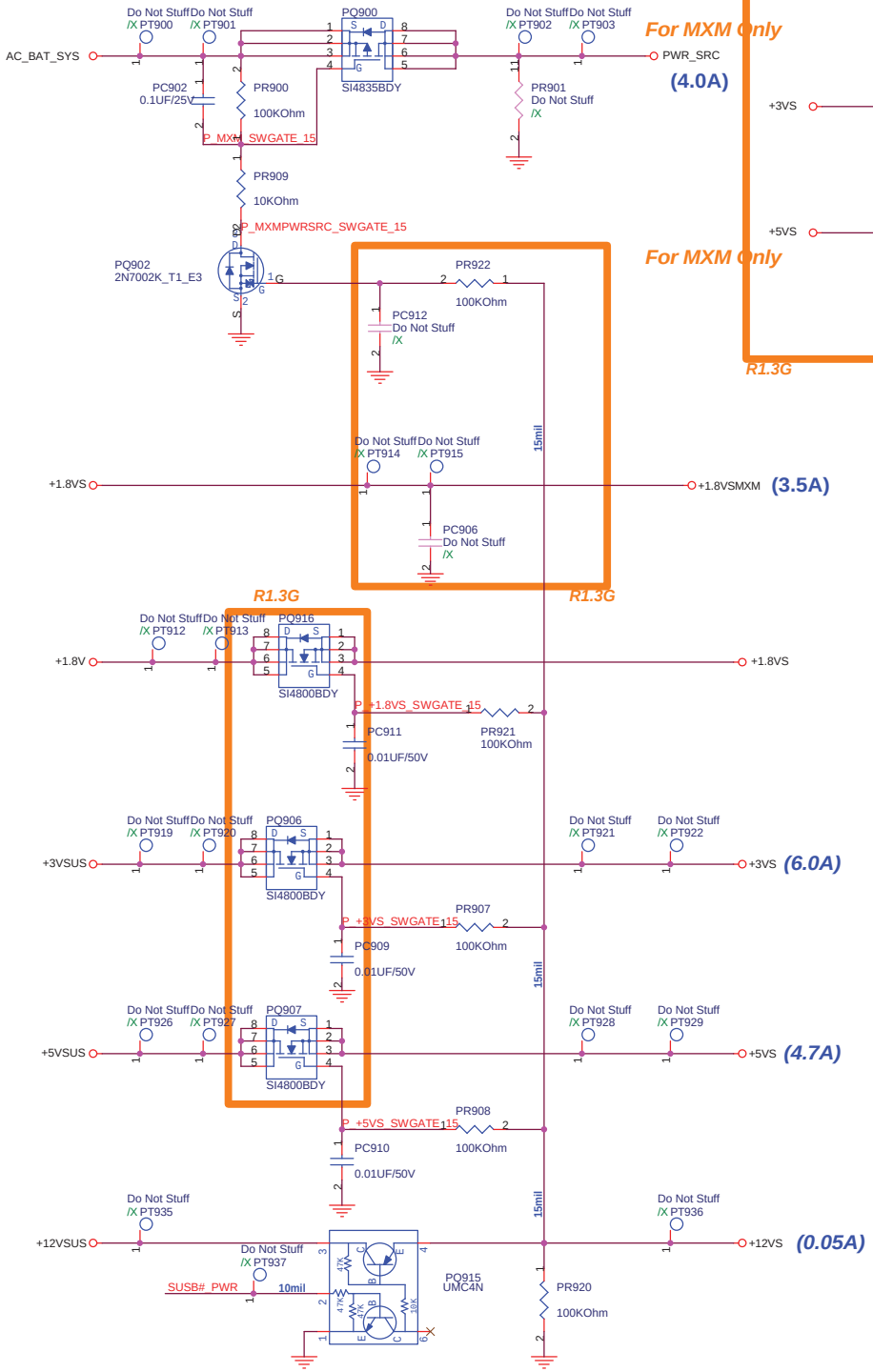


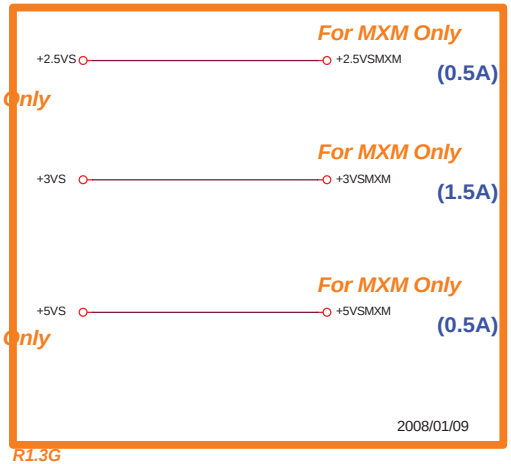


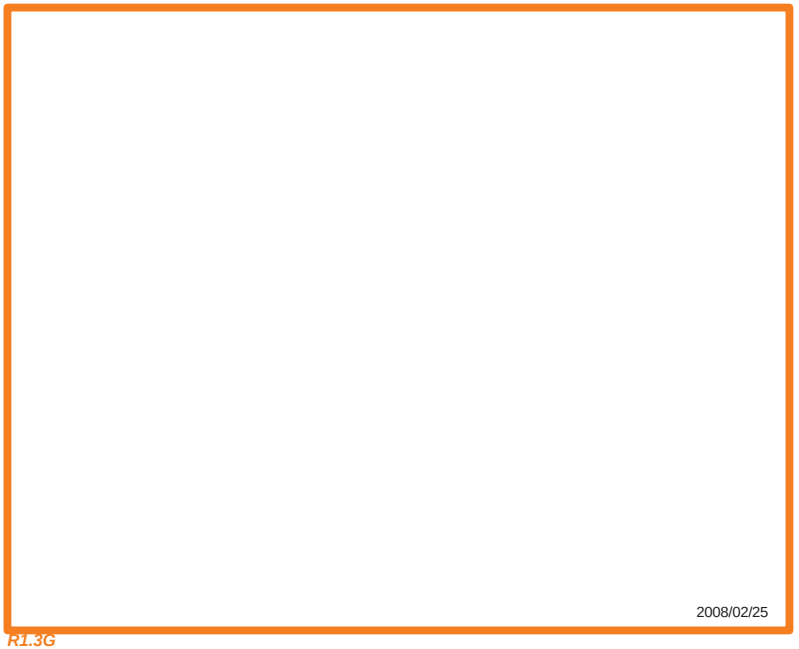
0414_1209

ASUSTek Computer INC.	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 57 of 66	

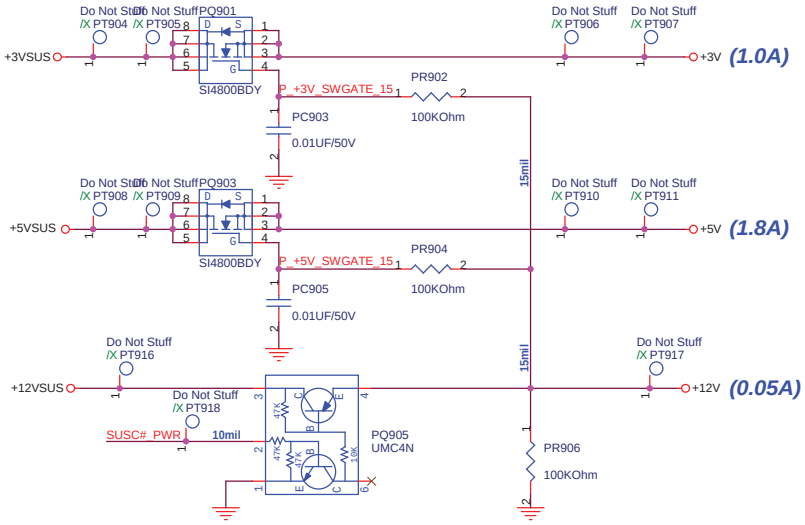
SUSB#_PWR POWER

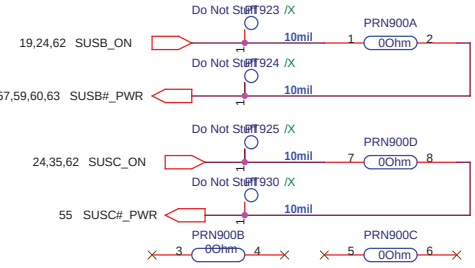






SUSC#_PWR POWER





0414_1209

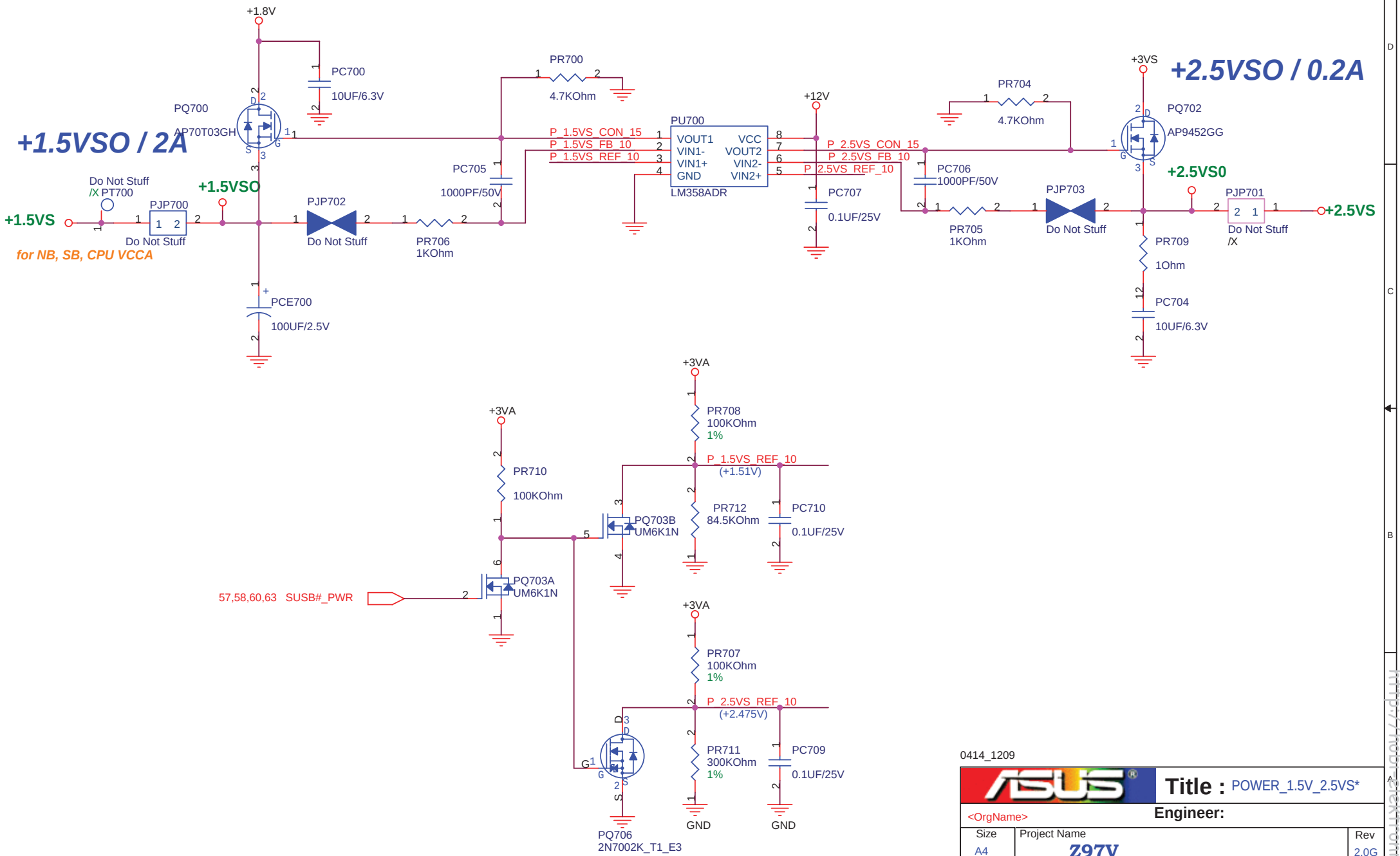
ASUSTek Computer INC.

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
A3	Z97V	2.0G

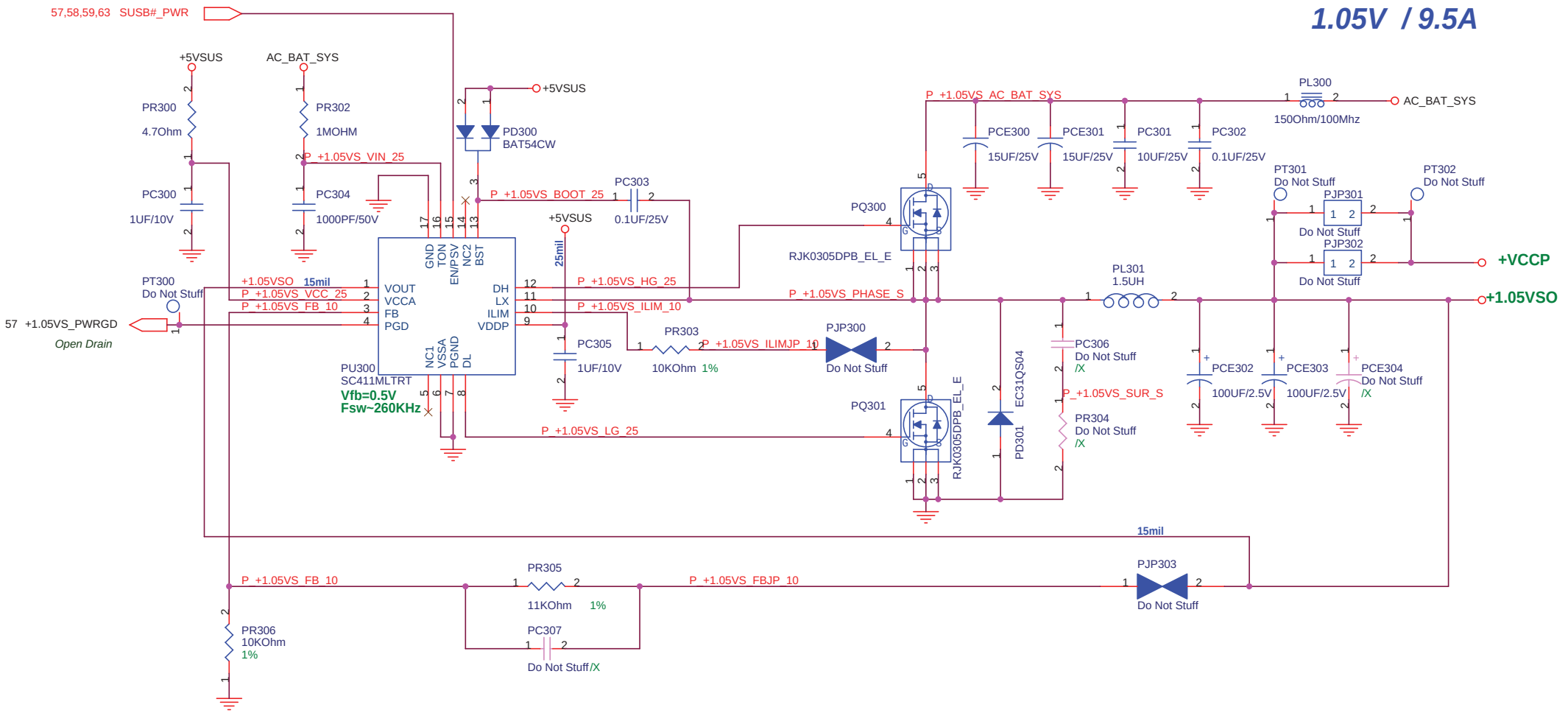
Date: Friday, May 09, 2008 Sheet 58 of 66



0414_1209

Title : POWER_1.5V_2.5VS*		
<OrgName>	Engineer:	
Size: A4	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 59 of 66	

1.05V / 9.5A



0414_1209

Title : POWER_1.05VS

<OrgName>

Engineer:

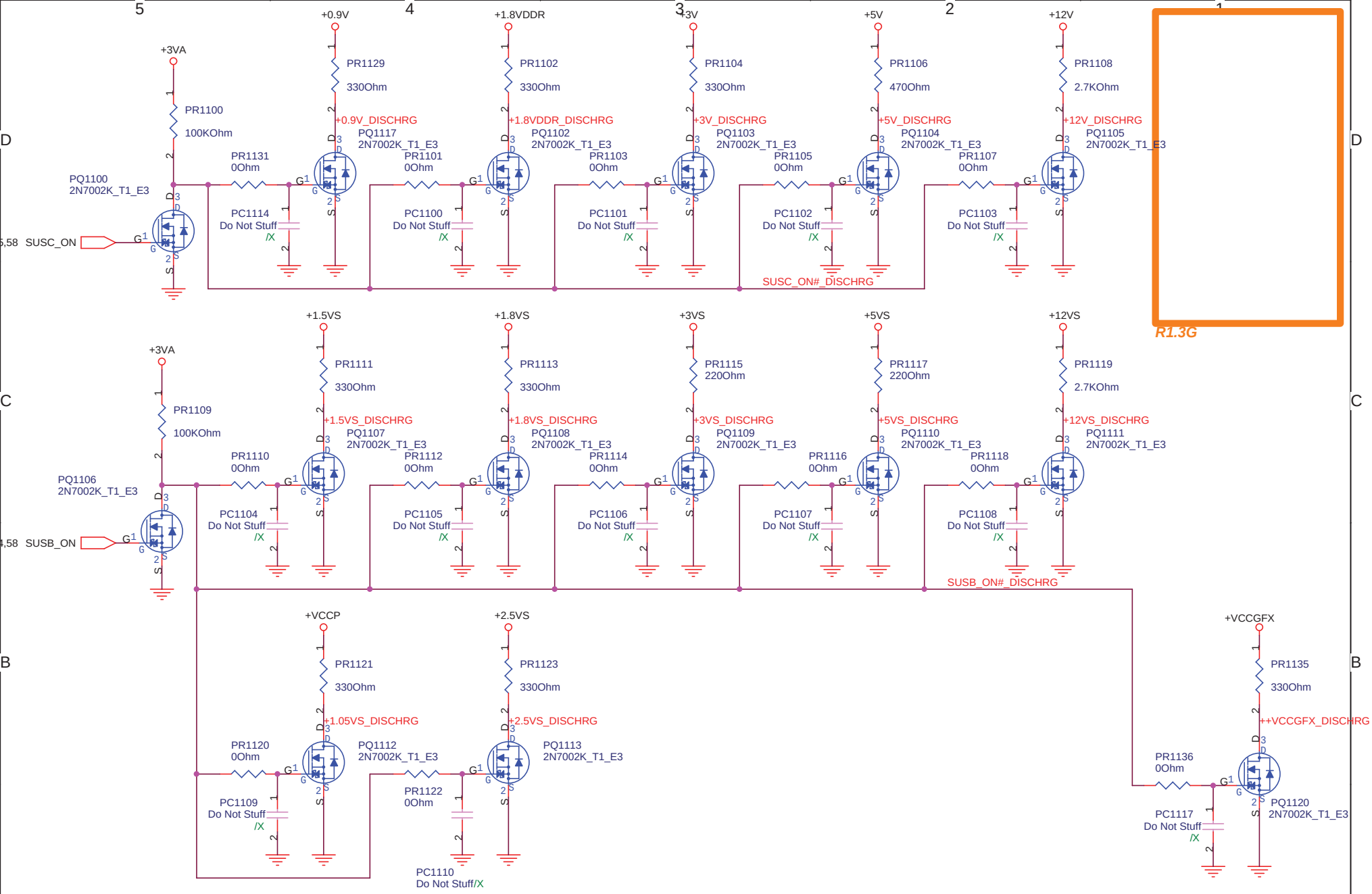
Size	Project Name	Rev
Custom		2.0G

Date: Friday, May 09, 2008 Sheet 60 of 66

R1.3G

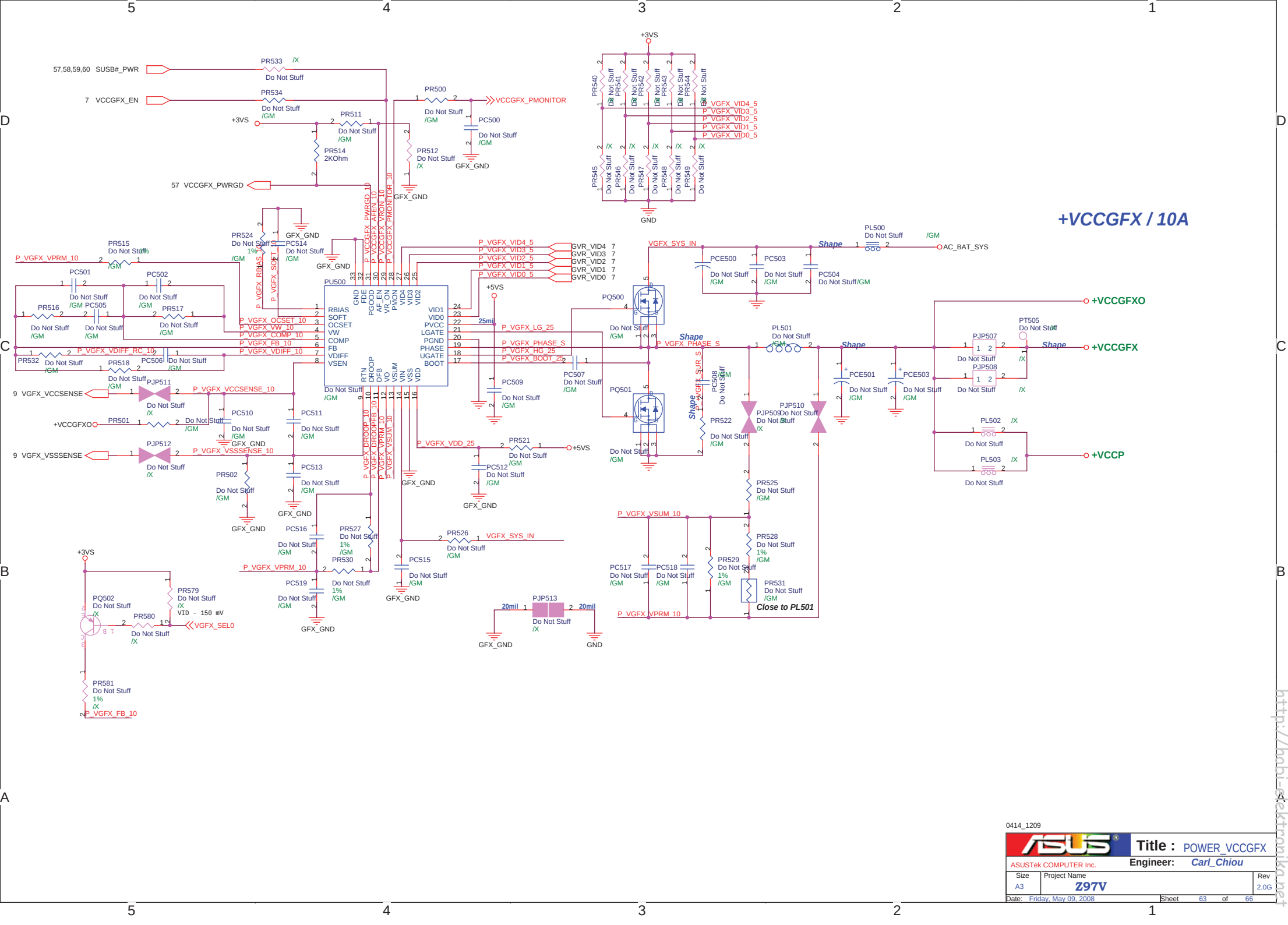
0414_1209

ASUSTek Computer INC.	Title : POWER-ON SEQ.	
	Engineer: Mike Lee	
Size: A3	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 61 of 66	



0414_1209

ASUSTek COMPUTER Inc.	Title : POWER_Discharge	
	Engineer: Carl_Chiou	
Size: Custom	Project Name: Z97V	Rev: 2.0G
Date: Friday, May 09, 2008	Sheet 62 of 66	



0414_1209

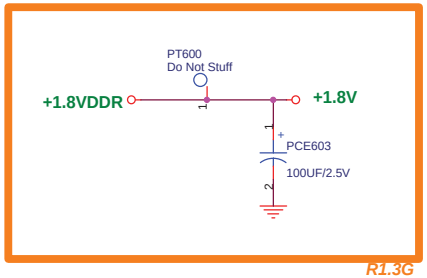
ASUSTek COMPUTER Inc.

Title : POWER_VCCGFX

Engineer: Carl_Chiou

Size	Project Name	Rev
A3	Z97V	2.0G

Date: Friday, May 09, 2008 Sheet 63 of 66



R1.3G

+1.8V / 6A

0414_1209

ASUSTek COMPUTER Inc.

Title : POWER_+1.8V

Engineer: Carl_Chiou

Size	Project Name	Rev
A3	Z97V	2.0G

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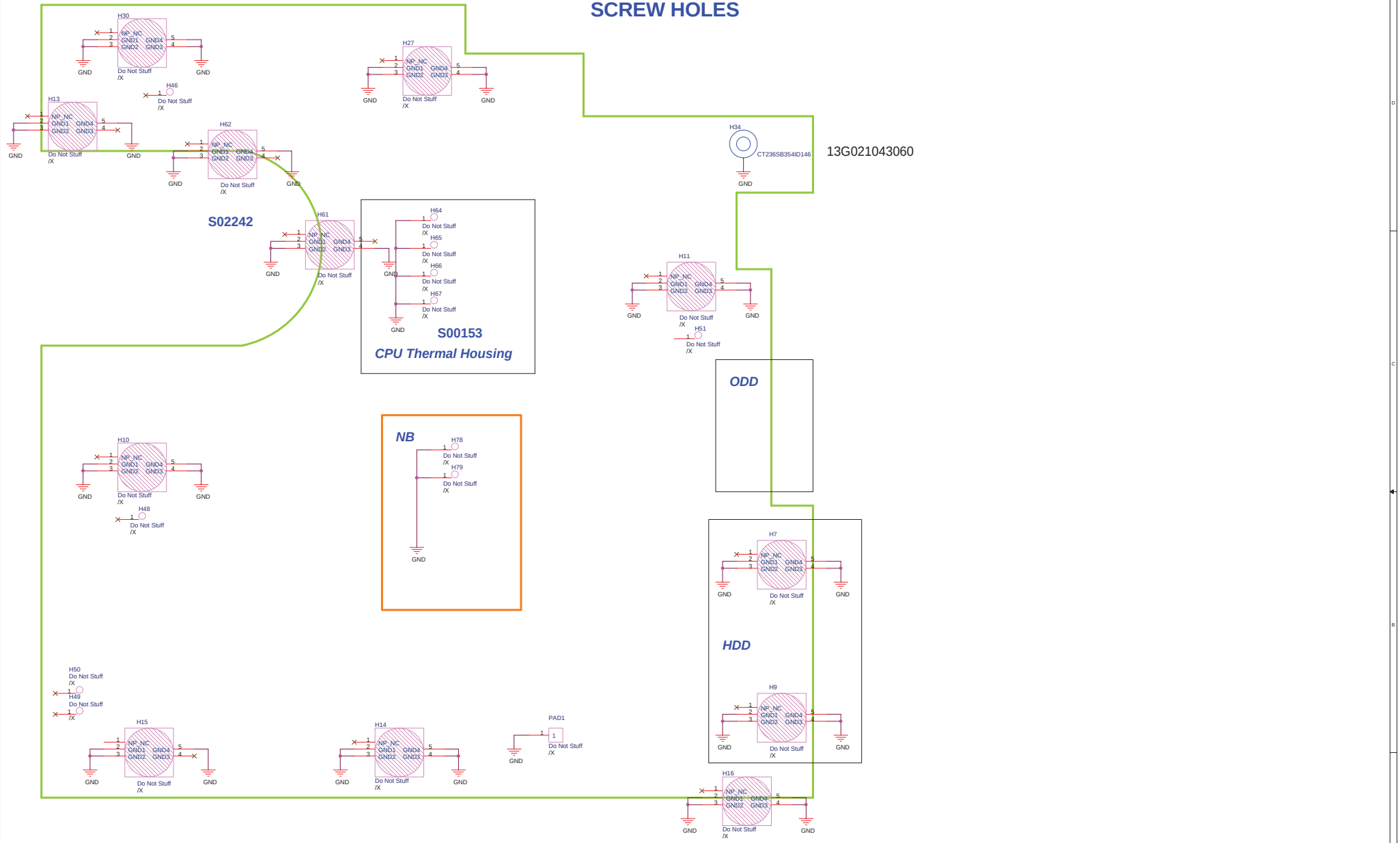
SCREW HOLES



0414_1209

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Mike Lee	
Size: C	Project Name: Z97V	Rev: 2.0G
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