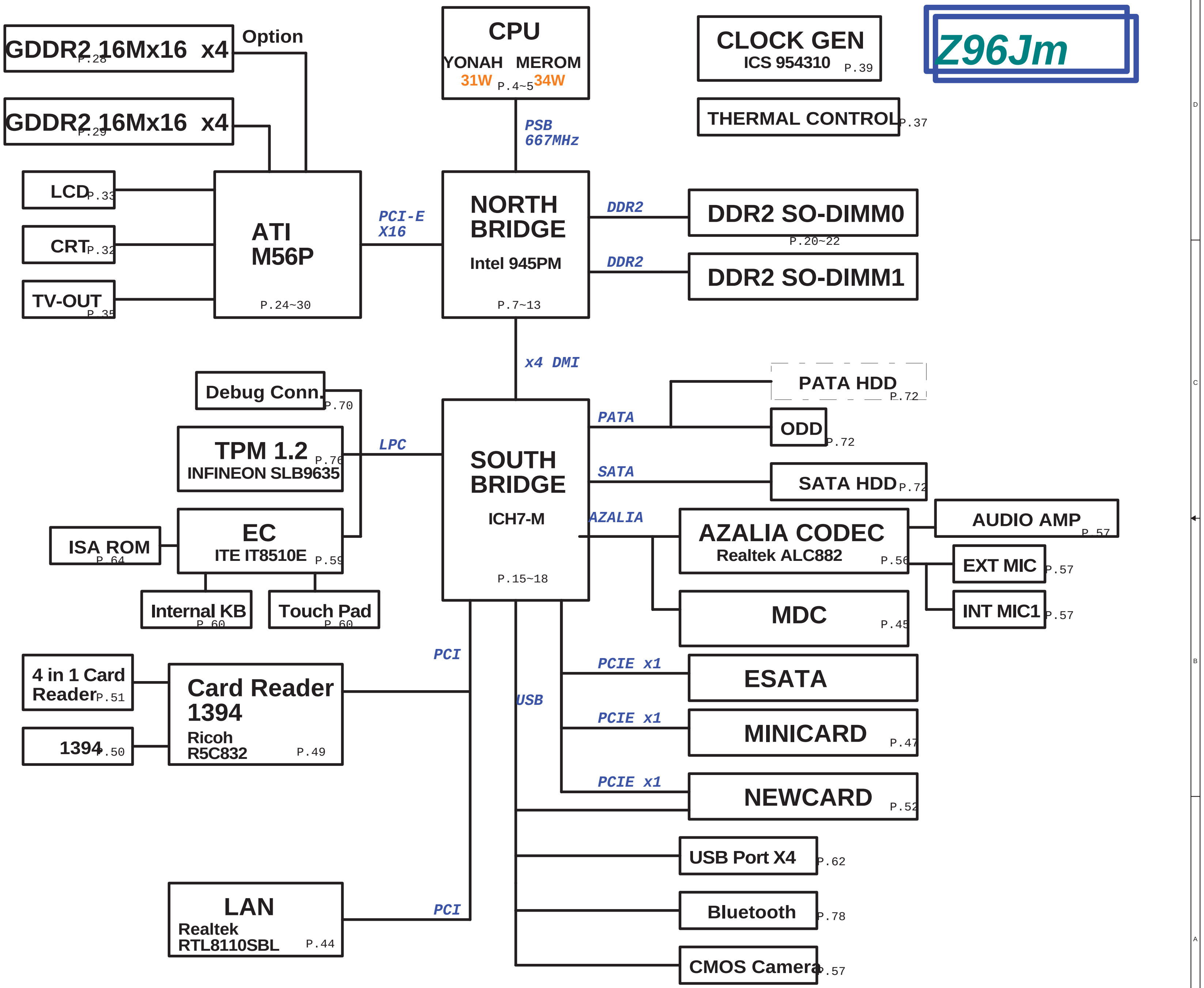


ASUS

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 1 of 91

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

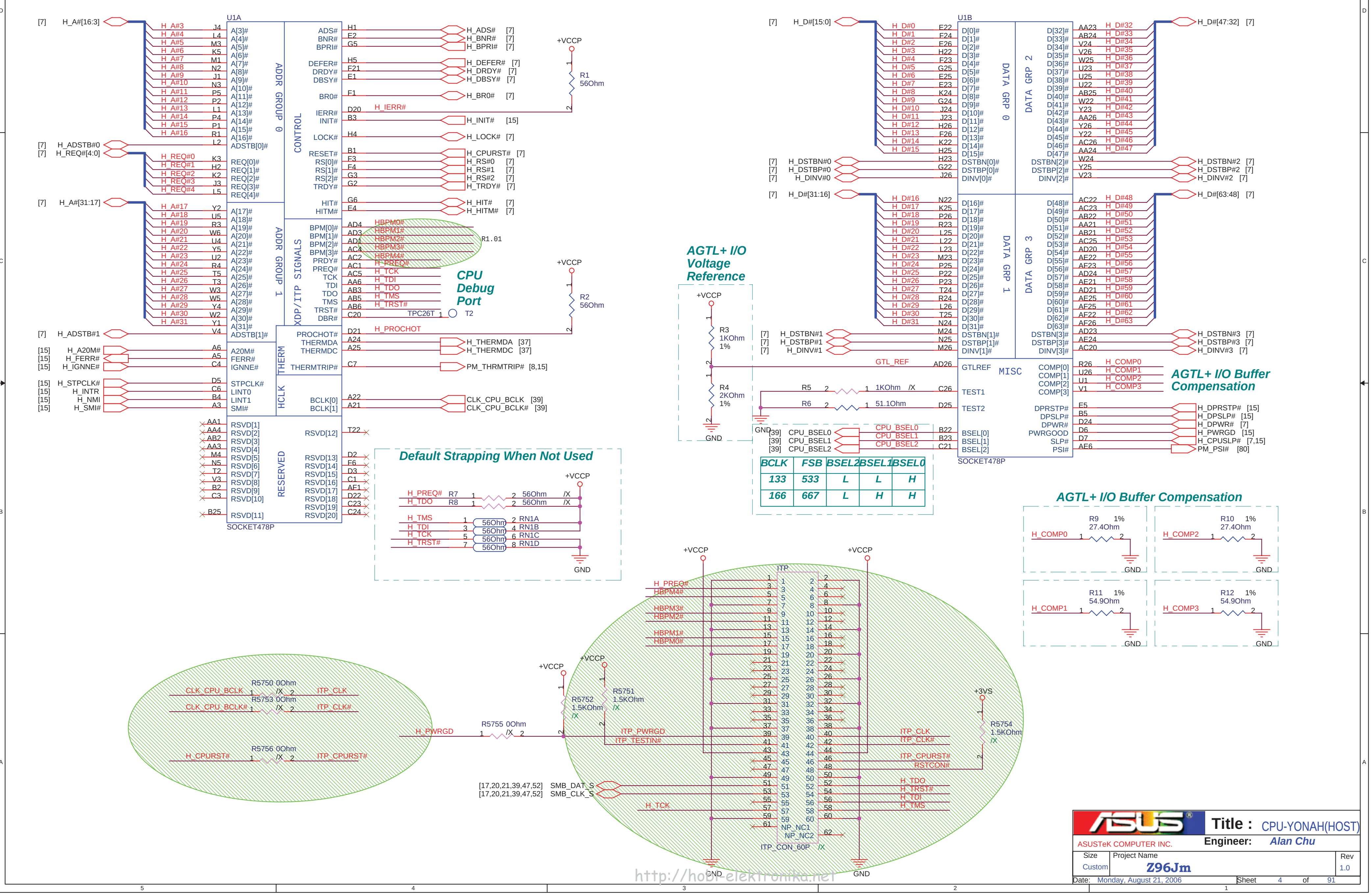
Pin	Pin Name	Signal Name	Type	Default
48	GPH0	VSUS_ON	O	L GPI
54	GPH1	VSUS_GD#	I	H GPI
55	GPH2	CPUPWR_GD#	I	H GPI
69	GPH3	PM_PWRBTN#	O	H GPI
70	GPH4	SUSC_ON	O	L GPI
75	GPH5	SUSB_ON	O	L GPI
76	GPH6	CPU_VRON	O	L GPI
105	GPH7	PM_RSMRST#	O	L GPI
148	GPI0	ICH7_PWROK	O	L GPI
149	GPI1	/	O	GPI
152	GPI2	MCHOK	I	L GPI
155	GPI3	CHG_EN#	O	H GPI
156	GPI4	PRECHG	O	L GPI
168	GPI5	BAT_LL#	O	H GPI
174	GPI6	BAT_LEARN	O	L GPI
93	ADC8	KID0	I	
94	ADC9	KID1	I	
101	DAC2	BL_PWM_DA	O	
102	DAC3	BATSEL_2P#	O	

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0100110X (98)

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

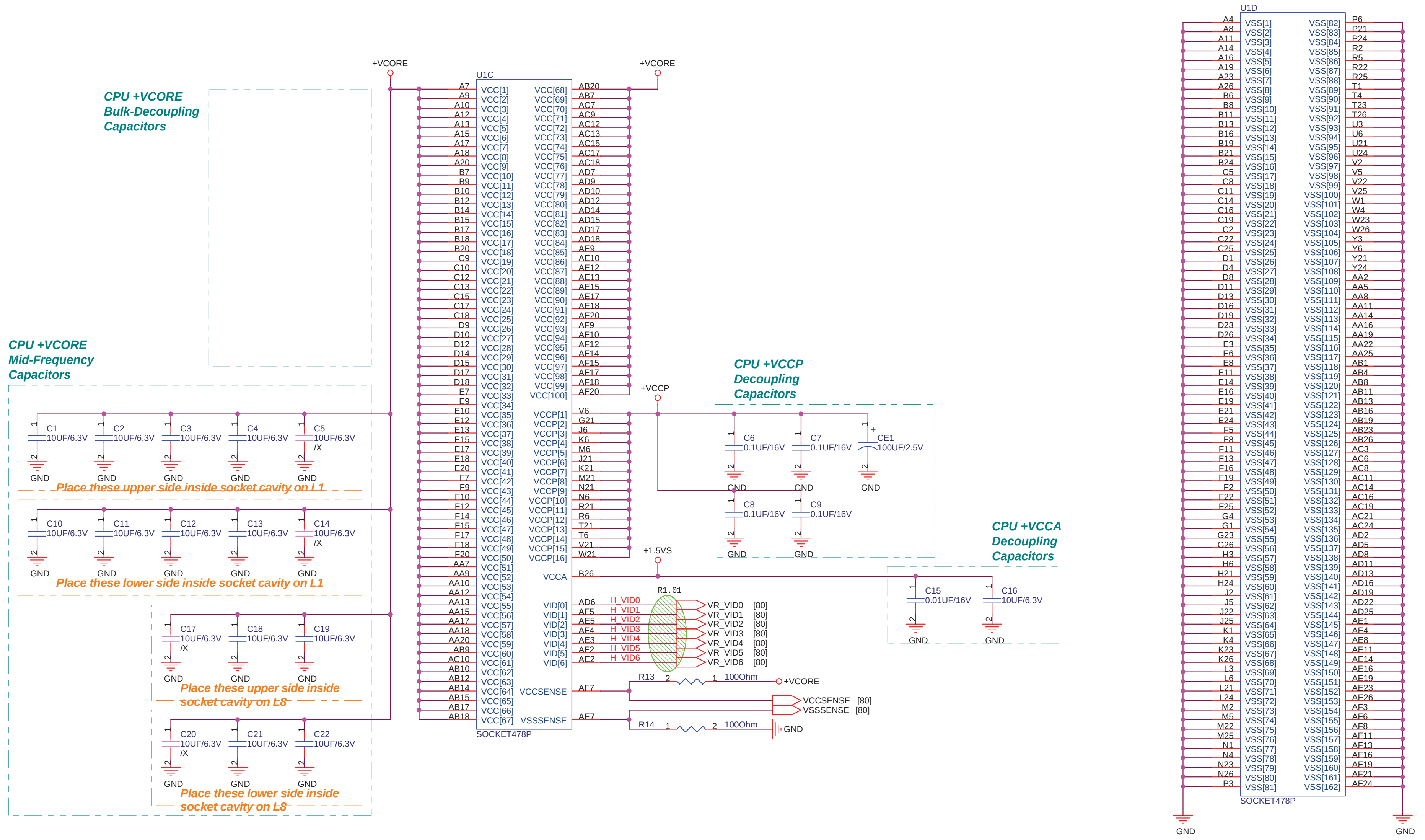
ASUSTeK COMPUTER INC.

Title : CPU-YONAH(HOST)

Engineer: Alan Chu

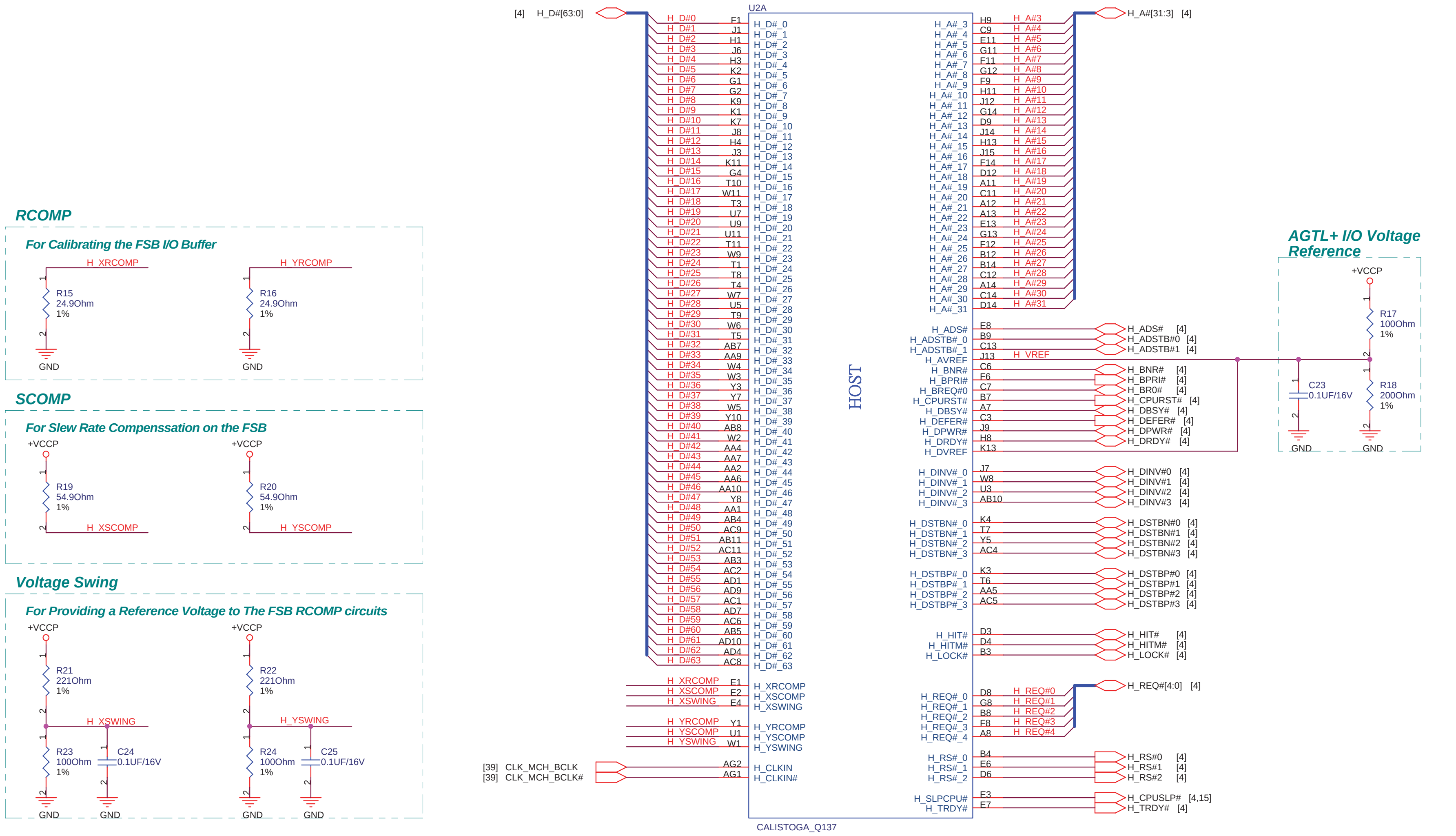
Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 4 of 91



+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 5 of 91		



ASUSTeK COMPUTER INC.

Title : NB-945PM(HOST)

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 7 of 91

GMCH Strapping

CFG5 : DMI Strap
- 0 = DMI x2
- 1 = DMI x4 (D)

MCH_CFG_5 — R25 1KOhm /X — GND

CFG[13:12] : GMCH Test Mode
- 00= Partial CLK Gating Disable
- 01 = XOR Mode Enable
- 10 = All Z Mode Enable
- 11 = Normal Operation (D)

CFG7 : CPU Strap
- 0 = DT/Transpotable CPU
- 1 = Mobile CPU (D)

MCH_CFG_7 — R26 1KOhm /X — GND

CFG15 : ICH RESET Disable
- 0 = ICH Reset Disable
- 1 = Normal Operation (D)

MCH_CFG_15 — R27 1KOhm /X — GND

CFG9 : PCIE Graphic Lane
- 0 = Reverse Lane
- 1 = Normal Operation (D)

MCH_CFG_9 — R30 1KOhm — GND

CFG16 : FSB Dynamic ODT
- 0 = Dynamic ODT Disable
- 1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 1KOhm /X — GND

CFG10 : HOST PLL VCO Select
- 0 = Reserved
- 1 = Mobility (D)

MCH_CFG_10 — R34 1KOhm /X — GND

CFG18 : VCC Select
- 0 = 1.05V (D)
- 1 = 1.5V

MCH_CFG_18 — R35 1KOhm /X — +2.5VS

CFG11 : PSB 4x CLK Enable
- 0 = 4x Enable
- 1 = 8x Enable (D)

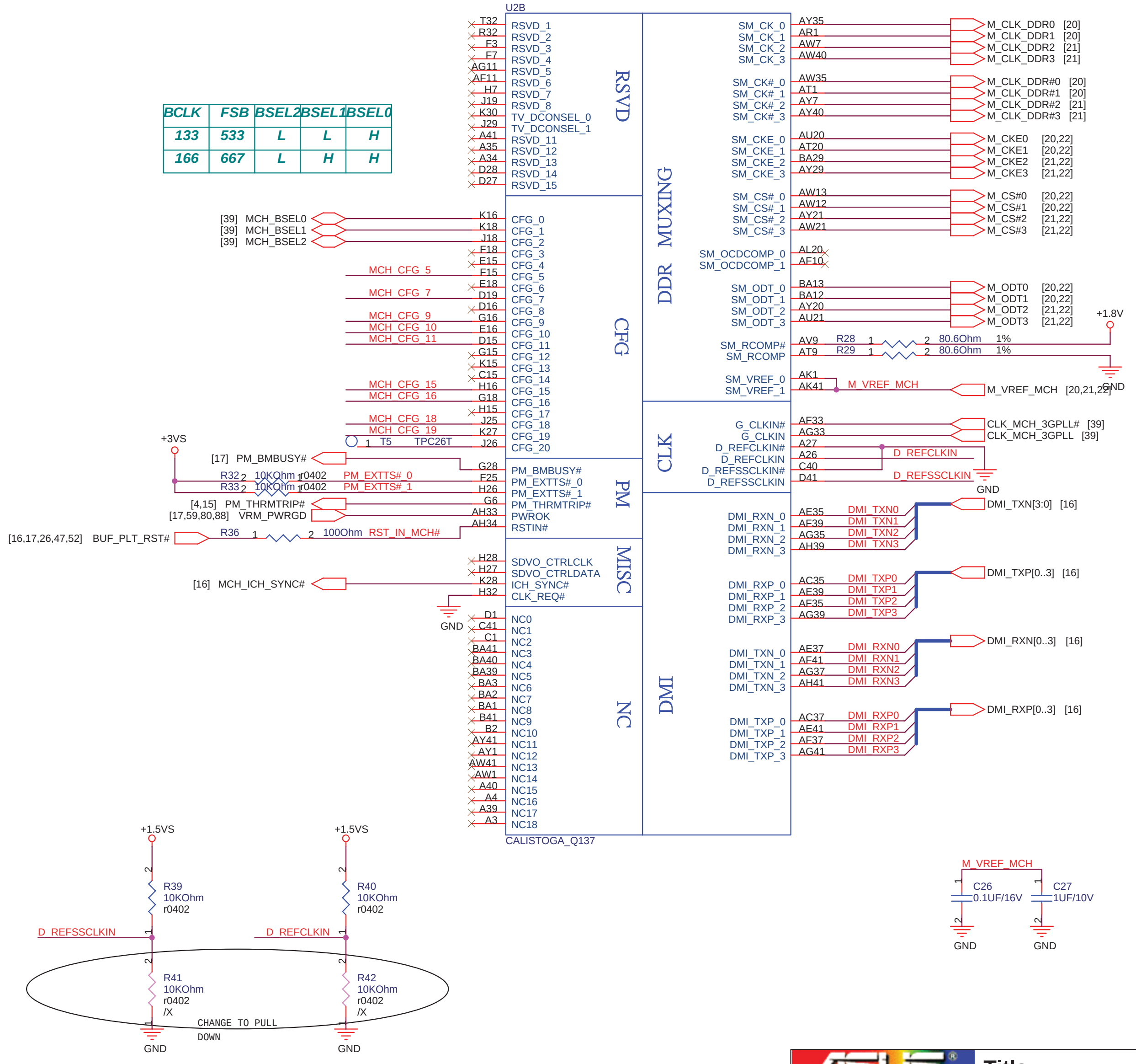
MCH_CFG_11 — R37 1KOhm /X — GND

CFG19 : DMI Lane Reversal
- 0 = Normal Operation (D)
- 1 = Lanes Reversed

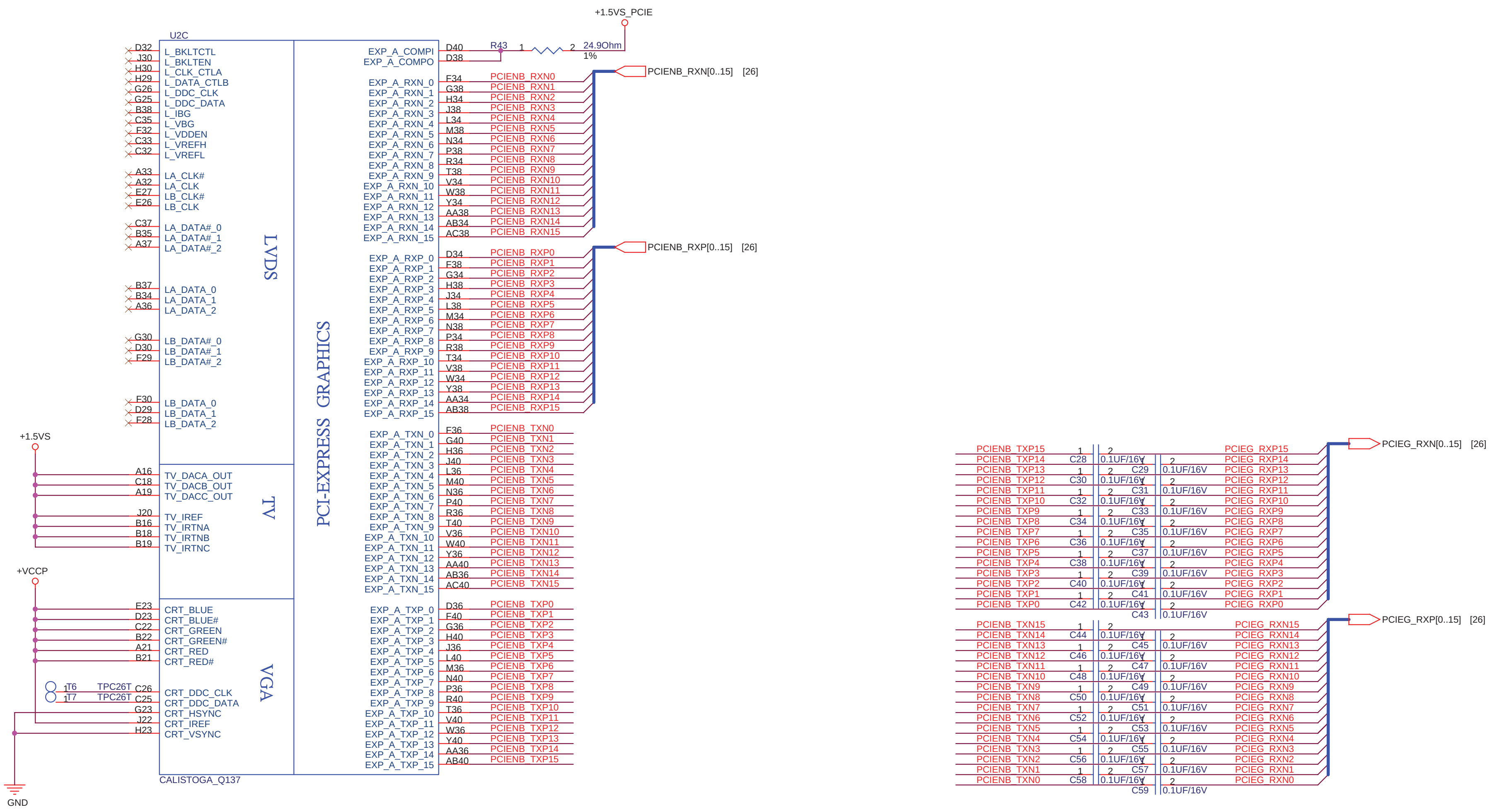
MCH_CFG_19 — R38 1KOhm /X — +2.5VS

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

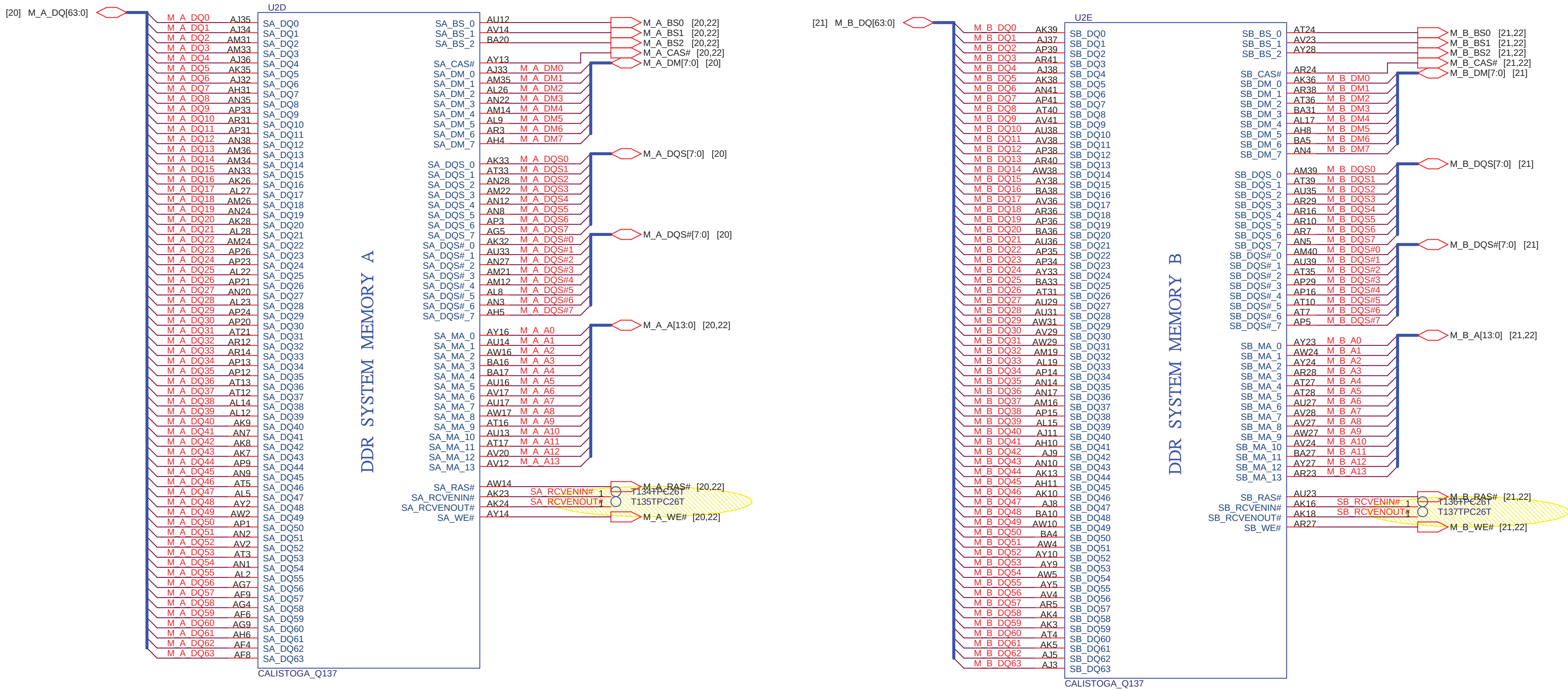
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



ASUSTeK COMPUTER INC.	Title : NB-945PM(DMI & CFG)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 8	of 91	

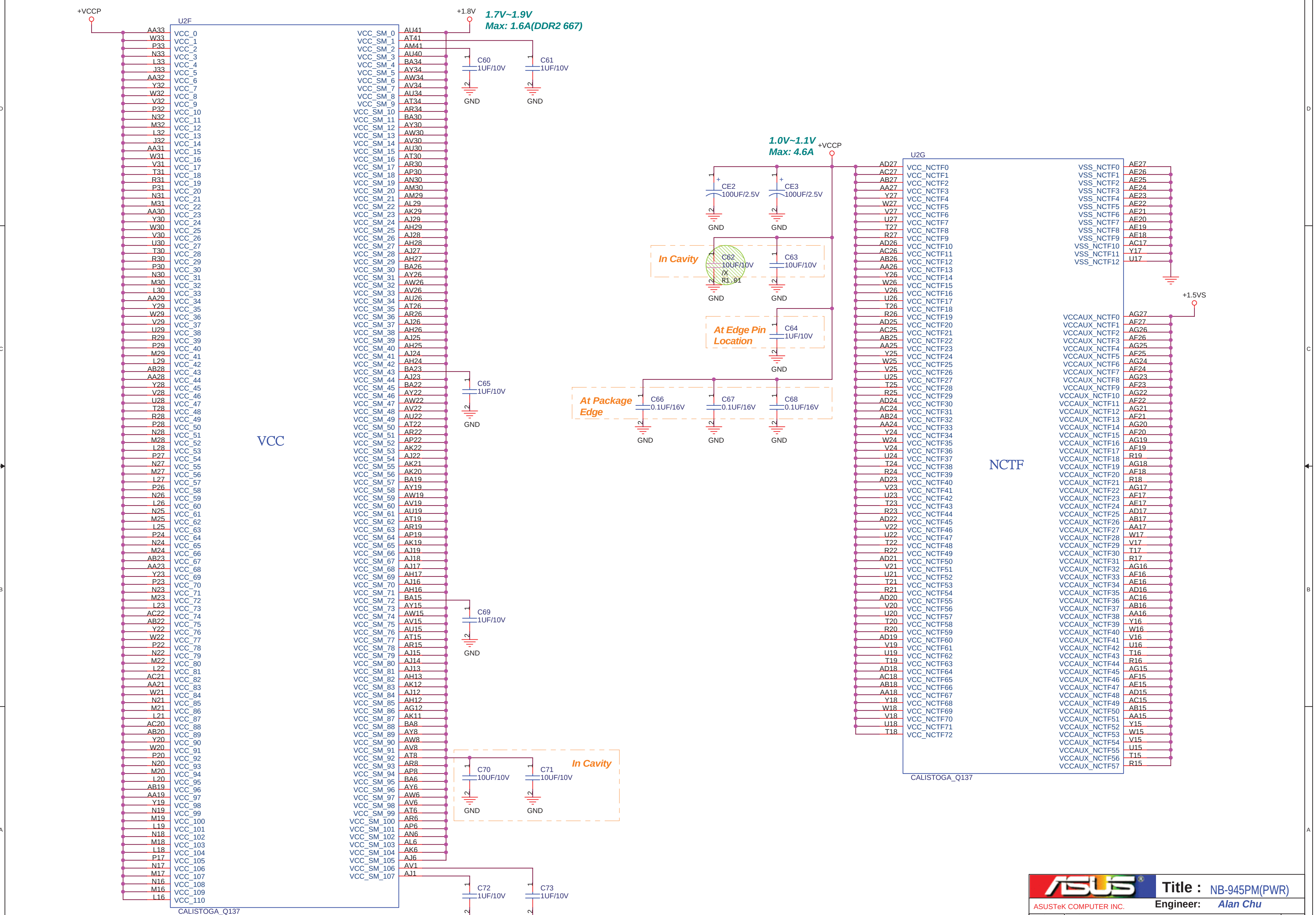


ASUSTeK COMPUTER INC.	Title : NB_945PM(GRAPHIC)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 9 of 91		



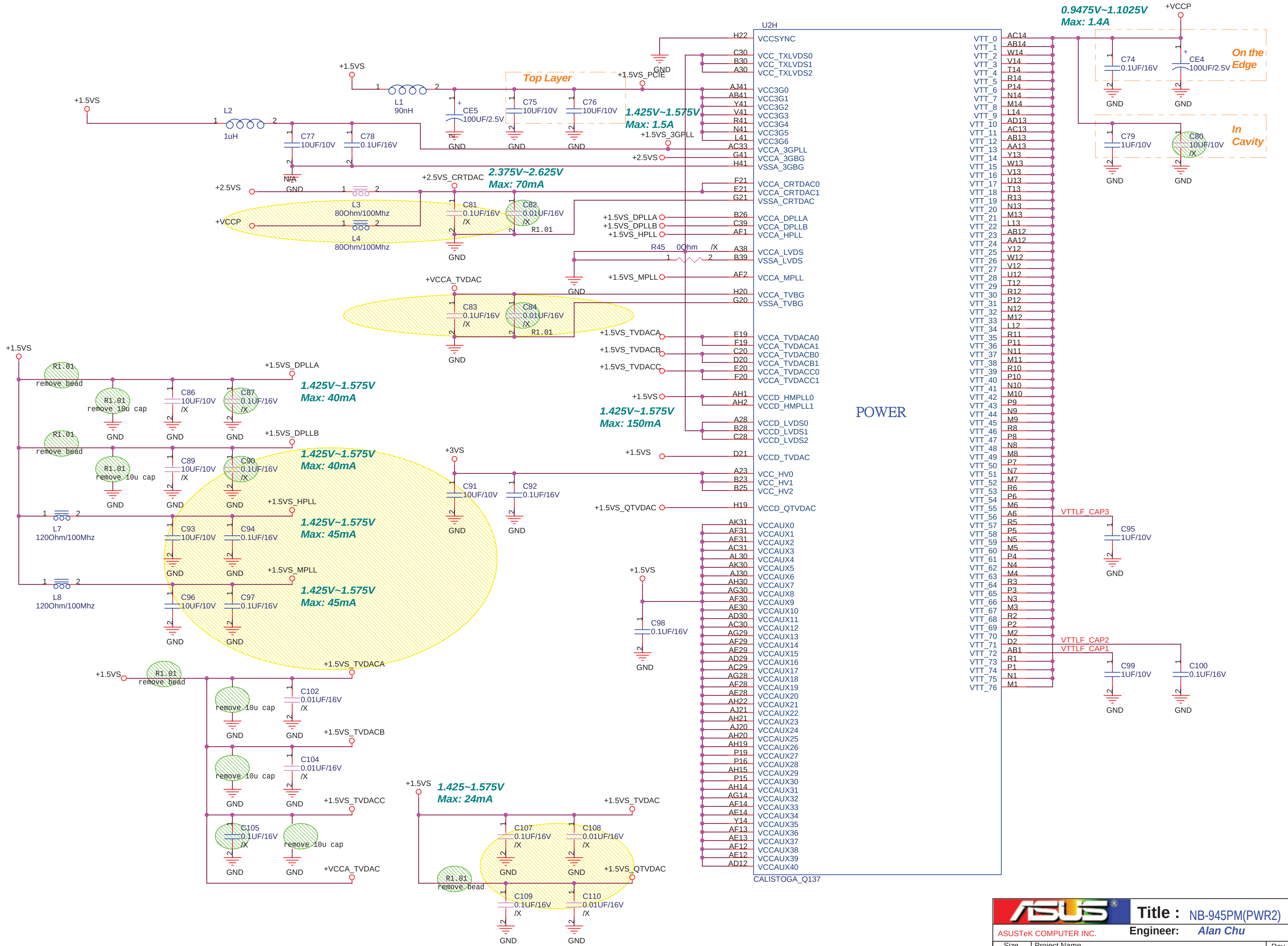
ASUSTeK COMPUTER INC.

Title :	NB-945PM(DDR2)	
Engineer:	Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 10 of 91	

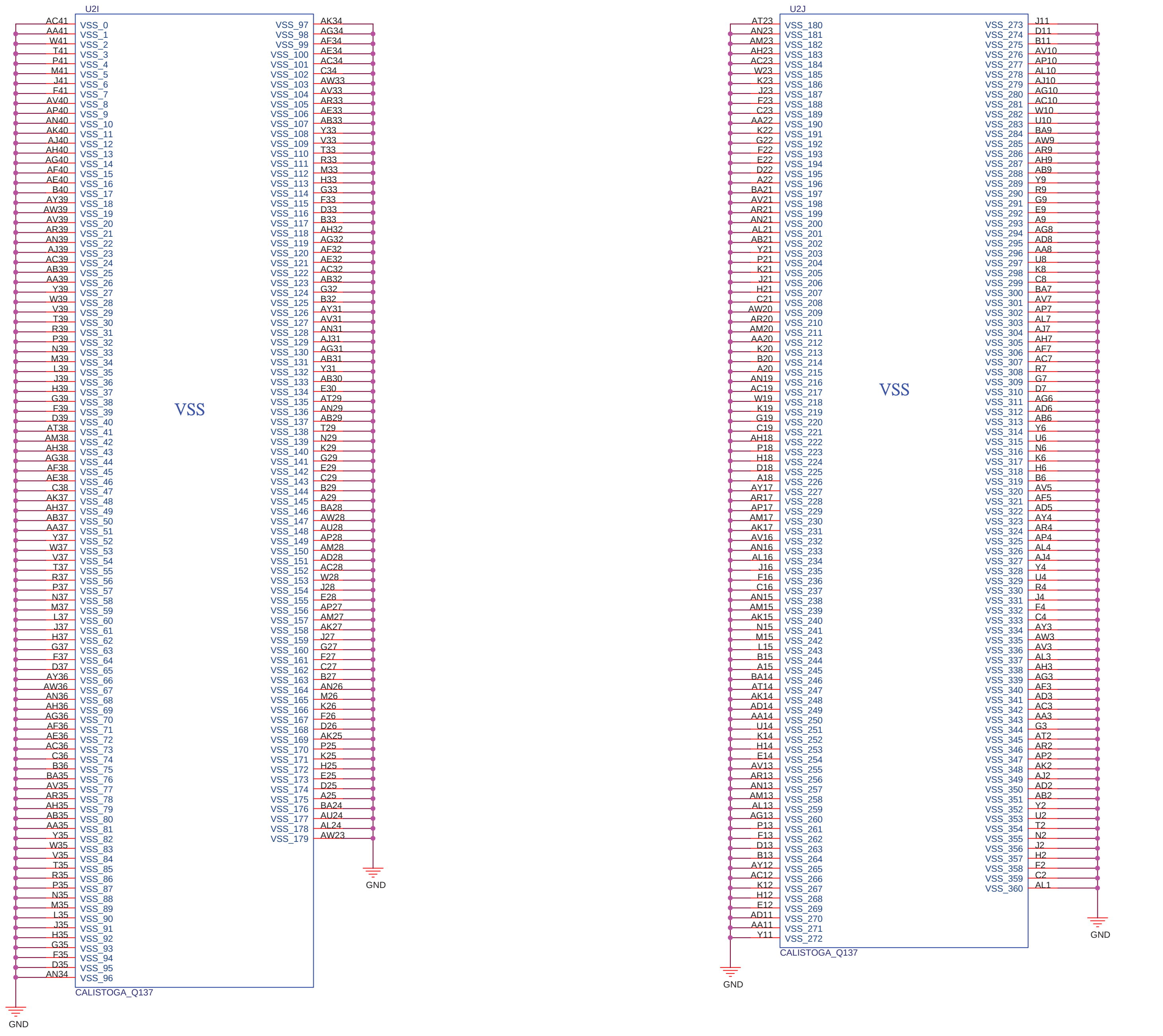


ASUSTeK COMPUTER INC.

Title : NB-945PM(PWR)		
Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 11 of 91	



ASUSTeK COMPUTER INC.	Title : NB-945PM(PWR2)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 12 of 91		



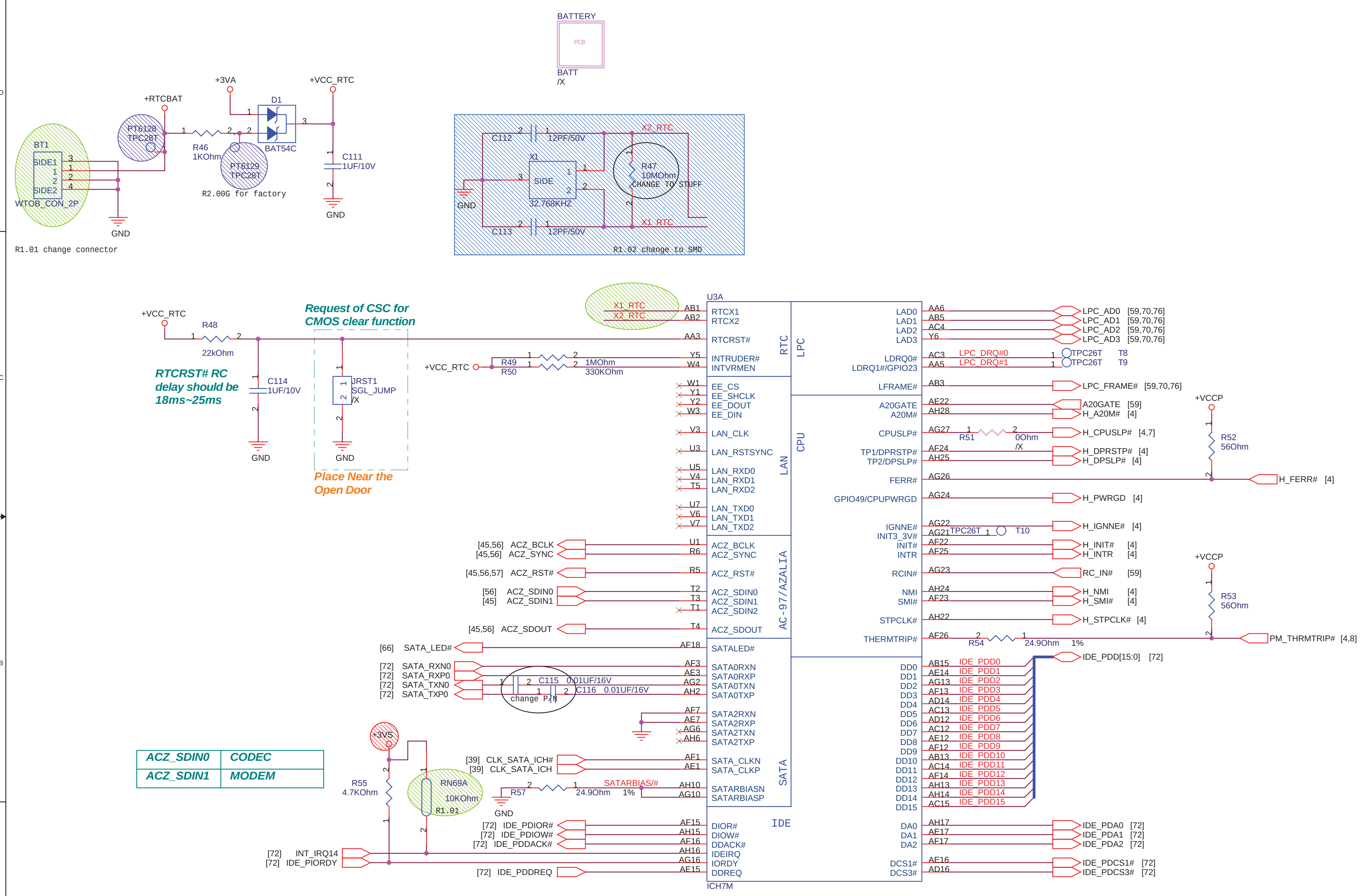
Title : NB-945PM(GND)

ASUSTeK COMPUTER INC.

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 13 of 91



ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM

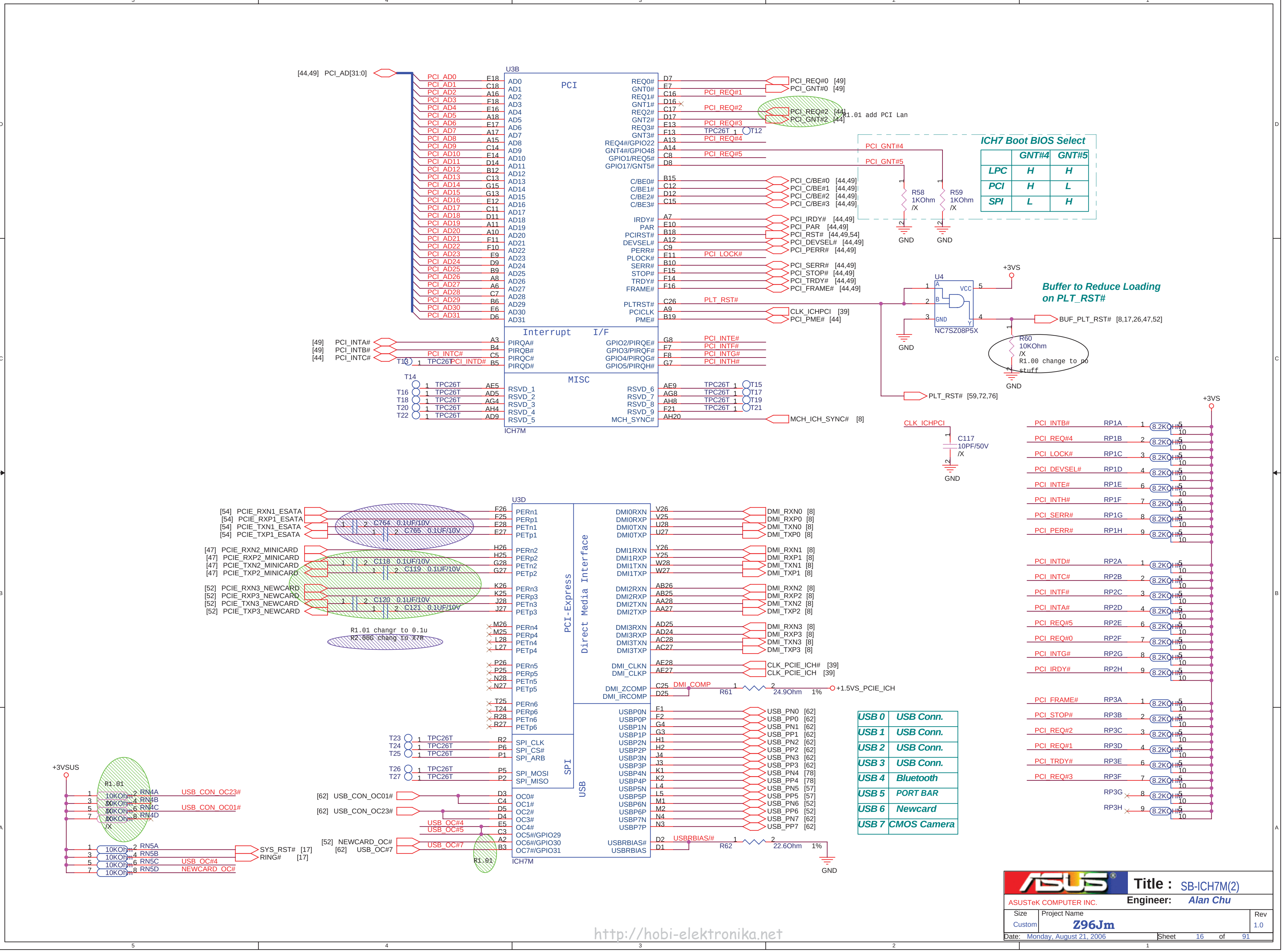
ASUSTeK COMPUTER INC.

Title : SB-ICH7-M(1)

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 15 of 91



ICH7 Boot BIOS Select

	GNT#4	GNT#5
LPC	H	H
PCI	H	L
SPI	L	H

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	Bluetooth
USB 5	PORT BAR
USB 6	Newcard
USB 7	CMOS Camera

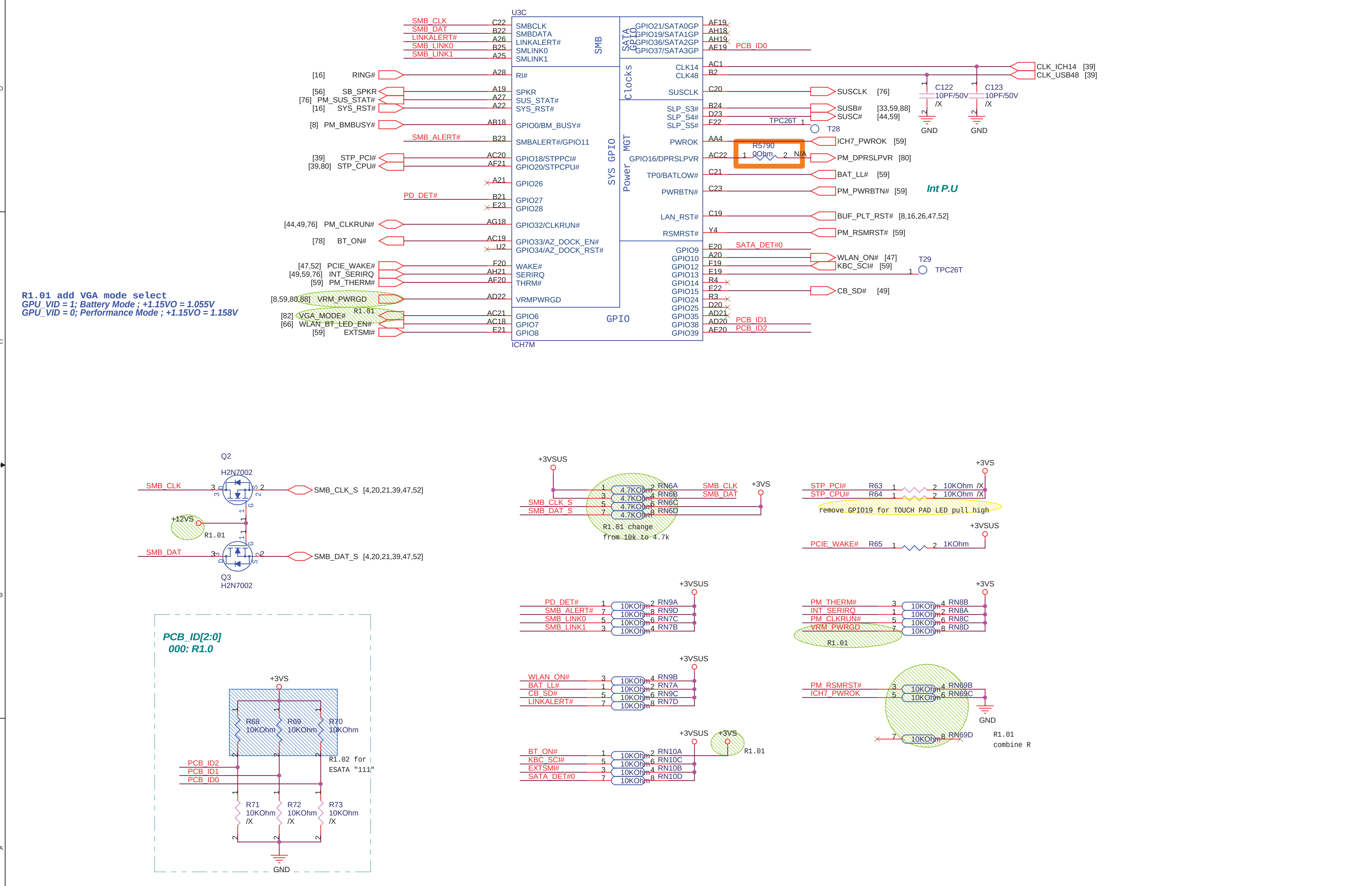
ASUSTeK COMPUTER INC.

Title : SB-ICH7M(2)

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 16 of 91



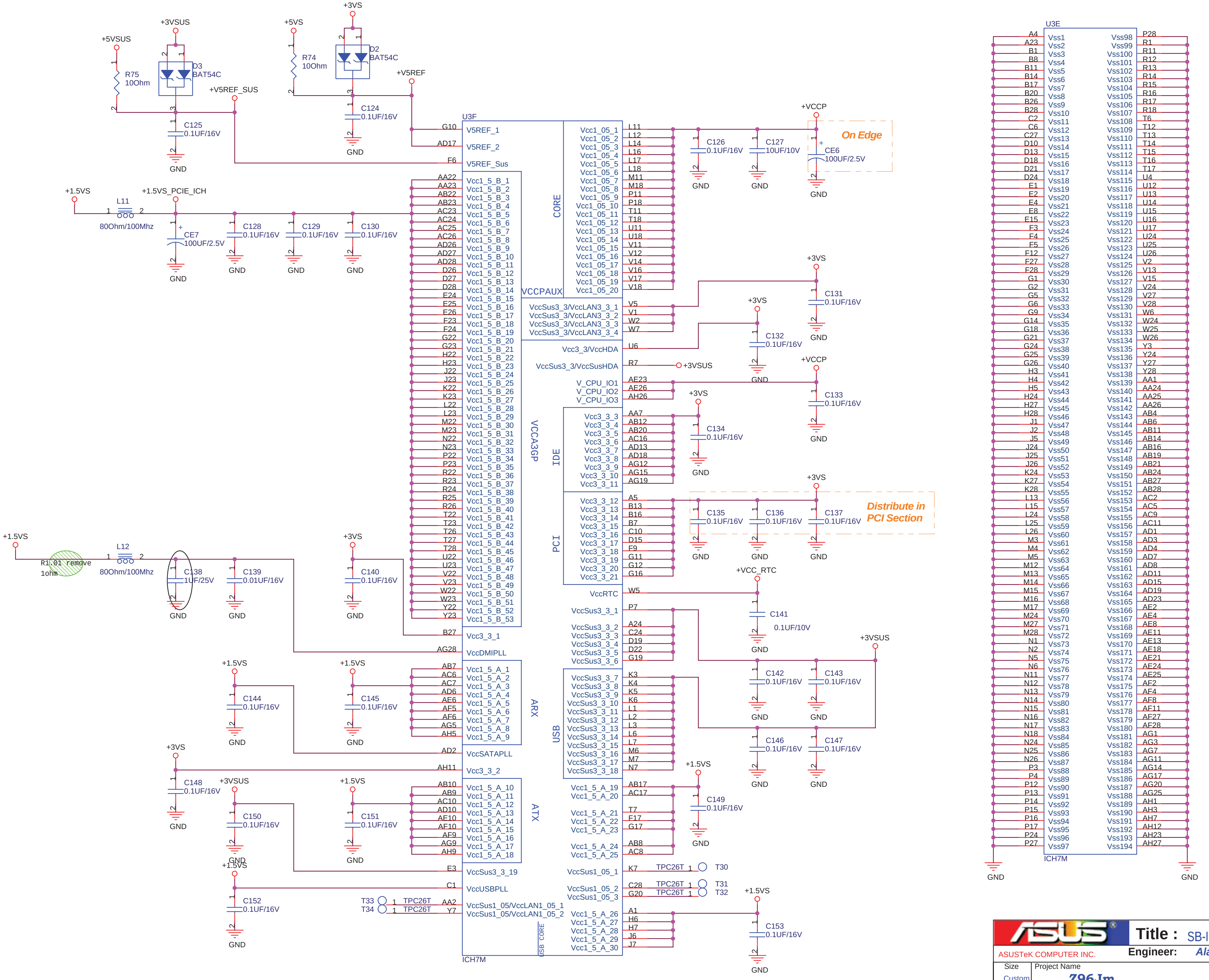
ASUSTeK COMPUTER INC

Title : SB-ICH7M(3)

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 17 of 91



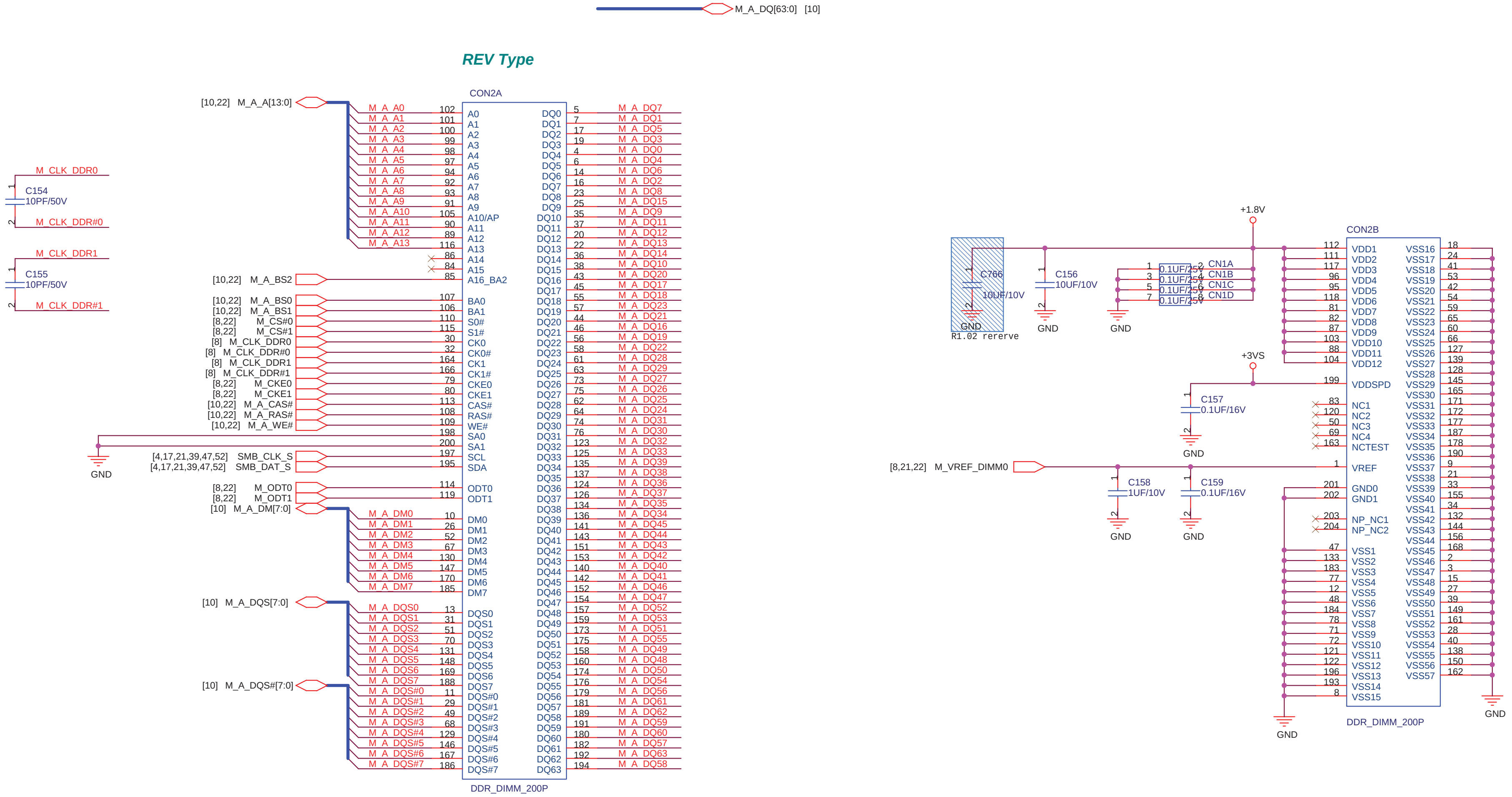
ASUSTeK COMPUTER INC.

Title : SB-ICH7M(PWR)

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 18 of 91



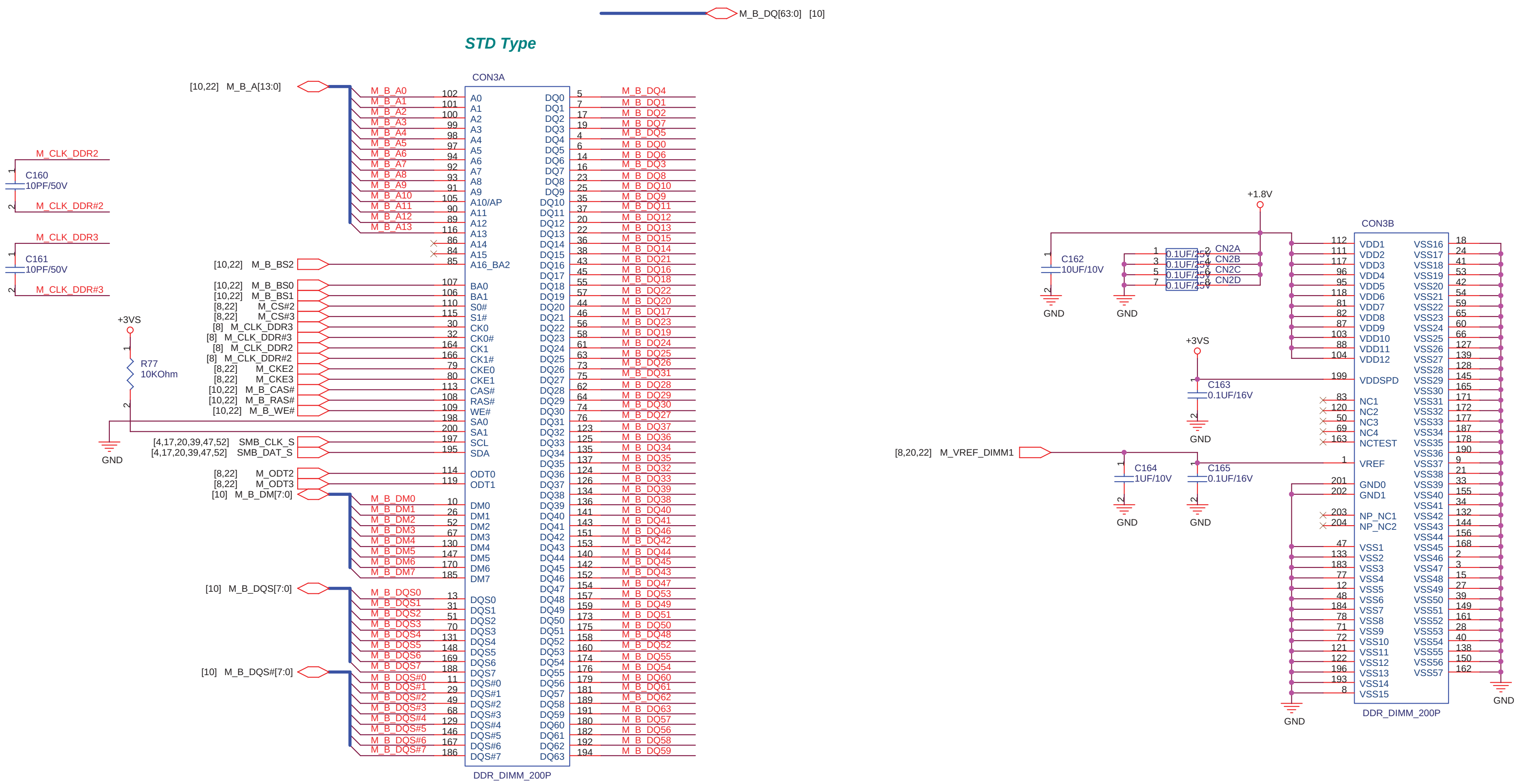
Title : DDR2 SO-DIMM0

ASUSTeK COMPUTER INC.

Engineer: *Alan Chu*

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 20 of 91



ASUS

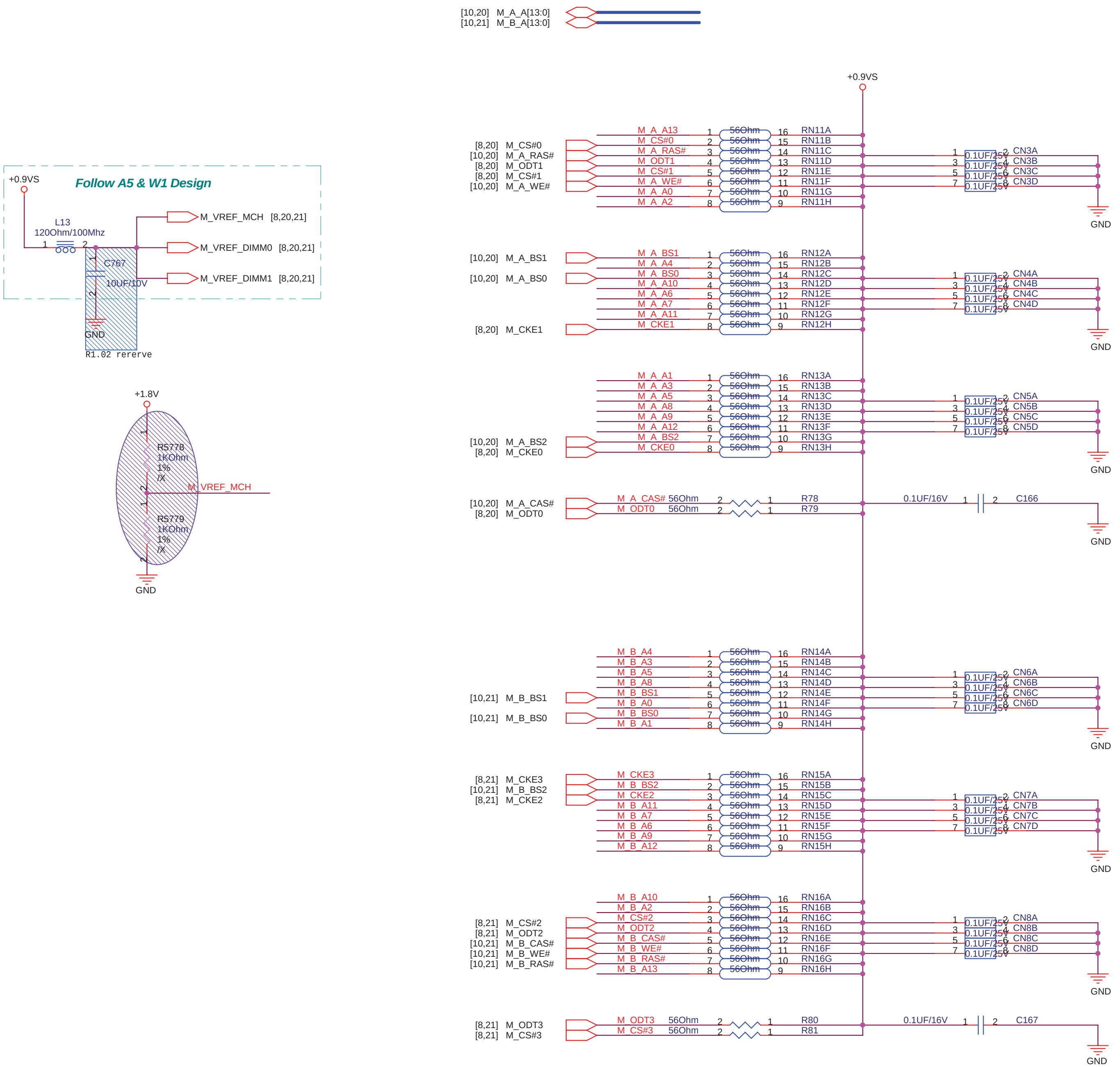
ASUSTeK COMPUTER INC. NB1

Title : DDR2 SO-DIMM1

Engineer: Alan Chu

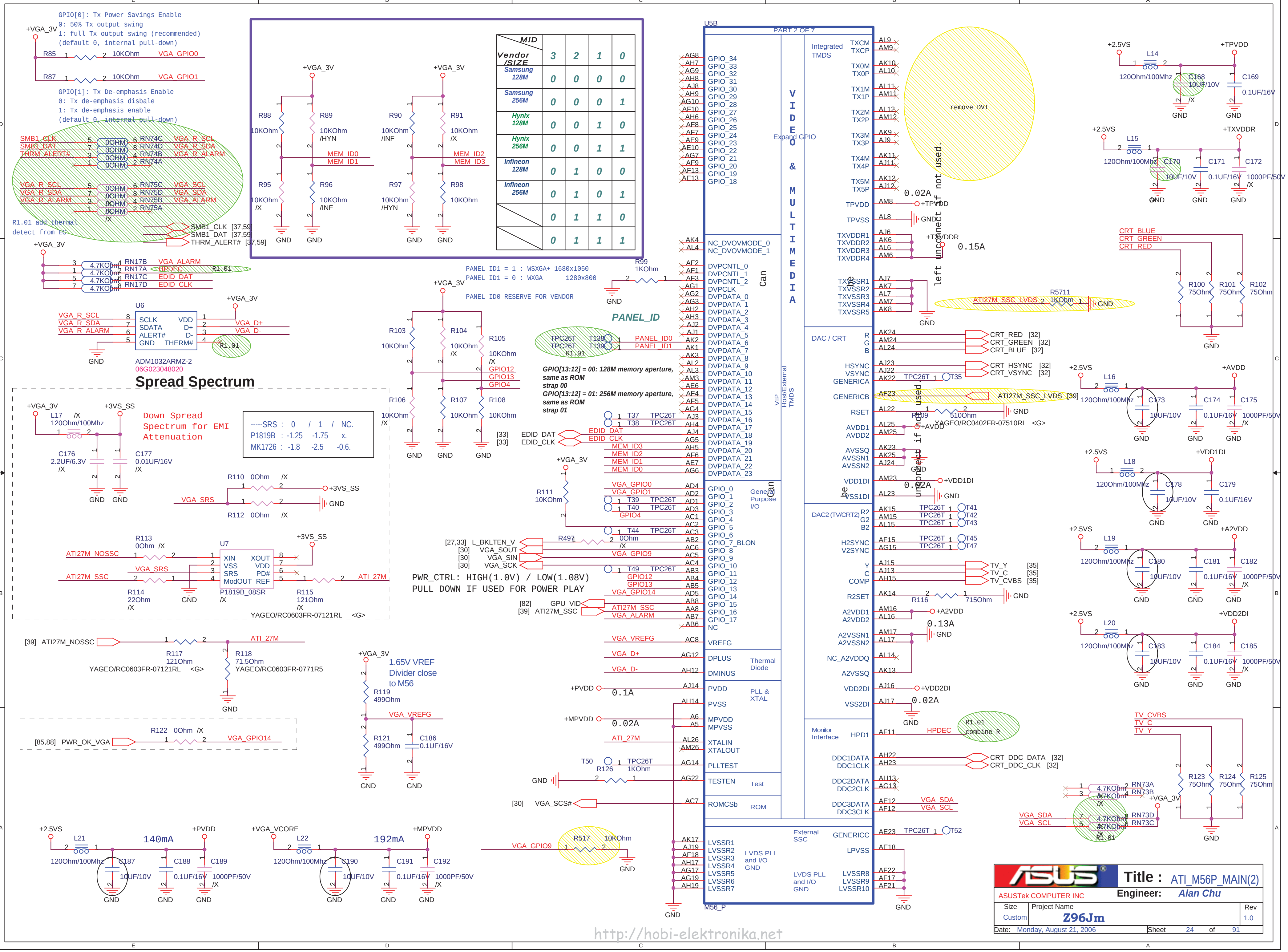
Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 | Sheet 21 of 91

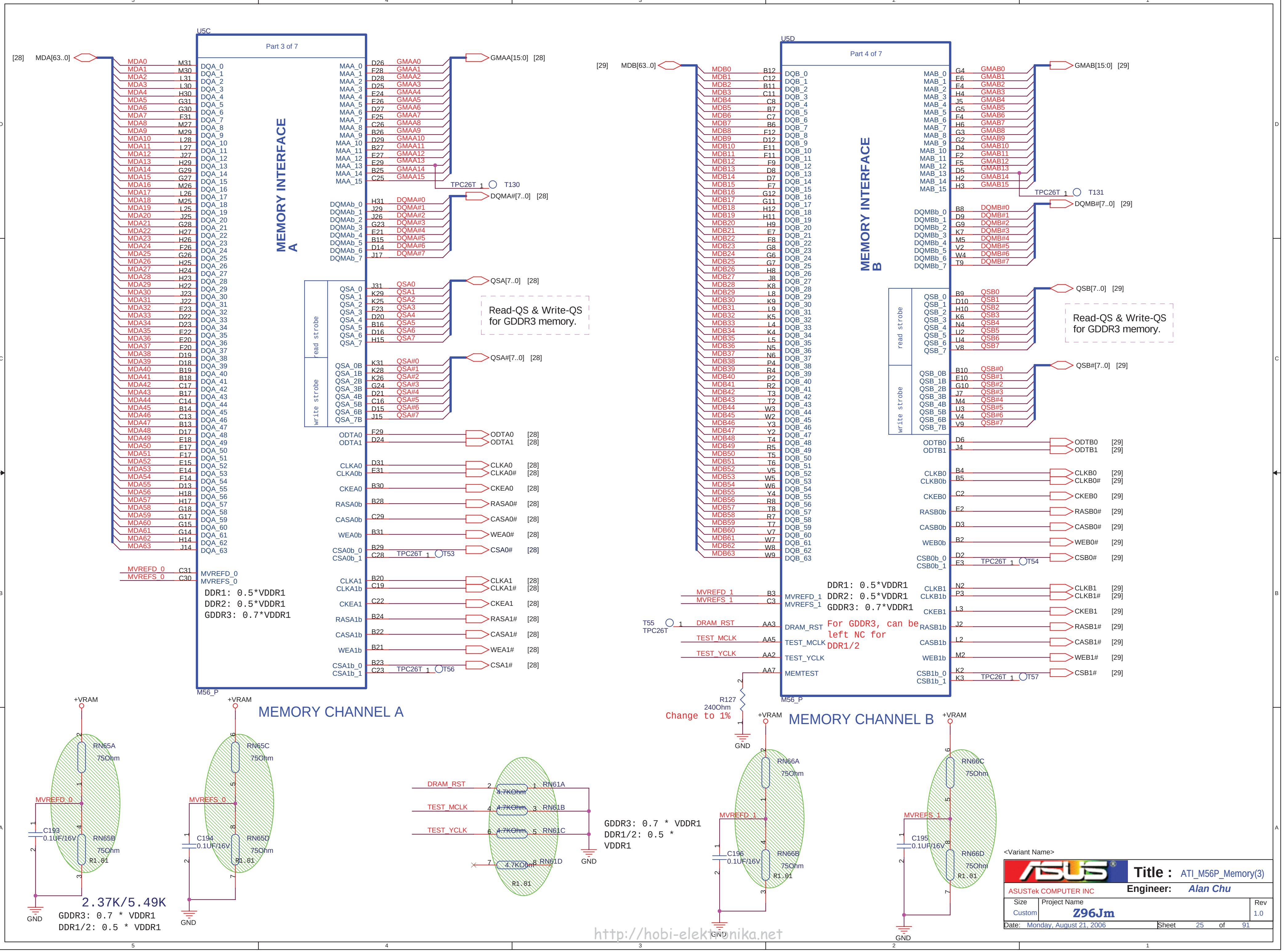


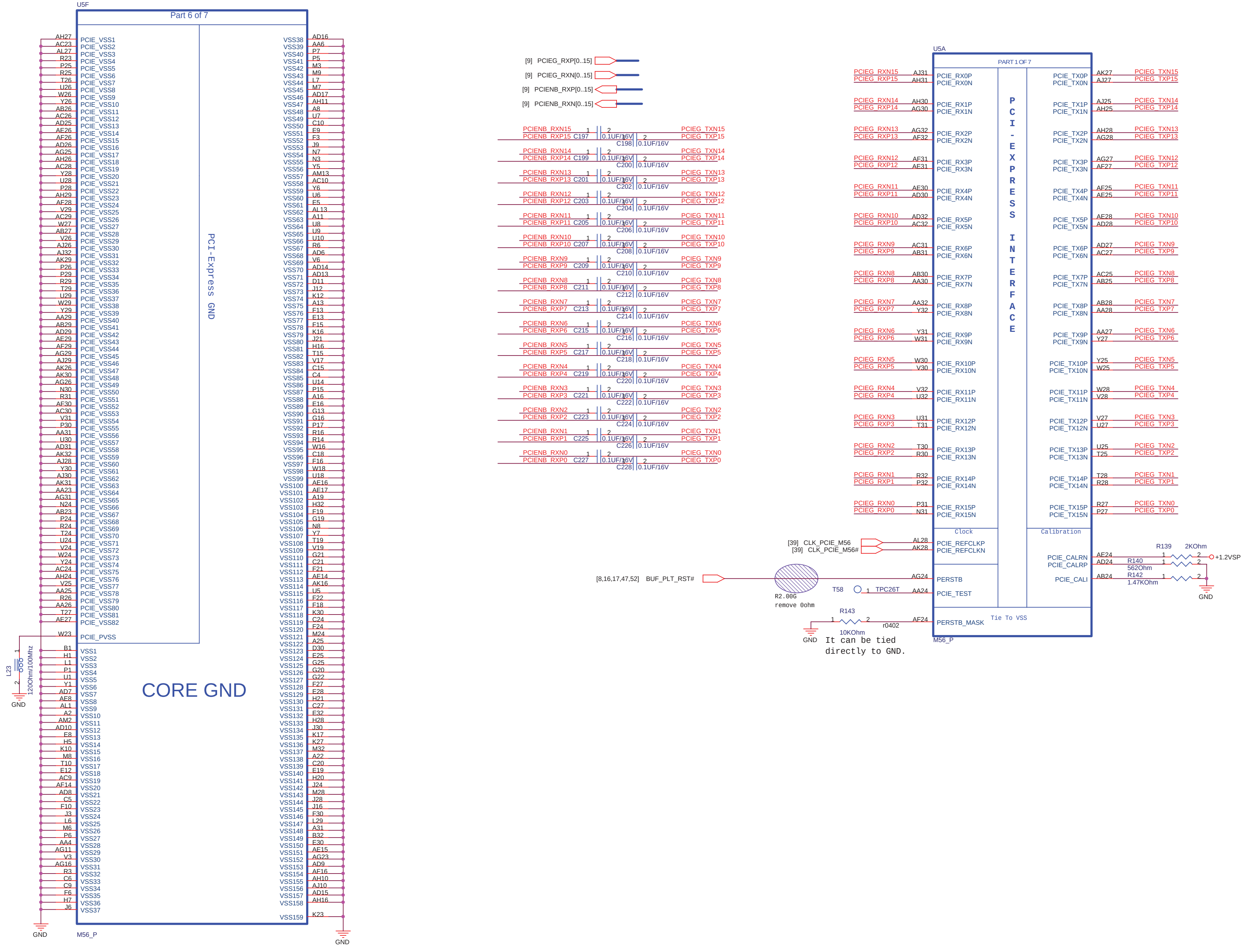
ASUSTeK COMPUTER INC. NB1

Title :	DDR2 TERMINATION		
Engineer:	Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev 1.0
Date: Monday, August 21, 2006	Sheet 22	of 91	



MID / Vendor /SIZE	3	2	1	0
Samsung 128M	0	0	0	0
Samsung 256M	0	0	0	1
Hynix 128M	0	0	1	0
Hynix 256M	0	0	1	1
Infineon 128M	0	1	0	0
Infineon 256M	0	1	0	1
	0	1	1	0
	0	1	1	1


U5C
Part 3 of 7
MEMORY INTERFACE A
MDA[63..0] [28]
GMAA[15:0] [28]
DQMA#[7..0] [28]
QSA[7..0] [28]
QSA#[7..0] [28]
read strobe
write strobe
Read-QS & Write-QS for GDDR3 memory.
TPC26T T130
TPC26T T53
TPC26T T56
ODTA0 [28]
ODTA1 [28]
CLKA0 [28]
CLKA0# [28]
CKEA0 [28]
RASA0# [28]
CASA0# [28]
WEA0# [28]
CSA0# [28]
CLKA1 [28]
CLKA1# [28]
CKEA1 [28]
RASA1# [28]
CASA1# [28]
WEA1# [28]
CSA1# [28]
MVREFD_0
MVREFS_0
DDR1: 0.5*VDDR1
DDR2: 0.5*VDDR1
GDDR3: 0.7*VDDR1
M56_P
MEMORY CHANNEL A
U5D
Part 4 of 7
MEMORY INTERFACE B
MDB[63..0] [29]
GMAB[15:0] [29]
DQMB#[7..0] [29]
QSB[7..0] [29]
QSB#[7..0] [29]
TPC26T T131
TPC26T T54
TPC26T T57
T55 TPC26T
ODTB0 [29]
ODTB1 [29]
CLKB0 [29]
CLKB0# [29]
CKEB0 [29]
RASB0# [29]
CASB0# [29]
WEB0# [29]
CSB0# [29]
CLKB1 [29]
CLKB1# [29]
CKEB1 [29]
RASB1# [29]
CASB1# [29]
WEB1# [29]
CSB1# [29]
MVREFD_1
MVREFS_1
DRAM_RST
TEST_MCLK
TEST_YCLK
MEMTEST
DDR1: 0.5*VDDR1
DDR2: 0.5*VDDR1
GDDR3: 0.7*VDDR1
For GDDR3, can be left NC for DDR1/2
R127 240Ohm
Change to 1%
MEMORY CHANNEL B
+VRAM
RN65A 75Ohm
RN65B 75Ohm
RN65C 75Ohm
RN65D 75Ohm
C193 0.1UF/16V
C194 0.1UF/16V
R1.01
2.37K/5.49K
GDDR3: 0.7 * VDDR1
DDR1/2: 0.5 * VDDR1
RN61A 4.7KOhm
RN61B 4.7KOhm
RN61C 4.7KOhm
RN61D 4.7KOhm
GDDR3: 0.7 * VDDR1
DDR1/2: 0.5 * VDDR1
RN66A 75Ohm
RN66B 75Ohm
RN66C 75Ohm
RN66D 75Ohm
C195 0.1UF/16V
C196 0.1UF/16V
GND
<Variant Name>
ASUS
Title : ATI_M56P_Memory(3)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 25 of 91



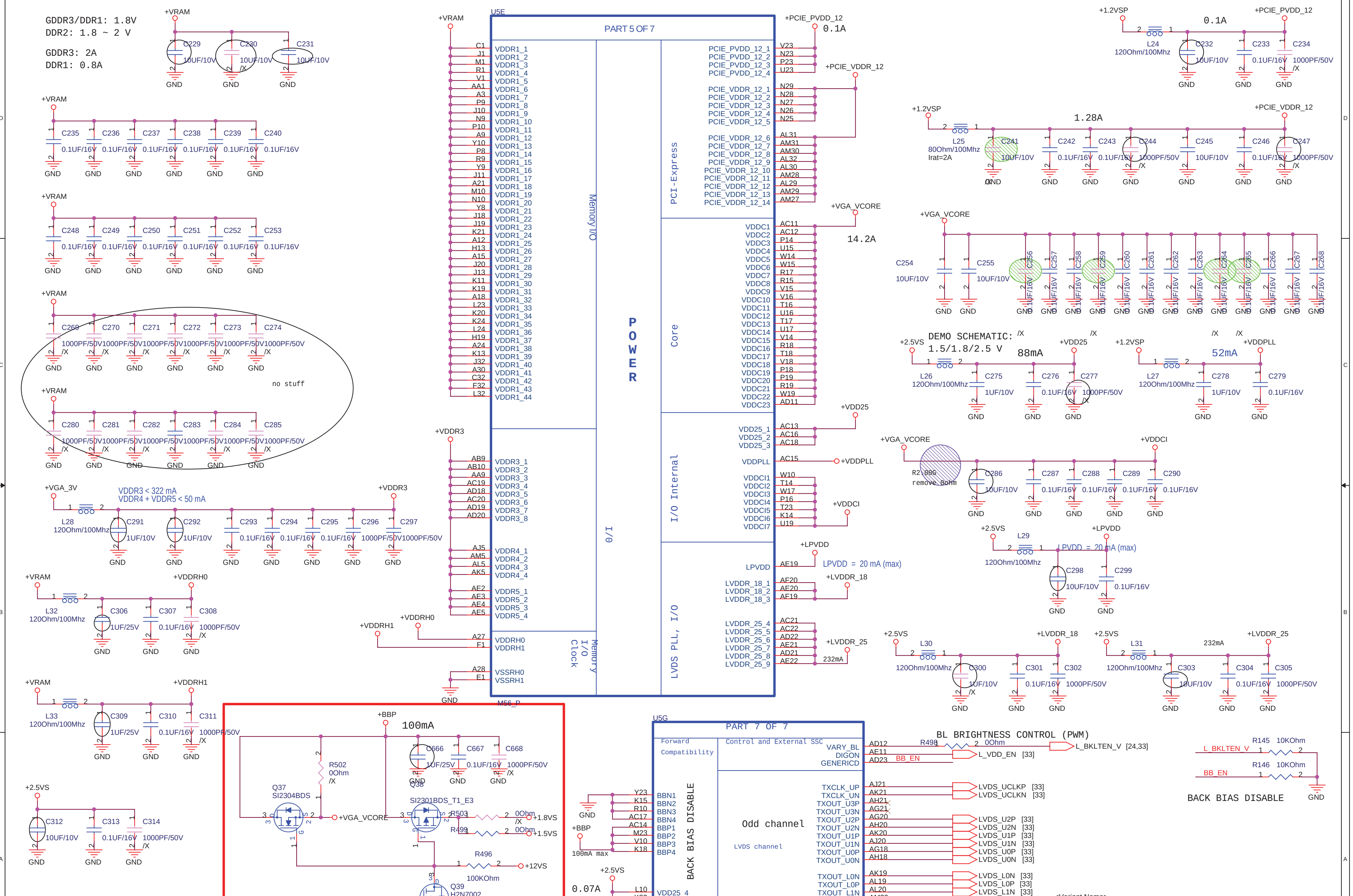
Title : ATI_M56P_PCI-E(1)

ASUSTek COMPUTER INC

Engineer: Alan Chu

Size	Project Name	Rev
C	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 26 of 91



<Variant Name>

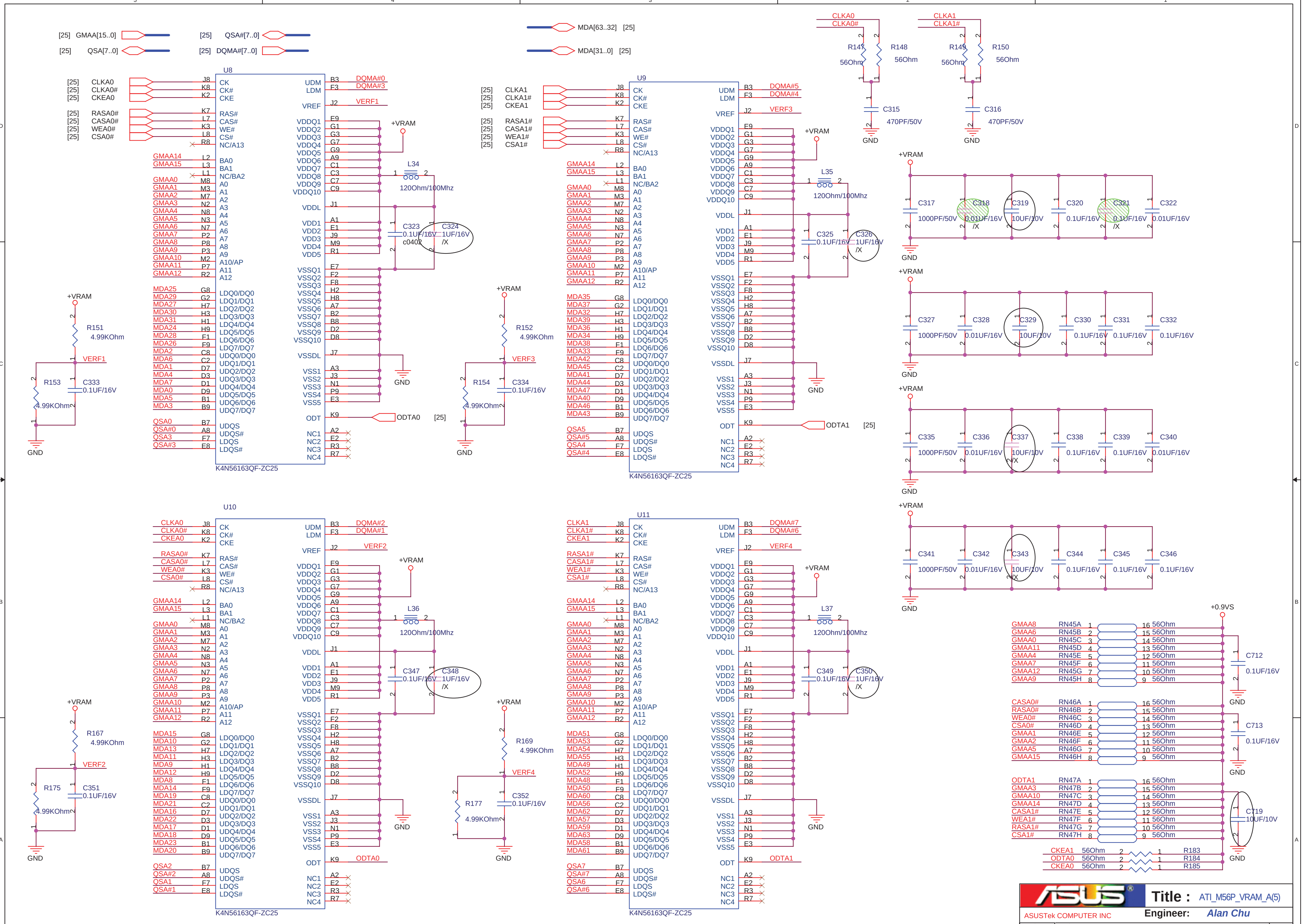
ASUSTek COMPUTER INC

Title : ATI_M56P_POWER(4)

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 27 of 91



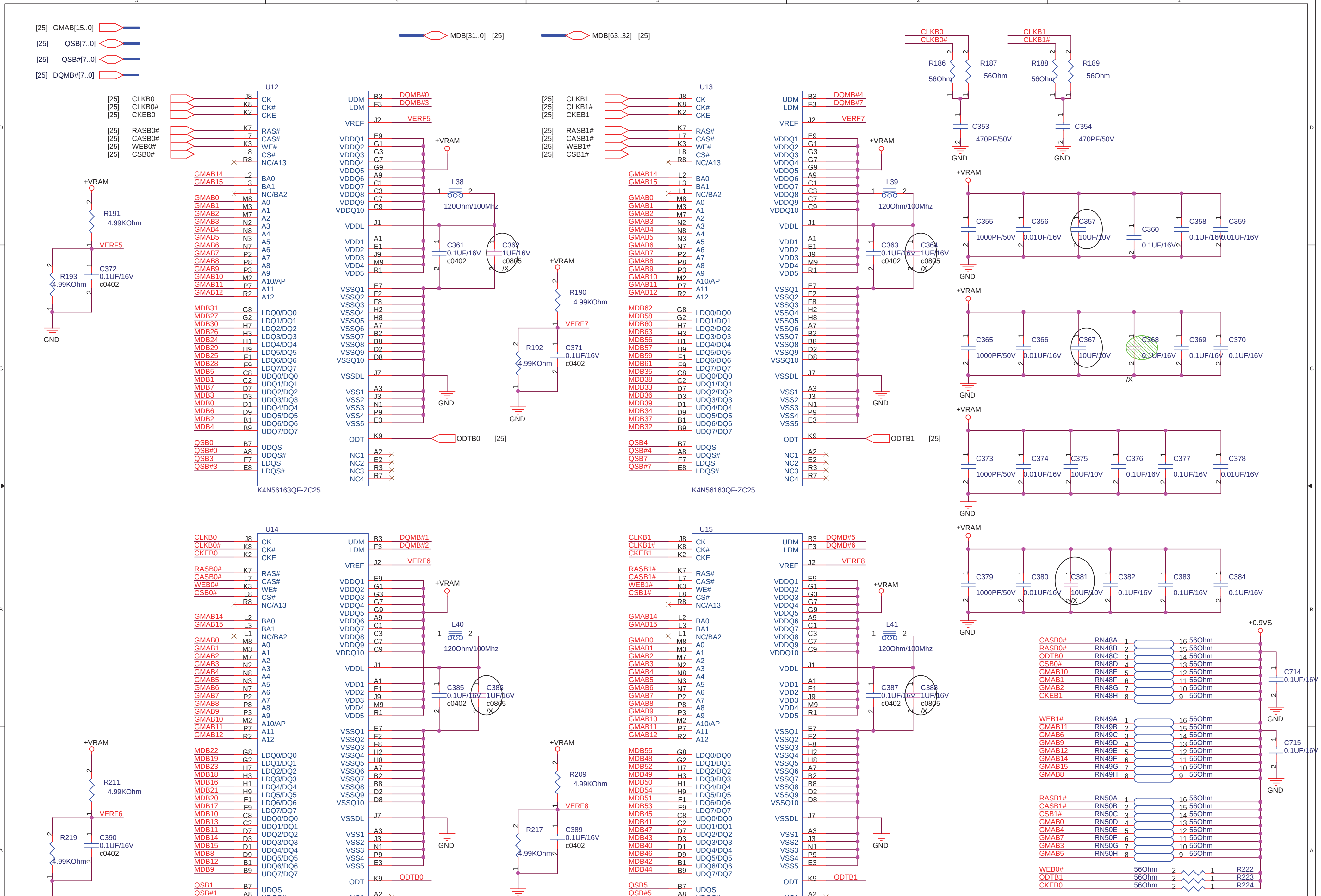
Title : ATI_M56P_VRAM_A(5)

ASUSTek COMPUTER INC

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 28 of 91



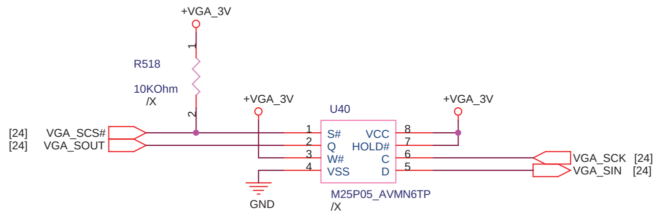
Title : ATI_M56P_VRAM_B(6)

ASUSTek COMPUTER INC

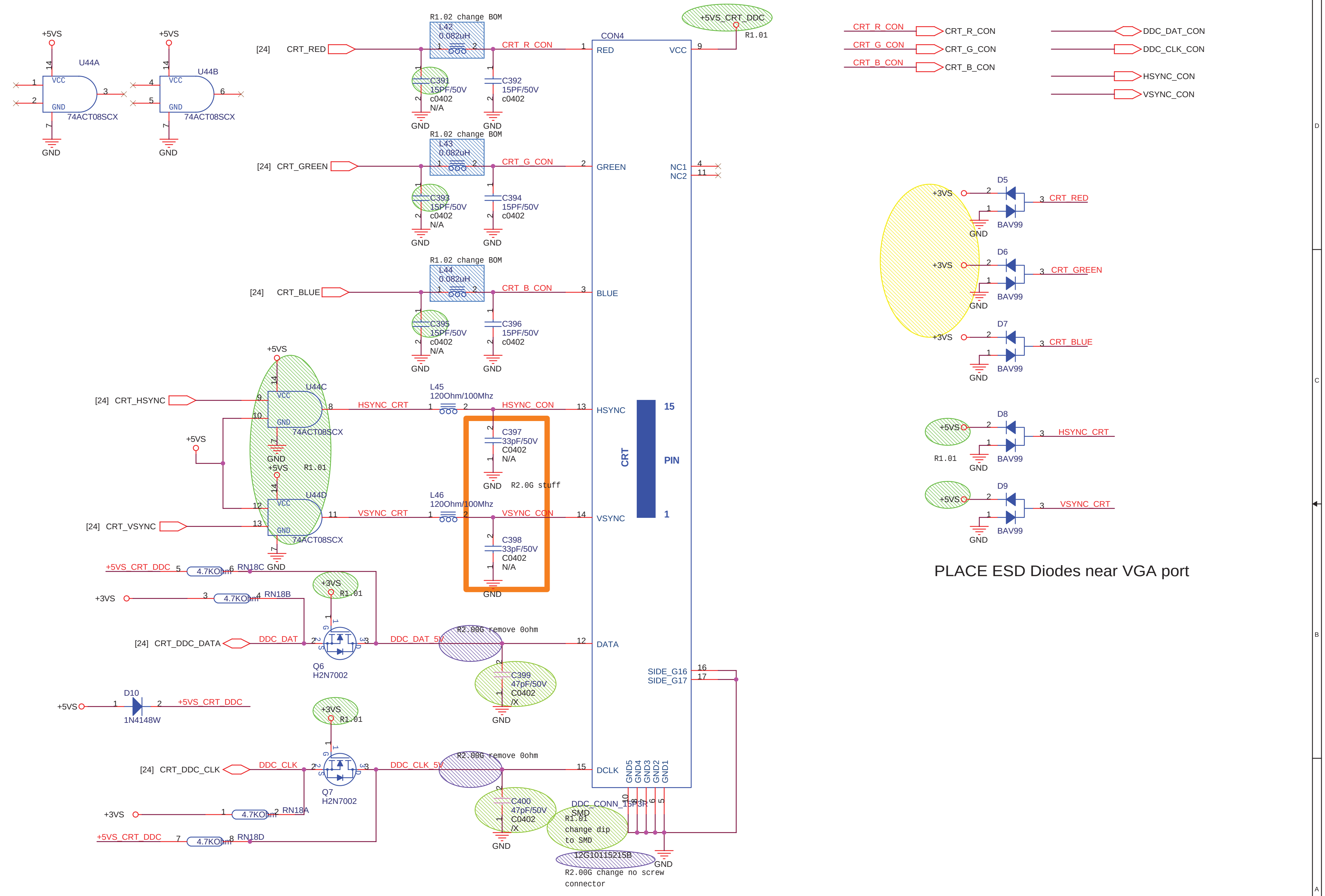
Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 29 of 91



ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 30	of 91	



ASUS

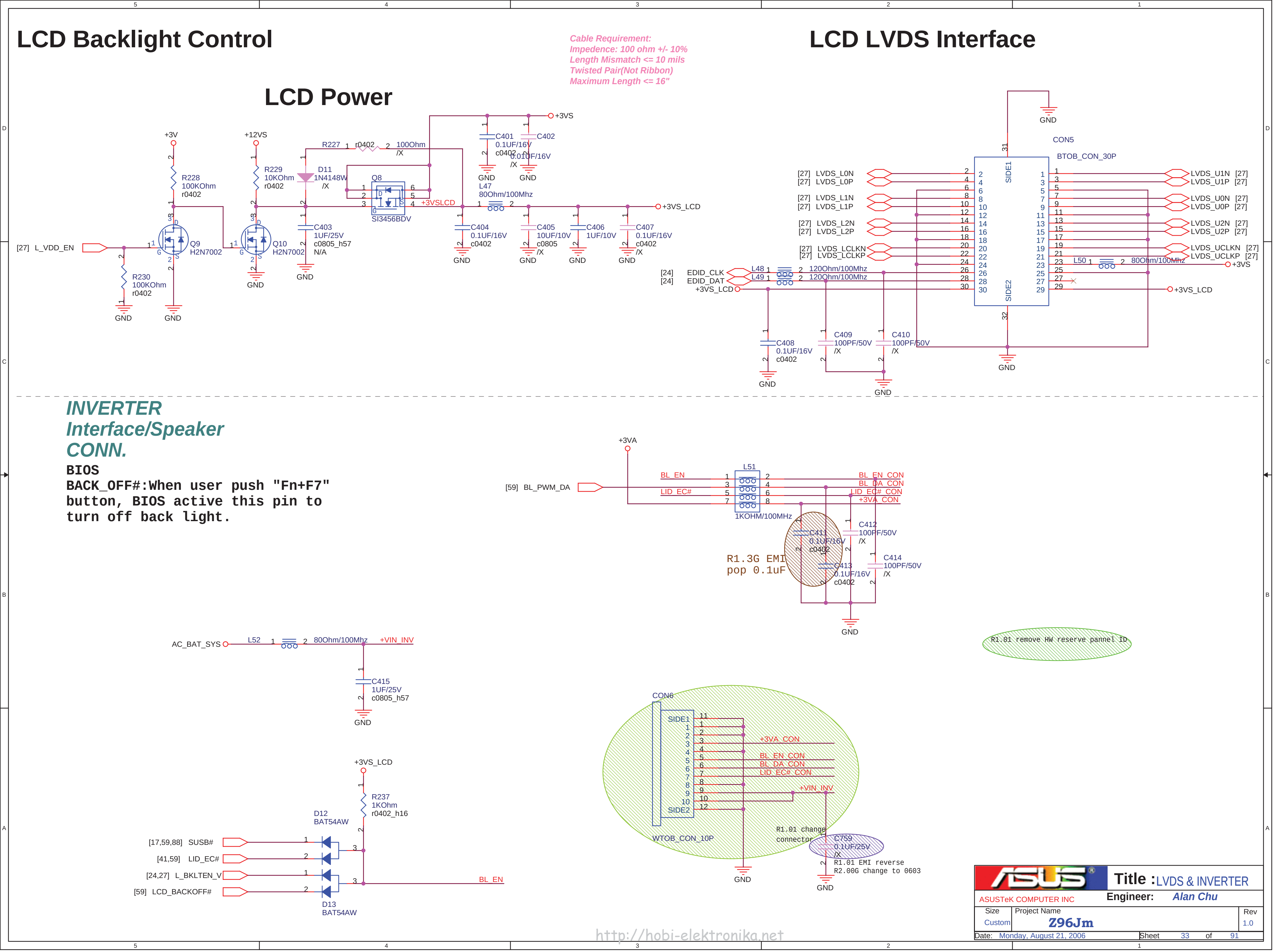
Title : CRT

ASUSTeK COMPUTER INC

Engineer: *Alan Chu*

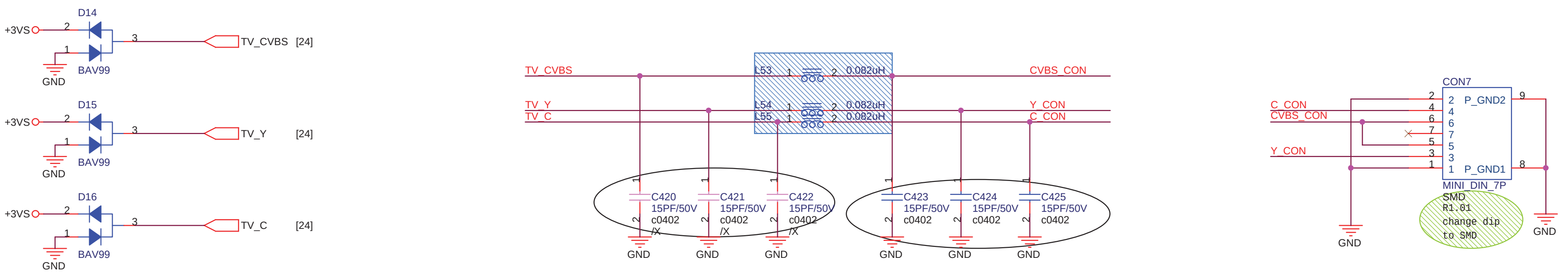
Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 32 of 91



LCD Backlight Control
LCD Power
LCD LVDS Interface
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"
+3V
+12VS
+3VS
R228 100KOhm r0402
R229 10KOhm r0402
R230 100KOhm r0402
R227 r0402 100Ohm /X
D11 1N4148W /X
Q8 SI3456BDV
Q9 H2N7002
Q10 H2N7002
[27] L_VDD_EN
C401 0.1UF/16V c0402
C402 0.01UF/16V /X
C403 1UF/25V c0805_h57 N/A
C404 0.1UF/16V c0402
C405 10UF/10V c0805 /X
C406 1UF/10V
C407 0.1UF/16V c0402 /X
L47 80Ohm/100Mhz
+3VSLCD
+3VS_LCD
GND
CON5 BTOB_CON_30P
SIDE1
SIDE2
[27] LVDS_L0N
[27] LVDS_L0P
[27] LVDS_L1N
[27] LVDS_L1P
[27] LVDS_L2N
[27] LVDS_L2P
[27] LVDS_LCLKN
[27] LVDS_LCLKP
LVDS_U1N [27]
LVDS_U1P [27]
LVDS_U0N [27]
LVDS_U0P [27]
LVDS_U2N [27]
LVDS_U2P [27]
LVDS_UCLKN [27]
LVDS_UCLKP [27]
[24] EDID_CLK
[24] EDID_DAT
L48 120Ohm/100Mhz
L49 120Ohm/100Mhz
L50 80Ohm/100Mhz
C408 0.1UF/16V c0402
C409 100PF/50V /X
C410 100PF/50V /X
INVERTER Interface/Speaker CONN.
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.
+3VA
[59] BL_PWM_DA
BL_EN
LID_EC#
L51 1KOHM/100MHZ
BL_EN_CON
BL_DA_CON
LID_EC#_CON
+3VA_CON
C411 0.1UF/16V c0402
C412 100PF/50V /X
C413 0.1UF/16V c0402
C414 100PF/50V /X
R1.3G EMI pop 0.1uF
R1.01 remove HW reserve pannel ID
AC_BAT_SYS
L52 80Ohm/100Mhz
+VIN_INV
C415 1UF/25V c0805_h57
CON6 WTOB_CON_10P
R1.01 change connector
C759 0.1UF/25V /X
R1.01 EMI reverse
R2.00G change to 0603
R237 1KOhm r0402_h16
D12 BAT54AW
D13 BAT54AW
[17,59,88] SUSB#
[41,59] LID_EC#
[24,27] L_BKLTEN_V
[59] LCD_BACKOFF#
Title : LVDS & INVERTER
ASUSTeK COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 33 of 91

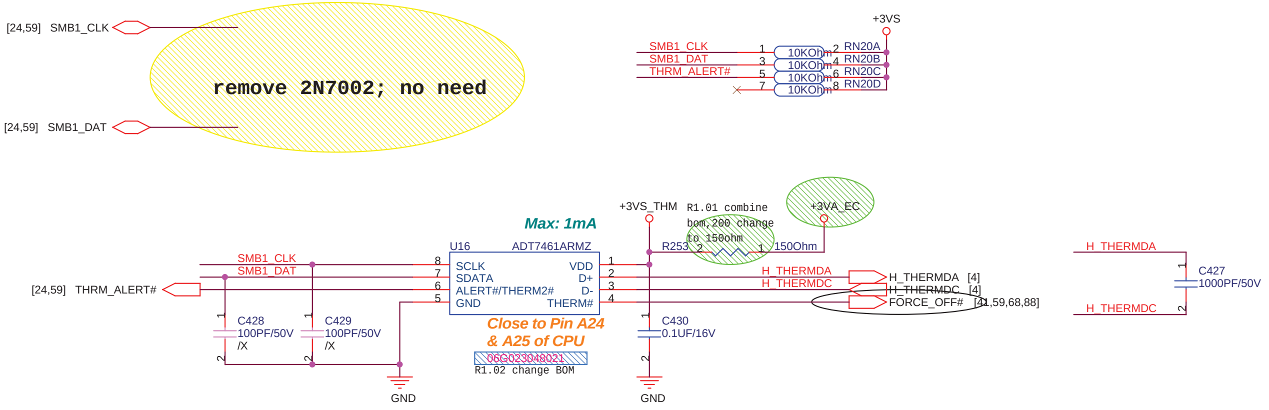
TV OUT



PLACE ESD
Diodes near
TV port

ASUSTeK COMPUTER INC	Title : TV OUT & DVI CON.	Engineer: Alan Chu
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 35 of 91	

Thermal Sensor

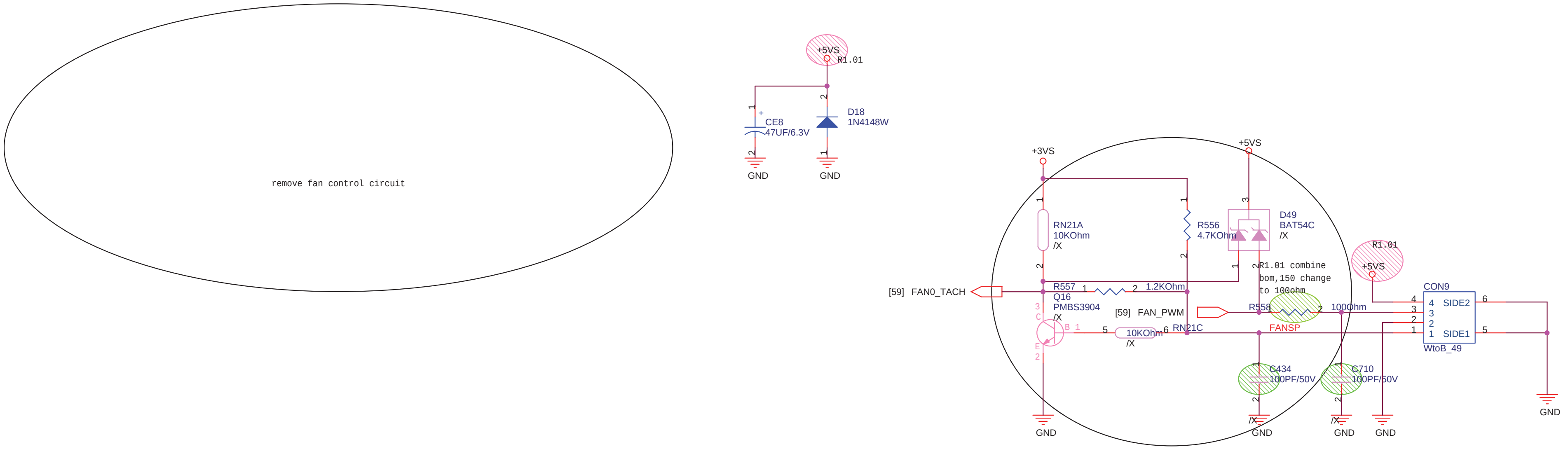


Route H_THERMDA and H_THERMDC on the same layer

------------------OTHER SIGNALS
15 mils
===============GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
--------------------OTHER SIGNALS

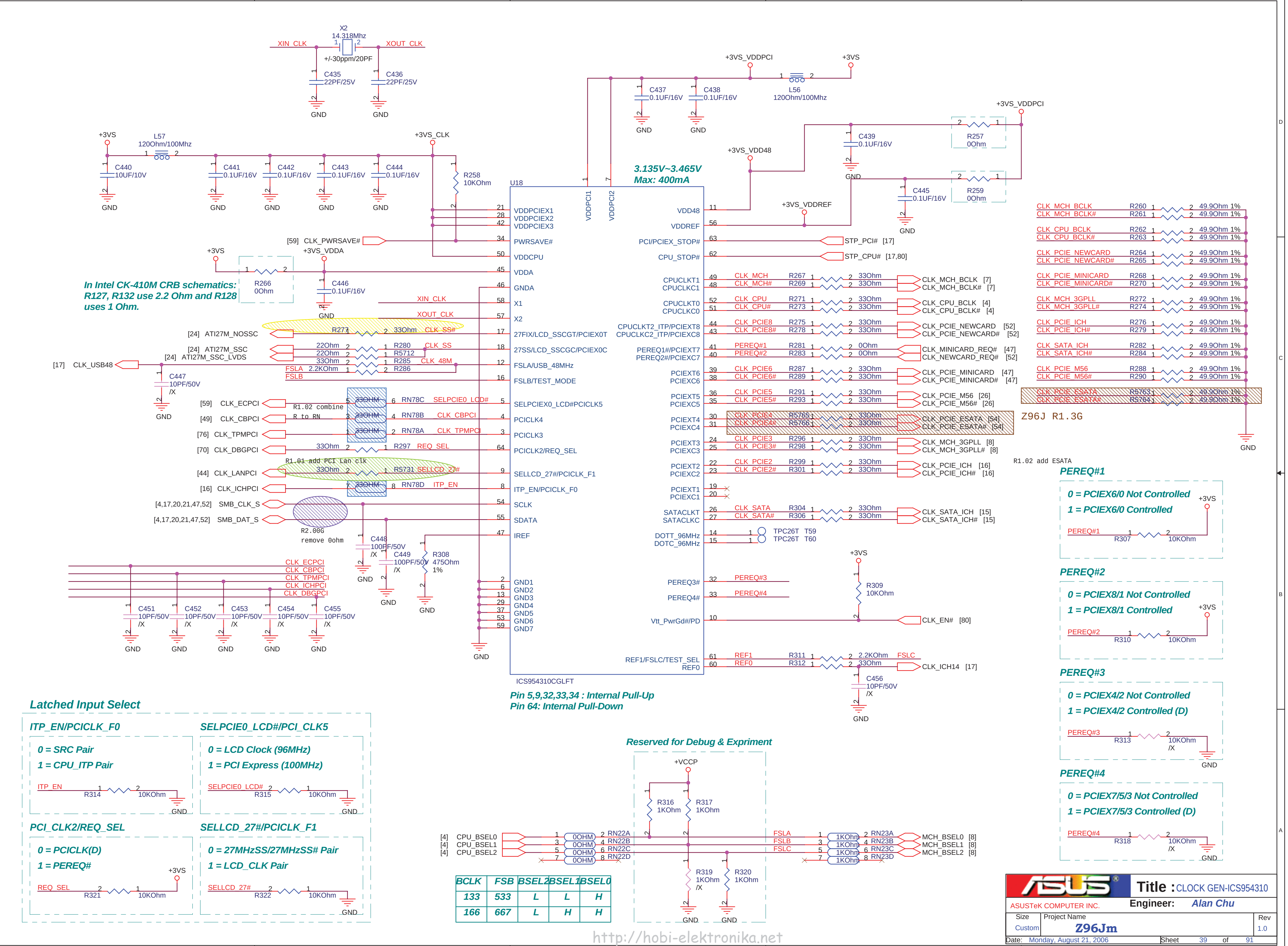
Avoid FSB,Power

DC FAN Control



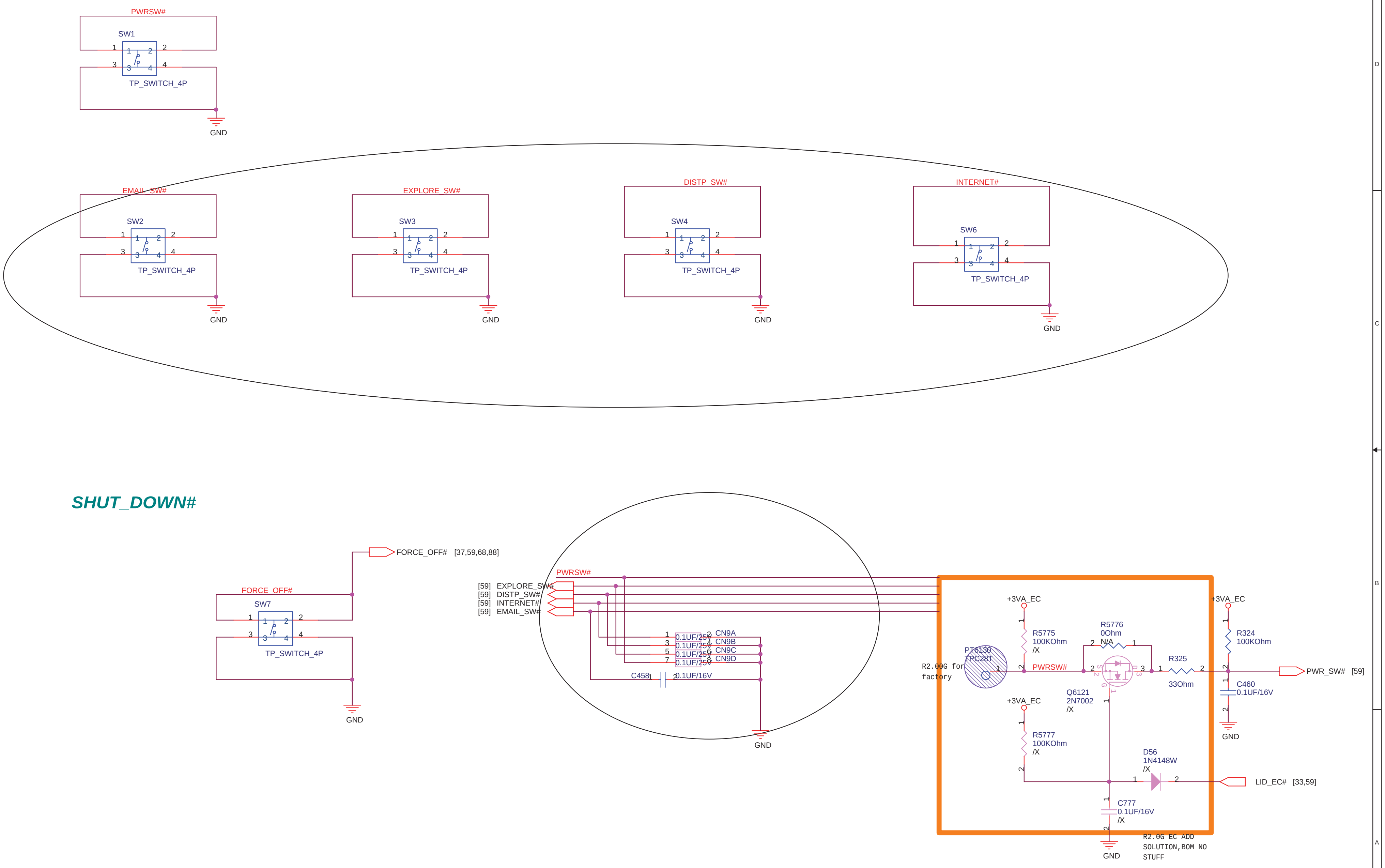
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006		Sheet 37 of 91	



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

ASUSTeK COMPUTER INC.
Title : CLOCK GEN-ICS954310
Engineer: Alan Chu
Size: Custom
Project Name: Z96Jm
Rev: 1.0
Date: Monday, August 21, 2006
Sheet 39 of 91



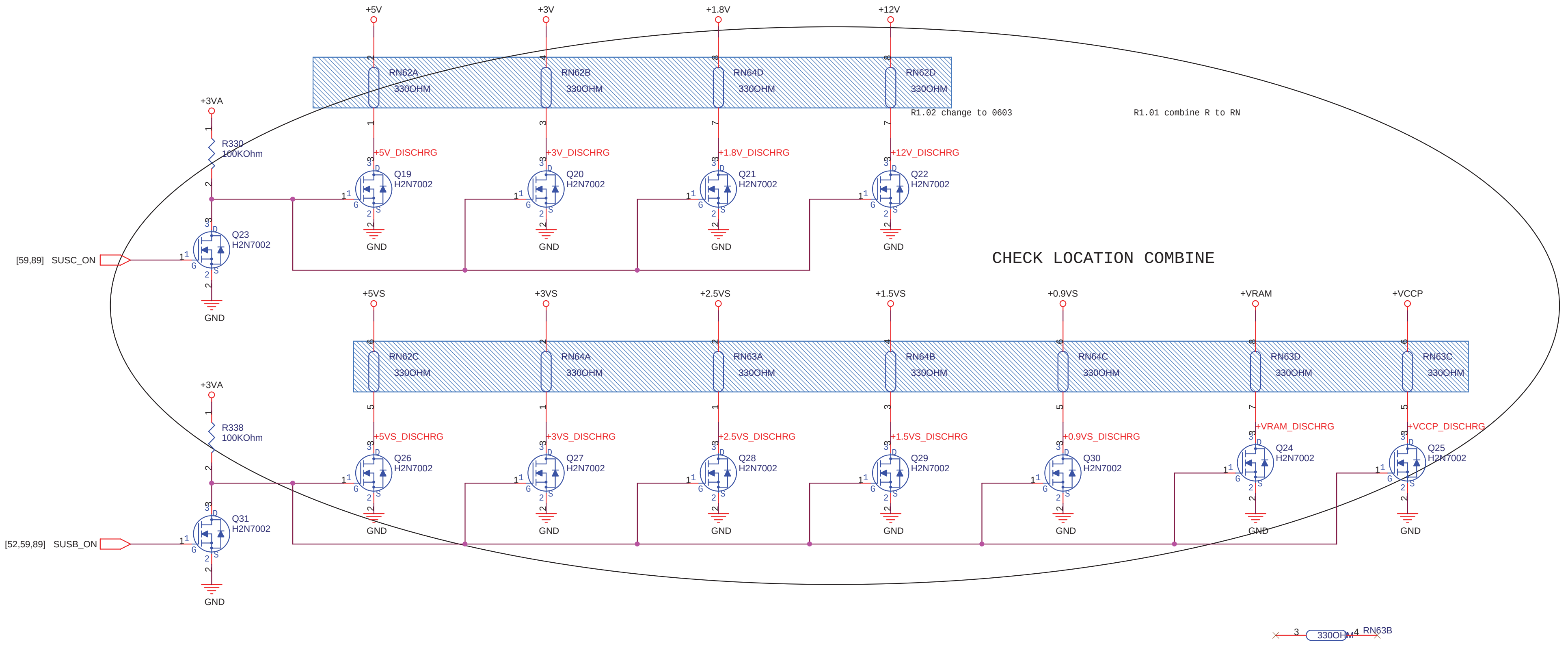
ASUSTeK COMPUTER INC

Title : Power on & Res Freq

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 41 of 91



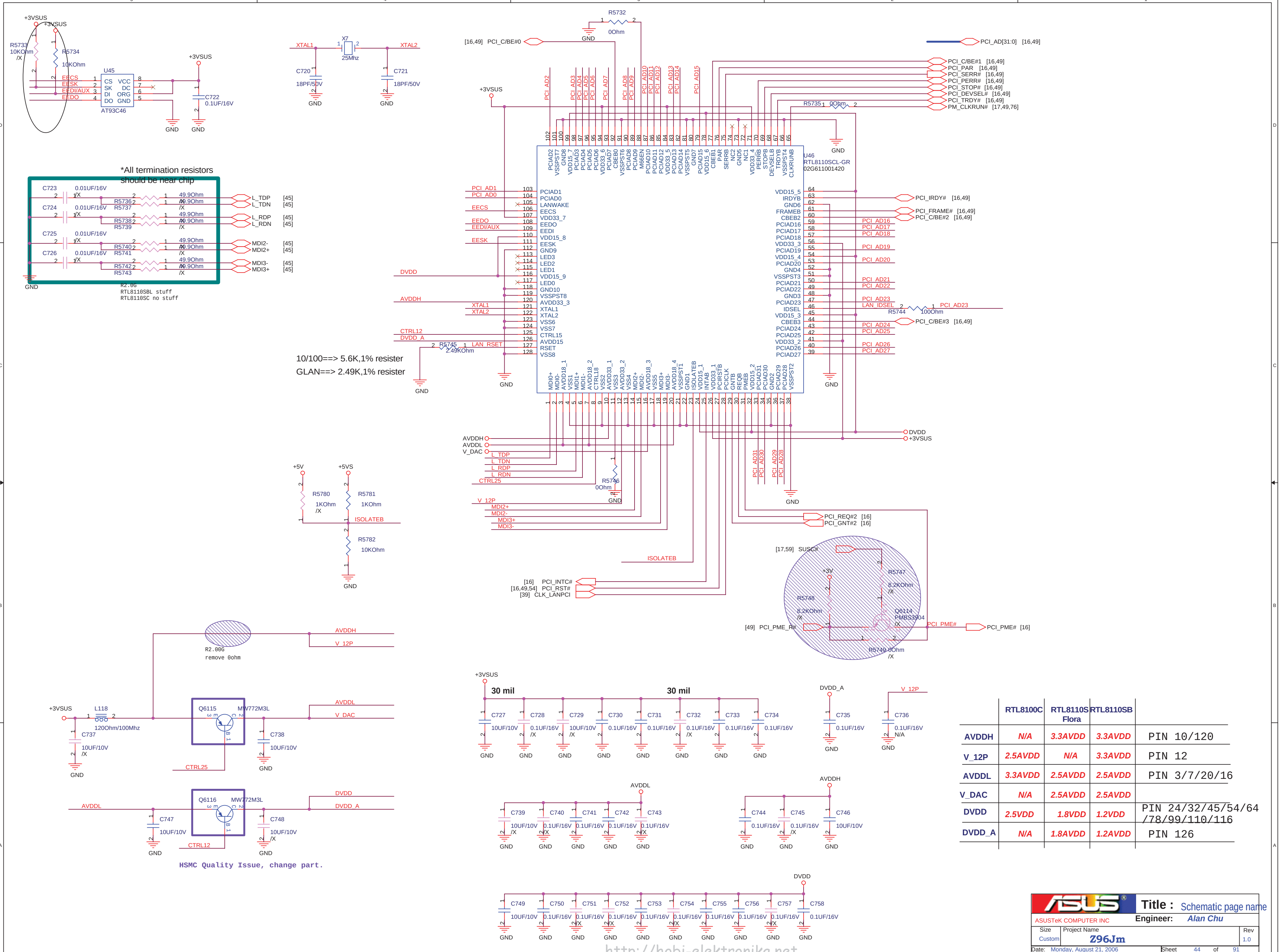
ASUSTeK COMPUTER INC. NB1

Title : DISCHARGE & EMI CAP

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 42 of 91



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

ASUSTeK COMPUTER INC

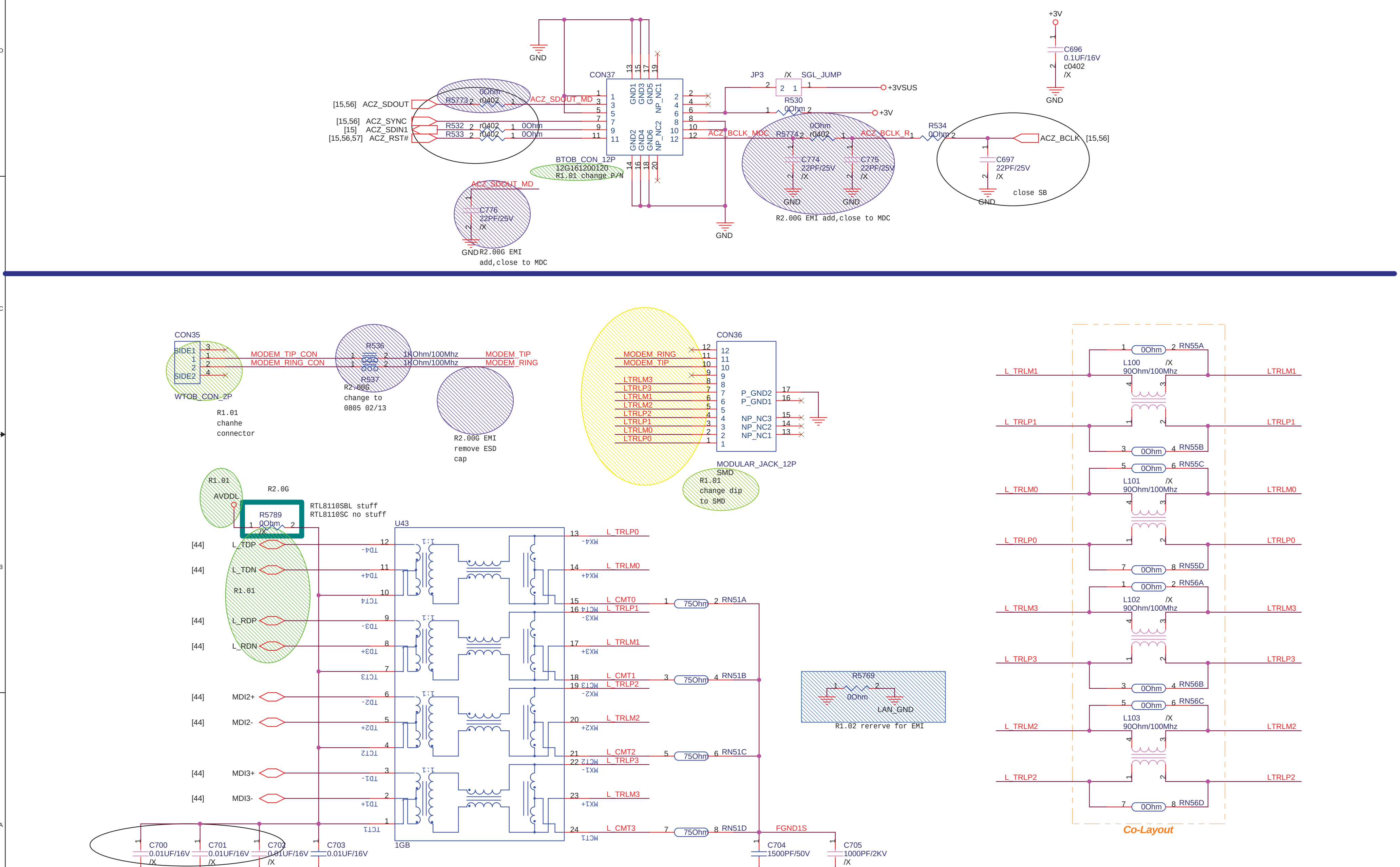
Title : Schematic page name

Engineer: Alan Chu

Size: Custom | Project Name: Z96Jm | Rev: 1.0

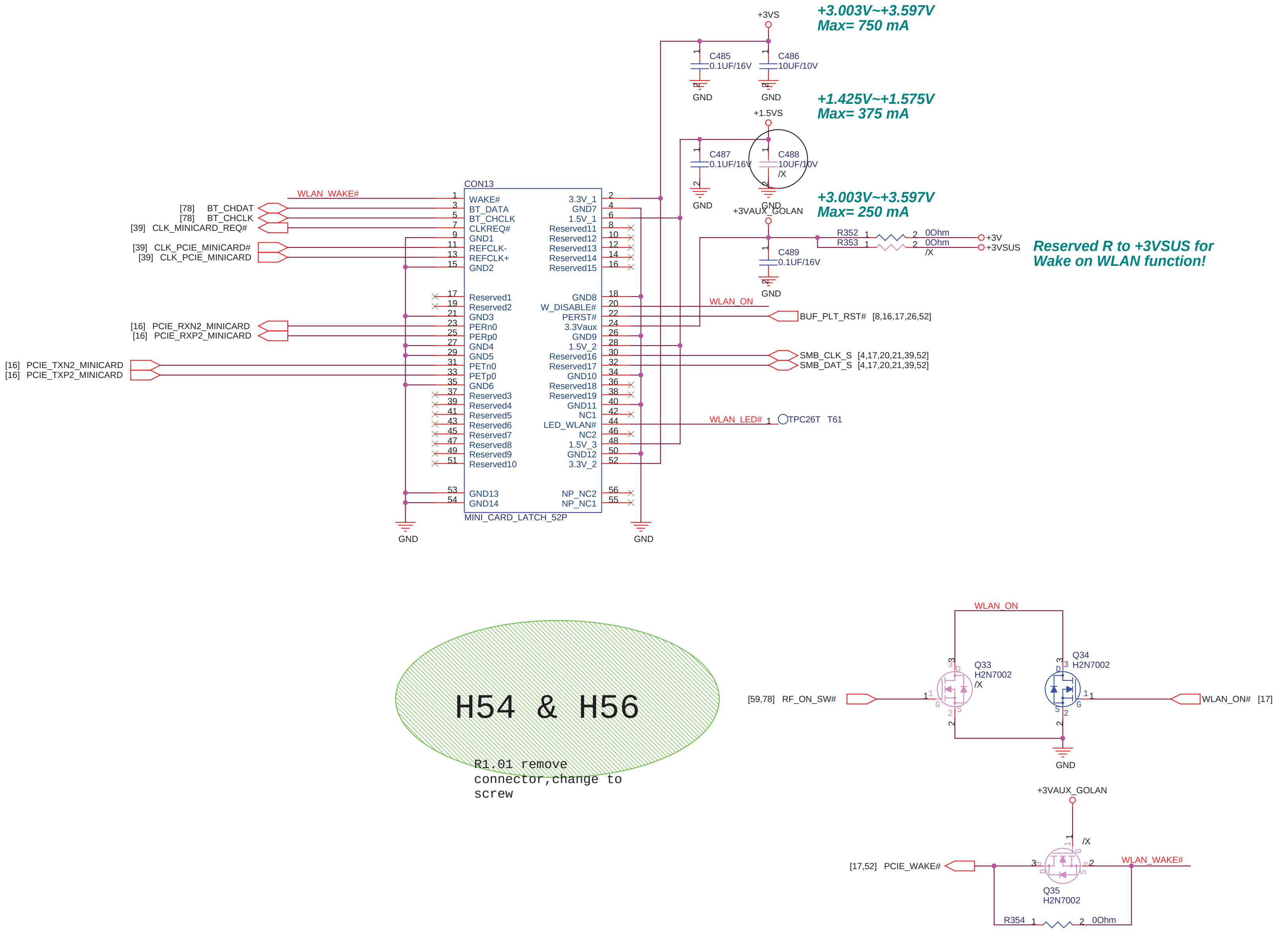
Date: Monday, August 21, 2006 | Sheet 44 of 91

MDC CONN.



ASUSTeK COMPUTER INC.

Title : RJ45&RJ11		
Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 45 of 91	



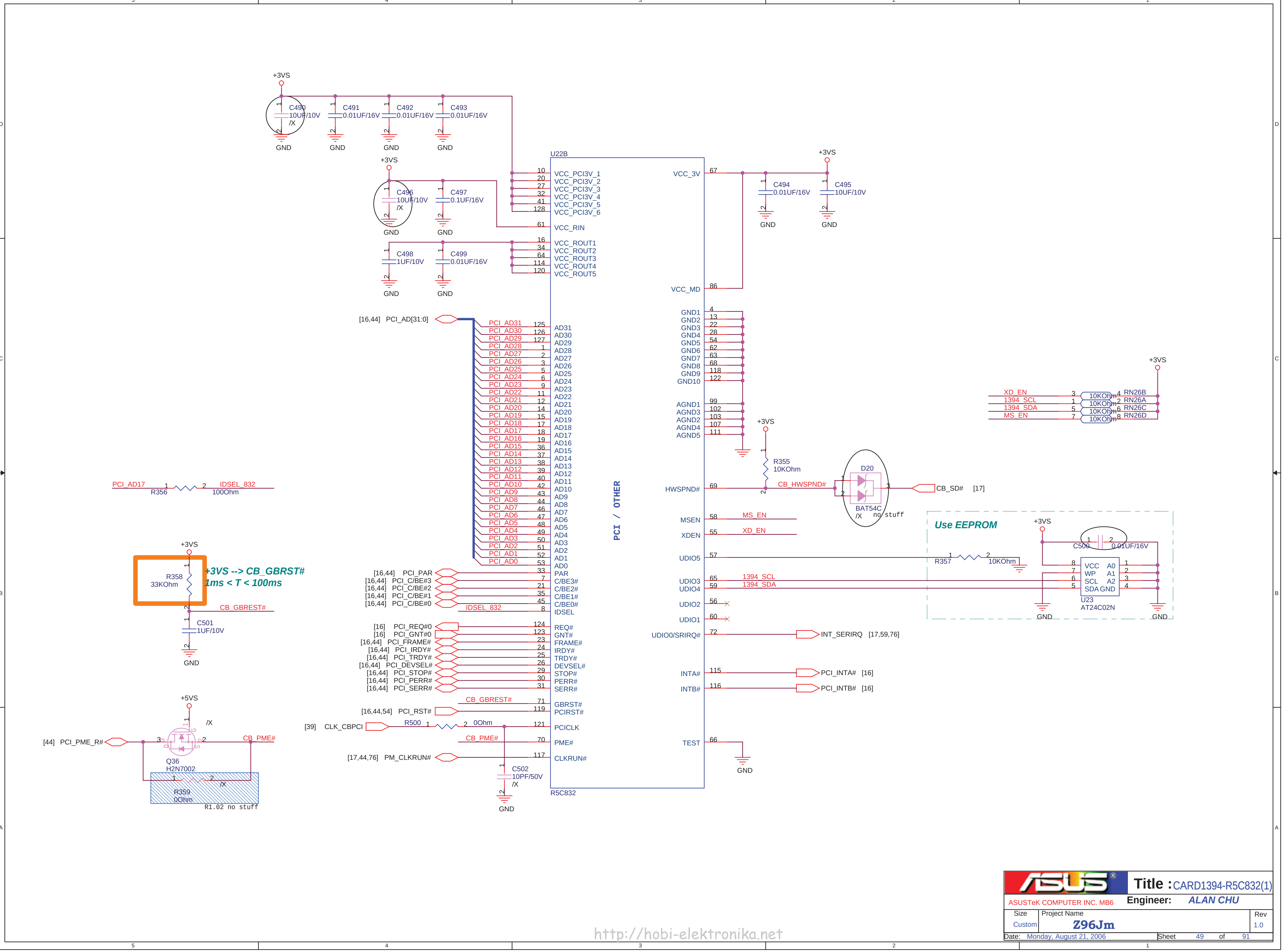
Title : MINICARD

ASUSTeK COMPUTER INC.

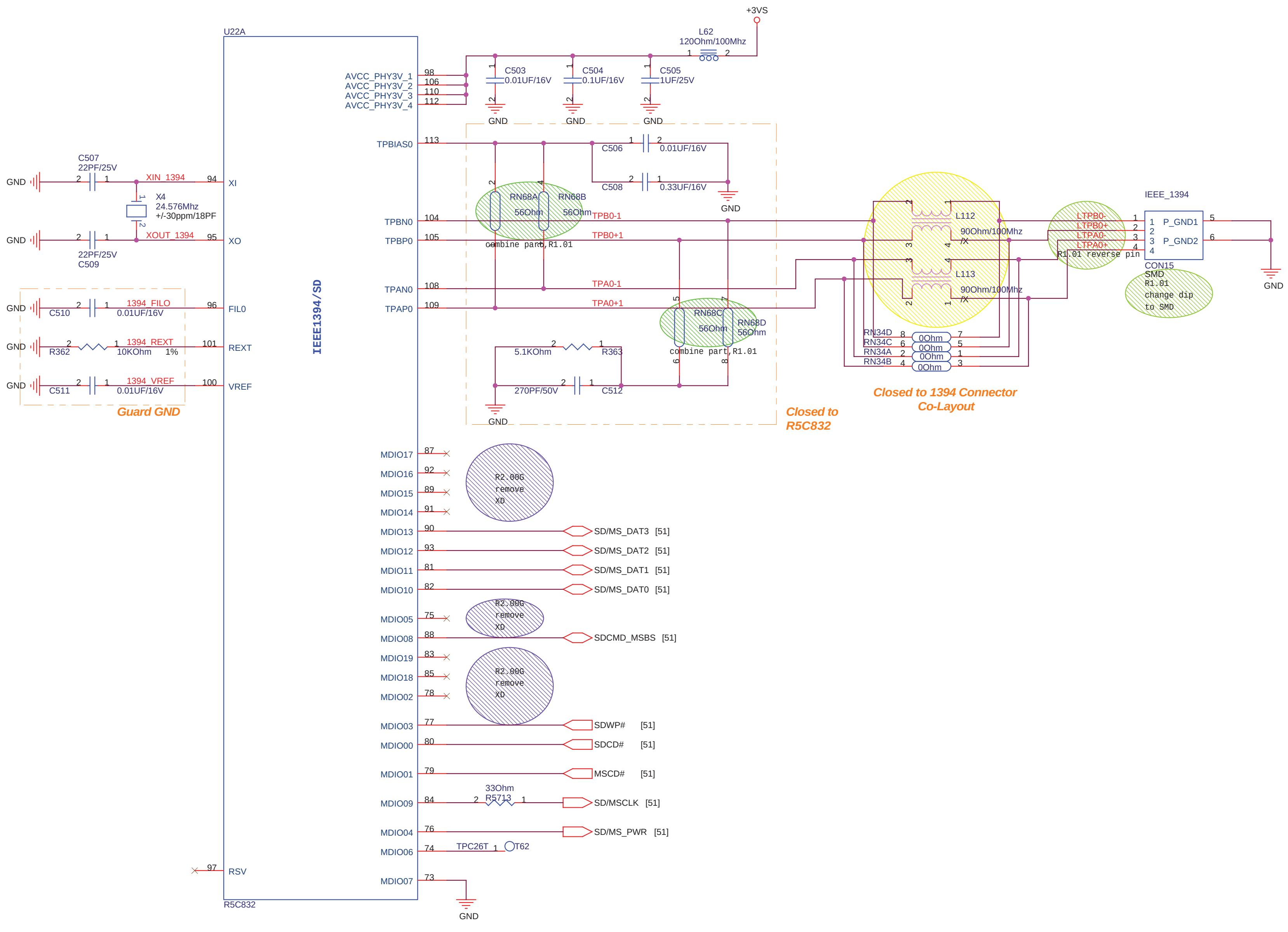
Engineer: *Alan Chu*

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 47 of 91



+3VS
C490 10UF/10V /X
C491 0.01UF/16V
C492 0.01UF/16V
C493 0.01UF/16V
GND
C496 10UF/10V /X
C497 0.1UF/16V
C498 1UF/10V
C499 0.01UF/16V
U22B
VCC_PCI3V_1
VCC_PCI3V_2
VCC_PCI3V_3
VCC_PCI3V_4
VCC_PCI3V_5
VCC_PCI3V_6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C494 0.01UF/16V
C495 10UF/10V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND1 AGND2 AGND3 AGND4 AGND5
[16,44] PCI_AD[31:0]
PCI_AD31 … PCI_AD0
AD31 … AD0
PAR
C/BE3# C/BE2# C/BE1# C/BE0#
IDSEL
[16,44] PCI_PAR
[16,44] PCI_C/BE#3
[16,44] PCI_C/BE#2
[16,44] PCI_C/BE#1
[16,44] PCI_C/BE#0
IDSEL_832
[16] PCI_REQ#0
[16] PCI_GNT#0
[16,44] PCI_FRAME#
[16,44] PCI_IRDY#
[16,44] PCI_TRDY#
[16,44] PCI_DEVSEL#
[16,44] PCI_STOP#
[16,44] PCI_PERR#
[16,44] PCI_SERR#
REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
CB_GBREST#
GBRST#
[16,44,54] PCI_RST#
PCIRST#
[39] CLK_CBPCI
R500 0Ohm
PCICLK
CB_PME#
PME#
[17,44,76] PM_CLKRUN#
CLKRUN#
C502 10PF/50V /X
R5C832
PCI / OTHER
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SERIRQ#
INTA#
INTB#
TEST
R355 10KOhm
CB_HWSPND#
D20
BAT54C
/X no stuff
CB_SD# [17]
MS_EN
XD_EN
1394_SCL
1394_SDA
INT_SERIRQ [17,59,76]
PCI_INTA# [16]
PCI_INTB# [16]
RN26B RN26A RN26C RN26D 10KOhm
Use EEPROM
R357 10KOhm
C500 0.01UF/16V
VCC WP SCL SDA A0 A1 A2 GND
U23
AT24C02N
PCI_AD17
R356 100Ohm
IDSEL_832
R358 33KOhm
+3VS --> CB_GBRST#
1ms < T < 100ms
C501 1UF/10V
+5VS
/X
[44] PCI_PME_R#
Q36
H2N7002
R359 0Ohm
R1.02 no stuff
ASUS
ASUSTeK COMPUTER INC. MB6
Title : CARD1394-R5C832(1)
Engineer: ALAN CHU
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 49 of 91



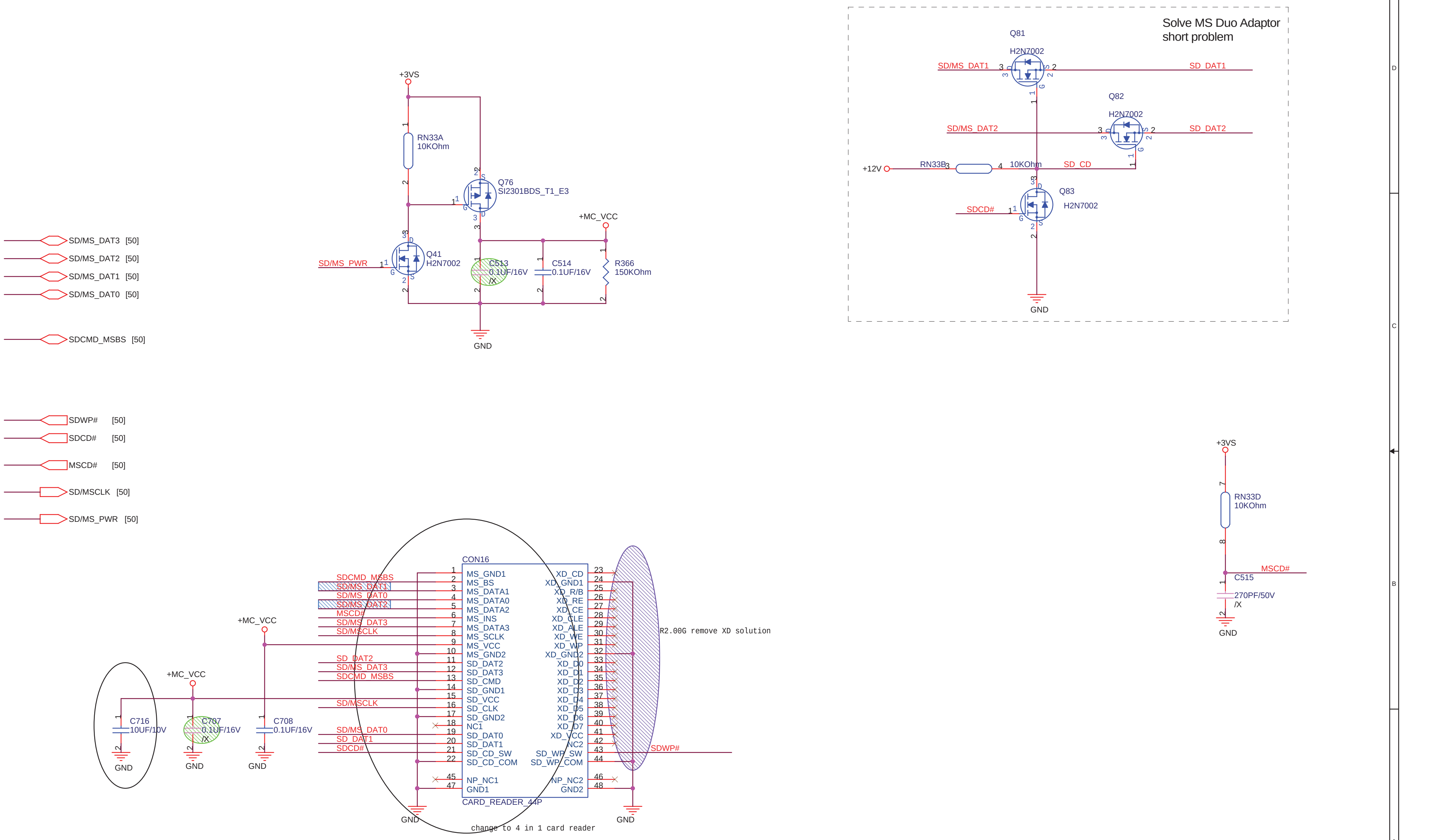
Title : CARD1394-R5C832(2)

ASUSTeK COMPUTER INC. MB6

Engineer: ALAN CHU

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 50 of 91



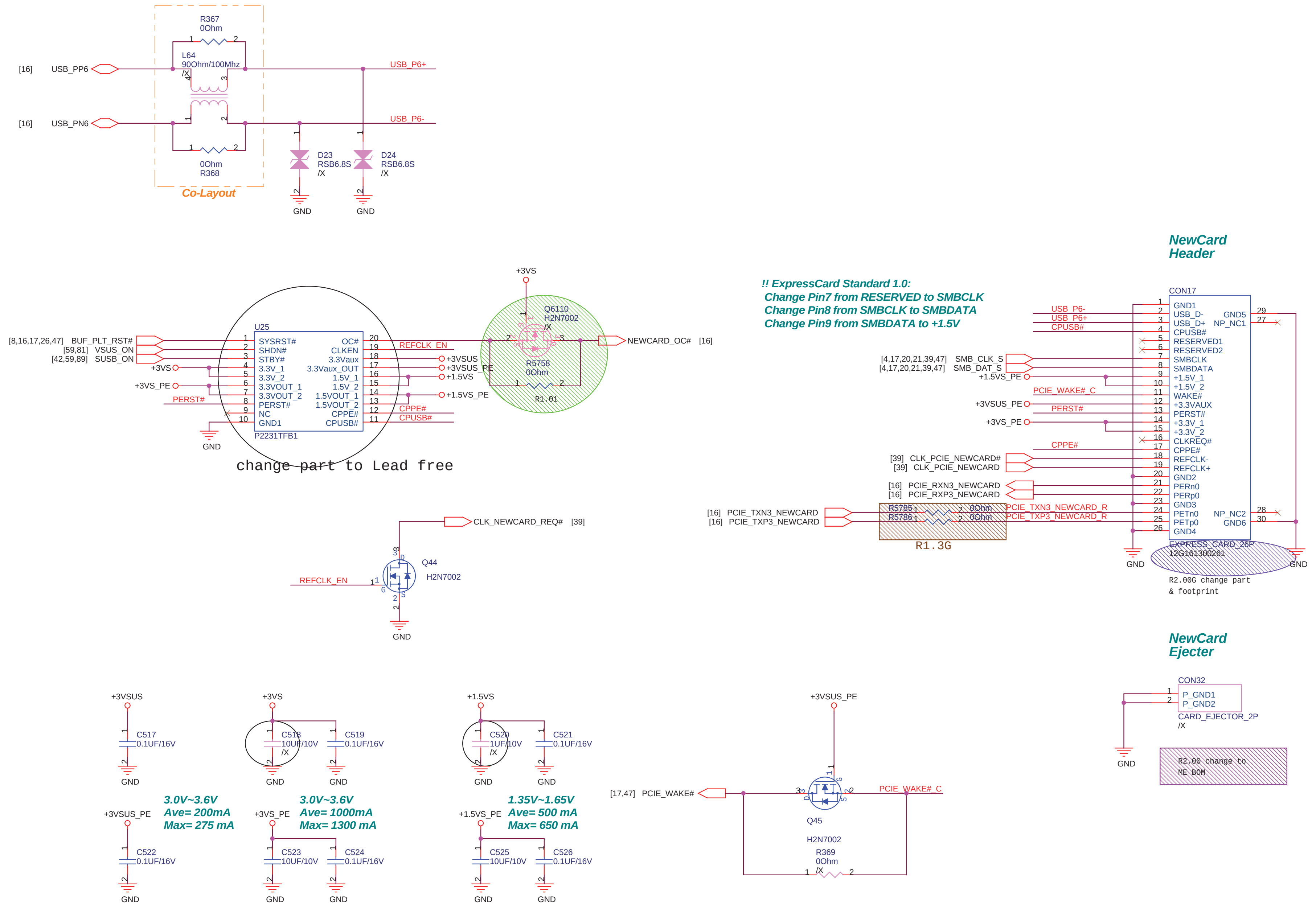
Title : 4 in 1 CARD READER

ASUSTeK COMPUTER INC

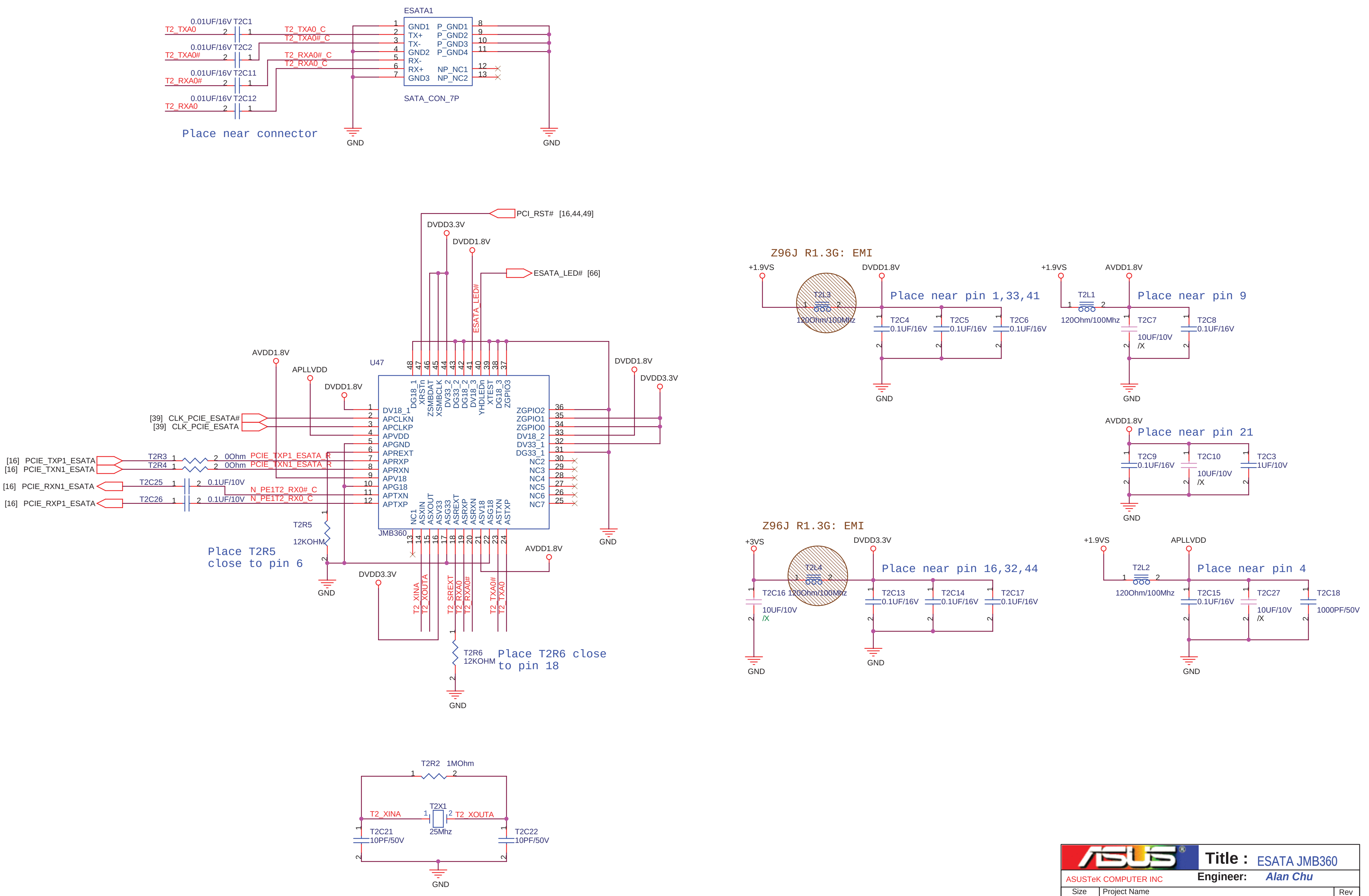
Engineer: ALAN CHU

Size	Project Name	Rev
A3	Z96Jm	1.0

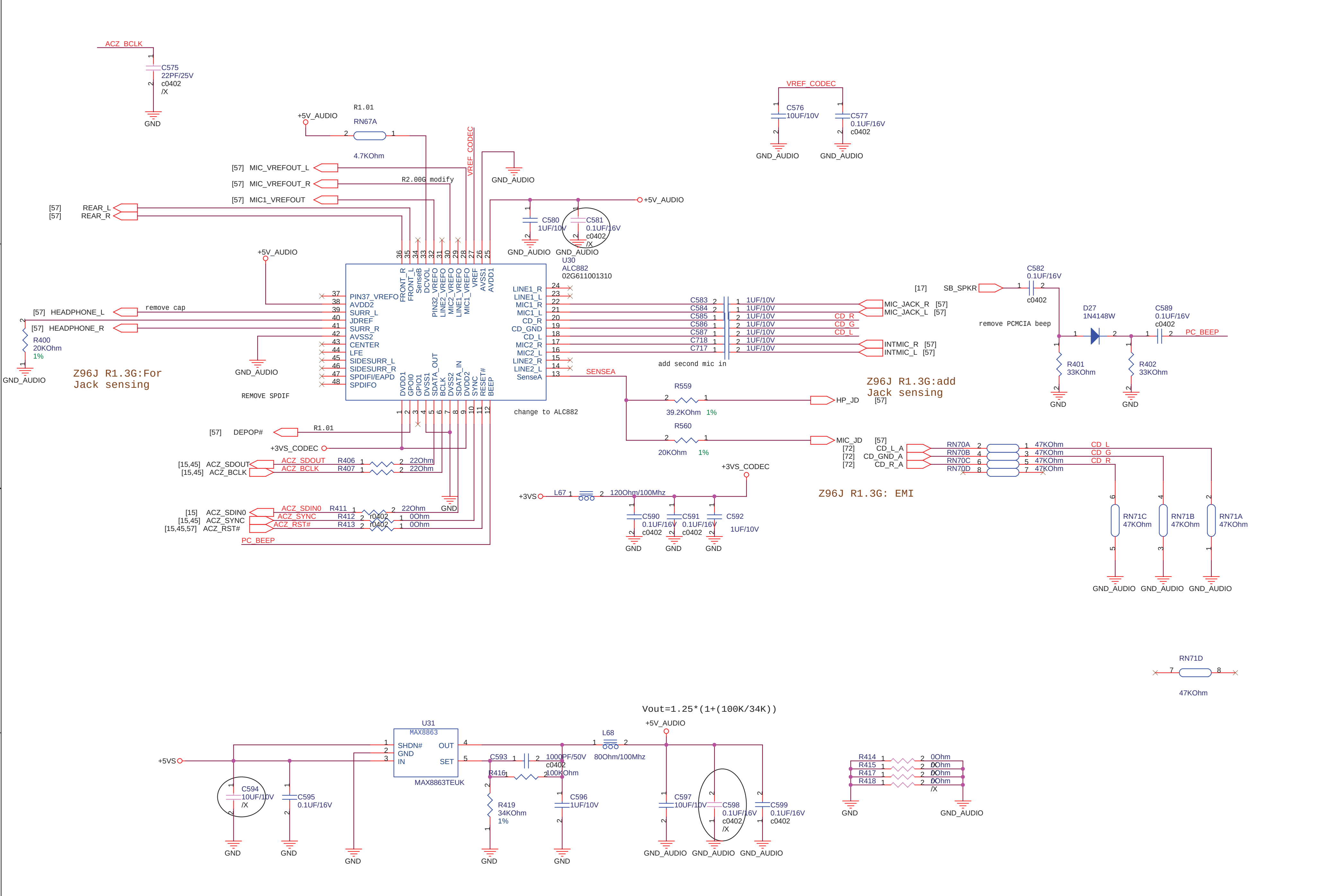
Date: Monday, August 21, 2006 Sheet 51 of 91



ASUS	Title : NEWCARD		
ASUSTeK COMPUTER INC. NB1	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 52 of 91		



ASUSTeK COMPUTER INC	Title : ESATA JMB360		
	Engineer: Alan Chu		
Size A3	Project Name Z96Jm		Rev 1.0
Date: Monday, August 21, 2006		Sheet 54	of 91



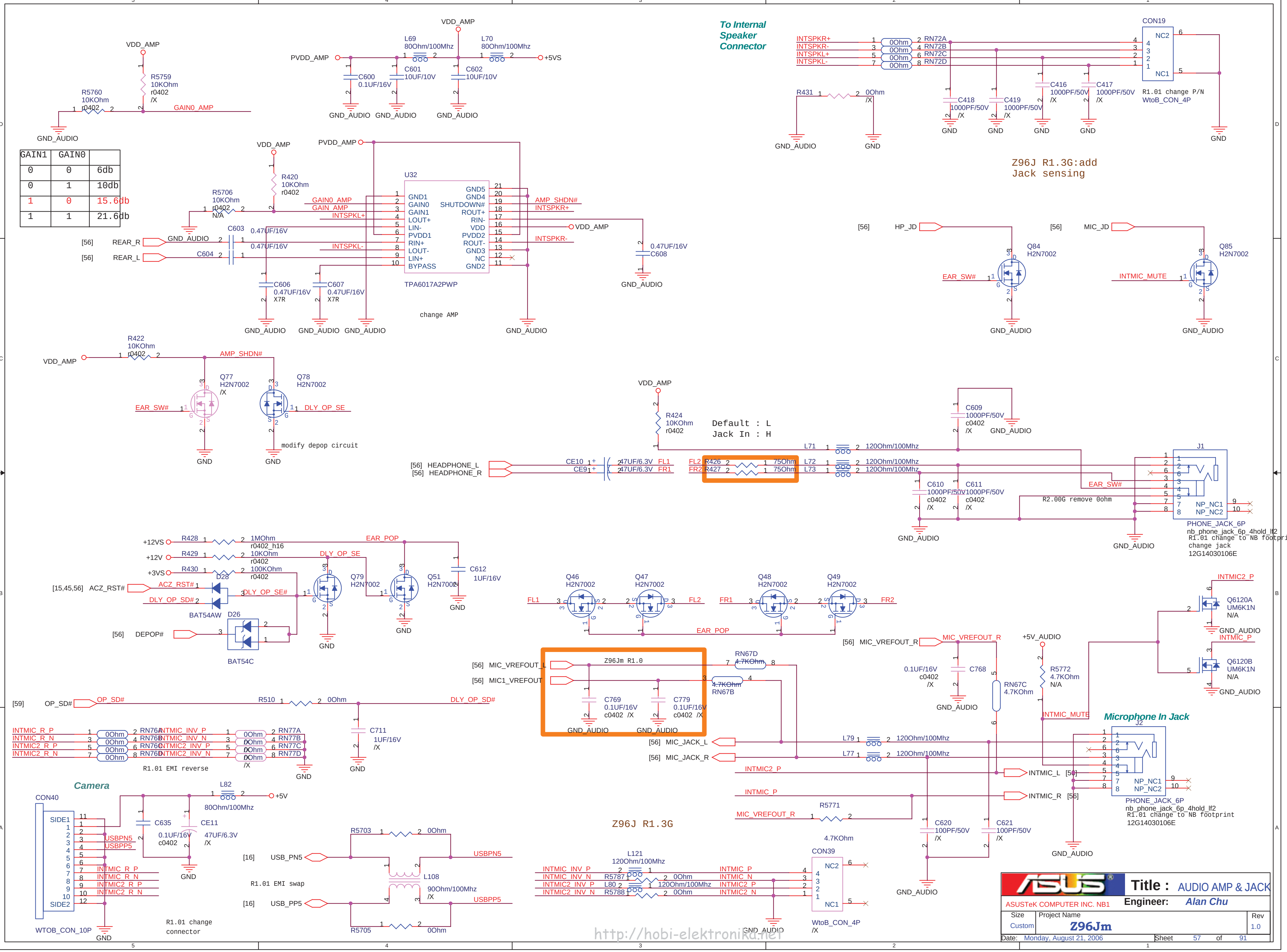
Title : CODEC-ALC660

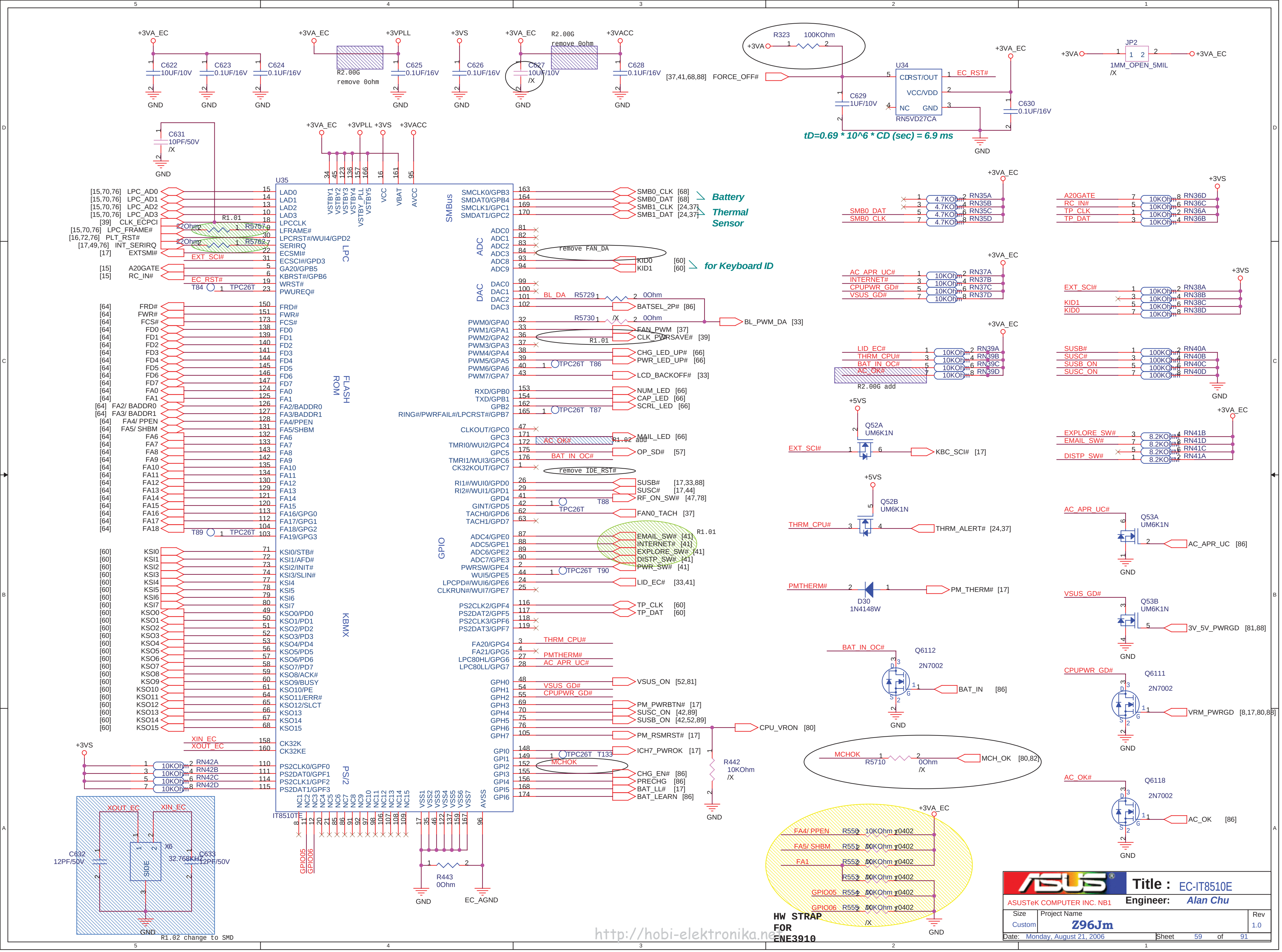
ASUSTeK COMPUTER INC. NB1

Engineer: Alan Chu

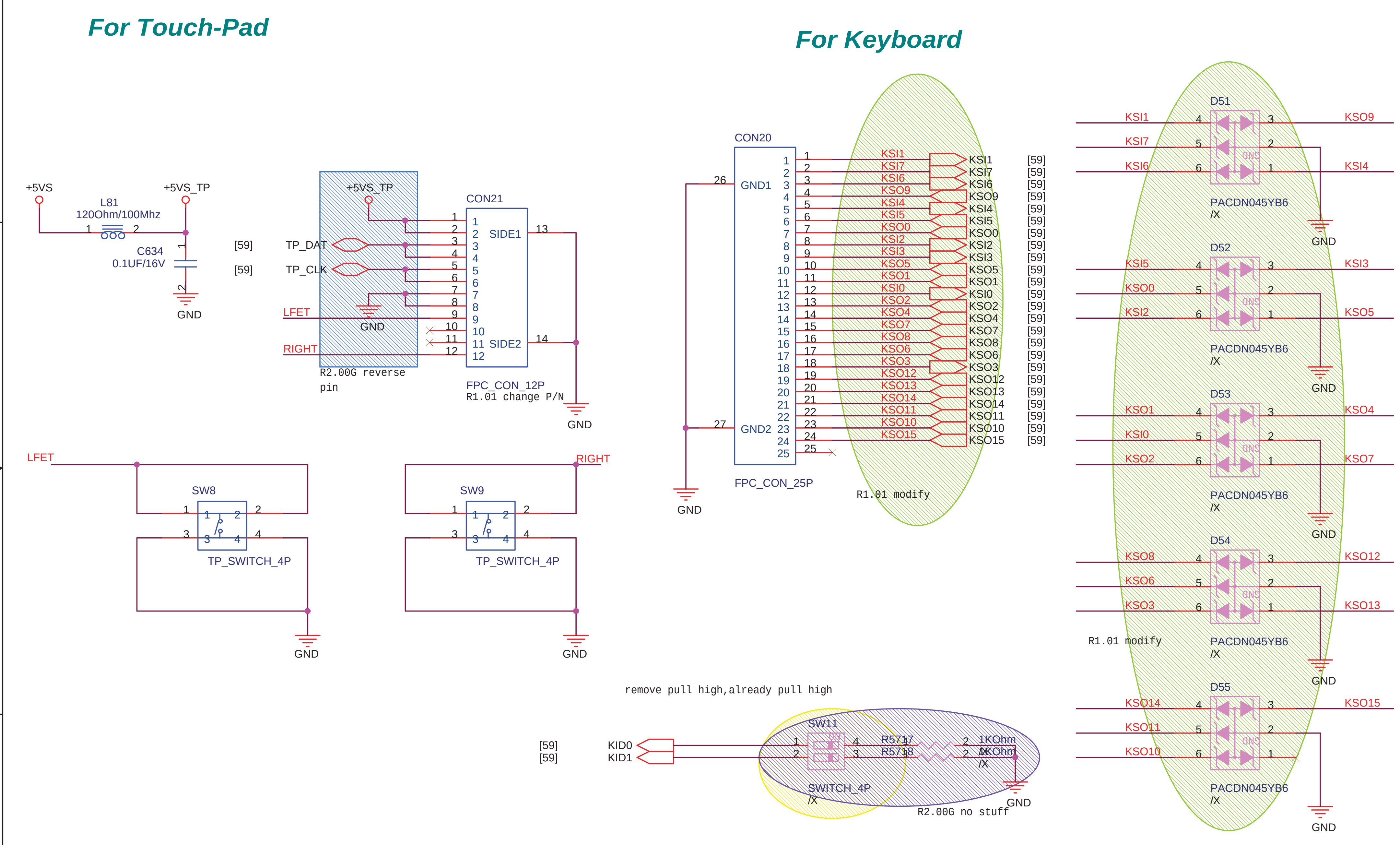
Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 56 of 91


To Internal Speaker Connector
Z96J R1.3G:add Jack sensing
change AMP
TPA6017A2PWP
modify depop circuit
Default : L
Jack In : H
R2.00G remove 0ohm
R1.01 change P/N WtoB_CON_4P
R1.01 change to NB footprint change jack 12G14030106E
R1.01 EMI reverse
Camera
R1.01 EMI swap
R1.01 change connector
Microphone In Jack
Z96Jm R1.0
Z96J R1.3G
GAIN1 GAIN0
0 0 6db
0 1 10db
1 0 15.6db
1 1 21.6db
ASUSTeK COMPUTER INC. NB1
Title : AUDIO AMP & JACK
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 57 of 91
http://hobi-elektronika.net



tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Battery
Thermal
Sensor
for Keyboard ID
U35
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
SMBus
ADC
DAC
U34
RN5VD27CA
HW STRAP FOR ENE3910
R1.02 change to SMD
R2.00G add
remove FAN_DA
remove IDE_RST#
R1.01
R1.02 add
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chu
Size
Custom
Project Name
Z96Jm
Rev
1.0
Date: Monday, August 21, 2006
Sheet 59 of 91



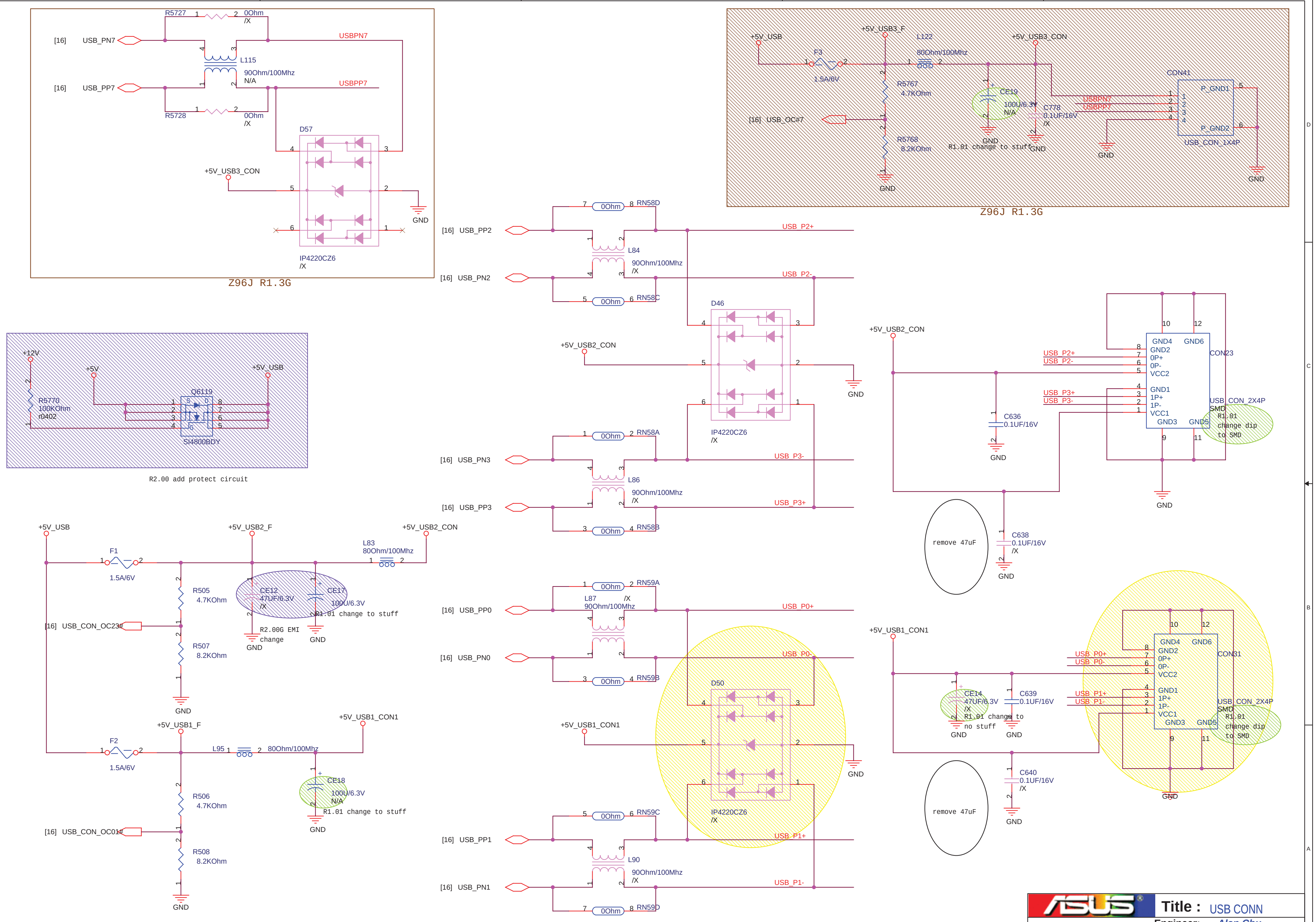
ASUSTeK COMPUTER INC. MB6

Title : Touch Pad & KB

Engineer: ALAN CHU

Size	Project Name	Rev
A4	Z96Jm	1.0

Date: Monday, August 21, 2006 | Sheet 60 of 91



ASUSTeK COMPUTER INC

Title :	USB CONN	
Engineer:	Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 62 of 91	

ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved

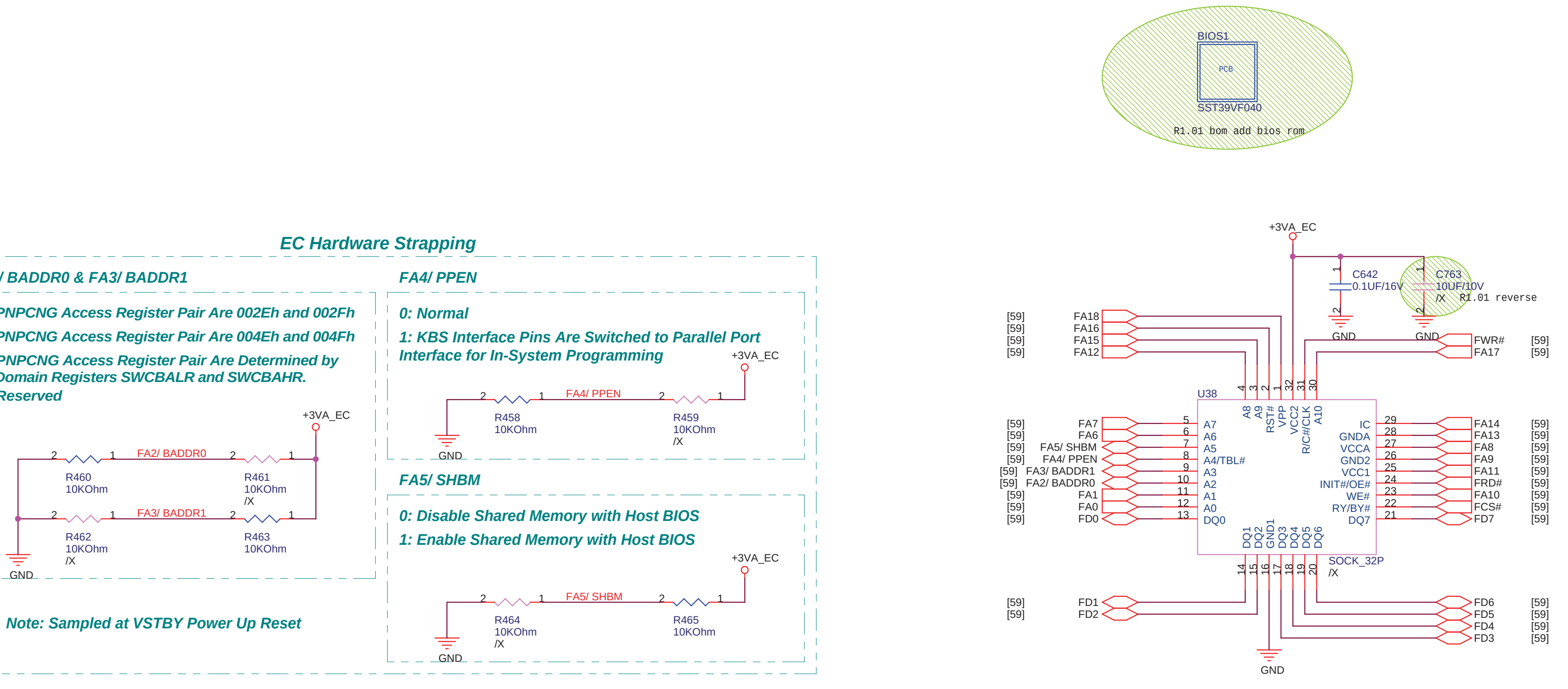
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

FA5/ SHBM

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

Note: Sampled at VSTBY Power Up Reset



ASUSTeK COMPUTER INC. NB1

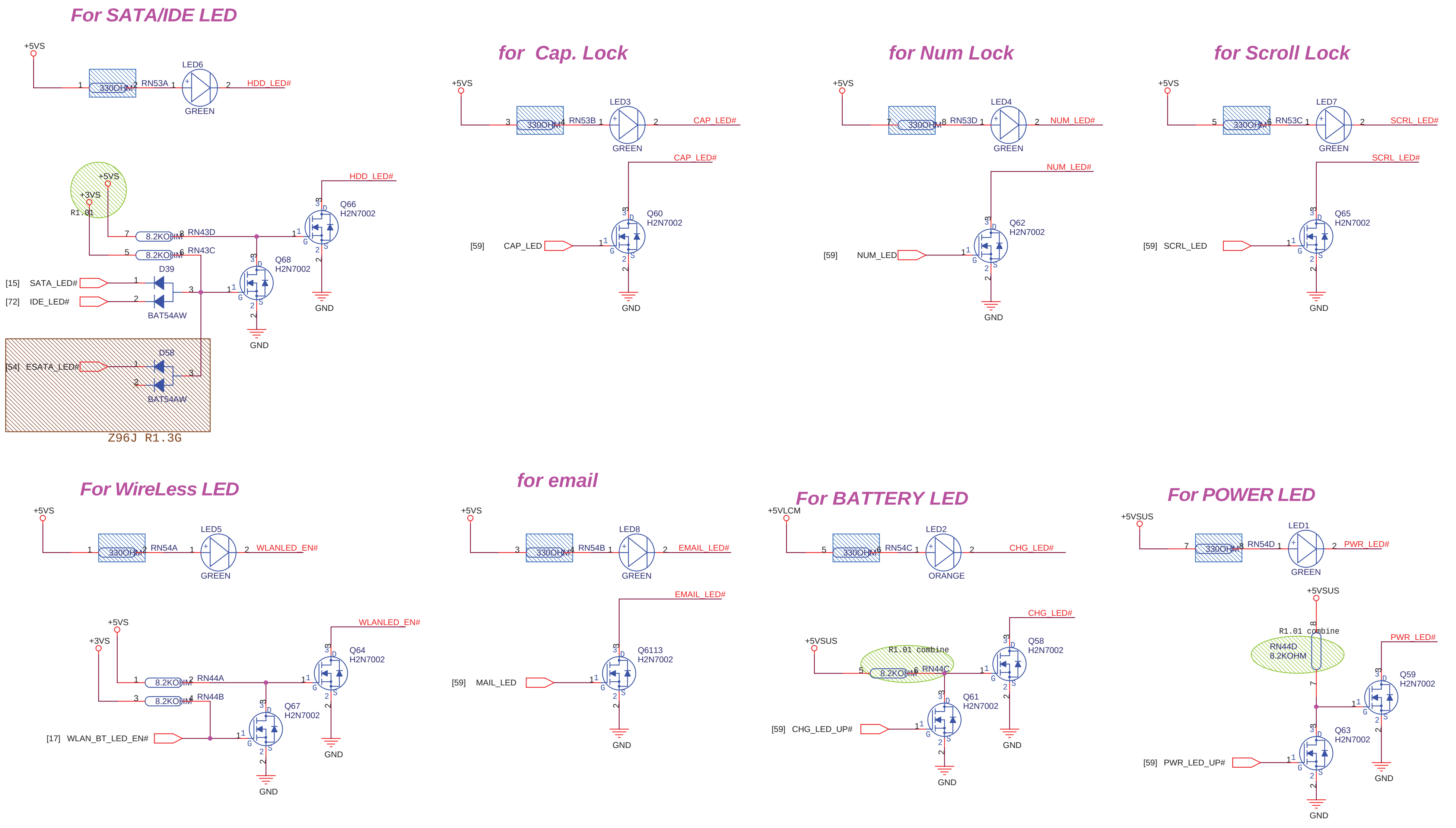
Title : ISA ROM

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 64 of 91

For LED



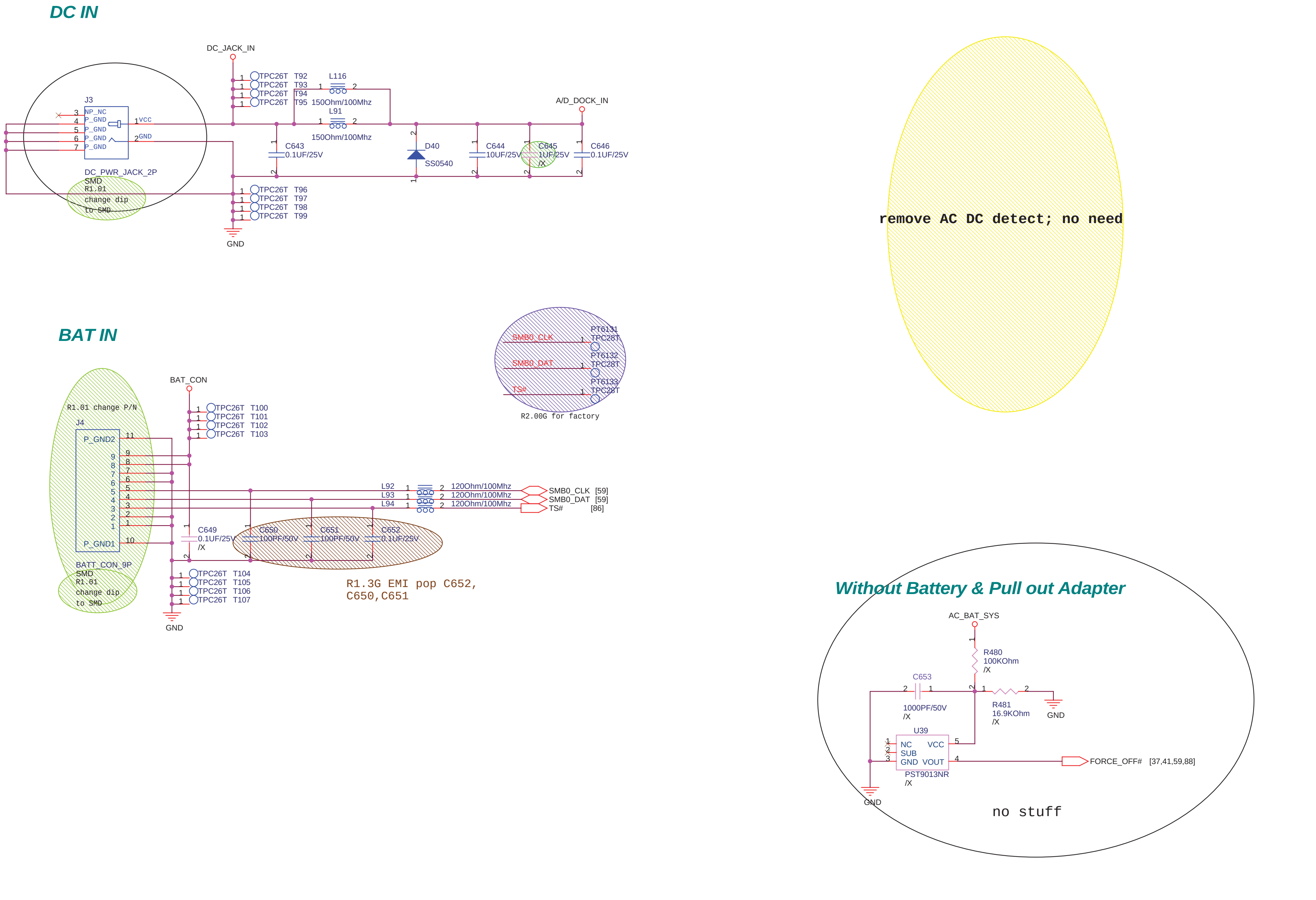
ASUSTeK COMPUTER INC

Title : LED

Engineer: Alan Chu

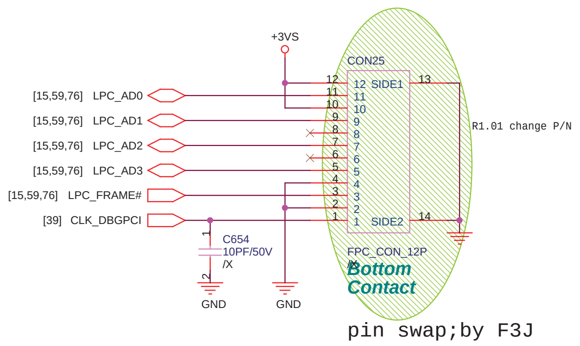
Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 66 of 91

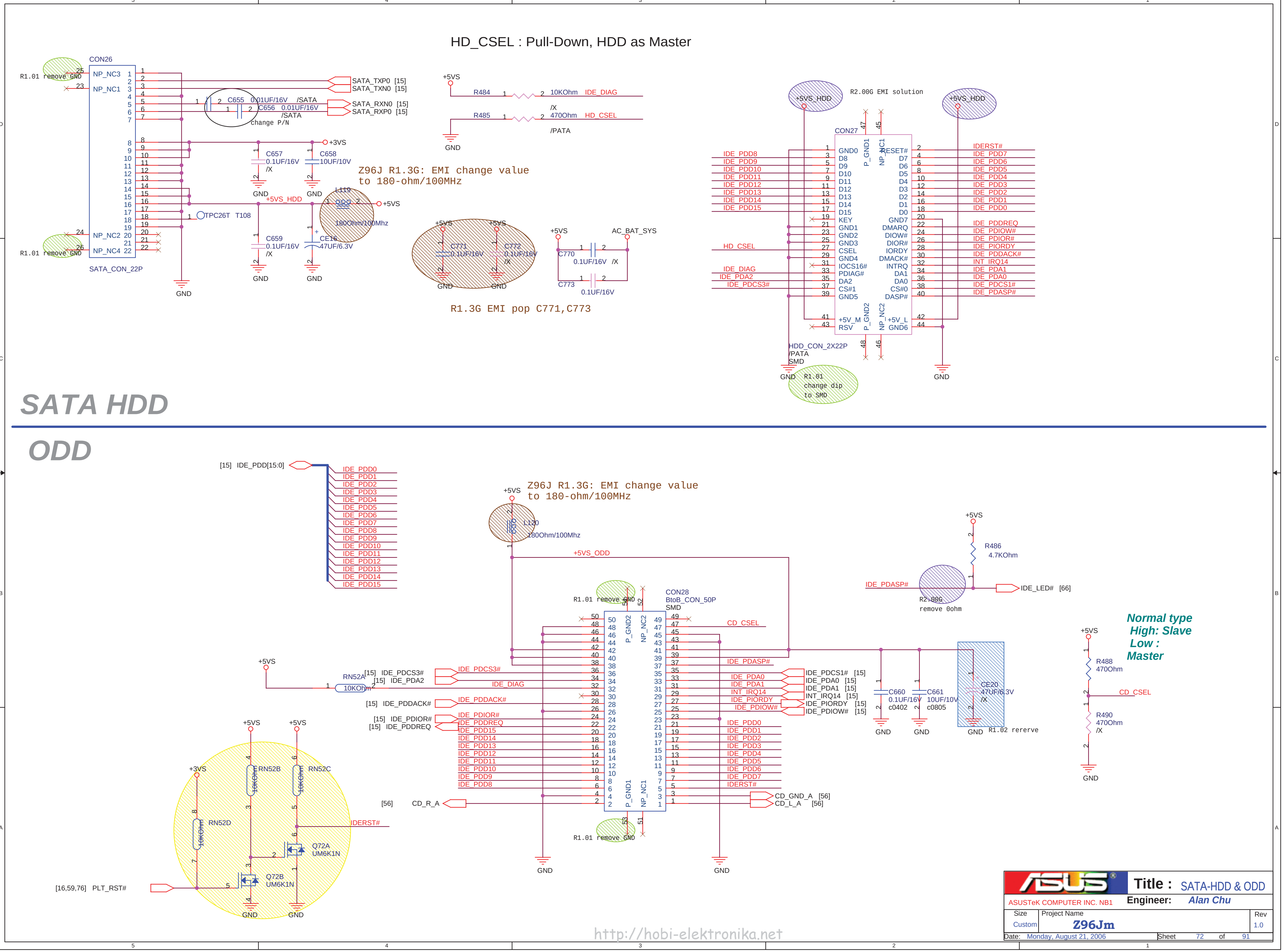


ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 68	of 91	

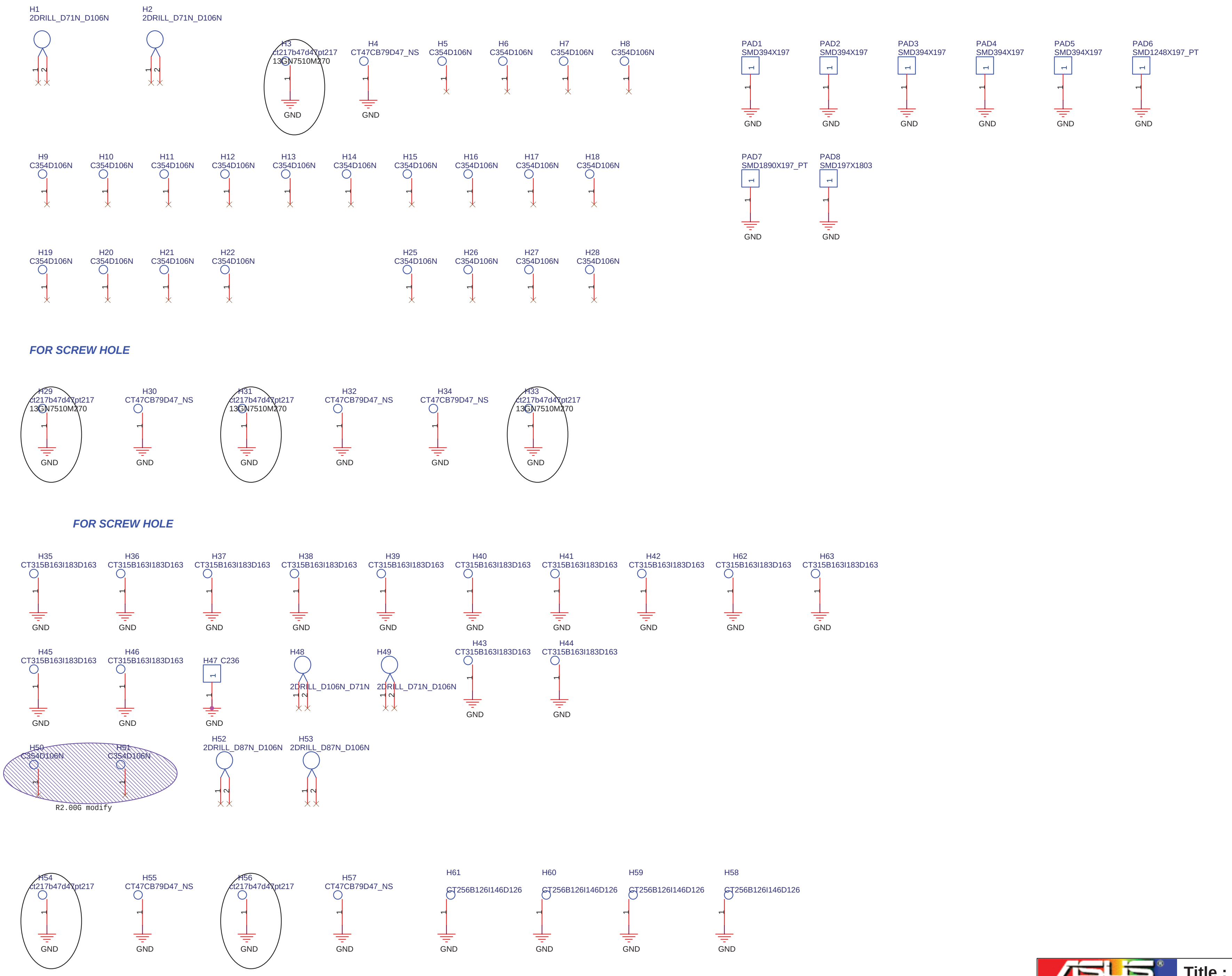
For Debug



ASUSTeK COMPUTER INC	Title : Debug CONN.		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006		Sheet 70	of 91

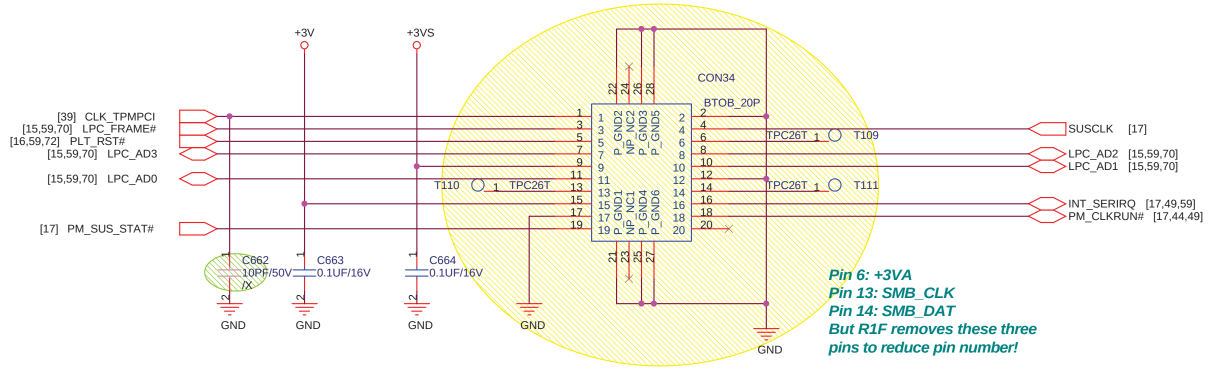


HD_CSEL : Pull-Down, HDD as Master
CON26
SATA_CON_22P
R1.01 remove GND
SATA_TXP0 [15]
SATA_TXN0 [15]
SATA_RXN0 [15]
SATA_RXP0 [15]
change P/N
Z96J R1.3G: EMI change value
to 180-ohm/100MHz
L119
180Ohm/100Mhz
+5VS_HDD
R1.3G EMI pop C771,C773
R484 10KOhm IDE_DIAG
R485 470Ohm HD_CSEL
/PATA
R2.00G EMI solution
CON27
HDD_CON_2X22P
/PATA
SMD
R1.01
change dip
to SMD
SATA HDD
ODD
[15] IDE_PDD[15:0]
Z96J R1.3G: EMI change value
to 180-ohm/100MHz
L120
180Ohm/100Mhz
+5VS_ODD
CON28
BtoB_CON_50P
SMD
R1.01 remove GND
R2.00G
remove 0ohm
R486 4.7KOhm
IDE_LED# [66]
Normal type
High: Slave
Low :
Master
R488 470Ohm
R490 470Ohm
CD_CSEL
CE20 47UF/6.3V
R1.02 rerere
RN52A RN52B RN52C RN52D 10KOhm
Q72A UM6K1N
Q72B UM6K1N
[16,59,76] PLT_RST#
IDERST#
[56] CD_R_A
CD_GND_A [56]
CD_L_A [56]
ASUSTeK COMPUTER INC. NB1
Title : SATA-HDD & ODD
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 72 of 91



ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: ALan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 74 of 91	

For TPM Module

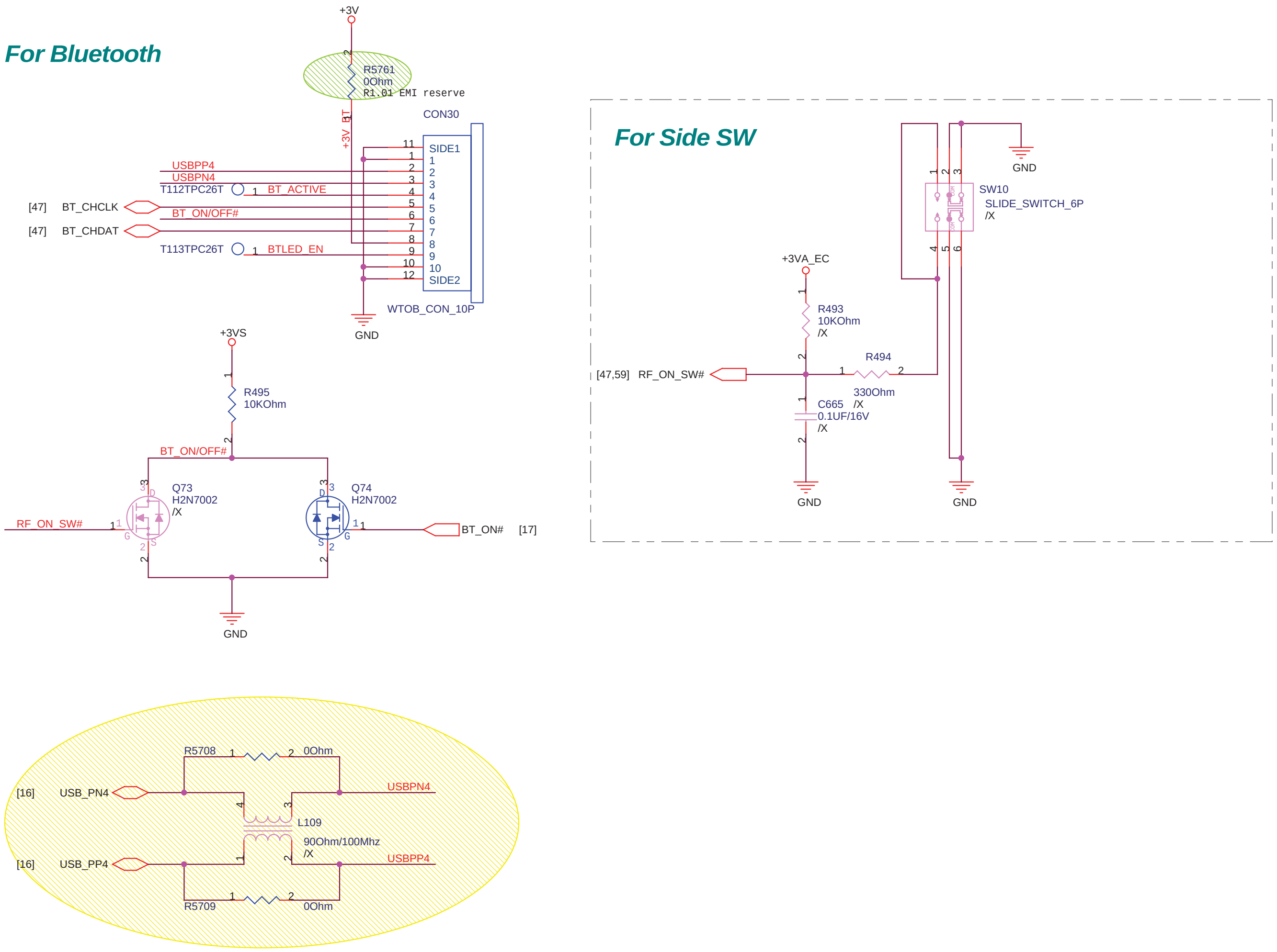


Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

ASUSTeK COMPUTER INC	Title : TPM	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 76 of 91		

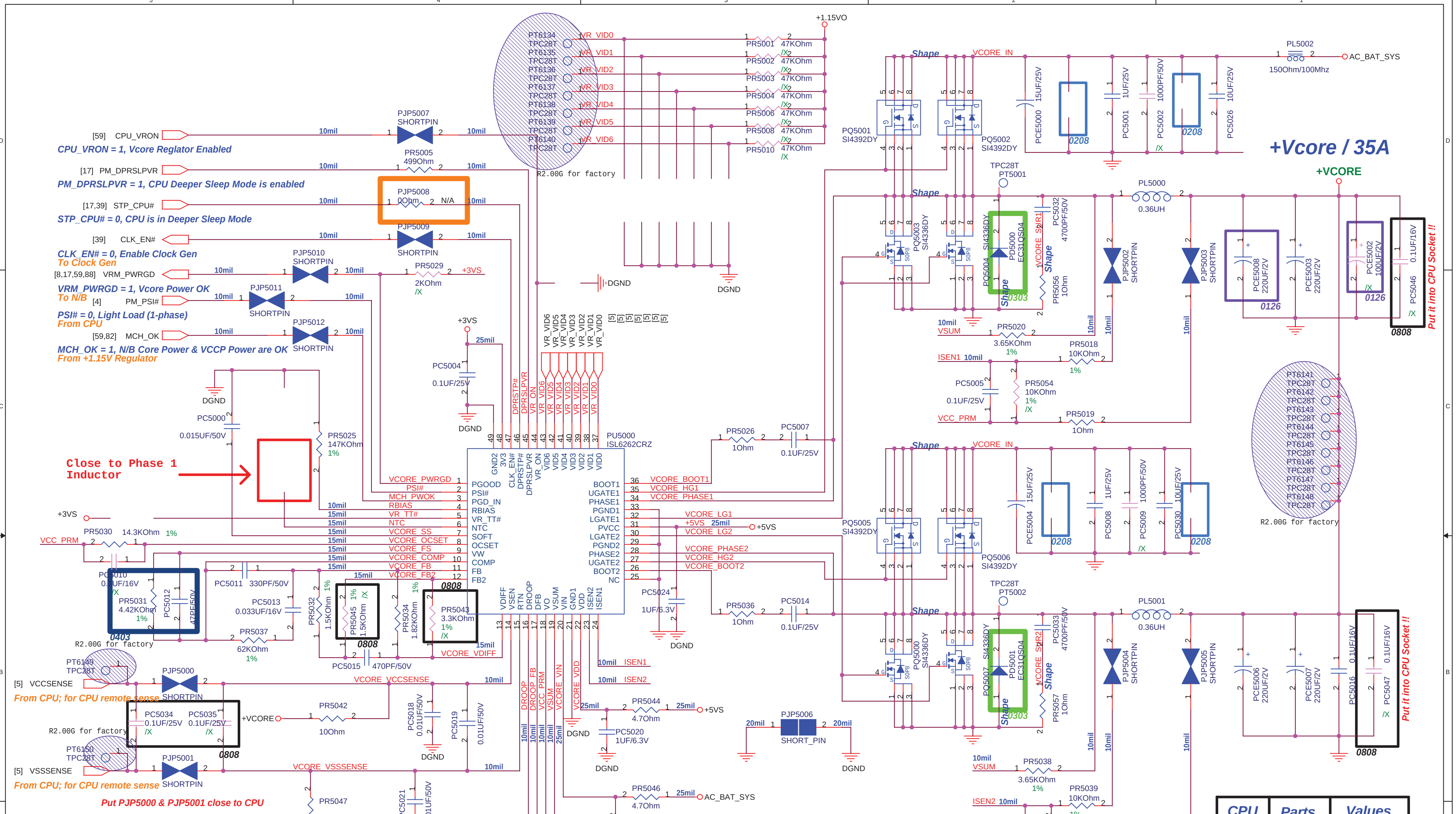
For Bluetooth

For Side SW



ASUSTeK COMPUTER INC

Title :	Blue Tooth
Engineer:	Alan Chu
Size	Custom
Project Name	Z96Jm
Rev	1.0
Date:	Monday, August 21, 2006
Sheet	78 of 91



Net	Width	Net	Width
VR_VIO0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape

CPU	Parts	Values
Yonha	PCE5002 PCE5003	220UF/2V 11G08D222795
Merom	PCE5006 PCE5007	330UF/2V 11G08D337791

<Variant Name>

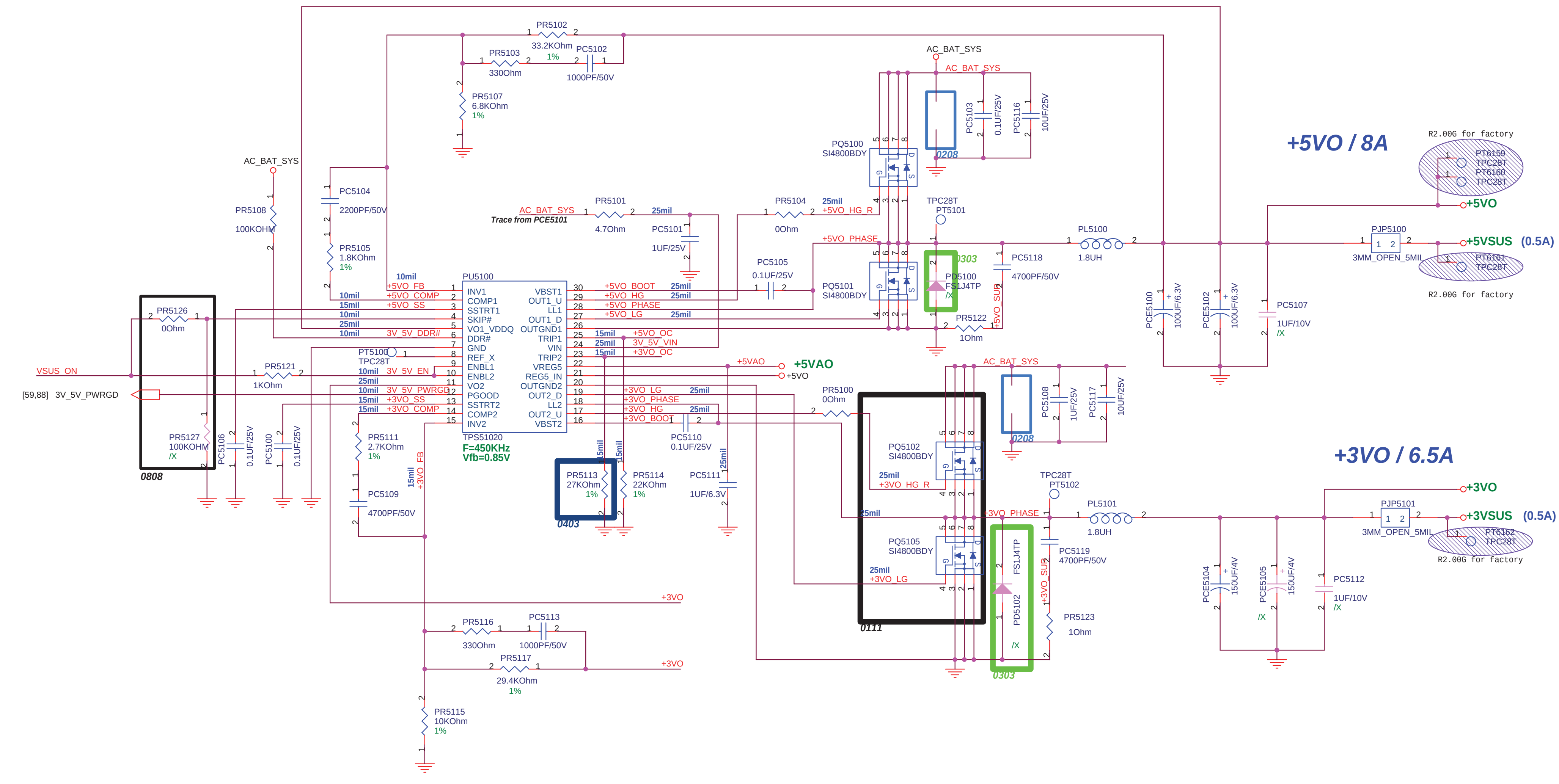
Title : POWER_VCORE

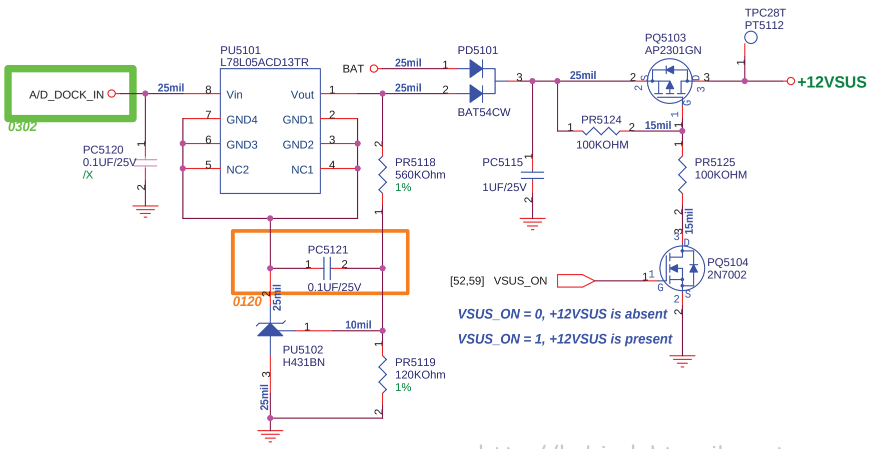
<OrgName>

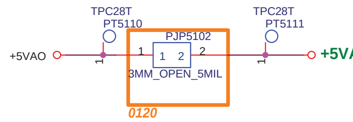
Engineer:

Size	Project Name	Rev
Custom	NAPA	1.0

Date: Monday, August 21, 2006 Sheet 80 of 91







Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

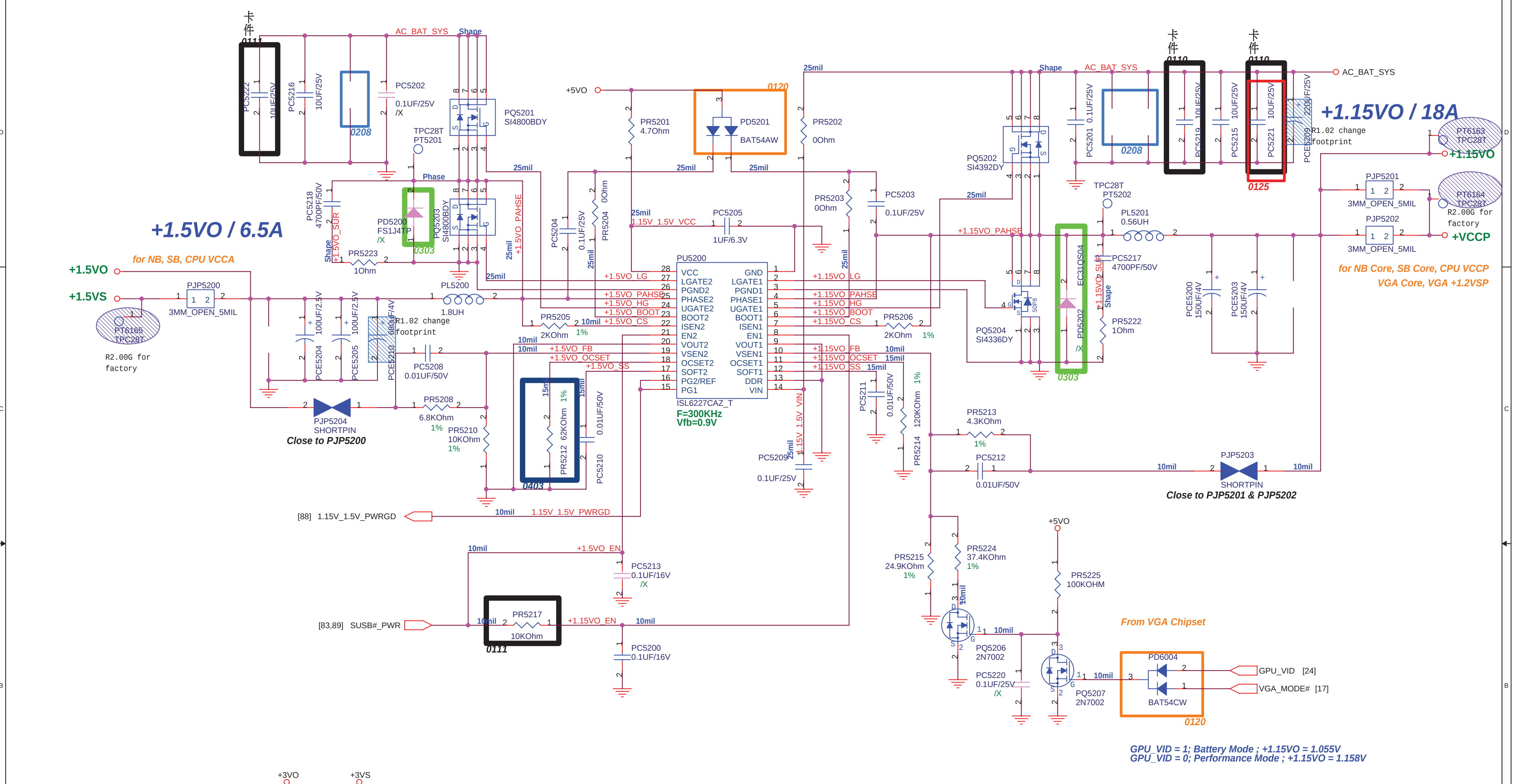
Title : POWER_SYSTEM

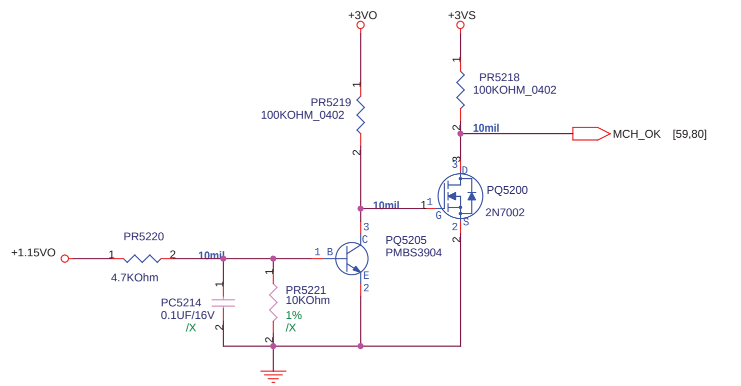
<OrgName>

Engineer:

Size: Custom | Project Name: NAPA | Rev: 1.0

Date: Monday, August 21, 2006 | Sheet 81 of 91





Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

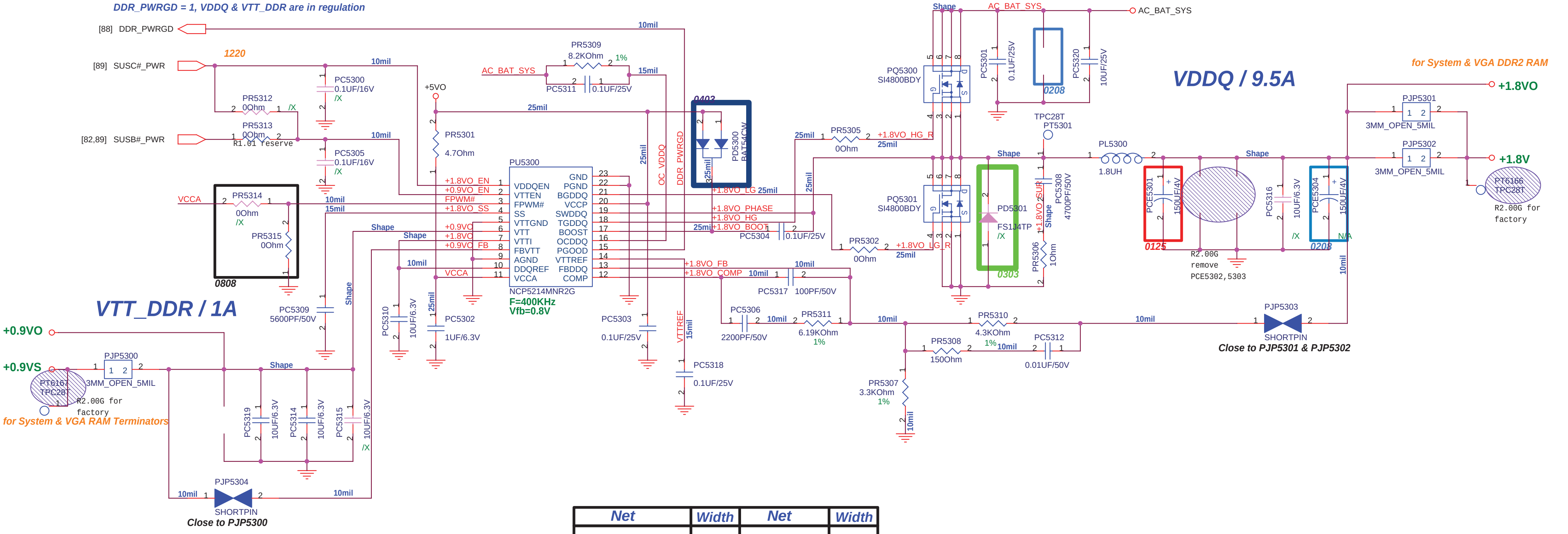
Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	1.0

Date: Monday, August 21, 2006 Sheet 82 of 91



Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

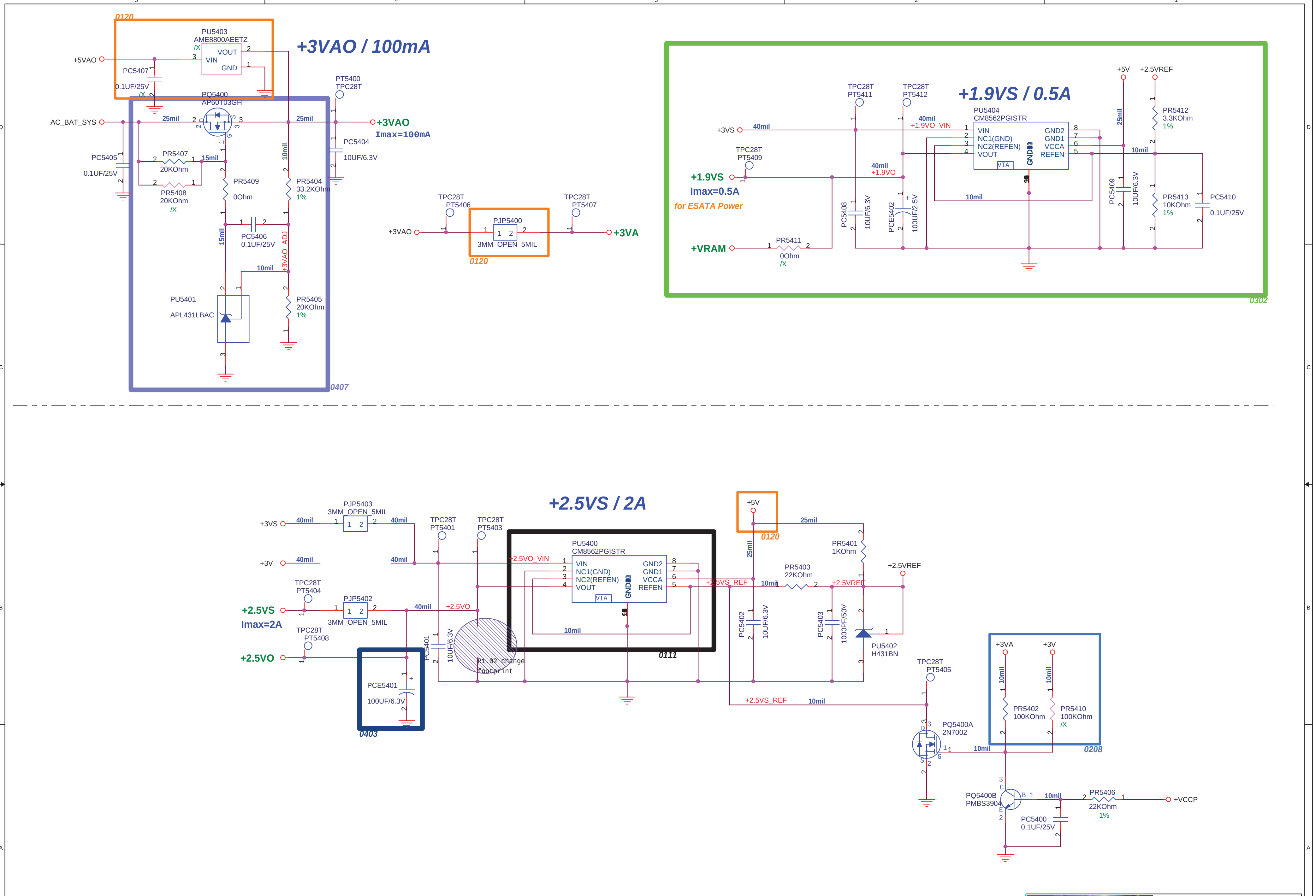
Title : POWER_I/O_DDR & VTT

<OrgName>

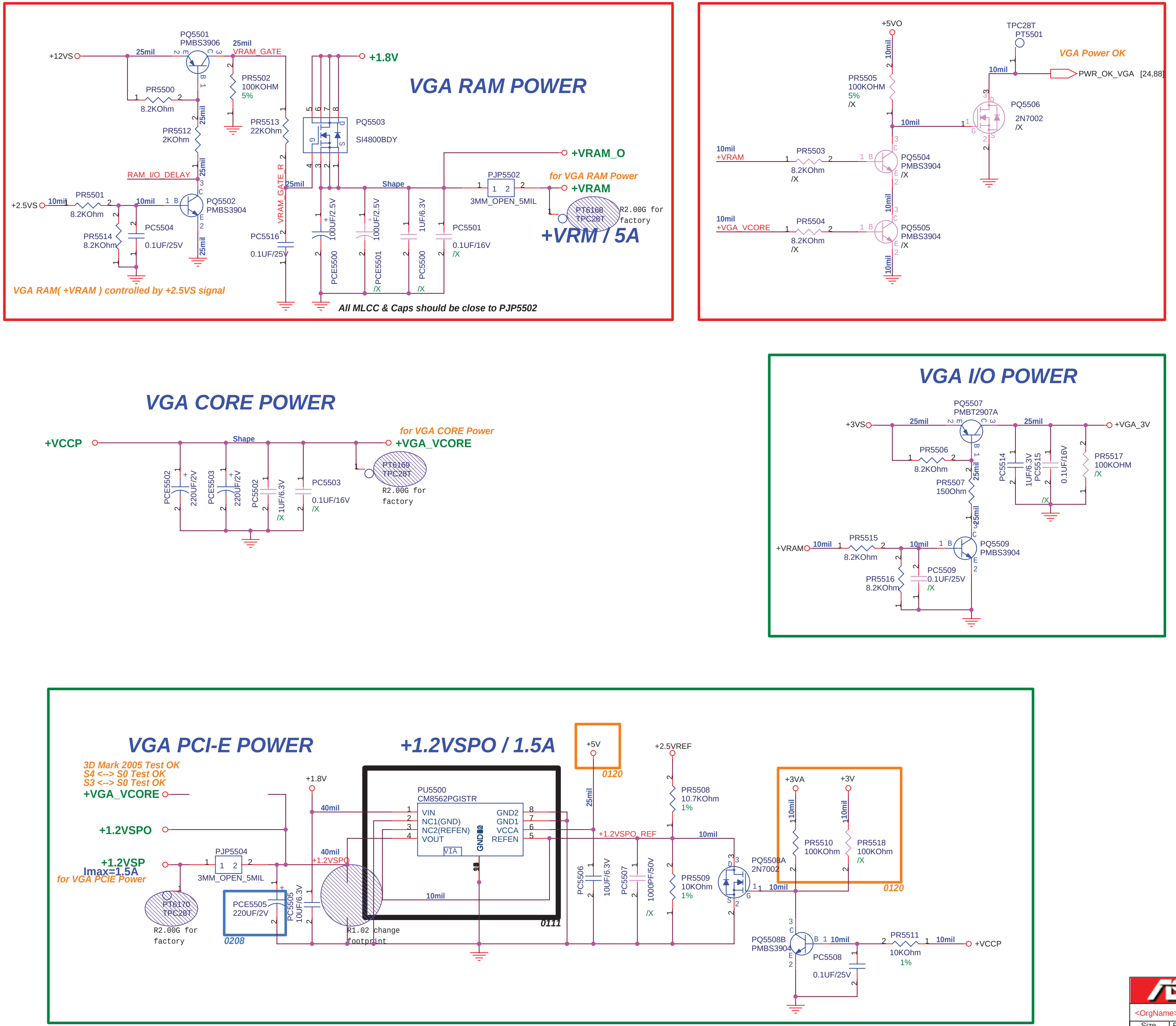
Engineer:

Size	Project Name	Rev
Custom	NAPA	2.1

Date: Monday, August 21, 2006 Sheet 83 of 91



Title :	POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 2.1
Date: Monday, August 21, 2006	Sheet 84	of 91	



Title : POWER_VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.1

Date: Monday, August 21, 2006 Sheet 85 of 91

POWER PATH & BAT_LEARN

Charger shut down condition :

1. Victl < 0.06V
2. PKPRES# > 55% of MAX8725_LDO
3. AC Adaptor Removed

The timing of PDL & PDS switch :

BAT - A/D_DOCK_IN > 100mV--> Battery mode

The current capacity of MAX8725_LDO is 10mA.

VBAT_DLGV is a voltage for driving MOSFET.

MAX8725_ACIN < 10.27V, AC Adaptor absent

MAX8725_ACIN > 10.27V, AC Adaptor present

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V<Vmoce<2V)	Battery Learn

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

Battery Charging Voltage :

+V_BAT= 3 x [4.2235+(Vvctl-1.8)/9.52]

Battery Charging Current :

Icharge=(0.075/PR5706) x (Victl/3.6))

Input Adaptor Max. Current Limit :

Ilimit_current=(0.075/PR5701) x (Vcls/4.2235)

Pre-Charging Mode :

Precharging current = 150 ~ 160mA

Victl = 0.100V ~ 0.120V

Battery Cell Selection :

BATSEL_2P# = 1, 6 Cells; Victl = 2.084V

=> Icharge = 2.894A

BATSEL_2P# = 0, 9 Cells; Victl = 3.219V

=> Icharge = 4.472A

Adaptor Max. Current :

PR5714 = 178K; Vcls = 3.79V, Ilimit = 4.5A; 90W

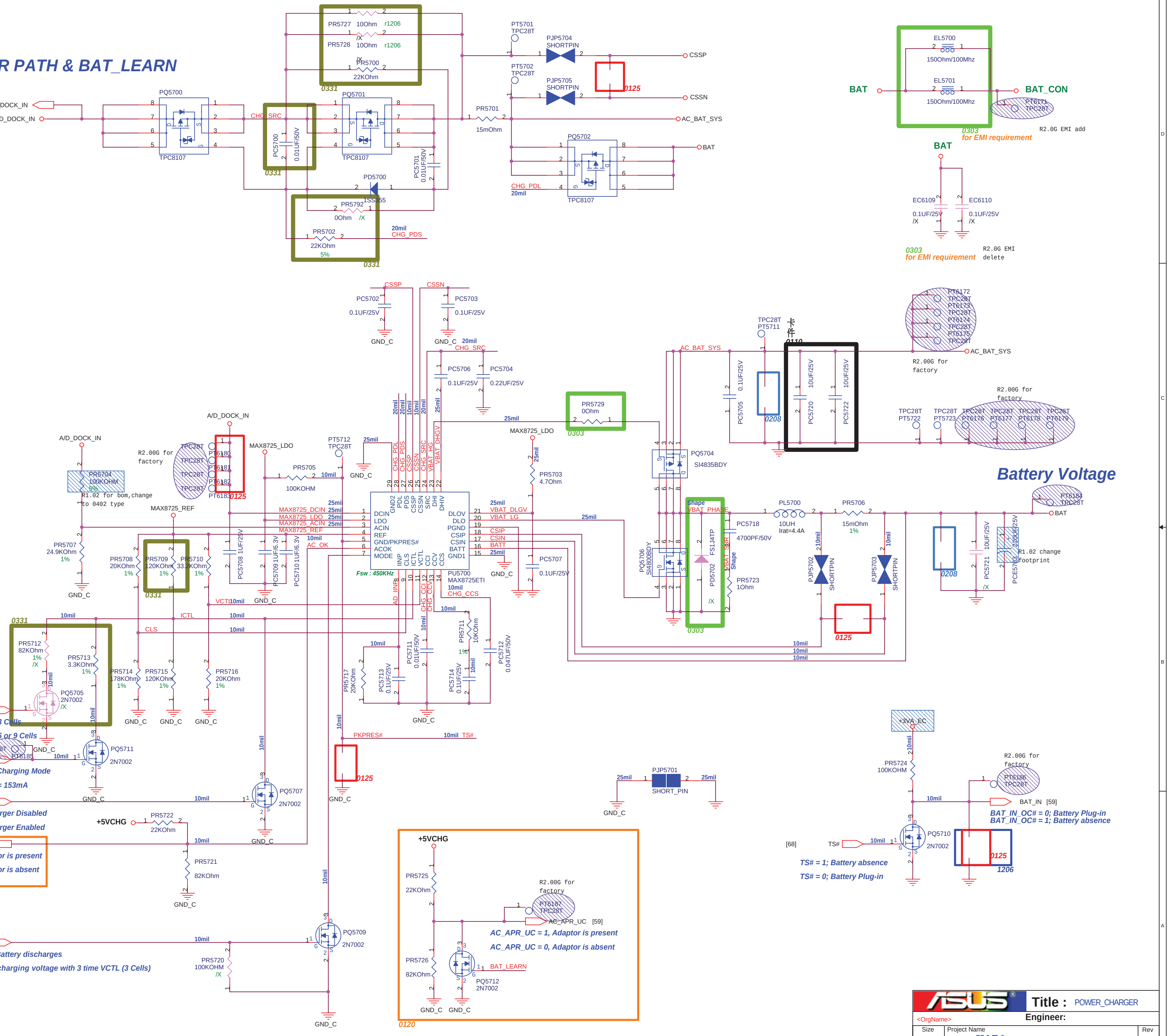
PR5714 = 47K; Vcls = 2.96V, Ilimit = 3.5A; 65W

BATSEL_SP# = 1, 3-Cell

Victl = 1.22V / Icharge = 1.69A

BATSEL_SP# = 0, 6-Cell or 9-Cell

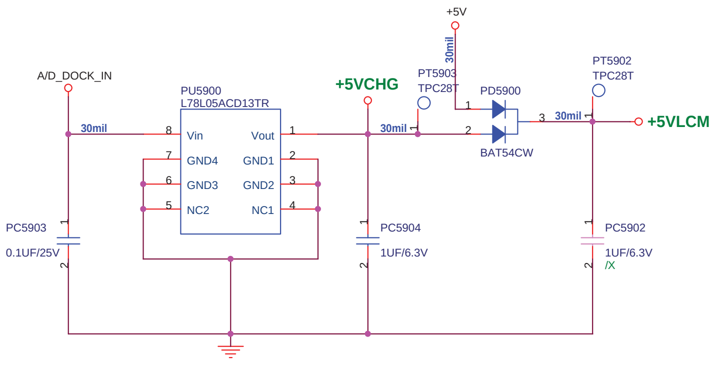
Victl = 2.11V / Icharge = 2.93A



Title : POWER_CHARGER	
Engineer:	
Size: C	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 86 of 91

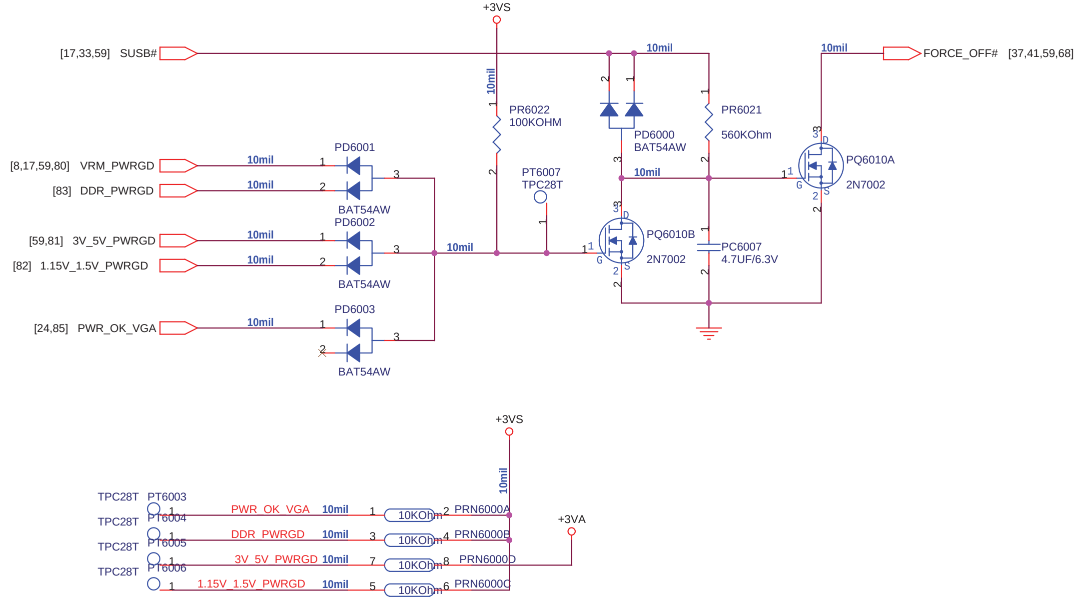
REMOVE BATTERY IN DETECT

+5VLCM / +5VCHG



ASUS	Title : POWER_DETECT		
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 2.1
Date: Monday, August 21, 2006	Sheet 87 of 91		

Power Good Detecter



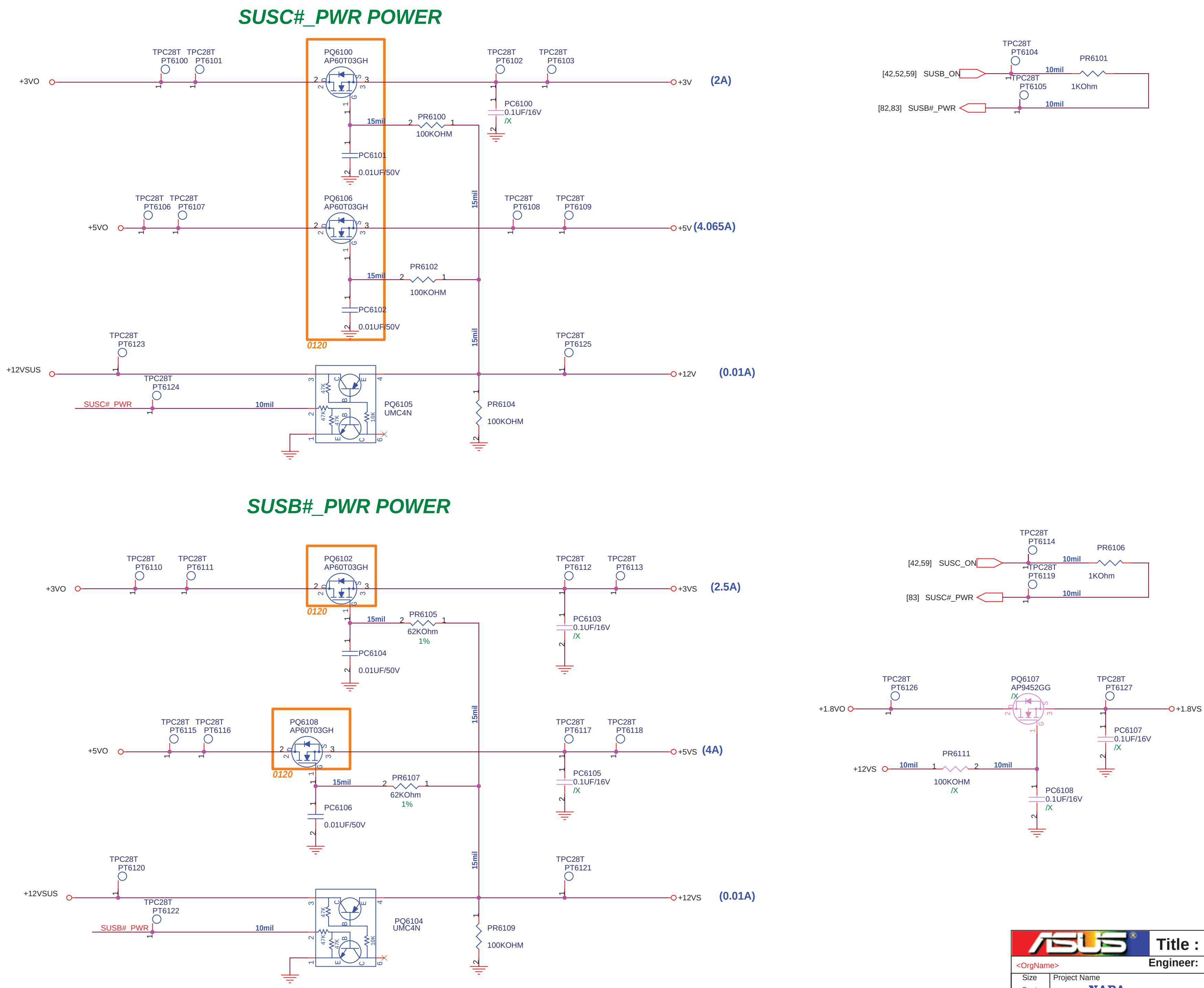
Title : POWER_PROTECT

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.1

Date: Monday, August 21, 2006 Sheet 88 of 91



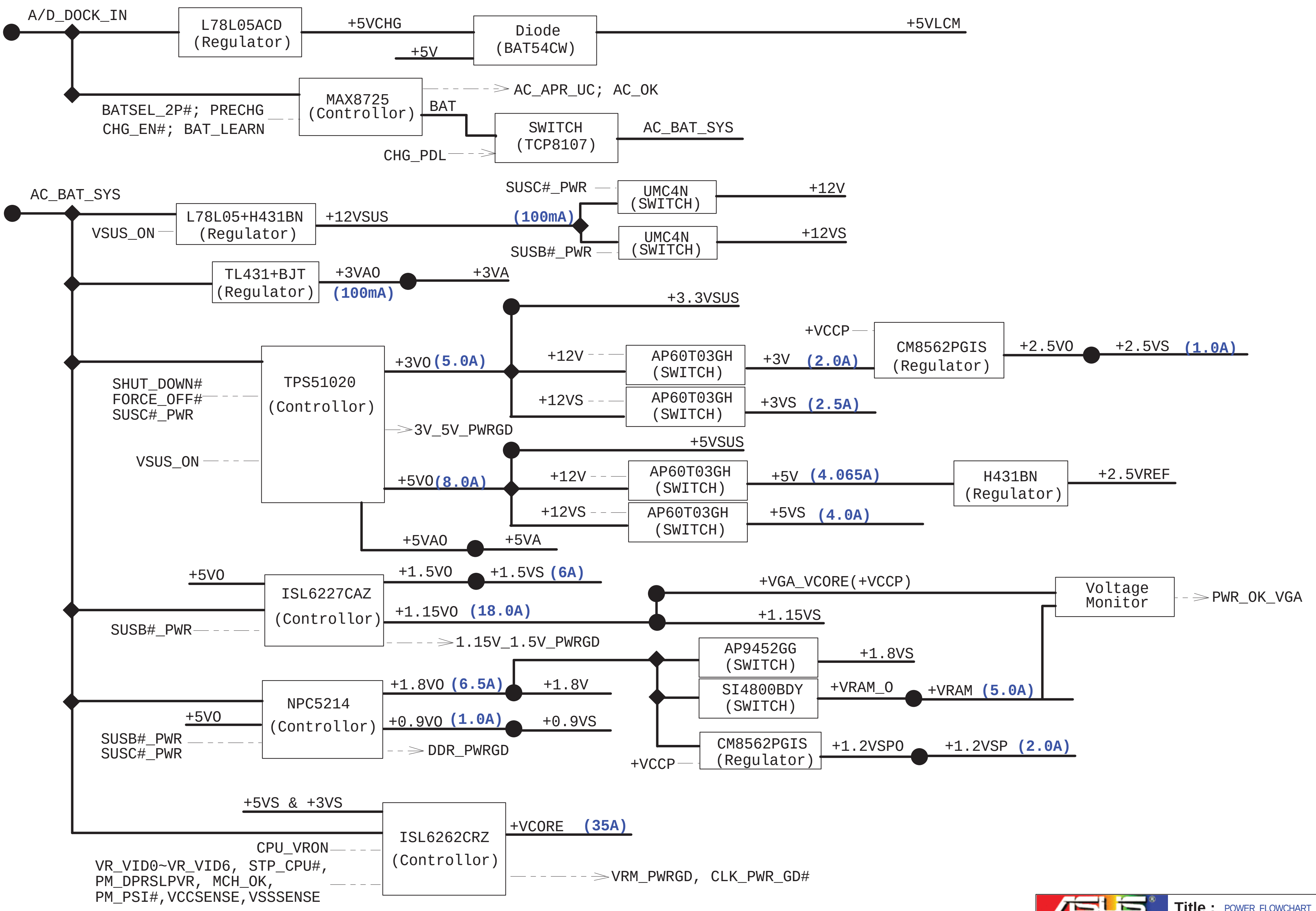
Title : POWER_LOAD SWITCH

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.1

Date: Monday, August 21, 2006 Sheet 89 of 91



ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 90 of 91	

AC_BAT_SYS	AC_BAT_SYS	[33,68,72,80,81,82,83,84,86]
+3VA	+3VA	[15,33,42,59,84,85,88]
+5VA	+5VA	[81]
+5VO	+5VO	[81,82,83,85,89]
+3VO	+3VO	[81,82,89]
+3VSUS	+3VSUS	[16,17,18,44,45,47,52,81]
+5VSUS	+5VSUS	[18,66,81]
+3V	+3V	[33,42,44,45,47,76,78,84,85,89]
+3VS	+3VS	[4,8,12,15,16,17,18,20,21,32,33,35,37,39,42,47,49,50,51,52,54,56,57,59,66,70,72,76,78,80,82,84,85,88,89]
+12VSUS	+12VSUS	[81,89]
+12V	+12V	[42,51,57,62,89]
+12VS	+12VS	[17,27,33,57,85,89]
+5V	+5V	[42,44,57,62,84,85,87,89]
+5VS	+5VS	[18,32,37,42,44,49,56,57,59,60,66,72,80,89]
+2.5VO	+2.5VO	[84]
+2.5VS	+2.5VS	[8,12,24,27,42,84,85]
+1.8VO	+1.8VO	[83,89]
+1.8V	+1.8V	[8,11,20,21,22,42,83,85]
+1.8VS	+1.8VS	[27,89]
+VCCP	+VCCP	[4,5,7,9,11,12,15,18,24,27,39,42,82,84,85]
+0.9VS	+0.9VS	[22,28,29,42,83]
BAT	BAT	[81,86]
+5VCHG	+5VCHG	[86,87]
+5VLCM	+5VLCM	[66,87]
+2.5VREF	+2.5VREF	[84,85]
+VCORE	+VCORE	[5,80]
+VGA_VCORE	+VGA_VCORE	[4,5,7,9,11,12,15,18,24,27,39,42,82,84,85]
+VRAM	+VRAM	[25,27,28,29,42,84,85]
+1.2VSP	+1.2VSP	[26,27,85]
BAT_CON	BAT_CON	[68,86]
+1.2VSPO	+1.2VSPO	[85]

Title : POWER_SIGNAL

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.1