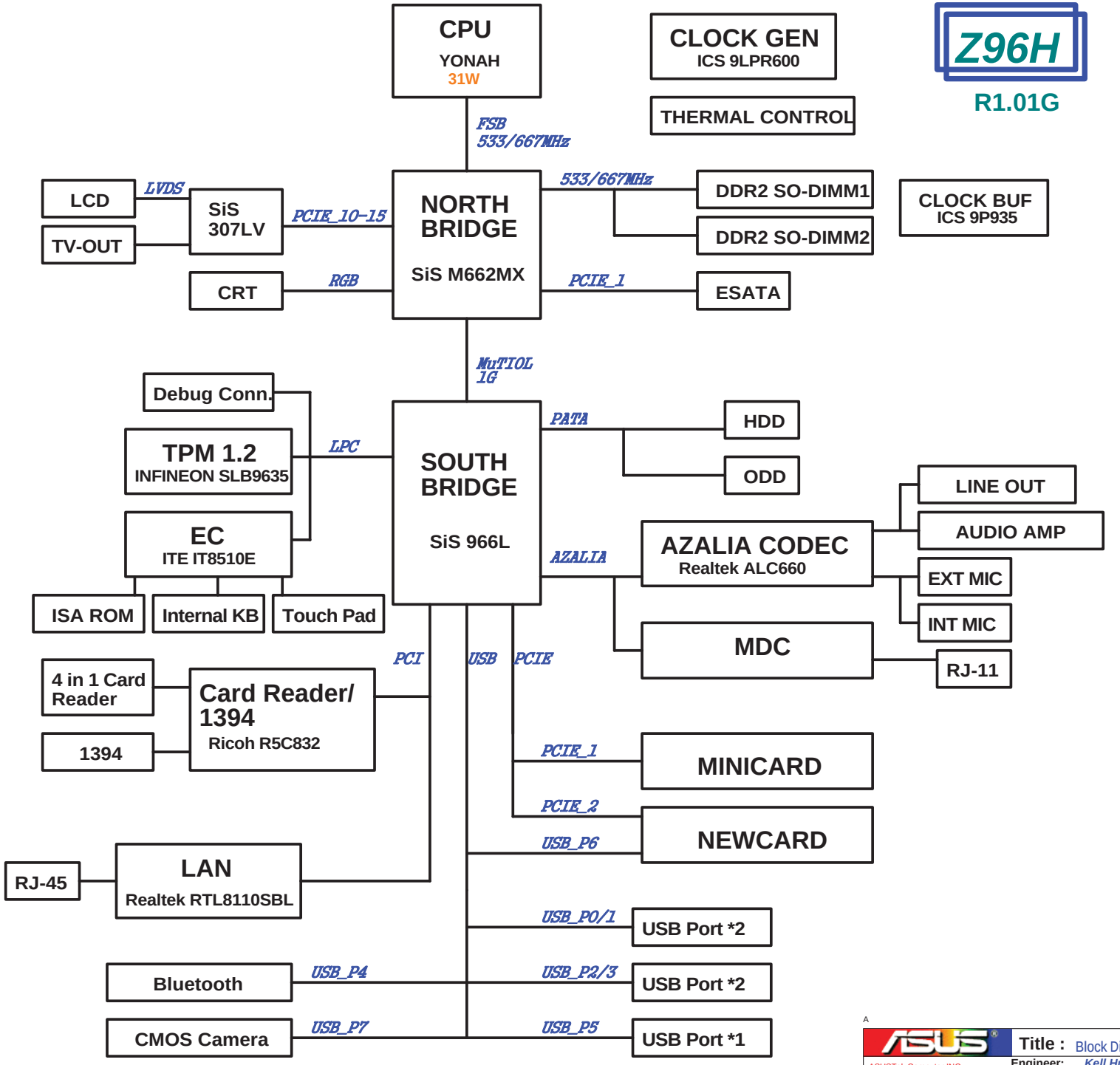


ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 1 of 60	

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O	H	GPI
37	PWM3/GPA3	/	I		GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	AC_OK#	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

06/01/23

Pin	Pin Name	Signal Name	Type	Default	
48	GPH0	VSUS_ON	O	L	GPI
54	GPH1	VSUS_GD#	I	H	GPI
55	GPH2	CPUPWR_GD#	I	H	GPI
69	GPH3	PM_PWRBTN#	O	H	GPI
70	GPH4	SUSC_ON	O	L	GPI
75	GPH5	SUSB_ON	O	L	GPI
76	GPH6	CPU_VRON	O	L	GPI
105	GPH7	PM_RSMRST#	O	L	GPI
148	GPI0	ICH7_PWROK	O	L	GPI
149	GPI1	/	O		GPI
152	GPI2	MCHOK	I	L	GPI
155	GPI3	CHG_EN#	O	H	GPI
156	GPI4	PRECHG	O	L	GPI
168	GPI5	BAT_LL#	O	H	GPI
174	GPI6	BAT_LEARN	O	L	GPI
93	ADC8	KID0	I		
94	ADC9	KID1	I		
101	DAC2	BL_PWM_DA	O		
102	DAC3	BATSEL_2P#	O		

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	01001100 (4C)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD24	0	C
1394	AD24	0	B
LAN	AD23	1	D

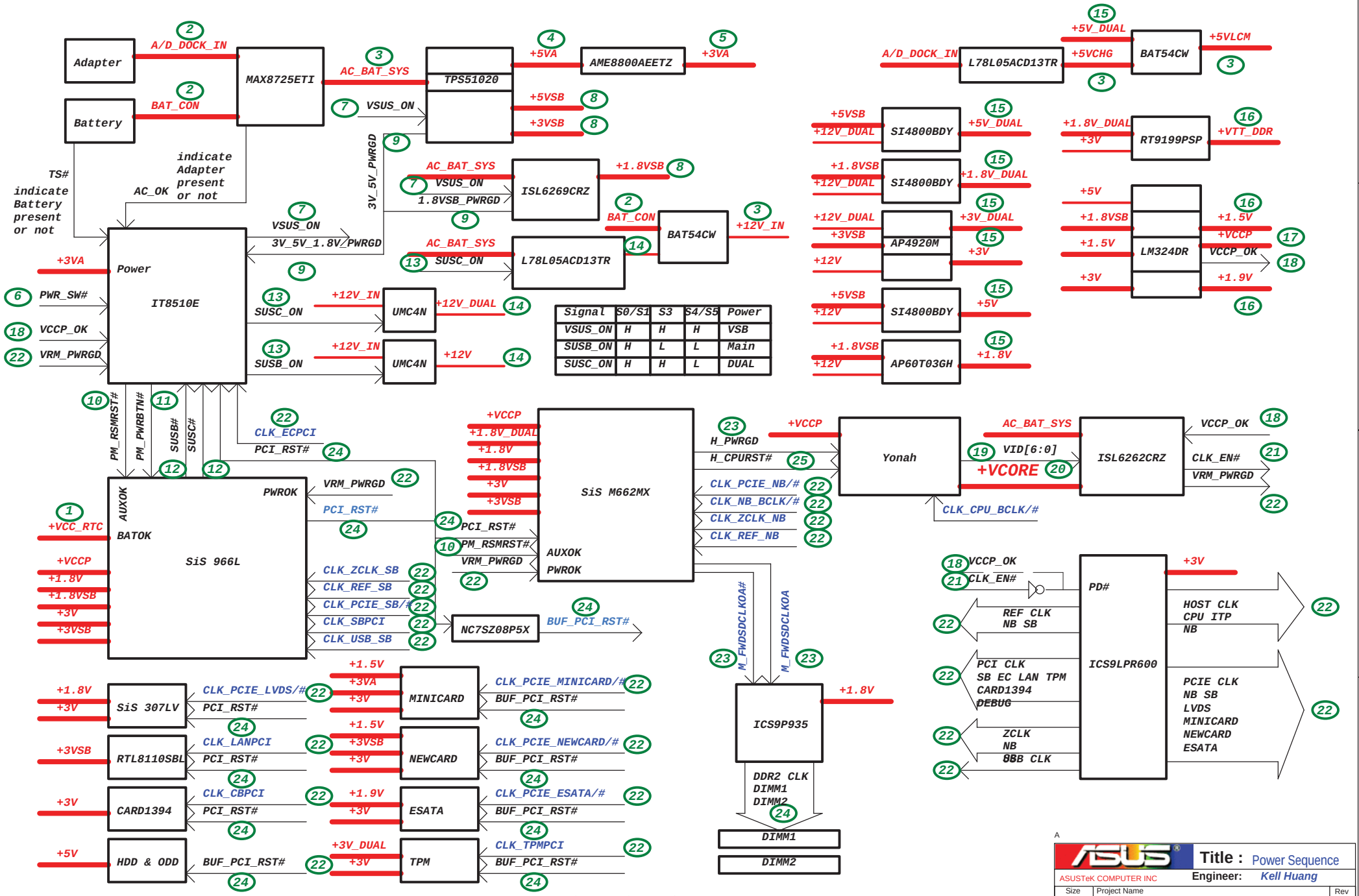
ASUSTek Computer INC.

Title : System Setting

Engineer: Kell Huang

Size	Project Name	Rev
Custom	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 2 of 60



CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.00G	2006/03/06	Z96H Schematic 1.00G (base on Z96F), NB: SiS M662MX SB: SiS 966L

Rev	Date	Description

ASUSTeK COMPUTER INC

Title : History

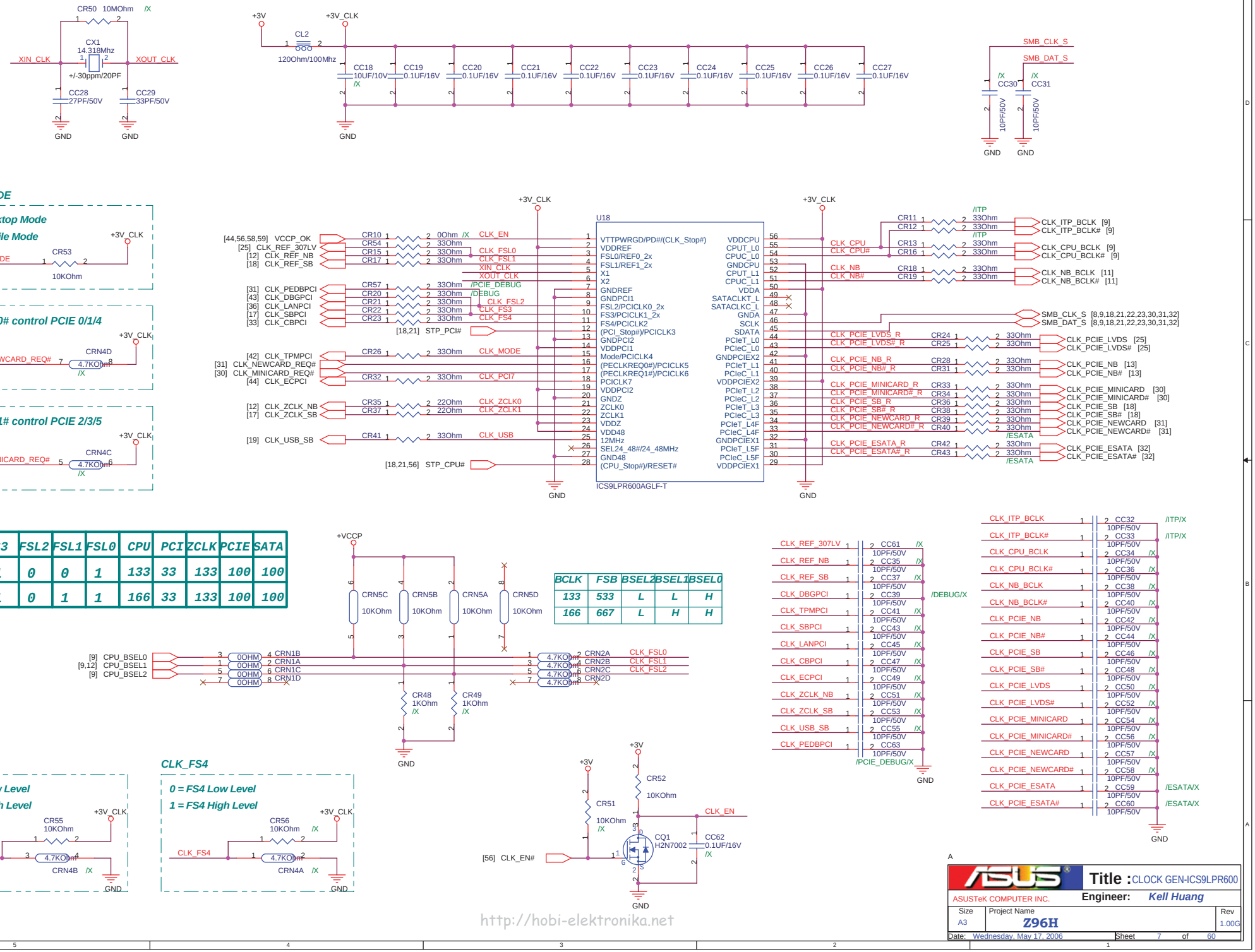
Engineer: Kell Huang

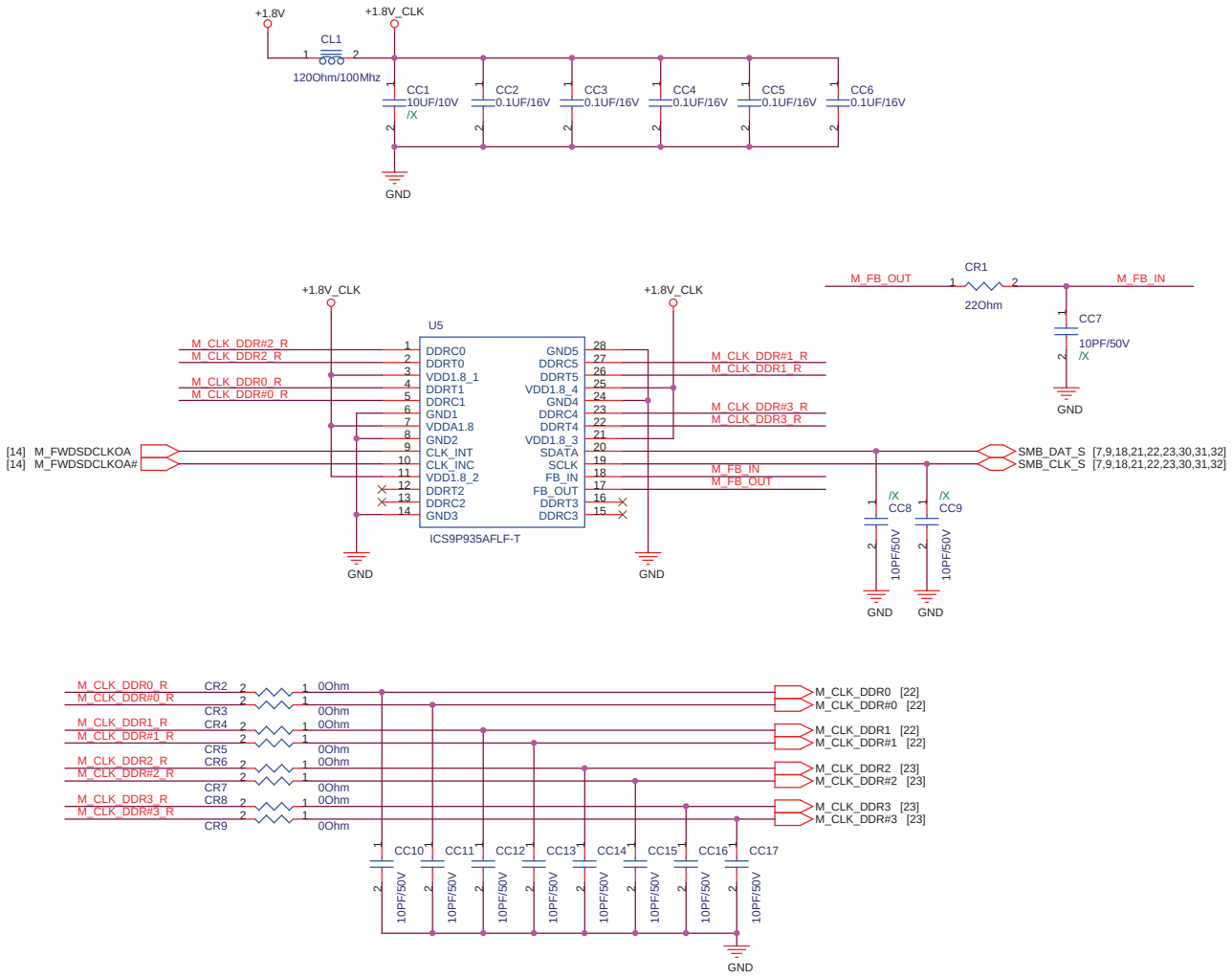
Size	Project Name	Rev
Custom	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 4 of 60

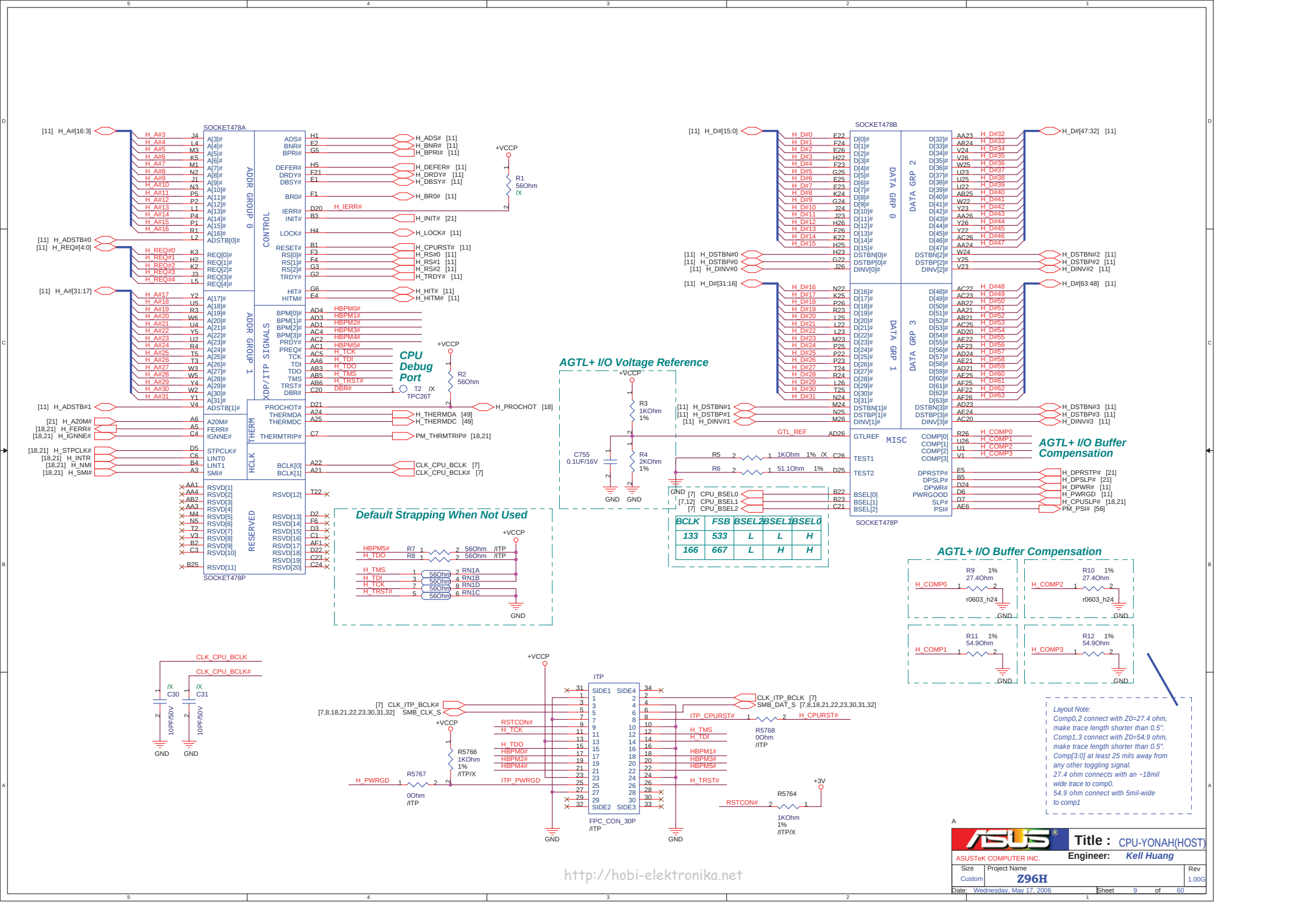
Title :	Blank
ASUSTeK COMPUTER INC	Engineer: Kell Huang
Size: A3	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 5 of 60

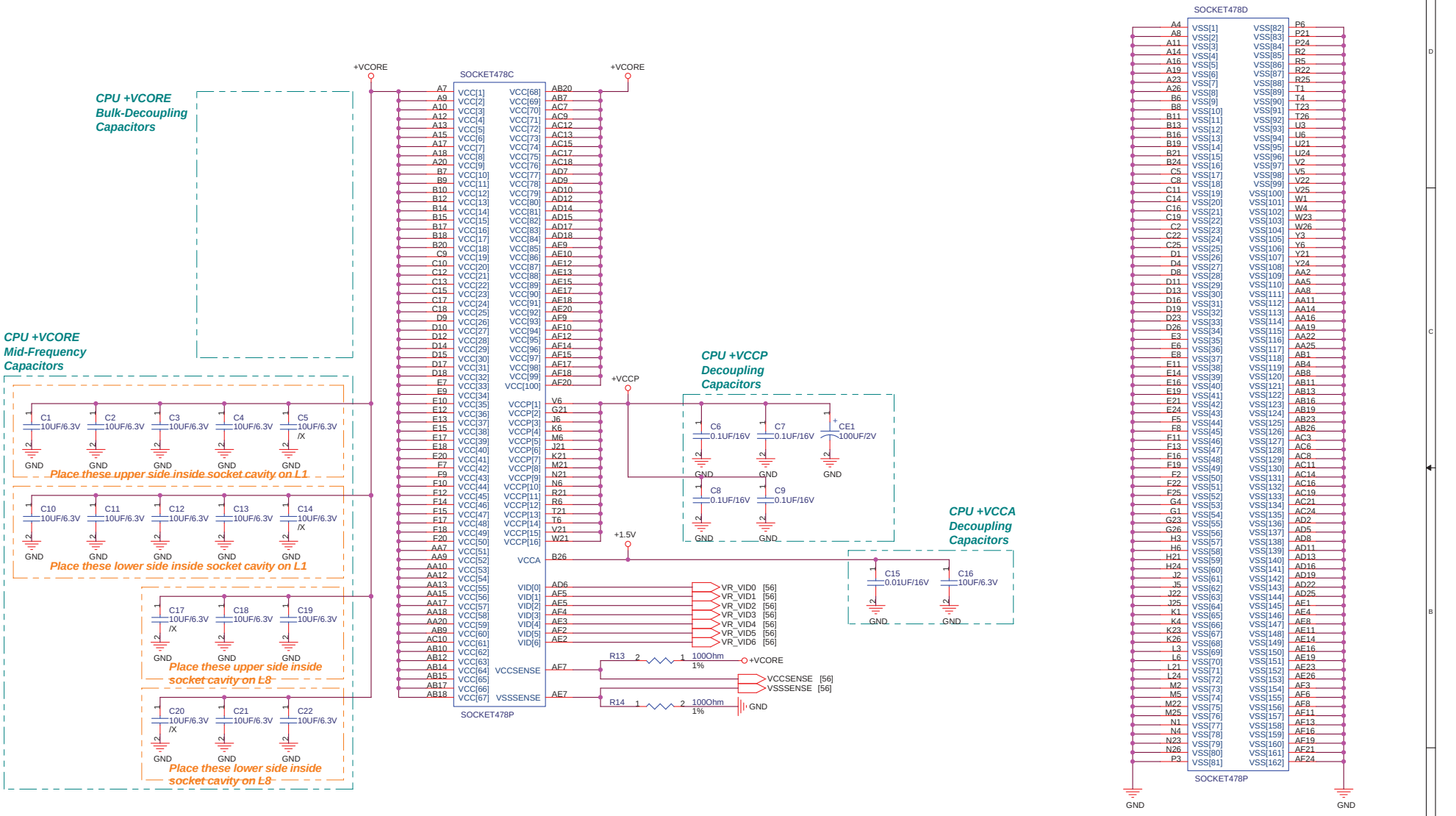
ASUSTeK COMPUTER INC	Title : Blank		
	Engineer: Kell Huang		
Size: A3	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 6 of 60		


CR50 10MOhm /X
CX1
14.318Mhz
+/-30ppm/20PF
XIN_CLK
XOUT_CLK
CC28 27PF/50V
CC29 33PF/50V
GND
+3V
+3V_CLK
CL2
120Ohm/100Mhz
CC18 10UF/10V /X
CC19 0.1UF/16V
CC20 0.1UF/16V
CC21 0.1UF/16V
CC22 0.1UF/16V
CC23 0.1UF/16V
CC24 0.1UF/16V
CC25 0.1UF/16V
CC26 0.1UF/16V
CC27 0.1UF/16V
SMB_CLK_S
SMB_DAT_S
CC30 10PF/50V
CC31 10PF/50V
CLK_MODE
0 = Desktop Mode
1 = Mobile Mode
CR53 10KOhm
PEREQ0# control PCIE 0/1/4
CLK_NEWCARD_REQ#
CRN4D 4.7KOhm /X
PEREQ1# control PCIE 2/3/5
CLK_MINICARD_REQ#
CRN4C 4.7KOhm /X
U18
ICS9LPR600AGLF-T
VTTPWRGD/PD#/(CLK_Stop#)
VDDREF
FSL0/REF0_2x
FSL1/REF1_2x
X1
X2
GNDREF
GNDPCI1
FSL2/PCICLK0_2x
FS3/PCICLK1_2x
FS4/PCICLK2
(PCI_Stop#)/PCICLK3
GNDPCI2
VDDPCI1
Mode/PCICLK4
(PECLKREQ0#)/PCICLK5
(PECLKREQ1#)/PCICLK6
PCICLK7
VDDPCI2
GNDZ
ZCLK0
ZCLK1
VDDZ
VDD48
12MHz
SEL24_48#/24_48MHz
GND48
(CPU_Stop#)/RESET#
VDDCPU
CPUT_L0
CPUC_L0
GNDCPU
CPUT_L1
CPUC_L1
VDDA
SATACLKT_L
SATACLKC_L
GNDA
SCLK
SDATA
PCIeT_L0
PCIeC_L0
GNDPCIEX2
PCIeT_L1
PCIeC_L1
VDDPCIEX2
PCIeT_L2
PCIeC_L2
PCIeT_L3
PCIeC_L3
PCIeT_L4F
PCIeC_L4F
GNDPCIEX1
PCIeT_L5F
PCIeC_L5F
VDDPCIEX1
[44,56,58,59] VCCP_OK
[25] CLK_REF_307LV
[12] CLK_REF_NB
[18] CLK_REF_SB
CR10 0Ohm /X CLK_EN
CR54 33Ohm
CR15 33Ohm CLK_FSL0
CR17 33Ohm CLK_FSL1
XIN_CLK
XOUT_CLK
[31] CLK_PEDBPCI
[43] CLK_DBGPCI
[36] CLK_LANPCI
[17] CLK_SBPCI
[33] CLK_CBPCI
CR57 33Ohm /PCIE_DEBUG
CR20 33Ohm /DEBUG
CR21 33Ohm CLK_FSL2
CR22 33Ohm CLK_FS3
CR23 33Ohm CLK_FS4
[18,21] STP_PCI#
[42] CLK_TPMPCI
[31] CLK_NEWCARD_REQ#
[30] CLK_MINICARD_REQ#
[44] CLK_ECPCI
CR26 33Ohm CLK_MODE
CR32 33Ohm CLK_PCI7
[12] CLK_ZCLK_NB
[17] CLK_ZCLK_SB
CR35 22Ohm CLK_ZCLK0
CR37 22Ohm CLK_ZCLK1
[19] CLK_USB_SB
CR41 33Ohm CLK_USB
[18,21,56] STP_CPU#
/ITP
CR11 33Ohm CLK_ITP_BCLK [9]
CR12 33Ohm CLK_ITP_BCLK# [9]
CLK_CPU
CLK_CPU#
CR13 33Ohm CLK_CPU_BCLK [9]
CR16 33Ohm CLK_CPU_BCLK# [9]
CLK_NB
CLK_NB#
CR18 33Ohm CLK_NB_BCLK [11]
CR19 33Ohm CLK_NB_BCLK# [11]
SMB_CLK_S [8,9,18,21,22,23,30,31,32]
SMB_DAT_S [8,9,18,21,22,23,30,31,32]
CLK_PCIE_LVDS_R
CLK_PCIE_LVDS#_R
CR24 33Ohm CLK_PCIE_LVDS [25]
CR25 33Ohm CLK_PCIE_LVDS# [25]
CLK_PCIE_NB_R
CLK_PCIE_NB#_R
CR28 33Ohm CLK_PCIE_NB [13]
CR31 33Ohm CLK_PCIE_NB# [13]
CLK_PCIE_MINICARD_R
CLK_PCIE_MINICARD#_R
CLK_PCIE_SB_R
CLK_PCIE_SB#_R
CLK_PCIE_NEWCARD_R
CLK_PCIE_NEWCARD#_R
CR33 33Ohm CLK_PCIE_MINICARD [30]
CR34 33Ohm CLK_PCIE_MINICARD# [30]
CR36 33Ohm CLK_PCIE_SB [18]
CR38 33Ohm CLK_PCIE_SB# [18]
CR39 33Ohm CLK_PCIE_NEWCARD [31]
CR40 33Ohm CLK_PCIE_NEWCARD# [31]
/ESATA
CLK_PCIE_ESATA_R
CLK_PCIE_ESATA#_R
CR42 33Ohm CLK_PCIE_ESATA [32]
CR43 33Ohm CLK_PCIE_ESATA# [32]
/ESATA
FS4 FS3 FSL2 FSL1 FSL0 CPU PCI ZCLK PCIE SATA
0 1 0 0 1 133 33 133 100 100
0 1 0 1 1 166 33 133 100 100
+VCCP
CRN5C 10KOhm
CRN5B 10KOhm
CRN5A 10KOhm
CRN5D 10KOhm
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
[9] CPU_BSEL0
[9,12] CPU_BSEL1
[9] CPU_BSEL2
0OHM CRN1B
0OHM CRN1A
0OHM CRN1C
0OHM CRN1D
4.7KOhm CRN2A CLK_FSL0
4.7KOhm CRN2B CLK_FSL1
4.7KOhm CRN2C CLK_FSL2
4.7KOhm CRN2D
CR48 1KOhm /X
CR49 1KOhm /X
CLK_REF_307LV CC61 /X
CLK_REF_NB CC35 /X
CLK_REF_SB CC37 /X
CLK_DBGPCI CC39 /DEBUG/X
CLK_TPMPCI CC41 /X
CLK_SBPCI CC43 /X
CLK_LANPCI CC45 /X
CLK_CBPCI CC47 /X
CLK_ECPCI CC49 /X
CLK_ZCLK_NB CC51 /X
CLK_ZCLK_SB CC53 /X
CLK_USB_SB CC55 /X
CLK_PEDBPCI CC63
/PCIE_DEBUG/X
CLK_ITP_BCLK CC32 /ITP/X
CLK_ITP_BCLK# CC33 /ITP/X
CLK_CPU_BCLK CC34 /X
CLK_CPU_BCLK# CC36 /X
CLK_NB_BCLK CC38 /X
CLK_NB_BCLK# CC40 /X
CLK_PCIE_NB CC42 /X
CLK_PCIE_NB# CC44 /X
CLK_PCIE_SB CC46 /X
CLK_PCIE_SB# CC48 /X
CLK_PCIE_LVDS CC50 /X
CLK_PCIE_LVDS# CC52 /X
CLK_PCIE_MINICARD CC54 /X
CLK_PCIE_MINICARD# CC56 /X
CLK_PCIE_NEWCARD CC57 /X
CLK_PCIE_NEWCARD# CC58 /X
CLK_PCIE_ESATA CC59 /ESATA/X
CLK_PCIE_ESATA# CC60 /ESATA/X
CLK_FS3
0 = FS3 Low Level
1 = FS3 High Level
CR55 10KOhm
CRN4B /X
CLK_FS4
0 = FS4 Low Level
1 = FS4 High Level
CR56 10KOhm /X
CRN4A /X
CR51 10KOhm /X
CR52 10KOhm
CLK_EN
[56] CLK_EN#
CQ1 H2N7002
CC62 0.1UF/16V /X
Title : CLOCK GEN-ICS9LPR600
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 7 of 60
http://hobi-elektronika.net



ASUSTeK COMPUTER INC.	Title : CLOCK BUF-ICS9P935	
	Engineer: Kell Huang	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 8 of 60	

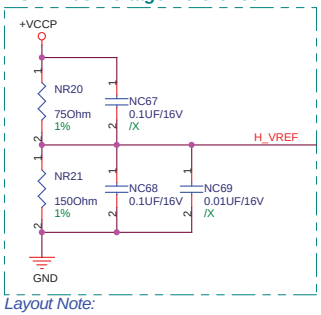

SOCKET478A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
SOCKET478P
CPU Debug Port
TPC26T
AGTL+ I/O Voltage Reference
Default Strapping When Not Used
SOCKET478B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
AGTL+ I/O Buffer Compensation
ITP
FPC_CON_30P
/ITP
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1
Title : CPU-YONAH(HOST)
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 9 of 60
http://hobi-elektronika.net



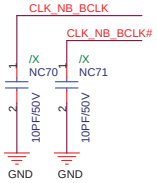
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

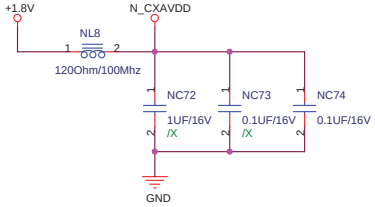
ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 10 of 60	

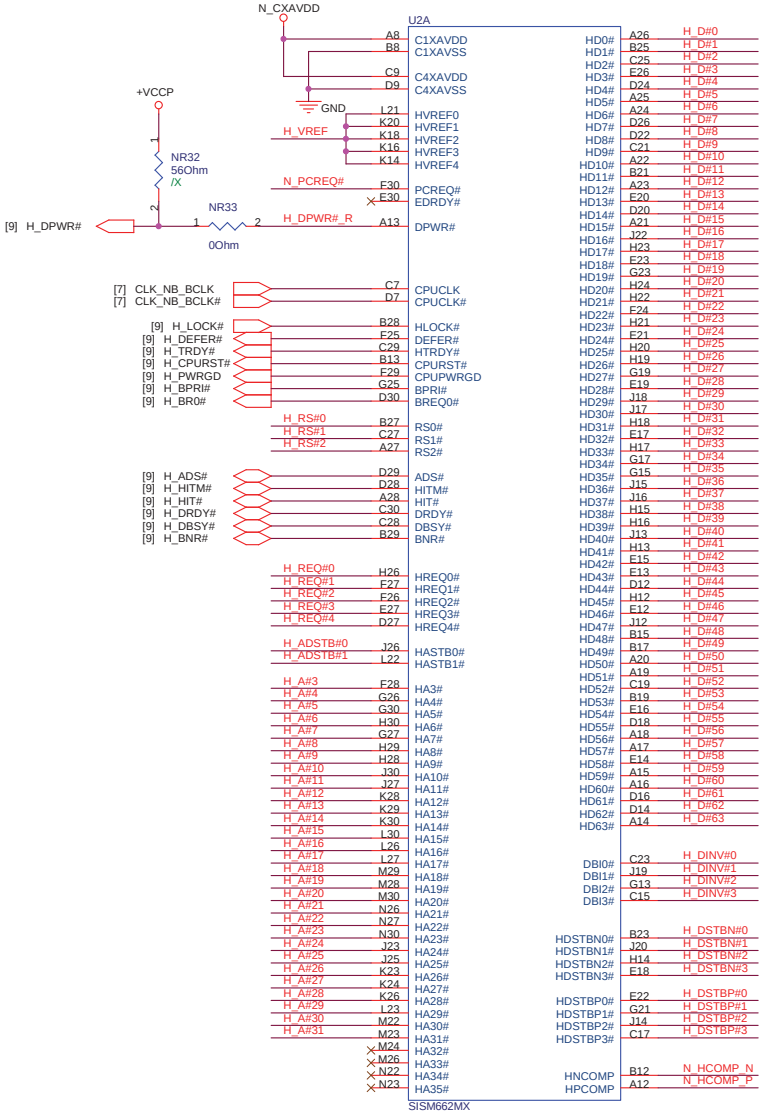
AGTL+ I/O Voltage Reference

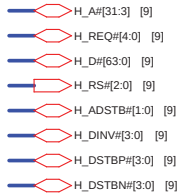


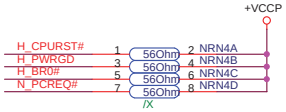
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

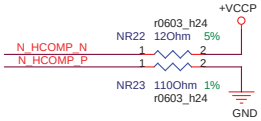








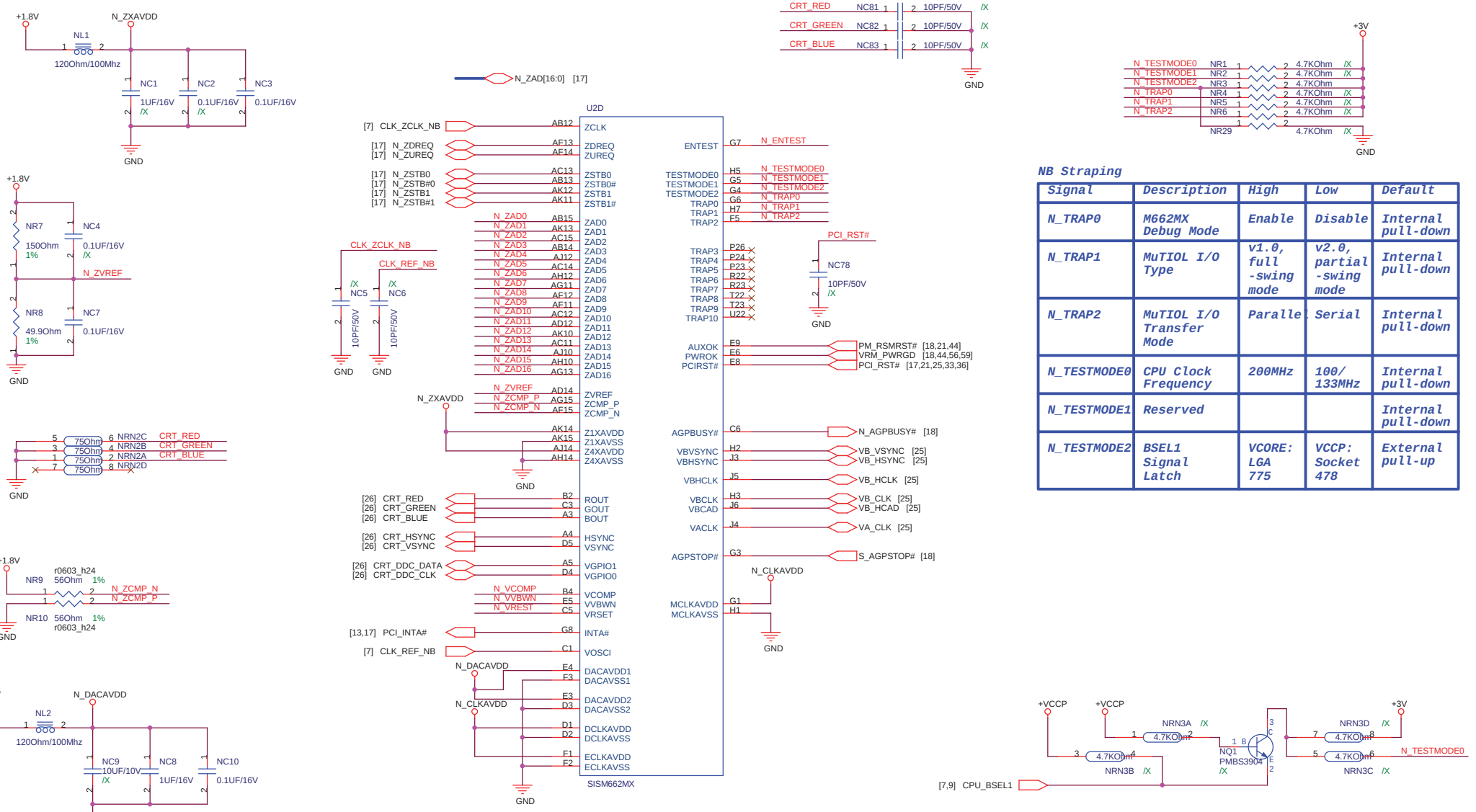




NR22 should be 1%

Trace should be 10 mil wide with 20 mil spacing

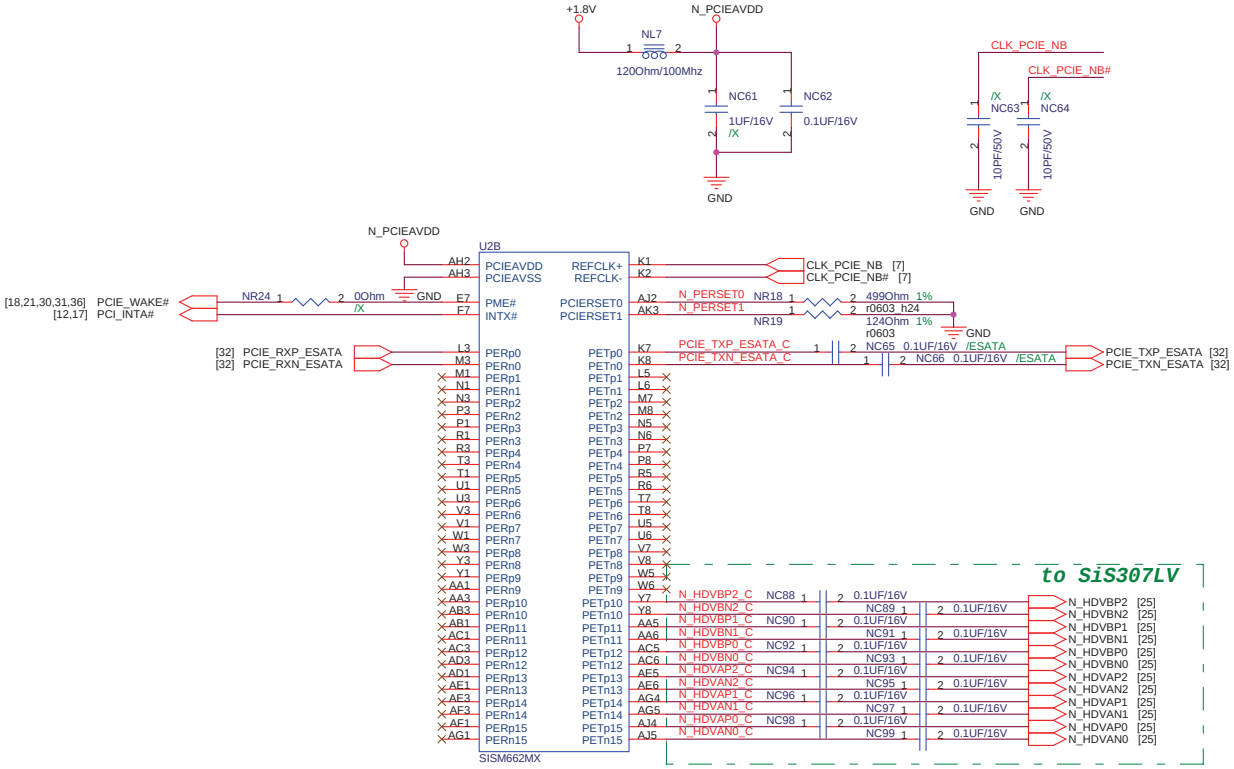
ASUSTeK COMPUTER INC.	Title : NB-M662MX(HOST)	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 11 of 60	



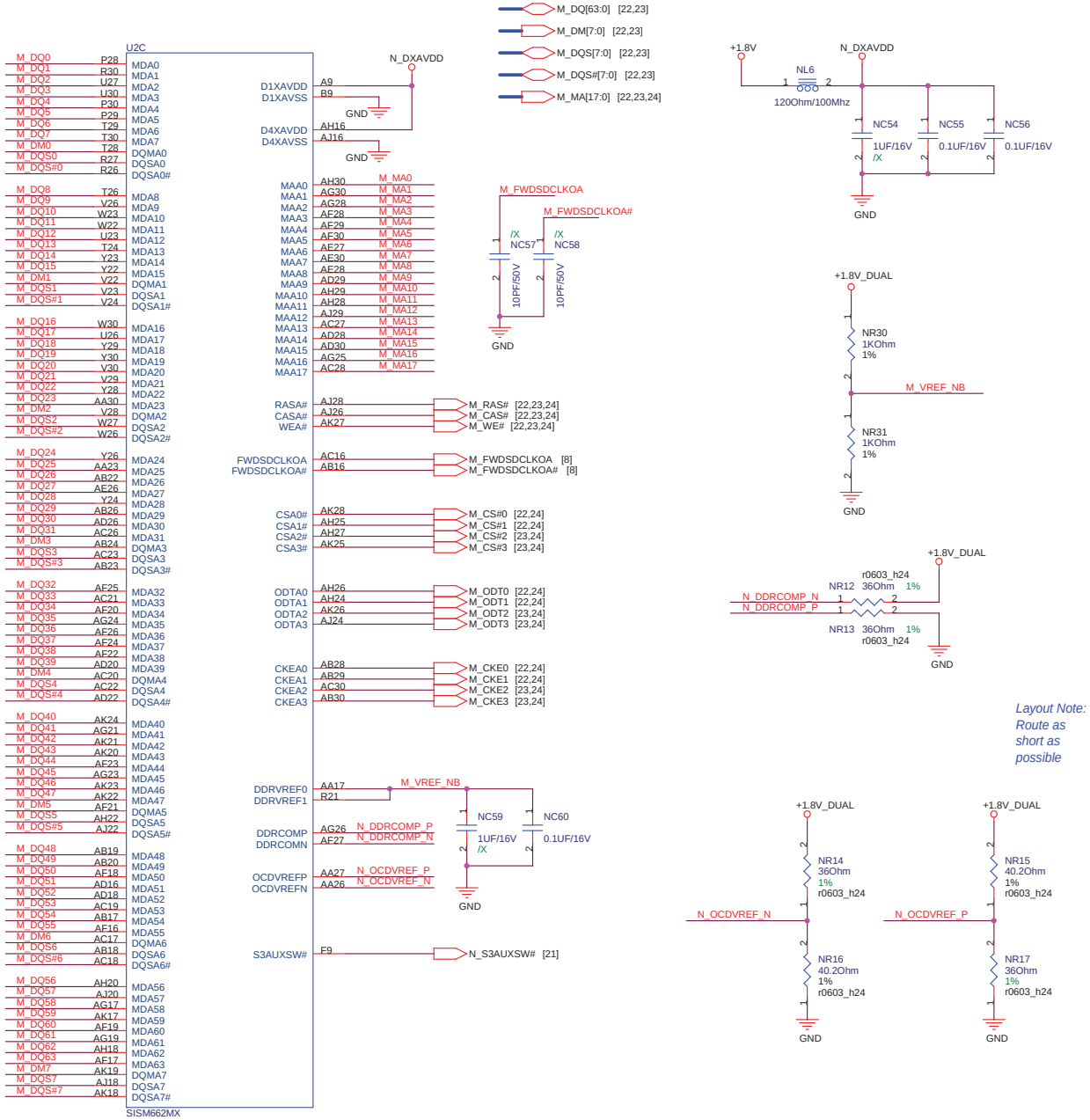
NB Straping

Signal	Description	High	Low	Default
N_TRAP0	M662MX Debug Mode	Enable	Disable	Internal pull-down
N_TRAP1	MuTIOL I/O Type	v1.0, full -swing mode	v2.0, partial -swing mode	Internal pull-down
N_TRAP2	MuTIOL I/O Transfer Mode	Parallel	Serial	Internal pull-down
N_TESTMODE0	CPU Clock Frequency	200MHz	100/ 133MHz	Internal pull-down
N_TESTMODE1	Reserved			Internal pull-down
N_TESTMODE2	BSEL1 Signal Latch	VCORE: LGA 775	VCCP: Socket 478	External pull-up

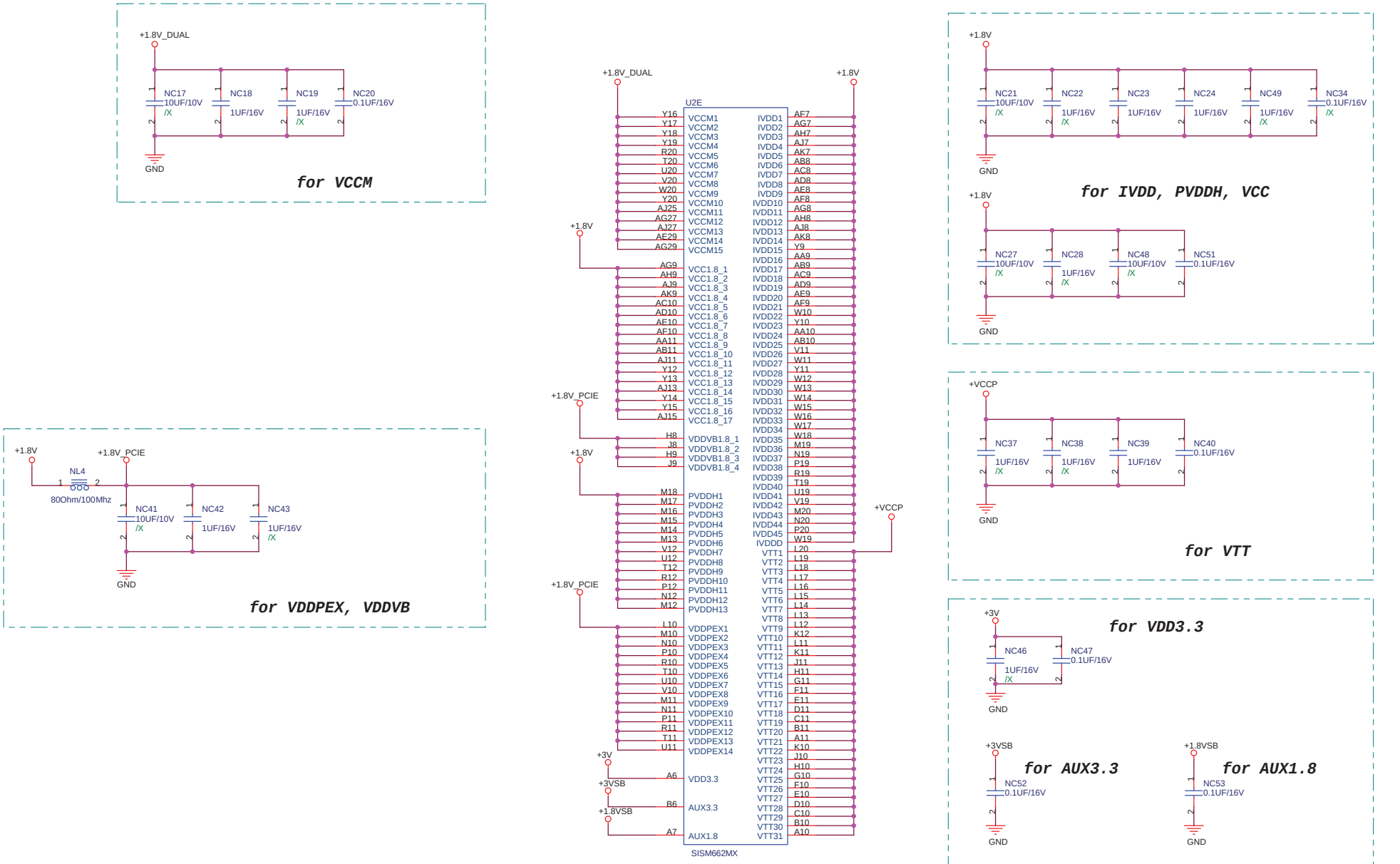
ASUSTeK COMPUTER INC.	Title : NB-M662MX(MuTIOL&VGA)		
	Engineer: Kell Huang		
Size: A3	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 12 of 60		



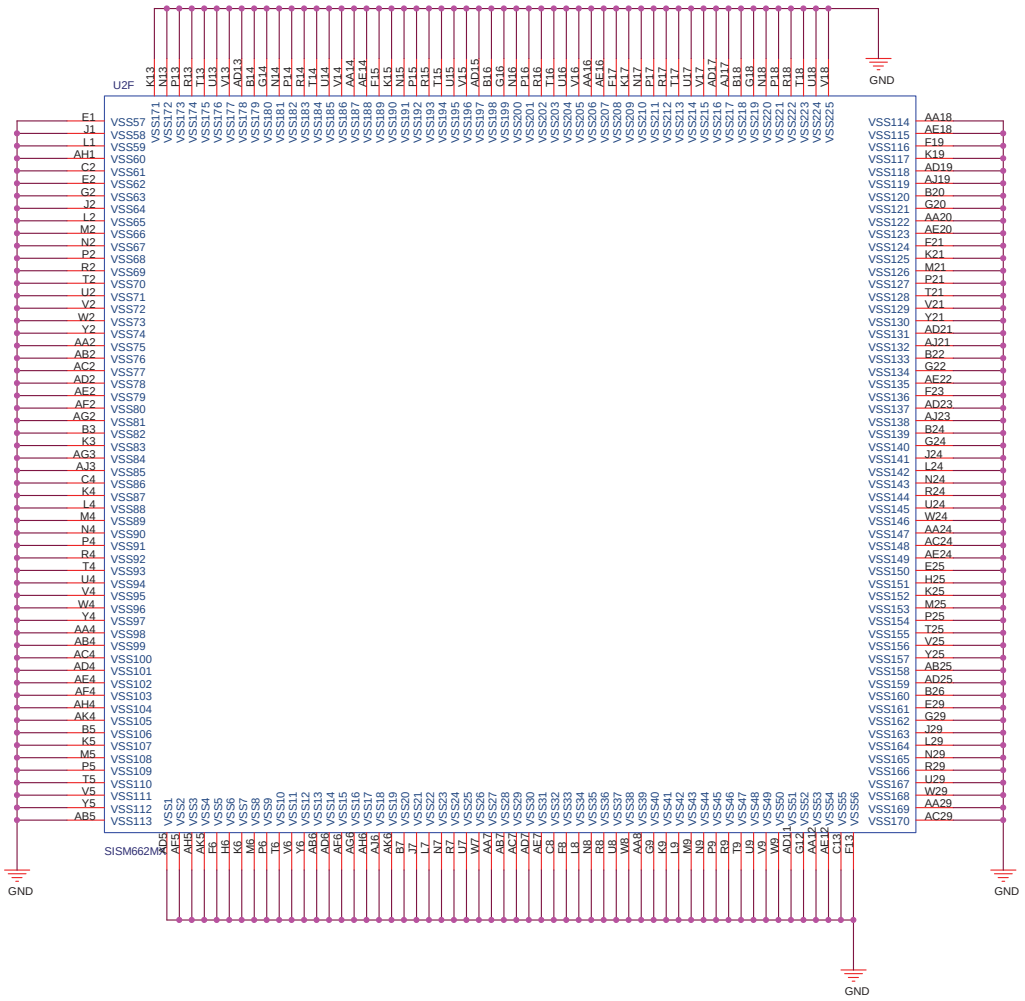
ASUSTeK COMPUTER INC.	Title : NB-M662MX(PCIE)		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 13 of 60		



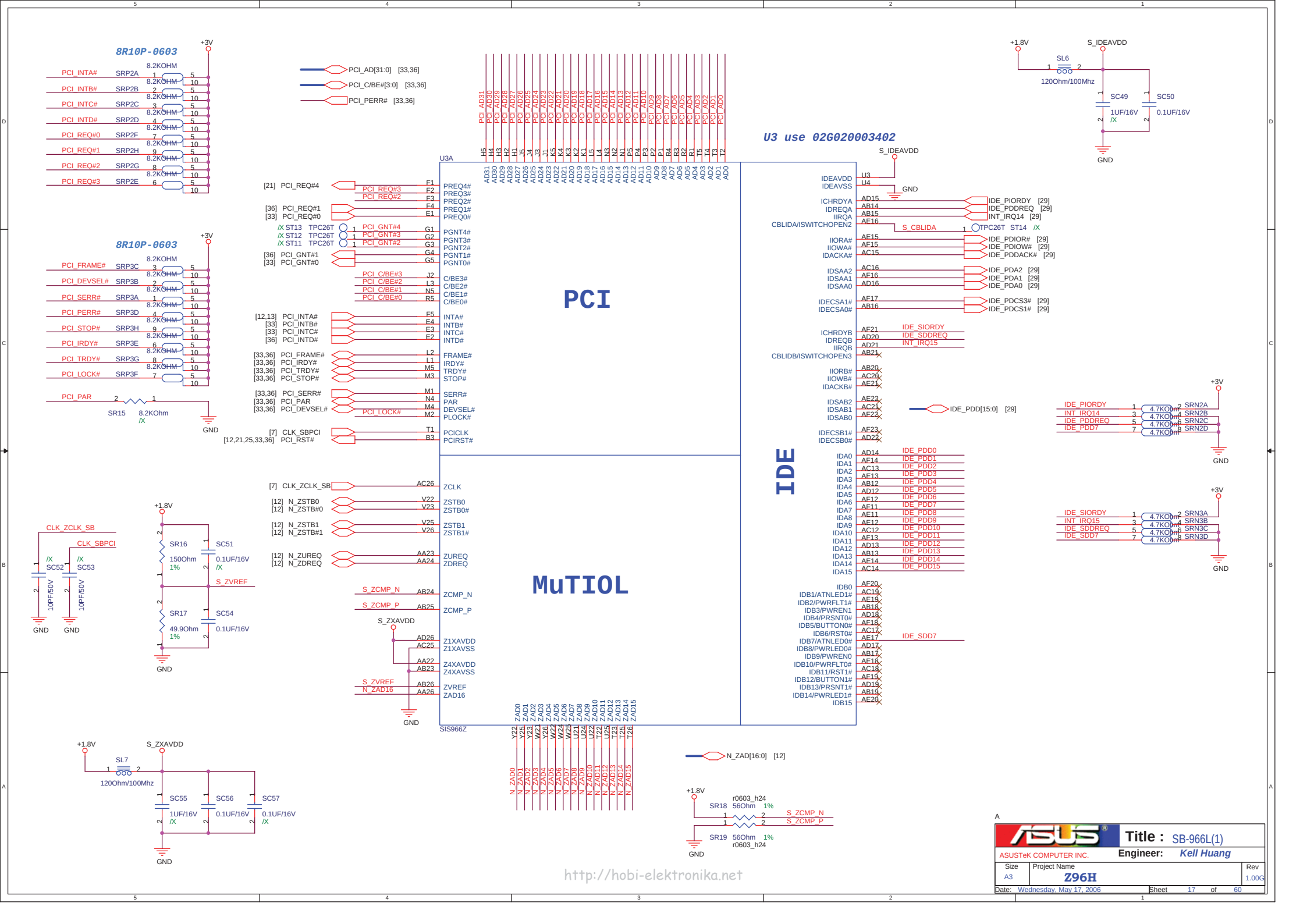
Title : NB-M662MX(DDR2)			
ASUSTeK COMPUTER INC.	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 14 of 60		



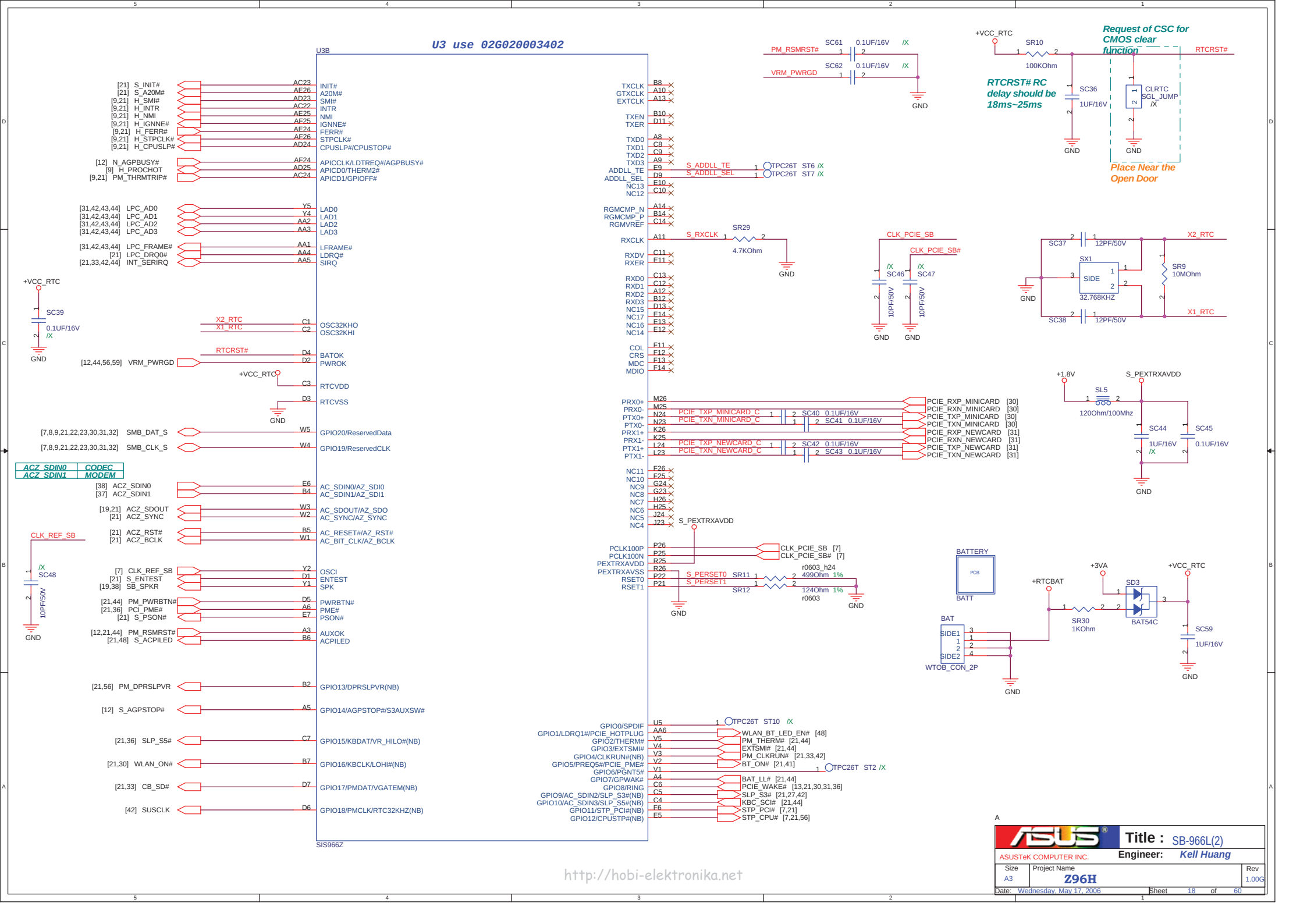
ASUSTeK COMPUTER INC.	Title : NB-M662MX(PWR)	
	Engineer: Kell Huang	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 15 of 60	

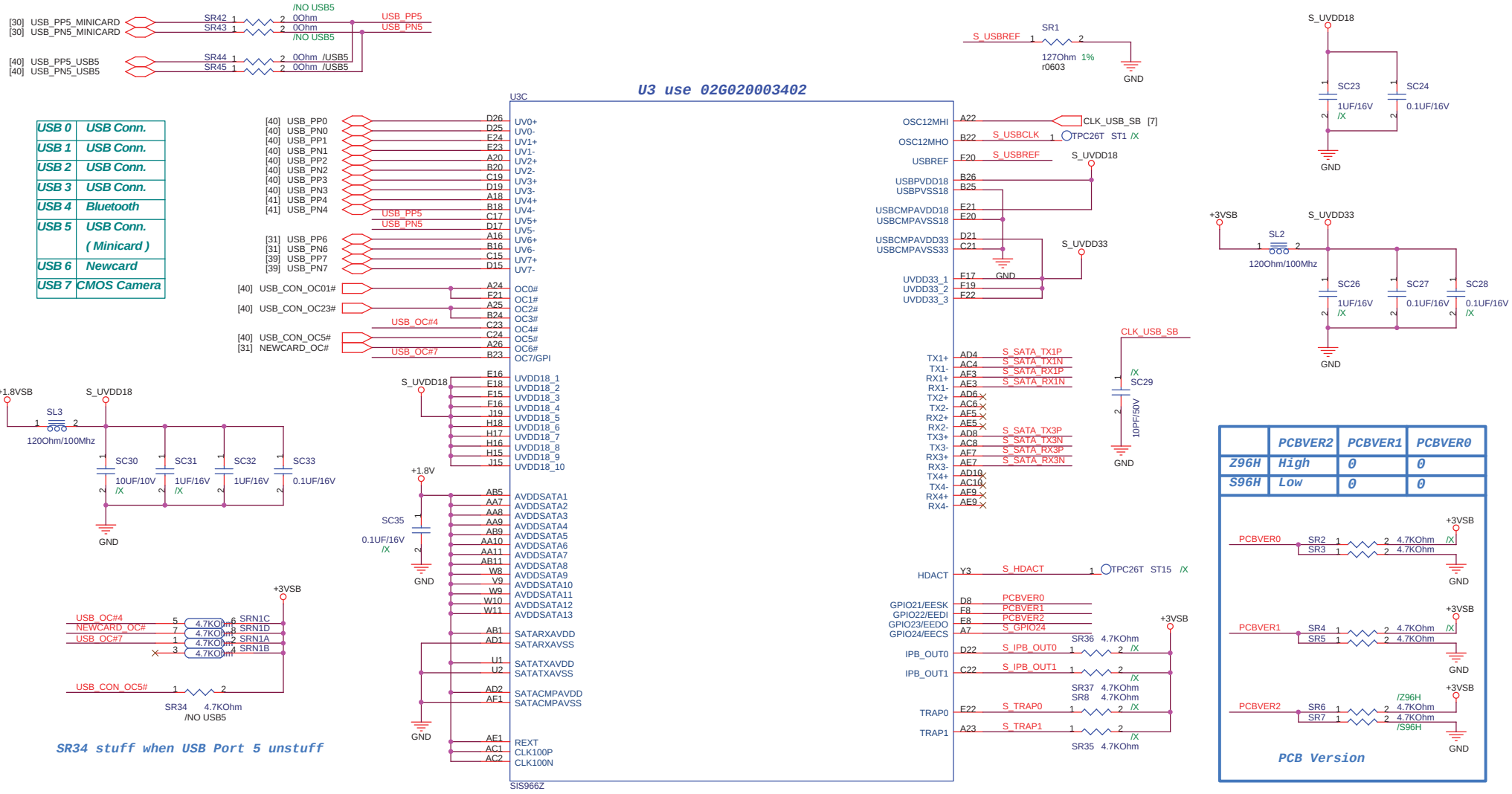


ASUSTeK COMPUTER INC.	Title : NB-M662MX(GND)		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 16 of 60		



Title :	SB-966L(1)
ASUSTeK COMPUTER INC.	Engineer: Kell Huang
Size: A3	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 17 of 60





SB Straping

Signal	Description	High	Low	Default
S_TRAP0	MuTIOL Operation Frequency	66MHz	133MHz	Internal pull-down
S_TRAP1	Reserved			Internal pull-down
S_IPB_OUT0	MuTIOL Clock PLL	Disable	Enable	Internal pull-down
S_IPB_OUT1	MuTIOL Version	v1.0	v2.0	Internal pull-down
SB_SPKR	First Flash Memory Cycle Type	Firmware Memory Type	LPC Memory Type	Internal pull-down
ACZ_SDOUT	Trap From	PCI AD	ROM	Internal pull-down
USB_OC#4	SB Debug Mode	Disable	Enable	External pull-up

	PCBVER2	PCBVER1	PCBVER0
Z96H	High	0	0
S96H	Low	0	0

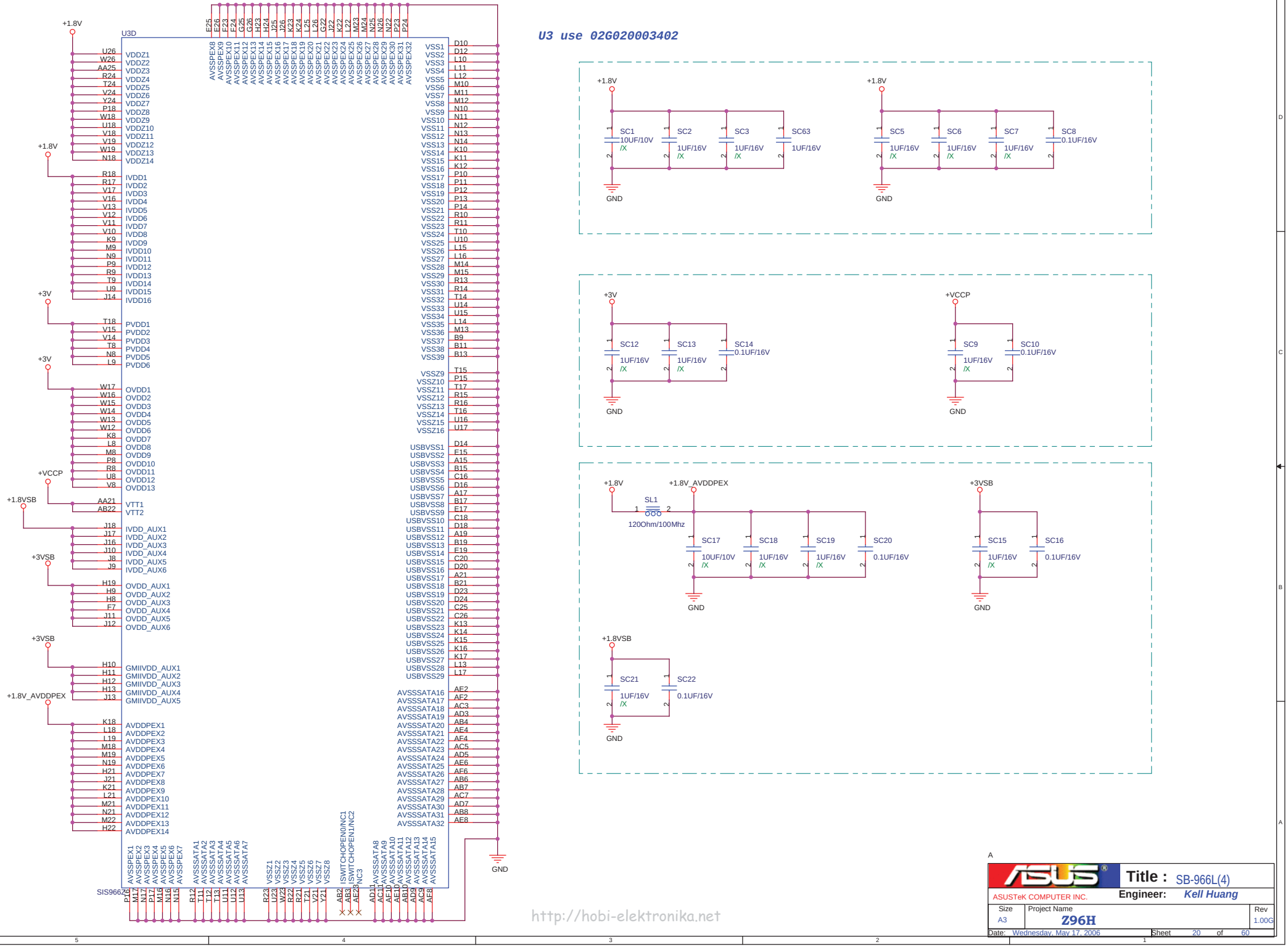
ASUSTeK COMPUTER INC

Title : SB-966L(3)

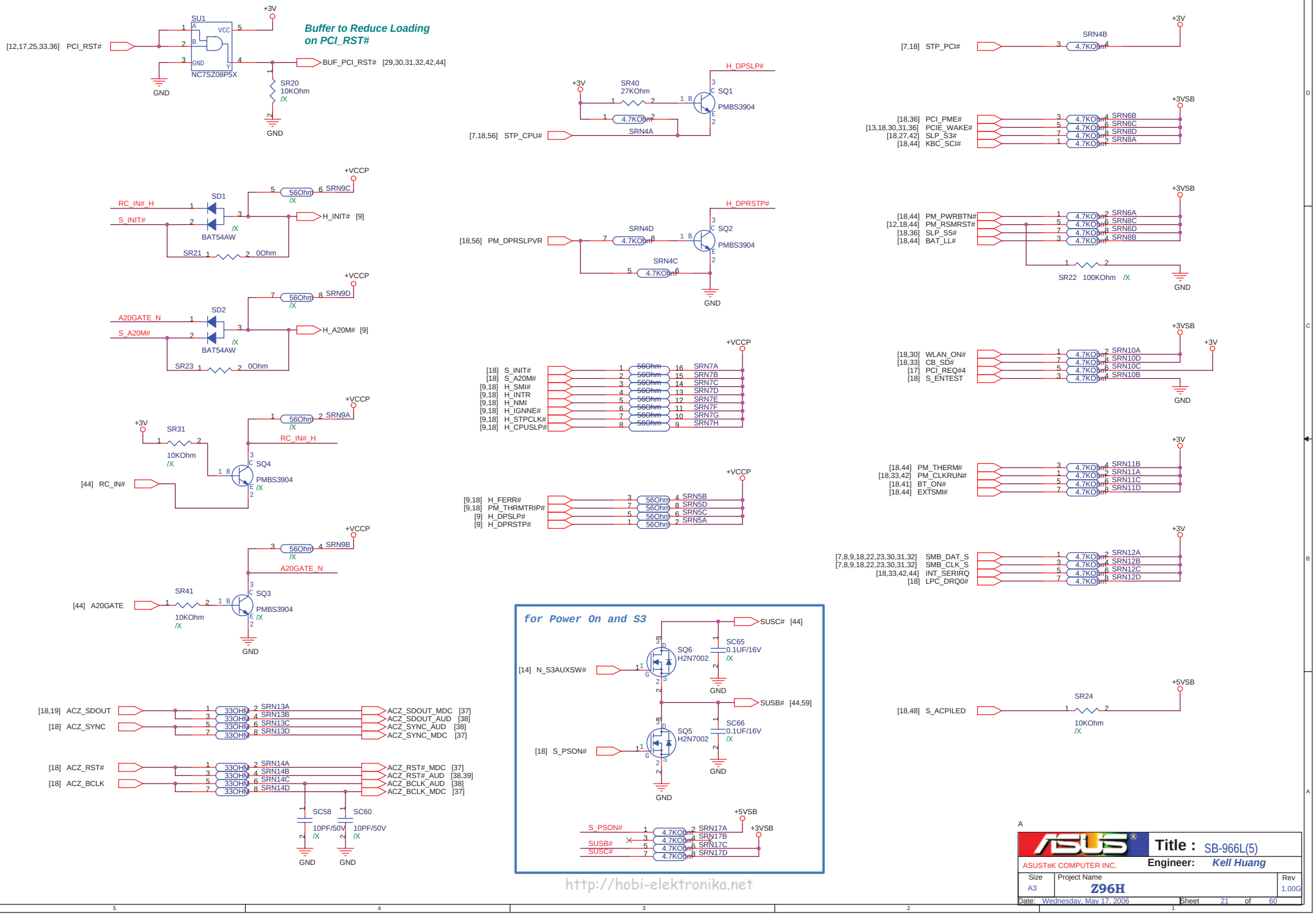
Engineer: Kell Huang

Size	Project Name	Rev
A3	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 19 of 60

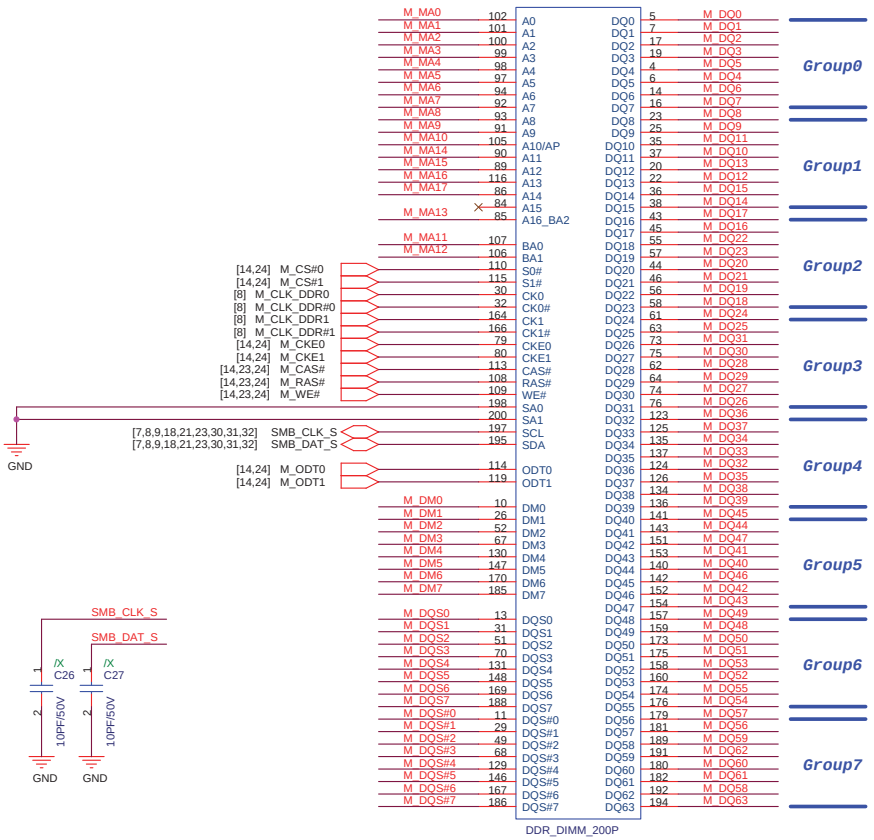


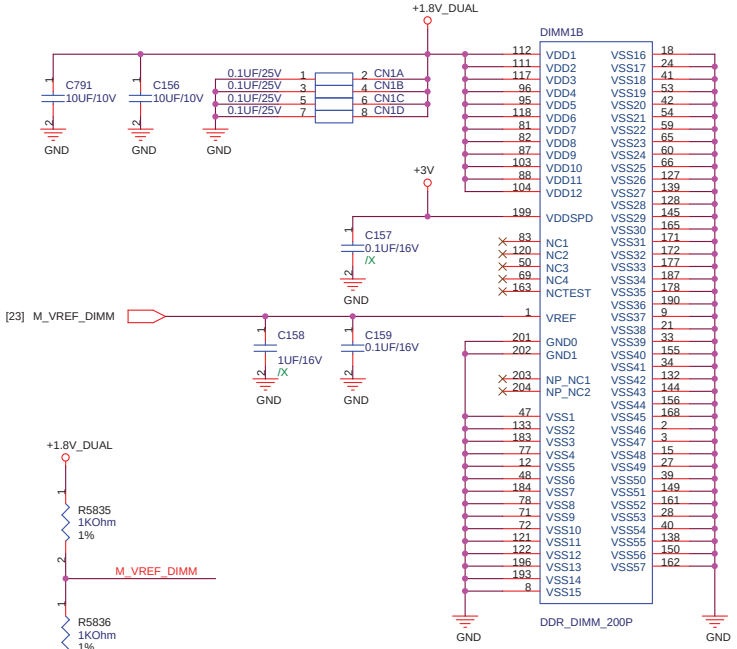
Title :	SB-966L(4)	
ASUSTeK COMPUTER INC.	Engineer:	Kell Huang
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 20 of 60	


Buffer to Reduce Loading on PCI_RST#
[12,17,25,33,36] PCI_RST#
SU1
NC7SZ08P5X
BUF_PCI_RST# [29,30,31,32,42,44]
SR20 10KOhm /X
GND
+3V
H_DPSLP#
SR40 27KOhm
SQ1
PMBS3904
SRN4A
[7,18,56] STP_CPU#
[7,18] STP_PCI#
SRN4B
+3VSB
[18,36] PCI_PME#
[13,18,30,31,36] PCIE_WAKE#
[18,27,42] SLP_S3#
[18,44] KBC_SCI#
SRN6B
SRN6C
SRN8D
SRN8A
+VCCP
SD1
RC_IN#_H
S_INIT#
BAT54AW
H_INIT# [9]
SR21 0Ohm
SRN9C
H_DPRSTP#
SRN4D
SQ2
[18,56] PM_DPRSLPVR
SRN4C
[18,44] PM_PWRBTN#
[12,18,44] PM_RSMRST#
[18,36] SLP_S5#
[18,44] BAT_LL#
SRN6A
SRN8C
SRN6D
SRN8B
SR22 100KOhm /X
SD2
A20GATE_N
S_A20M#
H_A20M# [9]
SR23 0Ohm
SRN9D
[18] S_INIT#
[18] S_A20M#
[9,18] H_SMI#
[9,18] H_INTR
[9,18] H_NMI
[9,18] H_IGNNE#
[9,18] H_STPCLK#
[9,18] H_CPUSLP#
SRN7A
SRN7B
SRN7C
SRN7D
SRN7E
SRN7F
SRN7G
SRN7H
[18,30] WLAN_ON#
[18,33] CB_SD#
[17] PCI_REQ#4
[18] S_ENTEST
SRN10A
SRN10D
SRN10C
SRN10B
SR31 10KOhm /X
SRN9A
[44] RC_IN#
[9,18] H_FERR#
[9,18] PM_THRMTRIP#
[9] H_DPSLP#
[9] H_DPRSTP#
SRN5B
SRN5D
SRN5C
SRN5A
[18,44] PM_THERM#
[18,33,42] PM_CLKRUN#
[18,41] BT_ON#
[18,44] EXTSMI#
SRN11B
SRN11A
SRN11C
SRN11D
SR41 10KOhm /X
SRN9B
A20GATE_N
[44] A20GATE
SQ3
[7,8,9,18,22,23,30,31,32] SMB_DAT_S
[7,8,9,18,22,23,30,31,32] SMB_CLK_S
[18,33,42,44] INT_SERIRQ
[18] LPC_DRQ0#
SRN12A
SRN12B
SRN12C
SRN12D
[18,19] ACZ_SDOUT
[18] ACZ_SYNC
33OHM
SRN13A
SRN13B
SRN13C
SRN13D
ACZ_SDOUT_MDC [37]
ACZ_SDOUT_AUD [38]
ACZ_SYNC_AUD [38]
ACZ_SYNC_MDC [37]
[18] ACZ_RST#
[18] ACZ_BCLK
SRN14A
SRN14B
SRN14C
SRN14D
ACZ_RST#_MDC [37]
ACZ_RST#_AUD [38,39]
ACZ_BCLK_AUD [38]
ACZ_BCLK_MDC [37]
SC58 10PF/50V /X
SC60 10PF/50V /X
[18,48] S_ACPILED
SR24 10KOhm /X
+5VSB
for Power On and S3
SUSC# [44]
SUSB# [44,59]
[14] N_S3AUXSW#
[18] S_PSON#
SQ6 H2N7002
SQ5 H2N7002
SC65 0.1UF/16V /X
SC66 0.1UF/16V /X
S_PSON#
SUSB#
SUSC#
SRN17A
SRN17B
SRN17C
SRN17D
http://hobi-elektronika.net
Title : SB-966L(5)
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 21 of 60

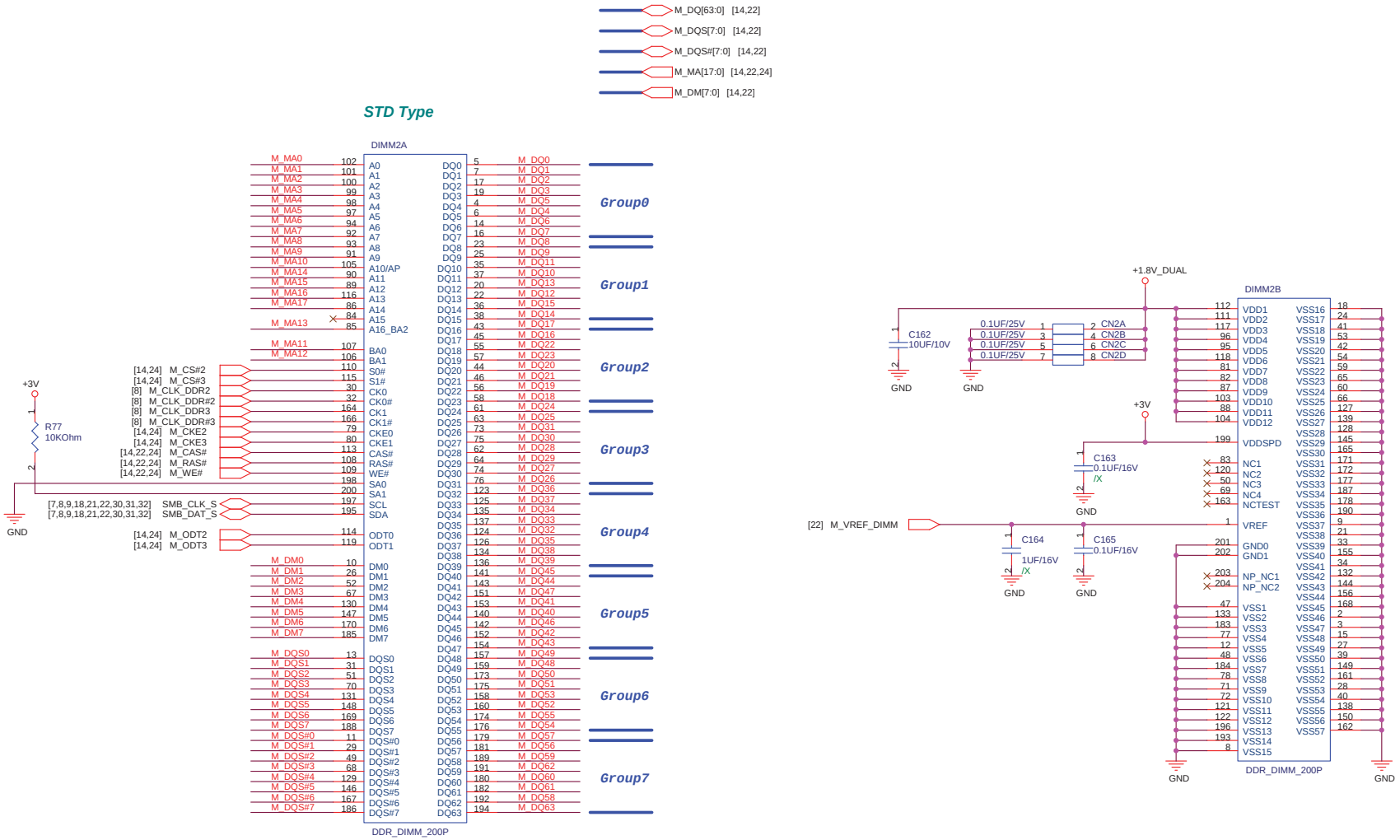
M_DQ[63:0] [14,23]
M_DQS[7:0] [14,23]
M_DQS#[7:0] [14,23]
M_MA[17:0] [14,23,24]
M_DM[7:0] [14,23]

REV Type



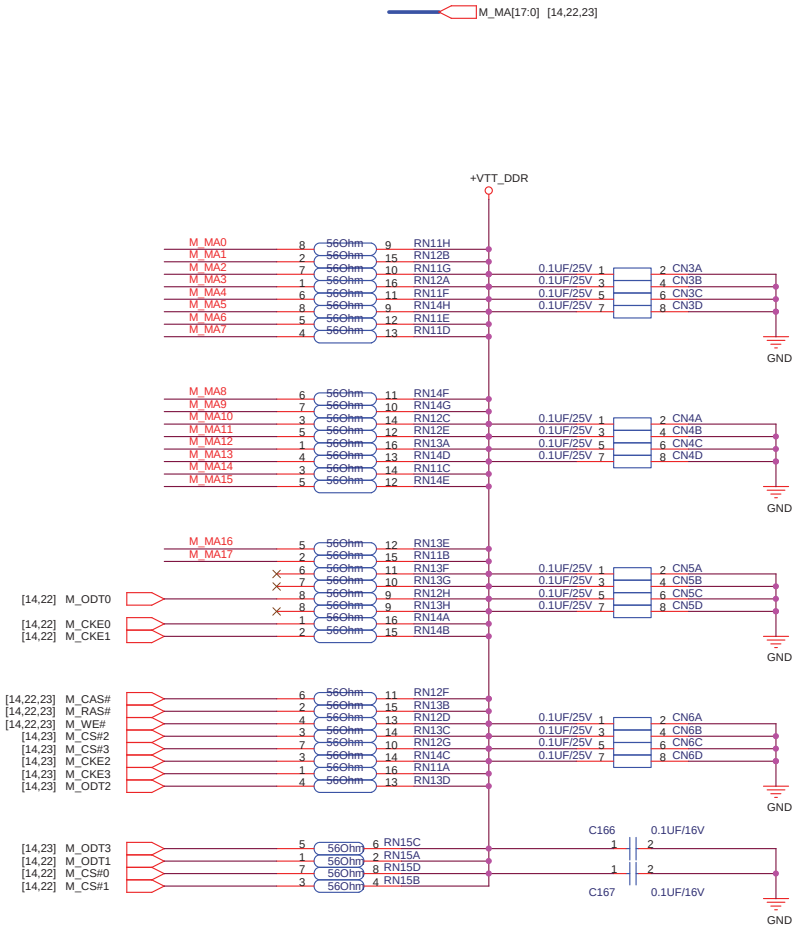


Title : DDR2 SO-DIMM1		
ASUSTeK COMPUTER INC.	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 22 of 60	

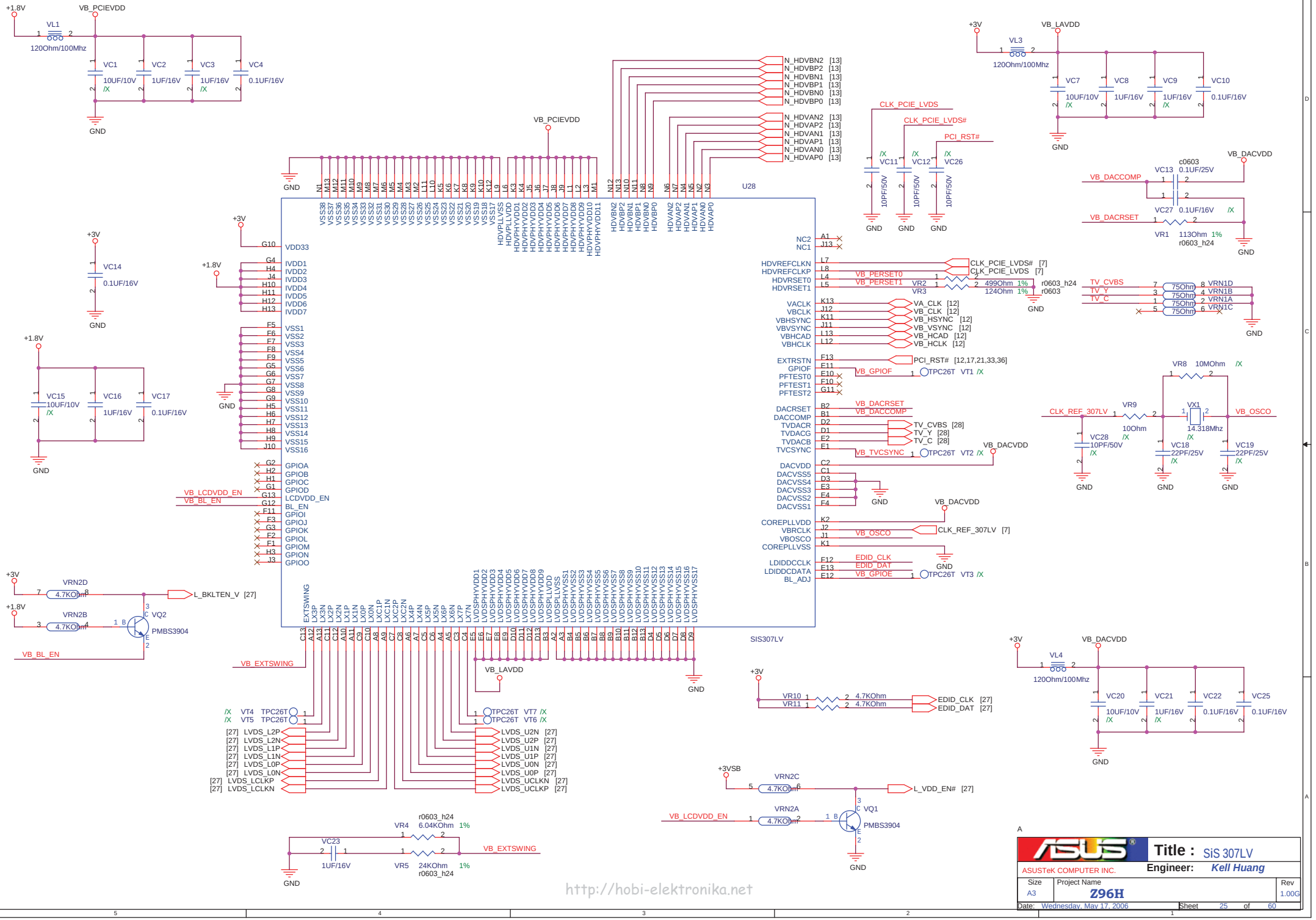


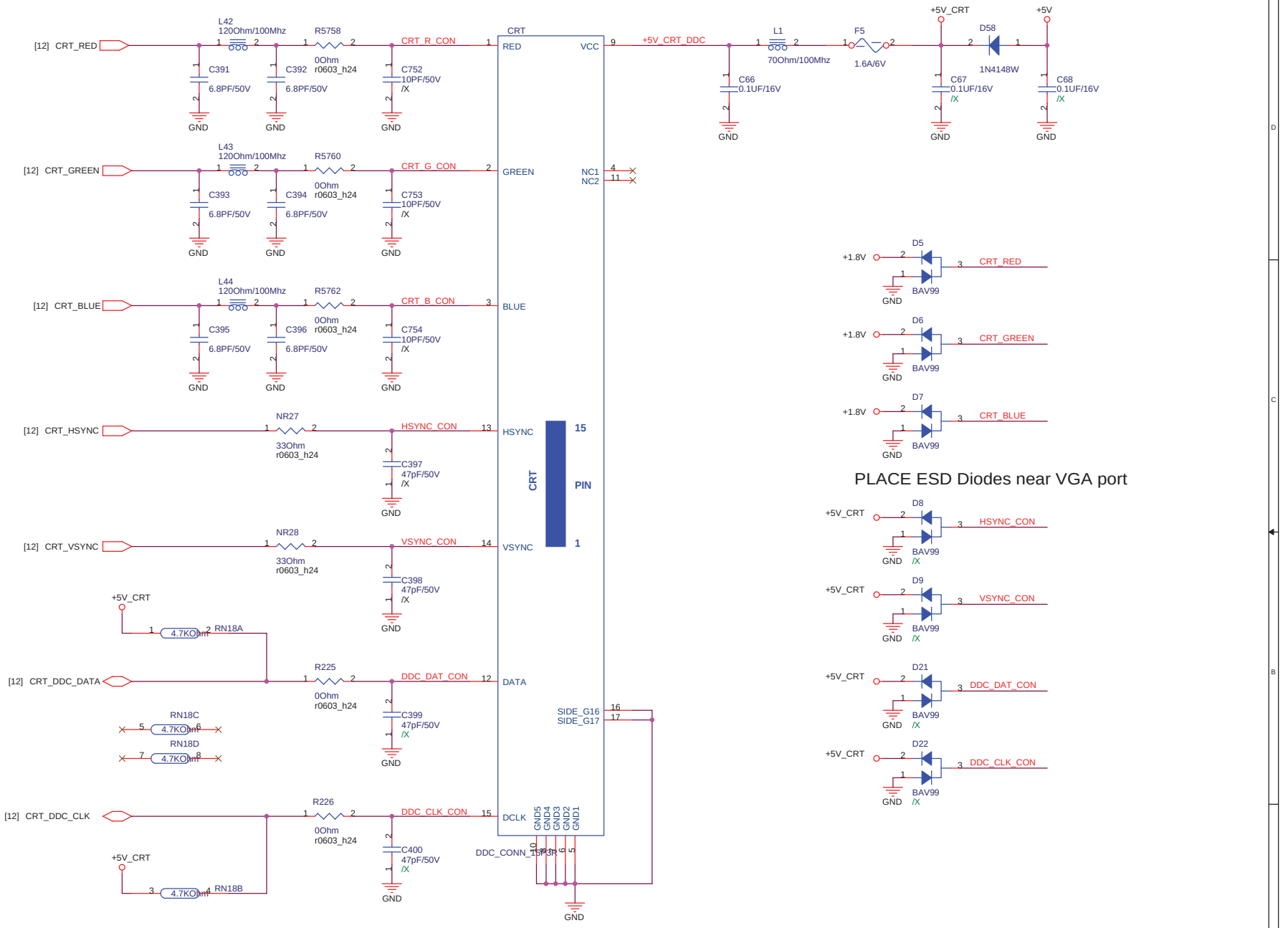
http://hobi-elektronika.net

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM2	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 23 of 60	



ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 24 of 60	

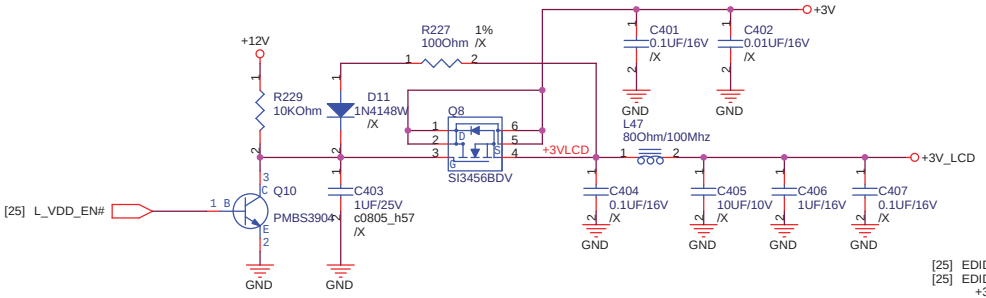

U28
SIS307LV
VB_PCIEVDD
VB_LAVDD
VB_DACVDD
VB_LCDVDD_EN
VB_BL_EN
VB_EXTSWING
VB_PERSET0
VB_PERSET1
VB_GPIOF
VB_DACRSET
VB_DACCOMP
VB_TVCSYNC
VB_OSCO
VB_GPIOE
EDID_CLK
EDID_DAT
CLK_PCIE_LVDS
CLK_PCIE_LVDS#
PCI_RST#
CLK_REF_307LV
L_BKLTEN_V [27]
L_VDD_EN# [27]
PMBS3904
http://hobi-elektronika.net
Title : SiS 307LV
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Project Name Z96H
Size A3
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 25 of 60



ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 26 of 60	

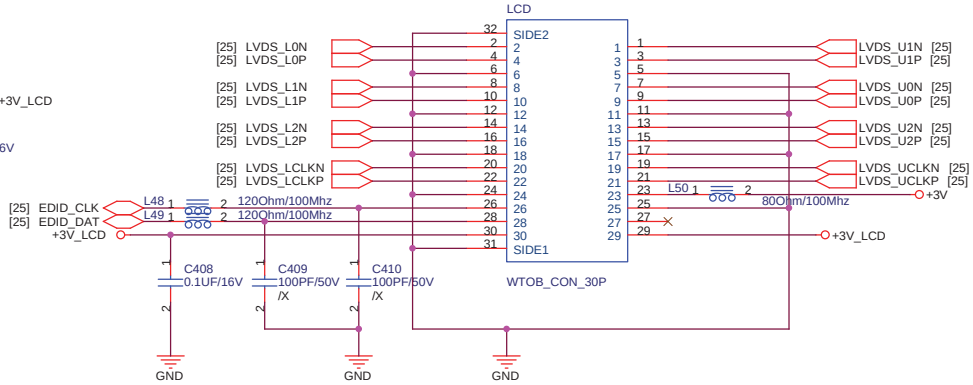
LCD Backlight Control

LCD Power



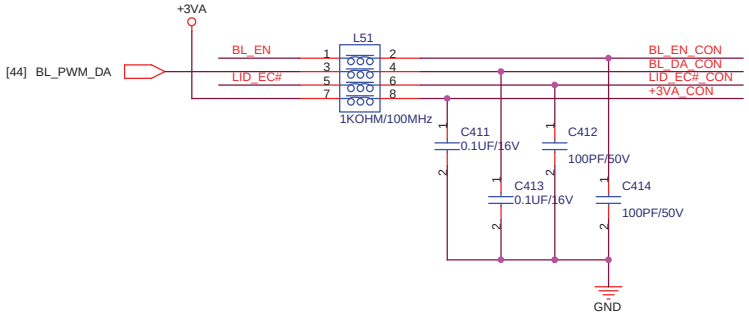
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

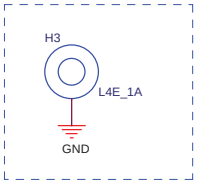
LCD LVDS Interface



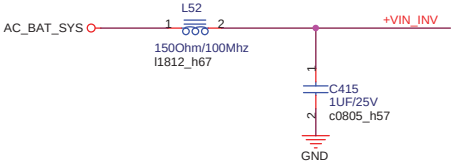
INVERTER Interface/Speaker CONN.

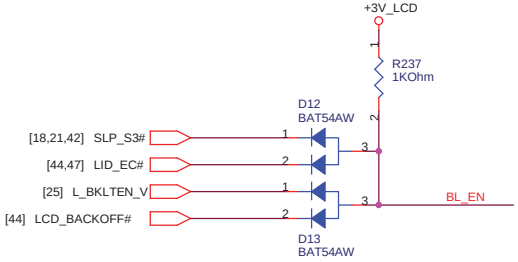
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

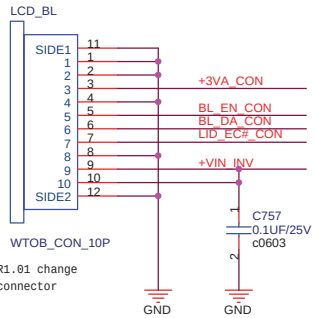




LCD NUT(3.0mm) *1



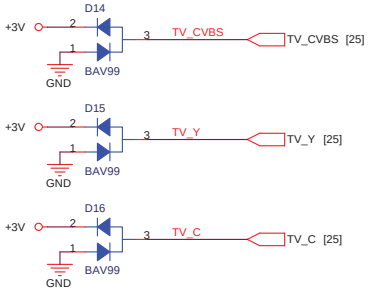




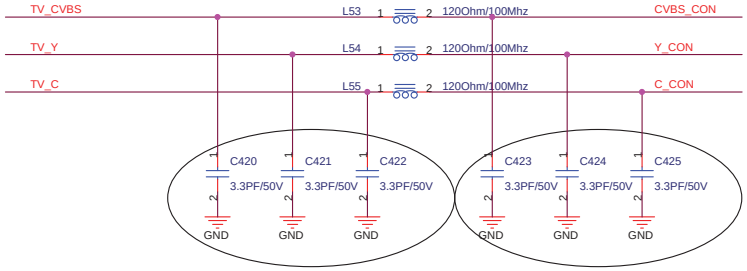
R1.01 change connector

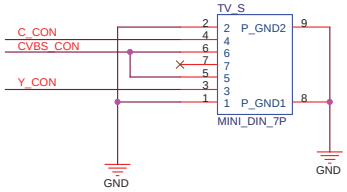
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 27 of 60	

TV OUT



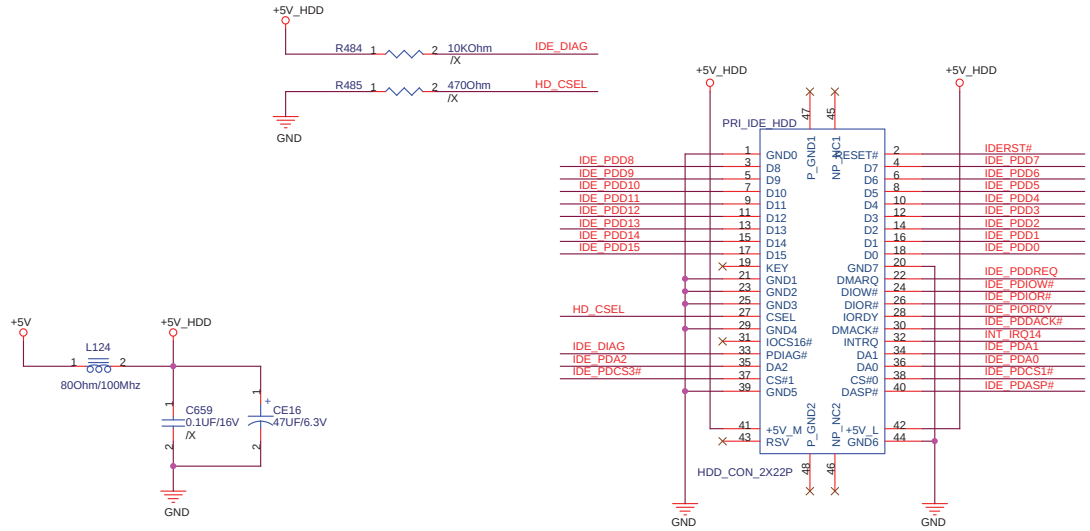
PLACE ESD Diodes near TV port





ASUSTeK COMPUTER INC	Title : TV OUT CONN	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 28 of 60	

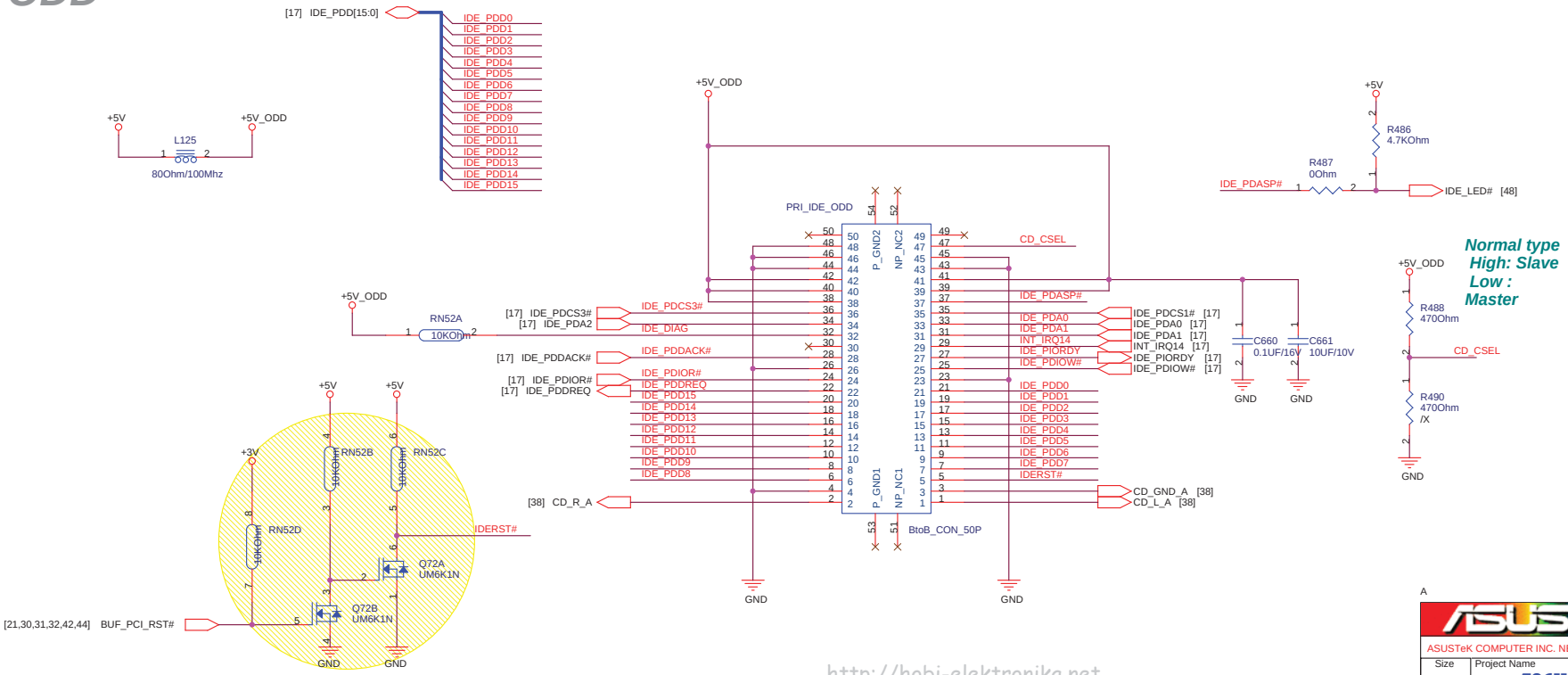
HD_CSEL : Pull-Down, HDD as Master



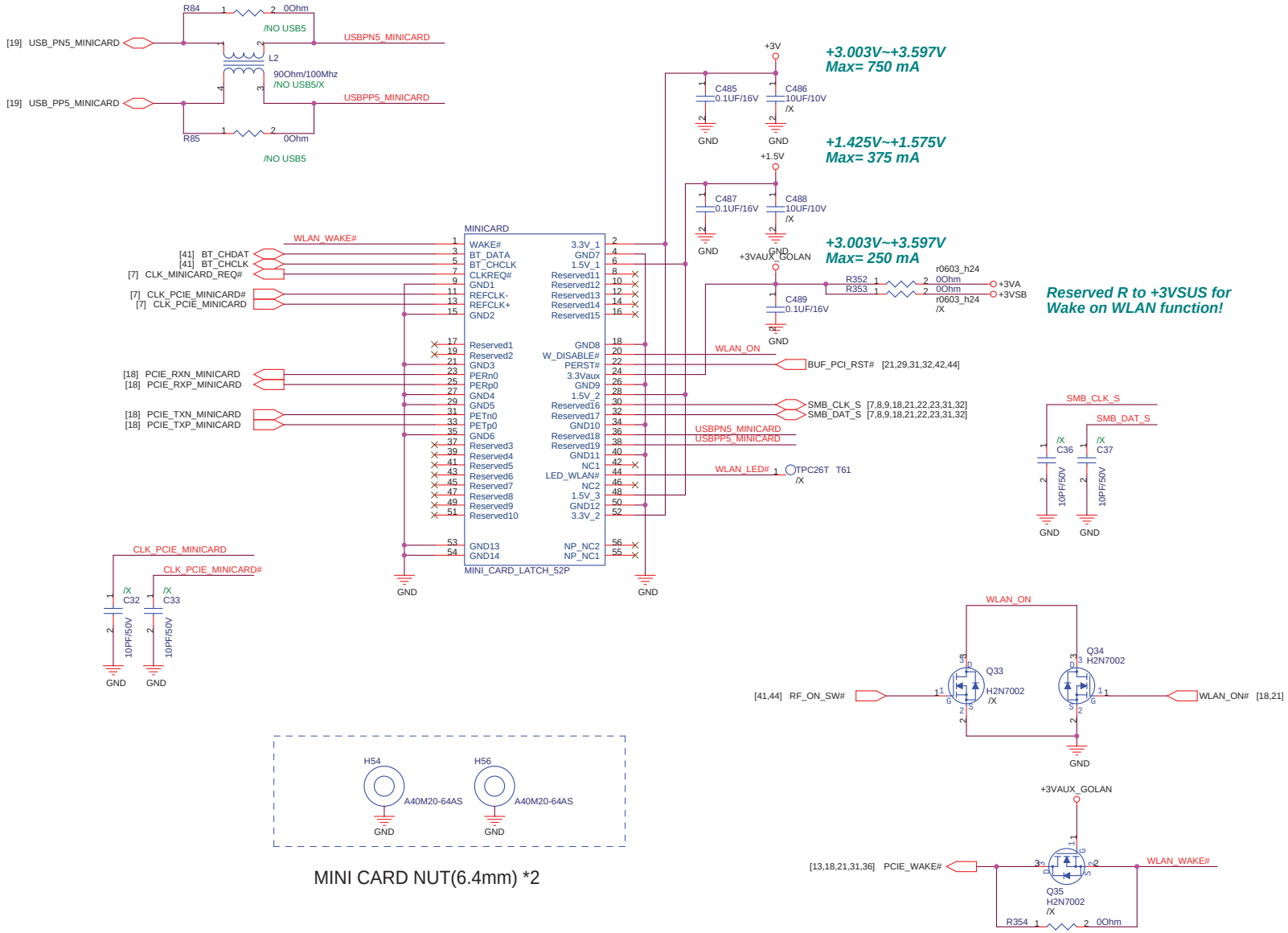
Remove SATA HDD

PATA HDD

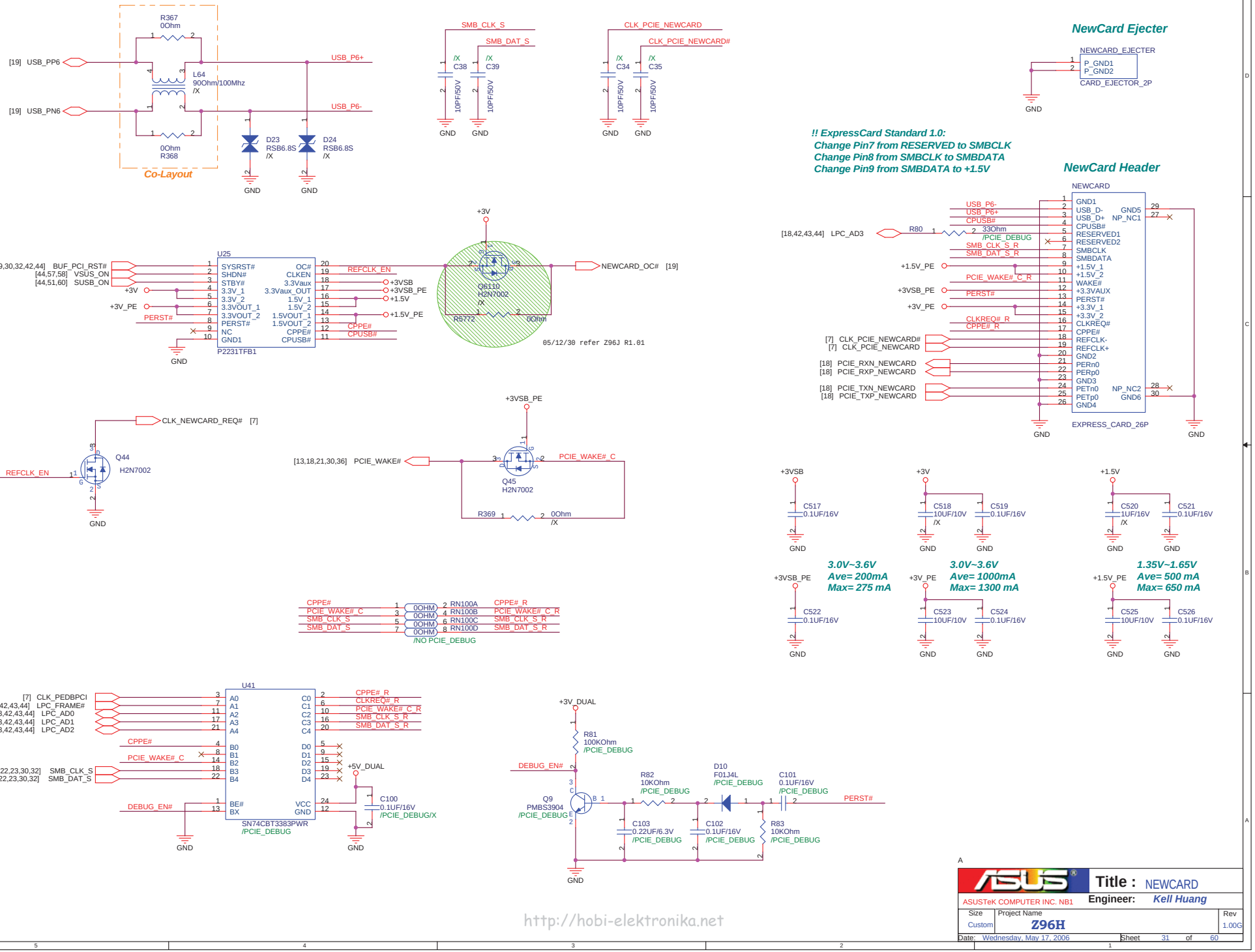
ODD

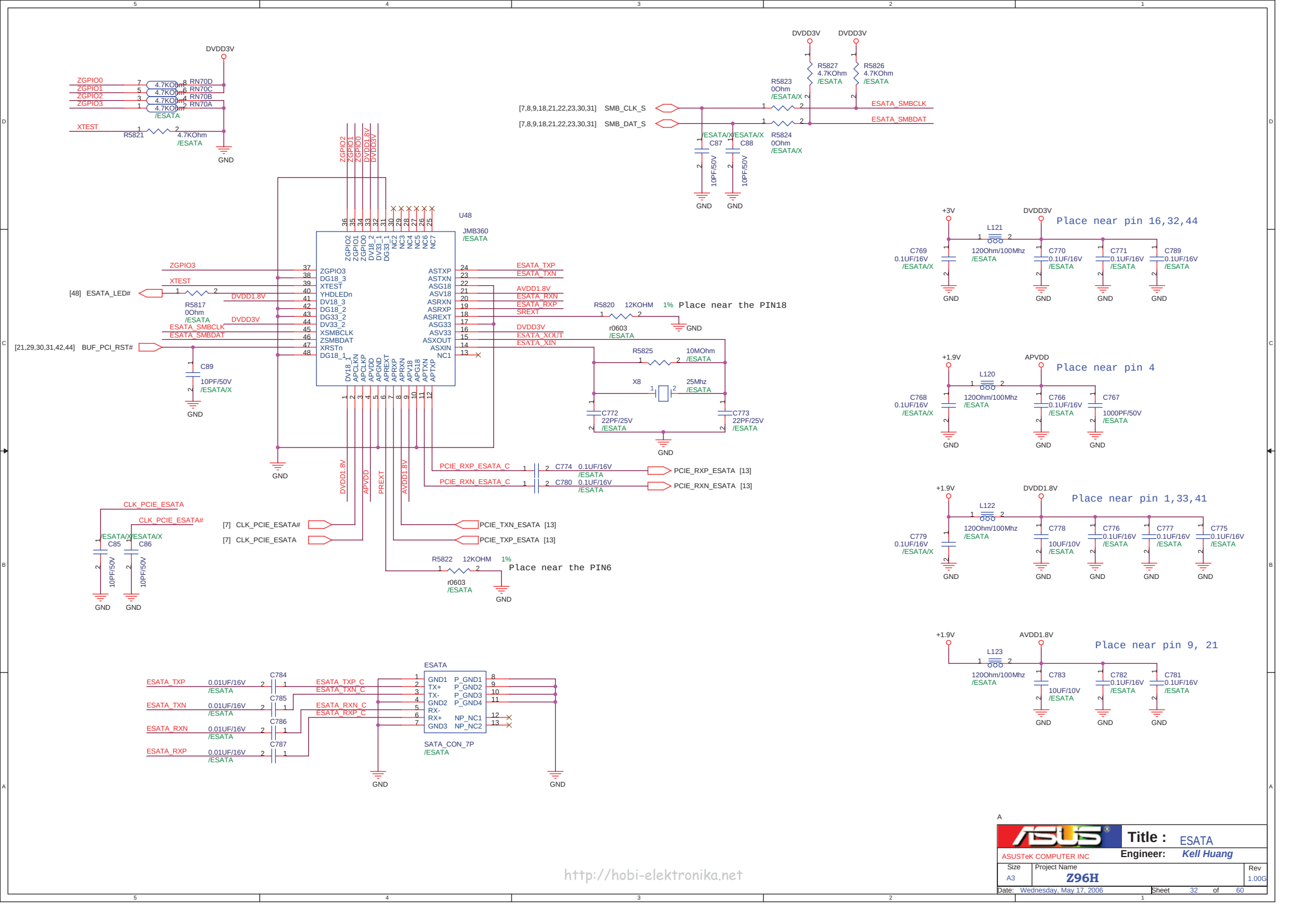


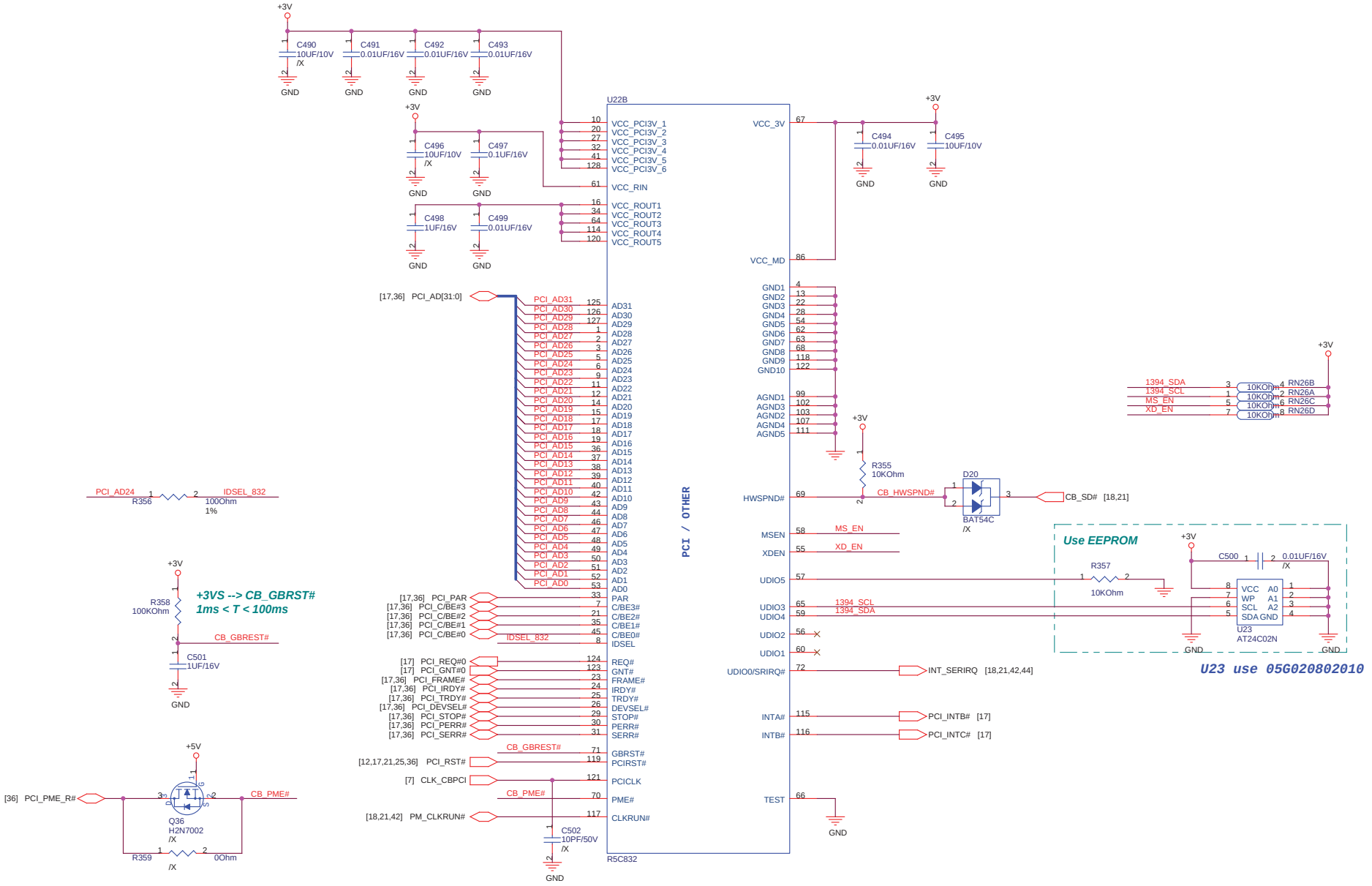
ASUSTeK COMPUTER INC. NB1	Title : HDD & ODD	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 29 of 60	



Title : MINICARD		
ASUSTeK COMPUTER INC.	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 30 of 60	

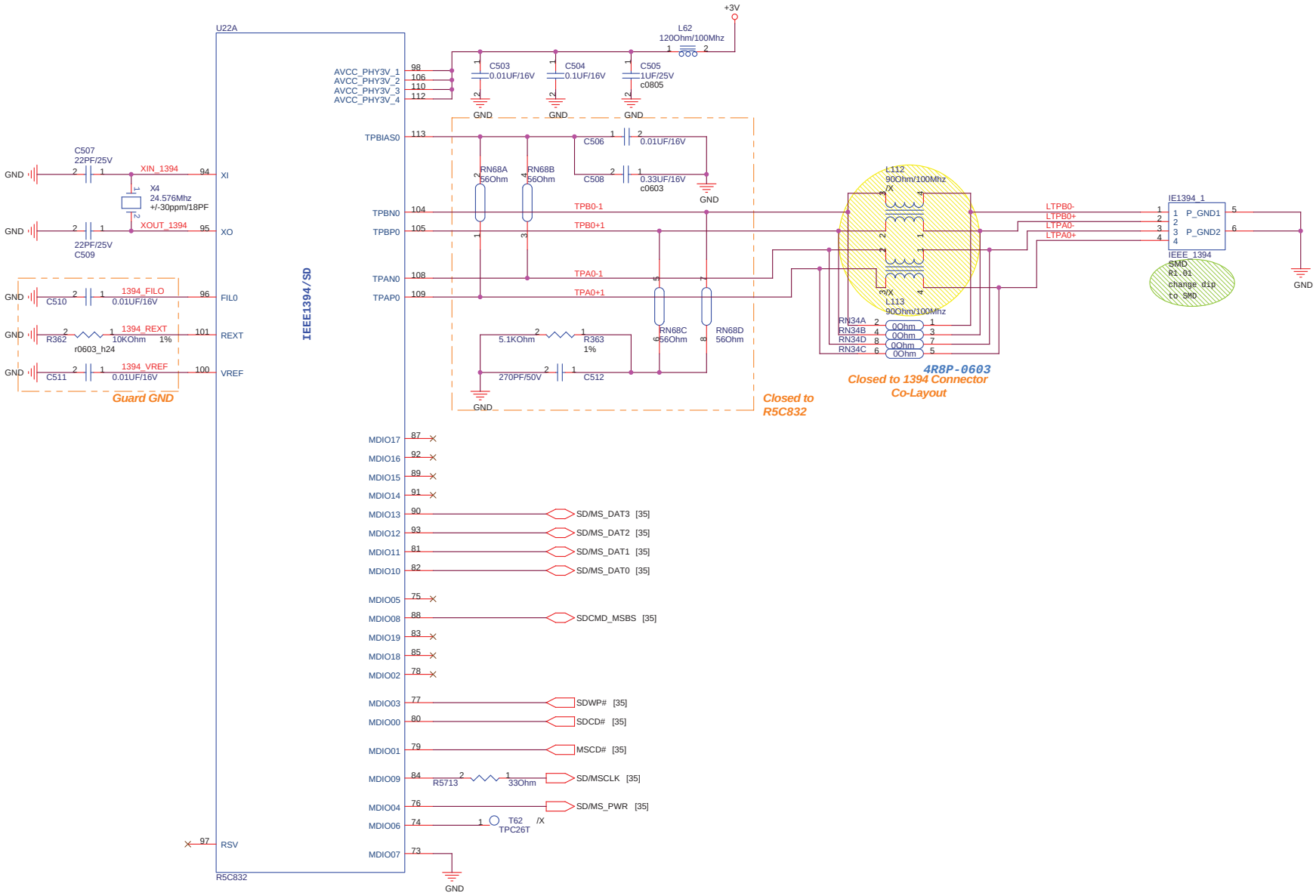

R367
0Ohm
[19] USB_PP6
[19] USB_PN6
L64
90Ohm/100Mhz
/X
USB_P6+
USB_P6-
0Ohm
R368
Co-Layout
D23
RSB6.8S
/X
D24
RSB6.8S
/X
GND
SMB_CLK_S
SMB_DAT_S
C38
C39
10PF/50V
CLK_PCIE_NEWCARD
CLK_PCIE_NEWCARD#
C34
C35
NewCard Ejecter
NEWCARD_EJECTER
P_GND1
P_GND2
CARD_EJECTOR_2P
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V
NewCard Header
NEWCARD
[21,29,30,32,42,44] BUF_PCI_RST#
[44,57,58] VSUS_ON
[44,51,60] SUSB_ON
U25
SYSRST#
SHDN#
STBY#
3.3V_1
3.3V_2
3.3VOUT_1
3.3VOUT_2
PERST#
NC
GND1
OC#
CLKEN
3.3Vaux
3.3Vaux_OUT
1.5V_1
1.5V_2
1.5VOUT_1
1.5VOUT_2
CPPE#
CPUSB#
P2231TFB1
REFCLK_EN
+3VSB
+3VSB_PE
+1.5V
+1.5V_PE
+3V
+3V_PE
Q6110
H2N7002
R5772
0Ohm
NEWCARD_OC# [19]
05/12/30 refer Z96J R1.01
[18,42,43,44] LPC_AD3
R80
33Ohm
/PCIE_DEBUG
SMB_CLK_S_R
SMB_DAT_S_R
PCIE_WAKE#_C_R
CLKREQ#_R
CPPE#_R
[7] CLK_PCIE_NEWCARD#
[7] CLK_PCIE_NEWCARD
[18] PCIE_RXN_NEWCARD
[18] PCIE_RXP_NEWCARD
[18] PCIE_TXN_NEWCARD
[18] PCIE_TXP_NEWCARD
GND1
USB_D-
USB_D+
CPUSB#
RESERVED1
RESERVED2
SMBCLK
SMBDATA
+1.5V_1
+1.5V_2
WAKE#
+3.3VAUX
PERST#
+3.3V_1
+3.3V_2
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND2
PERn0
PERp0
GND3
PETn0
PETp0
GND4
GND5
GND6
NP_NC1
NP_NC2
EXPRESS_CARD_26P
CLK_NEWCARD_REQ# [7]
Q44
H2N7002
[13,18,21,30,36] PCIE_WAKE#
PCIE_WAKE#_C
Q45
H2N7002
R369
0Ohm
/X
+3VSB
+3V
+1.5V
C517
0.1UF/16V
C518
10UF/10V
C519
C520
C521
3.0V~3.6V
Ave= 200mA
Max= 275 mA
3.0V~3.6V
Ave= 1000mA
Max= 1300 mA
1.35V~1.65V
Ave= 500 mA
Max= 650 mA
+3VSB_PE
+3V_PE
+1.5V_PE
C522
C523
C524
C525
C526
CPPE#
PCIE_WAKE#_C
SMB_CLK_S
SMB_DAT_S
0OHM
RN100A
RN100B
RN100C
RN100D
CPPE#_R
PCIE_WAKE#_C_R
SMB_CLK_S_R
SMB_DAT_S_R
/NO PCIE_DEBUG
U41
[7] CLK_PEDBPCI
[18,42,43,44] LPC_FRAME#
[18,42,43,44] LPC_AD0
[18,42,43,44] LPC_AD1
[18,42,43,44] LPC_AD2
[7,8,9,18,21,22,23,30,32] SMB_CLK_S
[7,8,9,18,21,22,23,30,32] SMB_DAT_S
DEBUG_EN#
A0
A1
A2
A3
A4
B0
B1
B2
B3
B4
BE#
BX
C0
C1
C2
C3
C4
D0
D1
D2
D3
D4
VCC
GND
SN74CBT3383PWR
/PCIE_DEBUG
+5V_DUAL
C100
0.1UF/16V
/PCIE_DEBUG/X
+3V_DUAL
R81
100KOhm
/PCIE_DEBUG
DEBUG_EN#
Q9
PMBS3904
/PCIE_DEBUG
R82
10KOhm
/PCIE_DEBUG
D10
F01J4L
/PCIE_DEBUG
C101
0.1UF/16V
/PCIE_DEBUG
PERST#
C103
0.22UF/6.3V
/PCIE_DEBUG
C102
0.1UF/16V
/PCIE_DEBUG
R83
10KOhm
/PCIE_DEBUG
http://hobi-elektronika.net
Title : NEWCARD
ASUSTeK COMPUTER INC. NB1
Engineer: Kell Huang
Size
Custom
Project Name
Z96H
Rev
1.00G
Date: Wednesday, May 17, 2006
Sheet 31 of 60



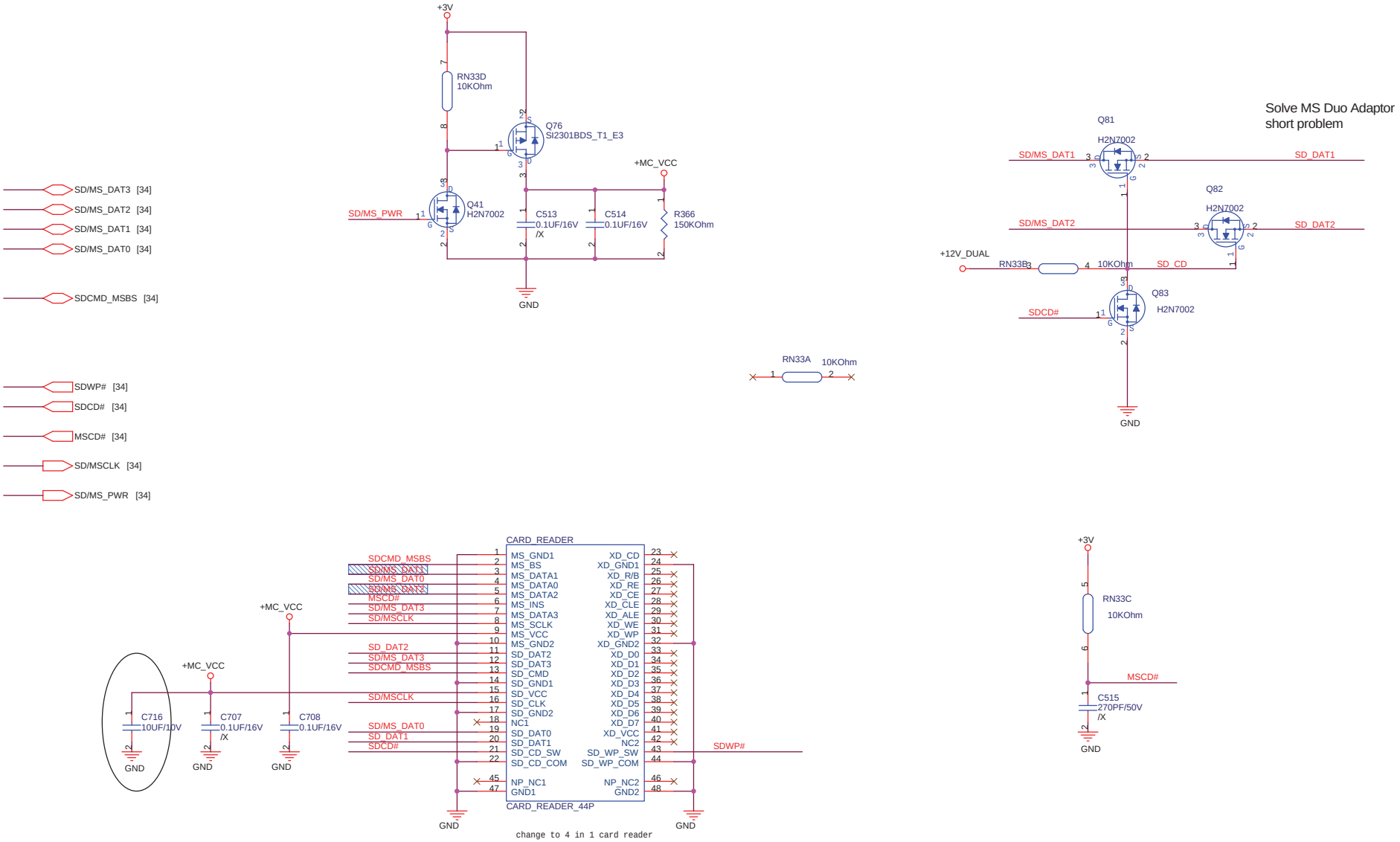


PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD24	0	C
1394	AD24	0	B

ASUSTeK COMPUTER INC. MB6	Title : CARD1394-R5C832(1)	
Engineer: Kell Huang		
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 33 of 60	



Title :	CARD1394-R5C832(2)	
ASUSTeK COMPUTER INC. MB6	Engineer:	kell Huang
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 34 of 60	



Title :	4 in 1 CARD READER	
ASUSTeK COMPUTER INC	Engineer:	Kell Huang
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 35 of 60	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	1	D

	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64/78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

*All termination resistors should be near chip

ASUSTeK COMPUTER INC

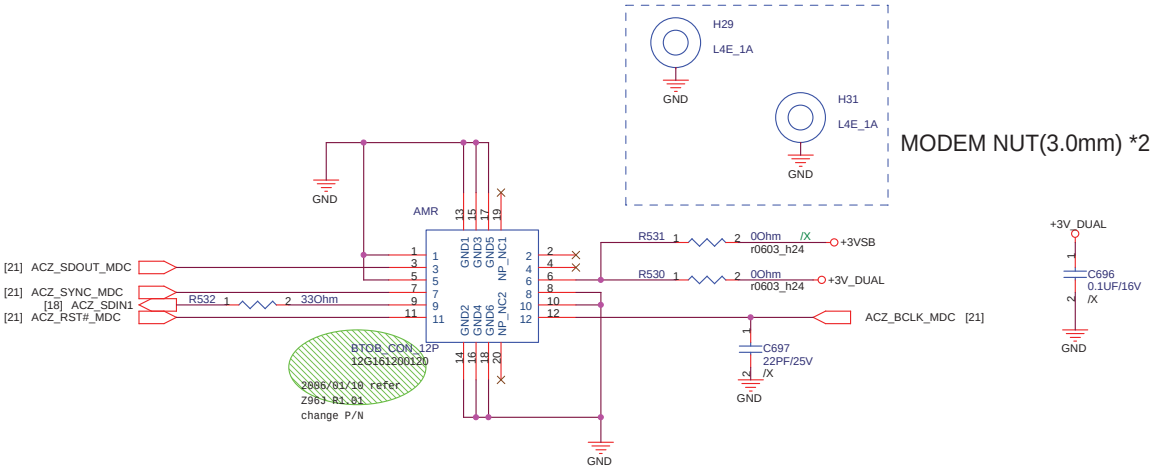
Title : LAN RTL8110SBL

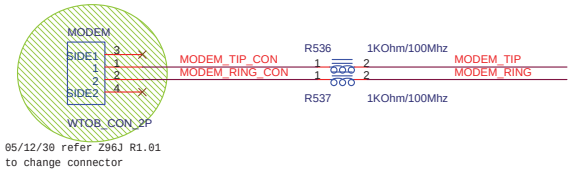
Engineer: Kell Huang

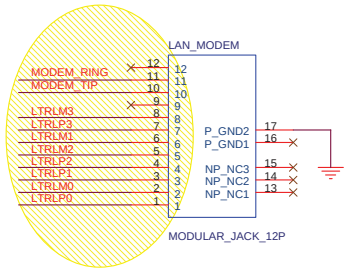
Size: Custom | Project Name: Z96H | Rev: 1.00G

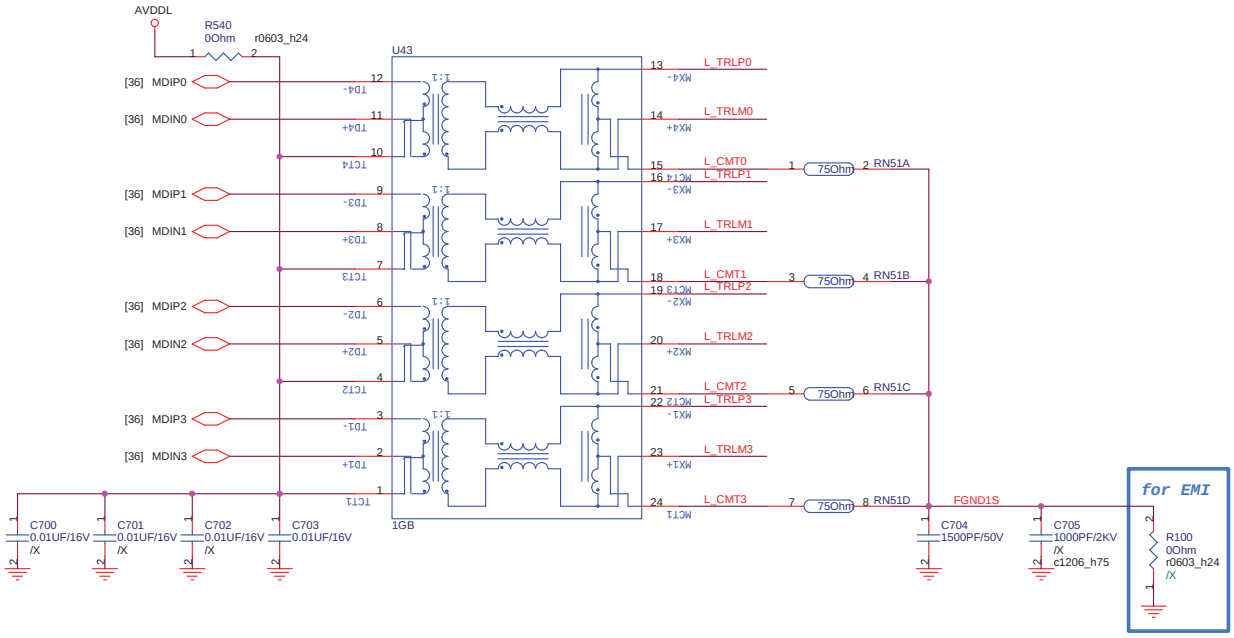
Date: Wednesday, May 17, 2006 | Sheet 36 of 60

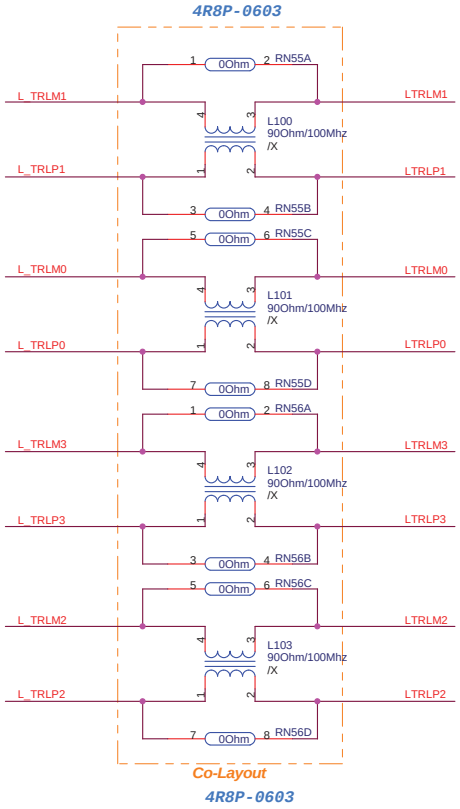
MDC CONN.



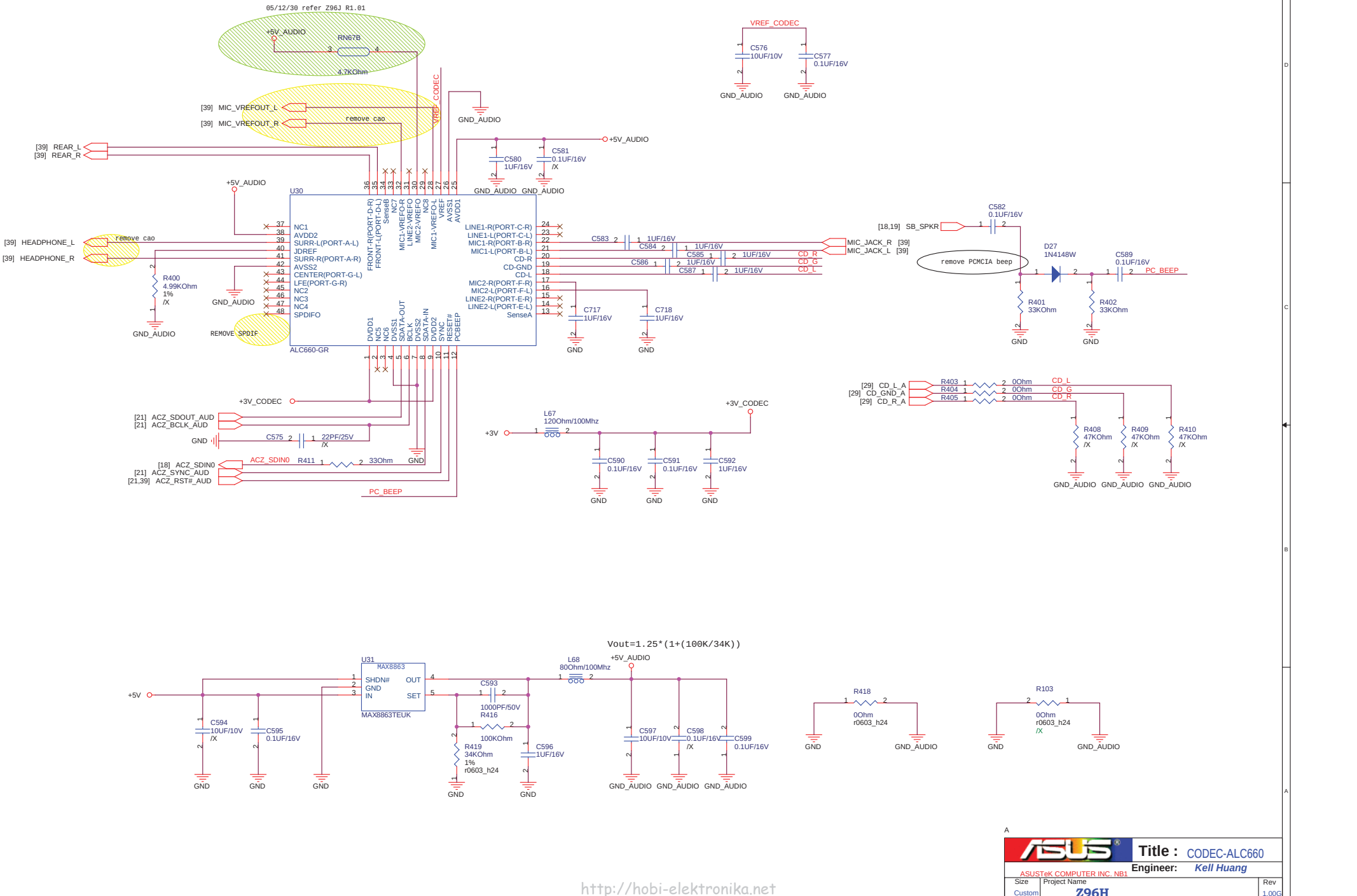




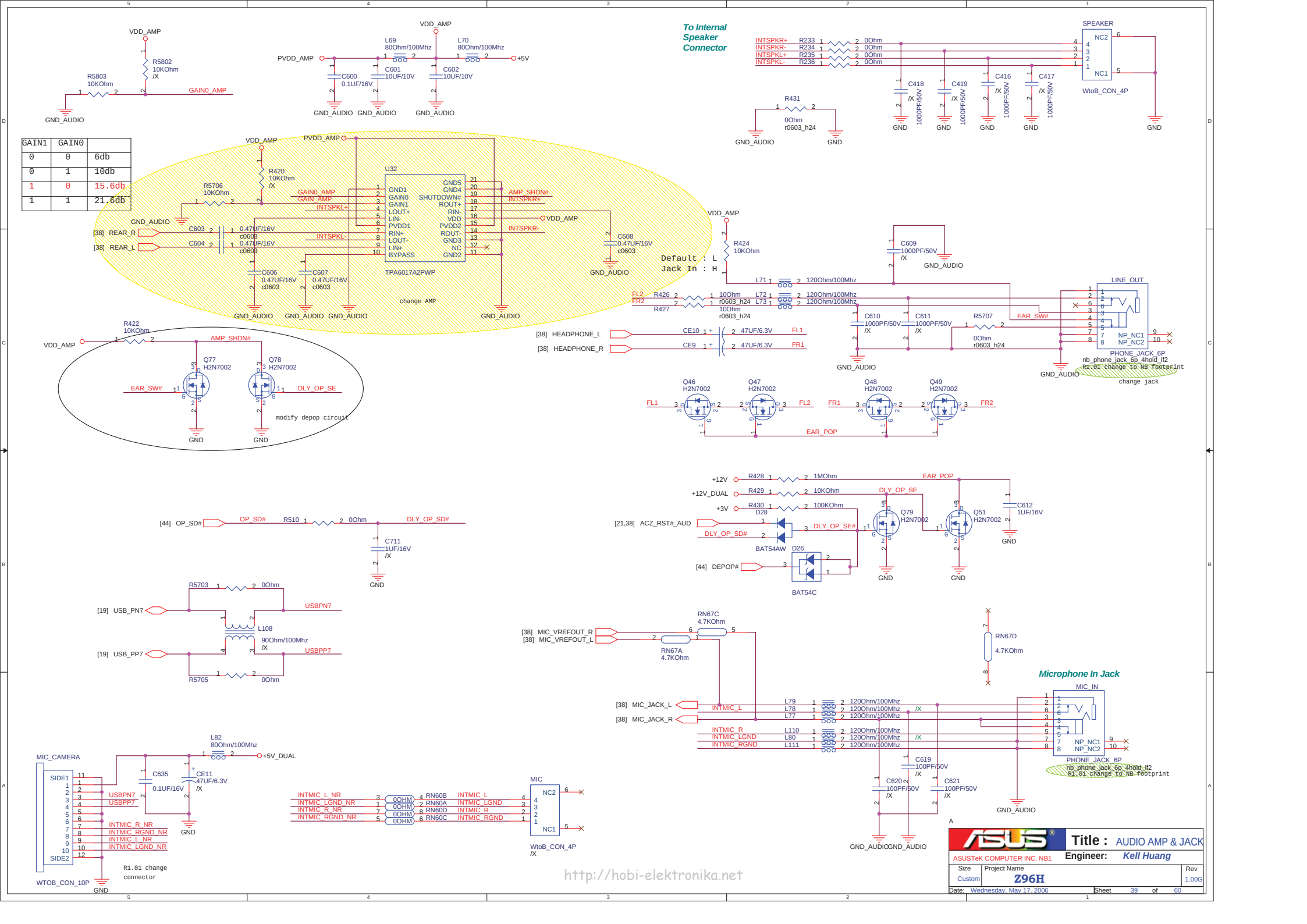


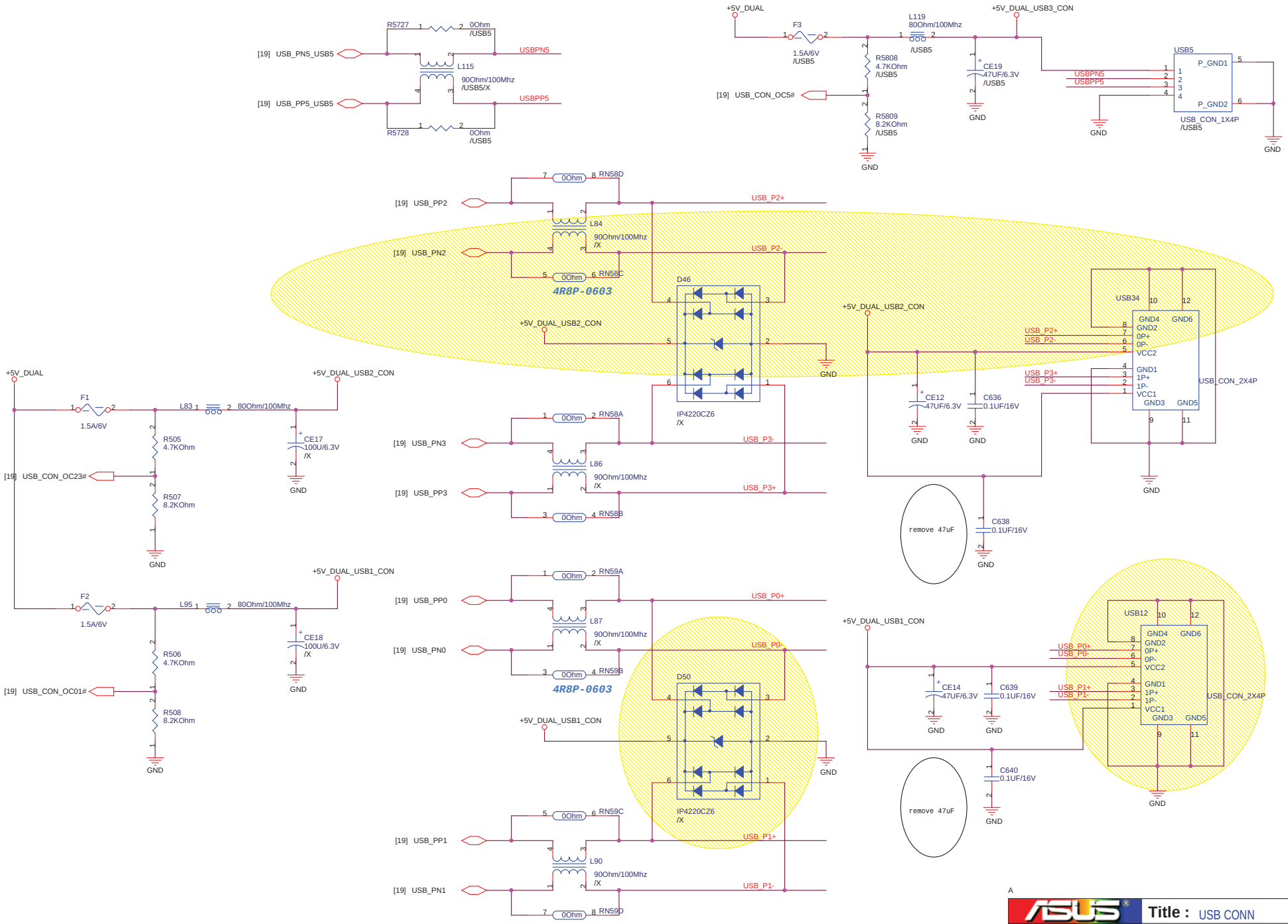


ASUSTeK COMPUTER INC.	Title : RJ45&RJ11	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 37 of 60	



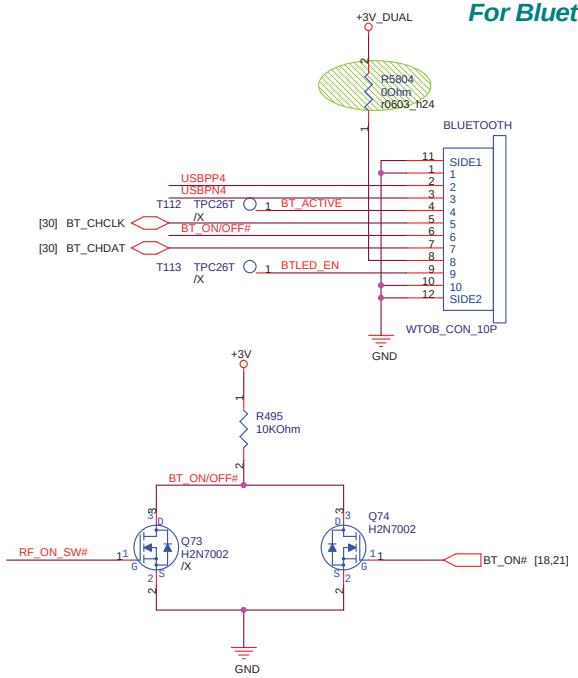
Title :	CODEC-ALC660	
Engineer:	Kell Huang	
ASUSTeK COMPUTER INC. NB1		
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 38 of 60	


VDD_AMP
R5802
10KOhm
/X
R5803
10KOhm
GAIN0_AMP
GND_AUDIO
PVDD_AMP
L69
80Ohm/100Mhz
L70
80Ohm/100Mhz
+5V
C600
0.1UF/16V
C601
10UF/10V
C602
10UF/10V
GND_AUDIO
To Internal Speaker Connector
INTSPKR+
INTSPKR-
INTSPKL+
INTSPKL-
R233
R234
R235
R236
0Ohm
C418
C419
C416
C417
1000PF/50V
SPEAKER
NC2
NC1
WtoB_CON_4P
R431
0Ohm
r0603_h24
GAIN1
GAIN0
GAIN_AMP
R420
10KOhm
R5706
10KOhm
U32
GND1
GAIN0
GAIN1
LOUT+
LIN-
PVDD1
RIN+
LOUT-
LIN+
BYPASS
GND5
GND4
SHUTDOWN#
ROUT+
RIN-
VDD
PVDD2
ROUT-
GND3
NC
GND2
AMP_SHDN#
INTSPKR+
INTSPKR-
TPA6017A2PWP
change AMP
C603
C604
0.47UF/16V
c0603
[38] REAR_R
[38] REAR_L
C606
C607
C608
Default : L
Jack In : H
R424
10KOhm
C609
1000PF/50V
L71
L72
L73
120Ohm/100Mhz
FL2
FR2
R426
R427
10Ohm
r0603_h24
C610
C611
R5707
EAR_SW#
LINE_OUT
NP_NC1
NP_NC2
PHONE_JACK_6P
nb_phone_jack_6p_4hold_lf2
R1.01 change to NB Footprint
change jack
R422
10KOhm
Q77
H2N7002
Q78
H2N7002
DLY_OP_SE
modify depop circuit
[38] HEADPHONE_L
[38] HEADPHONE_R
CE10
CE9
47UF/6.3V
FL1
FR1
Q46
Q47
Q48
Q49
EAR_POP
[44] OP_SD#
OP_SD#
R510
DLY_OP_SD#
C711
1UF/16V
+12V
+12V_DUAL
+3V
R428
R429
R430
1MOhm
10KOhm
100KOhm
D28
BAT54AW
D26
BAT54C
[21,38] ACZ_RST#_AUD
DLY_OP_SE#
[44] DEPOP#
Q79
H2N7002
Q51
H2N7002
C612
1UF/16V
R5703
R5705
0Ohm
[19] USB_PN7
[19] USB_PP7
USBPN7
USBPP7
L108
90Ohm/100Mhz
RN67C
4.7KOhm
RN67A
RN67D
[38] MIC_VREFOUT_R
[38] MIC_VREFOUT_L
Microphone In Jack
[38] MIC_JACK_L
[38] MIC_JACK_R
INTMIC_L
INTMIC_R
INTMIC_LGND
INTMIC_RGND
L79
L78
L77
L110
L80
L111
MIC_IN
C619
C620
C621
100PF/50V
MIC_CAMERA
SIDE1
SIDE2
L82
80Ohm/100Mhz
+5V_DUAL
C635
0.1UF/16V
CE11
47UF/6.3V
INTMIC_L_NR
INTMIC_R_NR
INTMIC_LGND_NR
INTMIC_RGND_NR
RN60A
RN60B
RN60C
RN60D
0OHM
MIC
WtoB_CON_4P
WTOB_CON_10P
R1.01 change connector
GAIN1 GAIN0 6db 0 0 0 1 10db 1 0 15.6db 1 1 21.6db
http://hobi-elektronika.net
ASUSTeK COMPUTER INC. NB1
Title : AUDIO AMP & JACK
Engineer: Kell Huang
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 39 of 60

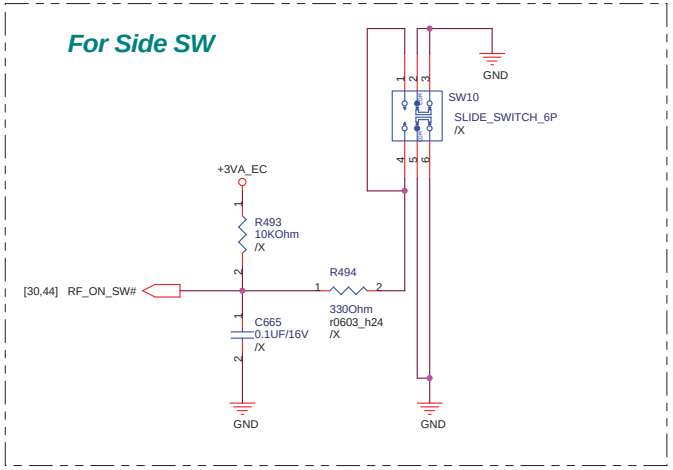


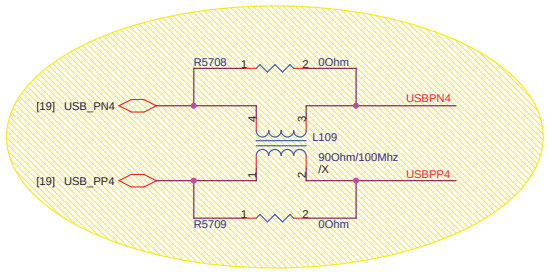
ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 40 of 60	

For Bluetooth



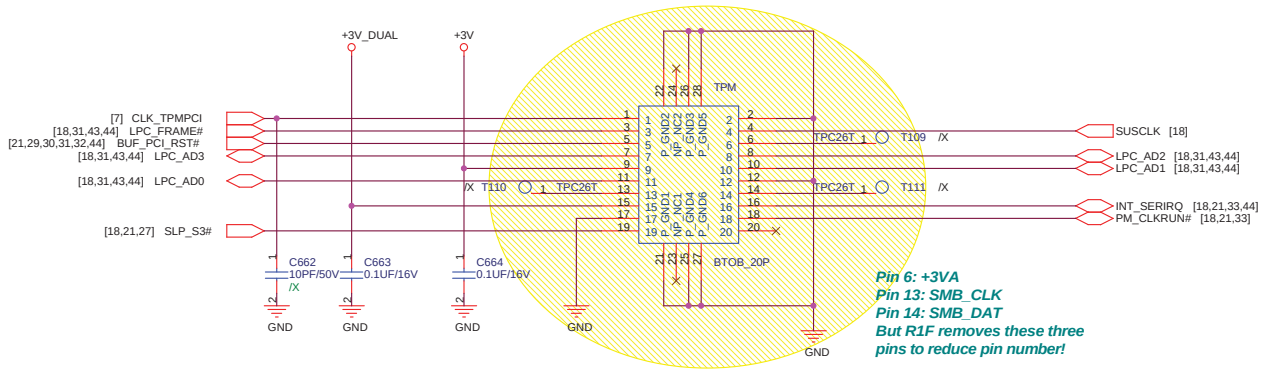
For Side SW



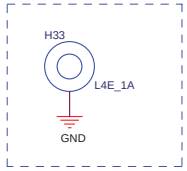


ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 41 of 60	

For TPM Module



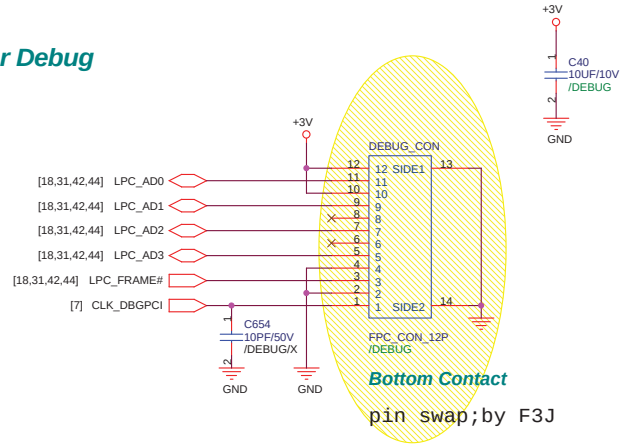
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!



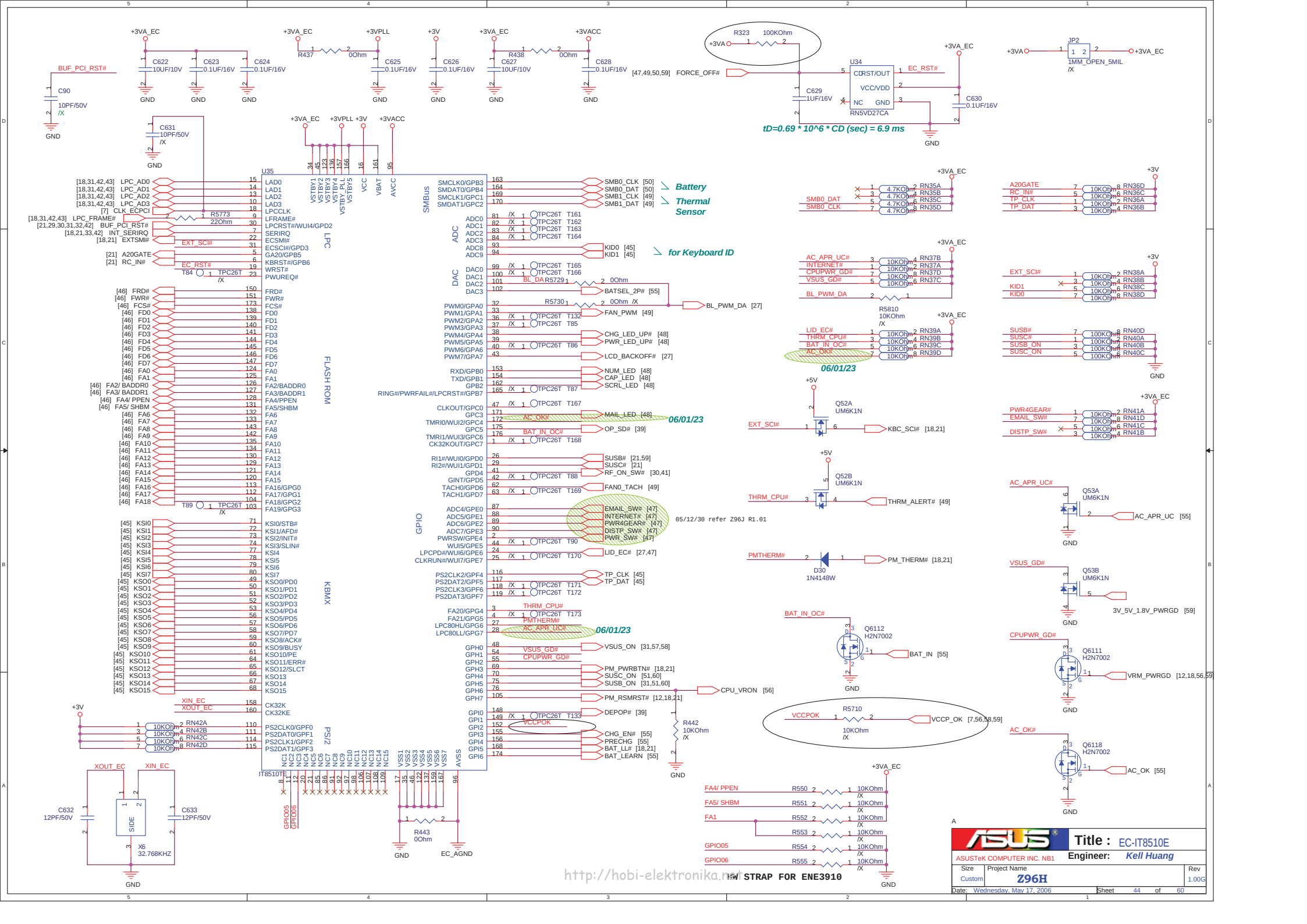
TPM MODULE NUT(3.0mm) *1

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 42 of 60	

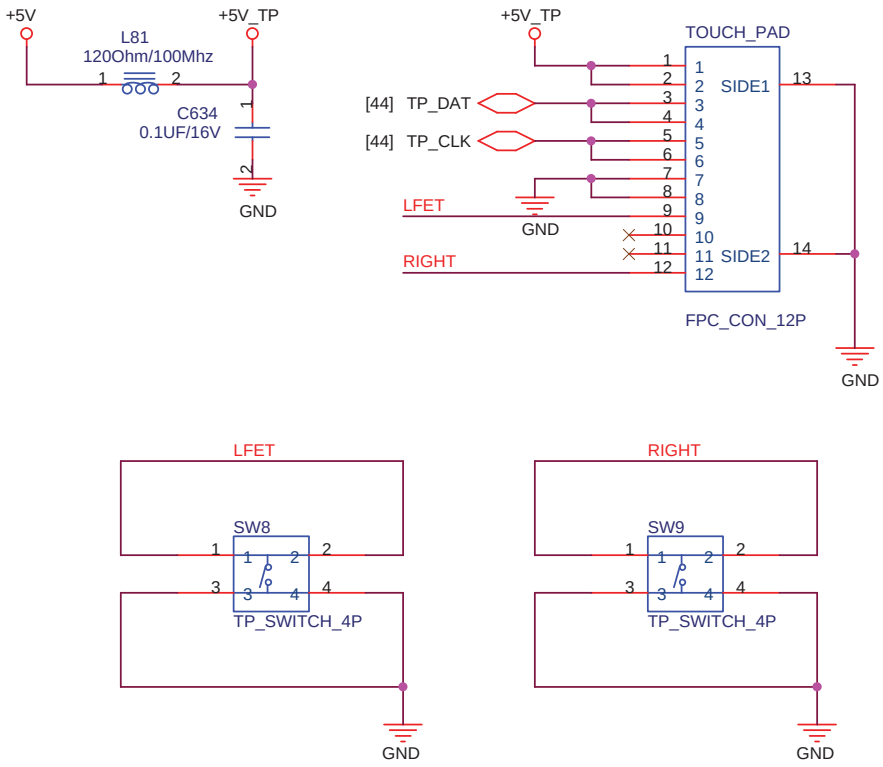
For Debug



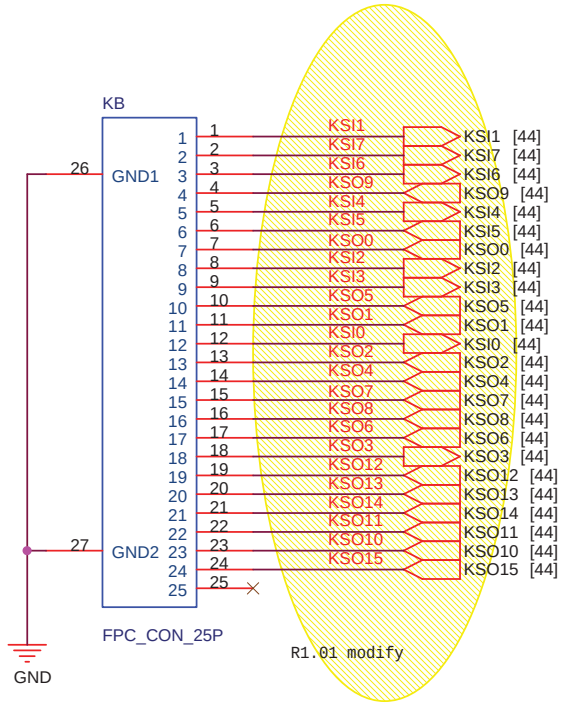
ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 43 of 60	

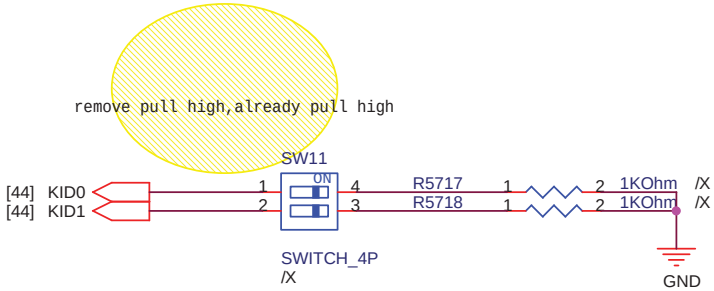

U35
IT8510TE
LPC
FLASH ROM
KBMX
PS2
GPIO
SMBus
ADC
DAC
Battery
Thermal Sensor
for Keyboard ID
06/01/23
05/12/30 refer Z96J R1.01
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
HW STRAP FOR ENE3910
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Kell Huang
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 44 of 60
http://hobi-elektronika.net

For Touch-Pad

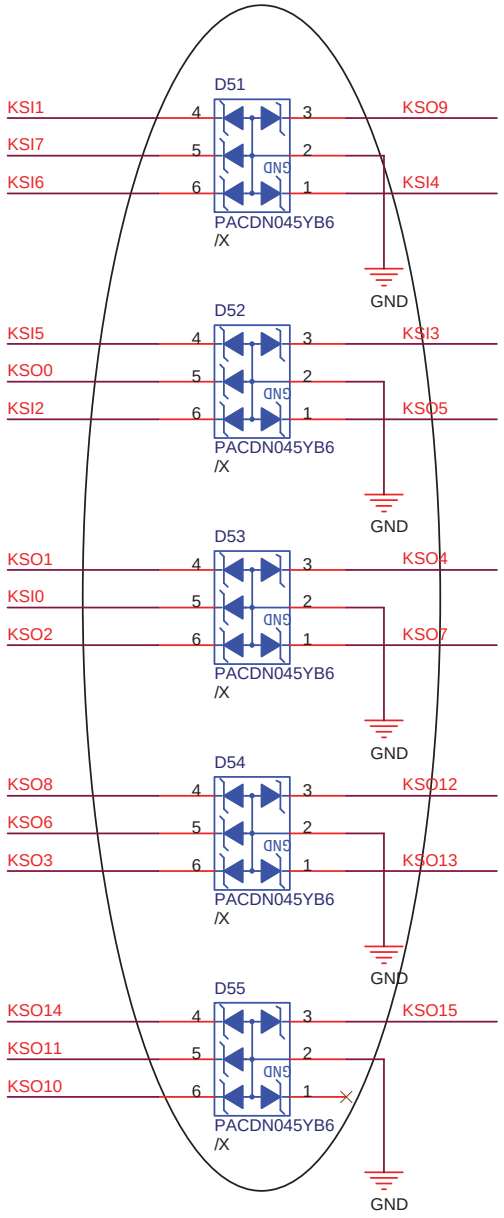


For Keyboard



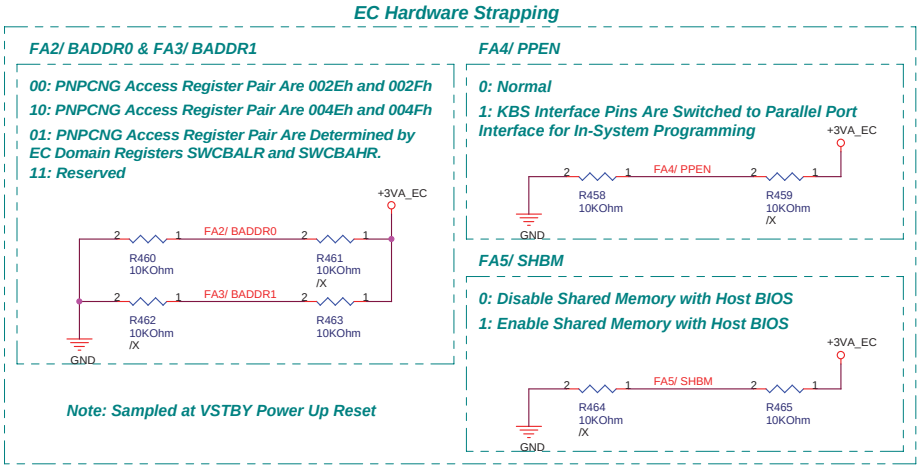


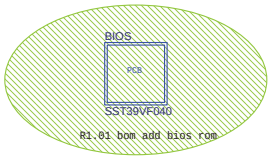
05/12/29 ESD DIODE PIN SWAPPED

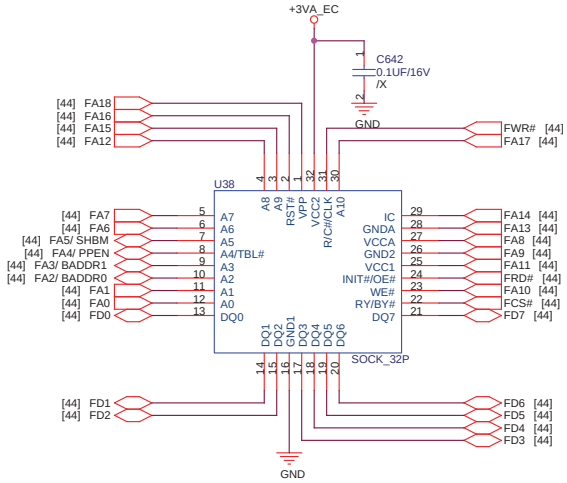


ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: Kell Huang	
Size: A4	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 45 of 60	

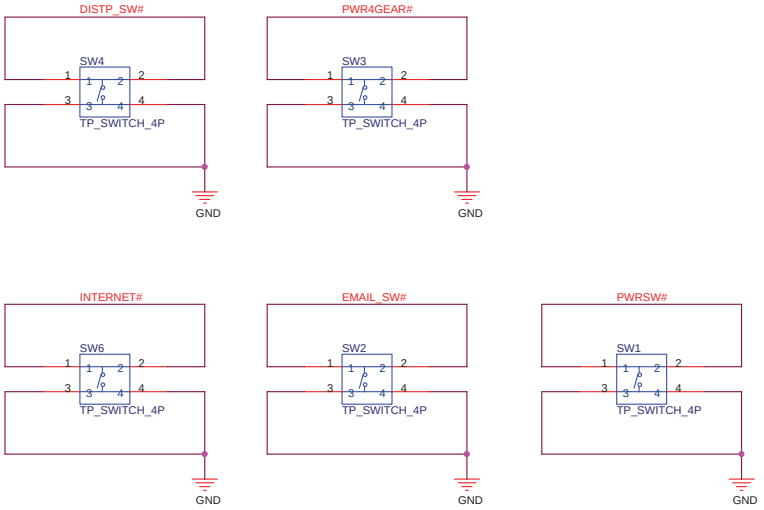
ISA ROM

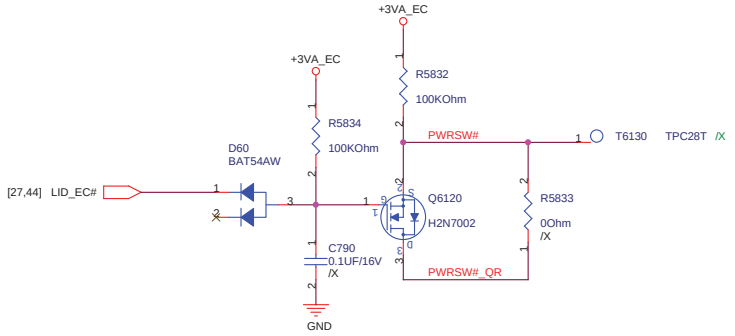




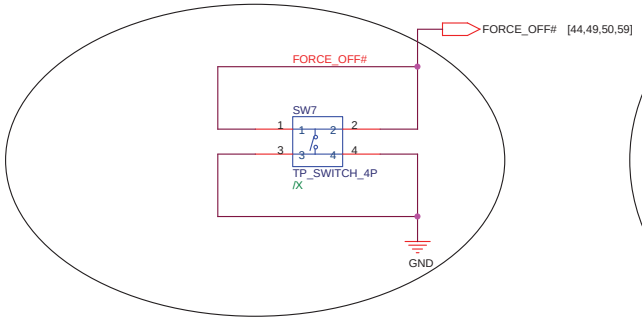


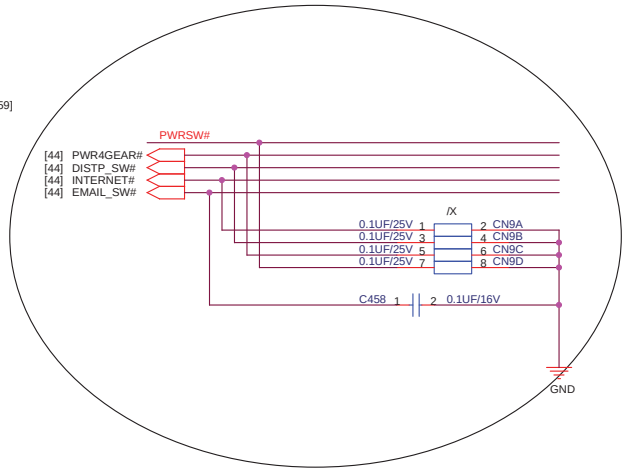
ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 46 of 60	

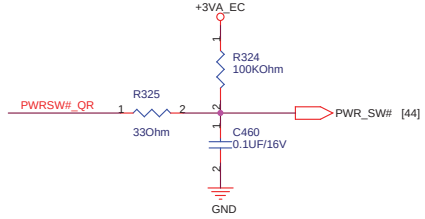




SHUT_DOWN#



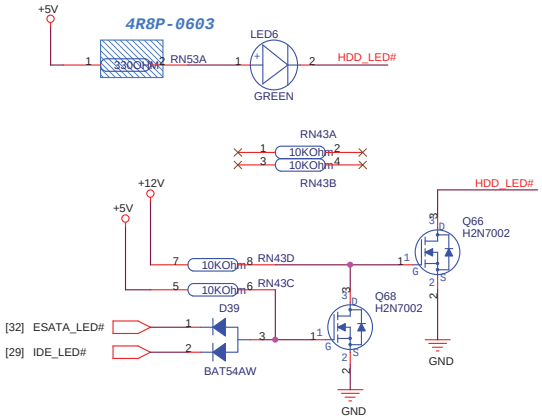




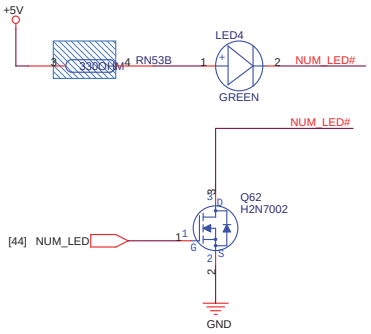
ASUSTeK COMPUTER INC	Title : SWITCH	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 47 of 60	

For LED

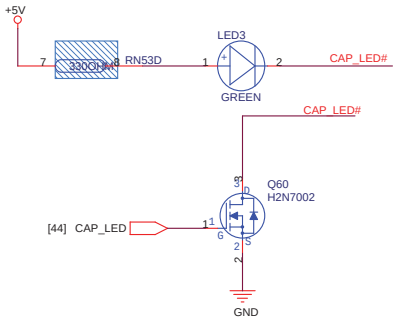
For SATA/IDE LED



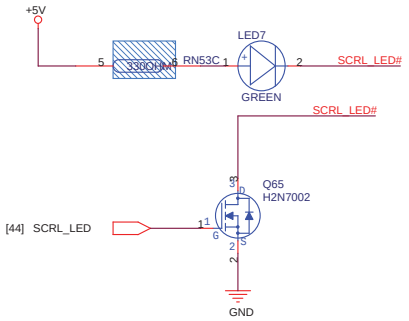
for Num Lock



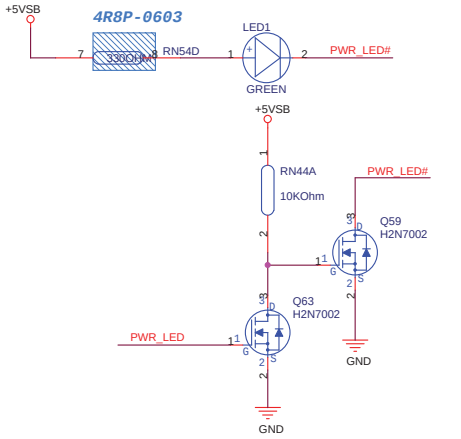
for Cap. Lock



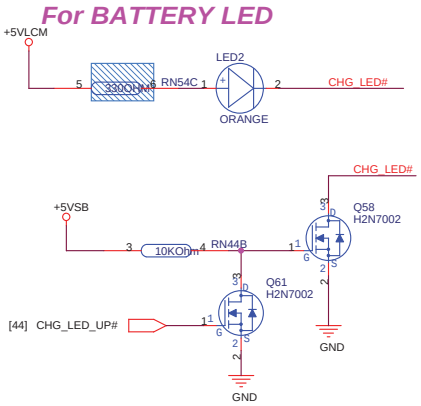
for Scroll Lock



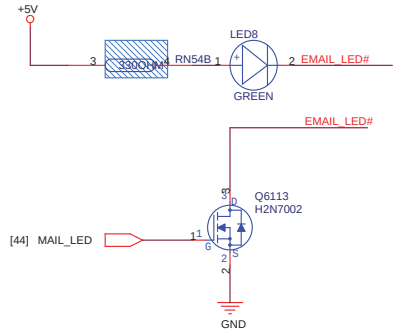
For POWER LED



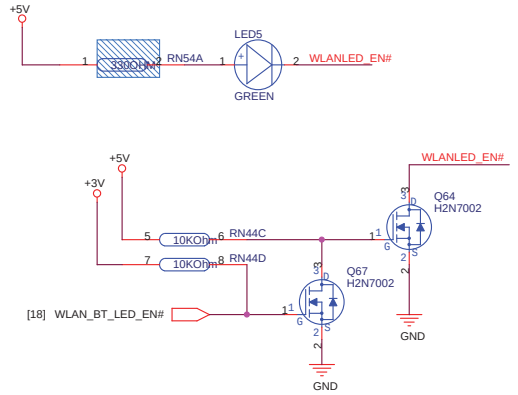
For BATTERY LED



for email

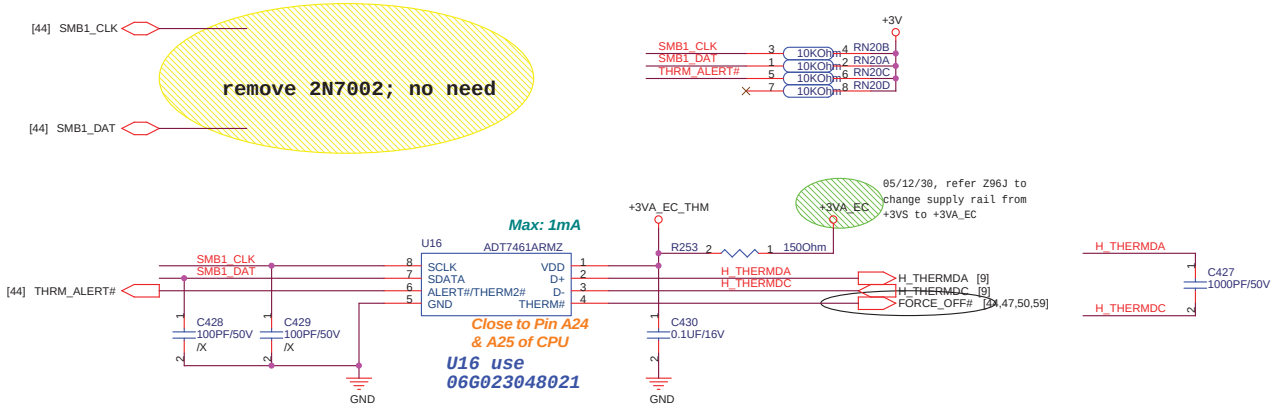


For WireLess LED



ASUSTeK COMPUTER INC	Title : LED		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 48 of 60		

Thermal Sensor

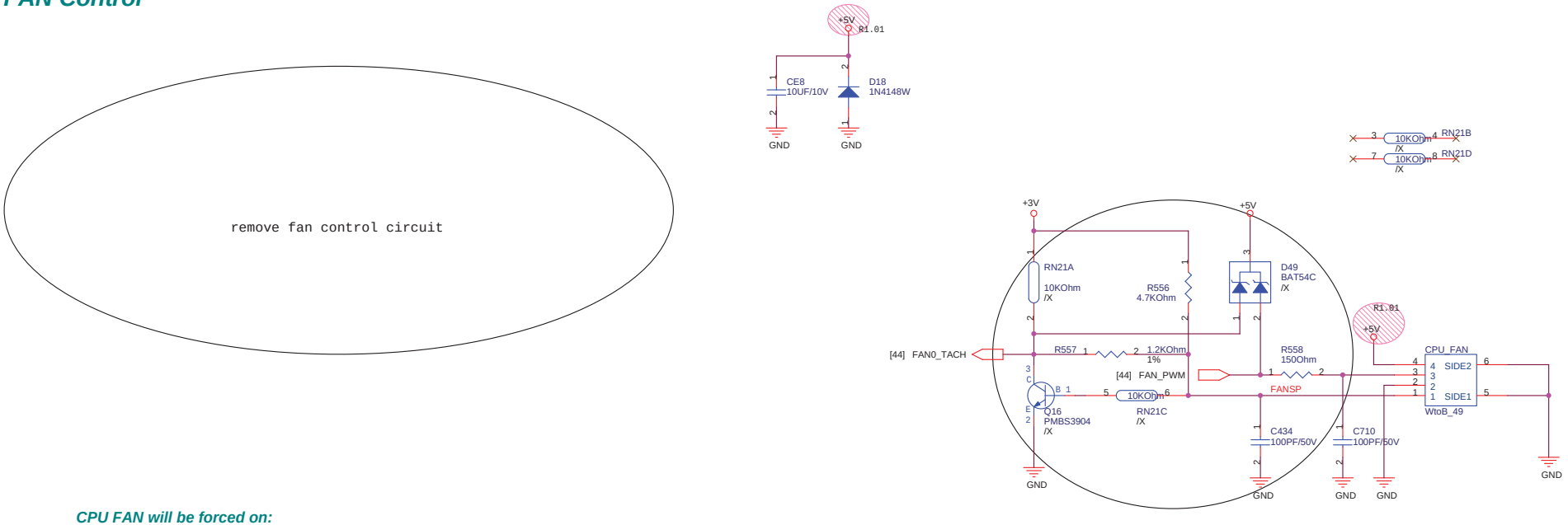


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

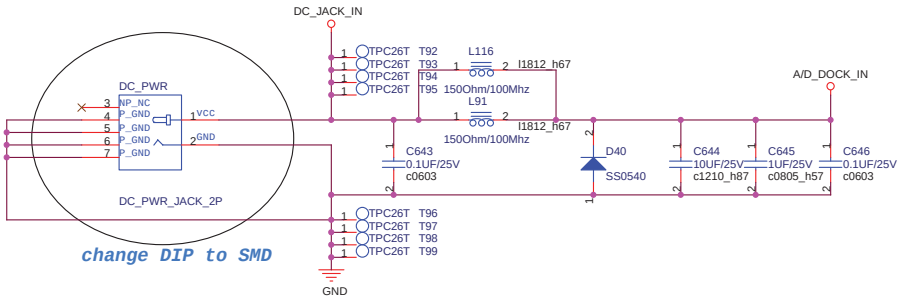
DC FAN Control



CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

Title :	THER SENSOR & FAN	
ASUSTeK COMPUTER INC.	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 49 of 60	

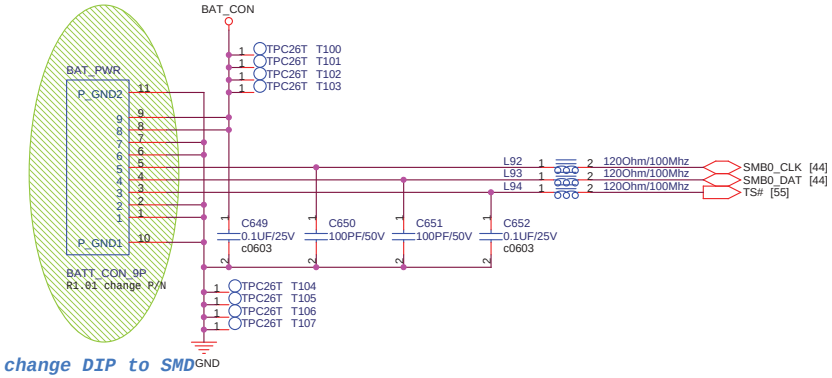
DC IN



change DIP to SMD

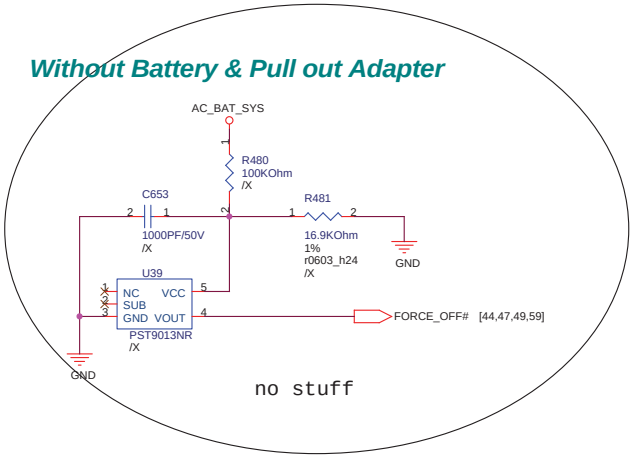
remove AC DC detect; no need

BAT IN



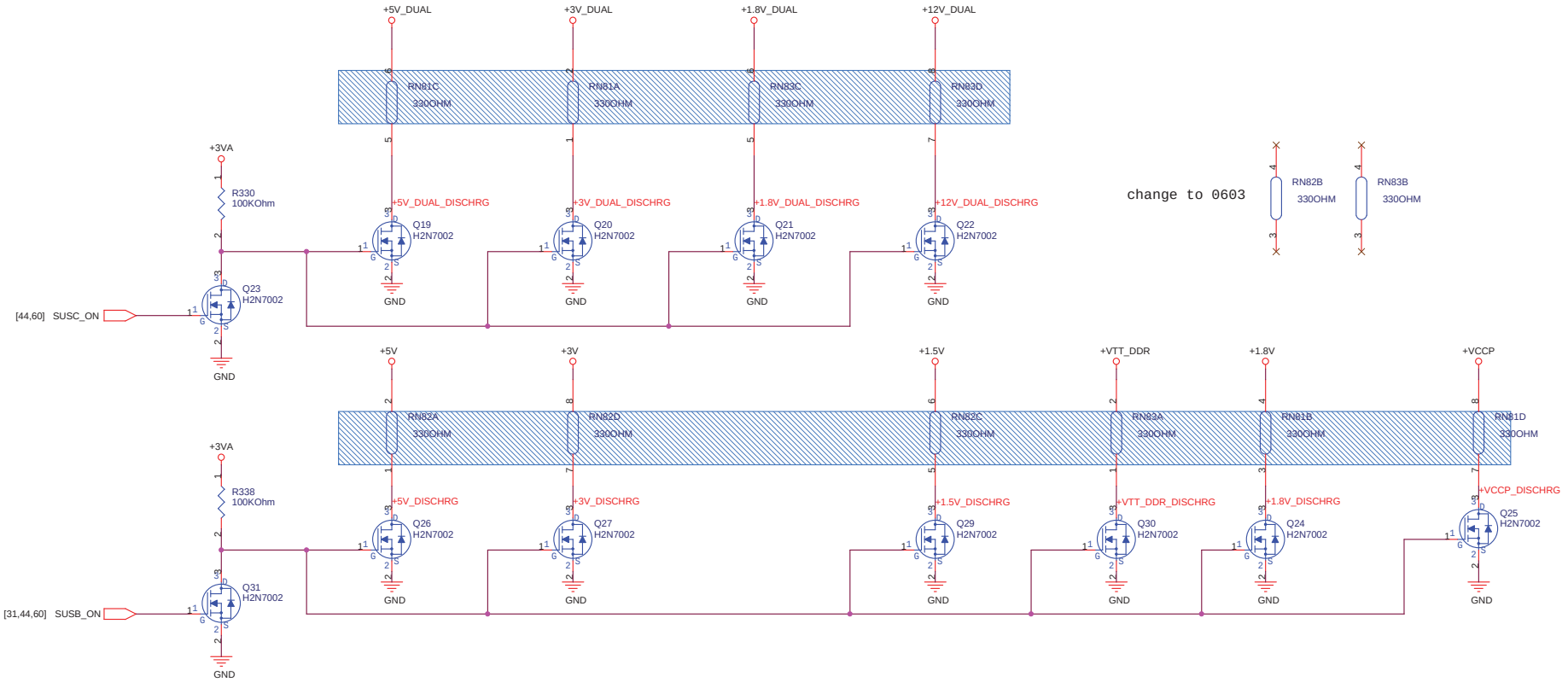
change DIP to SMD

Without Battery & Pull out Adapter



no stuff

Title :	DC & BAT IN	
ASUSTeK COMPUTER INC. NB1	Engineer:	Kell Huang
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 50 of 60	



ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 51 of 60	

PAD1 SMD394X197
PAD2 SMD394X197
PAD3 SMD394X197
PAD4 SMD394X197
PAD5 SMD394X197
PAD6 SMD1248X197_PT
H47 C236
PAD7 SMD1890X197_PT
PAD8 SMD197X1803
GND

H1
NP_NC1 GND
NP_NC2
2DRILL_D71N_D110N

H48
NP_NC1 GND
NP_NC2
2DRILL_D110N_D71N

H19
H5
H15
H25
H7
H13
H9
H17
H11
H27
H21
NP_NC GND
S354D110N

H50
2DRILL_D87N_D110N

H58
C256D126

H60
C256D126

H52
2DRILL_D110N_D87N

H35
C315D163

H39
C315D163

H62
C315D163

H37
C315D163

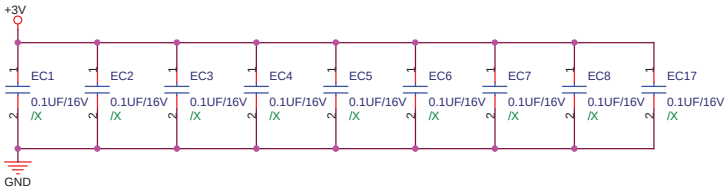
H70
C315D163

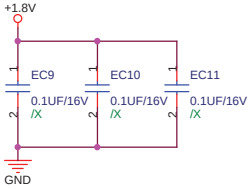
H71
C315D163

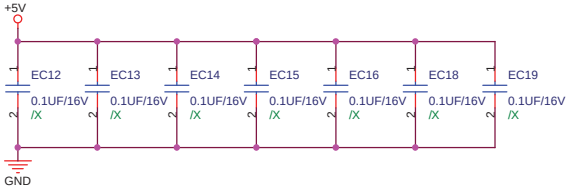
H72
C315D163

for NB

ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 52 of 60	

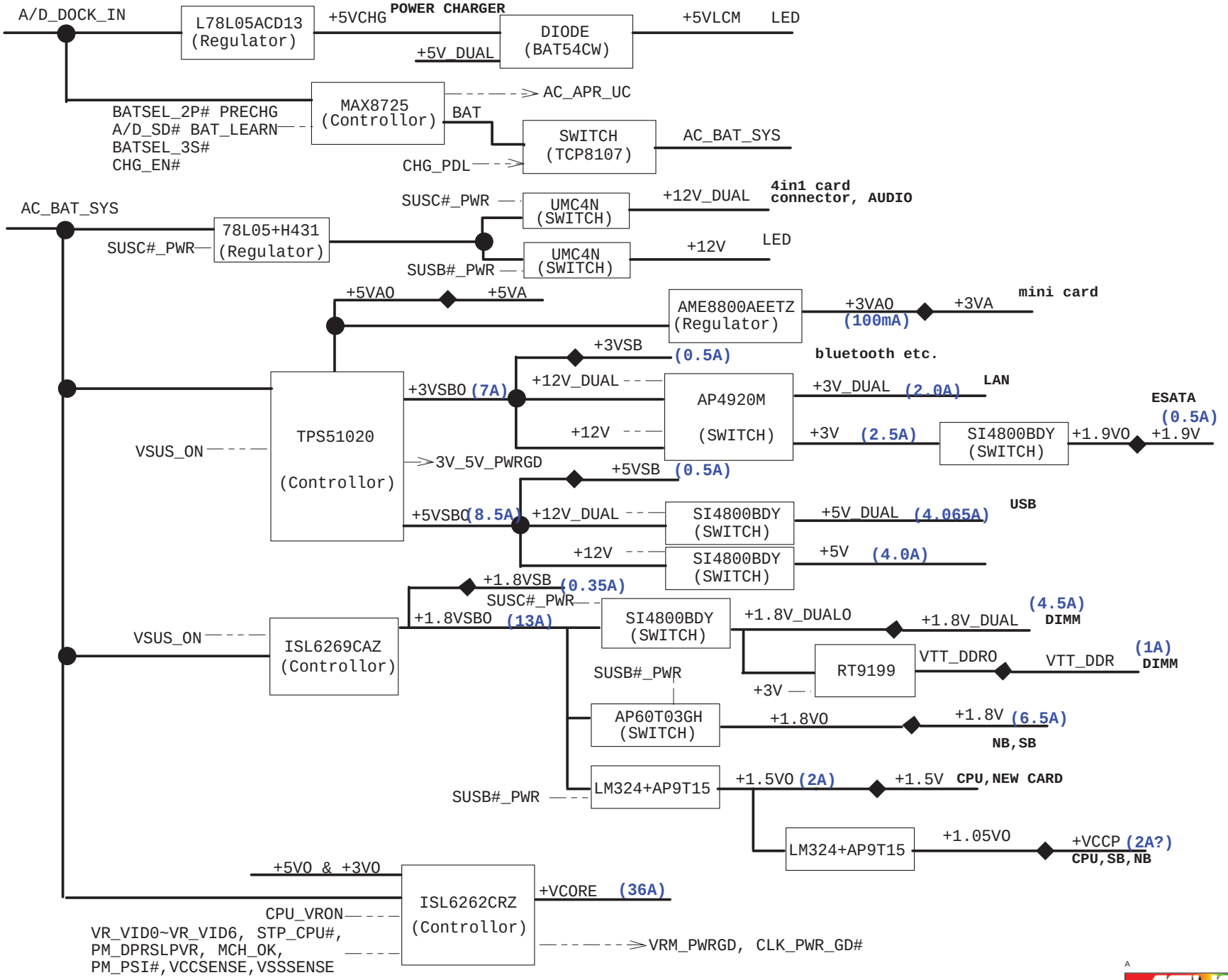






A

ASUSTeK COMPUTER INC.	Title : EMI	
	Engineer: Kell Huang	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 53 of 60	



ASUSTeK COMPUTER INC	Title : POWER_FLOWCHART	
	Engineer:	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 54 of 60	

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R5710=20K,R5715=137K

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V
=> Iin(max)=2.544A
=> Constant Power = 19 * 2.44 = 48.336W
=> R5710=20K,R5715=42.2K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)= 25m Ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.588V
=> Vbatt = 4.2V

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V<Vmoce<2V)	Battery Learn

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

Battery Charging Voltage :
+V_BAT= 4 x [4.2235+(Vvctl-1.8)/9.52]

Battery Charging Current :
Icharge=(0.075/PR5706) x (Victl/3.6))

Input Adaptor Max. Current Limit :
Ilimit_current=(0.075/PR5701) x (Vcls/4.2235)

Pre-Charging Mode :
Precharging current = 163.9mA
Victl = 0.098V

Battery Cell Selection :
BATSEL_2P# = 1, 6 Cells; Victl = 1.678V
=> Icharge = 2.331A
BATSEL_2P# = 0, 9 Cells; Victl = 2.785V
=> Icharge = 3.868A

[44] BATSEL_2P#
BATSEL_2P# = 1, 6 Cells
BATSEL_2P# = 0, 9 Cells

[44] PRECHG
PRECHG = 1, Pre-Charging Mode
Charging Current = 156mA

[44] CHG_EN#
CHG_EN# = 1, Charger Disabled
CHG_EN# = 0, Charger Enabled

[44] AC_OK
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent

A/D_SD#=1. Enable charger
A/D_SD#=0. Disable charger

[44] BAT_LEARN
BAT_LEARN = 1, Battery discharges
BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

AC_APR_UC [44]
AC_APR_UC = 1, Adaptor is present
AC_APR_UC = 0, Adaptor is absent

BAT_IN [44]
BAT_IN = 0; Battery absence
BAT_IN = 1; Battery Plug-in

[50] TS#
TS# = 1; Battery absence
TS# = 0; Battery Plug-in

Battery Voltage

Title :	POWER_CHARGER
Engineer:	
ASUSTeK COMPUTER INC	
Size	C
Project Name	Z96H
Rev	1.00G
Date:	Wednesday, May 17, 2006
Sheet	55 of 60

	DPRSLPVR	DPRSTP#	PSI#	Phase Operation Modes	Expected CPU mode
Intel IMVP 6 Compliant Logic	0	1	1	2-phase CCM	active mode
	0	1	0	1-phase CCM	active mode
	1	0	1	1-phase diode emulation	deeper sleep mode
	1	0	0	1-phase diode emulation	deeper sleep mode

+Vcore / 36A

change BOM to 11G040222721(220u/25v)

ESR 9mOHM

ESR 7mOHM

CPU	Parts	Values
Yonha	PCE5002	220UF/2V 11G08D222795
	PCE5003	
Merom	PCE5006	330UF/2V 11G08D337791
	PCE5007	

Net	Width	Net	Width
VR_VIO0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSENSE	10mil	AC_BAT_SYS	Shape

PC5028 & PC5029 for Transient Response

Close to Phase 1 Inductor

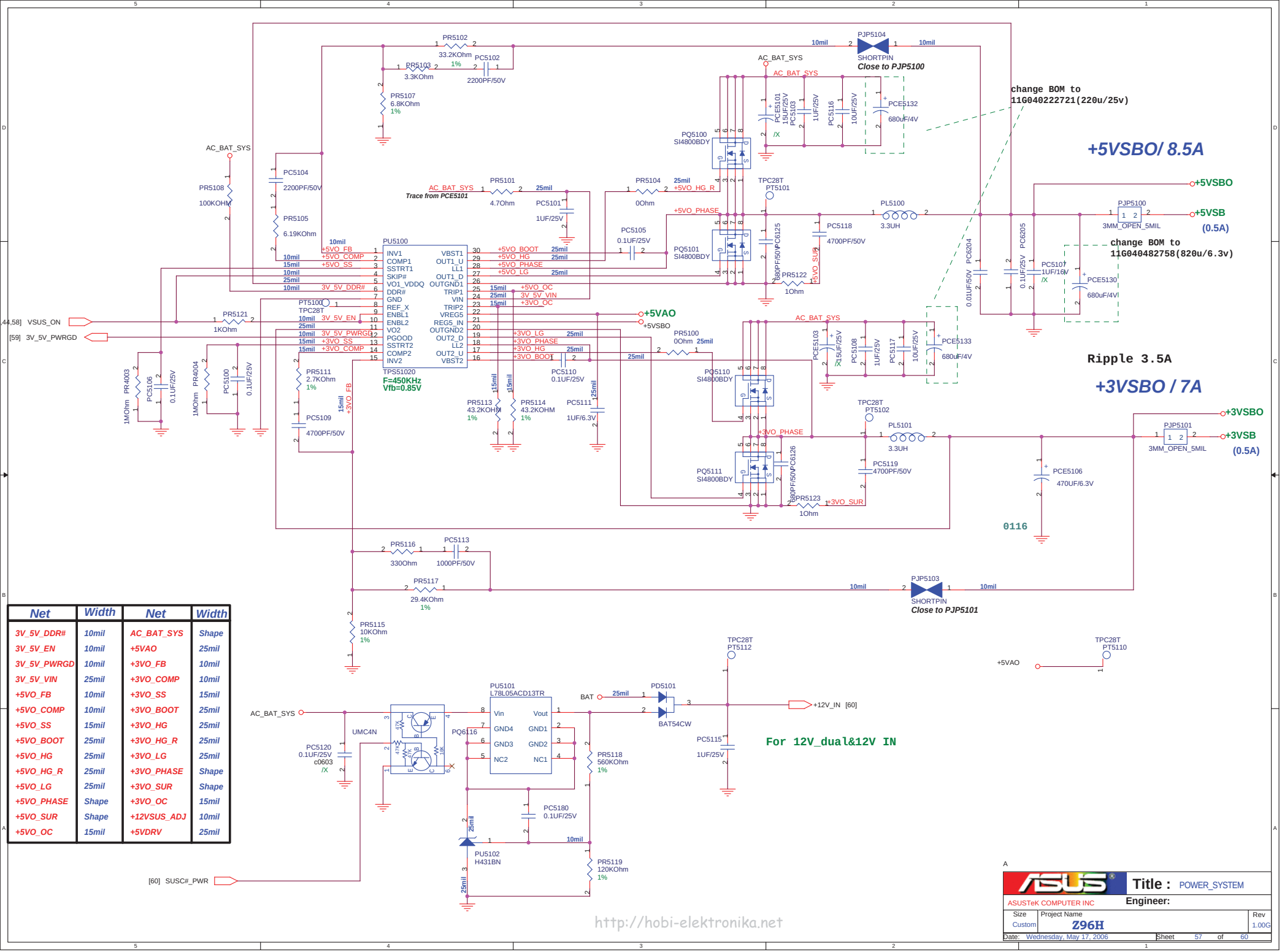
OCP Set : PR5030

AC Transient : PC5028 & PC5029

Loadline Droop : PR5050 & PR5049

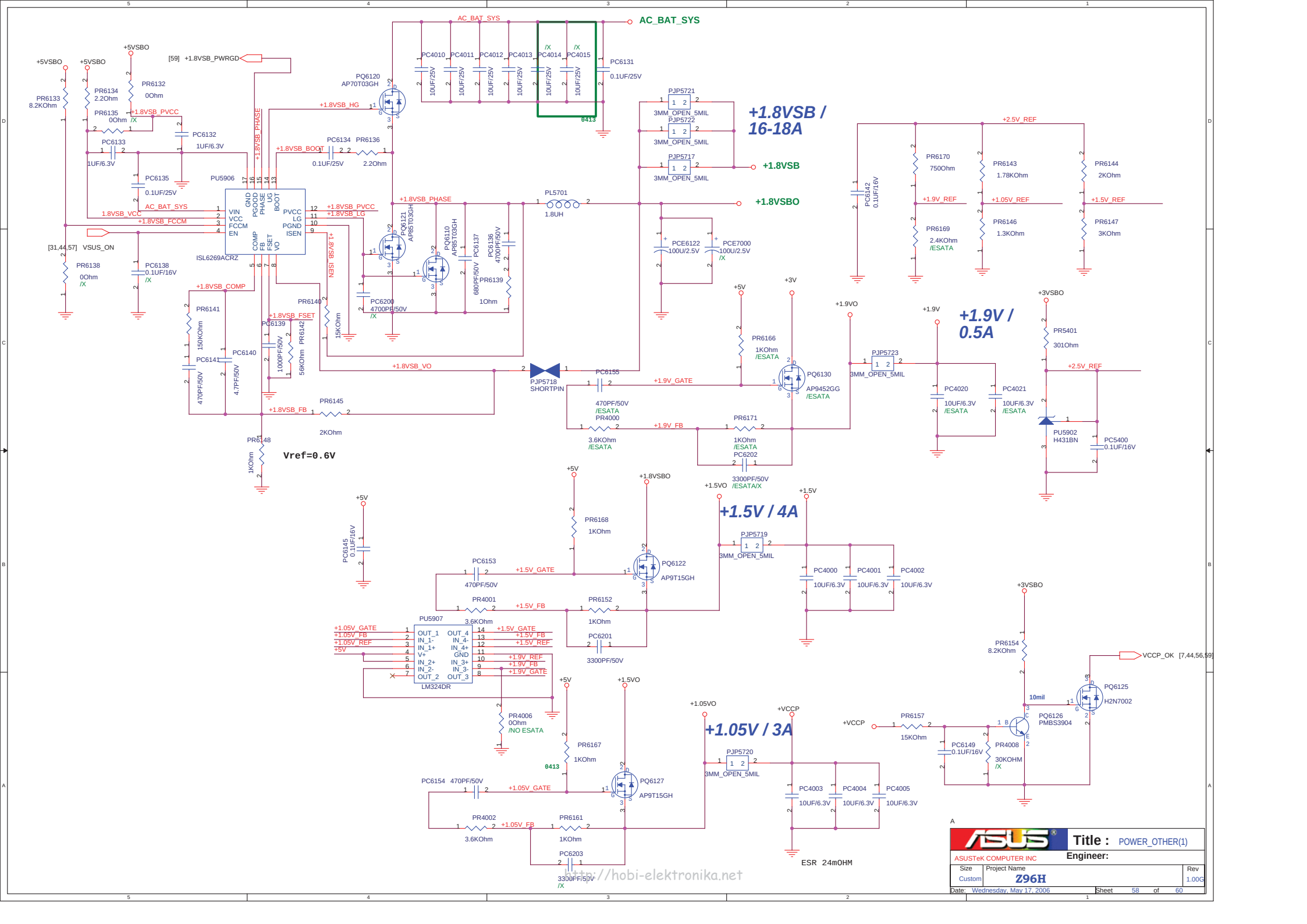
Put PJP5000 & PJP5001 close to CPU

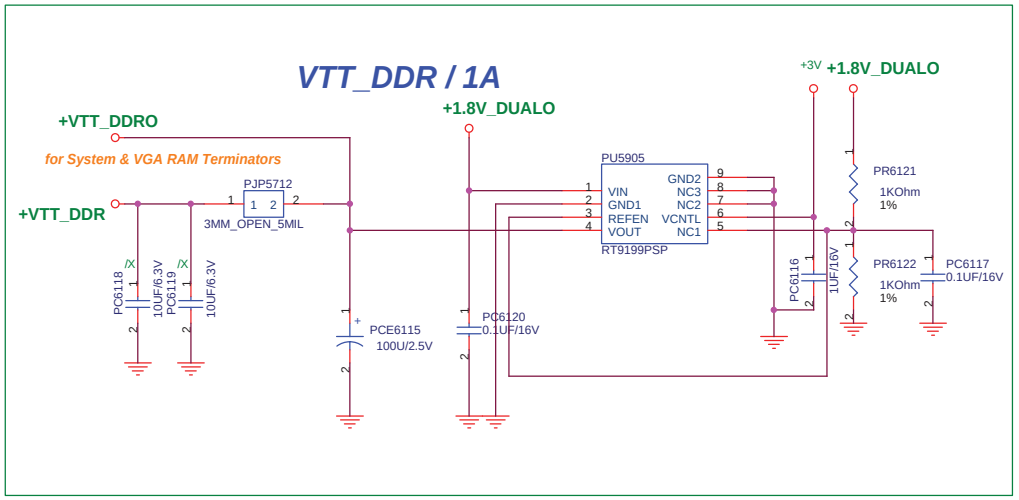
Title :	POWER_VCORE		
ASUSTeK COMPUTER INC	Engineer:		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 56 of 60		

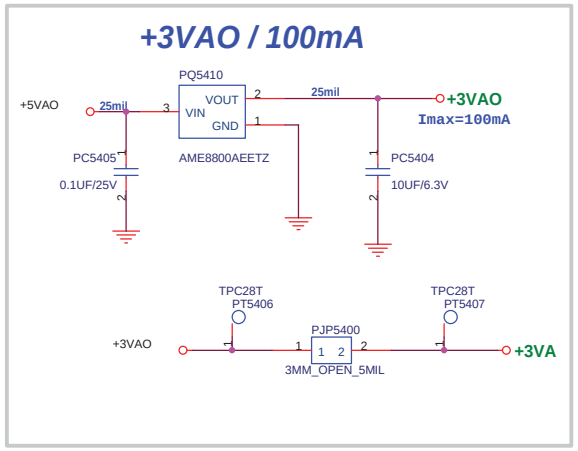


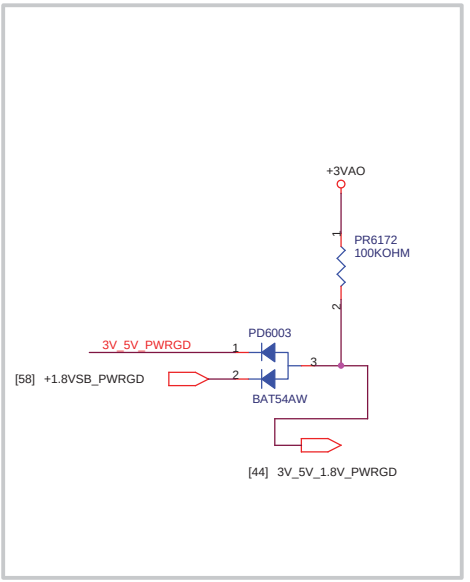
Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_HG	25mil
+5VO_SS	15mil	+3VO_BOOT	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

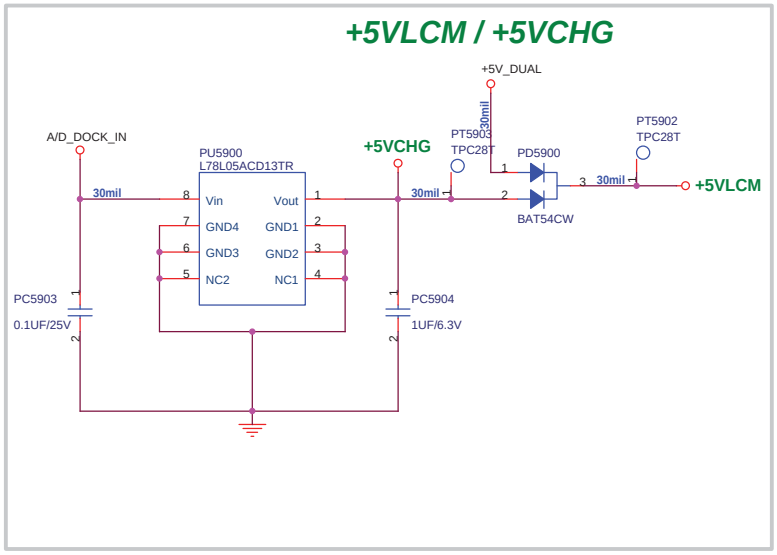
Title :	POWER_SYSTEM
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 57 of 60

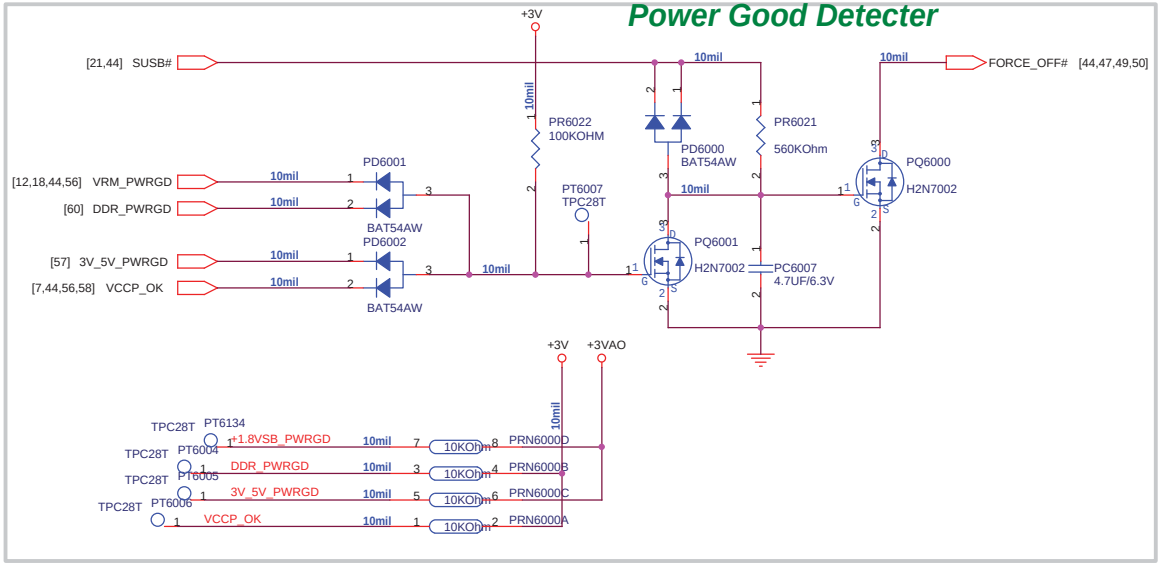

AC_BAT_SYS
+1.8VSB / 16-18A
+1.8VSB
+1.8VSBO
+1.9V / 0.5A
+1.5V / 4A
+1.05V / 3A
ESR 24mOHM
Vref=0.6V
ISL6269ACRZ
LM324DR
PU5906
PU5907
PU5902 H431BN
PJP5718 SHORTPIN
PQ6120 AP70T03GH
PQ6121 AP85T03GH
PQ6110 AP85T03GH
PQ6130 AP9452GG /ESATA
PQ6122 AP9T15GH
PQ6127 AP9T15GH
PQ6125 H2N7002
PQ6126 PMBS3904
PL5701 1.8UH
PJP5721 3MM_OPEN_5MIL
PJP5722 3MM_OPEN_5MIL
PJP5717 3MM_OPEN_5MIL
PJP5723 3MM_OPEN_5MIL
PJP5719 3MM_OPEN_5MIL
PJP5720 3MM_OPEN_5MIL
[59] +1.8VSB_PWRGD
VCCP_OK [7,44,56,59]
ASUSTeK COMPUTER INC
Title : POWER_OTHER(1)
Engineer:
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 58 of 60
http://hobi-elektronika.net



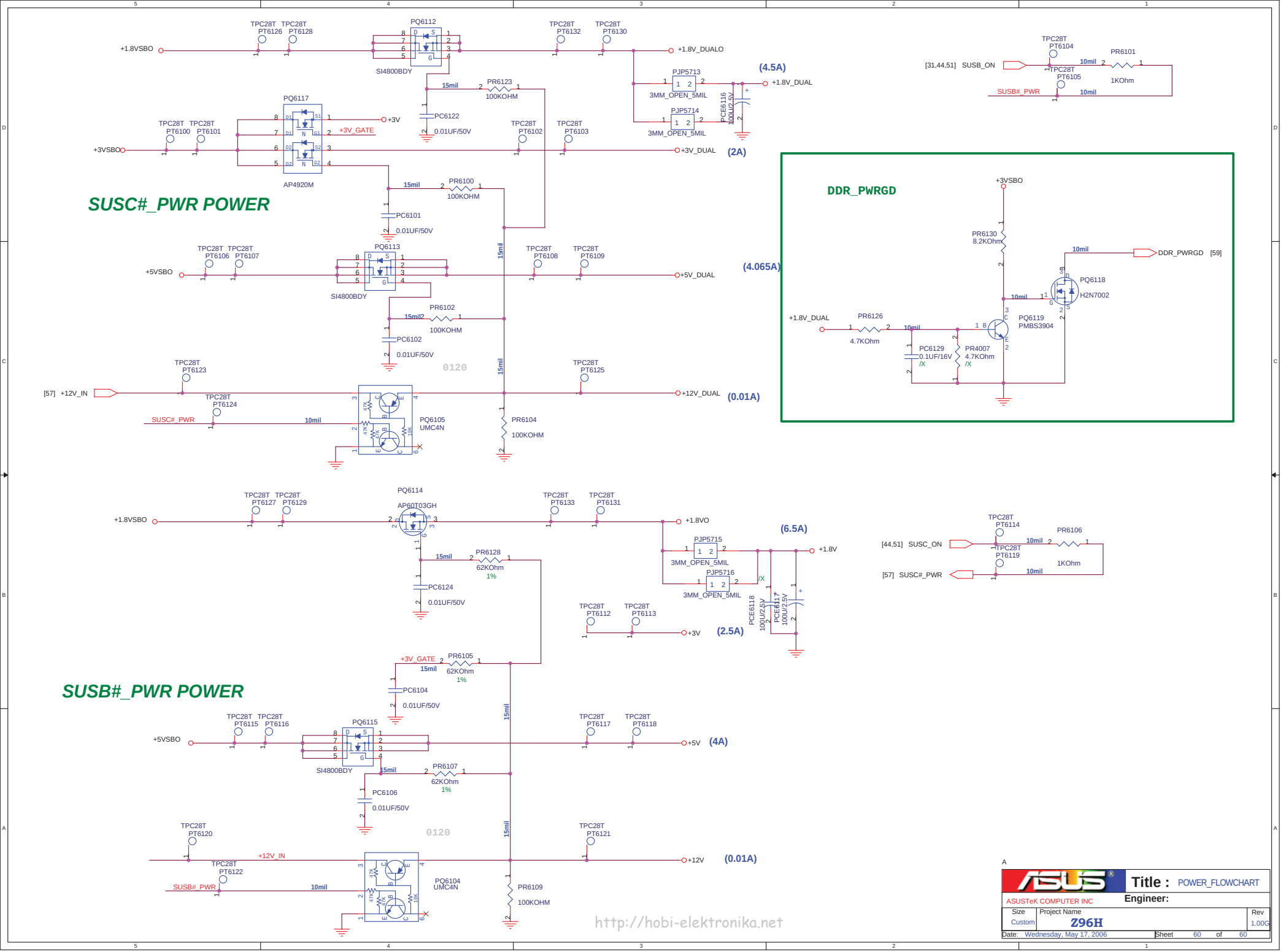








ASUSTeK COMPUTER INC	Title : POWER_OTHER(2)	
	Engineer:	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 59 of 60	


SUSC#_PWR POWER
+1.8VSBO
TPC28T PT6126
TPC28T PT6128
PQ6112
SI4800BDY
TPC28T PT6132
TPC28T PT6130
+1.8V_DUALO
(4.5A)
PJP5713
3MM_OPEN_5MIL
+1.8V_DUAL
PJP5714
3MM_OPEN_5MIL
PCE6116
100U/2.5V
PR6123
100KOHM
15mil
PC6122
0.01UF/50V
PQ6117
AP4920M
+3V
+3V_GATE
TPC28T PT6100
TPC28T PT6101
TPC28T PT6102
TPC28T PT6103
+3VSBO
+3V_DUAL
(2A)
PR6100
100KOHM
PC6101
0.01UF/50V
PQ6113
SI4800BDY
TPC28T PT6106
TPC28T PT6107
TPC28T PT6108
TPC28T PT6109
+5VSBO
+5V_DUAL
(4.065A)
PR6102
100KOHM
PC6102
0.01UF/50V
0120
TPC28T PT6123
TPC28T PT6124
TPC28T PT6125
[57] +12V_IN
+12V_DUAL
(0.01A)
SUSC#_PWR
10mil
PQ6105
UMC4N
PR6104
100KOHM
[31,44,51] SUSB_ON
TPC28T PT6104
TPC28T PT6105
PR6101
10mil
1KOhm
SUSB#_PWR
DDR_PWRGD
+3VSBO
PR6130
8.2KOhm
10mil
DDR_PWRGD [59]
PQ6118
H2N7002
+1.8V_DUAL
PR6126
4.7KOhm
PQ6119
PMBS3904
PC6129
0.1UF/16V
/X
PR4007
4.7KOhm
/X
SUSB#_PWR POWER
PQ6114
AP60T03GH
+1.8VSBO
TPC28T PT6127
TPC28T PT6129
TPC28T PT6133
TPC28T PT6131
+1.8VO
(6.5A)
PJP5715
3MM_OPEN_5MIL
PJP5716
3MM_OPEN_5MIL
+1.8V
PCE6118
100U/2.5V
PCE6117
100U/2.5V
TPC28T PT6112
TPC28T PT6113
+3V
(2.5A)
PR6128
62KOhm
1%
PC6124
0.01UF/50V
+3V_GATE
PR6105
62KOhm
1%
PC6104
0.01UF/50V
PQ6115
SI4800BDY
TPC28T PT6115
TPC28T PT6116
TPC28T PT6117
TPC28T PT6118
+5VSBO
+5V
(4A)
PR6107
62KOhm
1%
PC6106
0.01UF/50V
0120
TPC28T PT6120
TPC28T PT6122
TPC28T PT6121
+12V_IN
SUSB#_PWR
10mil
PQ6104
UMC4N
PR6109
100KOHM
+12V
(0.01A)
[44,51] SUSC_ON
[57] SUSC#_PWR
TPC28T PT6114
TPC28T PT6119
PR6106
10mil
1KOhm
http://hobi-elektronika.net
Title : POWER_FLOWCHART
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
Z96H
Rev
1.00G
Date: Wednesday, May 17, 2006
Sheet 60 of 60