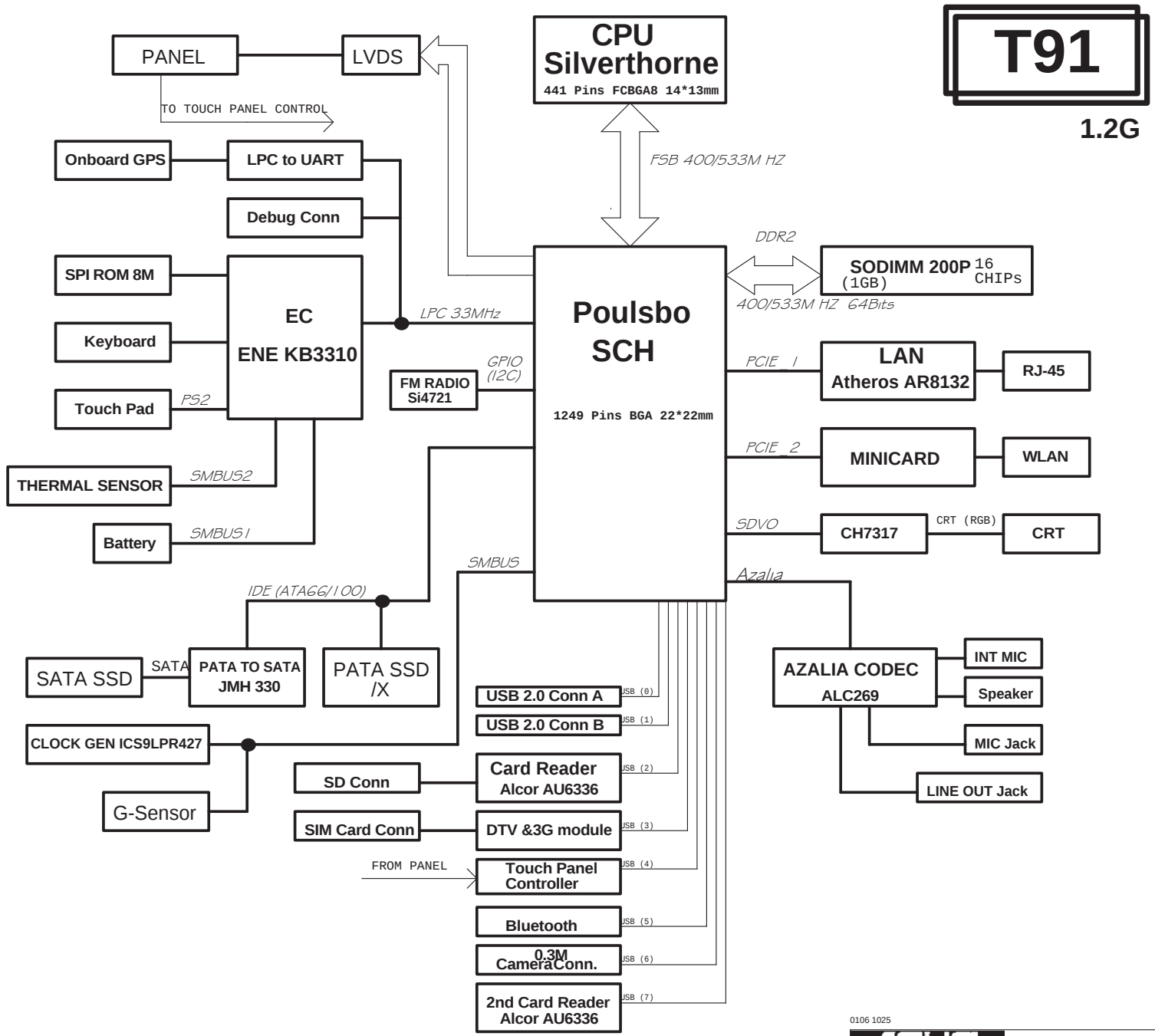


01_BLOCK DIAGRAM
02_SCH GPIO Setting
03_EC Pin Define
04_Power Sequense DC
05_Power Sequence AC
06_Power Sequence Description
07_Clock Gen_ICS9LPR427
08_CPU-SILVERTHORNE (1)
09_CPU-SILVERTHORNE (2)
10_CPU-SILVERTHORNE (3)
11_SCH_Poulsbo_HOST (1)
12_SCH_Poulsbo_DDR2 (2)
13_SCH_Poulsbo_LVDS/SDVO (3)
14_SCH_Poulsbo_PM/USB/IDE/AZ (4)
15_SCH_Poulsbo_STRAP(5)
16_SCH_Poulsbo_POWER (6)
17_SCH_Poulsbo_GND (7)
18_DDR2_SODIMM
19_DDR2_Termination
20_CH7317_SDVO_CRT
21_Onboard VGA
22_LCD Conn_LID
23_PCIEx 3.5G & Ext. Antenna
24_Mini WIFI / BT
25_Bluetooth_BT253
26_FM_RADIO_Si4721
27_Onboard GPS
28_LAN_Atheros AR8113/AR8132
29_RJ45
30_Flash Conn
31_PATA_TO_SATA
32_USB Port
33_Card Reader_AU6336C52
34_Camera Conn
35_Codec_ALC269
36_Audio Amp Jack
37_EC_ENE KB3310
38_EC_UART Contoller
39_SPI ROM_Debug Conn
40_Reset Map
41_KB_Touch Pad
42_Thermal Sensor
43_Small Board_Conn
44_G-Sensor
45_Discharge
46_PWR Jack
47_SCREW HOLE
48_EMI
49_Power Flow
50_Vcore
51_Power System
52_Power_+1.8V & VTTDDR
53_Power_VCCP
54_Power_+1.5VS & +2.5VS
55_Power_Charger
56_Power_Load Switch
57_Power Latch



SCH GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIO_SUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIO_SUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
N45	GPIO_SUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIO_SUS3/ USBCC	Test Point	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	PCB ID	I/O CMOS3.3	Core	OFF	OFF	Input
F34	GPIO2	GPS_EN	I/O CMOS3.3	Core	OFF	OFF	Output
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPI_OVR#	SLPI_OVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

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ASUS		Title : SCH GPIO Setting	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size	Project Name		Rev
A3	T91		1.2G
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EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	BUF_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Battery over temperature
15	GPIO08	EXT_SM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	Reserved for GPIO extender
18	GPIO0C/ESB_DAT	NC	O	Reserved for GPIO extender
19	GPIO0D	LID_EC_R#	I	Internal pull high
20	GPIO0E/SCI#	KBC_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GP138/AD0	BAT_A	I	
64	GP139/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

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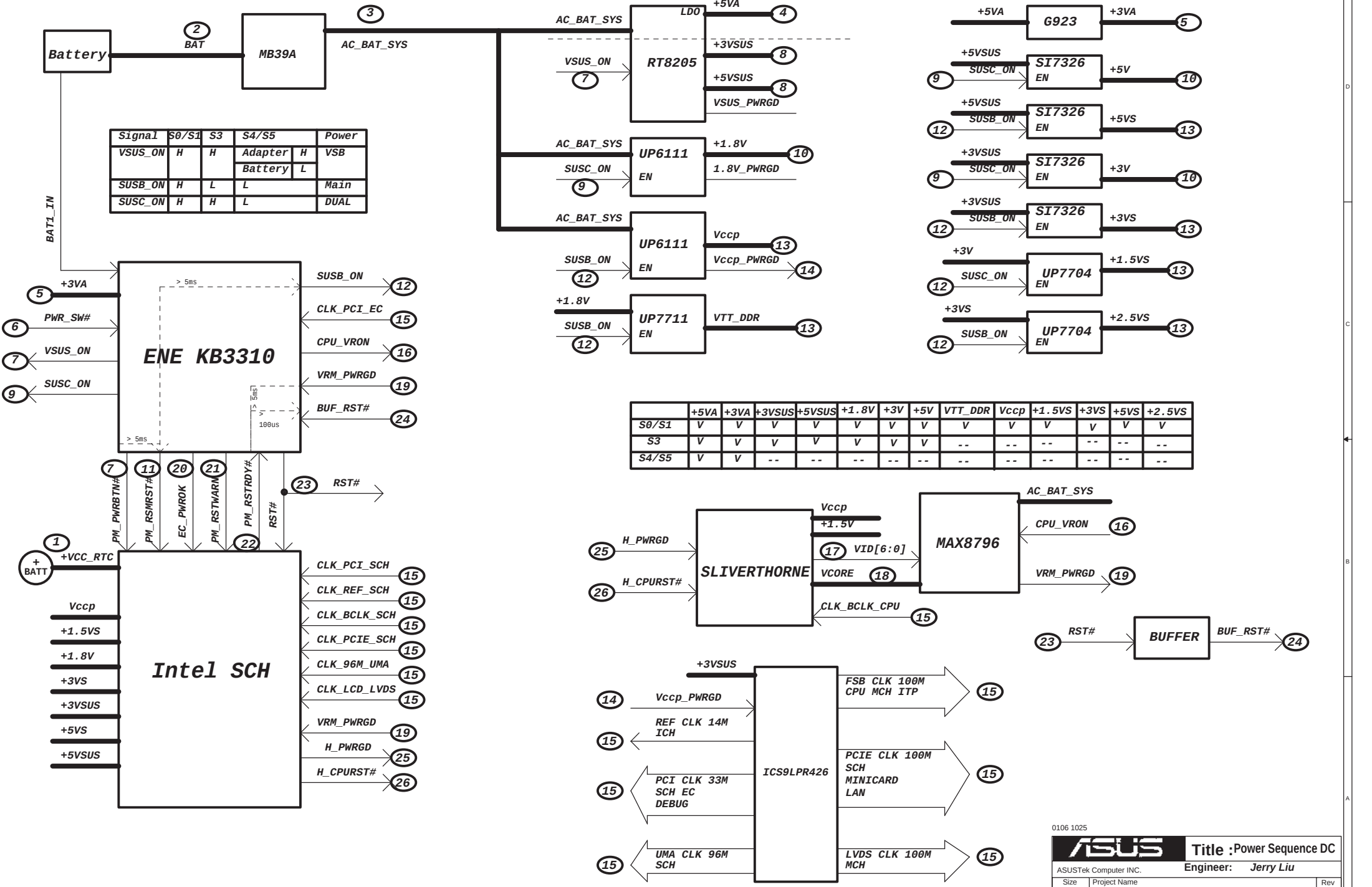
Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GP142	BAT_IN	I	Batt1 (Small/Internal): 1-present, 0-absent
76	GP143	BAT2_IN	I	Batt2 (Small/Internal): 1-present, 0-absent
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	N.C.	O	
85	GPIO4C/PSCLK2	N.C.	O	
86	GPIO4D/PSDAT2	GS2_INT2	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLLED	SCRL_LED#	O	
95	GPIO56	GS1_INT1	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPXOA06	CNT1_DIS#	O	batt1 discharging enabled
104	GPXOA07	CNT2_CHG#	O	batt2 (Small/Internal) charging enabled. Batt2 is charging priority in AC mode.
105	GPXOA08	CNT2_CHG#	O	batt2 discharging enabled
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#,100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#,100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1	O	

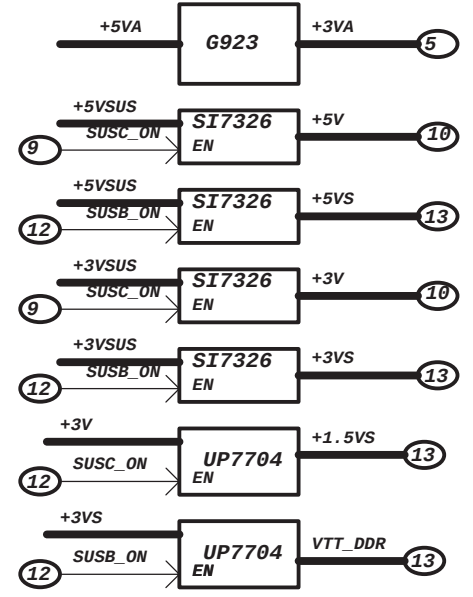
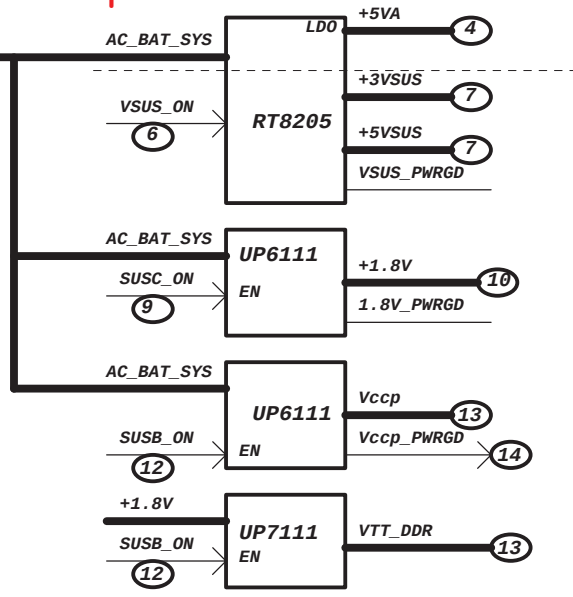
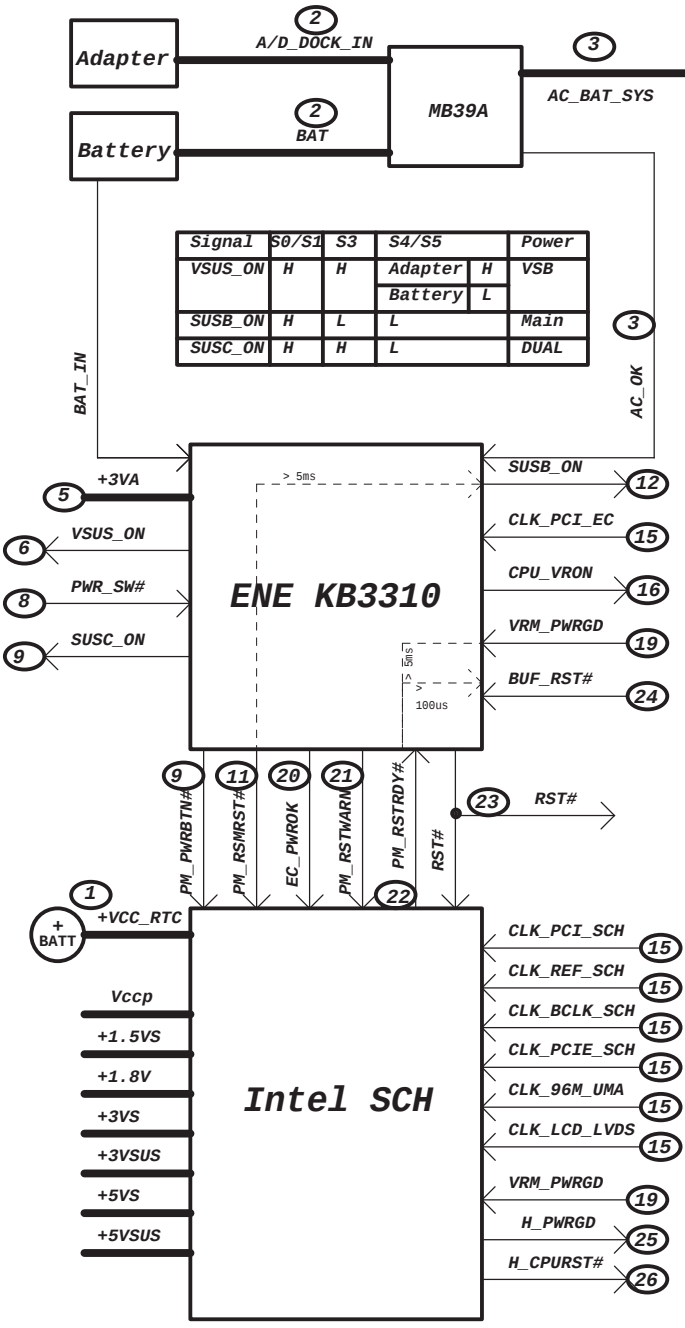
EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

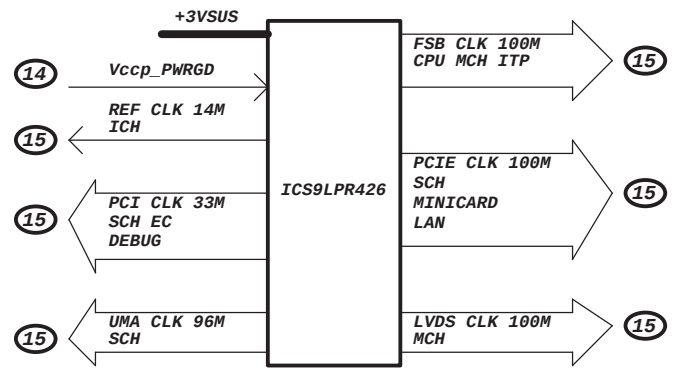
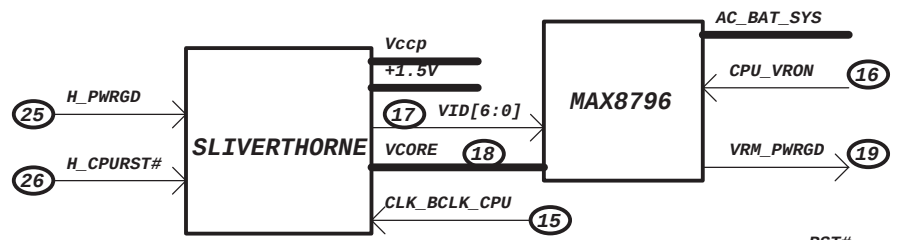
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ASUS		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A3	Project Name T91	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 3 of 57	





	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	V	V	--	--	--	--	--	--	--	--	--



S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for AC_OK until adaptor power is good, then
- 2.At least **5mS** after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.
- 3.At least **20mS** after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)
- 4.EC asserts RSTWARN.
- 5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 6.PM_RSMRST# is deasserted at least **5mS** after SUSC power is stable.
- 7.At least **5mS** after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 8.CPU_VRON is deasserted at least **100mS** after SUSB power is stable.
- 9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 10.At least **10mS** after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 11.Waiting for RSTRDY# until deasserted by SCH.
- 12.RESET# can be deasserted at lease **100uS** after PM_PWROK is asserted.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

- 1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.
- 2.For external wake event (PWR_SW#, keyboard wake up), then
- 3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.
- 4.EC asserts SUSB_ON to enable SUSB power.
- 5.CPU_VRON is deasserted at least **100mS** after SUSB power is stable.
- 6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 7.At least **5mS** after receiving CPUPWR_GD, ICH_PWROK is asserted.
- 8.Deasserts RSTWARN after ICH_PWROK is asserted.
- 9.RESET# can be deasserted **100uS** after RSTWARN is deasserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for BAT_IN until battery power is good, then
- 2.Waiting for PWR_SW# until user is pressed.
- 3.EC asserts VSUS_ON to enable VSUS power.
- 4.At least **20mS** after VSUS power is stable.
- 5.EC asserts RSTWARN.
- 6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.
- 8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.
- 10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 12.Waiting for RSTRDY# until deasserted by SCH.
- 13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# for **1200uS** to SCH after asserts RSTWARN.
- 4.EC deasserts RSTWARN.
- 5.EC deasserts RESET# after at least **100uS** delay from RSTWARN.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

- 1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).
 - 2.At least 20mS after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.
 - 3.Waiting for SLPRDY# until has been asserted.
 - 4.EC asserts RSTWARN to SCH to begin internal sequence.
 - 5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.
 - 6.EC asserts RESET# after detecting RSTRDY# asserted.
 - 7.EC deasserts ICH_PWROK.
 - 8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.
- This completes the entry to S3 (SLPMODE=1).**
- If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:
- 9.EC asserts PM_RSMRST#.
 - 10.EC deasserts SUSC_ON to turn off the other power planes.
 - 11.EC deasserts VSUS_ON if in battery mode.
 - 12.EC deasserts RSTWARN to save more power.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

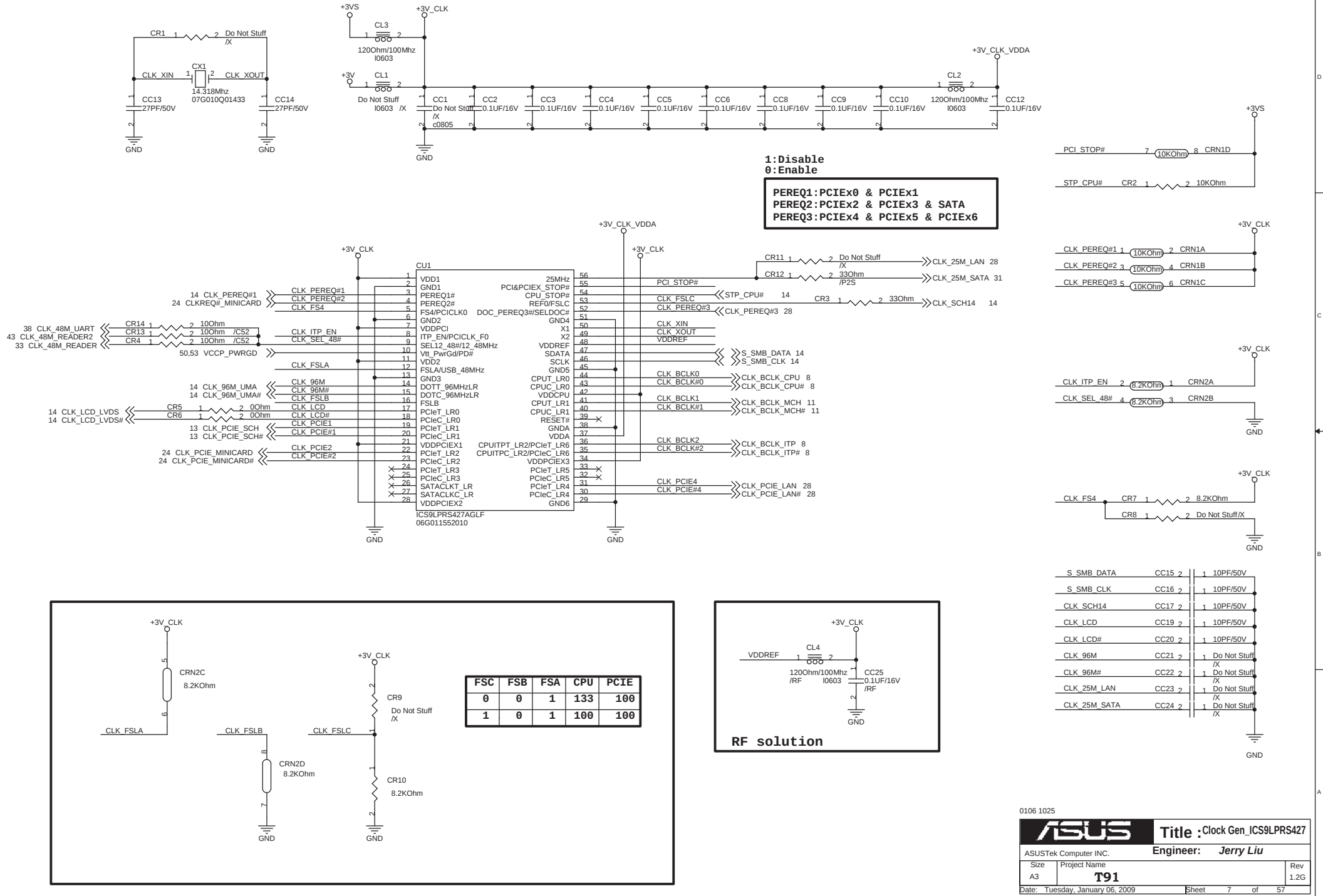
Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

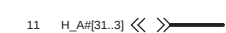
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# to SCH after asserts RSTWARN.
- 4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.
- 5.EC asserts PM_RSMRST# after CPU_VRON power is off.
- 6.EC disables SUSC_ON power for 3~5 seconds.
- 7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.

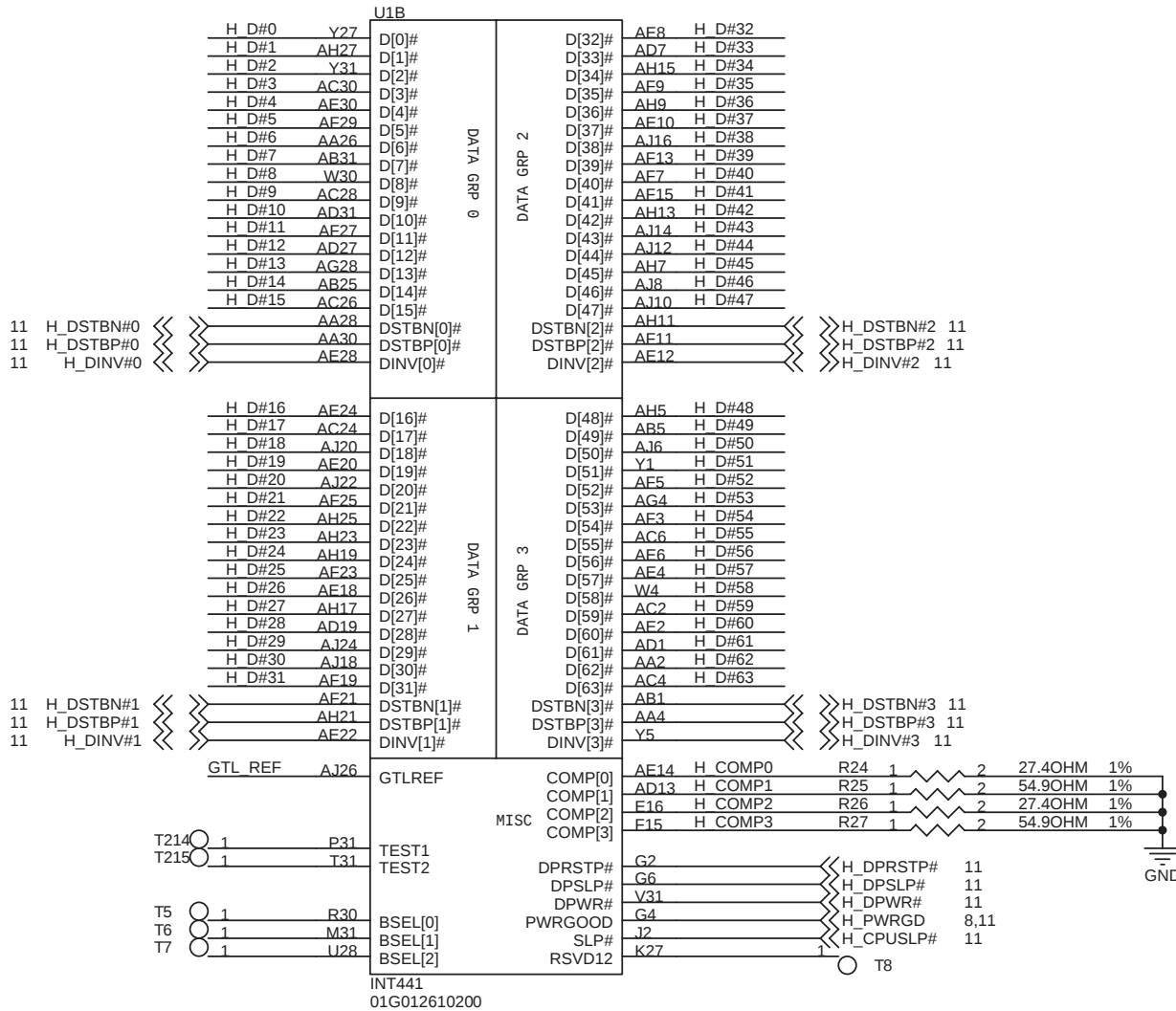
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Power Sequence Description

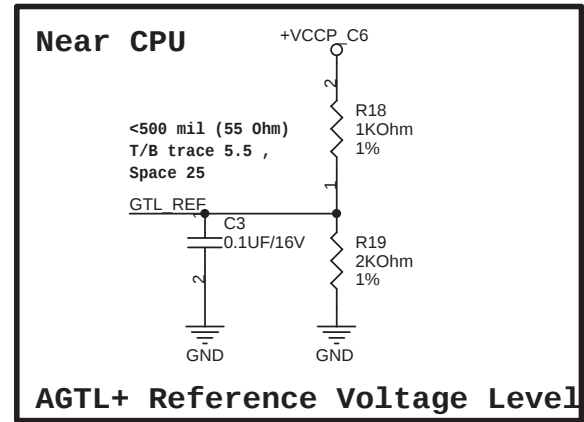
ASUS		Title :	
ASUSTek COMPUTER INC		Engineer: Jerry Liu	
Size	Project Name		Rev
Custom	T91		1.2G
Date: Tuesday, January 06, 2009		Sheet	6 of 57







H_D#[63:0] << >> H_D#[63:0] 11



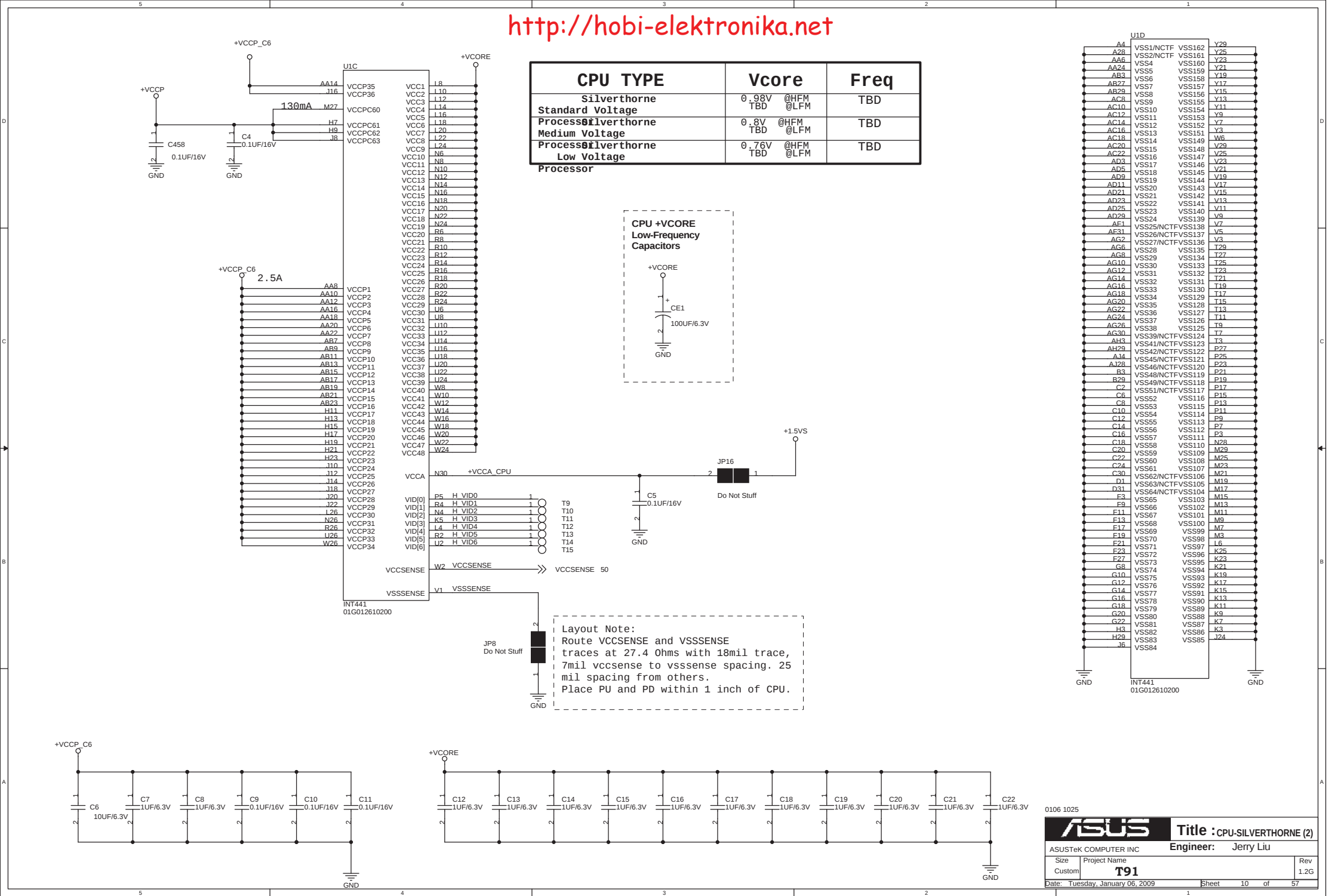
Layout Note

COMP 0 2 connect with Z0=27.4 ohm, L<0.5"

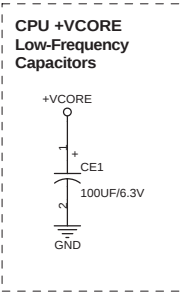
COMP 1 3 connect with Z0=55 ohm, L<0.5"

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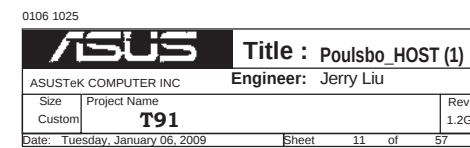
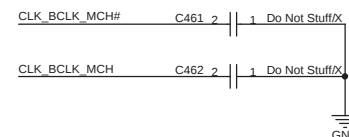
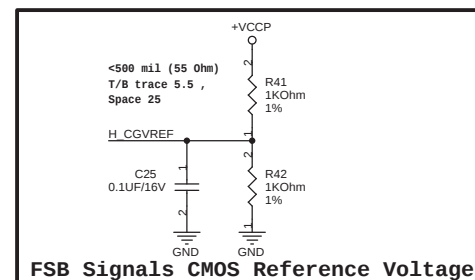
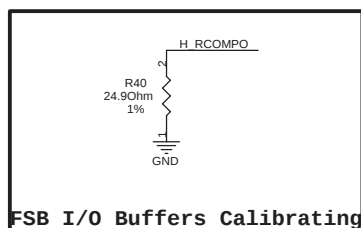
ASUS		Title : CPU-SLIVERTHORNE(1)	
ASUSTeK COMPUTER INC		Engineer: Jerry Liu	
Size A4	Project Name T91	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 9 of 57	



CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage	0.98V TBD @HFM @LFM	TBD
Processor Silverthorne Medium Voltage	0.8V TBD @HFM @LFM	TBD
Processor Silverthorne Low Voltage	0.76V TBD @HFM @LFM	TBD

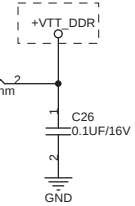
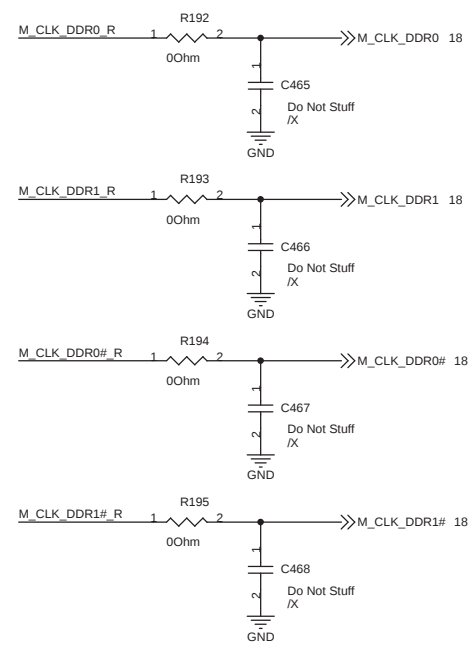
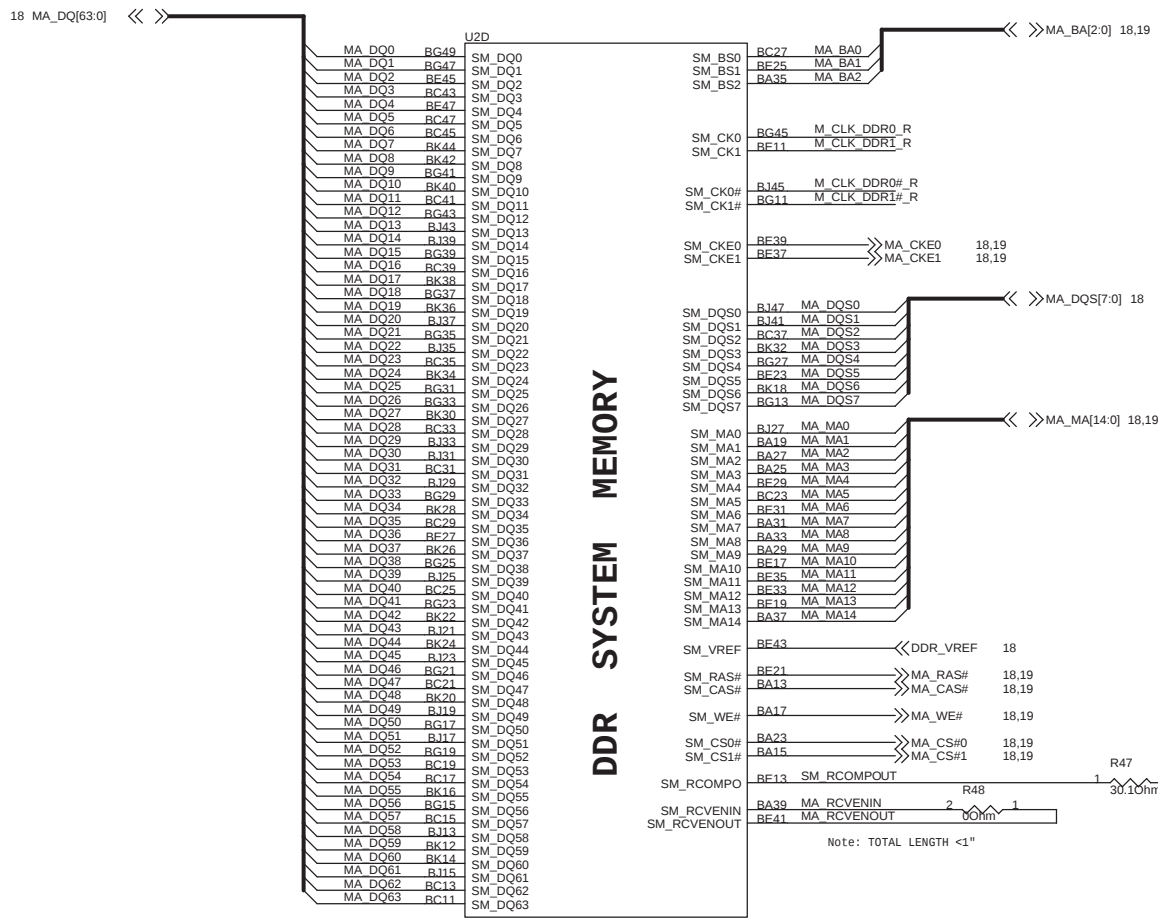


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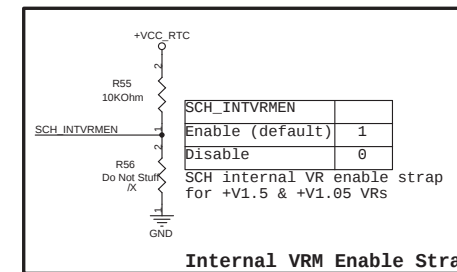
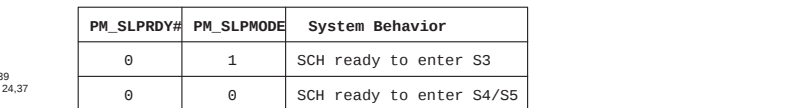
		Title : Poulsbo_HOST (1)	
ASUSTek COMPUTER INC		Engineer: Jerry Liu	
Size Custom	Project Name T91		Rev 1.2C
Date: Tuesday, January 06, 2009		Sheet	11 of 57



02G010018704

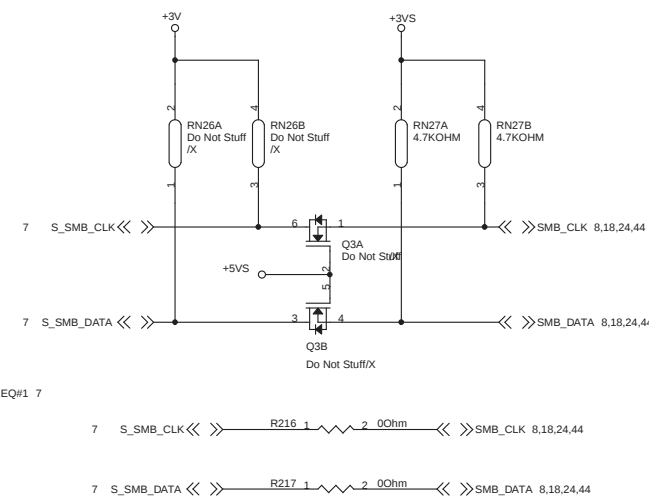
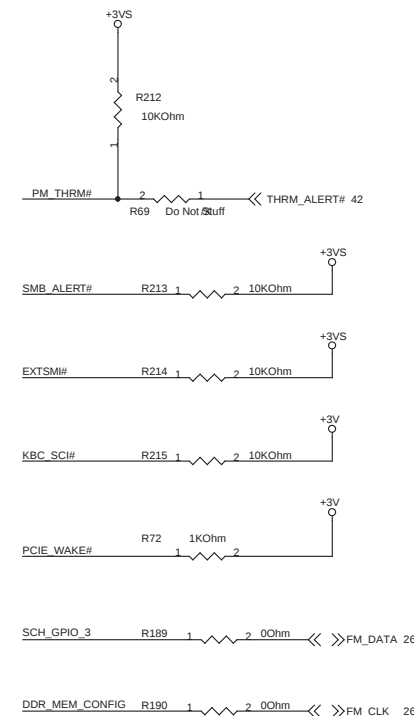
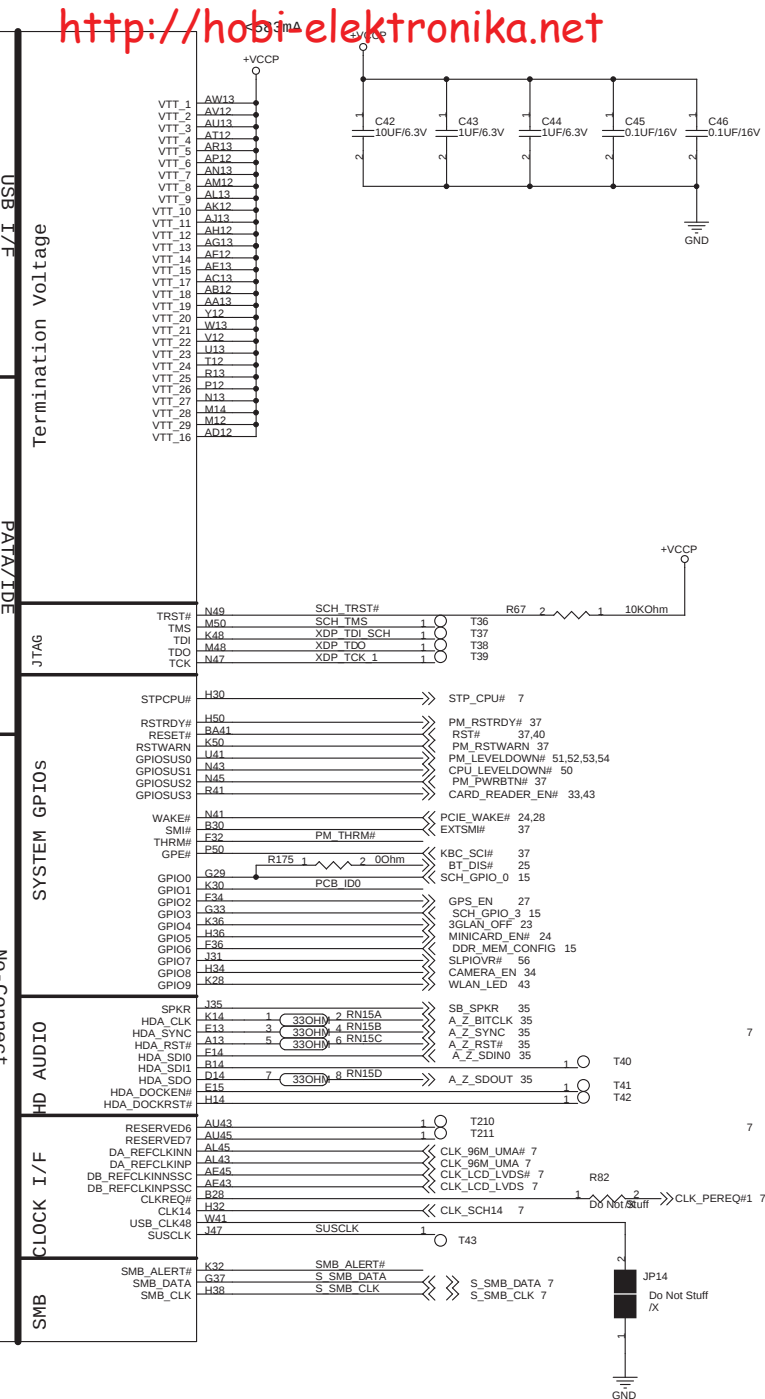
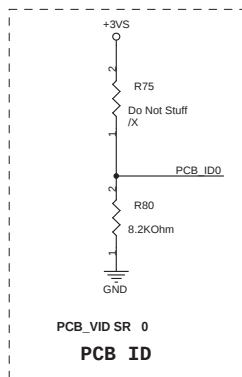
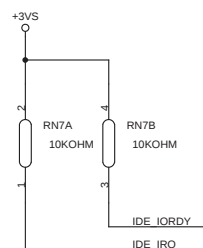
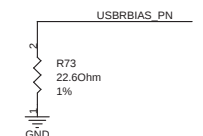
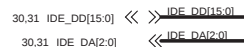
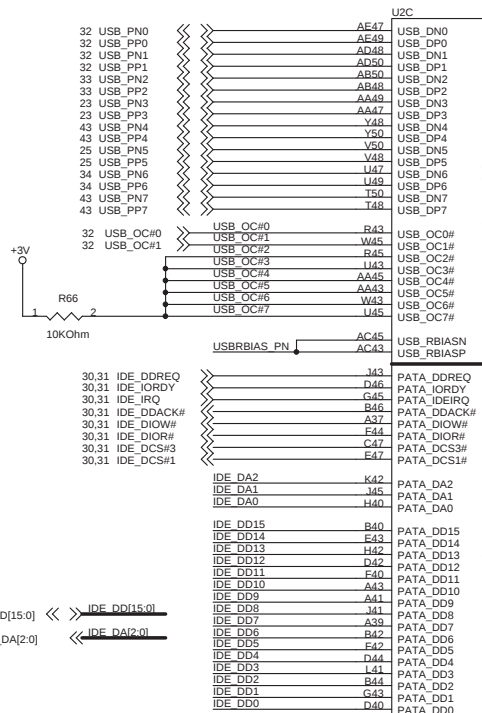
0106 1025

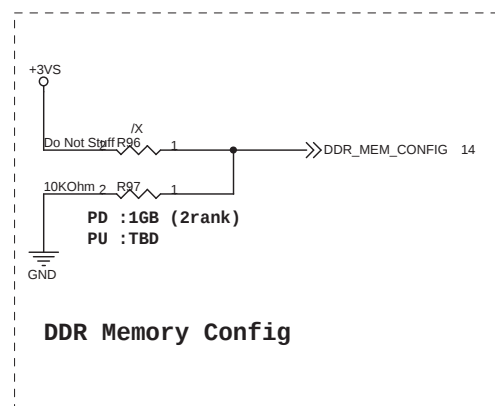
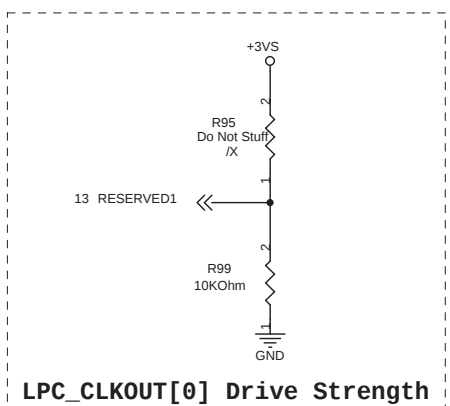
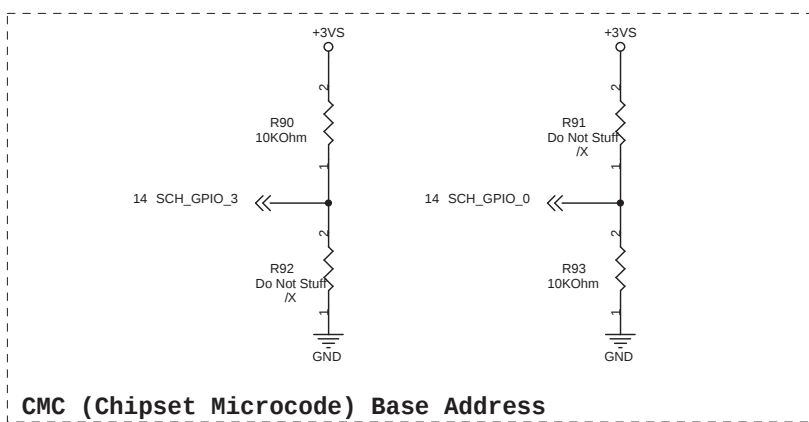
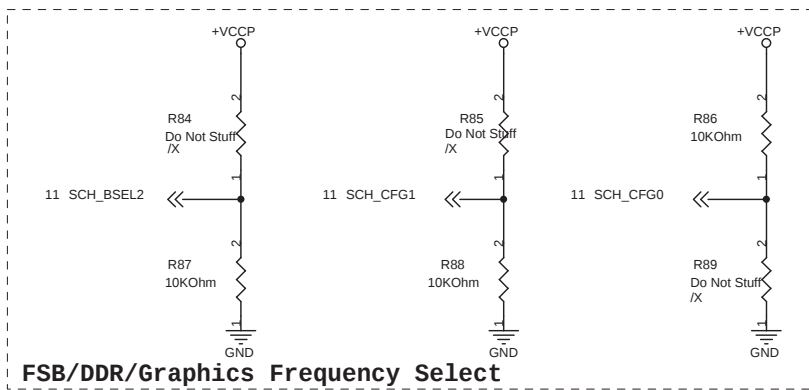
ASUS		Title : Poulsbo_DDR2 (2)	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size Custom	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet 12 of 57	



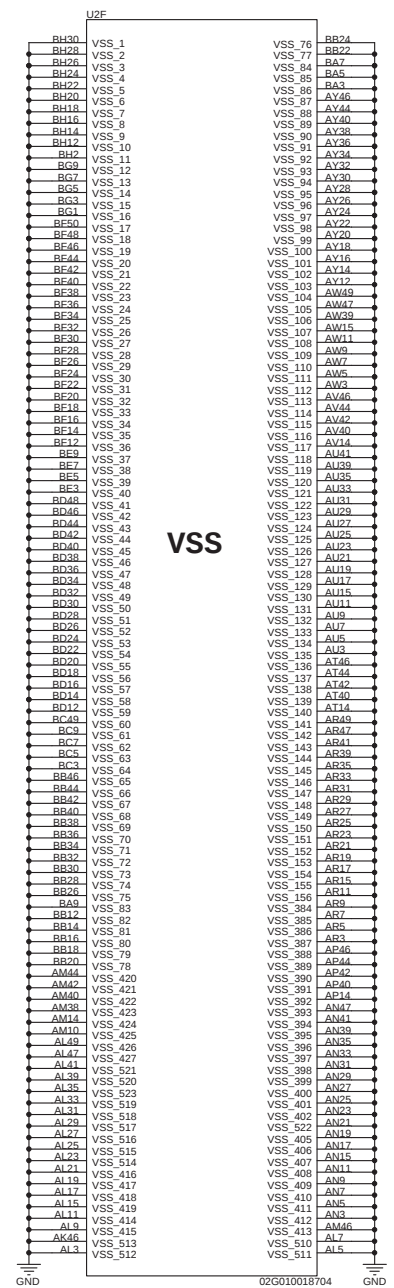
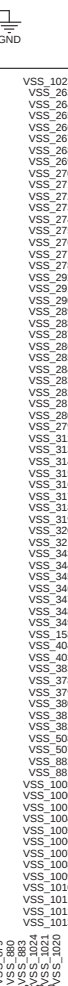
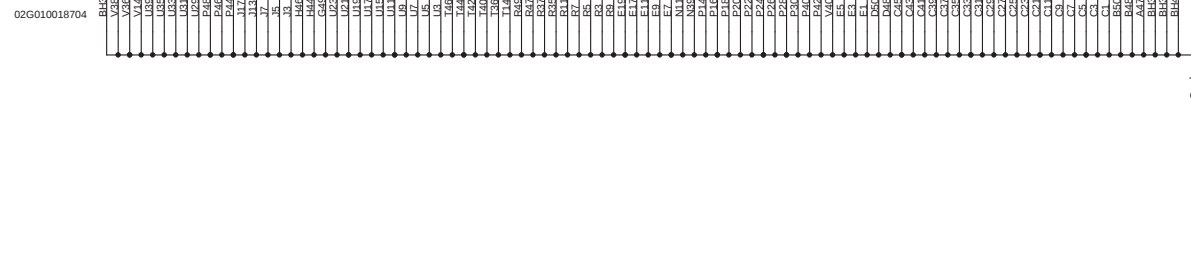
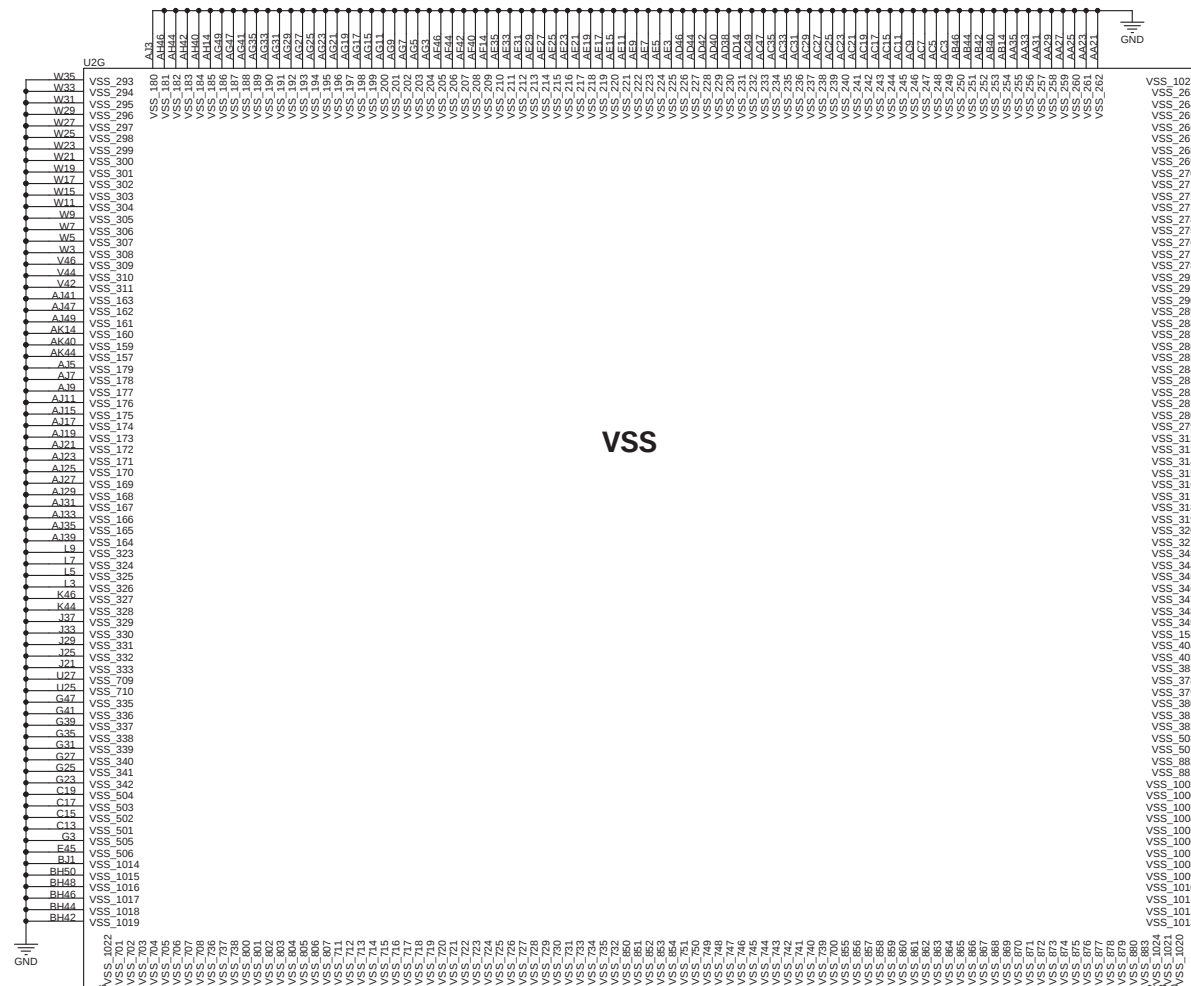
0106 1025		Poulsbo LVDS/SDVO	
		Title :	
ASUSTeK COMPUTER INC		Engineer: Jerry Liu	
Size Custom	Project Name T91	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 13 of 57	

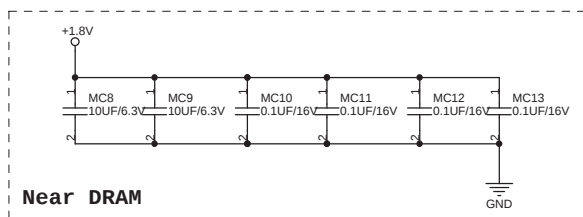
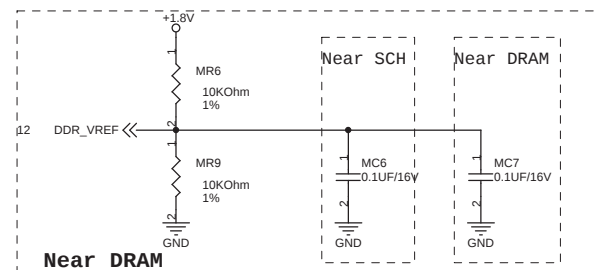
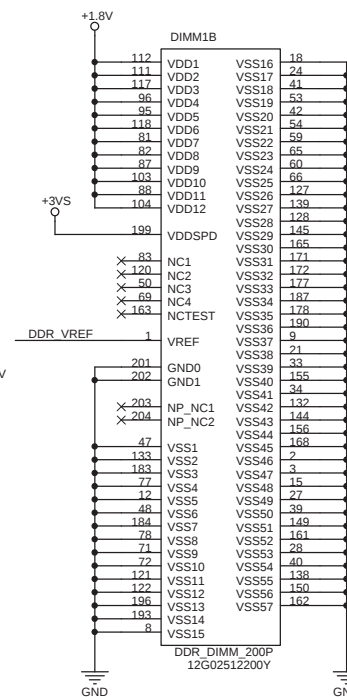
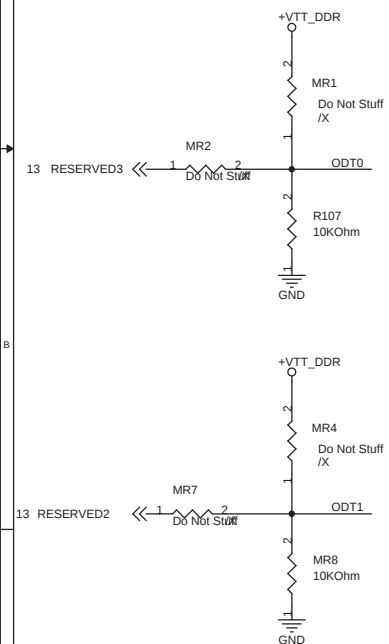
USB 0	USB PORT
USB 1	USB PORT
USB 2	Card Reader
USB 3	3.5G
USB 4	Touch Panel
USB 5	Bluetooth
USB 6	Camera
USB 7	2'nd Card Reader



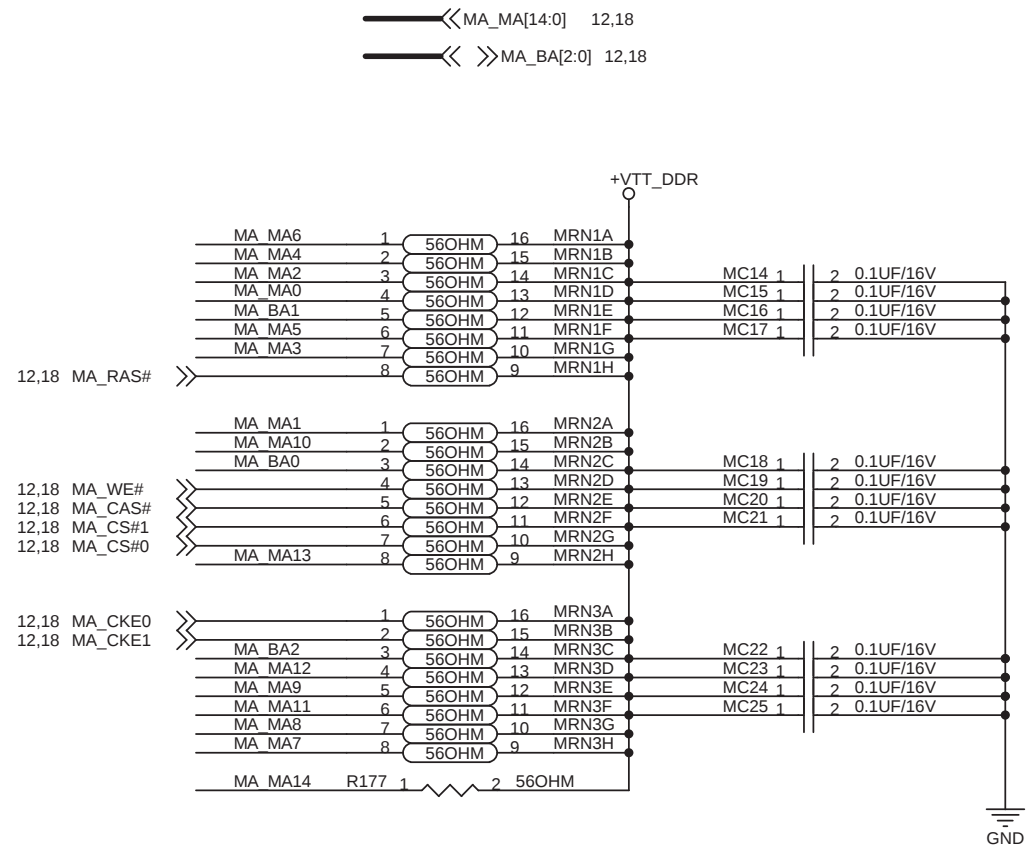


Strap Function	Singal Name			Strap		Comment
FSB/DDR Frequency Select Graphics Frequency Select	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed
	0	0	0	200	400	
	0	0	1	200	533	
CMC (Chipset Microcode) Base Address	GPIO3		GPIO0	Address		Selects the starting address that the CMC will use to start fetching code. (GPIO3 is the most significant)
	0		0	0xFFFFB0000		
	0		1	0xFFFFC0000		
	1		0	0xFFFFD0000 (default)		
	1		1	0xFFFFE0000		
LPC_CLKOUT[0] Buffer Strength	RESERVED1			Value		Selects the drive strength of the LPC_CLKOUT[0] clock.
	0			Reserved		
	0			1 Load (Default)		
	1			Reserved		
	1			2 Loads		



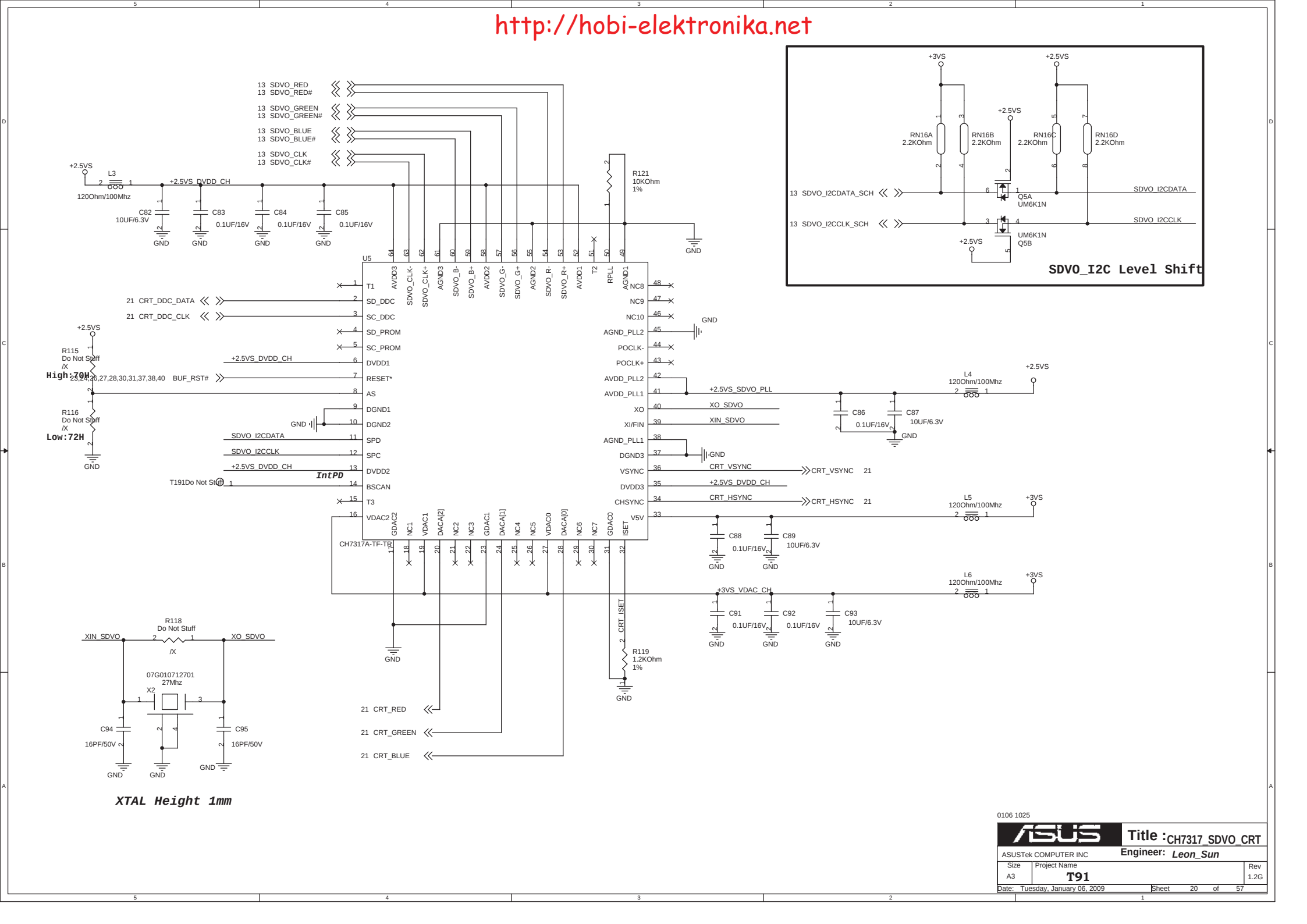


BOM use 12G02512200Y



0106 1025

ASUS		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91	Rev 1.2G	
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SDVO_I2C Level Shift

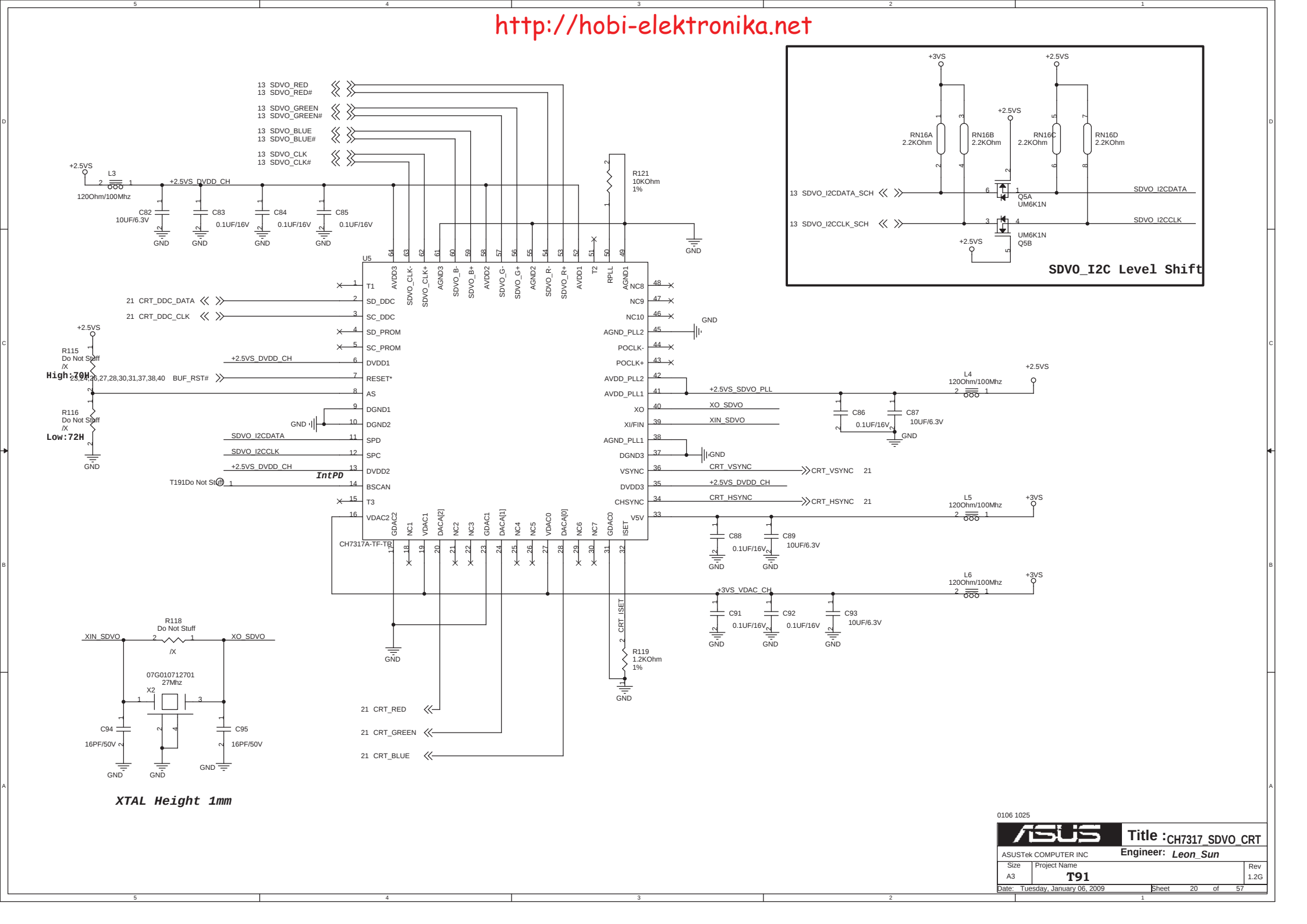
XTAL Height 1mm

ASUS Title :CH7317 SDVO CRT

ASUSTek COMPUTER INC Engineer: Leon Sun

Size A3 Project Name T91 Rev 1.2G

Date: Tuesday, January 06, 2009 Sheet 20 of 57



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SDVO_I2C Level Shift

The inset circuit shows the level shift for the SDVO_I2C signals. It uses two 2N7000 transistors (Q5A and Q5B) and resistors (RN16A, RN16B, RN16C, RN16D) to convert the 3V and 2.5V signals to the required levels for the SDVO_I2CDATA and SDVO_I2CCLK lines.

XTAL Height 1mm

The main circuit includes a crystal oscillator (X2, 27Mhz) and several capacitors (C82, C83, C84, C85, C86, C87, C88, C89, C91, C92, C93, C94, C95) for timing and decoupling.

ASUS

ASUSTek COMPUTER INC

Project Name: **T91**

Date: Tuesday, January 06, 2009

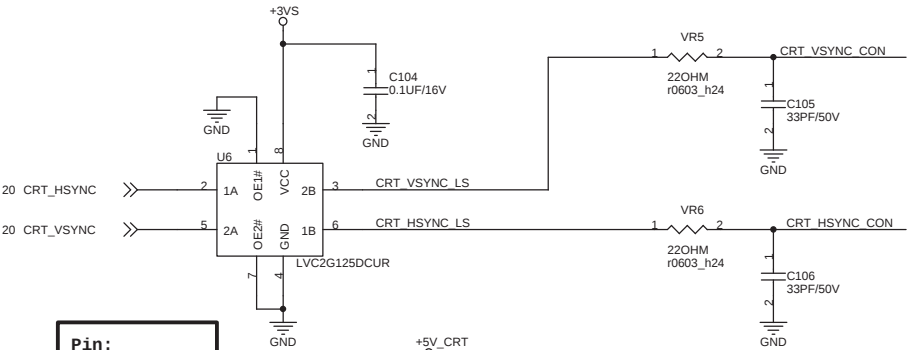
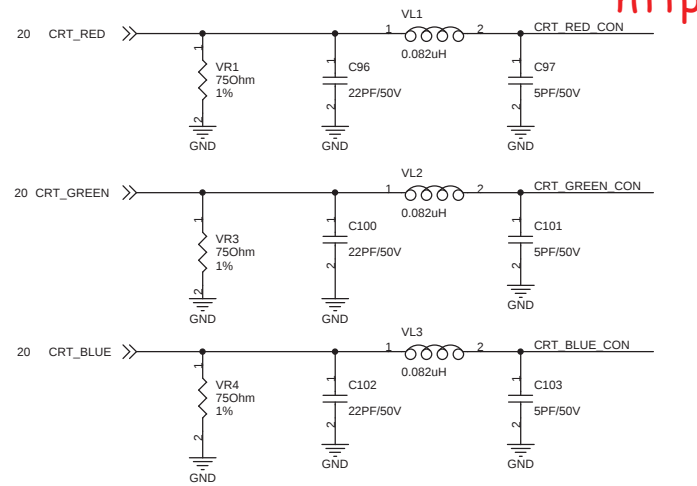
Sheet 20 of 57

Rev 1.2G

Engineer: **Leon Sun**

0106 1025

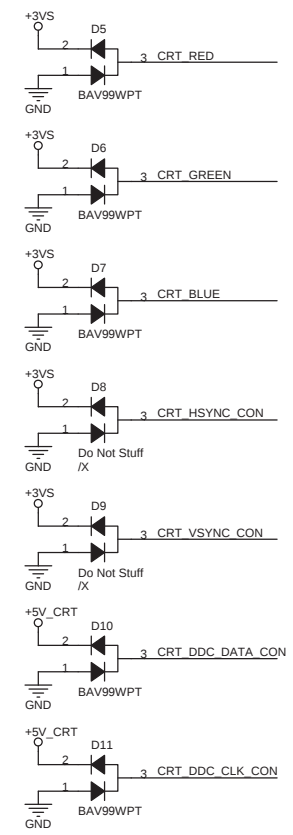
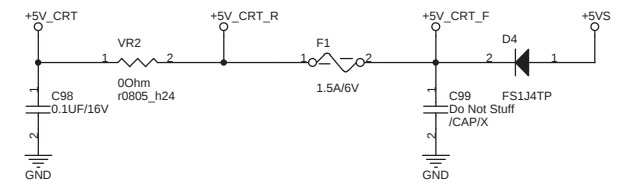
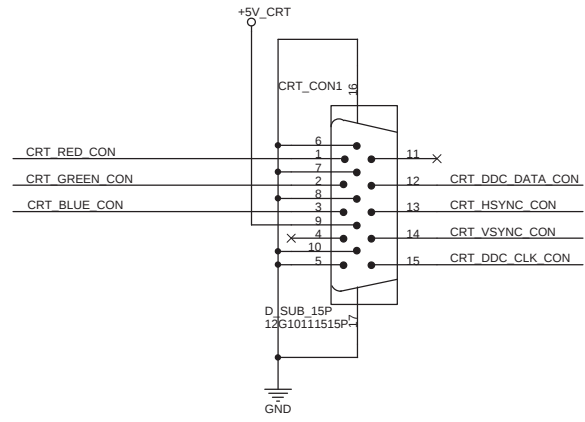
Title: **CH7317 SDVO CRT**

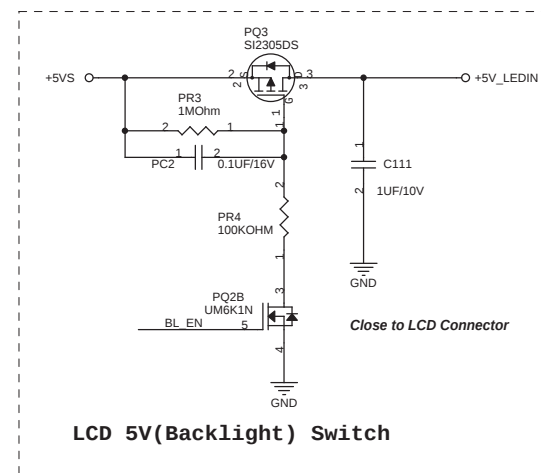
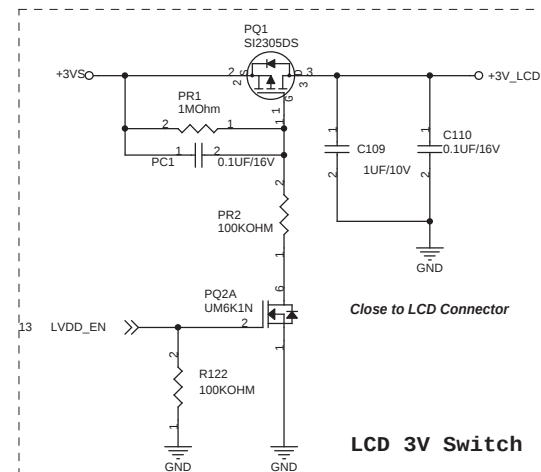
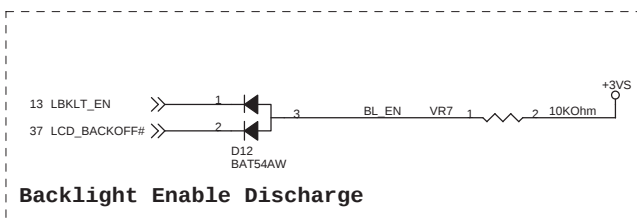
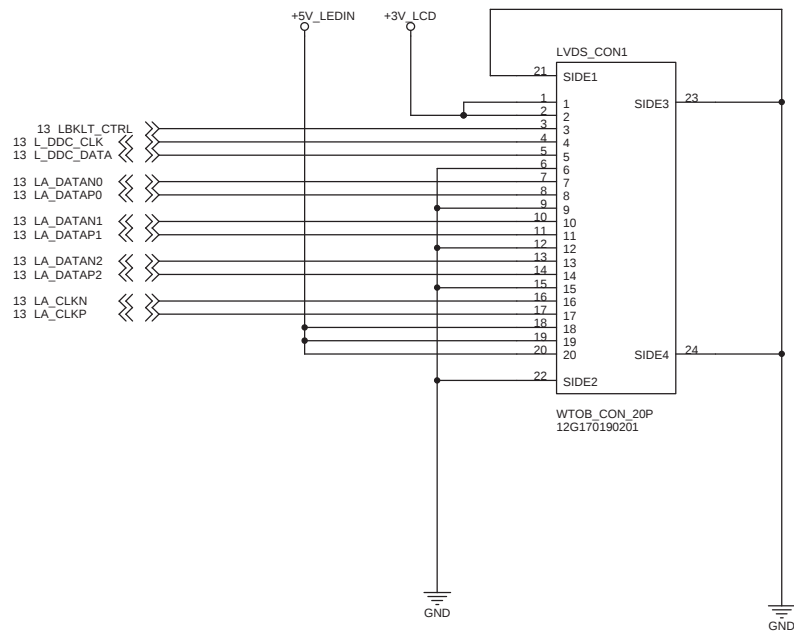
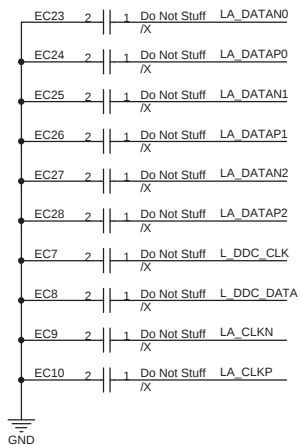


Pin:
2->6: (1A->1B)
5->3: (2A->2B)

C105 C106 for EA measurement
U6上:VR5 & VR6-->22 OHM
U6 /X :VR5 & VR6 -->0 OHM

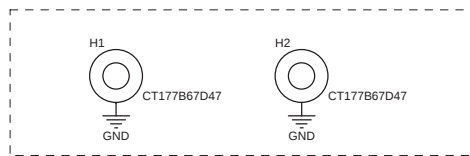
BUS BUFFER:
Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.





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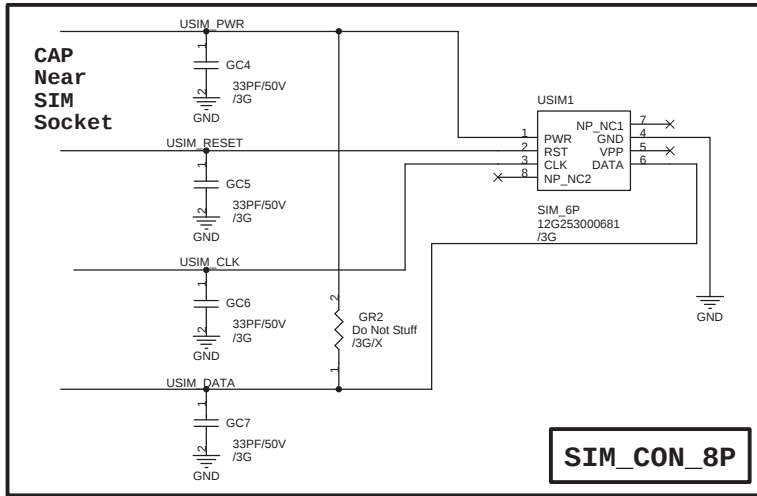
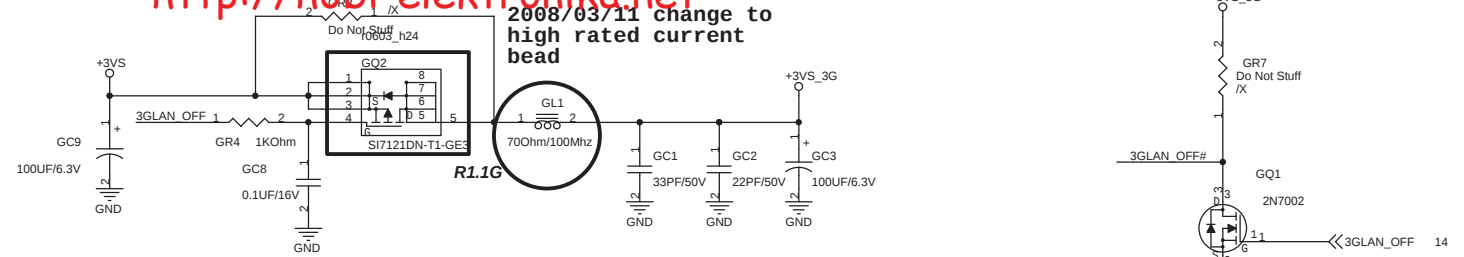
ASUS		Title : LVDS Conn	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size	Project Name		Rev
A3	T91		1.2G
Date: Tuesday, January 06, 2009		Sheet 22 of 57	



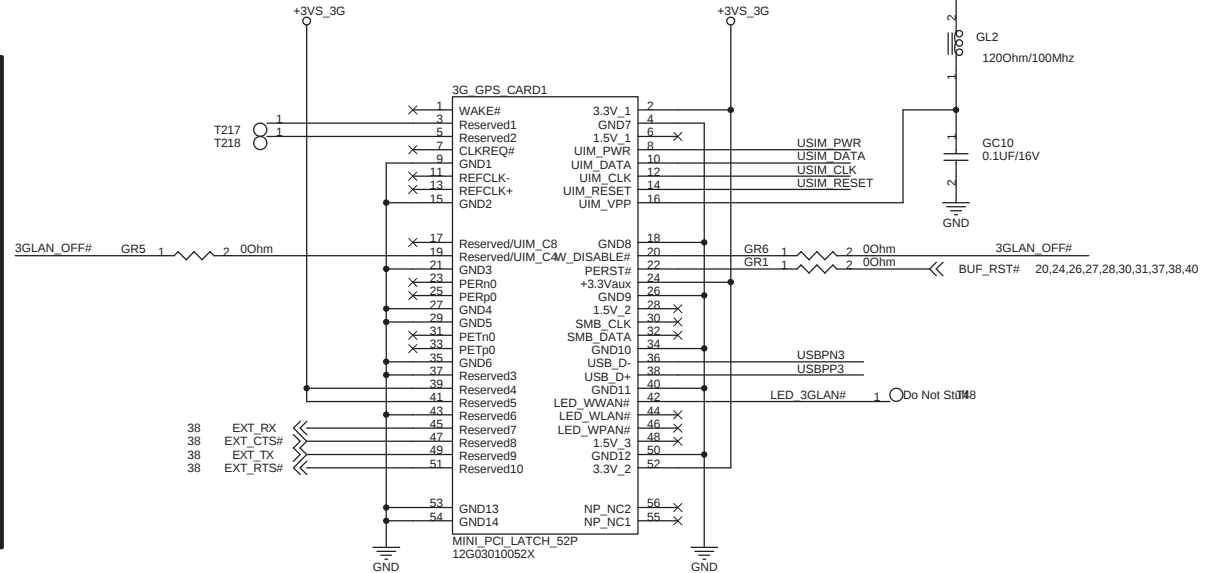
MINI CARD NUT(2.8mm) *2

<http://hobi-elektronika.net>

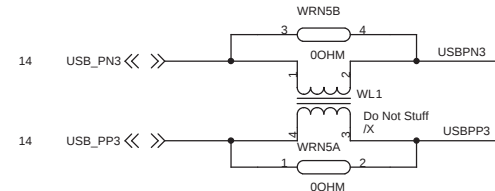
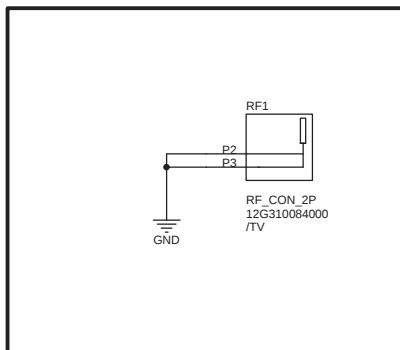
2008/03/11 change to high rated current bead



SIM_CON_8P



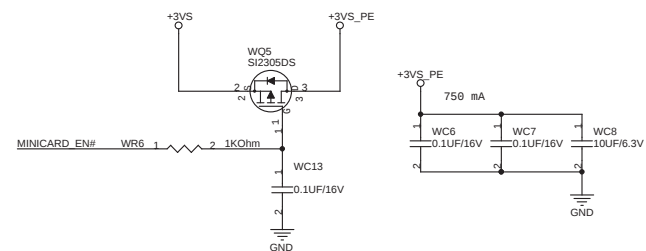
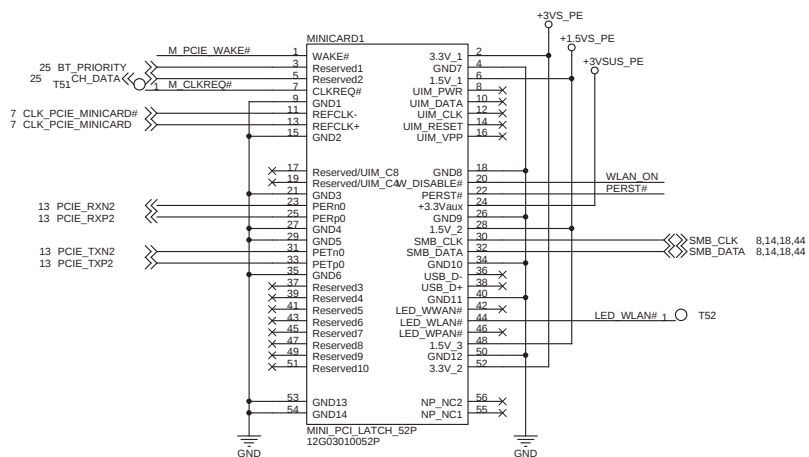
GPS/DTV Antenna



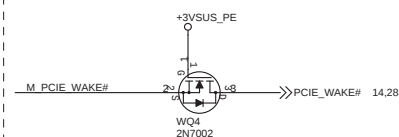
0106 1025

3.5G Module & External Antenna

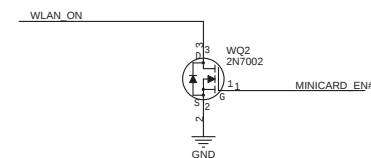
ASUS		Title :	
ASUSTek Computer INC.		Engineer: Leon Sun	
Size	Project Name	Rev	
A3	T91	1.2G	
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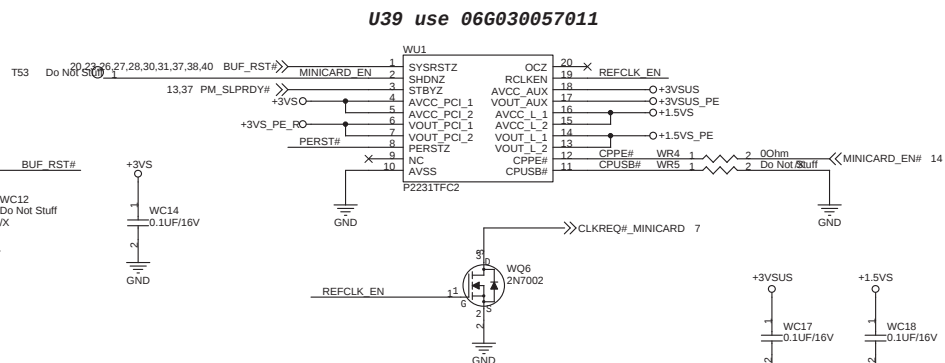
Mini Card Power Supply



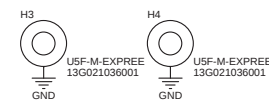
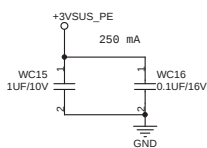
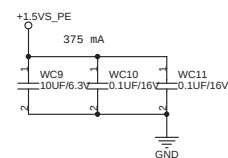
WLAN Wake Up



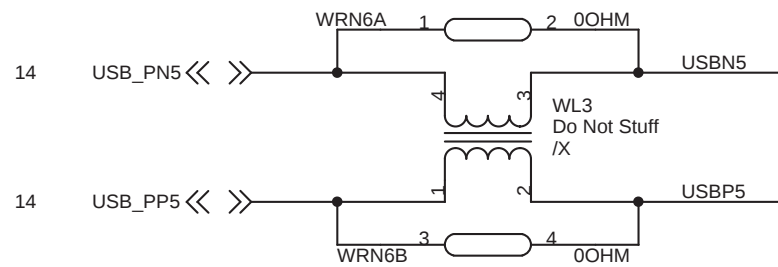
WLAN Radio ON/OFF Switch



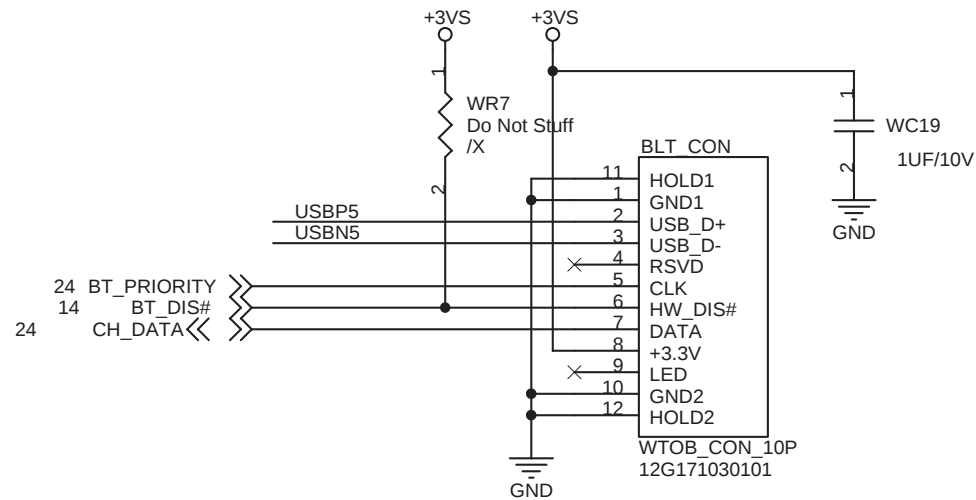
Mini Card Power Switch



MINI CARD NUT(1.6mm) *2



BT USB Port Common Choke



BT Conn

0106 1025



Title : Bluetooth

ASUSTek Computer INC.

Engineer: Jerry Liu

Size
A

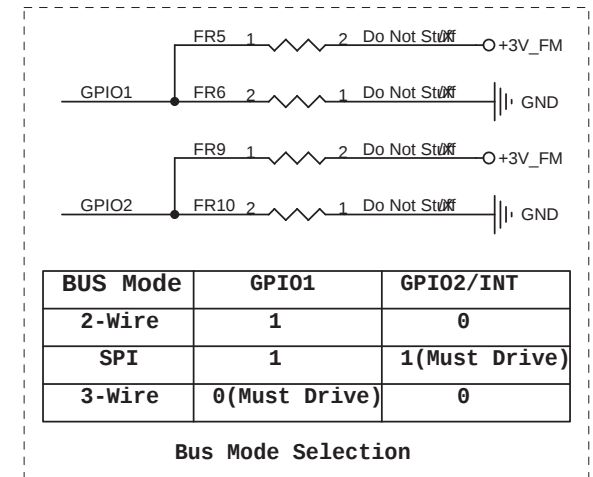
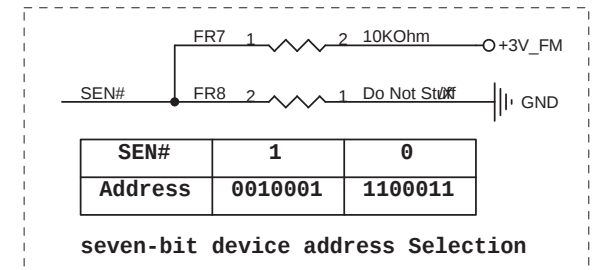
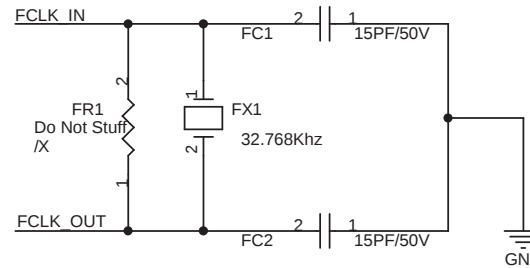
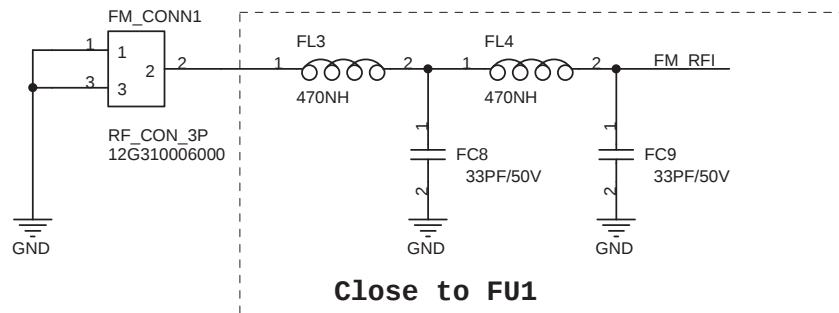
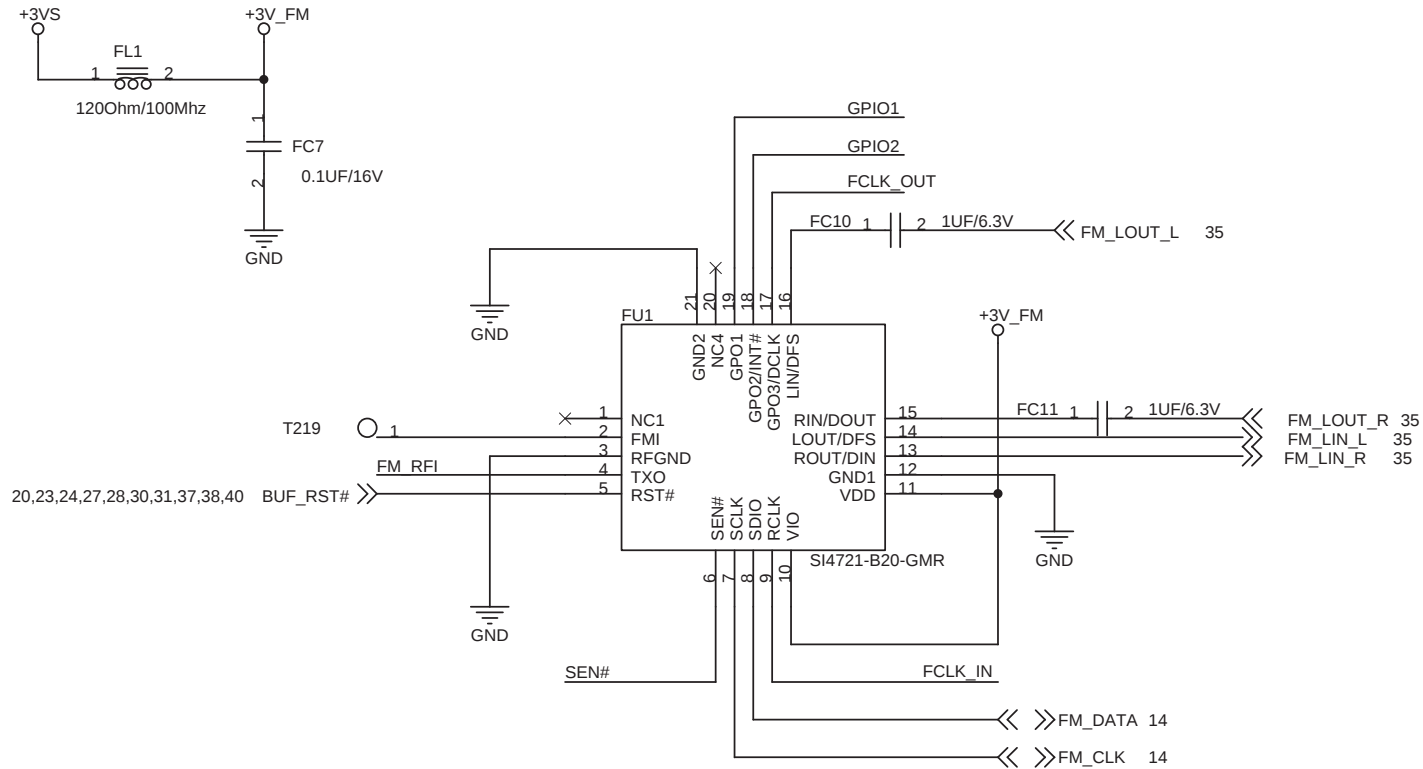
Project Name

T91

Rev
1.2G

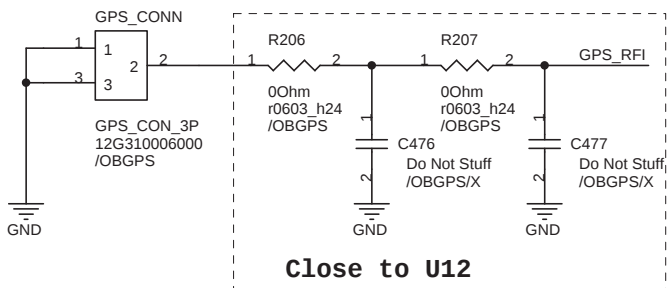
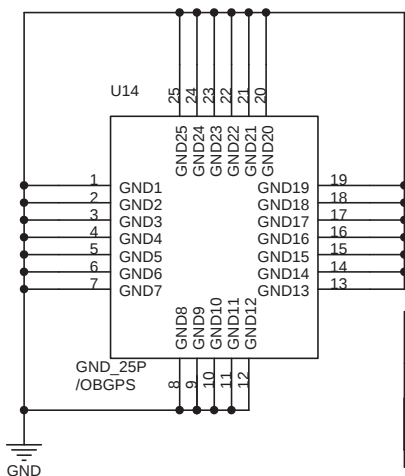
Date: Tuesday, January 06, 2009

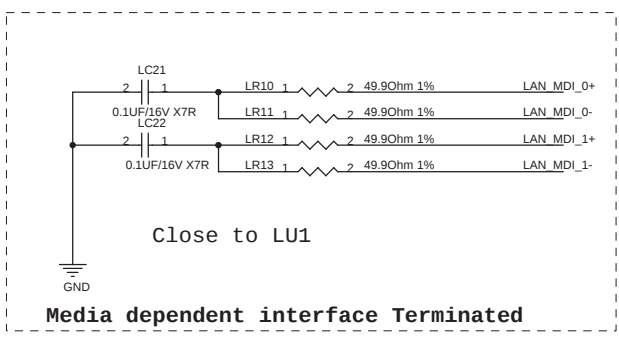
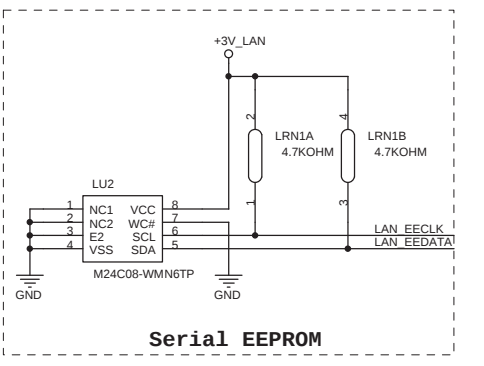
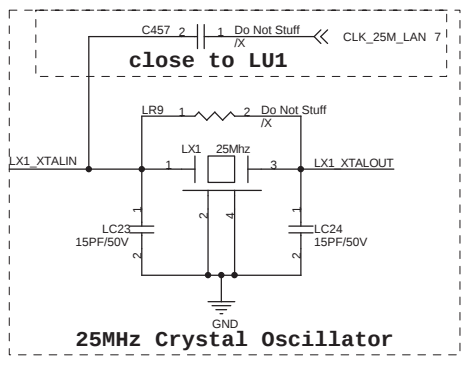
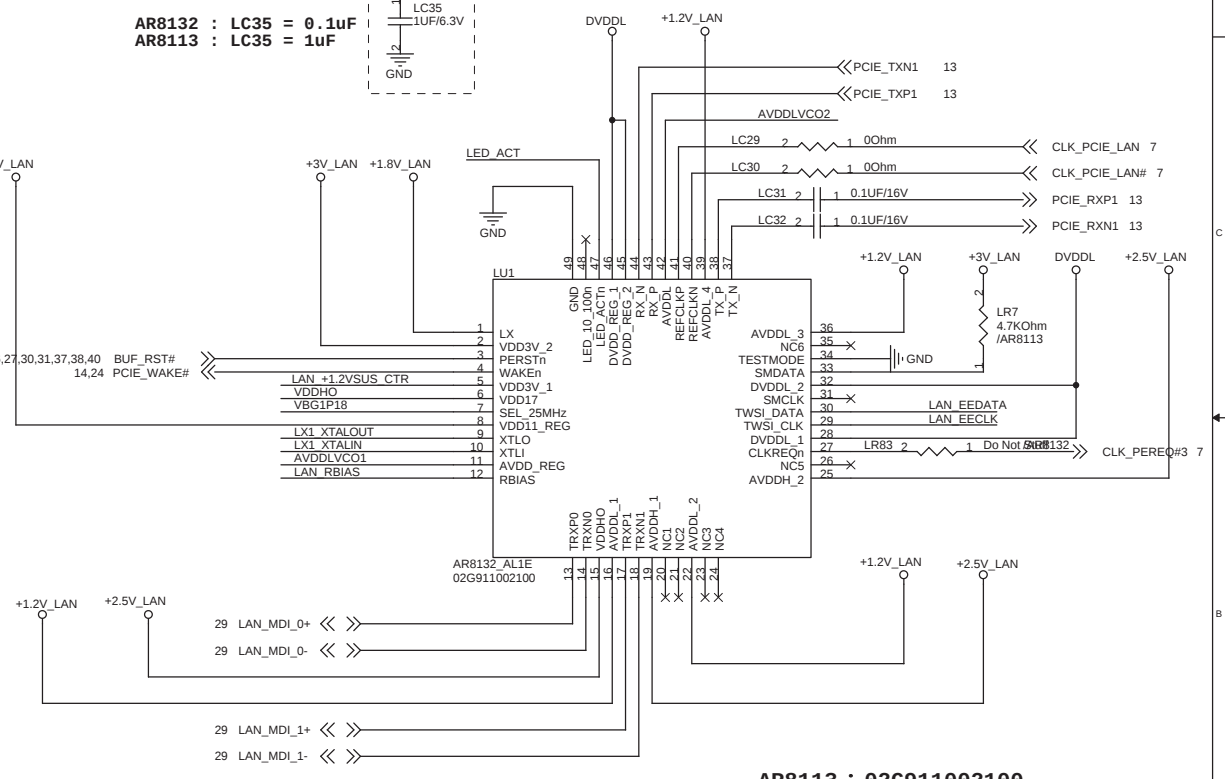
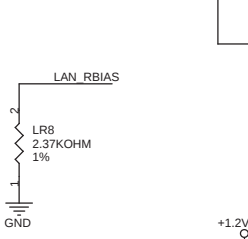
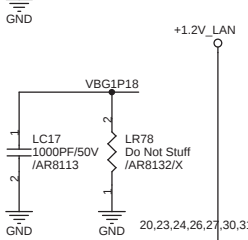
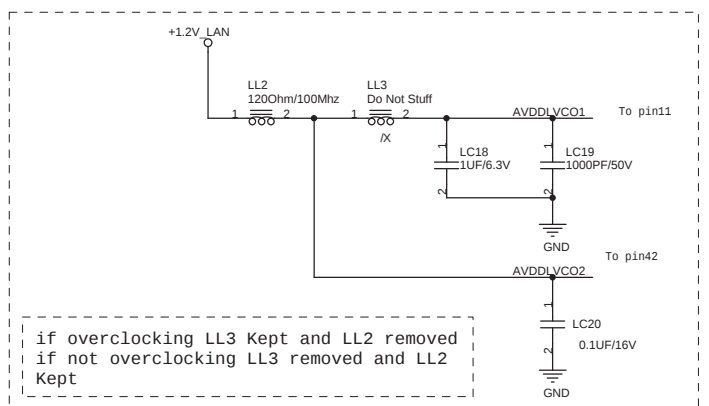
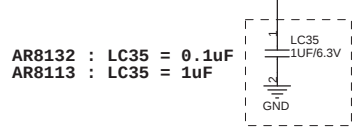
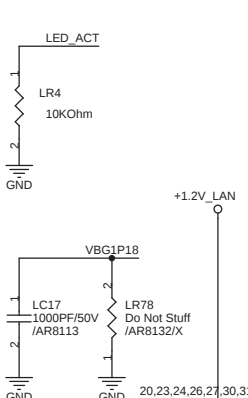
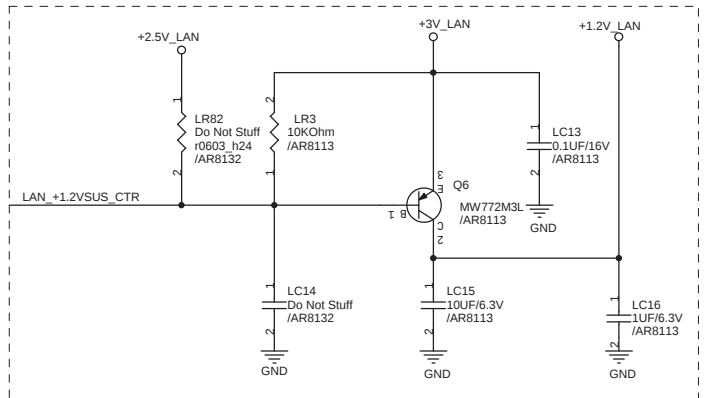
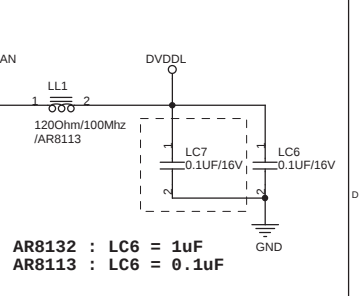
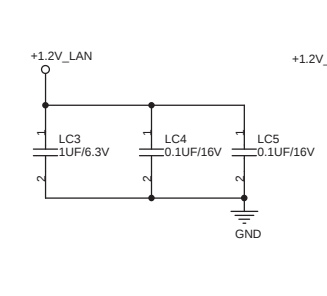
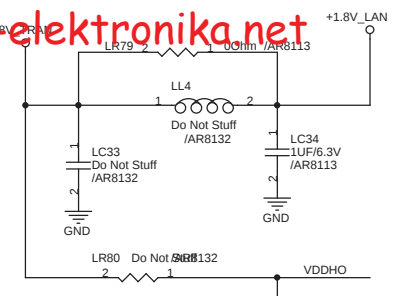
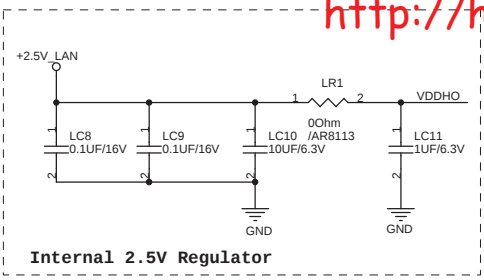
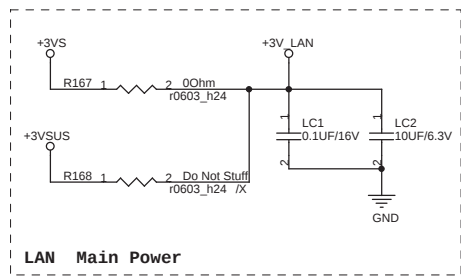
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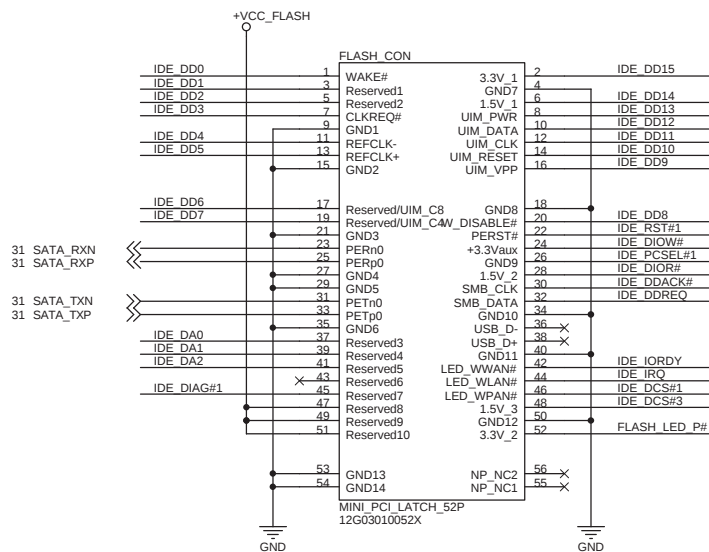
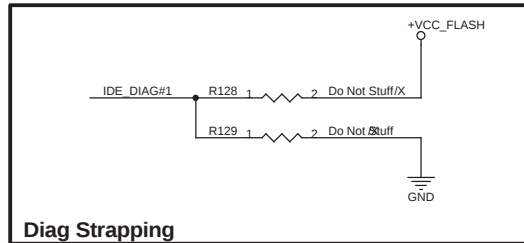
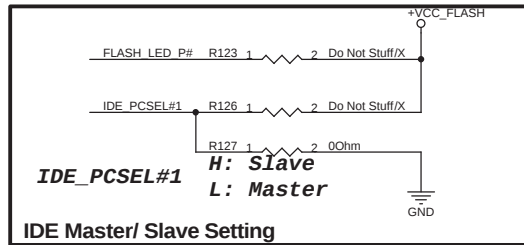
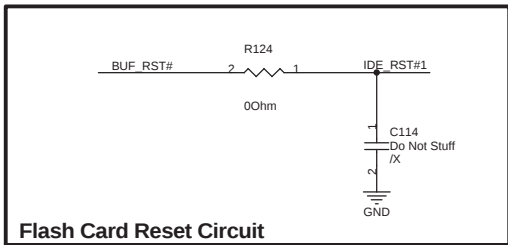
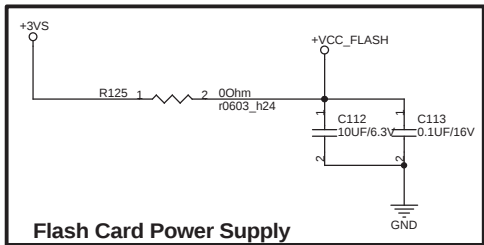
0106 1025

		Title : FM RADIO	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet 26 of 57	

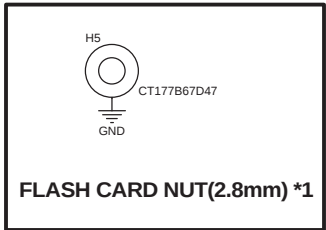


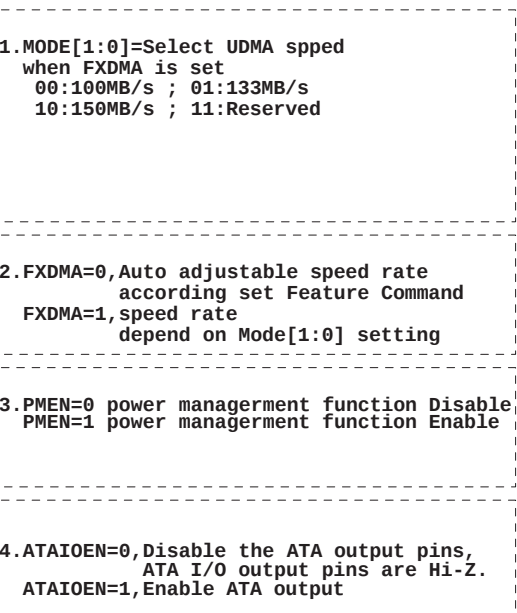
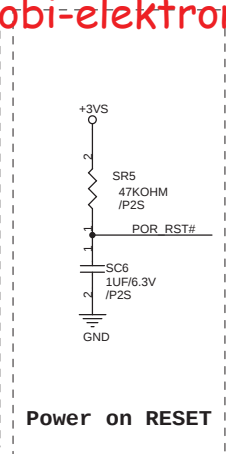


AR8113 : 02G911002100
AR8132 : 02G911002600 (Default)

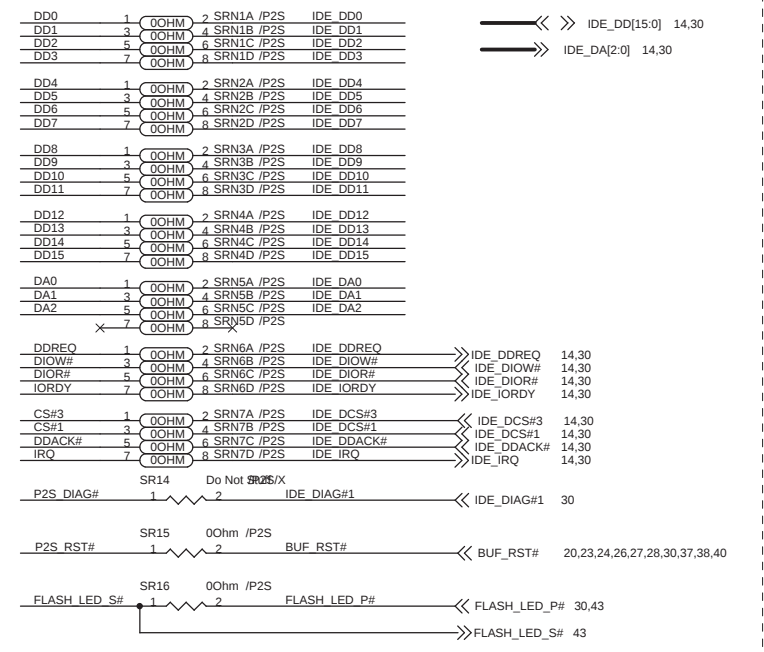


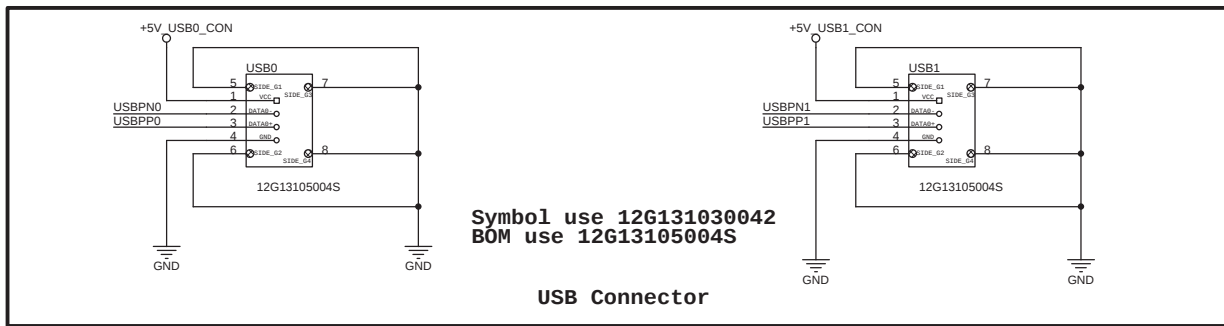
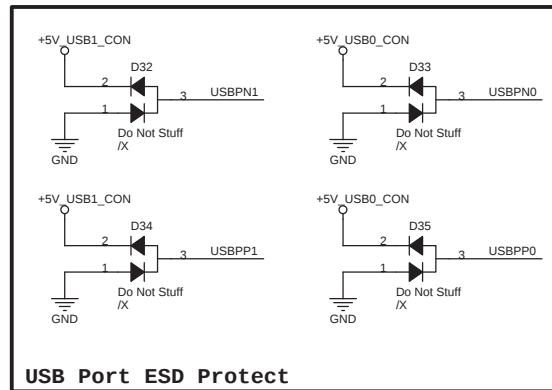
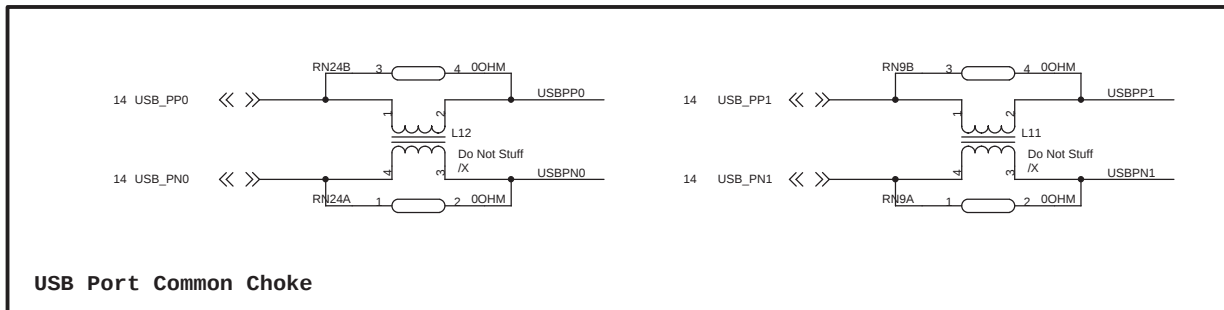
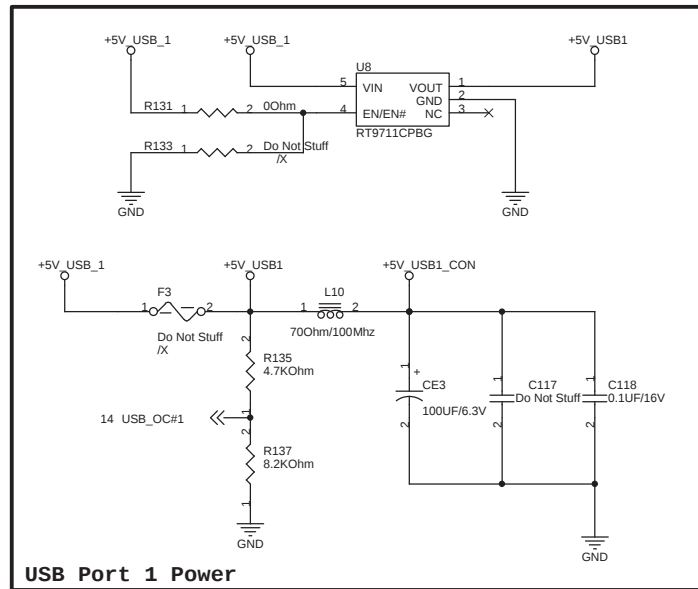
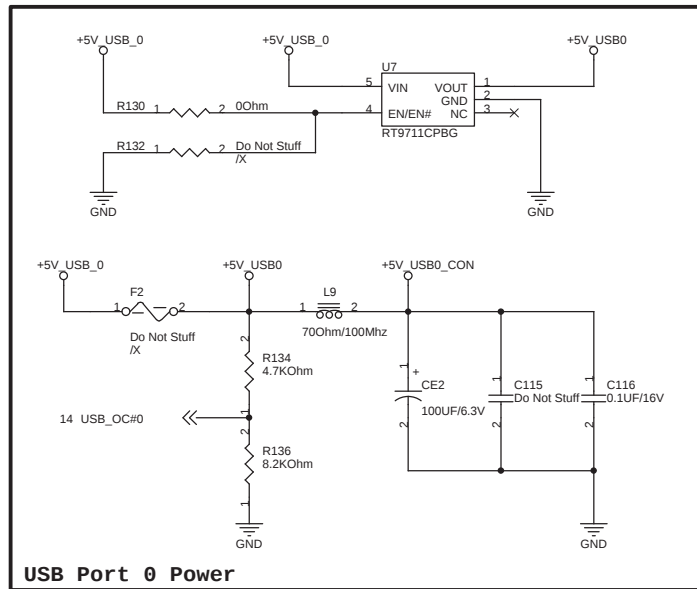
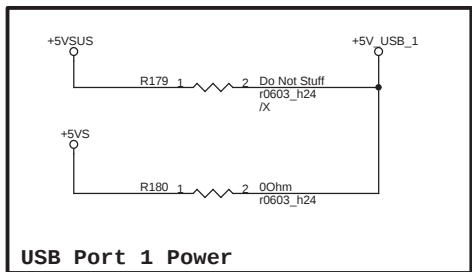
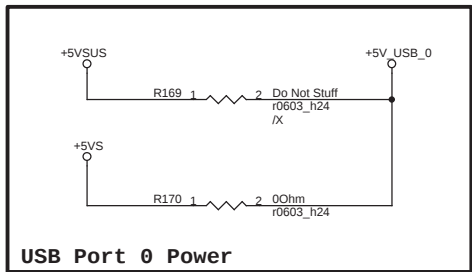
- IDE_DD[15:0] 14,31
- IDE_DA[2:0] 14,31
- IDE_DDACK# 14,31
- IDE_DDREQ 14,31
- IDE_DIOR# 14,31
- IDE_DIO# 14,31
- IDE_IORDY 14,31
- IDE_DCS#1 14,31
- IDE_DCS#3 14,31
- IDE_IRQ 14,31
- BUF_RST# 20,23,24,26,27,28,31,37,38,40
- FLASH_LED_P# 31,43
- IDE_DIAG#1 31

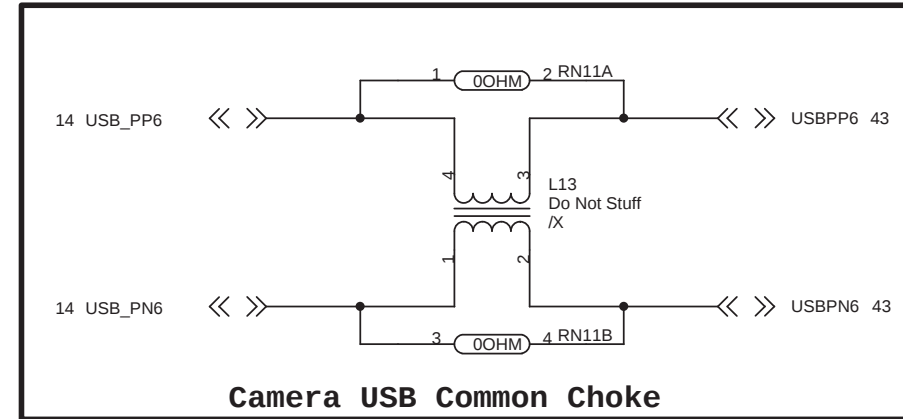
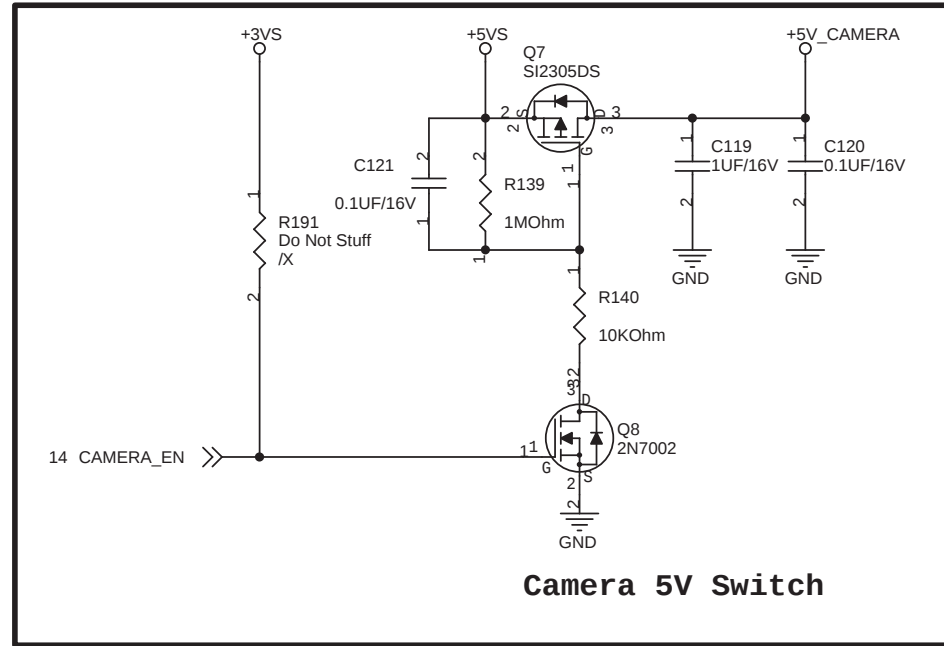




25MHz Crystal Oscillator

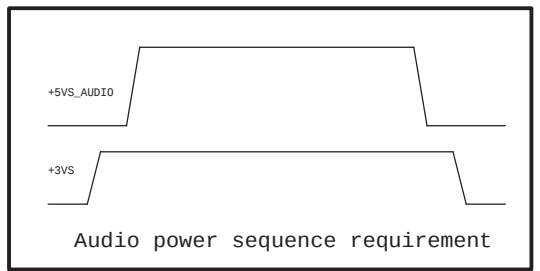
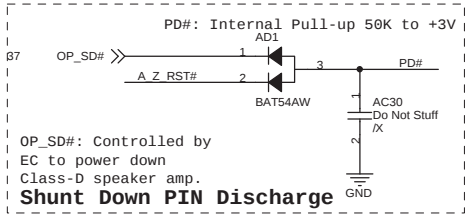
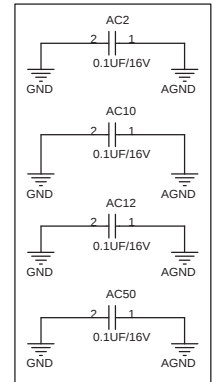
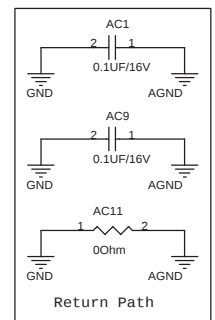
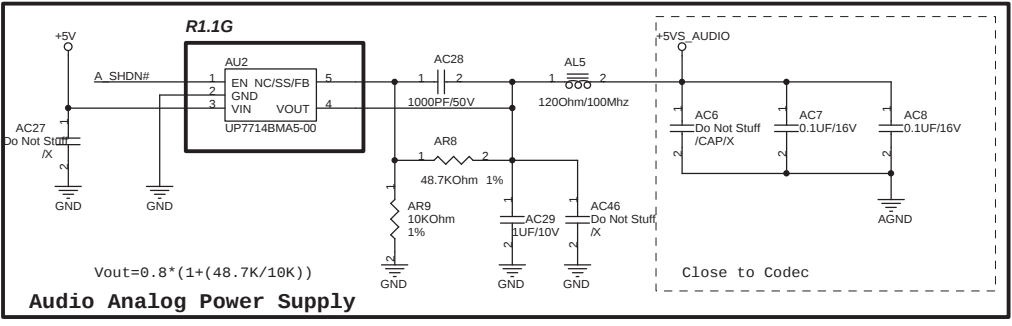
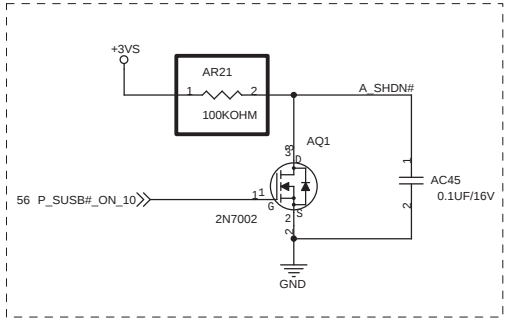
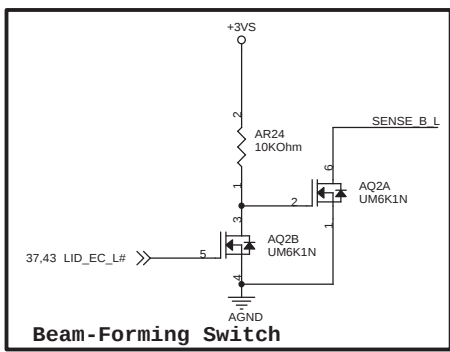
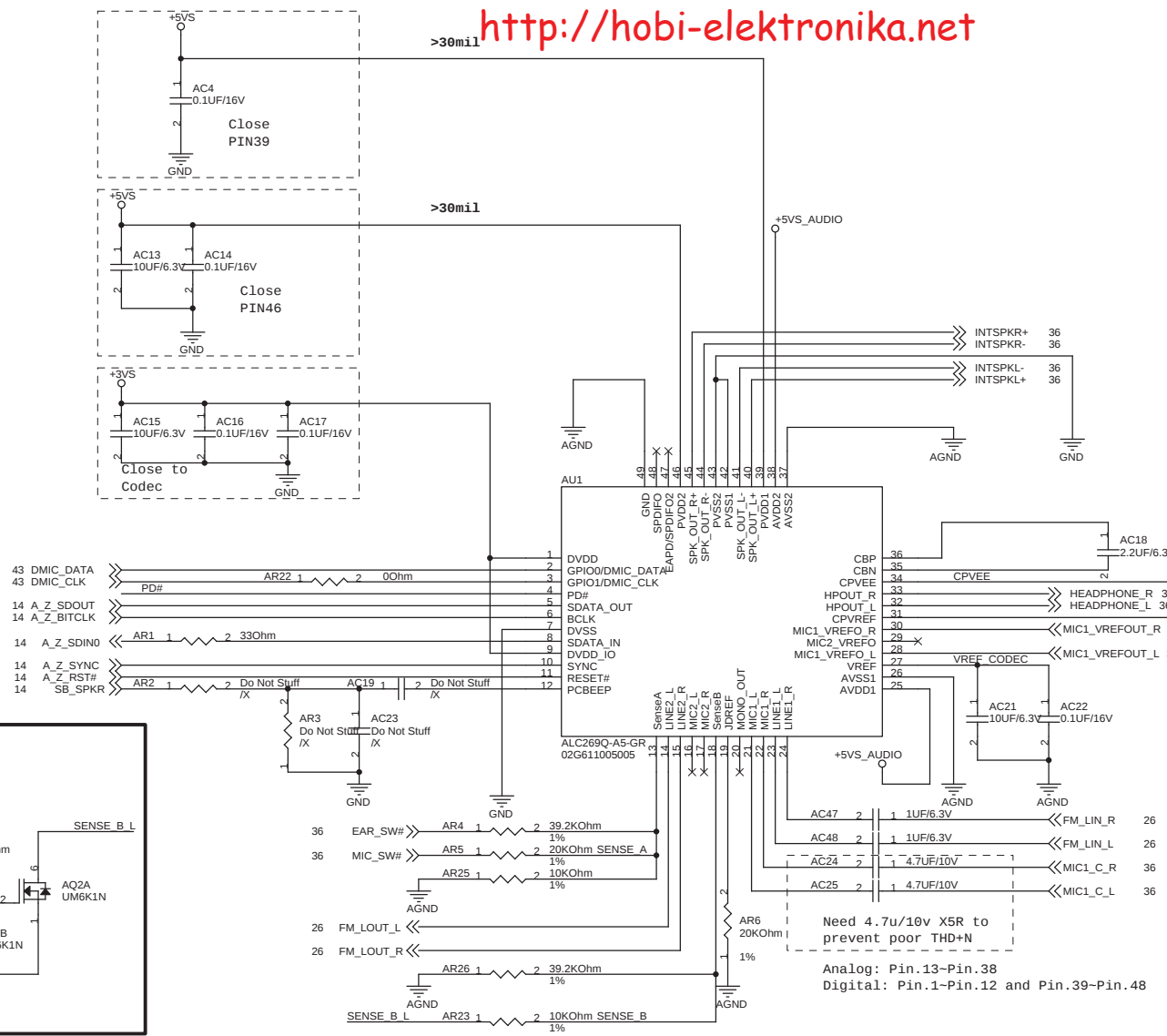


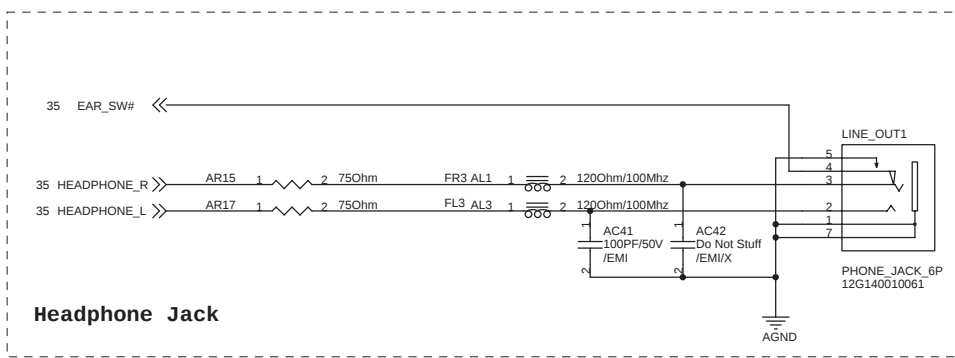
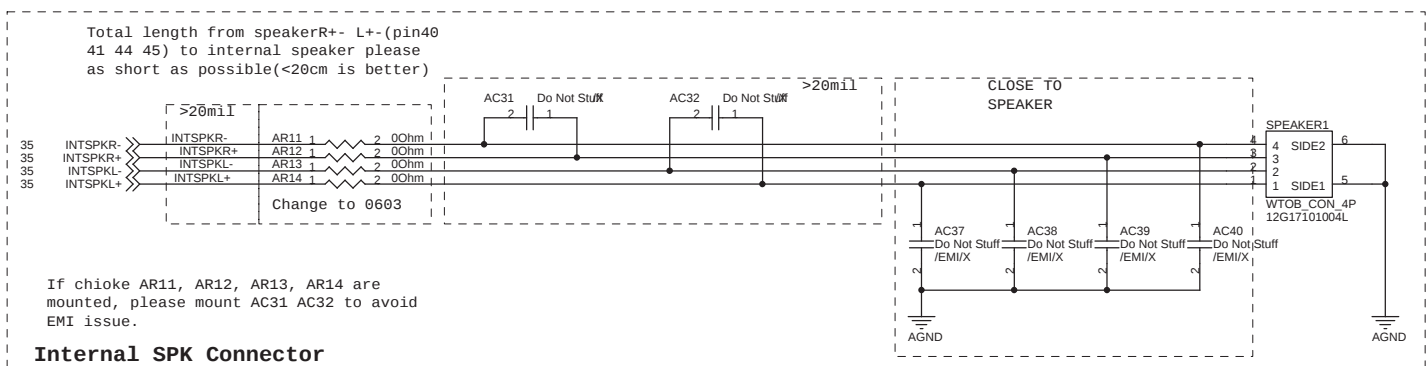




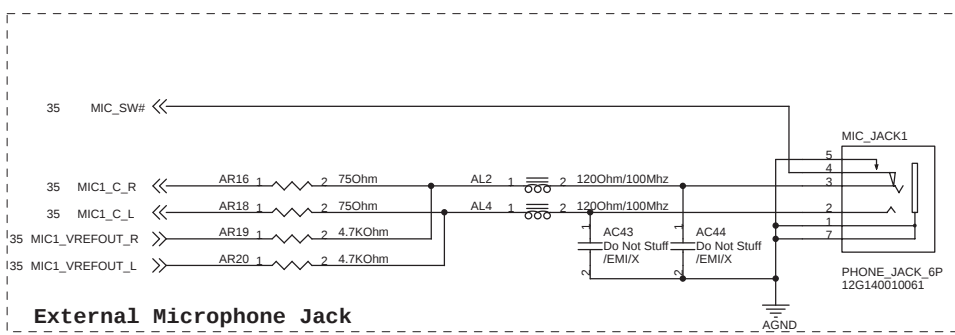
0106 1025

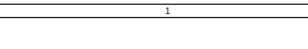
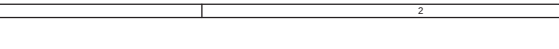
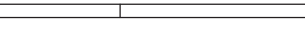
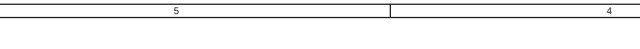
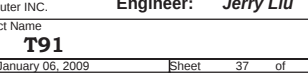
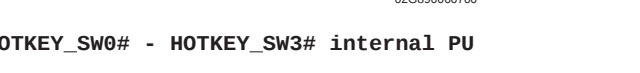
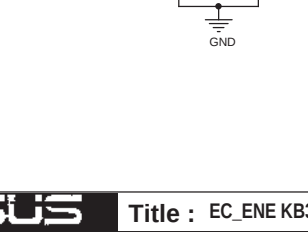
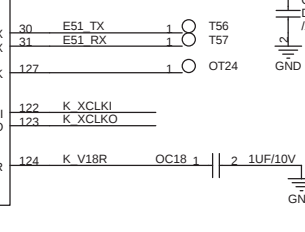
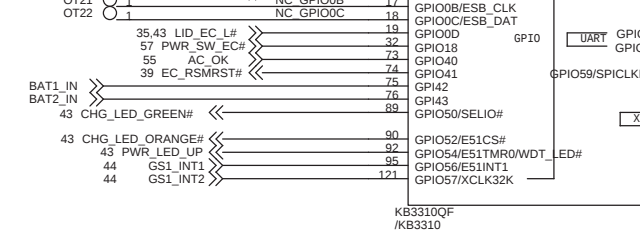
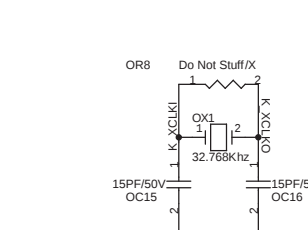
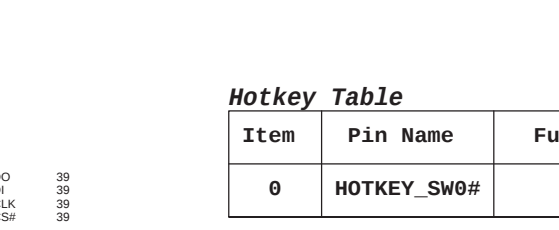
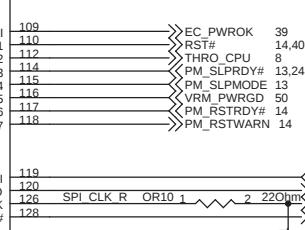
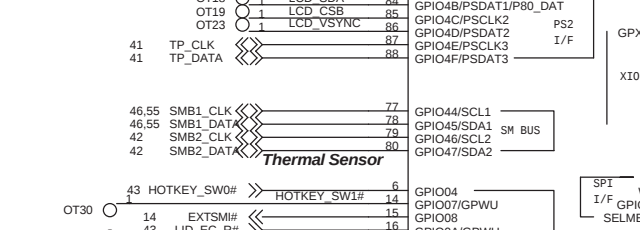
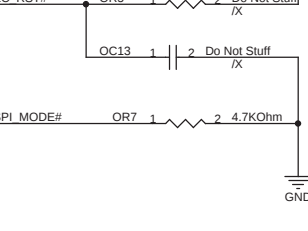
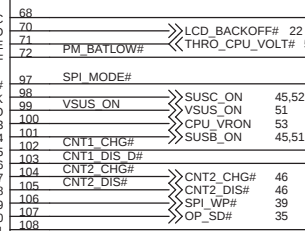
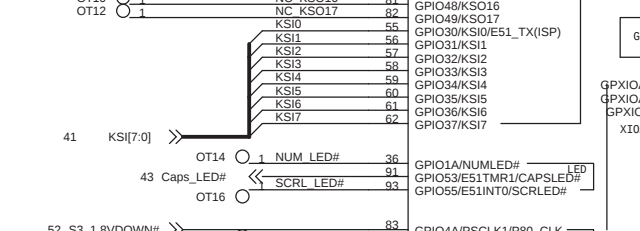
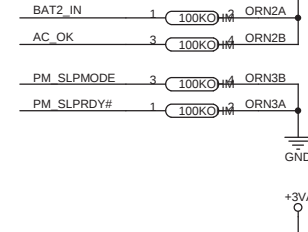
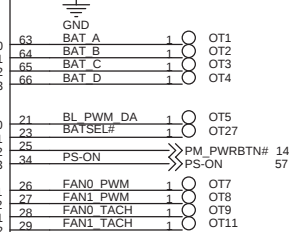
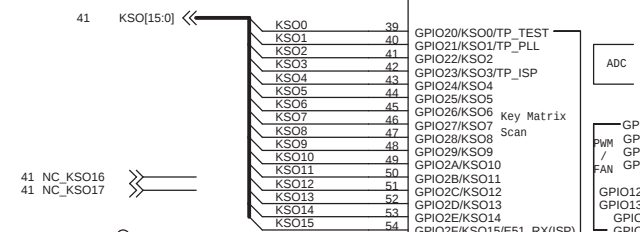
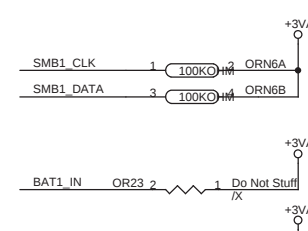
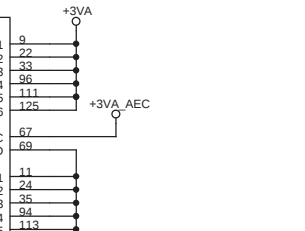
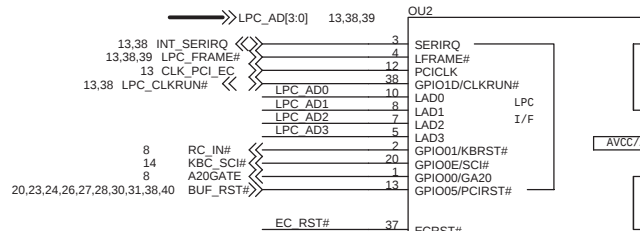
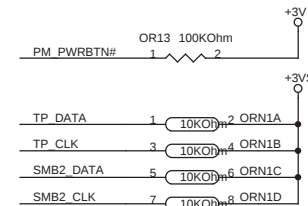
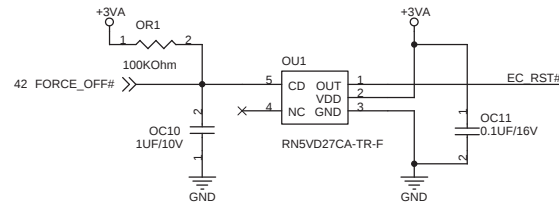
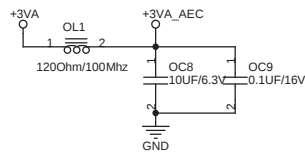
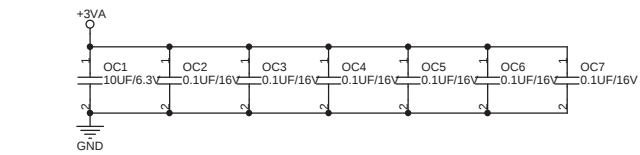
ASUS		Title : Camera Conn	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet	34 of 57





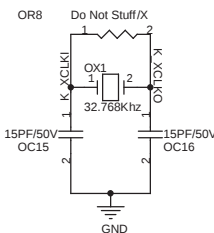
Symbol use 12G140010060
BOM use 12G140010061





Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home



0106 1025

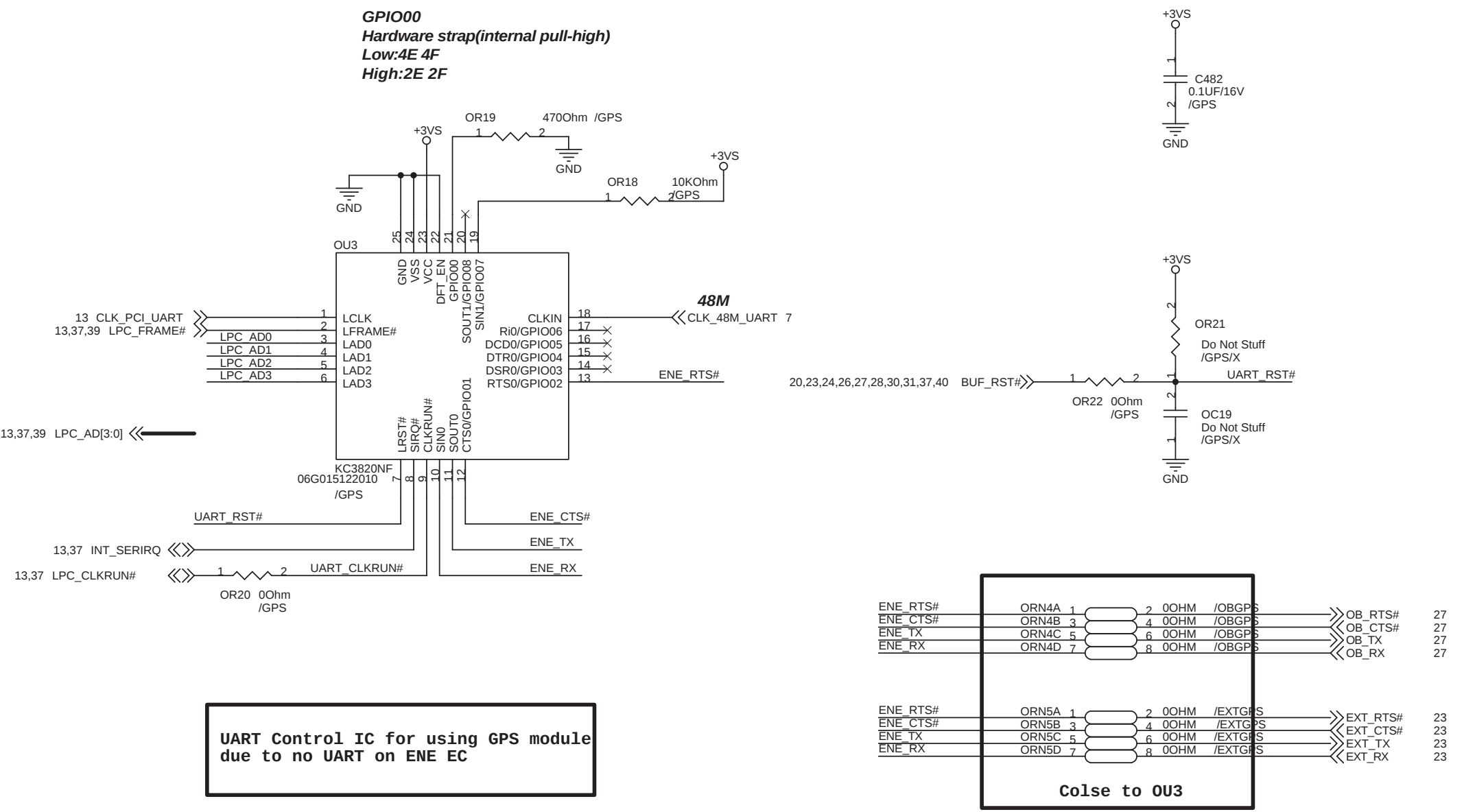
Title : EC_ENE KB3310

ASUSTek Computer INC. **Engineer: Jerry Liu**

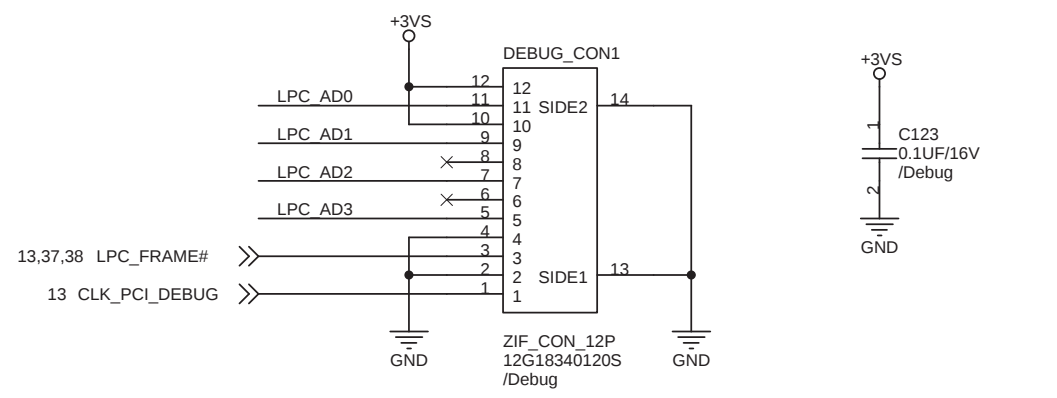
Size	Project Name	Rev
A3	T91	1.2G

Date: Tuesday, January 06, 2009 Sheet 37 of 57

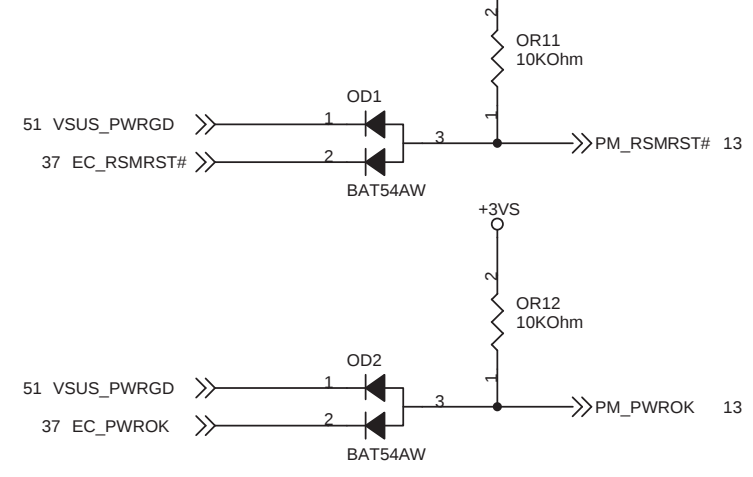
HOTKEY_SW0# - HOTKEY_SW3# internal PU



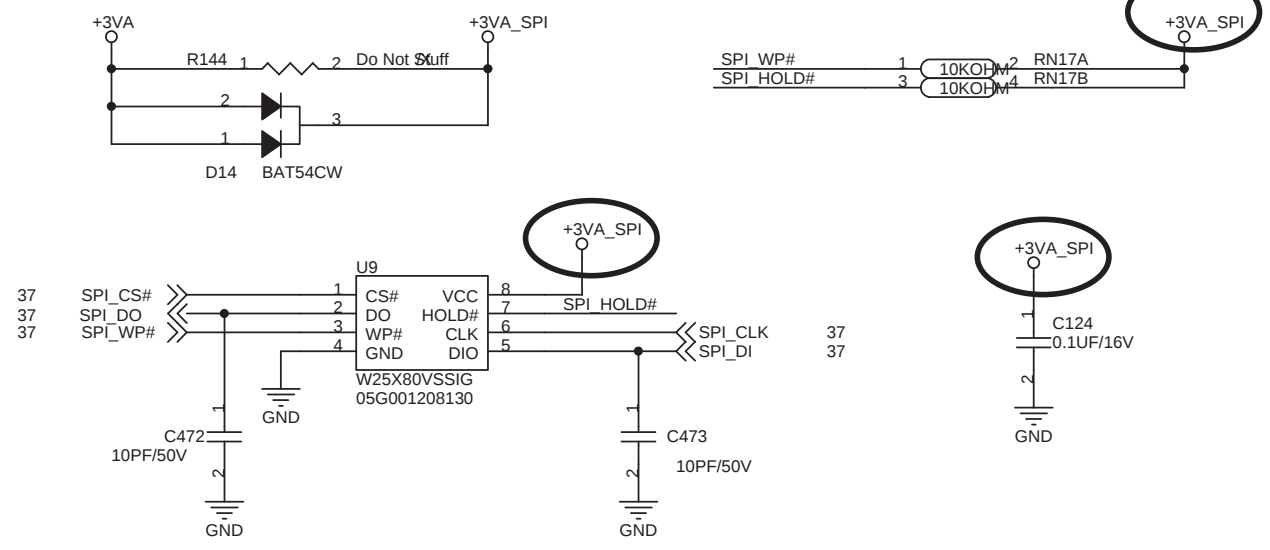
For Debug



Resolve auto-boot issue

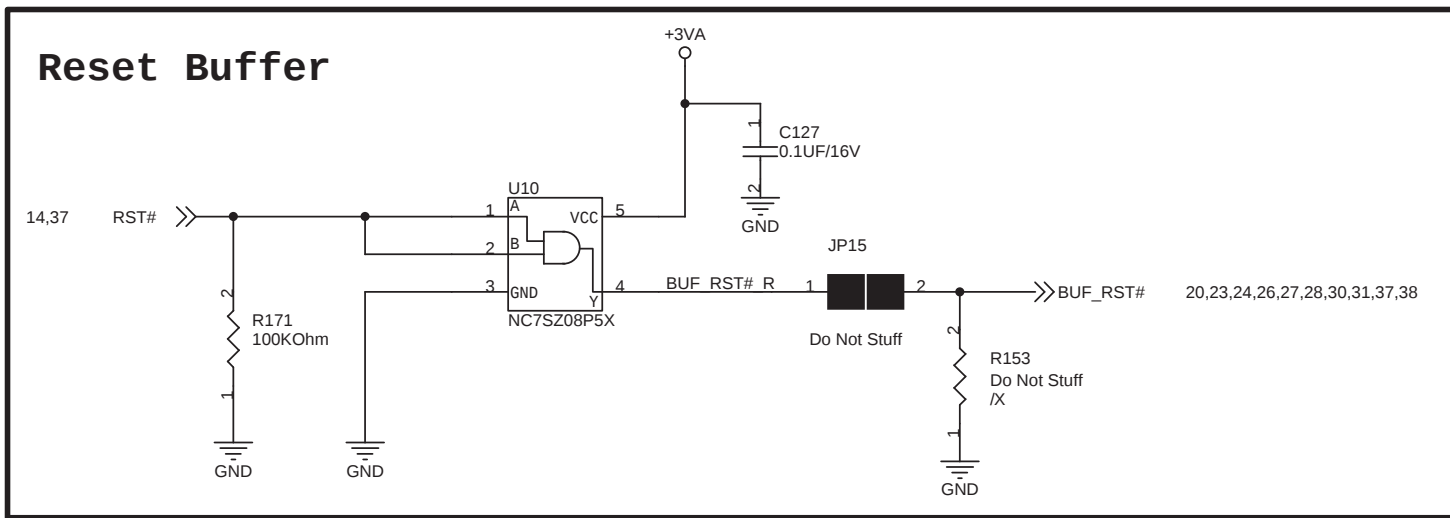
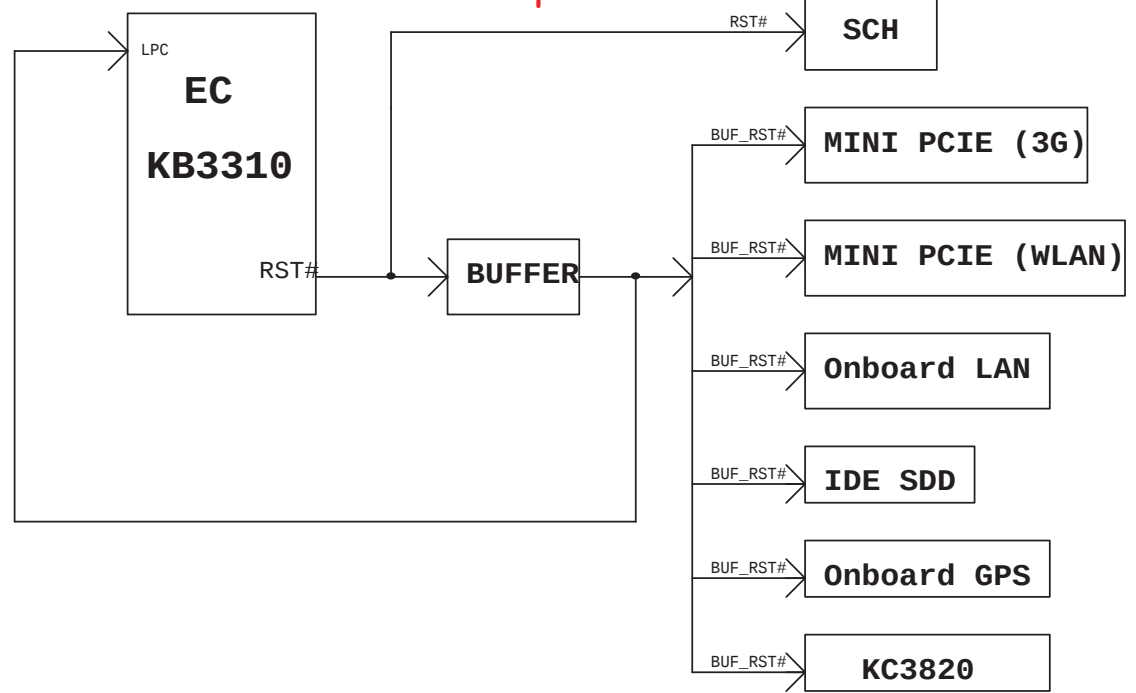


SPI ROM

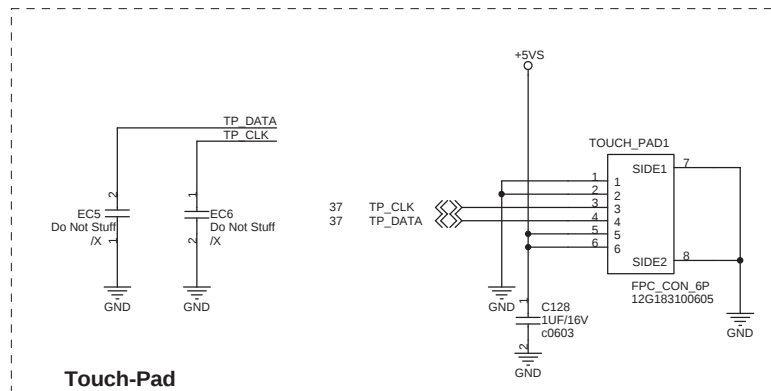
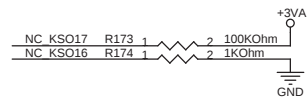
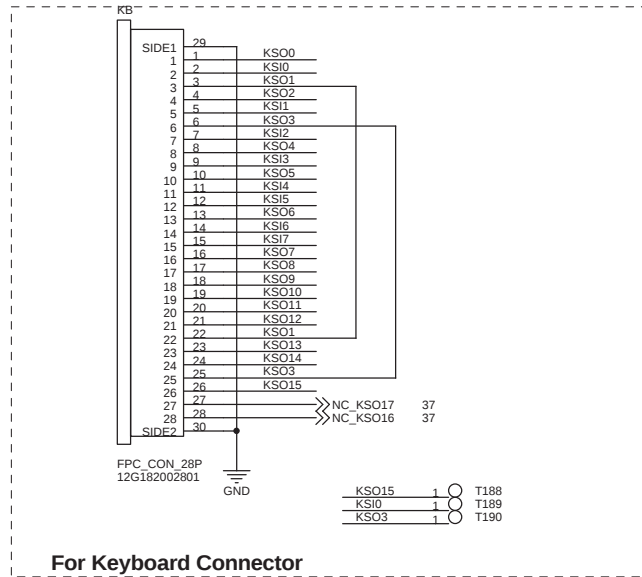


0106 1025

ASUS		Title : SPI ROM/ Debug	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet	39 of 57

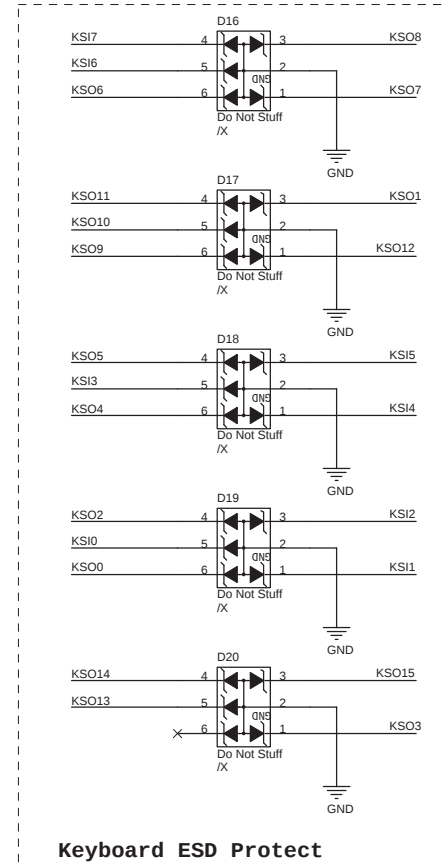


0106 1025



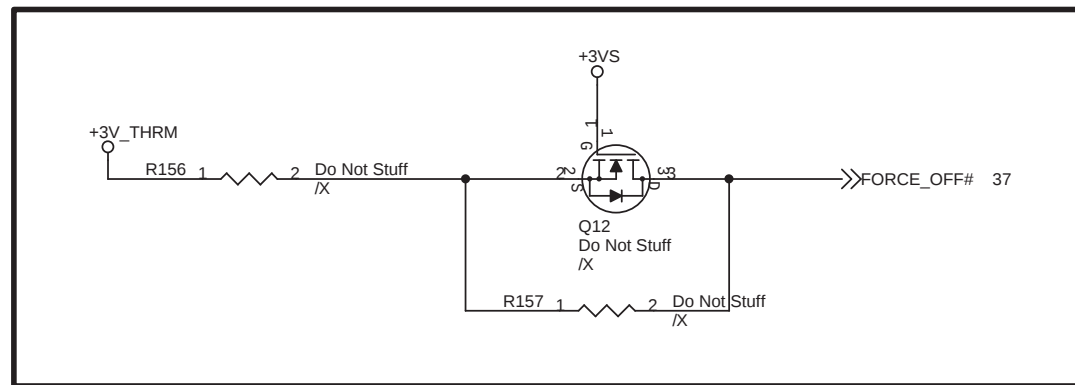
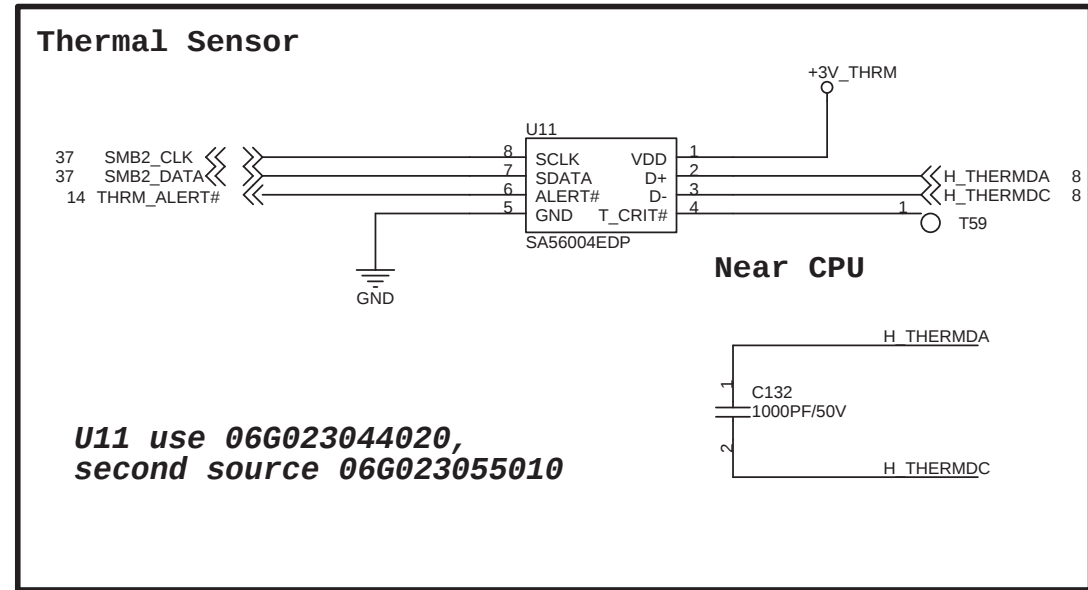
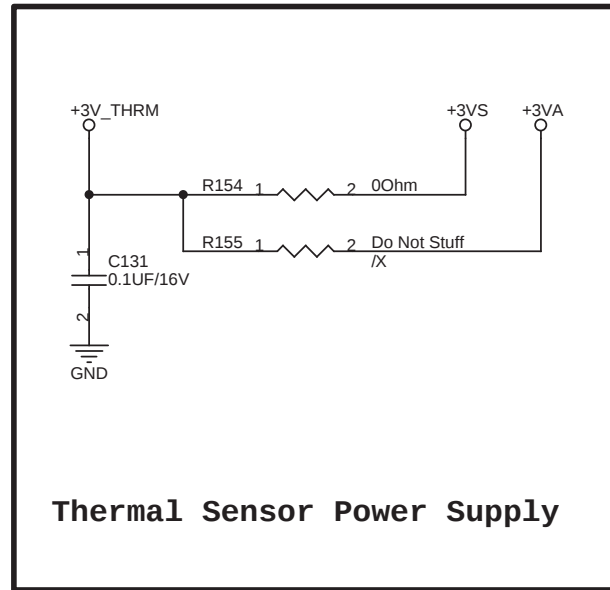
← KSO[15:0] 37

→ KSI[7:0] 37



0106 1025

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size	Project Name		Rev
A3	T91		1.2G
Date: Tuesday, January 06, 2009		Sheet	41 of 57

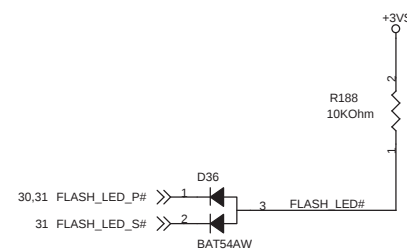


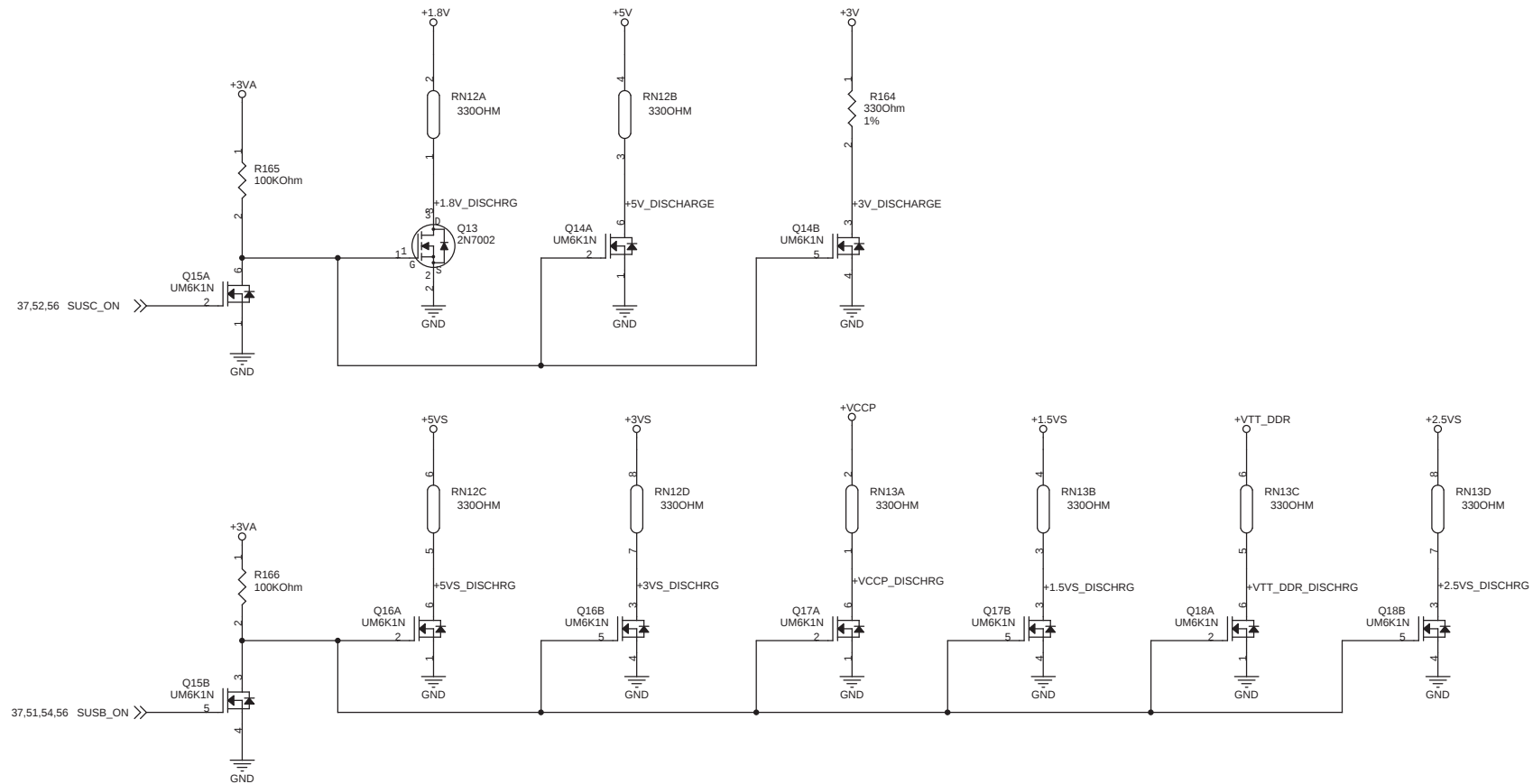
0106 1025

ASUS		Title : Thermal Sensor	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet	42 of 57



Item	Pin Name	Function
0	HOTKEY_SW0#	HOME

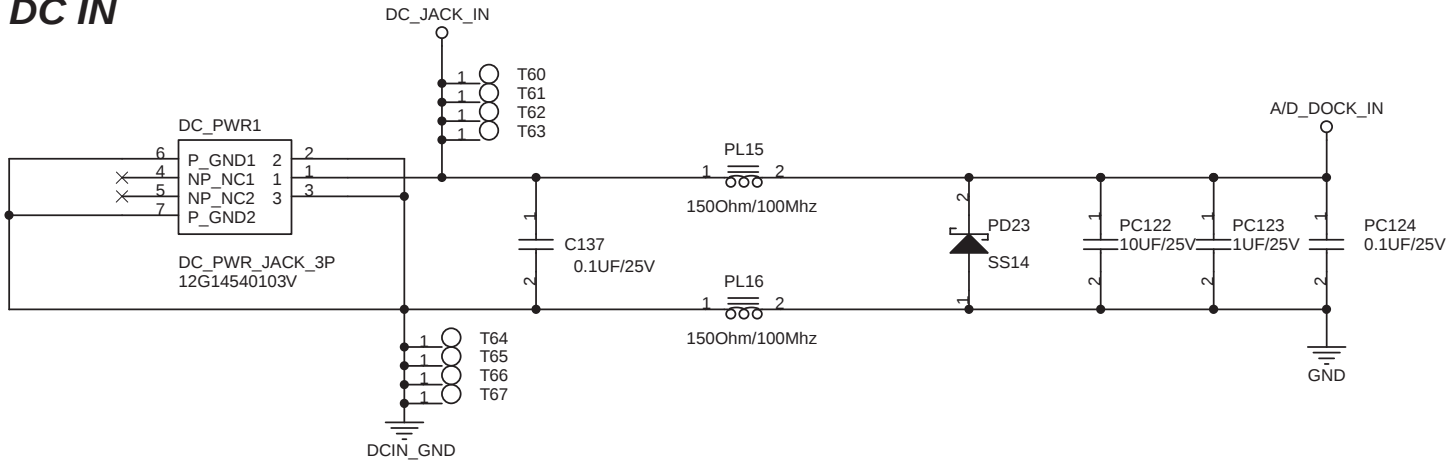




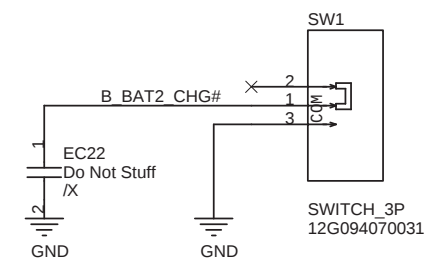
0106 1025

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A3	Project Name T91	Rev 1.2G	
Date: Tuesday, January 06, 2009		Sheet 45 of 57	

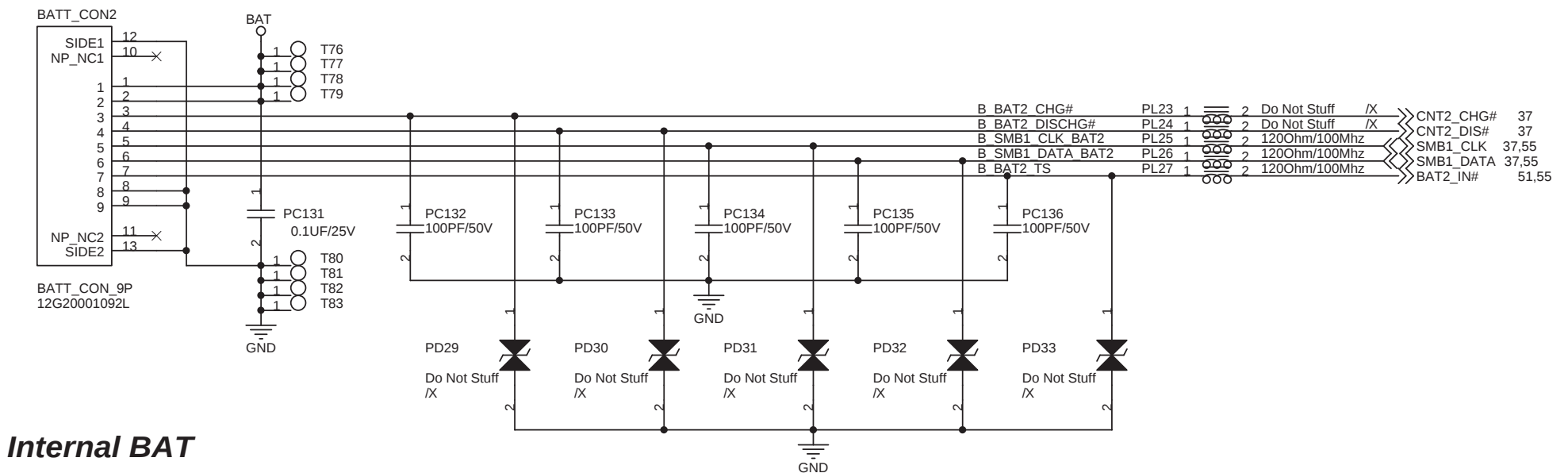
DC IN



Battery Switch



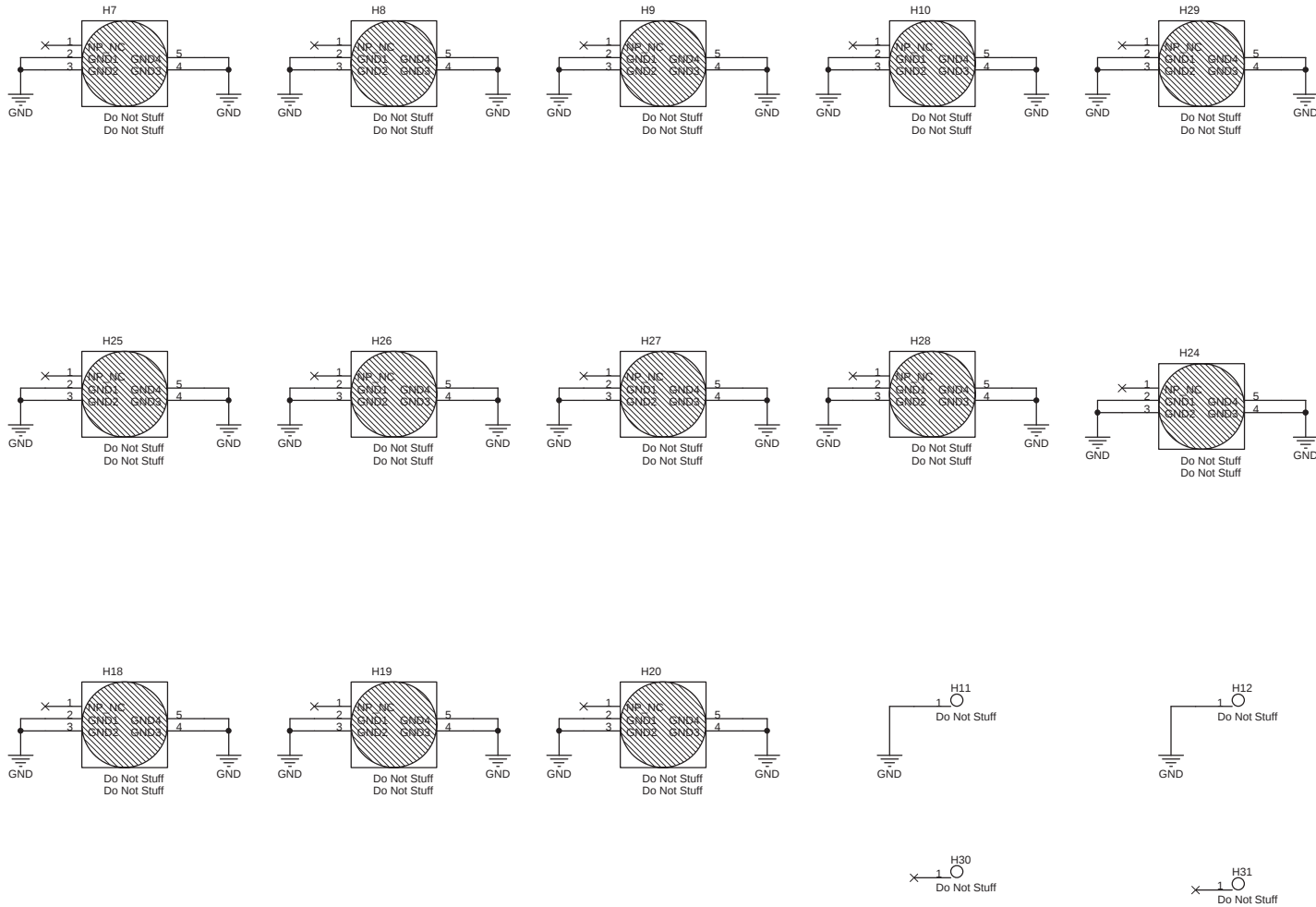
CNT2_CHG# : Low : Battery ON
CNT2_CHG# : open : Battery OFF



Internal BAT

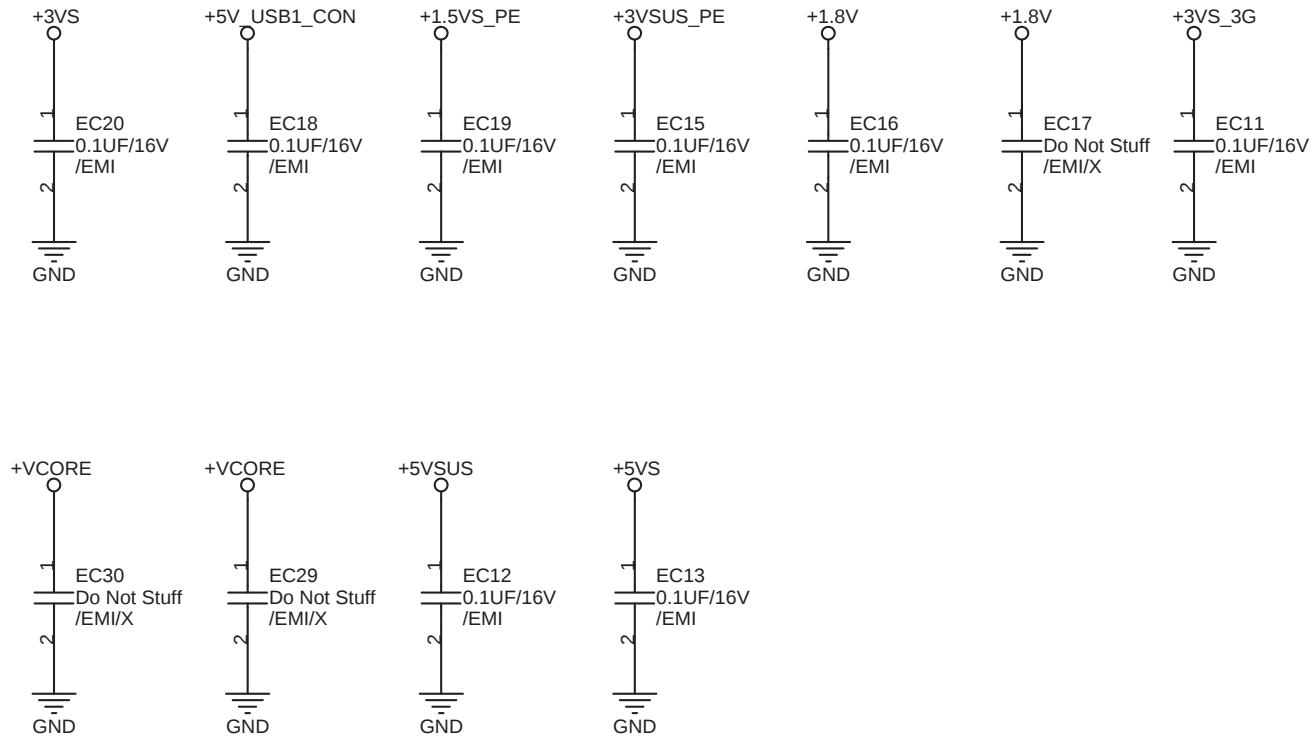
0106 1025

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet 46 of 57	



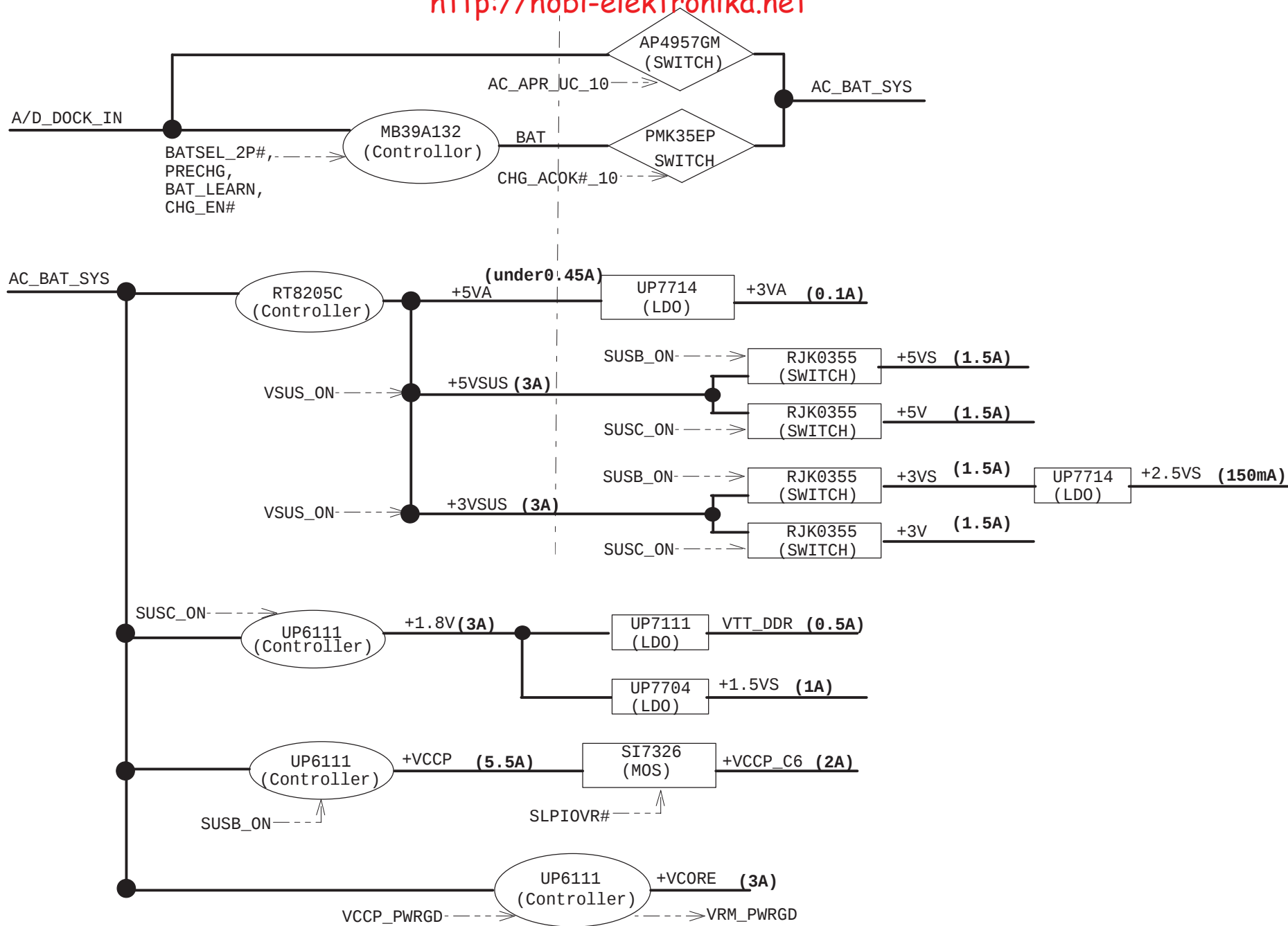
0106 1025

ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size	Project Name		Rev
A3	T91		1.2G
Date: Tuesday, January 06, 2009		Sheet	47 of 57



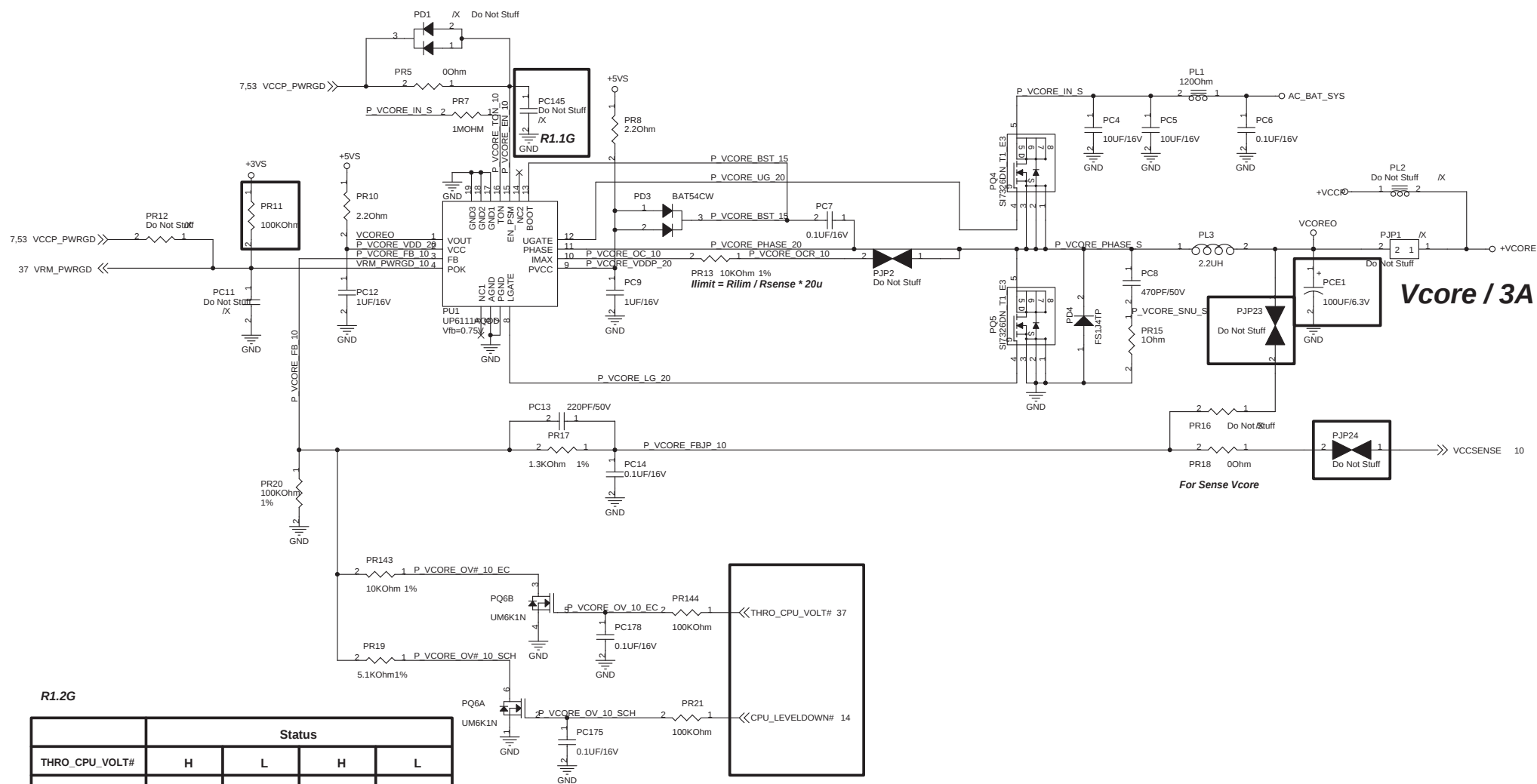
0106 1025

		Title : EMI	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet	48 of 57

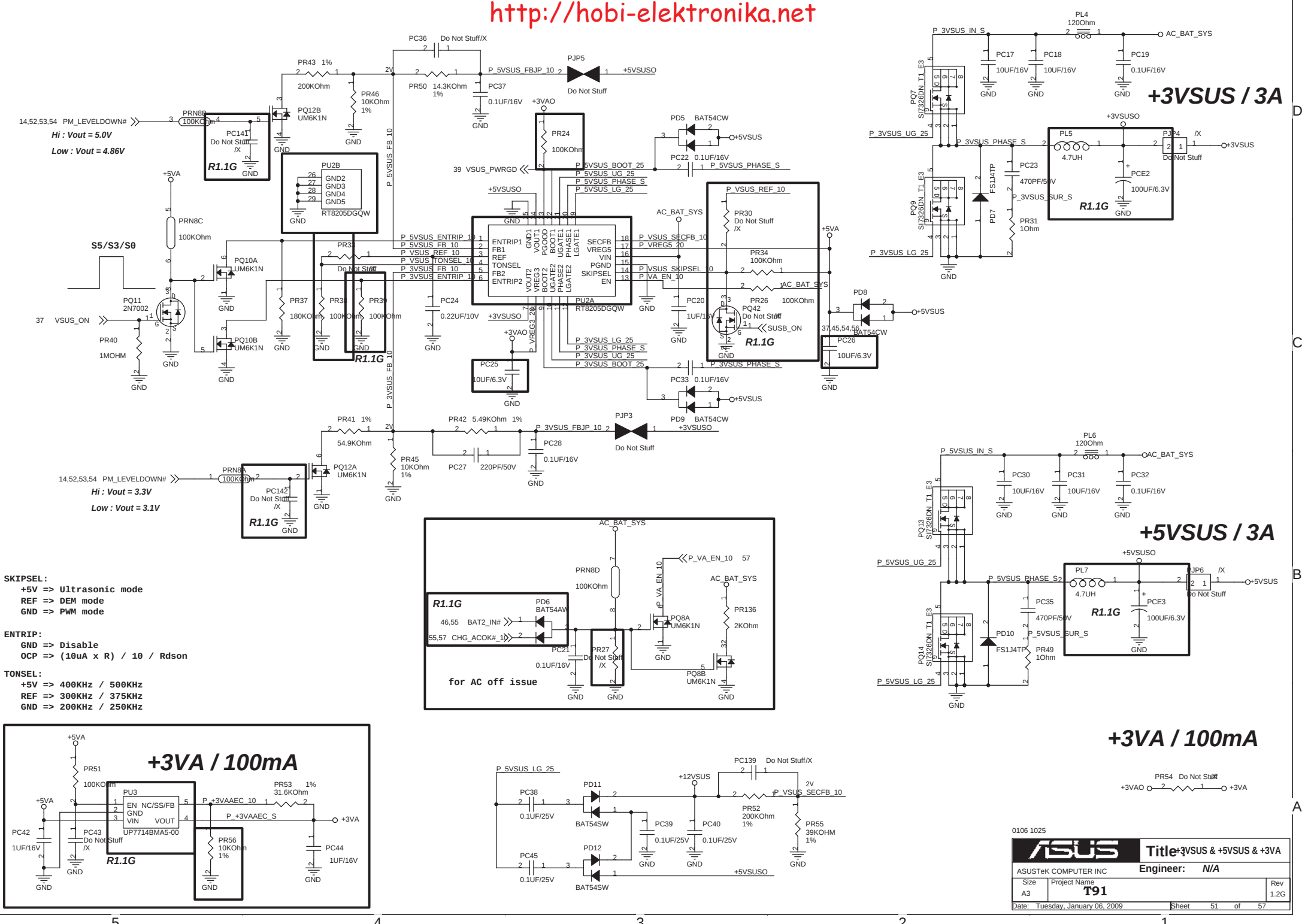


0106 1025

		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A3	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet 49 of 57	



R1.2G				
	Status			
THRO_CPU_VOLT#	H	L	H	L
CPU_LEVELDOWN#	H	H	L	L
Voltage	1.0484V	0.9509V	0.8573V	0.7598V
	Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

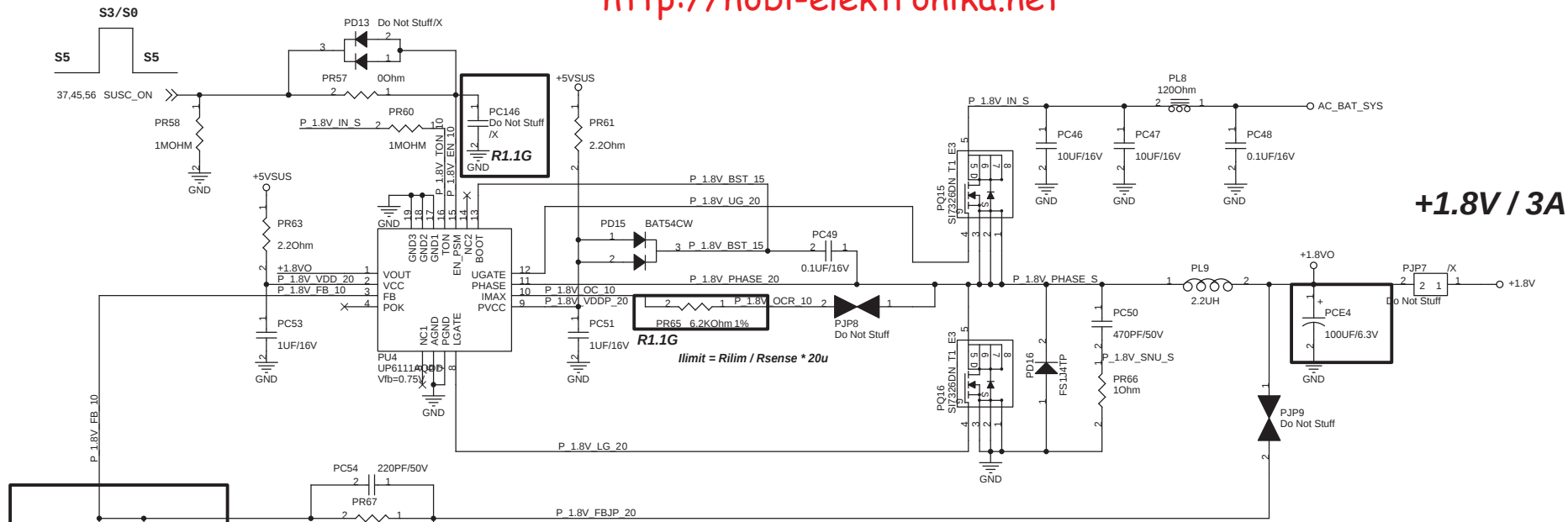


SKIPSEL:
+5V => Ultrasonic mode
REF => DEM mode
GND => PWM mode

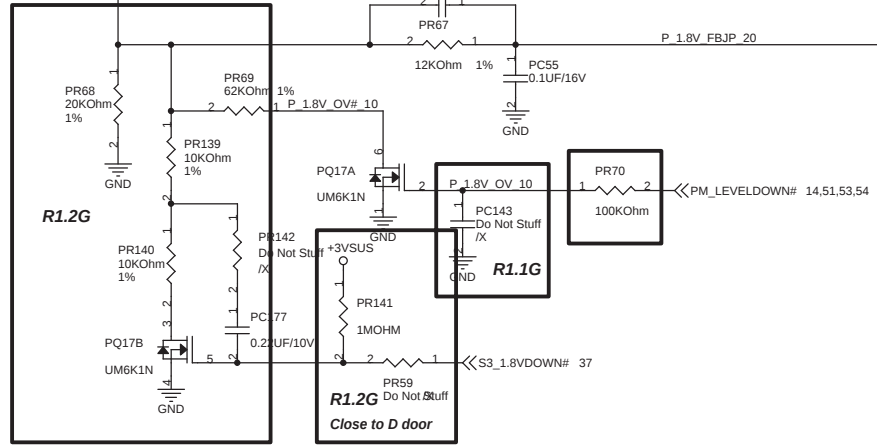
ENTRIP:
GND => Disable
OCP => (10uA x R) / 10 / Rdson

TONSEL:
+5V => 400KHz / 500KHz
REF => 300KHz / 375KHz
GND => 200KHz / 250KHz

for AC off issue

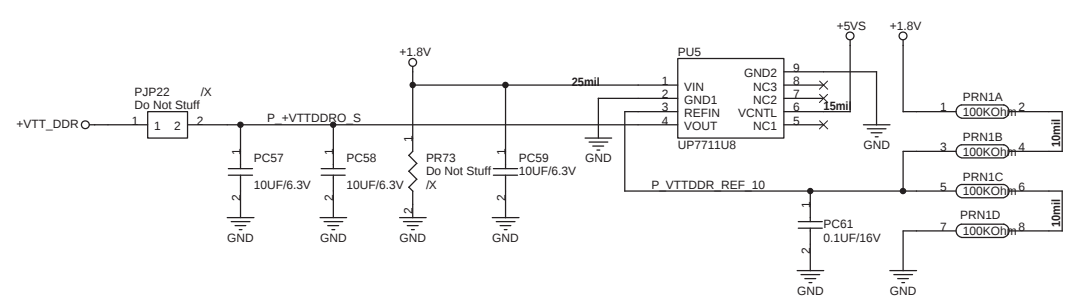


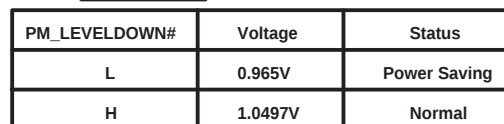
+1.8V / 3A

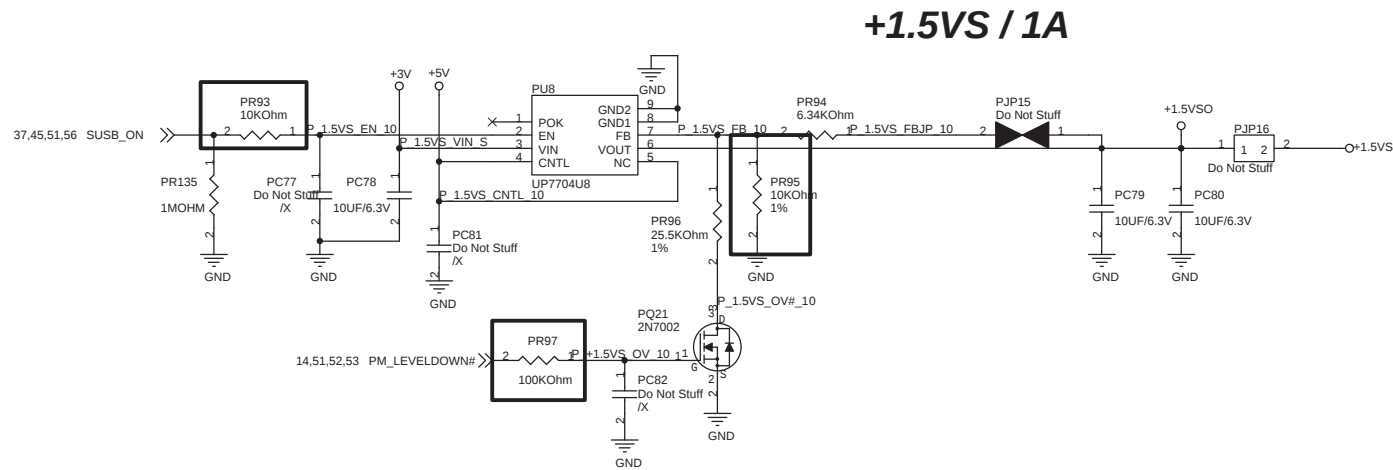
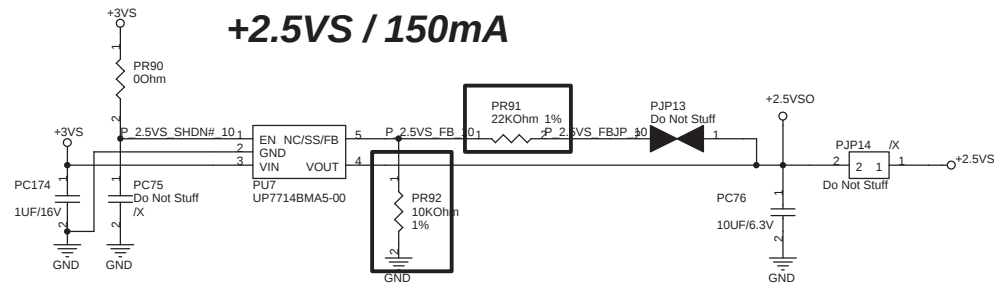


VTT_DDR / 0.5A

PM_LEVELDOWN#	Voltage	Status
L	1.65V	Power Saving
H	1.795V	Normal



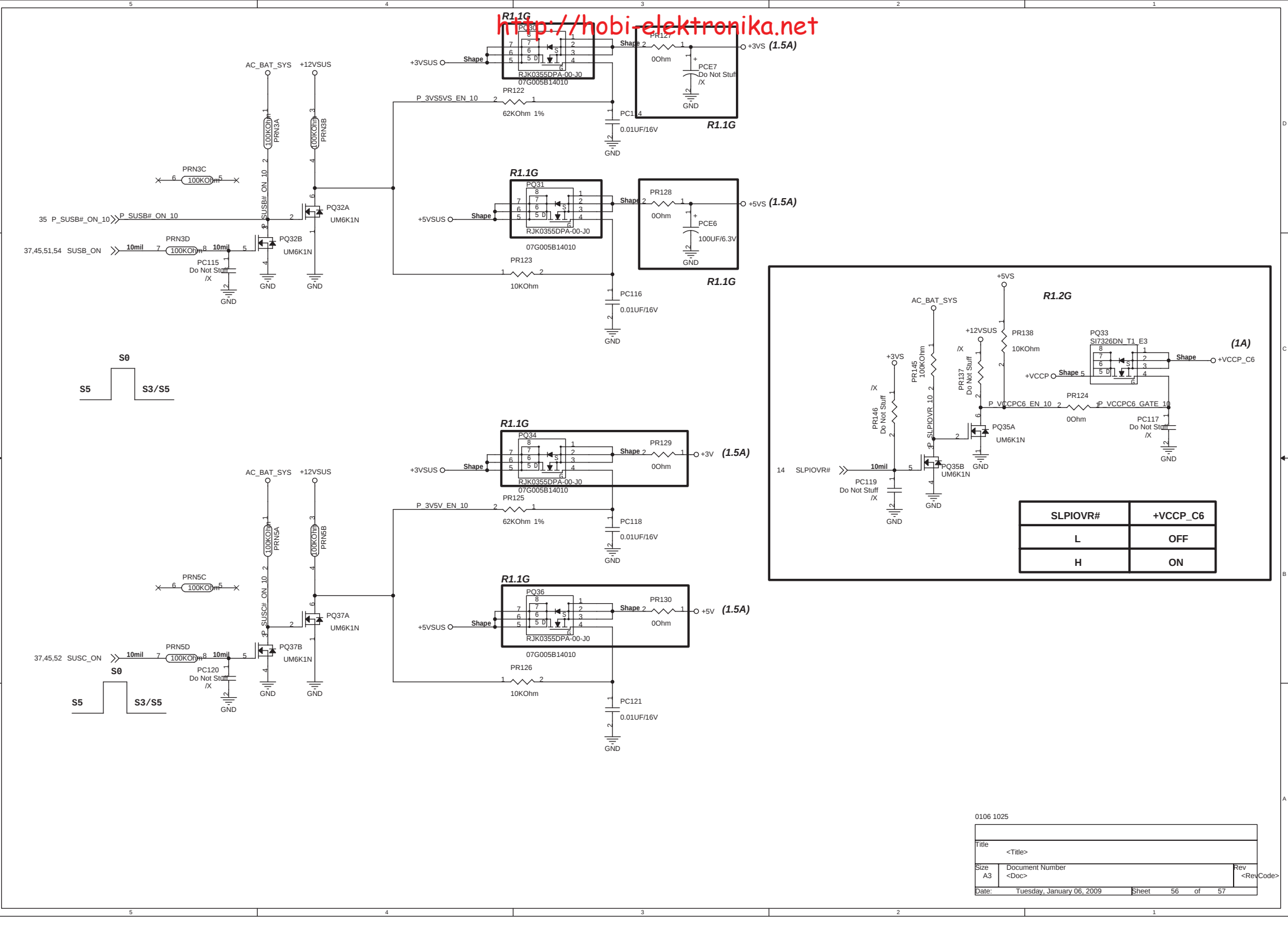




0106 1025

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC.		Engineer: Joy Zhou	
Size	Project Name	T91	Rev 1.2G
A3			
Date: Tuesday, January 06, 2009		Sheet	54 of 57

		Title : CHARGER	
ASUSTek Computer INC.		Engineer: Yaohwa_Chen	
Size Custom	Project Name T91		Rev 1.2G
Date: Tuesday, January 06, 2009		Sheet	55 of 57



Top-Left Section: USB Input and Level Shifters

AC_BAT_SYS +12VSUS

PRN3C 100kOhm

PRN3A 100kOhm

PRN3B 100kOhm

PRN3D 100kOhm

PC115 Do Not Stuff /X

PC116 0.01UF/16V

PC117 Do Not Stuff /X

PC118 0.01UF/16V

PC119 Do Not Stuff /X

PC120 Do Not Stuff /X

PC121 0.01UF/16V

PC122 0.01UF/16V

PC123 0.01UF/16V

PC124 0.01UF/16V

PC125 0.01UF/16V

PC126 0.01UF/16V

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PC275 0.01UF/16V

PC276 0.01UF/16V

PC277 0.01UF/16V

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PC280 0.01UF/16V

PC281 0.01UF/16V

PC282 0.01UF/16V

PC283 0.01UF/16V

PC284 0.01UF/16V

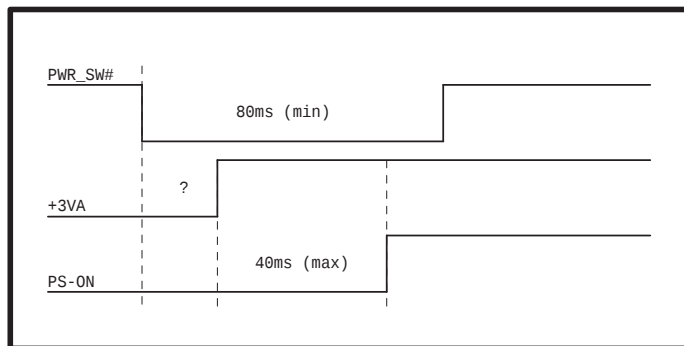
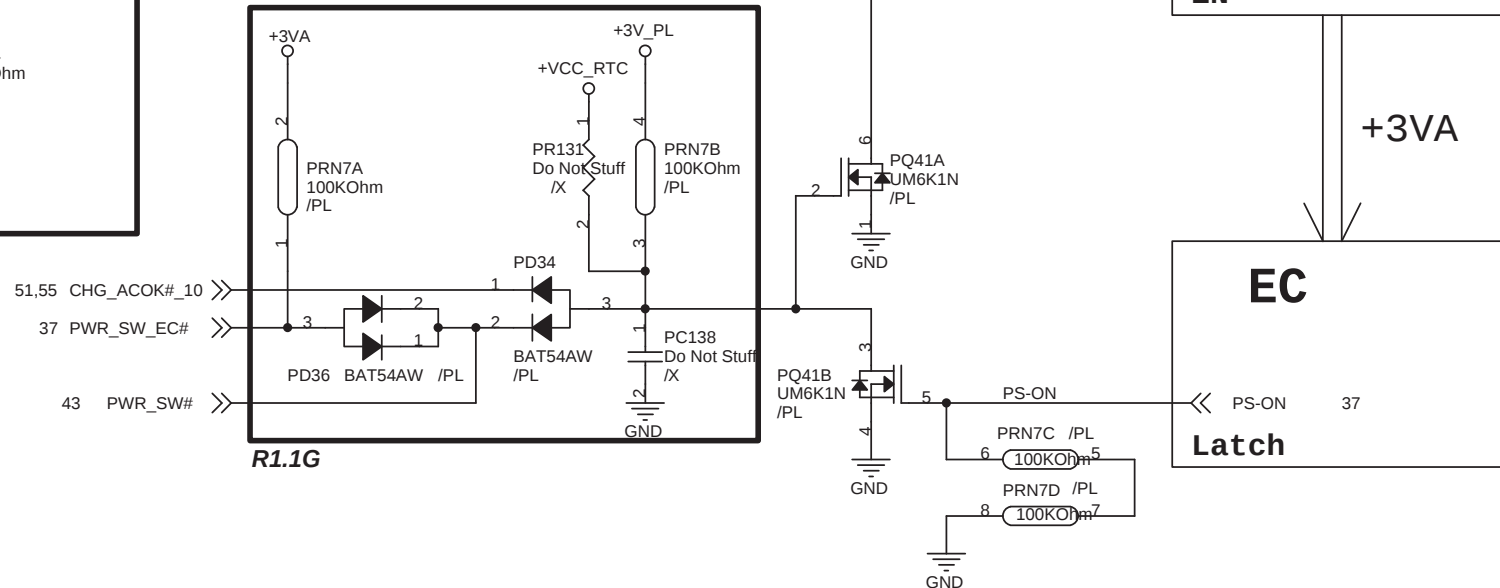
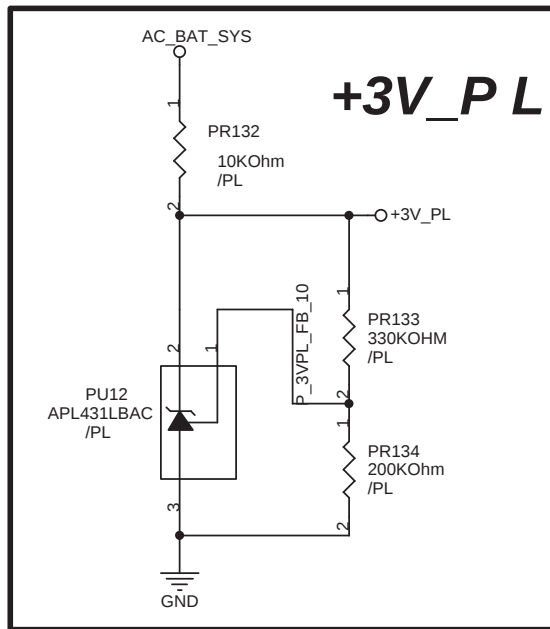
PC285 0.01UF/16V

PC286 0.01UF/16V

PC287 0.01UF/16V

PC288 0.01UF/16V

PC289 0.01UF/16V



0106 1025

ASUS		Title : Power Latch	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A4	Project Name T91		Rev 1.2G
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