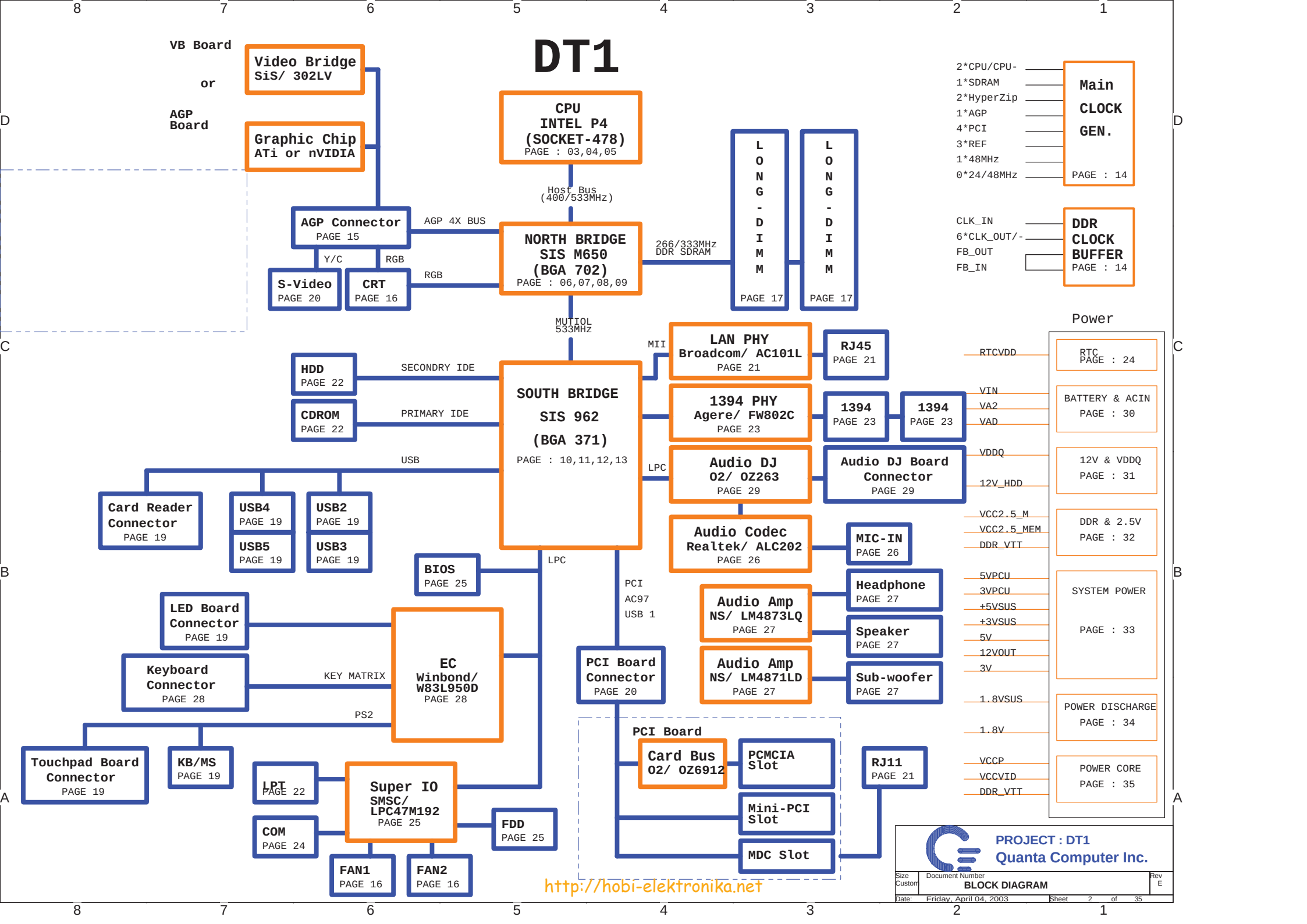
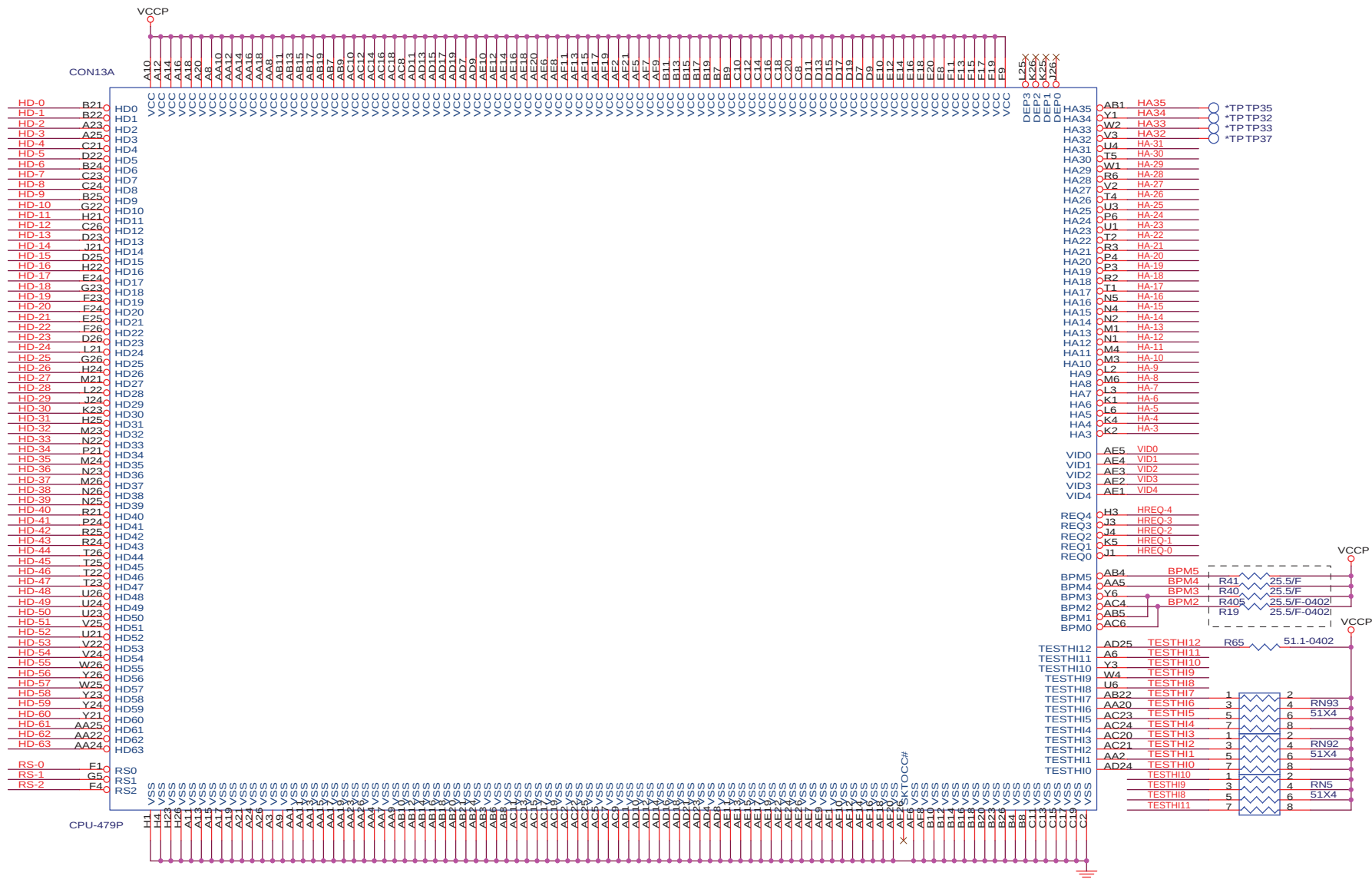


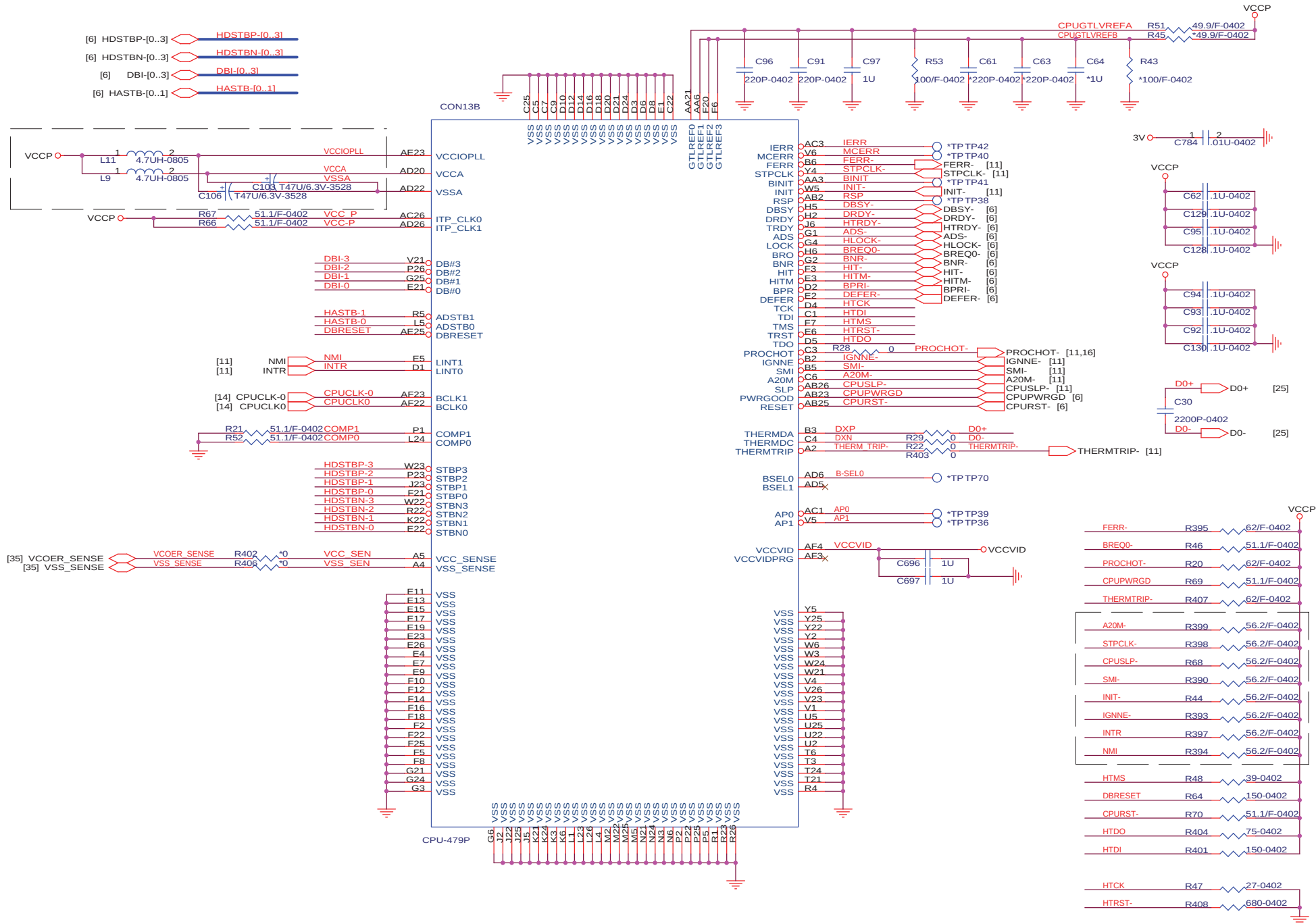
QUANTA COMPUTER INC.

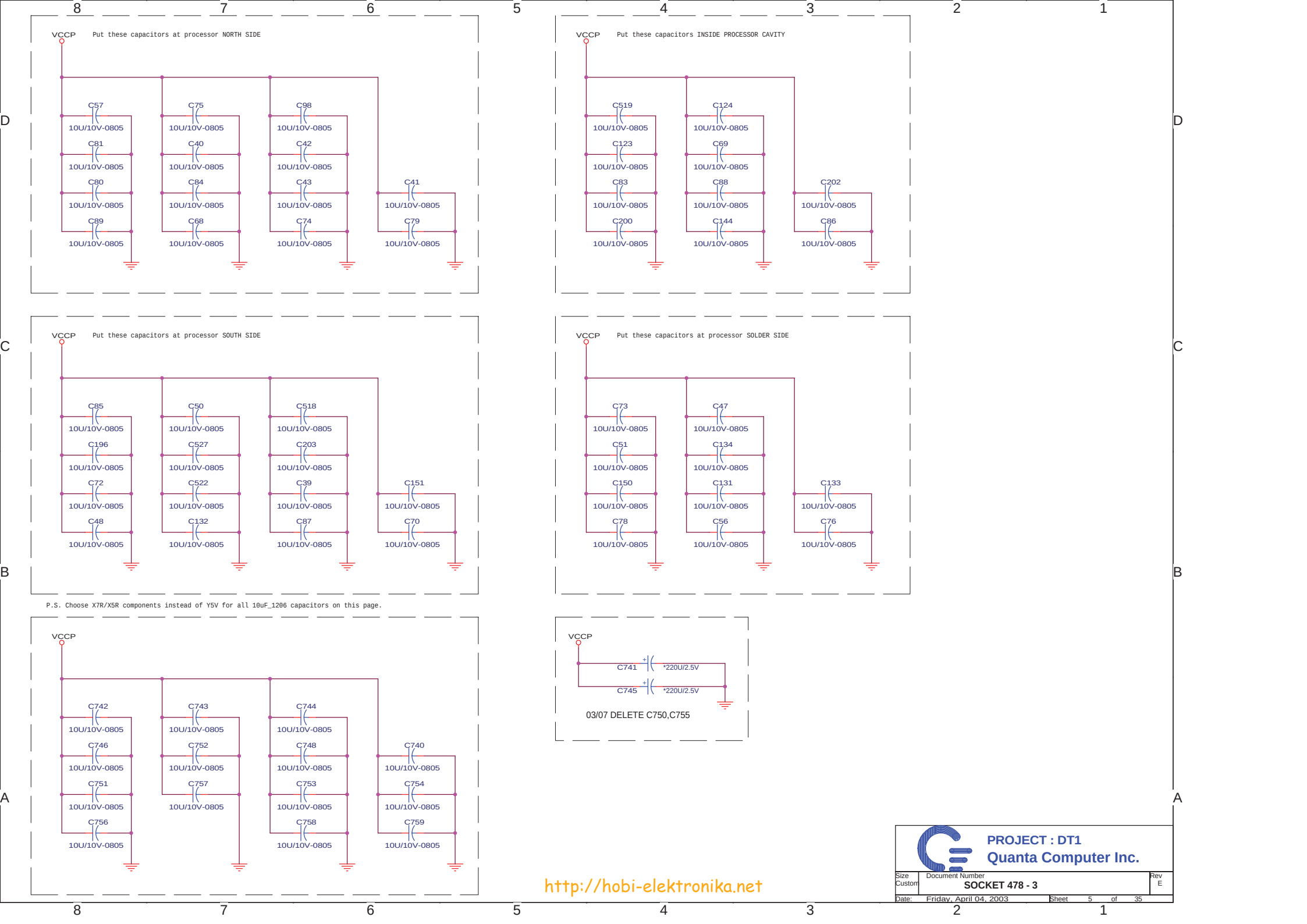
(March/31/2003) Rev : E

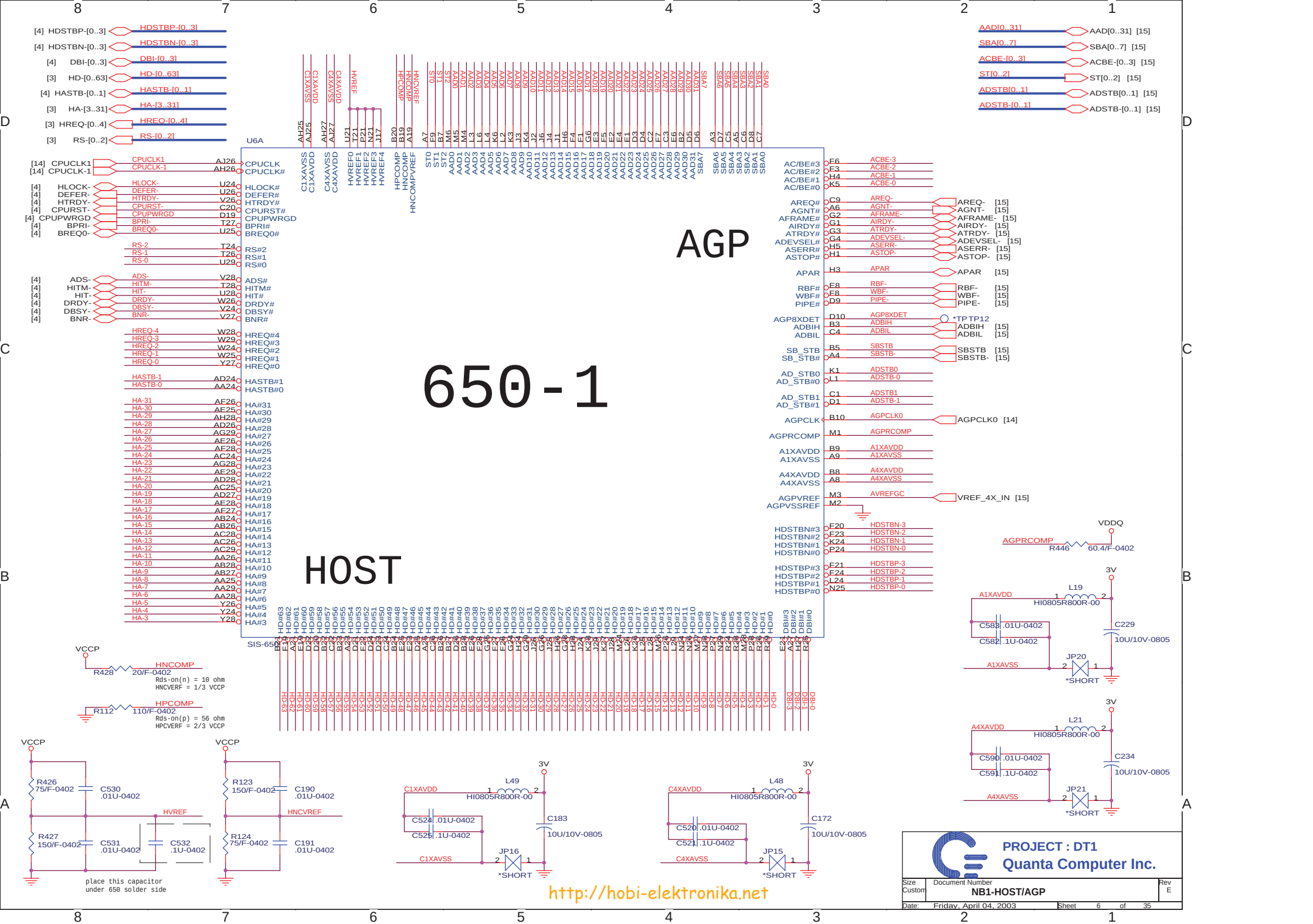
PAG	Content	PAG	Content
1	Cover Page	31	POWER 12V_HDD & AGP(VDDQ)
2	650 System Block Diagram	32	POWER - DDR & 2.5V
3	SOCKET 478 - 1	33	SYSTEM POWER
4	SOCKET 478 - 2	34	POWER DISCHARGE
5	SOCKET 478 - 3	35	POWER CORE
6	650-1 (Host/AGP)	36	
7	650-2 (Memory for DDR)	37	
8	650-3 (HyperZip/VGA/Misc.)	38	
9	650-4 (Powers)	39	
10	962-1 (PCI/IDE/HyperZip)	40	
11	962-2 (Misc. Signals)	41	
12	962-3 (USB/1394/IPB)	42	
13	962-4 (Powers)	43	
14	Main Clock Generator & BUFFER	44	
15	AGP SLOT	45	
16	CRT,LCD LID,BLON & FAN CONTROL	46	
17	DIMM1 & DIMM2	47	
18	DDR_TERMINASION	48	
19	USB,LED/B,PS2,PW & RST CONN	49	
20	PCI CONN & PULL UP	50	
21	LAN PHY (AC101L) & RJ45,RJ11	51	
22	IDE (HDD & CDR0M) & LPT	52	
23	1394(RTL8801B)	53	
24	HOLE,EMI,RTC & COM1	54	
25	SUPER_I/O & BIOS ROM	55	
26	AUDIO CODEC(ALC650)	56	
27	AUDIO AMPLIFIER(LM4873 & 4871)	57	
28	EC W83L950D	58	
29	AUDIO DJ (0Z263)	59	
30	BATTERY CONN & POWER JACK	60	

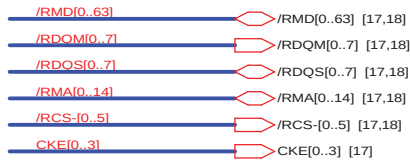




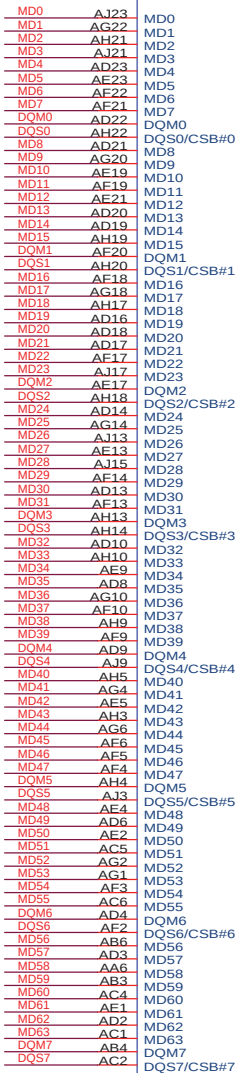
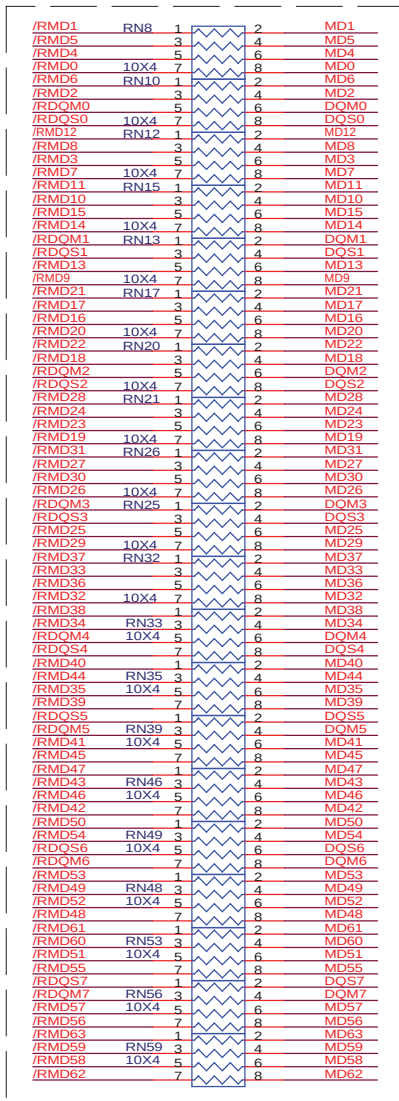






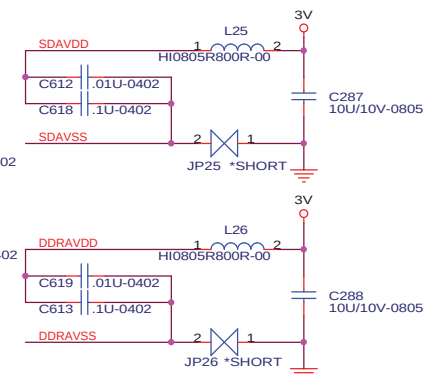
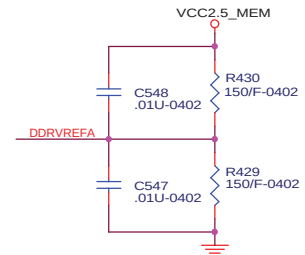
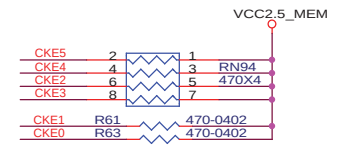
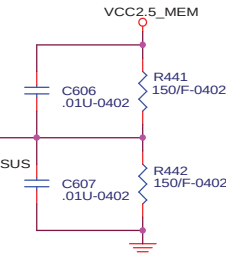
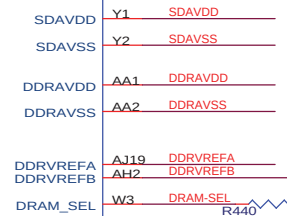
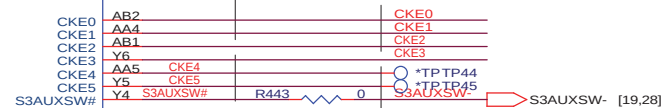
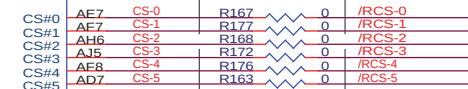
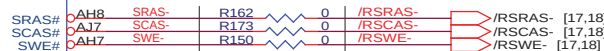
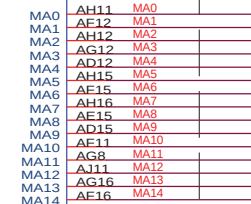
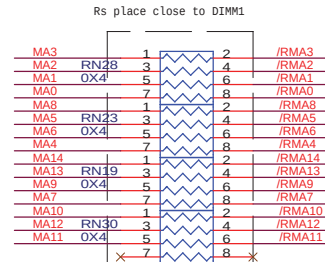


Rs place close to DIMM1



SIS-650

650-2



PROJECT : DT1
Quanta Computer Inc.

NOTE: This page is for universal PCB design(suitable for both 645 or 650)

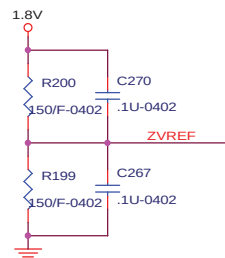
NB Hardware Trap Table

	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)			0
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

[10] ZAD[0..15] ZAD[0..15]

[10] ZSTB[0..1] ZSTB[0..1]

[10] ZSTB-[0..1] ZSTB-[0..1]



[14] ZCLK0 ZCLK0

[10] ZUREQ ZUREQ

[10] ZDREQ ZDREQ

ZSTB0 T3

ZSTB-0 T1

ZSTB1 P1

ZSTB-1 P3

ZAD0 T4

ZAD1 R3

ZAD2 T5

ZAD3 T6

ZAD4 R2

ZAD5 R6

ZAD6 R1

ZAD7 R4

ZAD8 P4

ZAD9 N3

ZAD10 P5

ZAD11 P6

ZAD12 N1

ZAD13 N6

ZAD14 N2

ZAD15 N4

ZVREF U3

VDDZCMP V5

ZCMP_N U4

ZCMP_P U2

VSSZCMP V6

Z1XAVDD W1

Z1XAVSS W2

Z4XAVDD V2

Z4XAVSS V1

U6C

VGA

Stereo Glass

HyperZip

650-3

SIS-650

[10,15,20,21,22,25,28,29] PCIRST- PCIRST-

[11,28] PWRGD PWRGD

[11,24] AUXOK AUXOK

VOSC1

ROUT

GOUT

BOUT

HSYNC

VSNC

VGPI00

VGPI01

INT#A

CSYNC

RSYNC

LSYNC

VCOMP

VRSET

VVBWN

DACAVDD1

DACAVSS1

DACAVDD2

DACAVSS2

DCLKAVDD

DCLKAVSS

ECLKAVDD

ECLKAVSS

C15 REFCLK0 REFCLK0 [14]

A12 R-OUT R438 BK1608LL680 ROUT [16]

B13 G-OUT R437 BK1608LL680 GOUT [16]

A13 B-OUT R436 BK1608LL680 BOUT [16]

E13 H-SYNC R434 BK1005LL121 HSYNC [16]

E13 V-SYNC R433 BK1005LL121 VSYNC [16]

D13 DDC1-CLK R435 BK1005LL121 DDC1CLK [16]

D12 DDC1-DATA R439 BK1005LL121 DDC1DATA [16]

B11 INT-A INT-A [10,15,20]

E12 CSYNC

A11 RSYNC

E12 LSNC

E14 VCOMP

D14 VRSET

E14 VVBWN

B12 DACAVDD

C12 DACAVSS

C13 DACAVDD

C14 DACAVSS

B15 DCLKAVDD

A15 DCLKAVSS

B14 ECLKAVDD

A14 ECLKAVSS

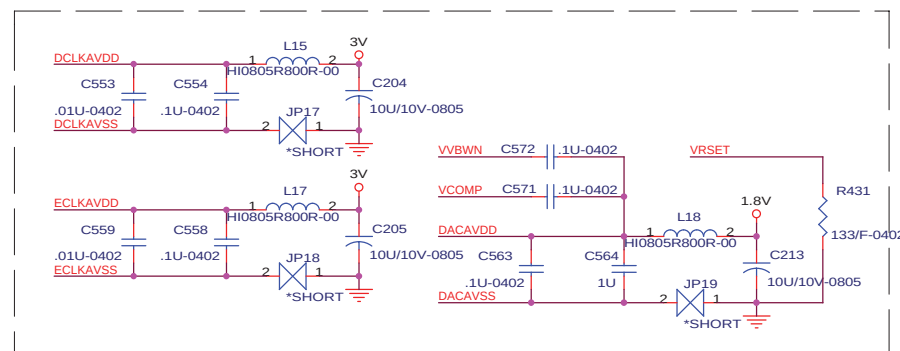
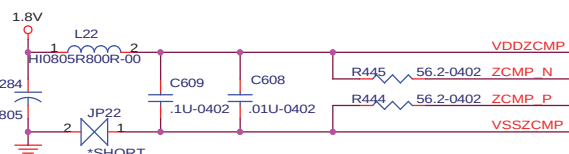
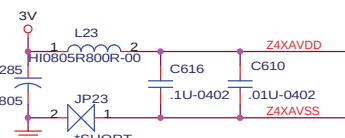
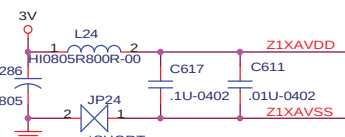
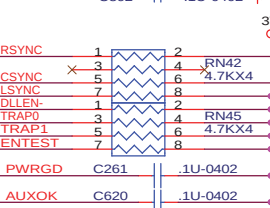
ROUT C603 *.1U-0402

GOUT C602 *.1U-0402

BOUT C601 *.1U-0402

HSYNC C593 *.1U-0402

VSNC C592 *.1U-0402



PROJECT : DT1

Quanta Computer Inc.

Size: Custom

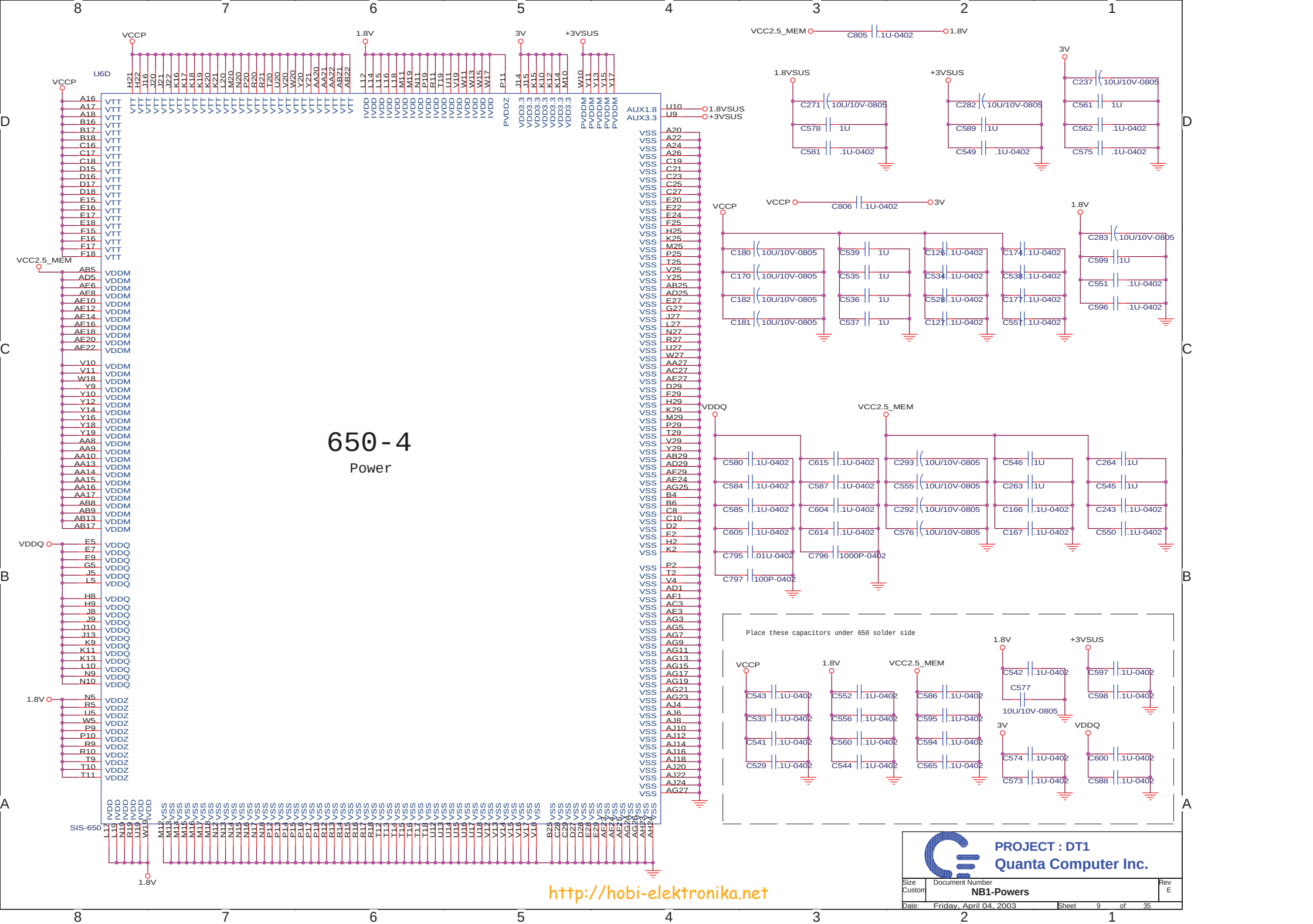
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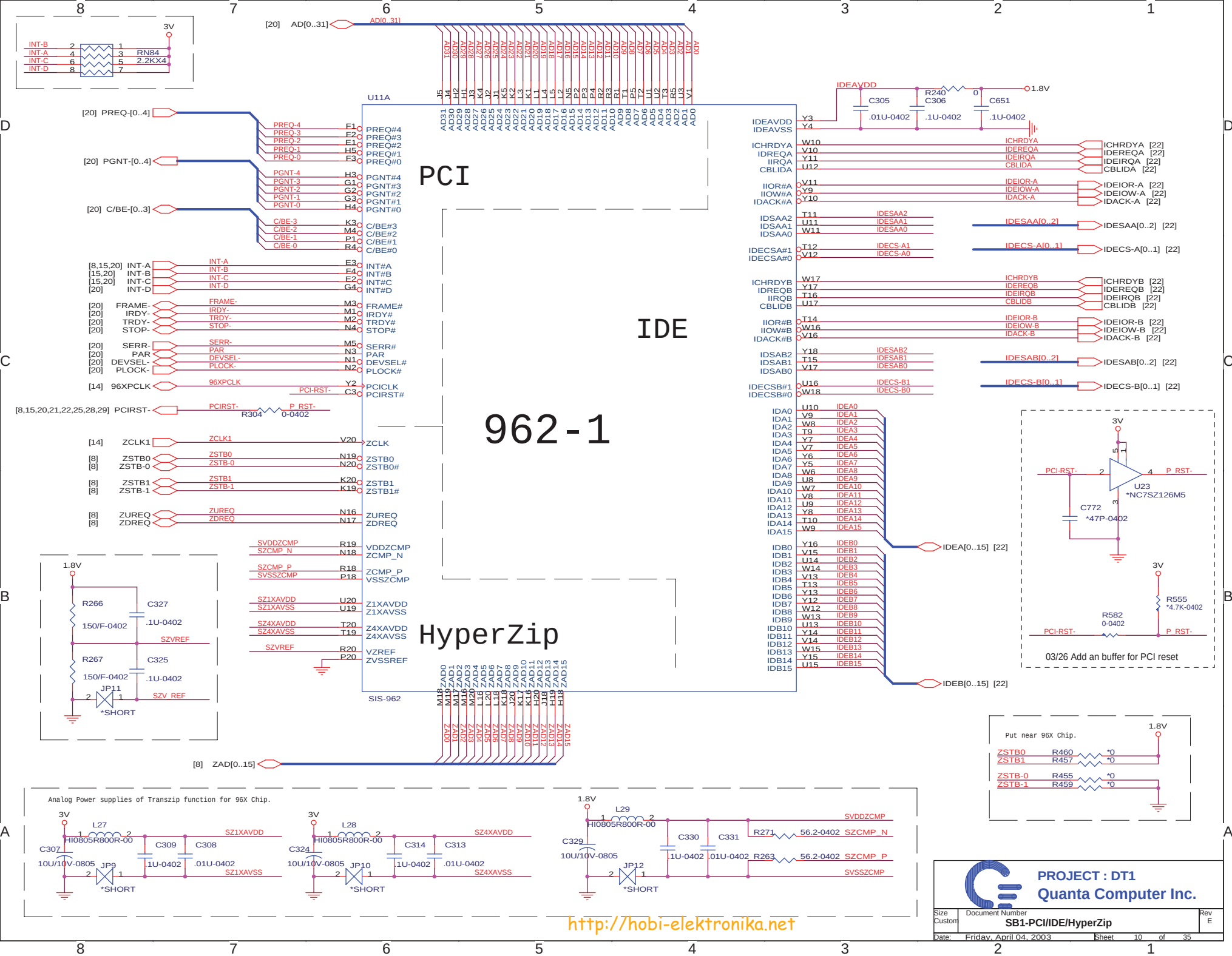
Date: Friday, April 04, 2003

Sheet: 8 of 35

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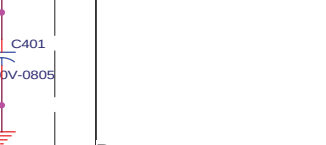
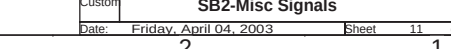
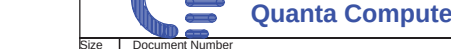
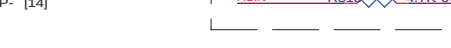
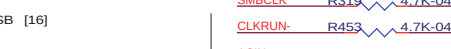
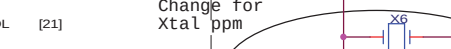
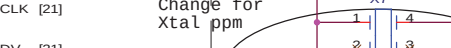
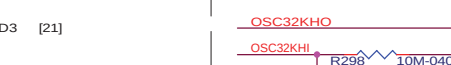
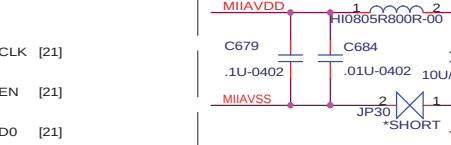
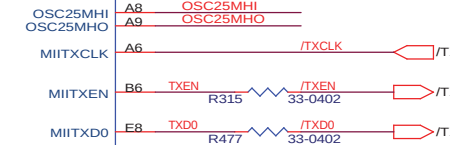
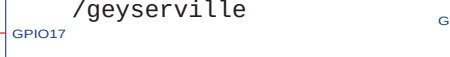
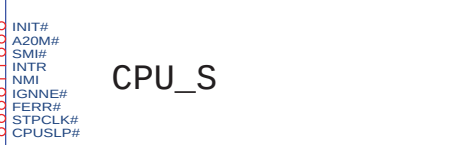
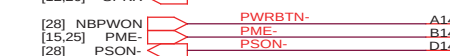
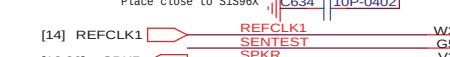
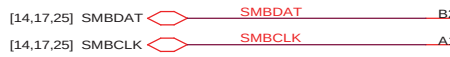
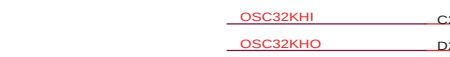
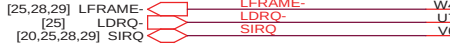
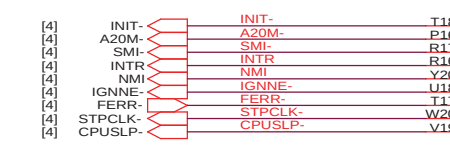


D

C

B

A



CPU_S

APIC

LPC

RTC

962-2

GPIO

AC97

ACPI
/others

GPIO

KBC

/geyserville

SIS-962

MII



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02/28 X7 COMPONENT FROM BG332768721 TO BG33768216

Change for
Xtal ppm

02/28 C399 FROM 20P TO 10P, C400 FROM 15P TO 10P

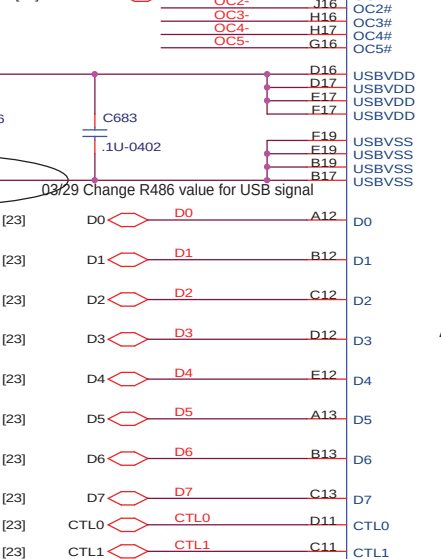
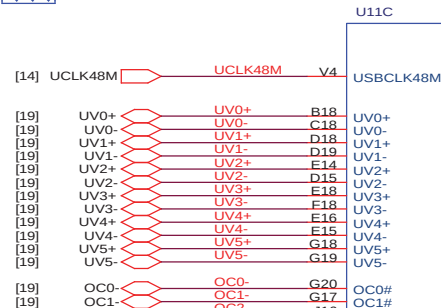
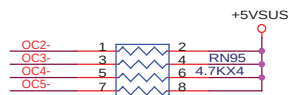
Change for
Xtal ppm

NEED NOT to place
close to 96X

GPIO pins pull down
NEED NOT to place

PROJECT : DT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB2-Misc Signals	E
Date:	Friday, April 04, 2003	Sheet 11 of 35



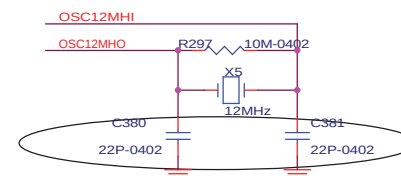
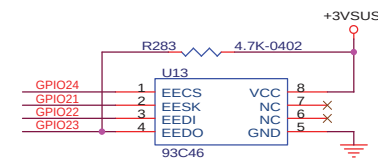
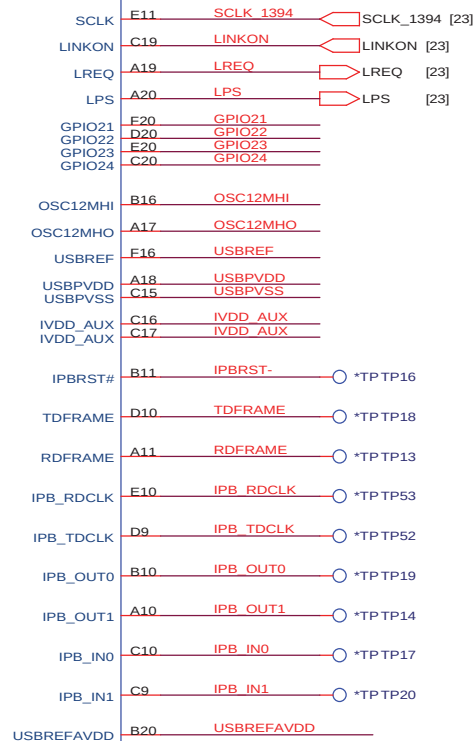
USB

962-3

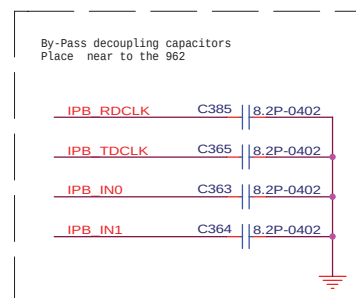
OTHERS

ACR-IPB
/ADSL
(For 962,963)

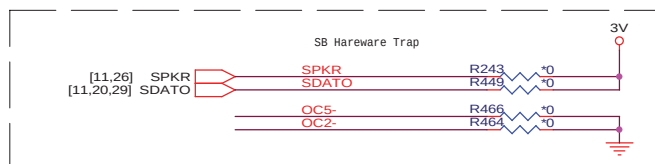
ACR-WIRELESS
/BLUETOOTH
(ONLY FOR 963)



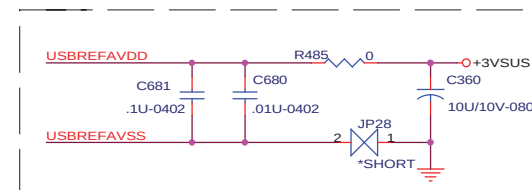
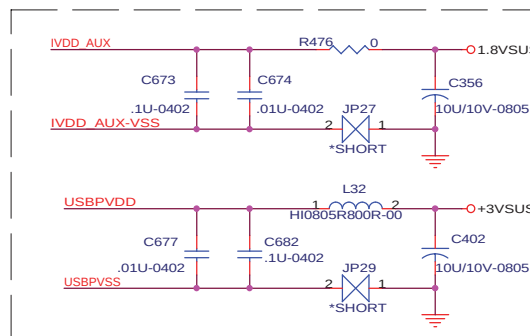
3/29 Modify for Xtal



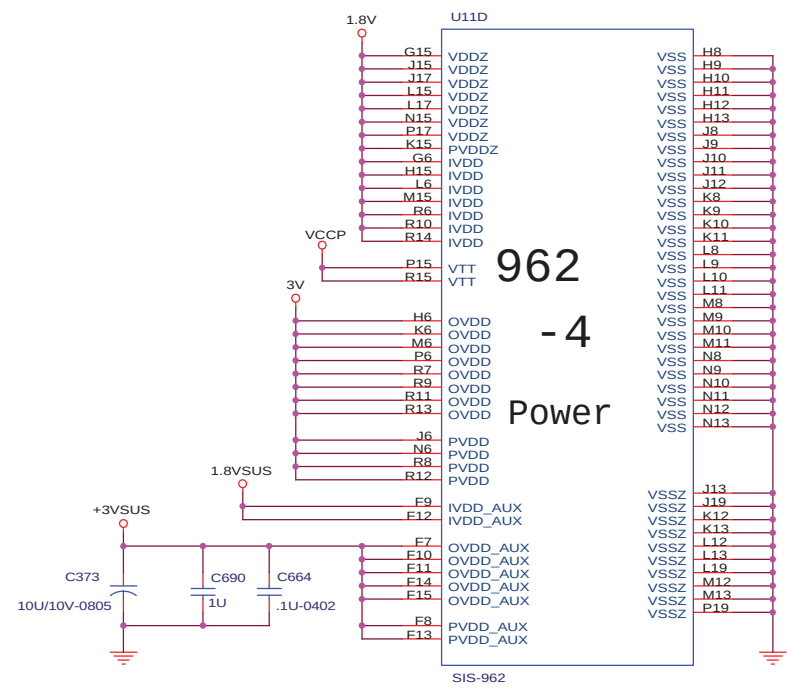
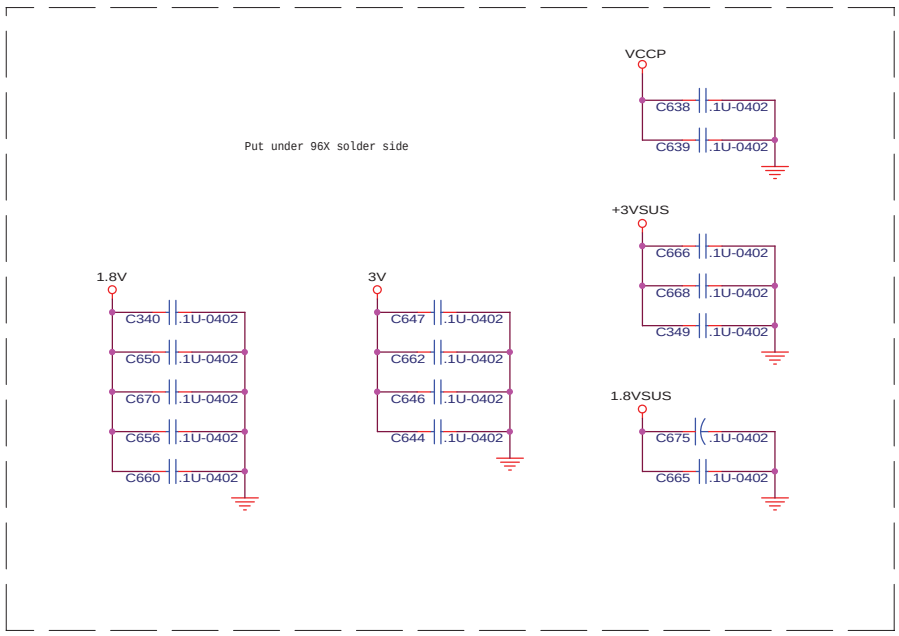
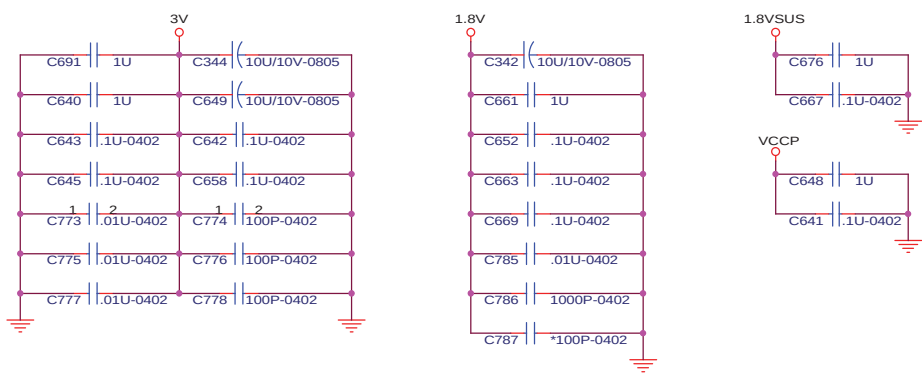
By-Pass decoupling capacitors
Place near to the 962



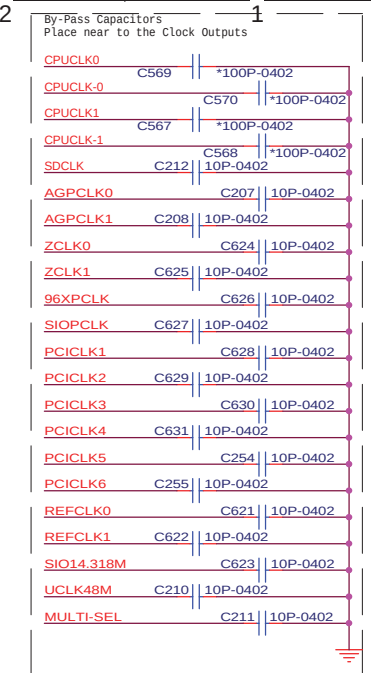
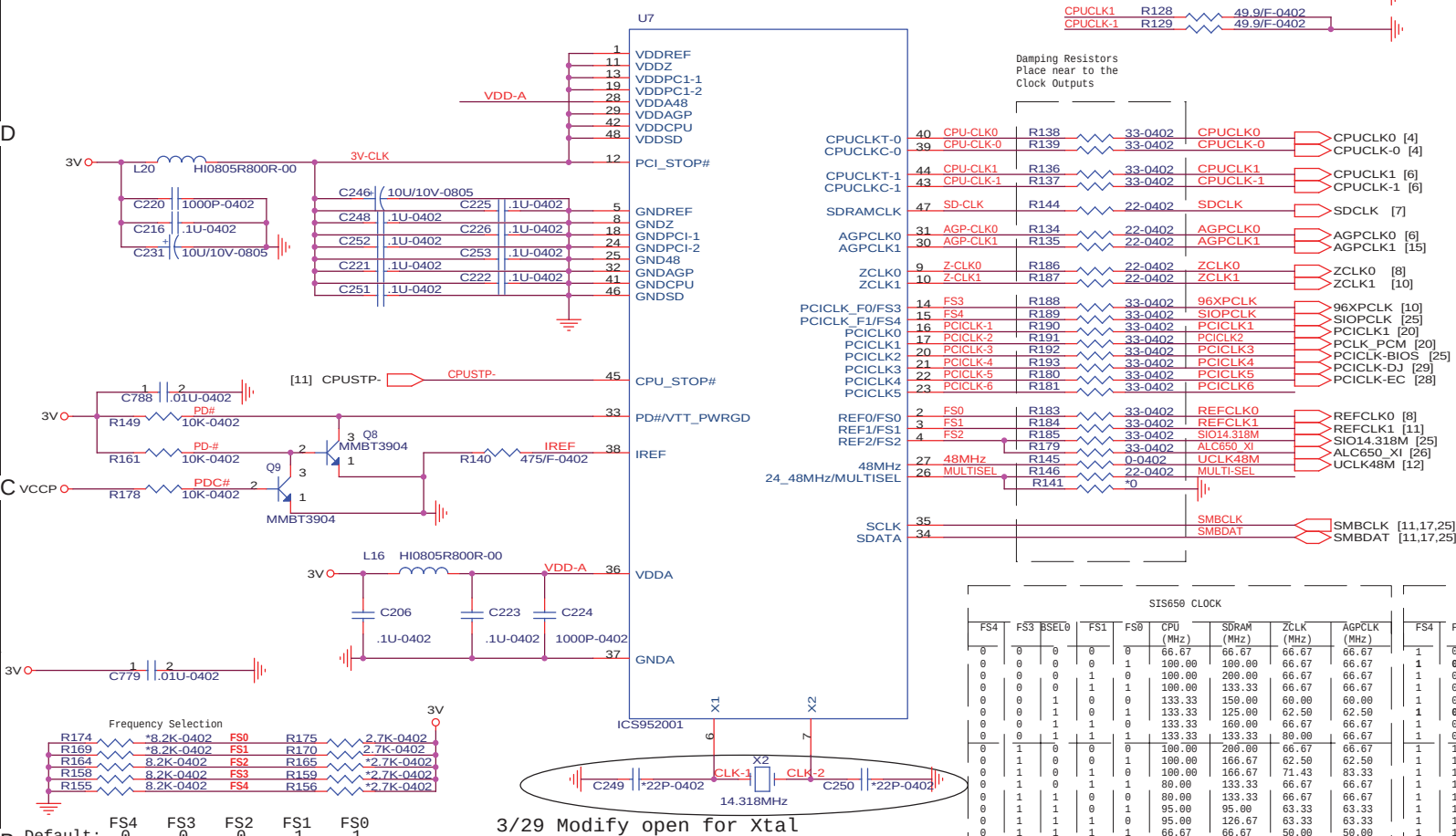
	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDATO(Trap mode)	ROM	PCI_AD	0
OC2-	enable	disable	1
OC5-	enable	disable	1



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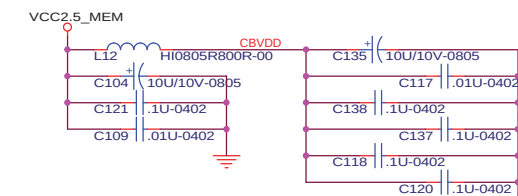
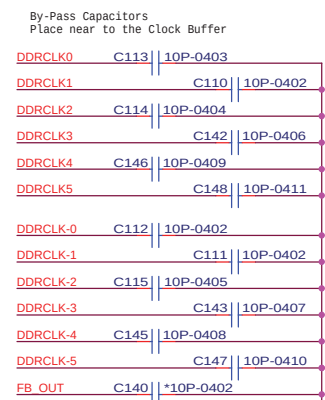
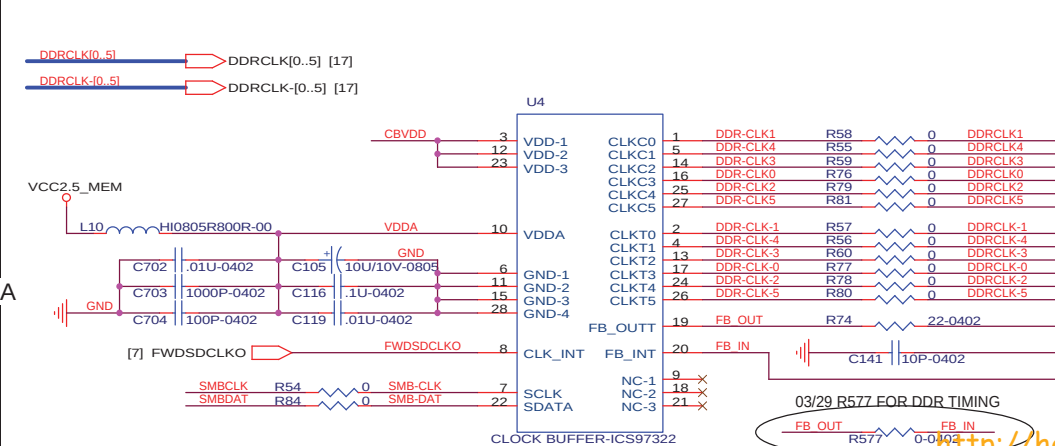
⁶MAIN ⁵CLOCK GENERATOR

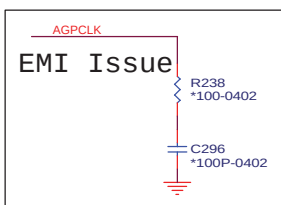


SIS650 CLOCK								
FS4	FS3	BSEL0	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)
0	0	0	0	0	66.67	66.67	66.67	66.67
0	0	0	0	1	100.00	67.90	66.67	66.67
0	0	0	1	0	100.00	200.00	66.67	66.67
0	0	0	1	1	100.00	133.33	66.67	66.67
0	0	1	0	0	133.33	150.00	60.00	60.00
0	0	1	0	1	133.33	125.00	62.50	62.50
0	1	0	1	1	133.33	160.00	66.67	66.67
0	1	0	1	0	133.33	333.33	66.00	66.00
0	1	1	0	0	100.00	200.00	66.67	66.67
0	1	1	0	1	100.00	166.67	62.50	62.50
0	1	1	0	0	100.00	166.67	71.43	83.33
0	1	1	1	1	80.00	133.33	66.67	66.67
0	1	1	1	0	80.00	133.33	66.67	66.67
0	1	1	0	1	95.00	95.00	63.33	63.33
0	1	1	0	0	95.00	126.67	63.33	63.33
0	1	1	1	1	66.67	66.67	50.00	50.00

SI5650 CLOCK								
FS4	FS3	BSEL0	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)
1	0	0	0	0	105.00	146.00	70.00	70.00
1	0	0	1	0	100.00	100.00	67.27	67.27
1	0	0	1	0	100.00	144.00	72.00	72.00
1	0	0	1	1	100.00	134.53	67.27	67.27
1	0	1	0	0	112.00	149.33	74.67	74.67
1	0	1	0	1	133.33	100.00	66.67	66.67
1	0	1	1	0	133.33	133.33	66.67	66.67
1	0	1	1	1	133.33	166.67	66.67	66.67
1	1	0	0	0	100.00	100.00	80.00	66.67
1	1	0	0	1	100.00	100.00	80.00	66.67
1	1	0	1	0	100.00	166.67	83.33	62.50
1	1	0	1	1	133.33	160.00	80.00	66.67
1	1	1	0	0	100.00	133.00	100.00	66.67
1	1	1	0	1	100.00	100.00	100.00	66.67
1	1	1	1	0	100.00	166.67	100.00	62.50
1	1	1	1	1	133.33	160.00	100.00	66.67

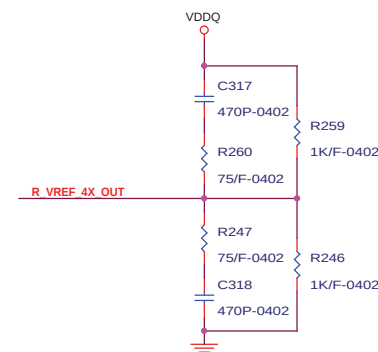
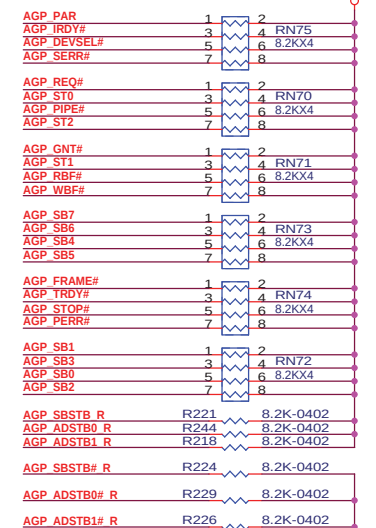
CLOCK BUFFER



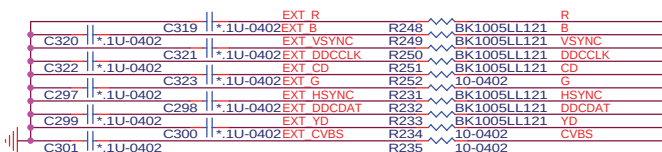
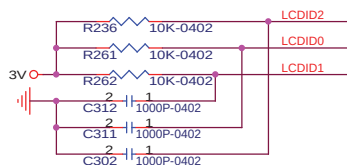


AGP 4X OUT INTERFACE

```
AGP_PLUG:
HI:  USE AGP GRAPHIC
LO:  USE ATI GRAPHIC
```



PLACE CLOSE TO CONNECTOR



02/26 +5VSUS CHANGE TO 5V

<http://hobi-elektronika.net>

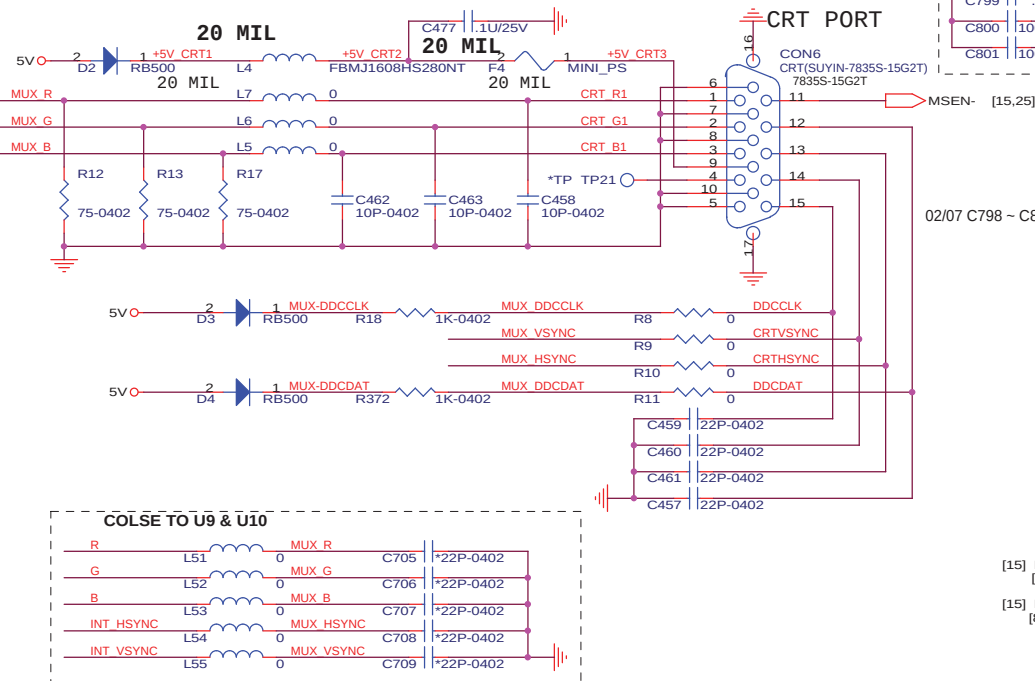


PROJECT : DT1
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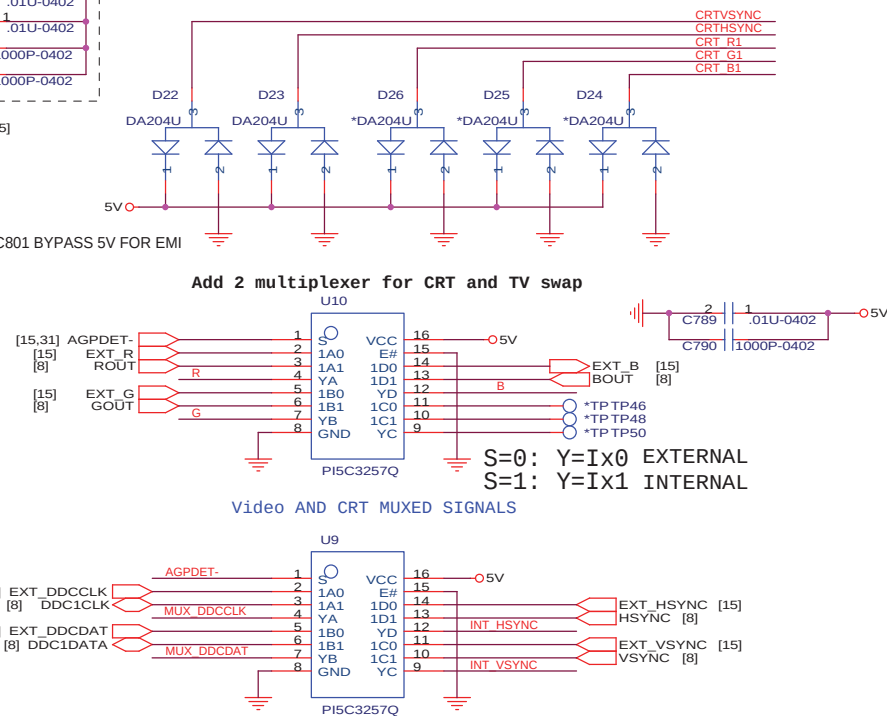
AGP SLOT

Size Custom	Document Number AGP SLOT
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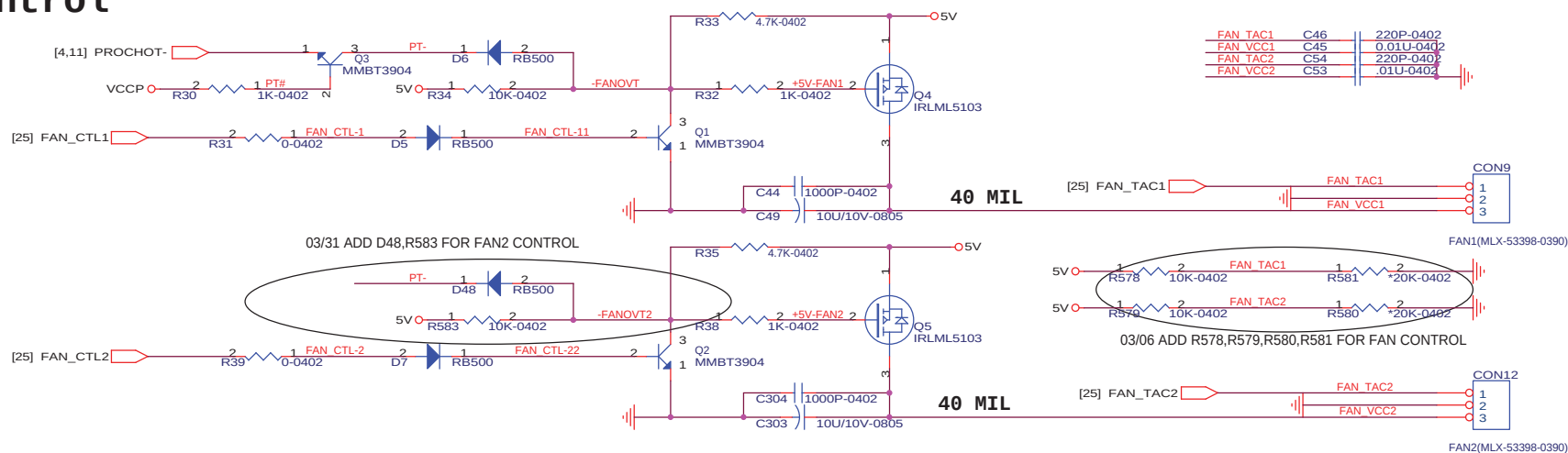
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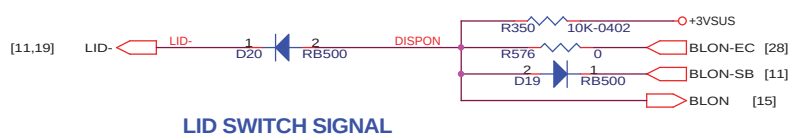
PS0T05LC

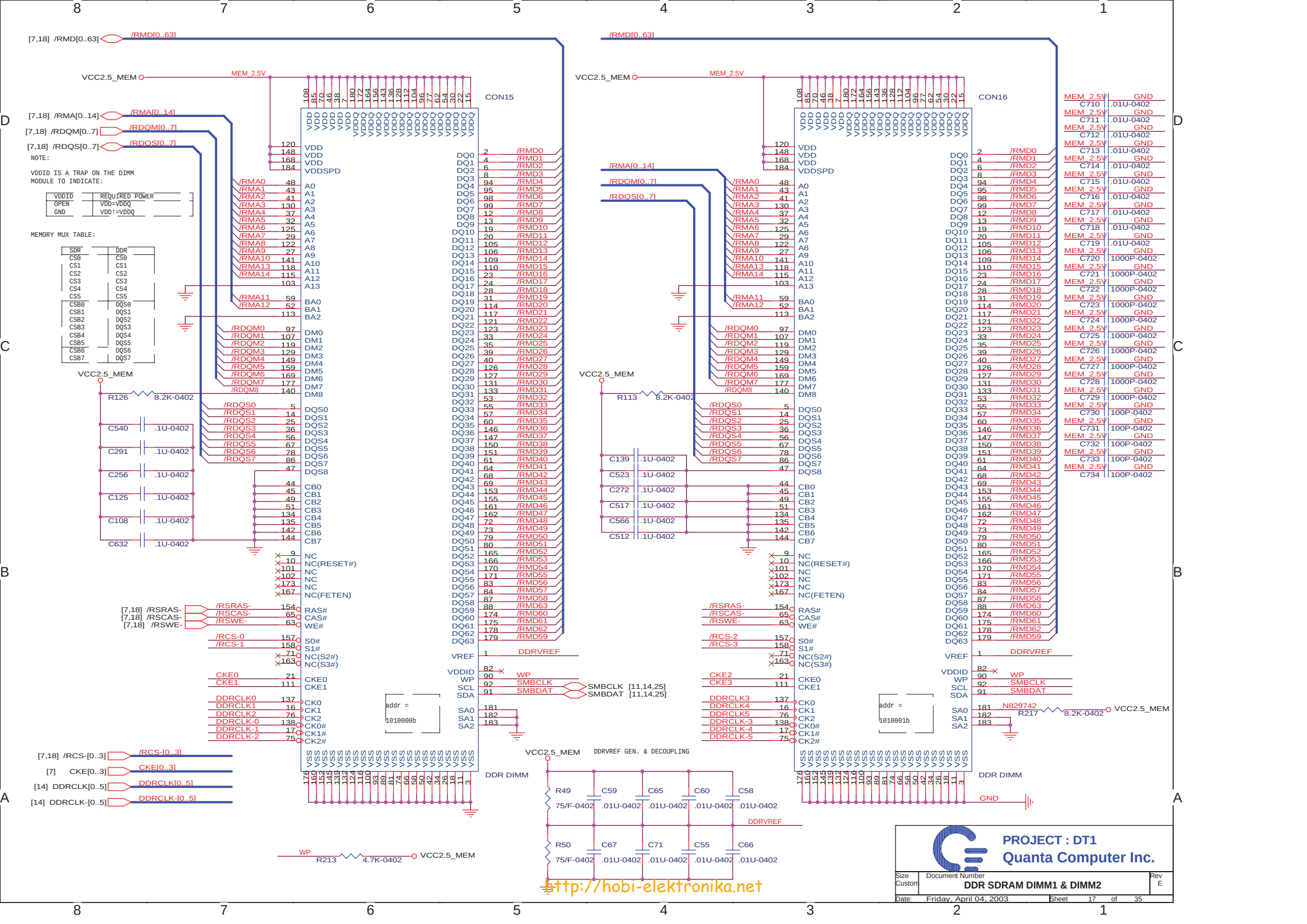


FAN Control



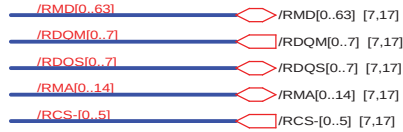
LCD-LID



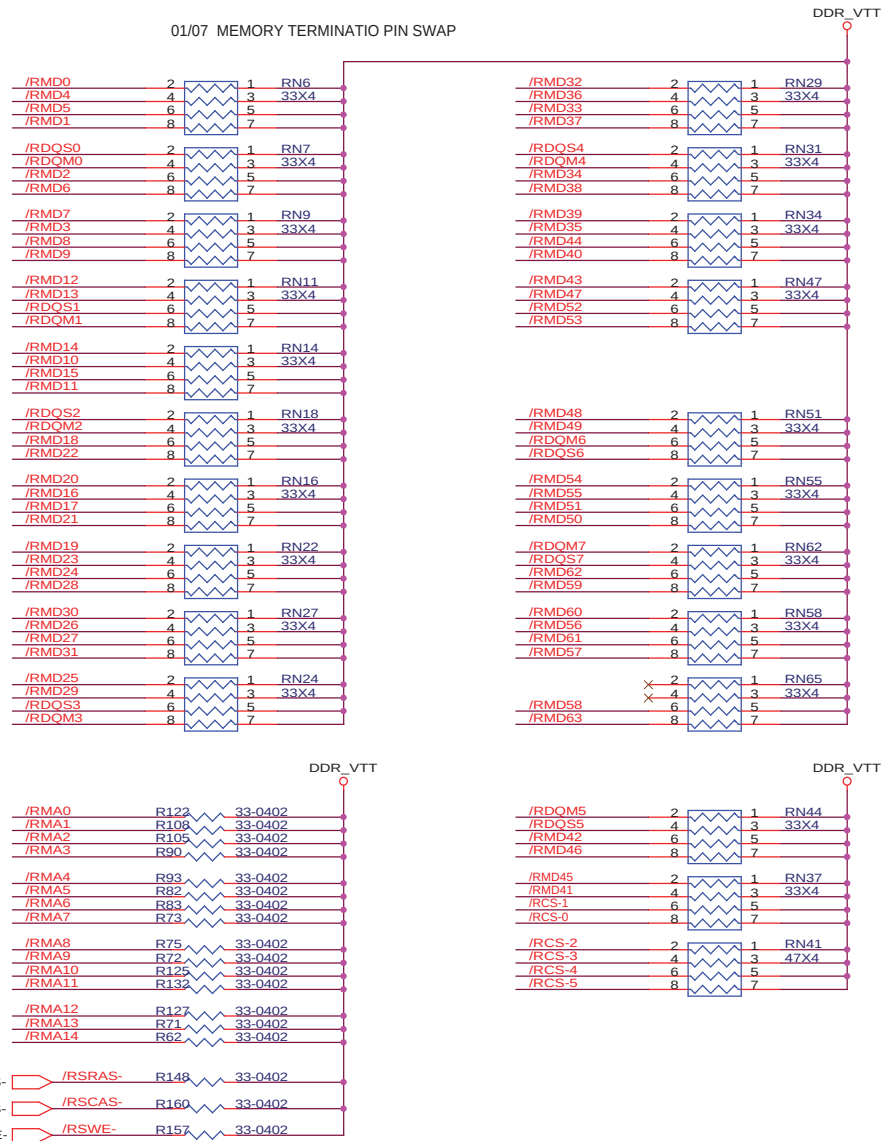


SSTL-2 Termination Resistors

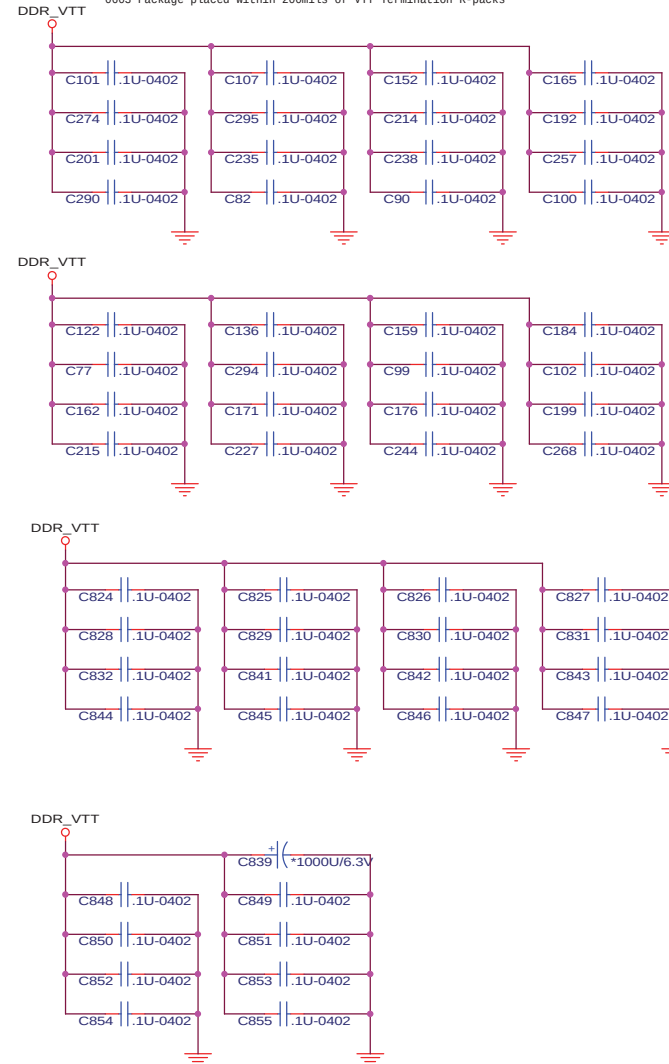
MD/DQM(/DQS) MA/Control CS CKE	SDR	Rs	DDR	Rs	Rtt
	LV-CMOS LV-CMOS OD 3.3V	0/10/- 10 0	SSTL-2 SSTL-2 OD 2.5V	10 0	33 33 47



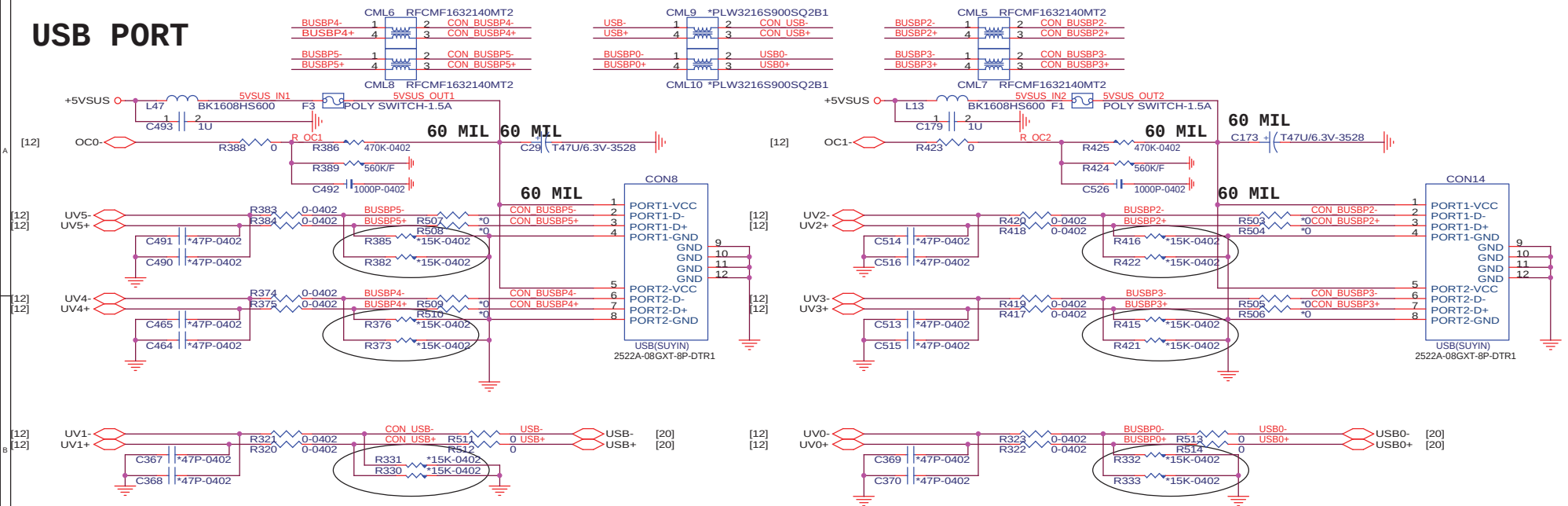
01/07 MEMORY TERMINATIO PIN SWAP



DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs



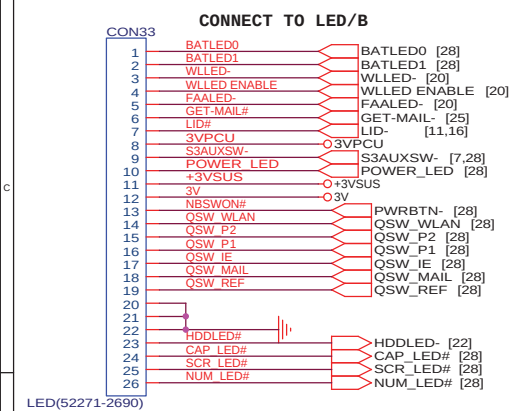
USB PORT



LED/B CONNECTOR

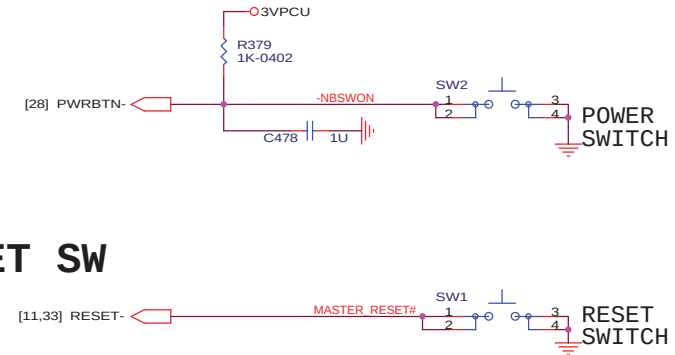
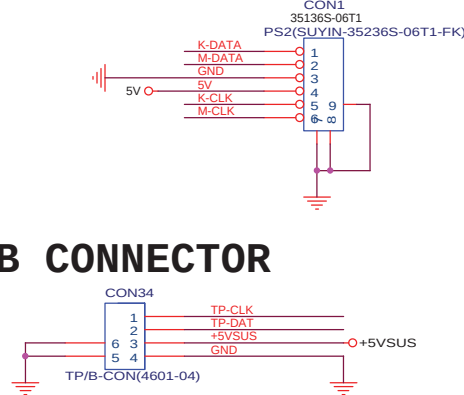
PS/2

POWER SW



TP/B CONNECTOR

RESET SW



QSW P1	C262	*1U-0402	C452	*1U-0402	3V
QSW P2	C266	*1U-0402	C482	*1U-0402	+5VSUS
NBSWON#	C266	*1U-0402	C482	*1U-0402	3VPCU
WLED ENABLE	C233	220P-0402	C484	*1U-0402	+3VSUS
FALED-	C233	220P-0402	C245	*1U-0402	QSW_REF
QSW WLAN	C247	220P-0402	C269	*1U-0402	BATLED0
QSW MAIL	C247	220P-0402	C228	*1U-0402	BATLED1
QSW IE	C258	*1U-0402	C230	*1U-0402	WLED-
HDDL#	C260	*1U-0402	C232	220P-0402	GET-MAIL#
CAP_LED#	C273	220P-0402	C239	220P-0402	TP-DAT
SCR_LED#	C275	220P-0402	C242	*47P-0402	TP-CLK
NUM_LED#	C280	220P-0402	C241	*47P-0402	TP-CLK
	C281	220P-0402	C240	220P-0402	

03/06 C241,C241 47P UNSTAFF

02/28 C45,C455,C456,C457 FROM 100P CHANGE TO 270P FOR EMI

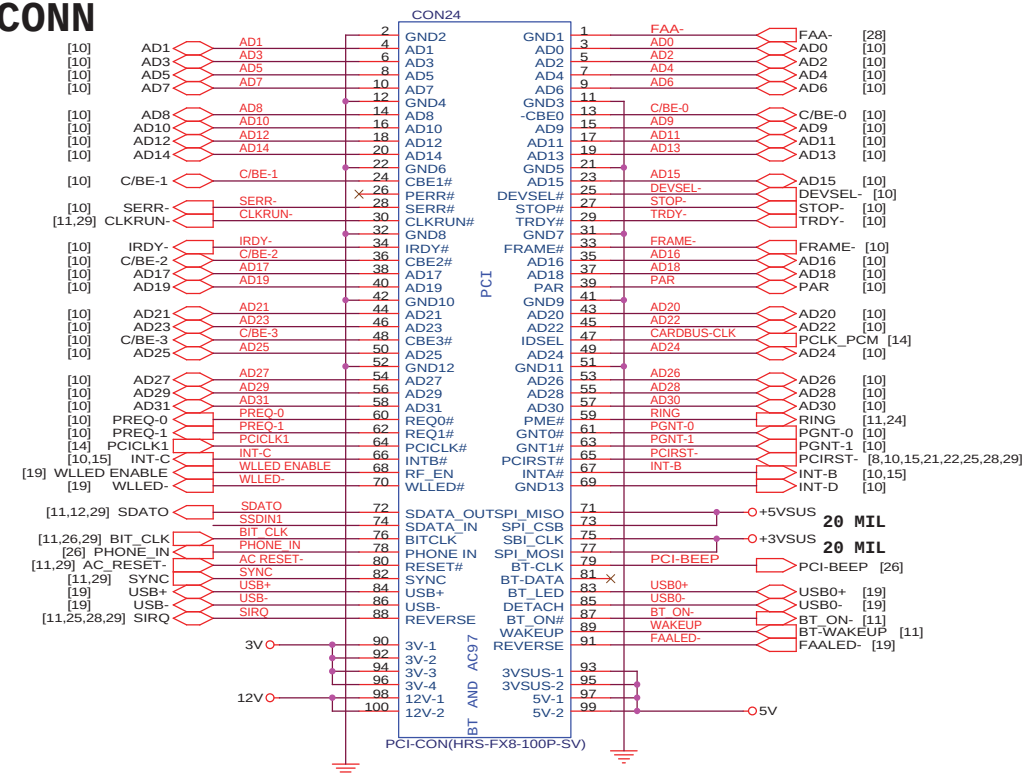


03/06 C453,C454,C455,C456 UNSTAFF

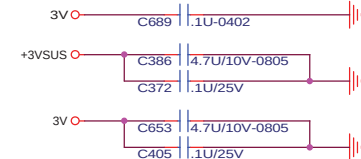
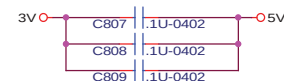
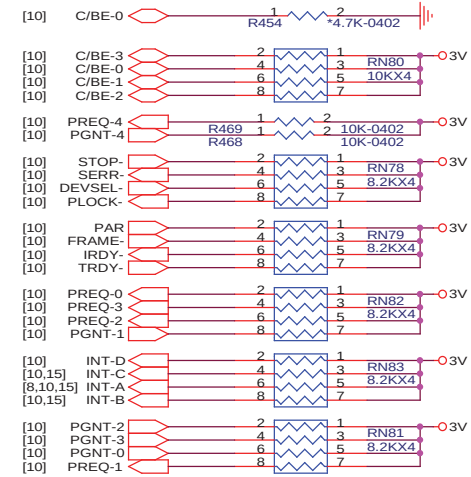
PROJECT : DT1
Quanta Computer Inc.

Size: Document Number: **USB,LED/B,PS2,PW & RST CONN** Rev: E
Date: Friday, April 04, 2003 Sheet: 19 of 35

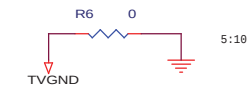
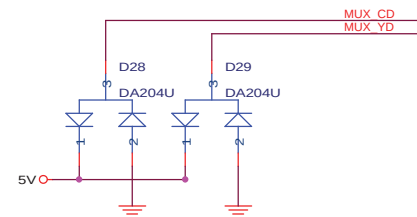
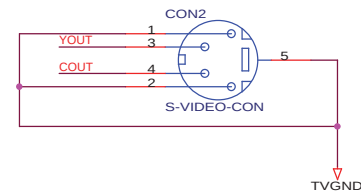
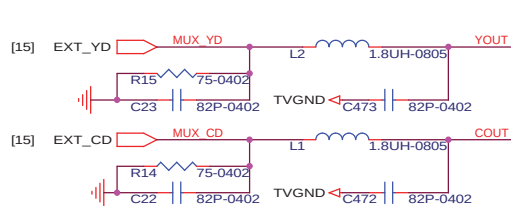
PCI-CONN



PCI PULL UP



S-VIDEO(TV OUT)



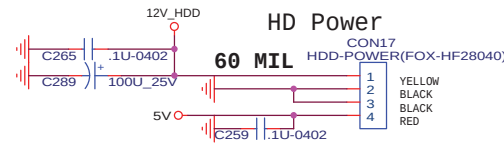
PS0T05LC

PROJECT : DT1
Quanta Computer Inc.

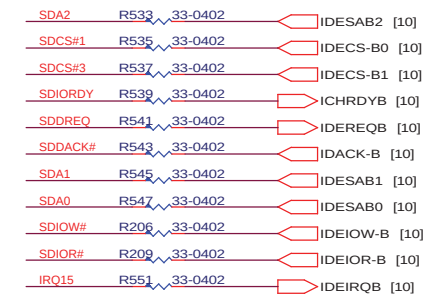
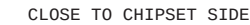
Size	Document Number	Rev
Custom	PCI CONN & PULL UP	E
Date:	Friday, April 04, 2003	Sheet 20 of 35

HDD POWER CONNECTOR

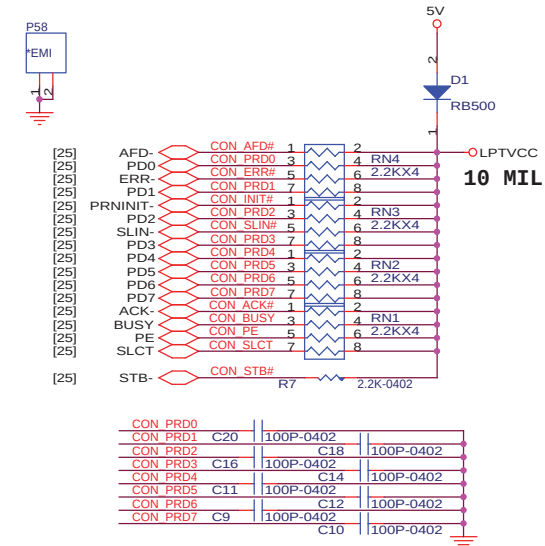
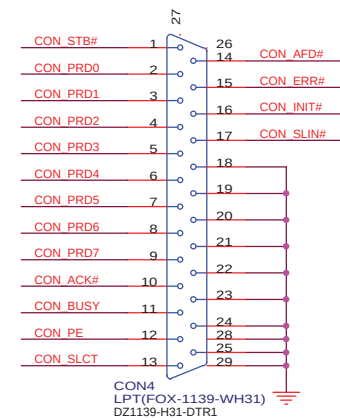
HD Power



CLOSE TO CHIPSET SIDE



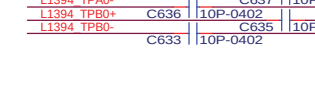
LPT CONN.

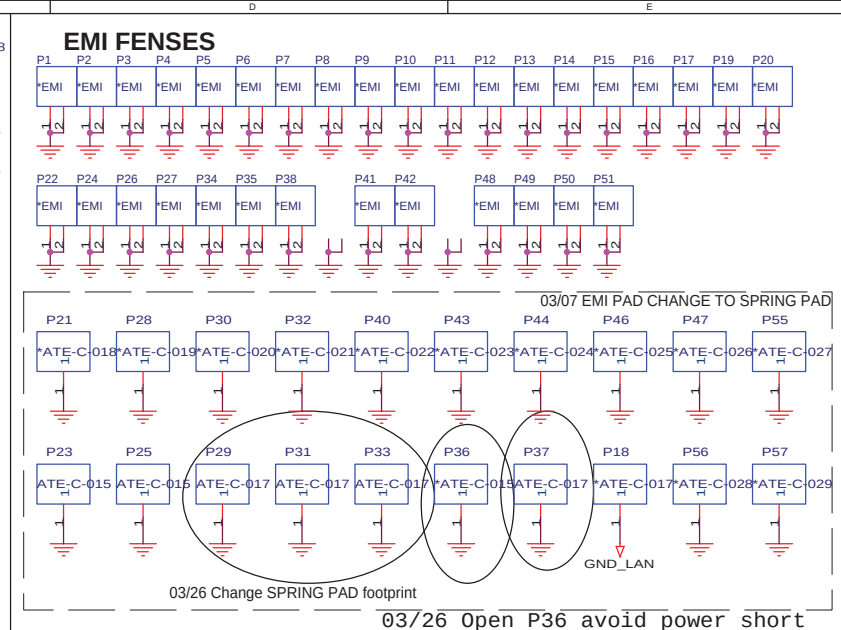
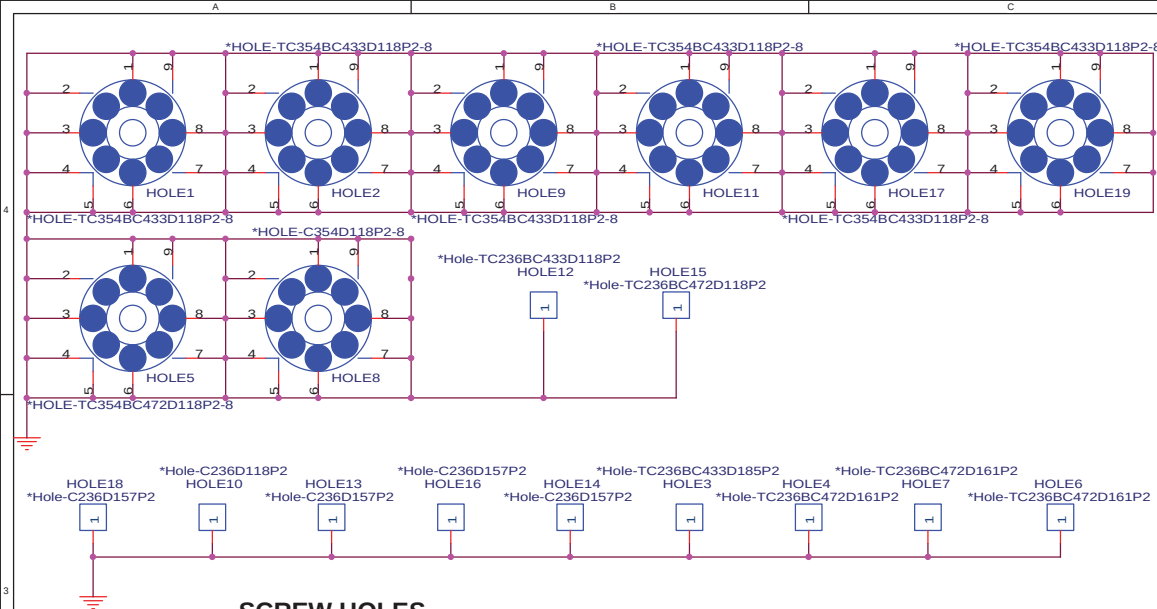


CON STB#			
CON ACK#	C21	100P-0402	
CON BUSY		C7	100P-0402
CON PE	C8	100P-0402	
CON SLCT		C5	100P-0402
CON AFD#	C6	100P-0402	
CON ERR#		C19	100P-0402
CON INIT#	C17	100P-0402	
CON SLIN#		C15	100P-0402
	C13	100P-0402	

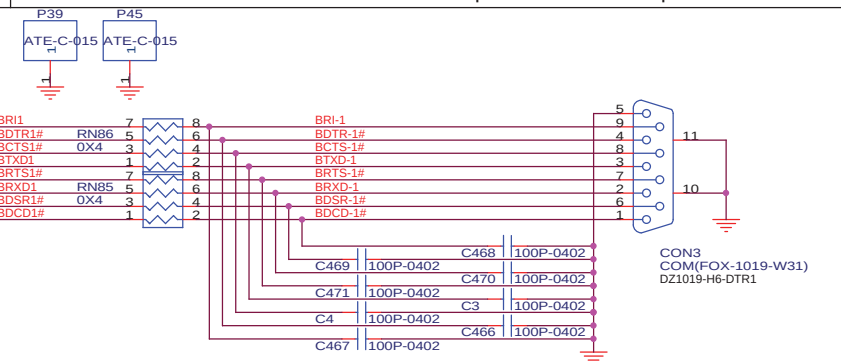
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Quanta Computer Inc.

Size Custom Document Number **IDE (HDD & CDROM) & LPT**
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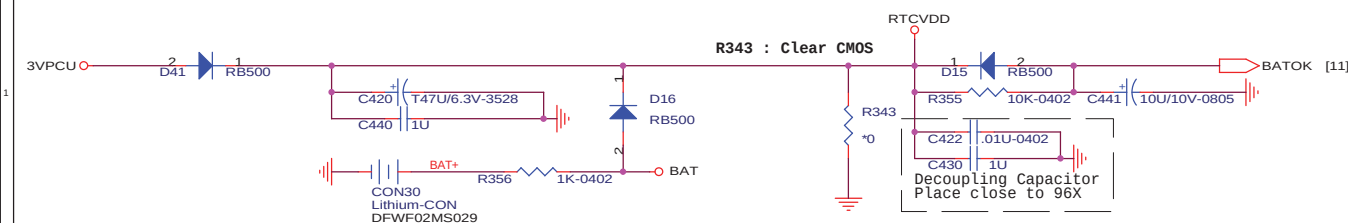
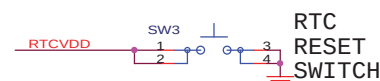
Serial Port

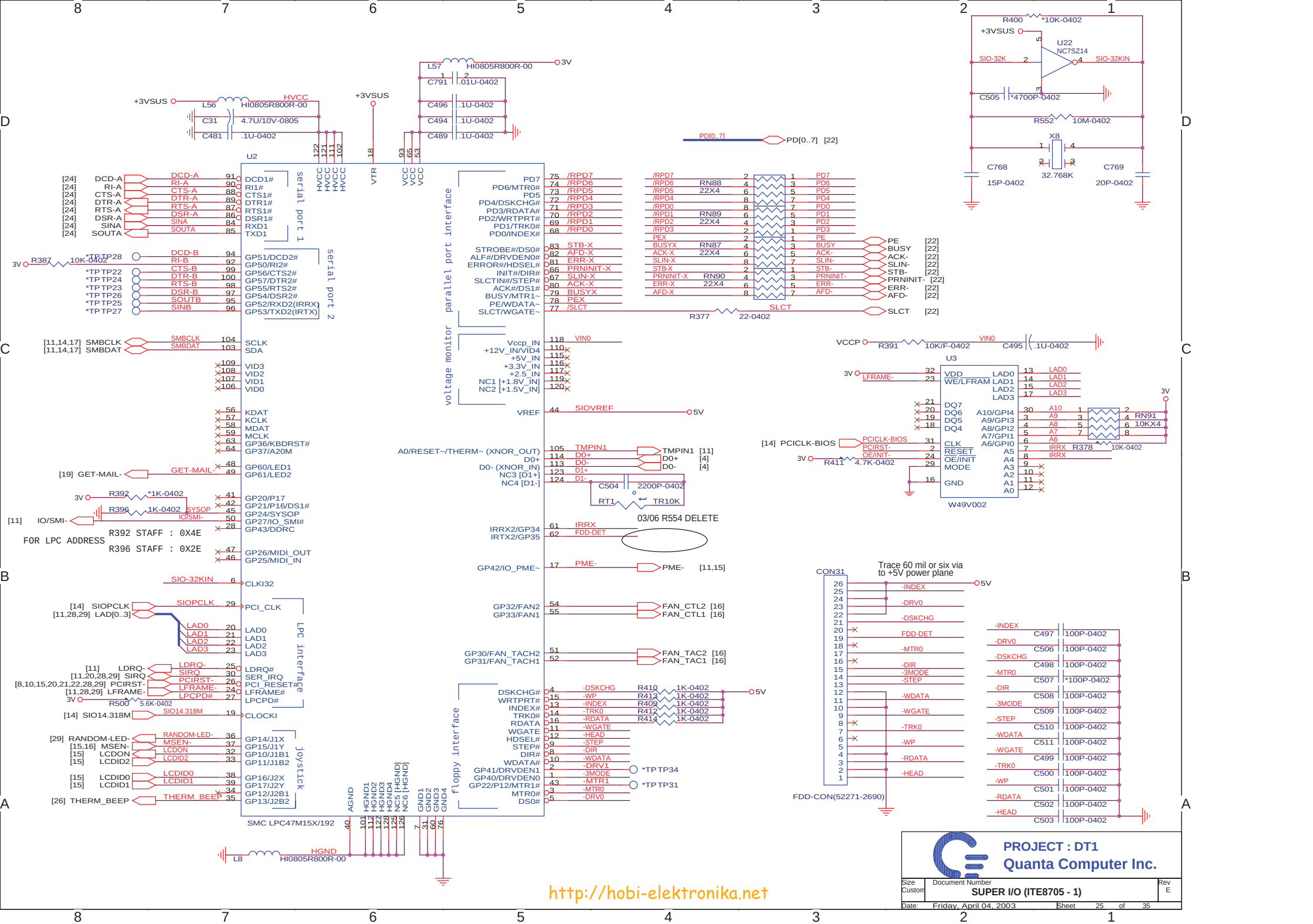


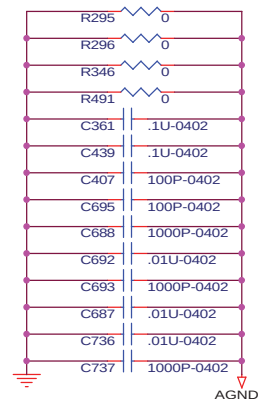
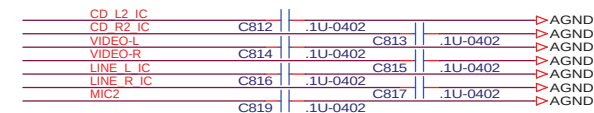
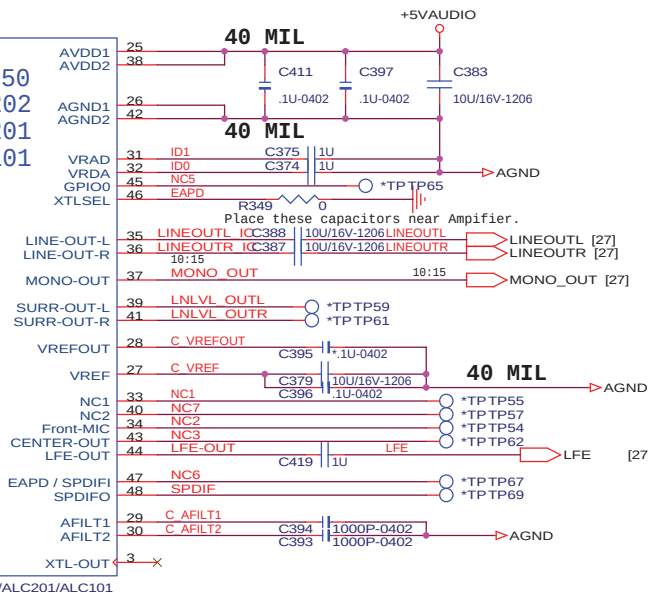
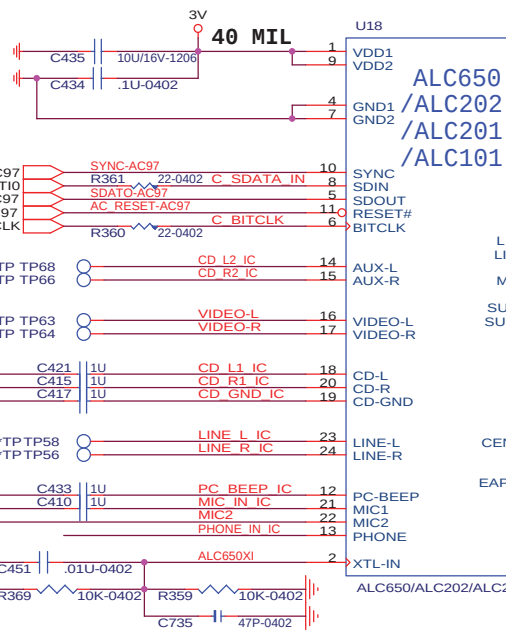
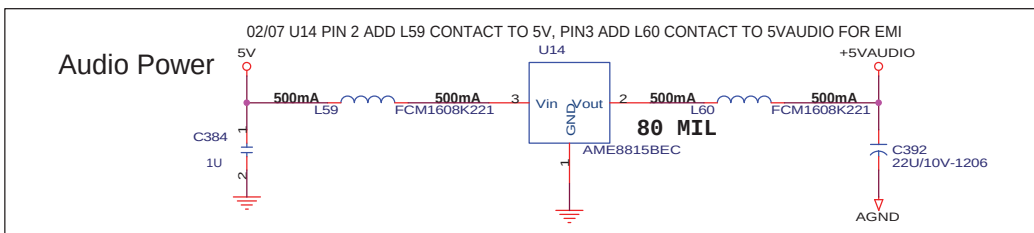
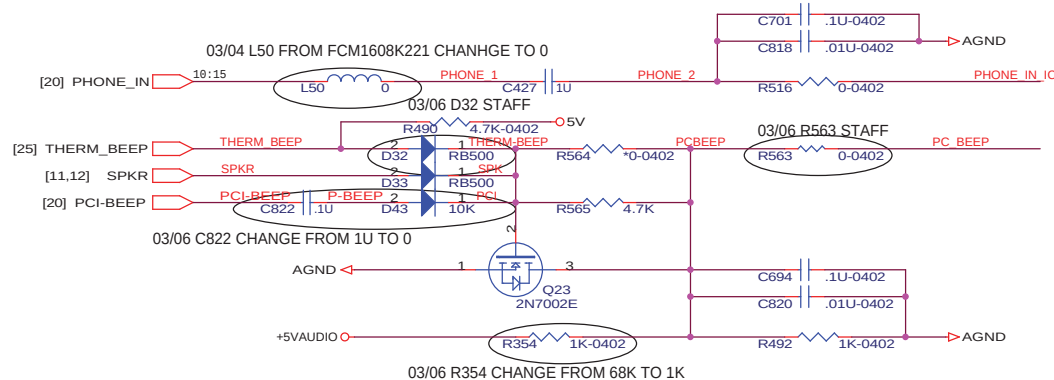
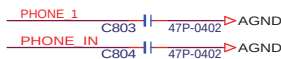
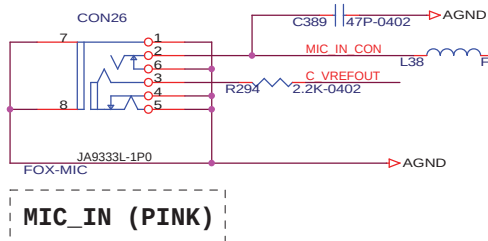
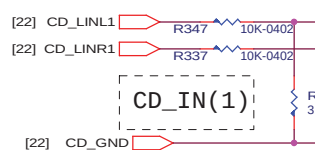
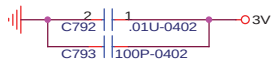
RTC

NOTE!

- 1.The RTCVDD is 3V
- 2.Decoupling capacitor must be close to 650 RTCVDD pin.
- 3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.

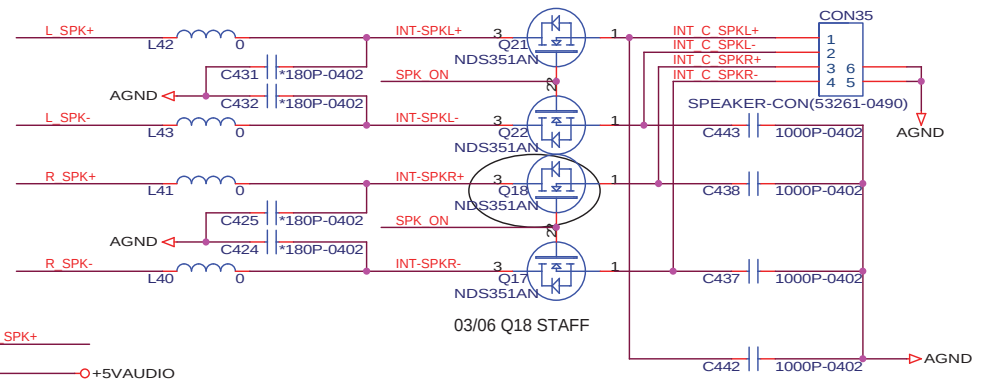
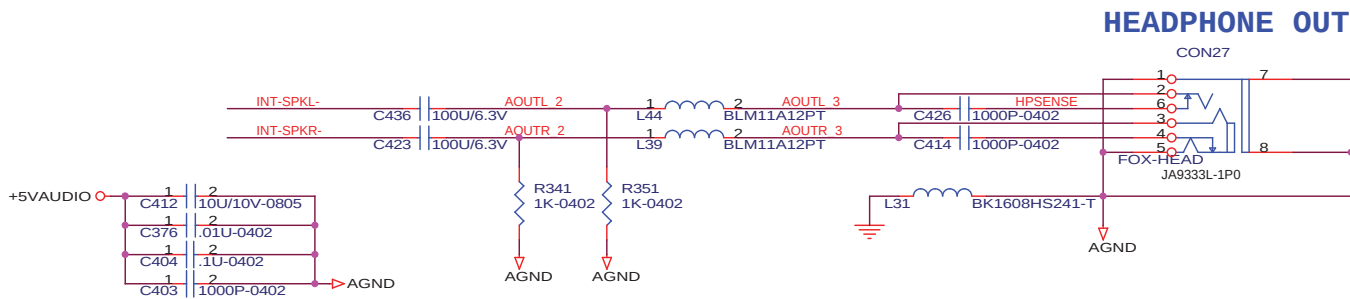
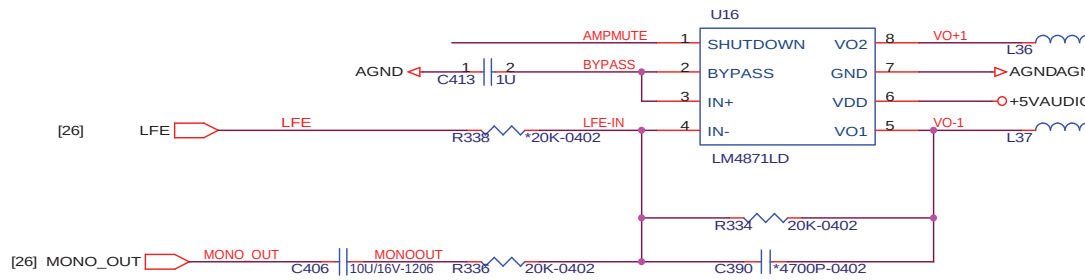
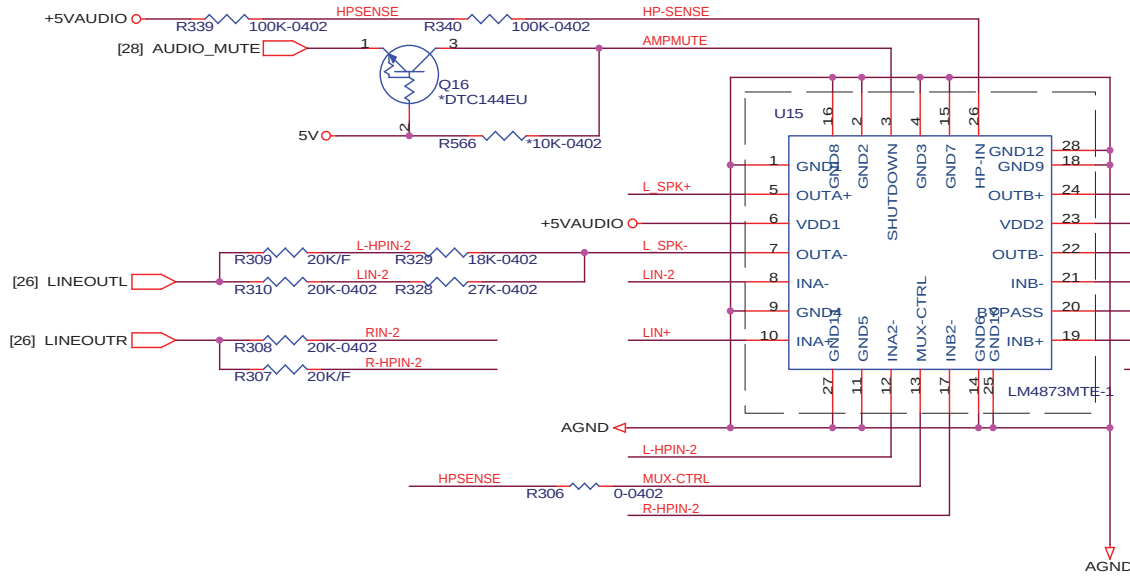




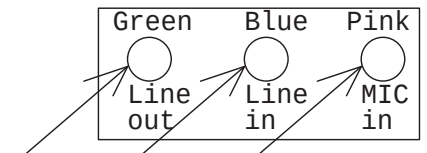
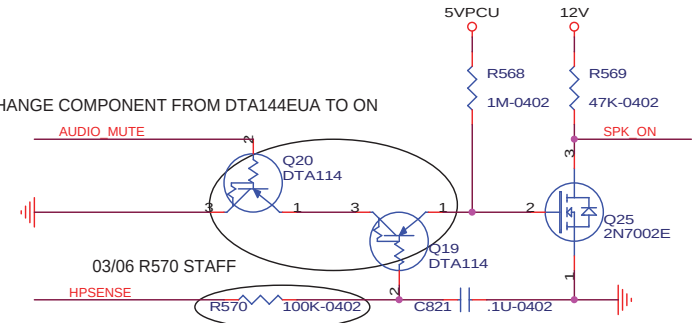


Audio amplifier

03/06 U15 CHANGE COMPONENT FROM LM4873LQ TO LM4873MTE-1

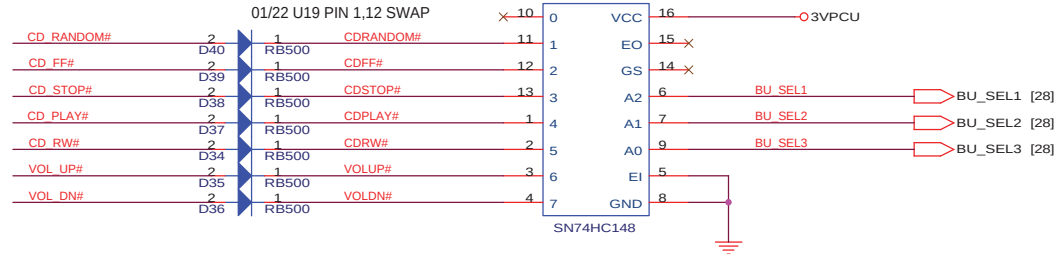
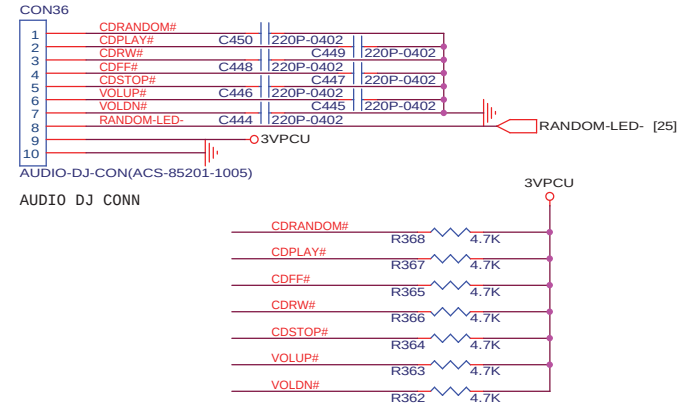
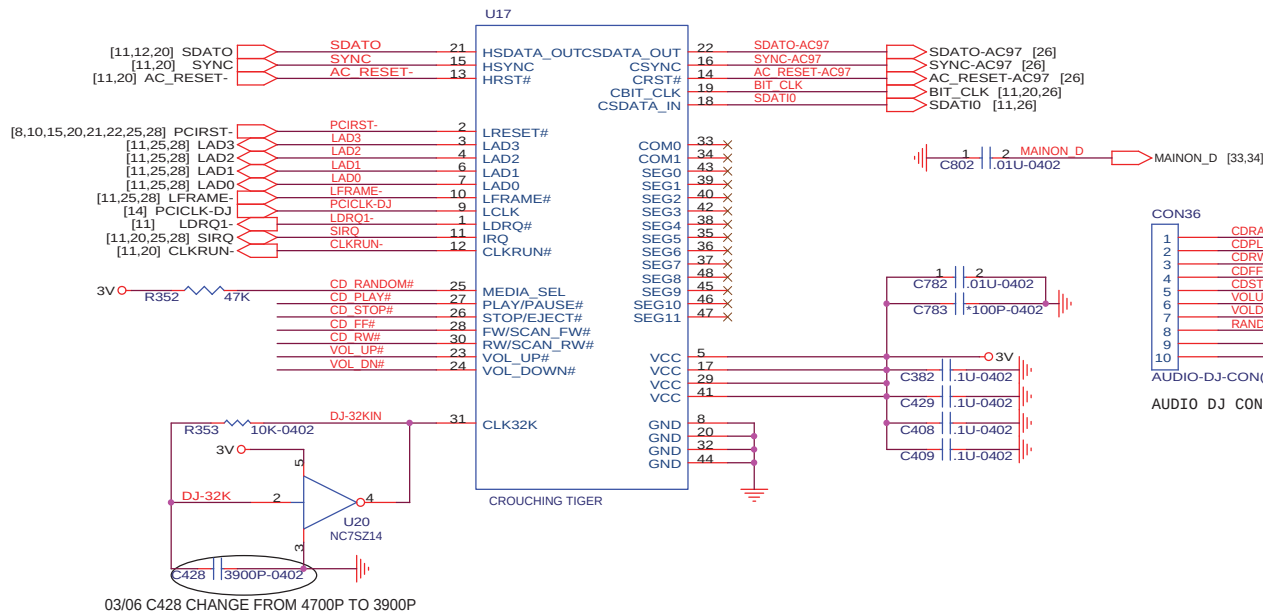


03/06 Q19, Q20 CHANGE COMPONENT FROM DTA144EUA TO ON

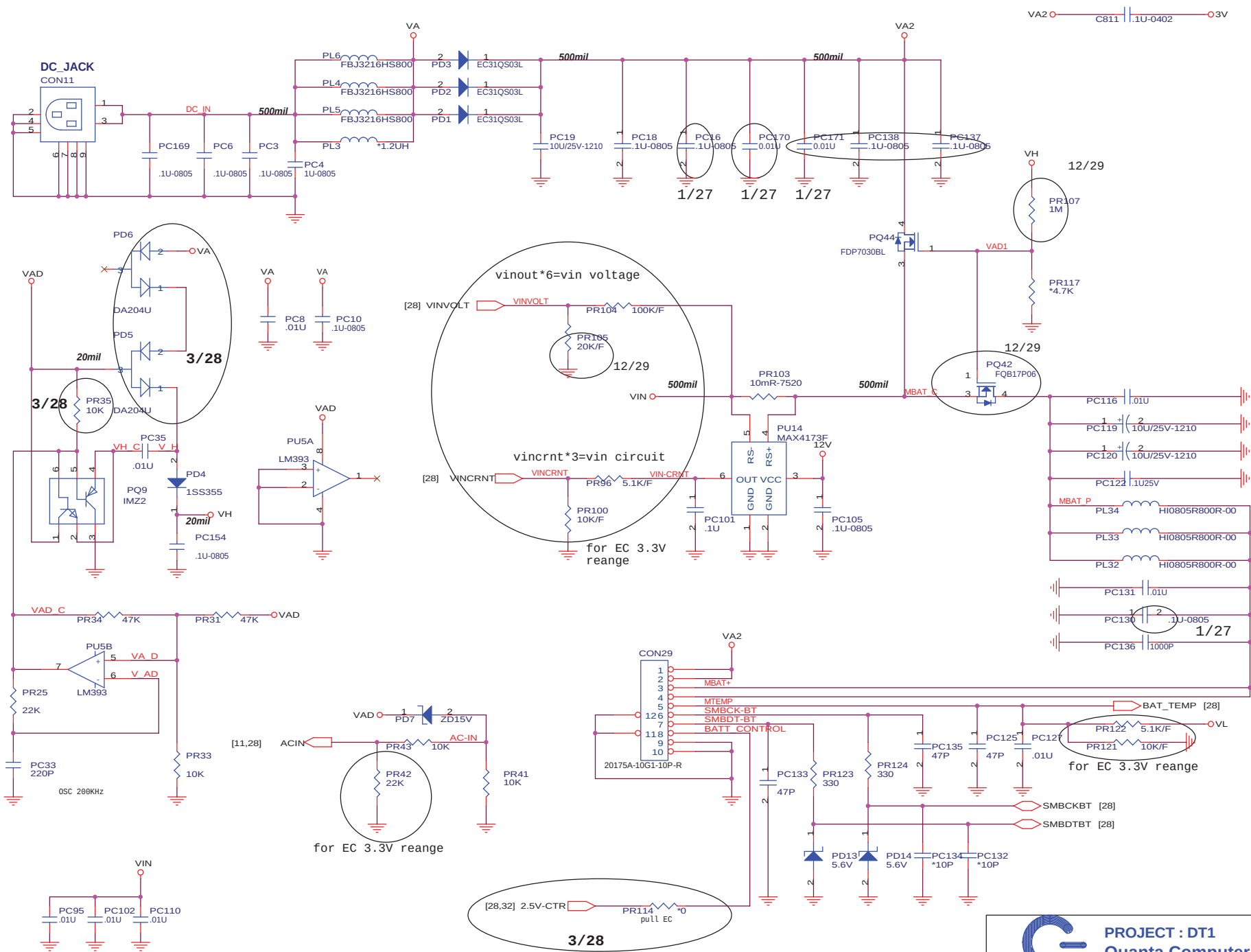


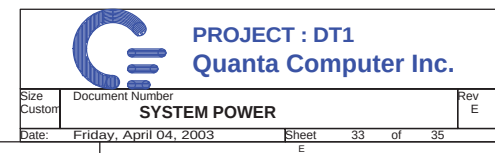
PROJECT : DT1
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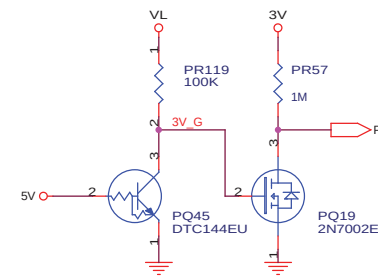
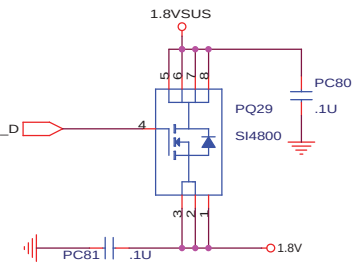
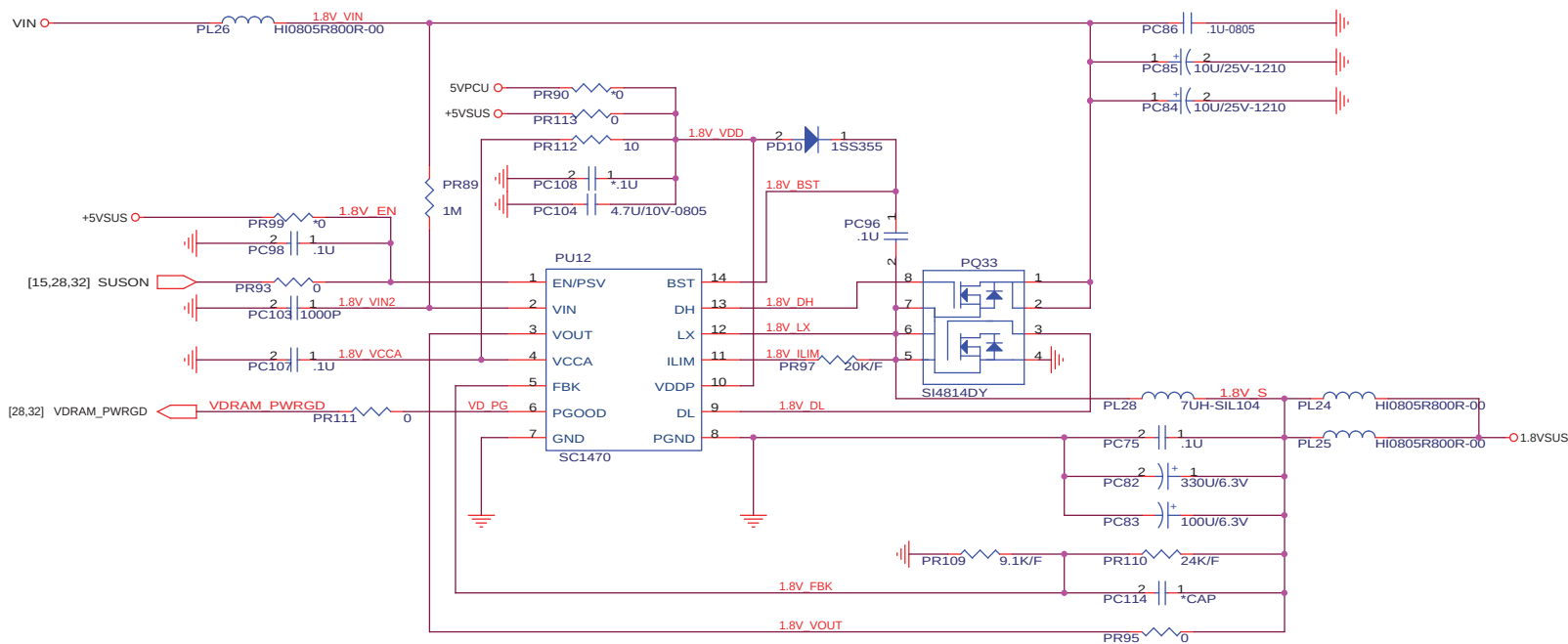
Size Custom	Document Number AUDIO AMPLIFIER(LM4873 & 4871)	Rev E
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SN74HC148 TABLE													
INPUTS								OUTPUTS					
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H







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H1P6301 FOR INTEL Brookdale POWER CKT-DDR

