Compal Confidential

NBLG0 Schematics Document

AMD Tigris (JV40-TR) : Caspian Processor with RS880M/SB710/M92-M2 XT

2009-06-04

REV:0.2

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Title: Cover Page

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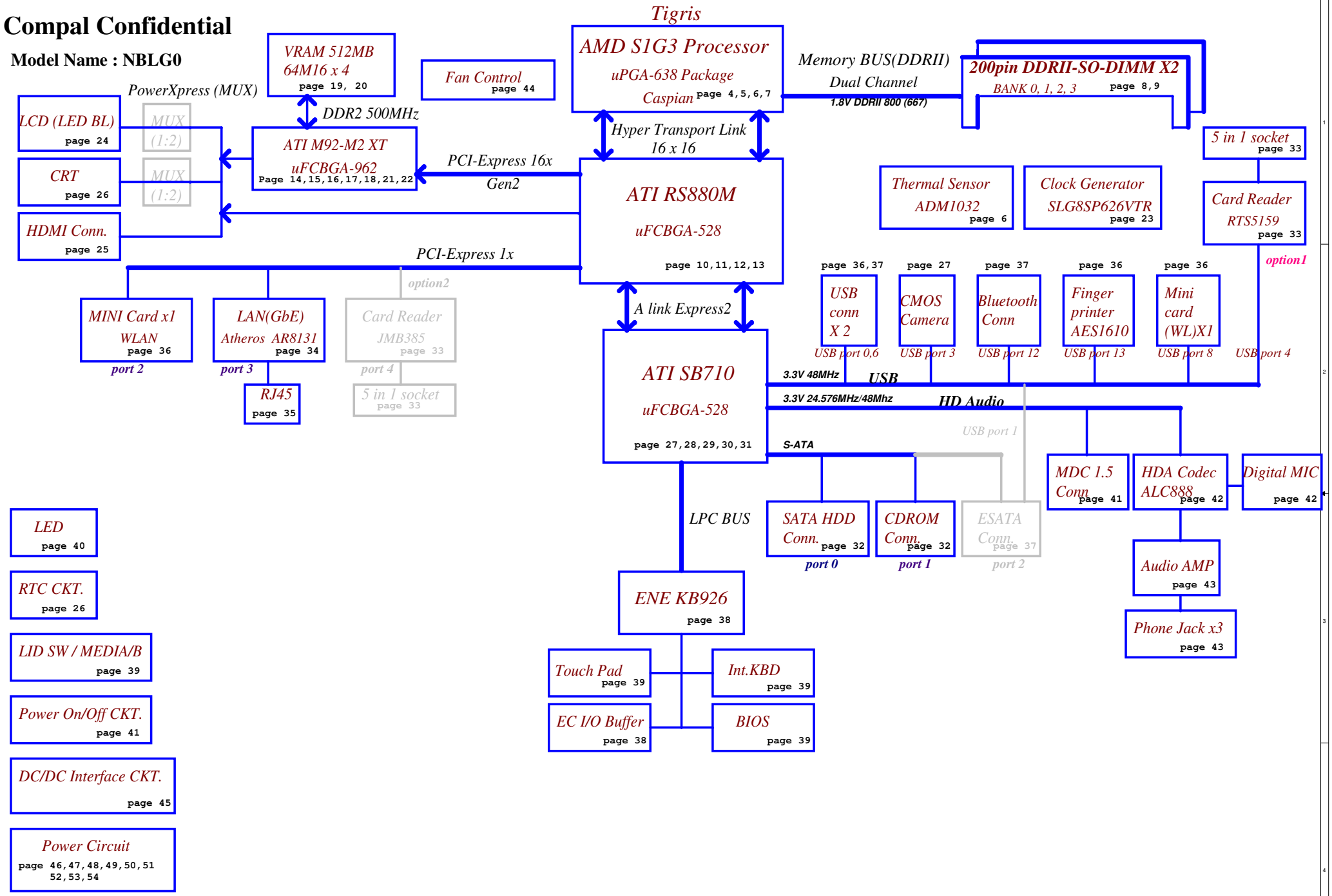
Model Name : NBLG0



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
GMT G781-1 (GPU)	1001 101X b	9AH
SB-Temp Sensor		9CH

SB700 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB700 SM Bus 1 address

Device	Address
New card	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.1(DVT)
2	0.2(PVT)
3	1.0(MP)
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : iGPU(DC) / H : dGPU(AC)	LVDS / CRT

	KB926					
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

	KB926
	PX_GPIO1_SB
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)
IGP only mode	X
PowerXpress mode	H : Enable

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			Size B / Document Number KBLG0 LA-4921P / Rev 0.1
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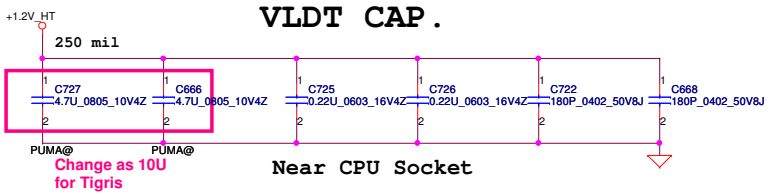

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Compal Electronics, Inc.

Title: AMD CPU S1G3 HT I/F

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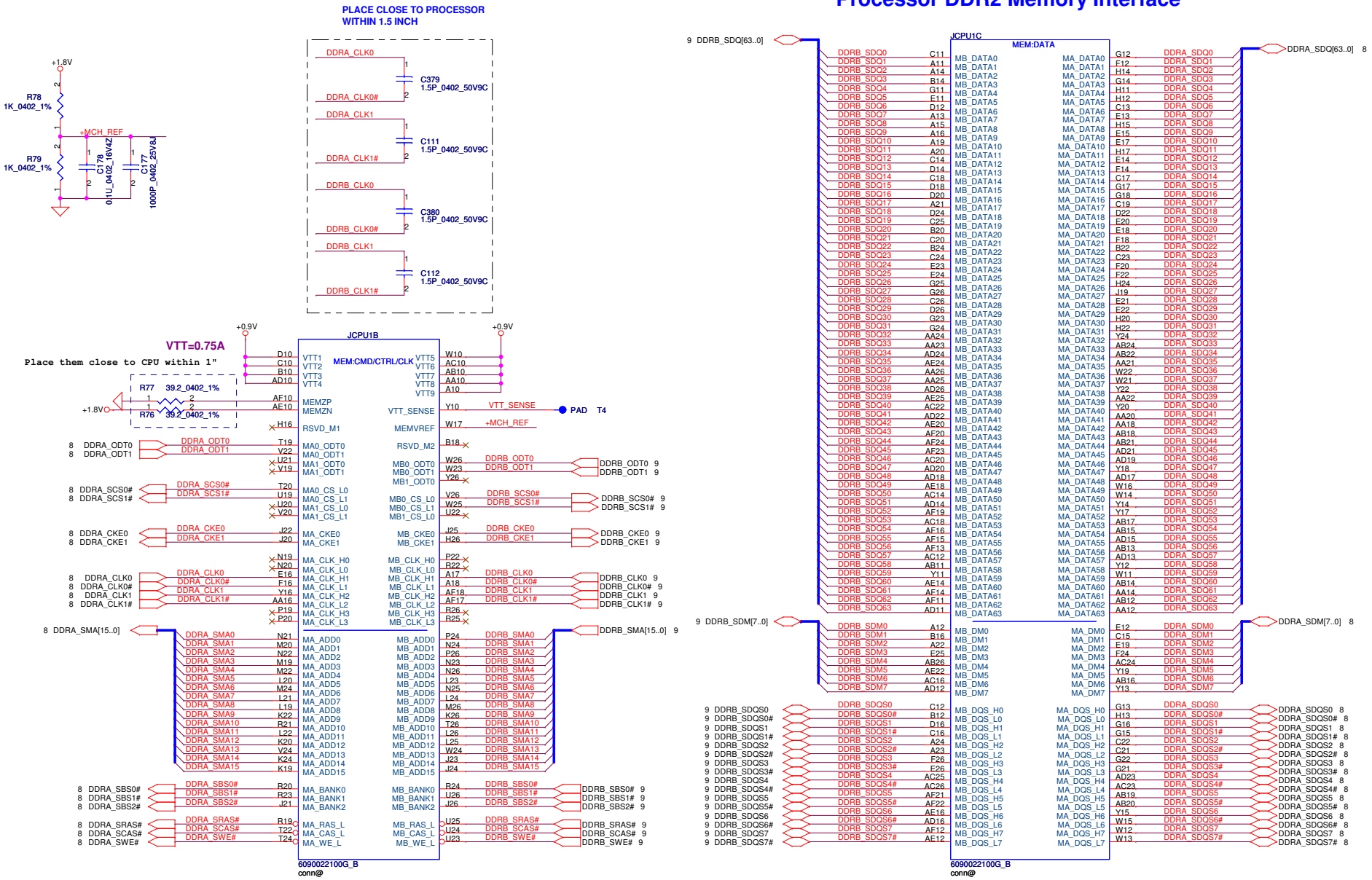
Processor DDR2 Memory Interface



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Title: AMD CPU S1G3 DDRII I/F

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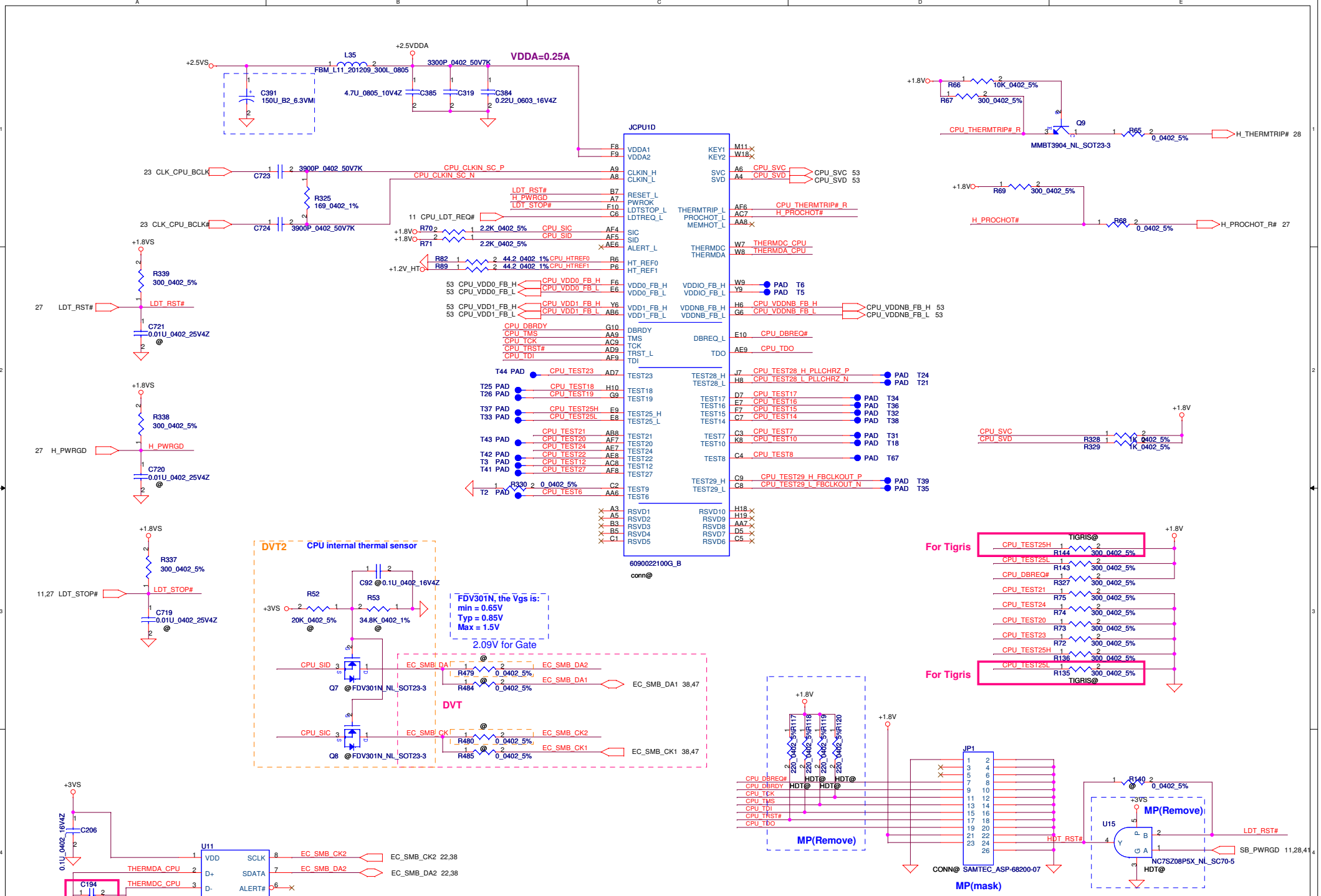

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Title: AMD CPU S1G3 CTRL

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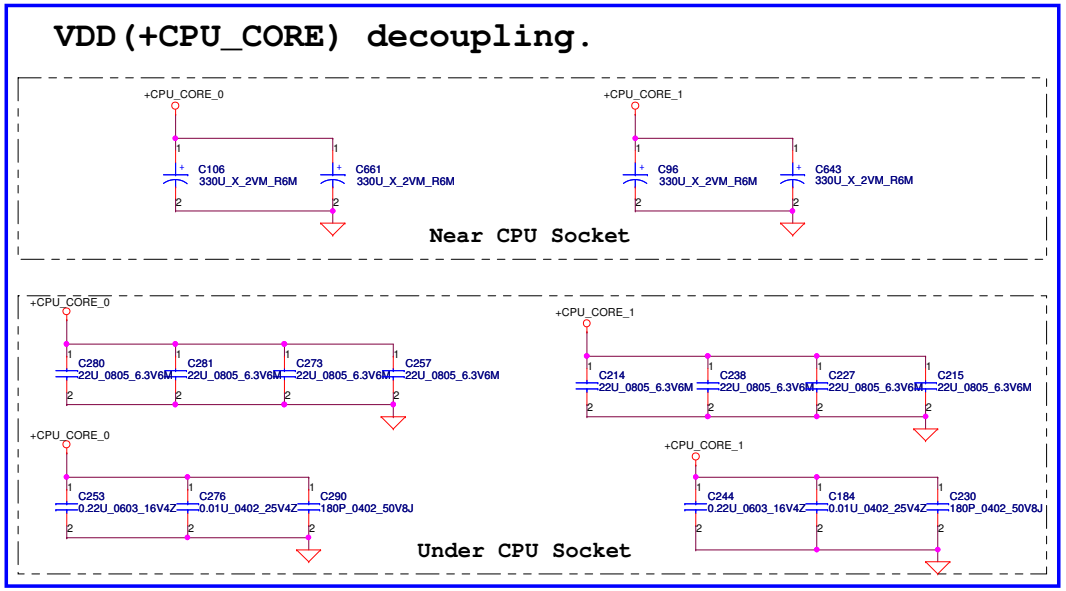

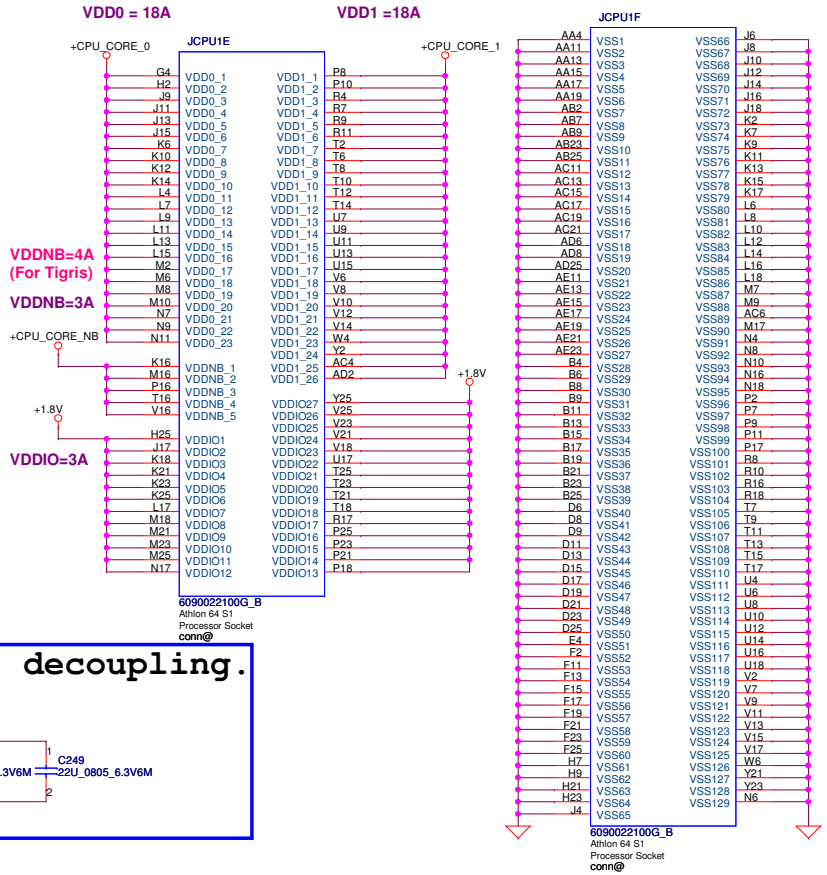

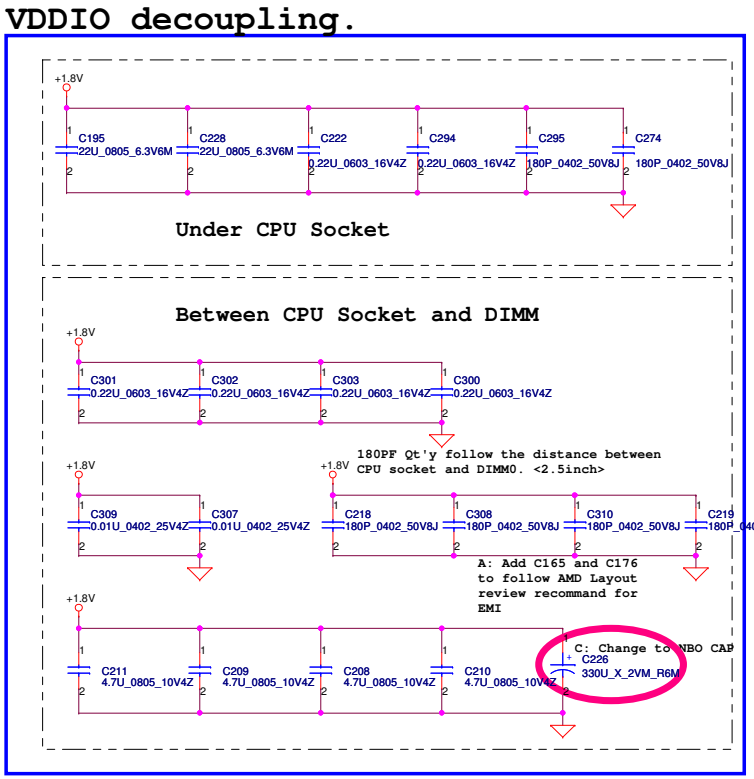

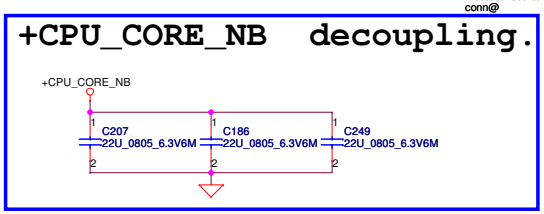

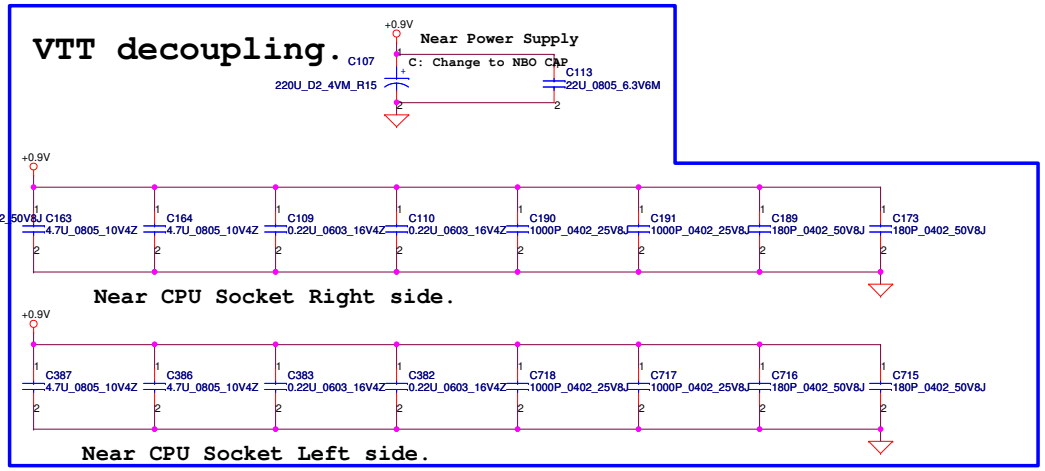

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Title: AMD CPU S1G3 PWR & GND

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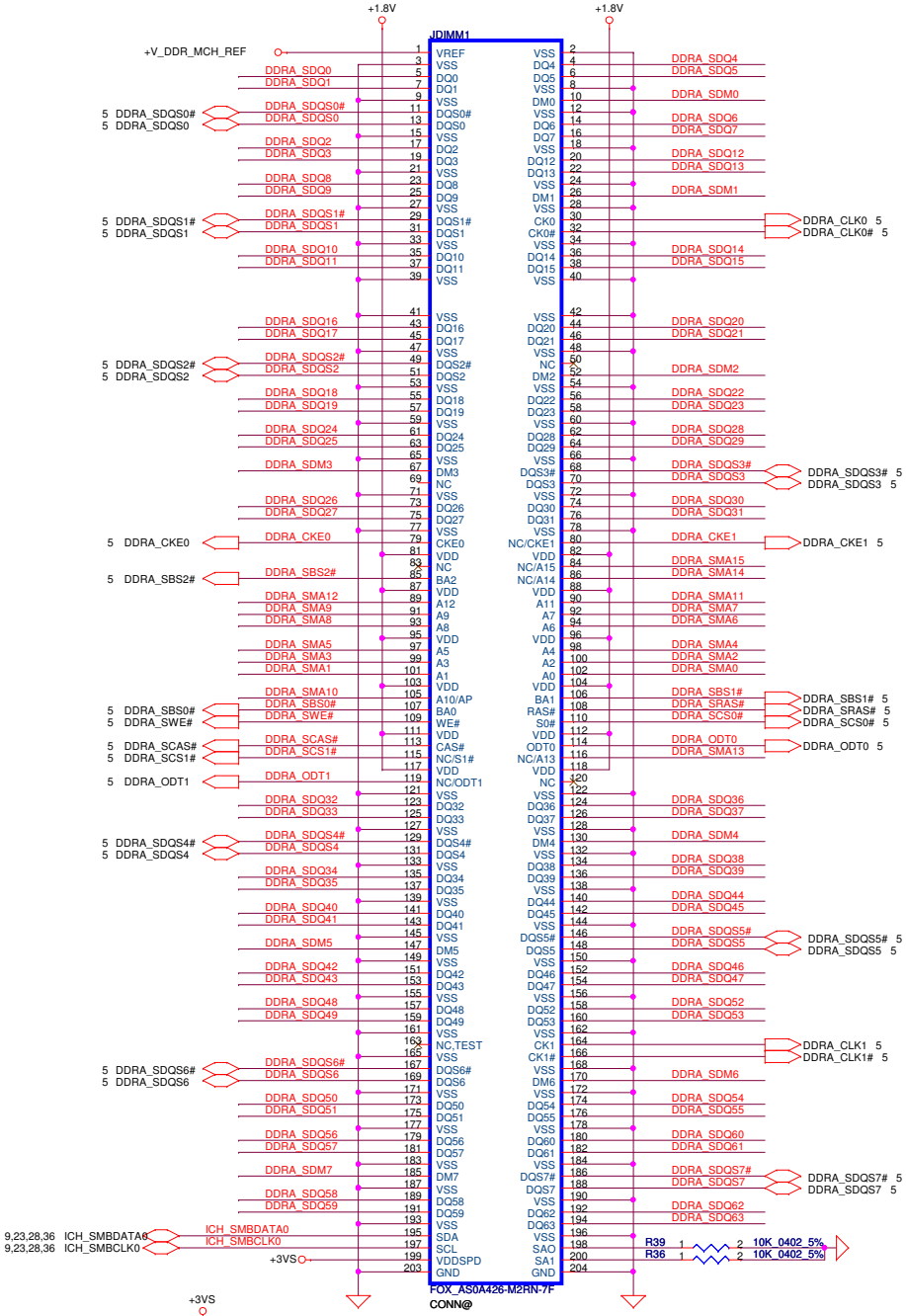

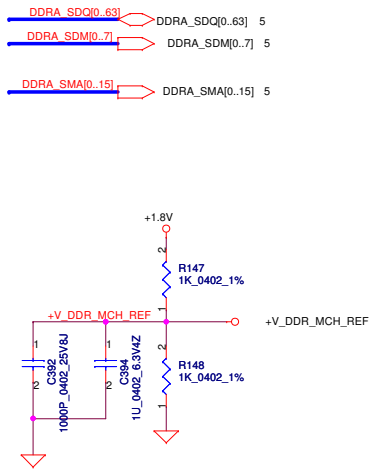

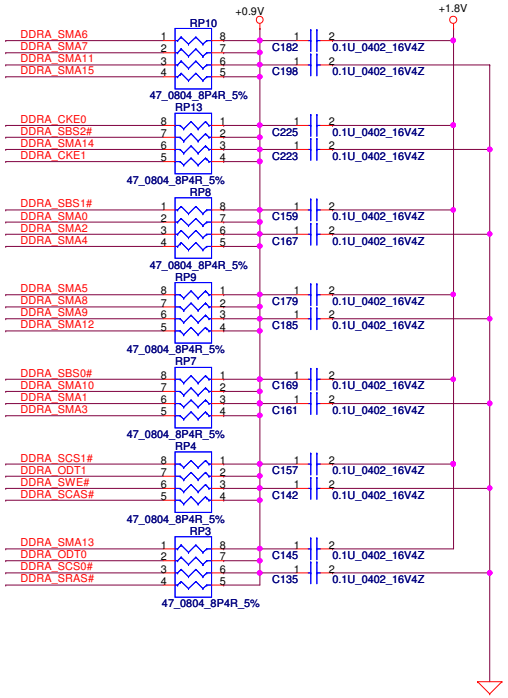

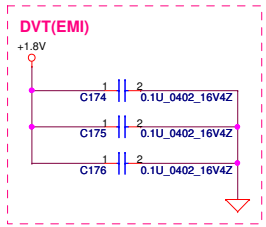

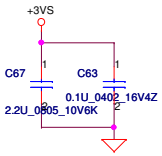

DIMM1 REV H:5.2mm (BOT)

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Title: DDRII SO-DIMM 1

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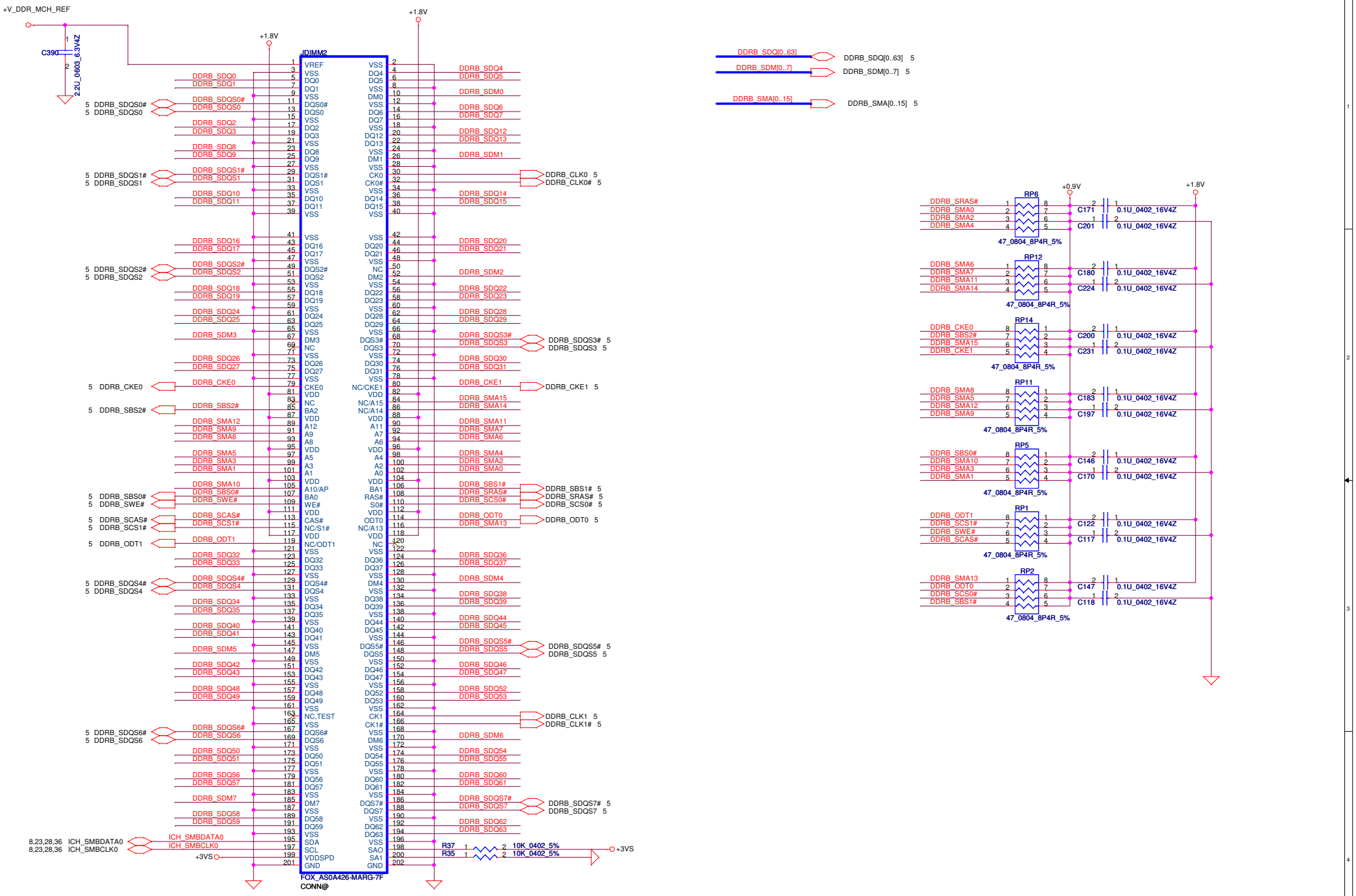

DIMM2 REV H:9.2mm (BOT)

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Title: DDRII SO-DIMM 2

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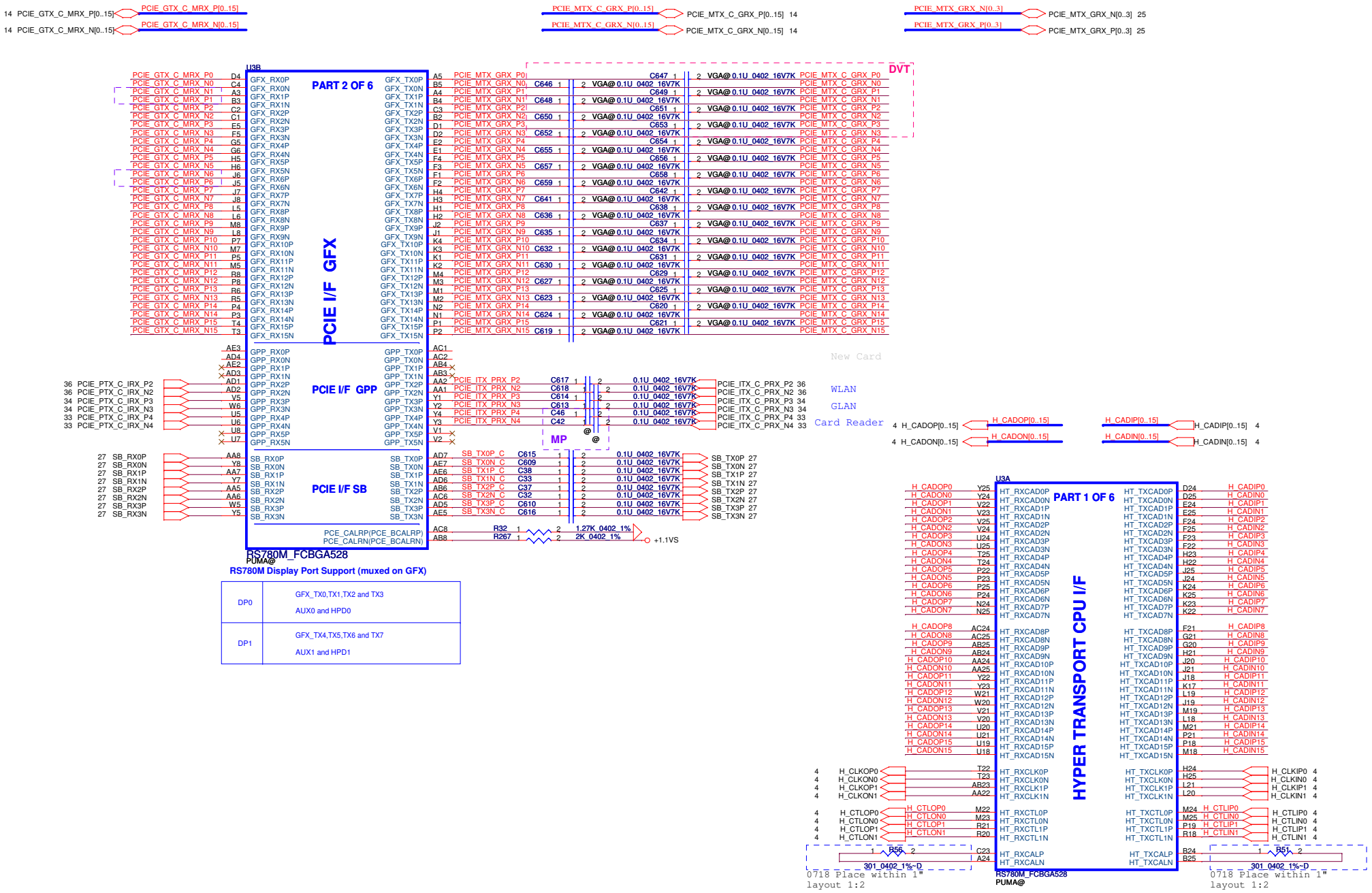

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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Title: RS880-HT/PCIE

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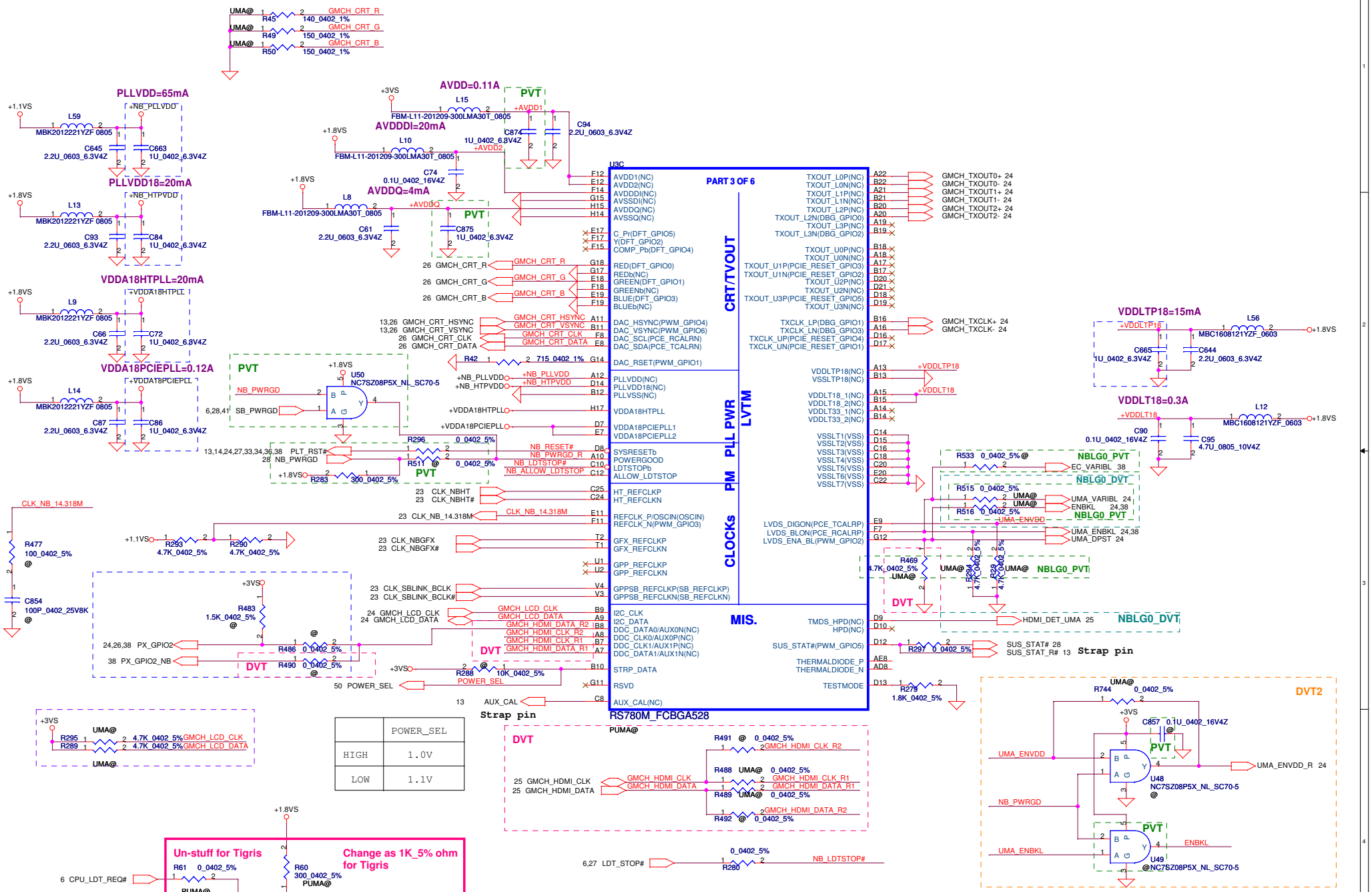
For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor



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Title: RS880 VEDIO/CLK GEN

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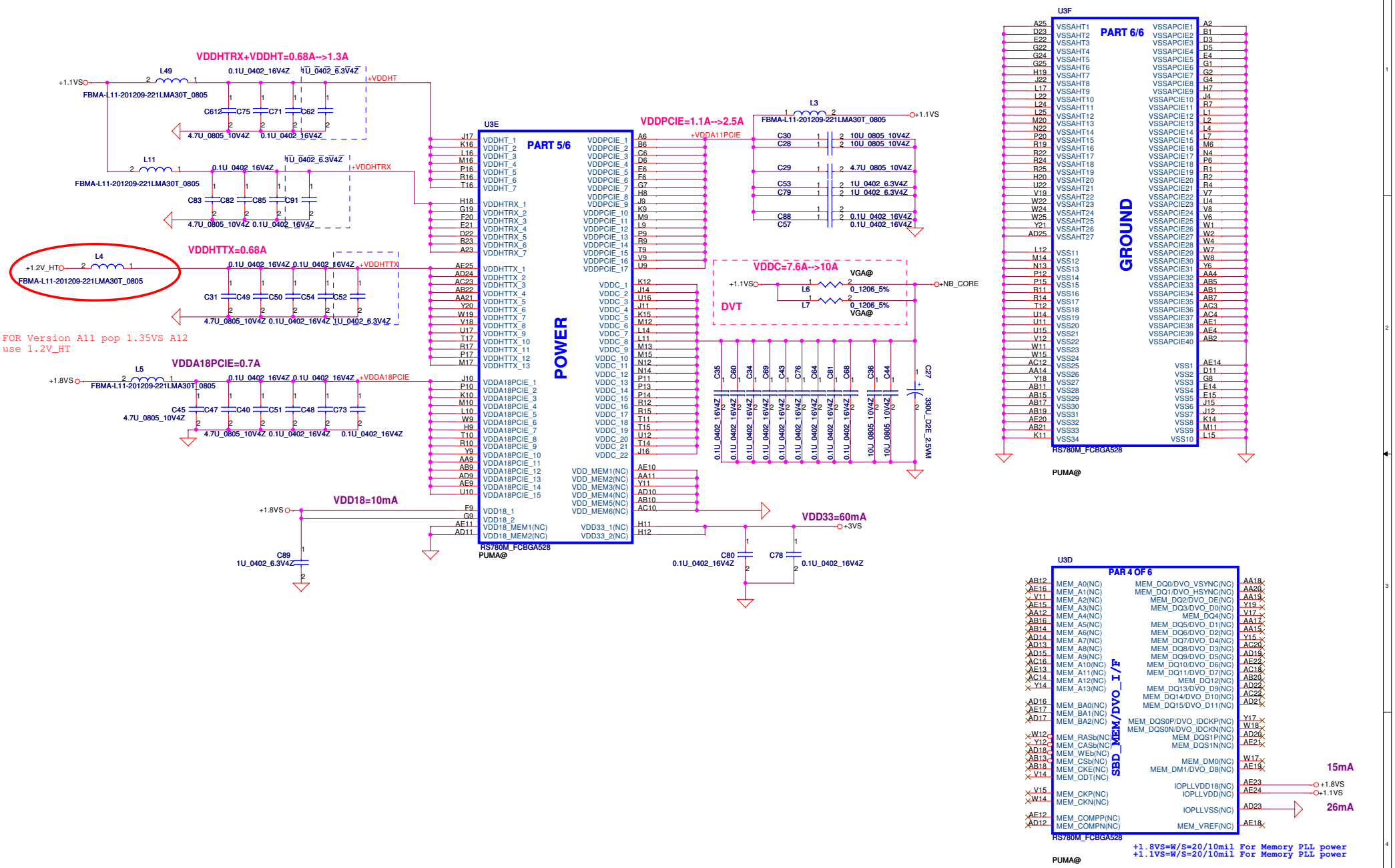

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Title: RS880 PWR/GND

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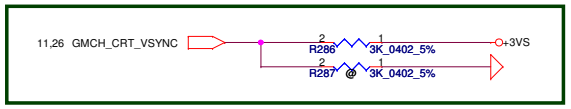
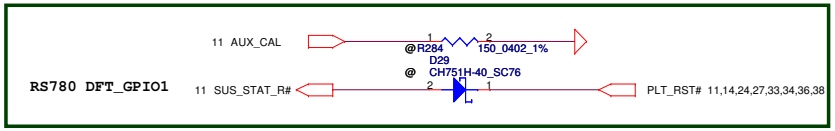


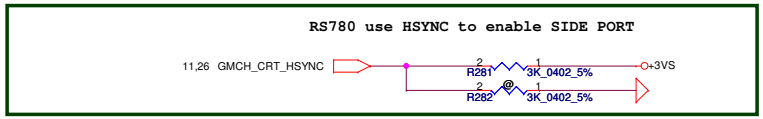
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```



RS780 use HSYNC to enable SIDE PORT

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.   Enable (RS780)
1 :  Disable(RS780)
```

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Title: RS880 STRAPS

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

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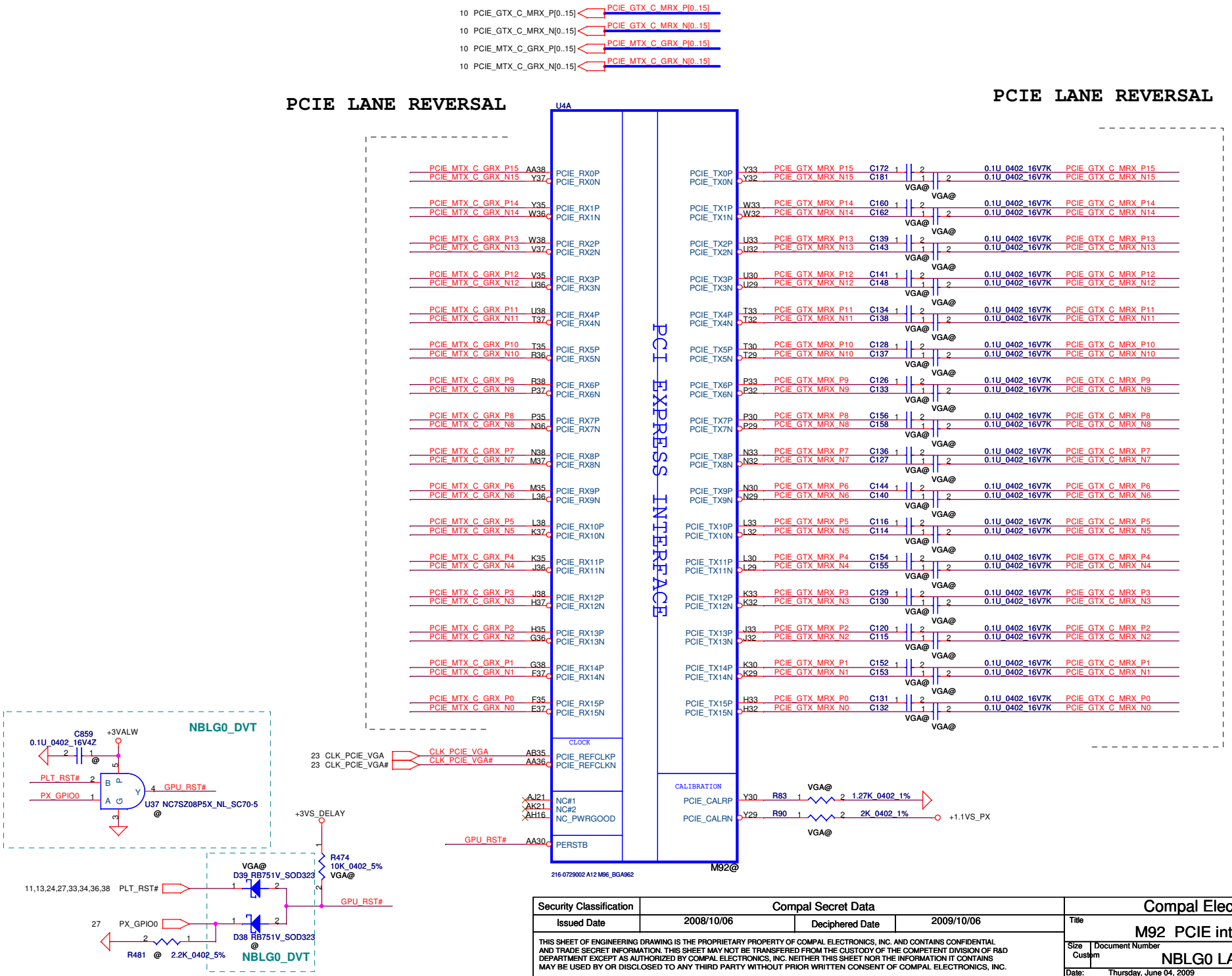

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Compal Electronics, Inc.

Title: M92 PCIE interface

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

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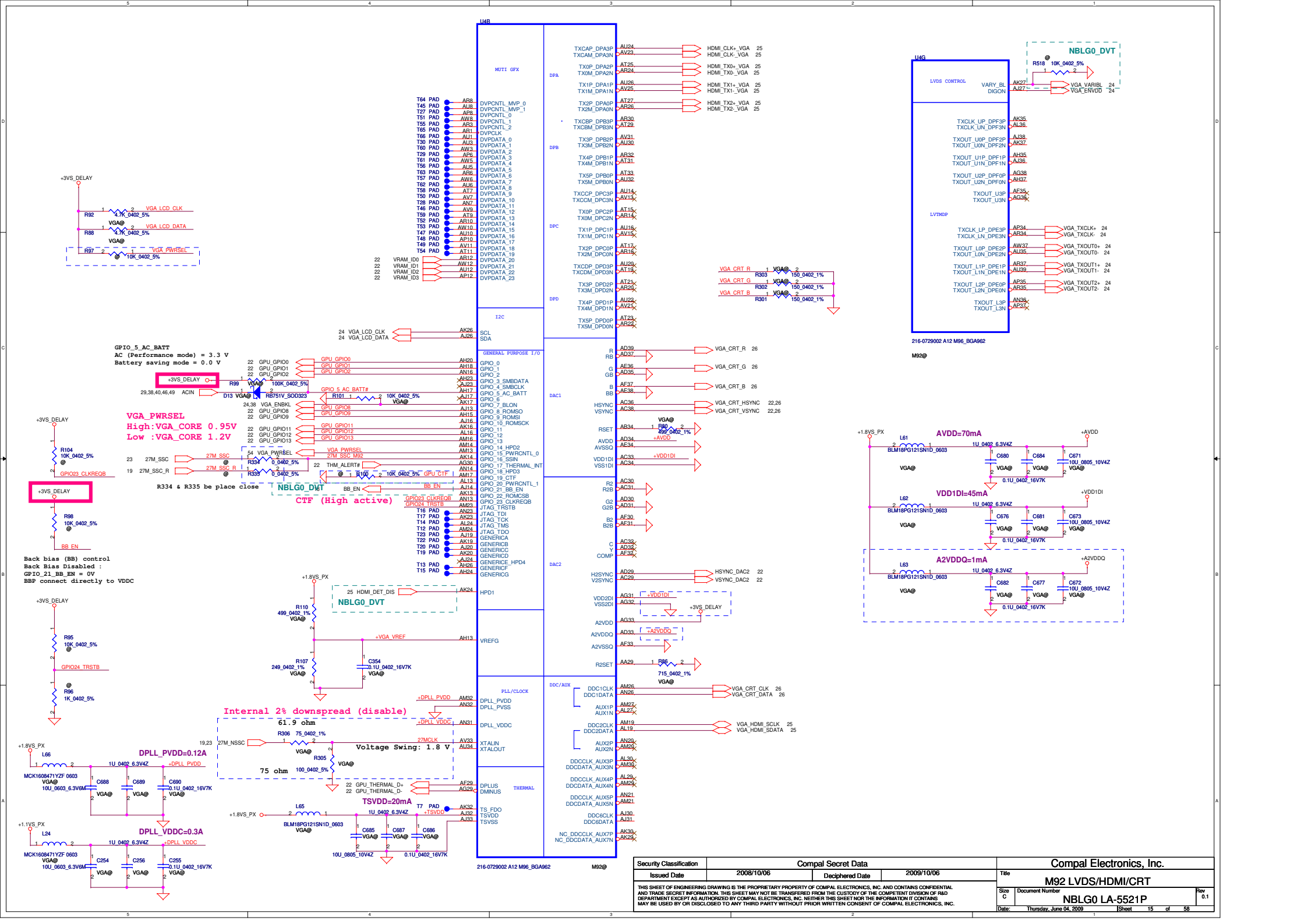

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Compal Electronics, Inc.

Title: M92 LVDS/HDMI/CRT

Size	Document Number	Rev
C	NBLG0 LA-5521P	0.1

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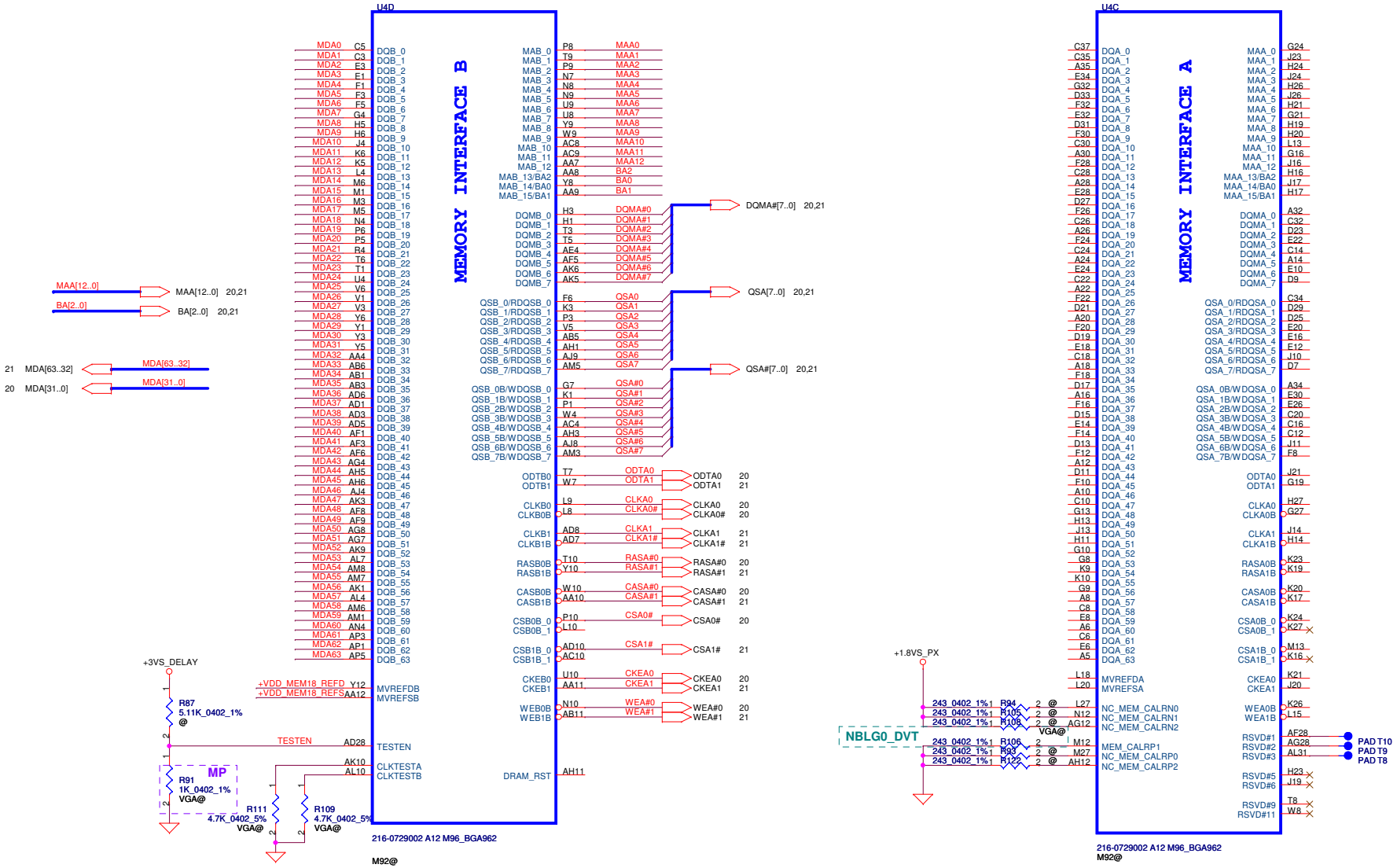
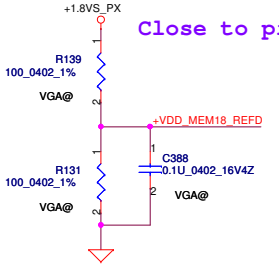
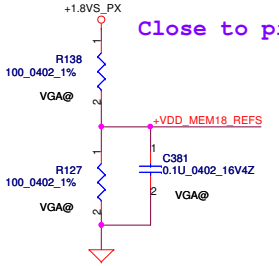


Close to pin Y12



Close to pin AA12



M92-S2 and M92-M use memory group A only
while M92-M2 uses memory group B only.

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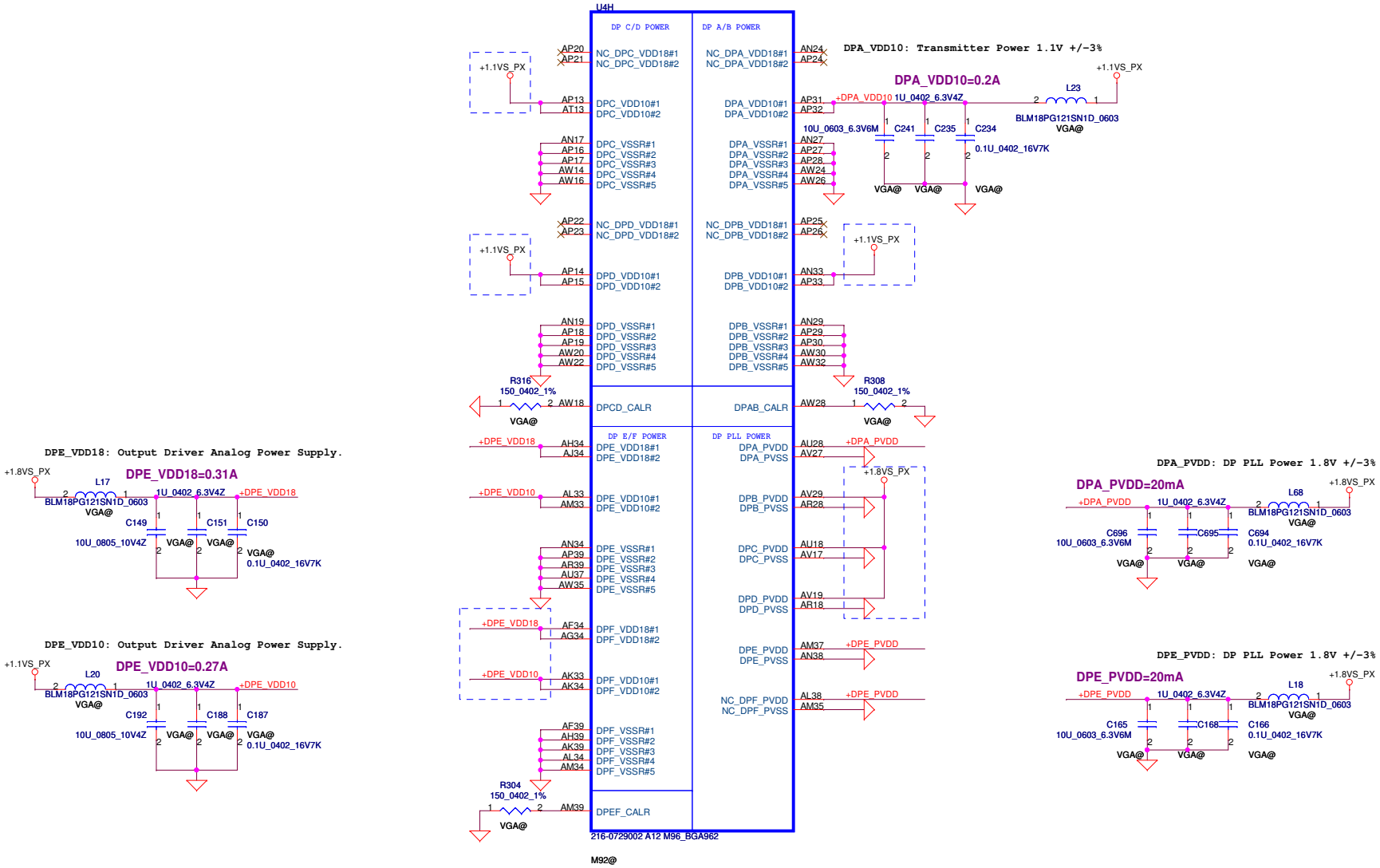
Compal Electronics, Inc.

Title: M92 MEM

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 16 of 58



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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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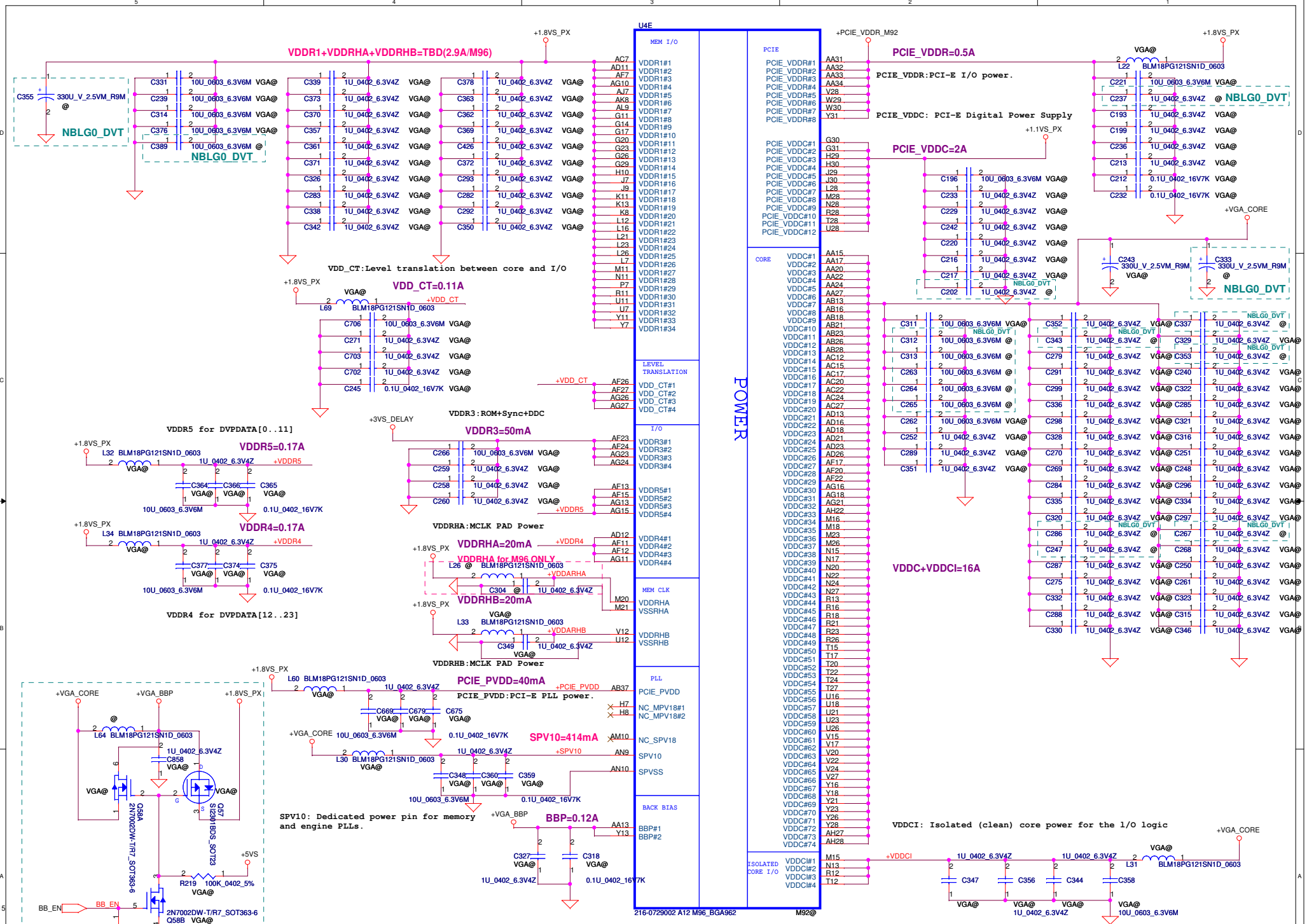
Compal Electronics, Inc.

Title: M92 DRX PWR

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Sunday, April 12, 2009 | Sheet 17 of 58



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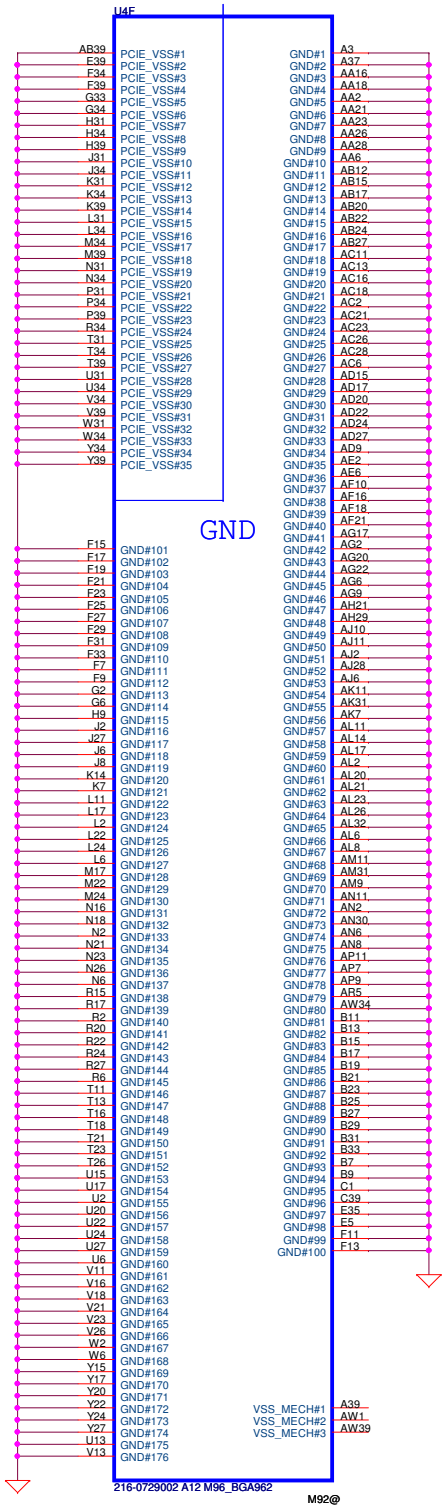
Compal Electronics, Inc.

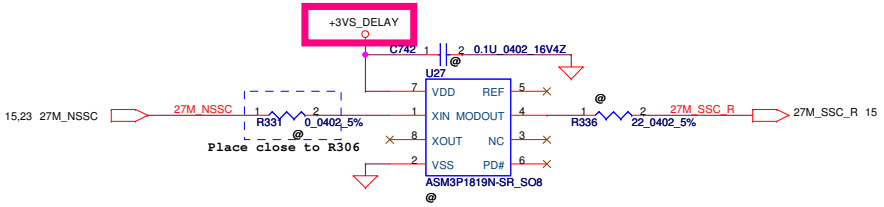
Title: M92 POWER

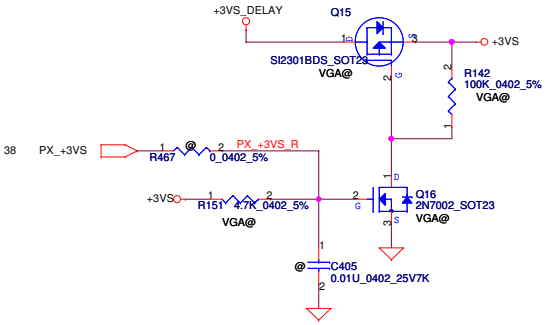
Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 18 of 58



Spread spectrum





Use Delay 3.3V BUS (VDDR3) for GPIO/DDC Pull up to reduce Leakage to VDDR3 Bus.

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Compal Electronics, Inc.

Title: M92 GND

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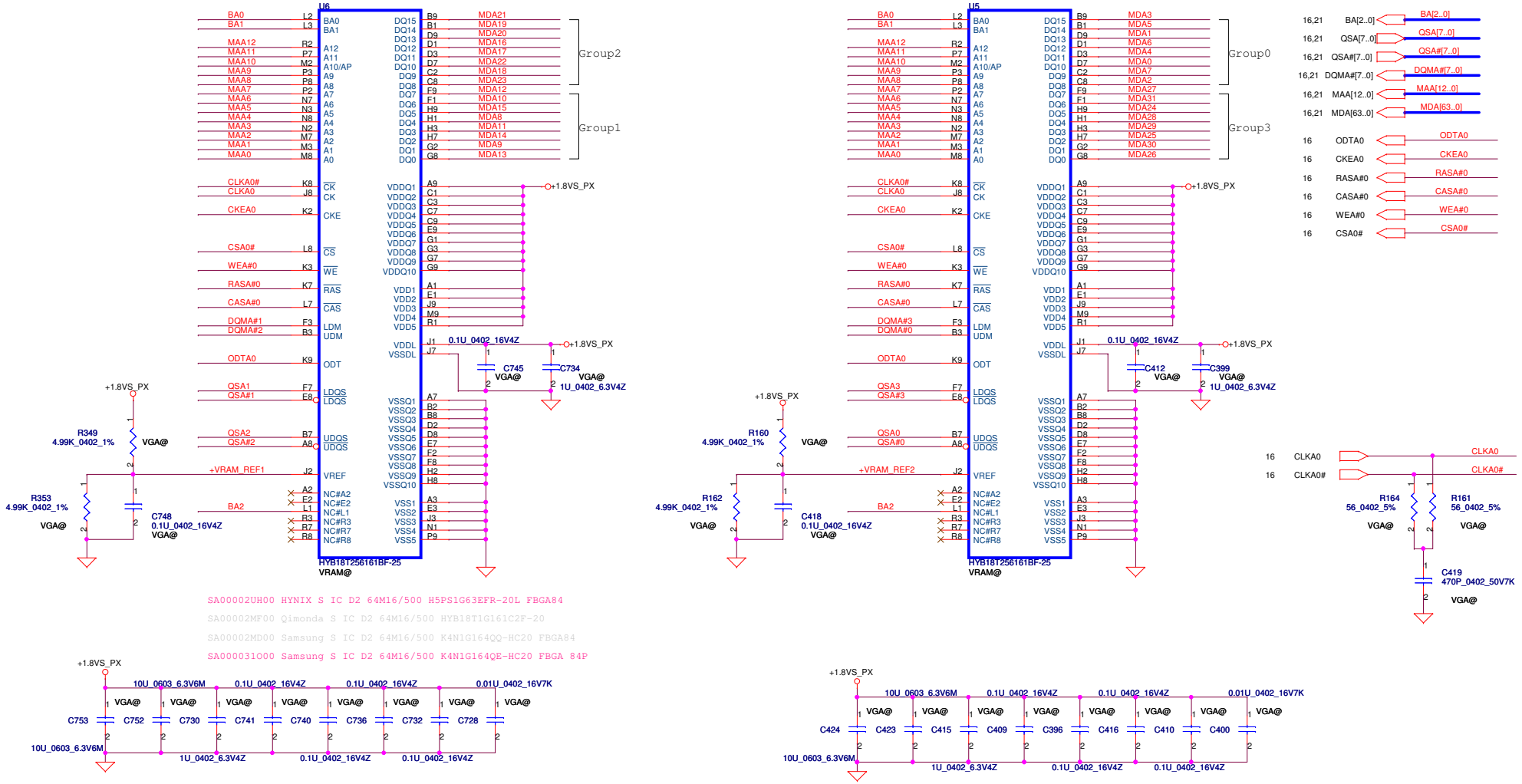

SA00002UH00 HYNIX S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

SA00002MF00 Qimonda S IC D2 64M16/500 HYB18T1G161C2F-20

SA00002MD00 Samsung S IC D2 64M16/500 K4N1G164QQ-HC20 FBGA84

SA000031O00 Samsung S IC D2 64M16/500 K4N1G164QE-HC20 FBGA 84P

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Compal Electronics, Inc.

Title: M92 VRAM

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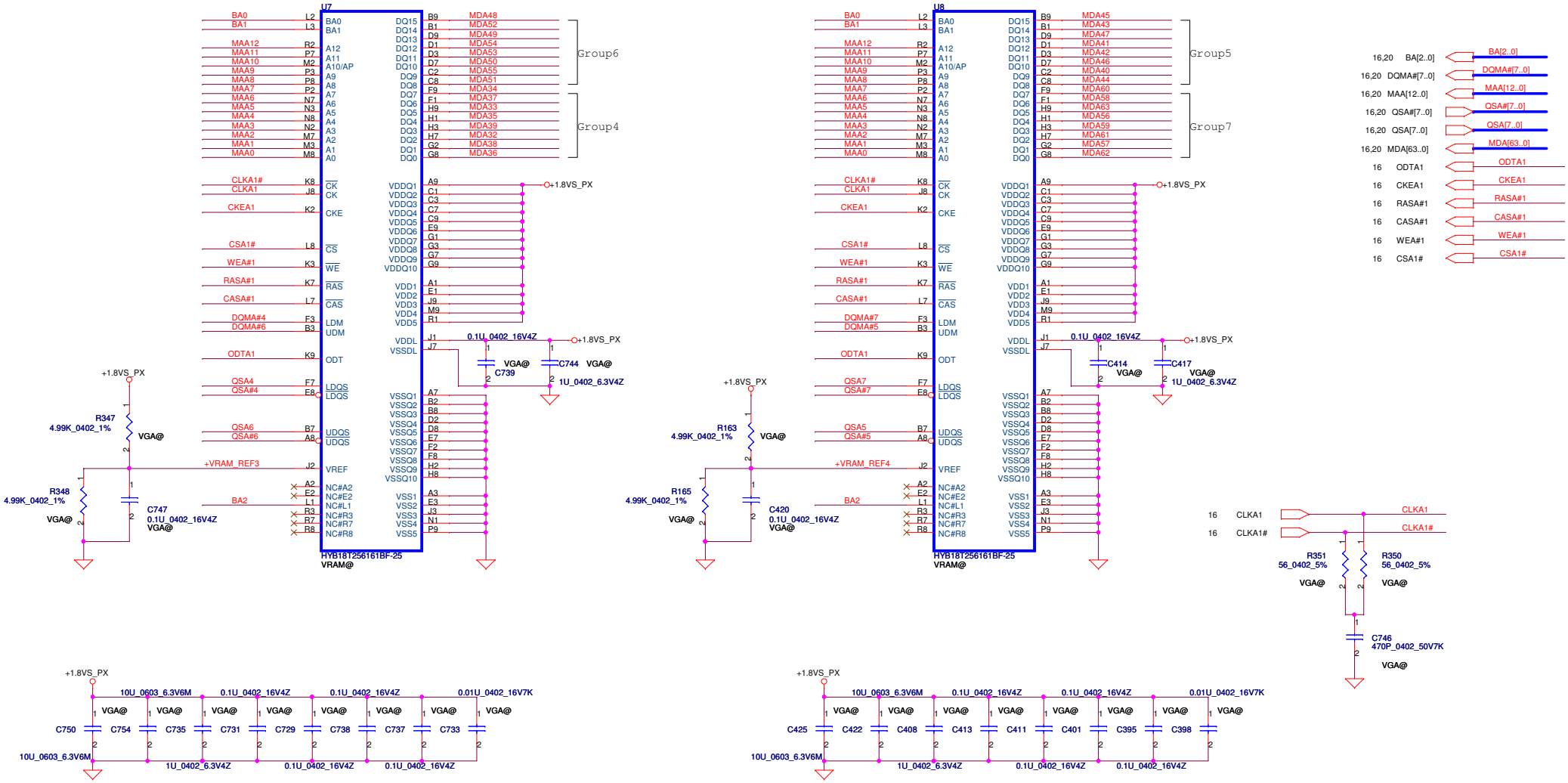
Date: Thursday, June 04, 2009 | Sheet 20 of 58



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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title: M92 VRAM
				Size: Custom; Document Number: NBLG0 LA-5521P; Rev: 0.1
				Date: Thursday, June 04, 2009; Sheet 21 of 58

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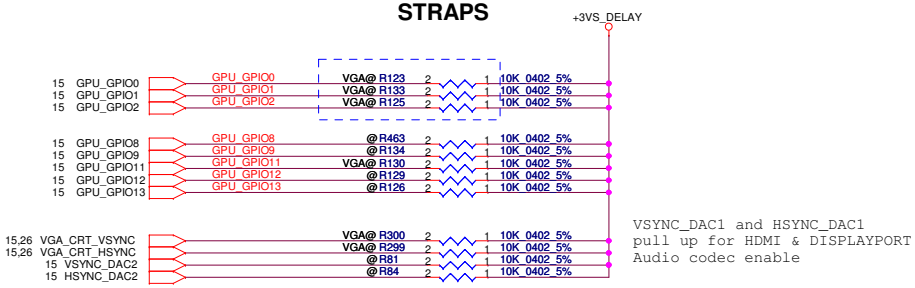
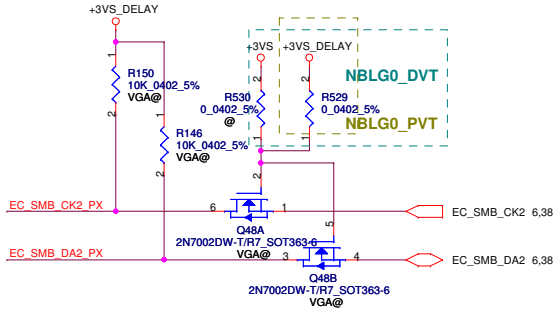
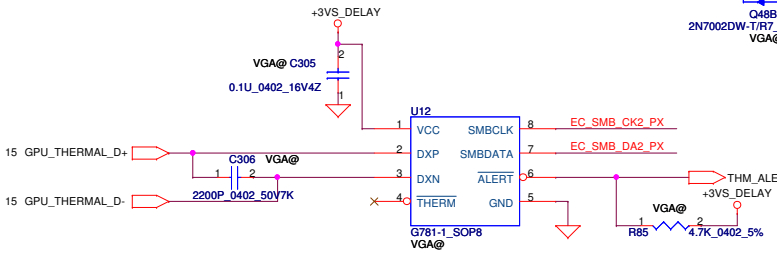
STRAPS



VSYNC_DAC1 and HSYNC_DAC1
pull up for HDMI & DISPLAYPORT
Audio codec enable

External VGA Thermal Sensor





Address 1001 101X b

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable	1 : PCIe bus Full Tx output swing 0 : PCIe bus 50% Tx output swing
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable	1 : Tx de-emphasis enabled 0 : Tx de-emphasis disabled
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 (5.0 GT/s capability will be controlled by software)
VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller	0 : VGA Controller capacity enabled 1 : The device will not be recognized as the system's VGA controller
CONFIG(2:0)	GPIO[13:11]	Size of the primary memory apertures	0 0 1
VIP_DEVICE_STRAP_EN	V2SYNC		0
RESERVED	H2SYNC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
RESERVED	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
CCBYPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0

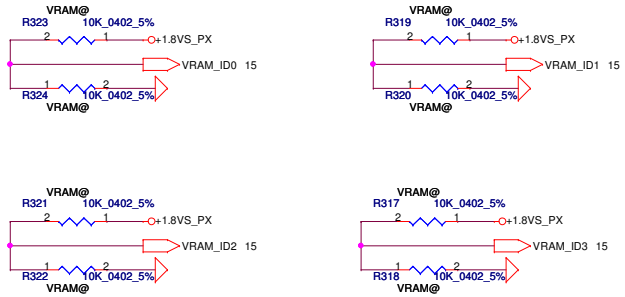
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN



STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M92-M2 XT	JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (Q-die)	SA00002MD00	0 0 0 0
			JV40-TR_NBLG0	512M(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
			JV40-TR_NBLG0	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00 PVT	0 0 1 0
			JV40-TR_NBLG0	512M(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

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Compal Electronics, Inc.

Title: M92 Strap

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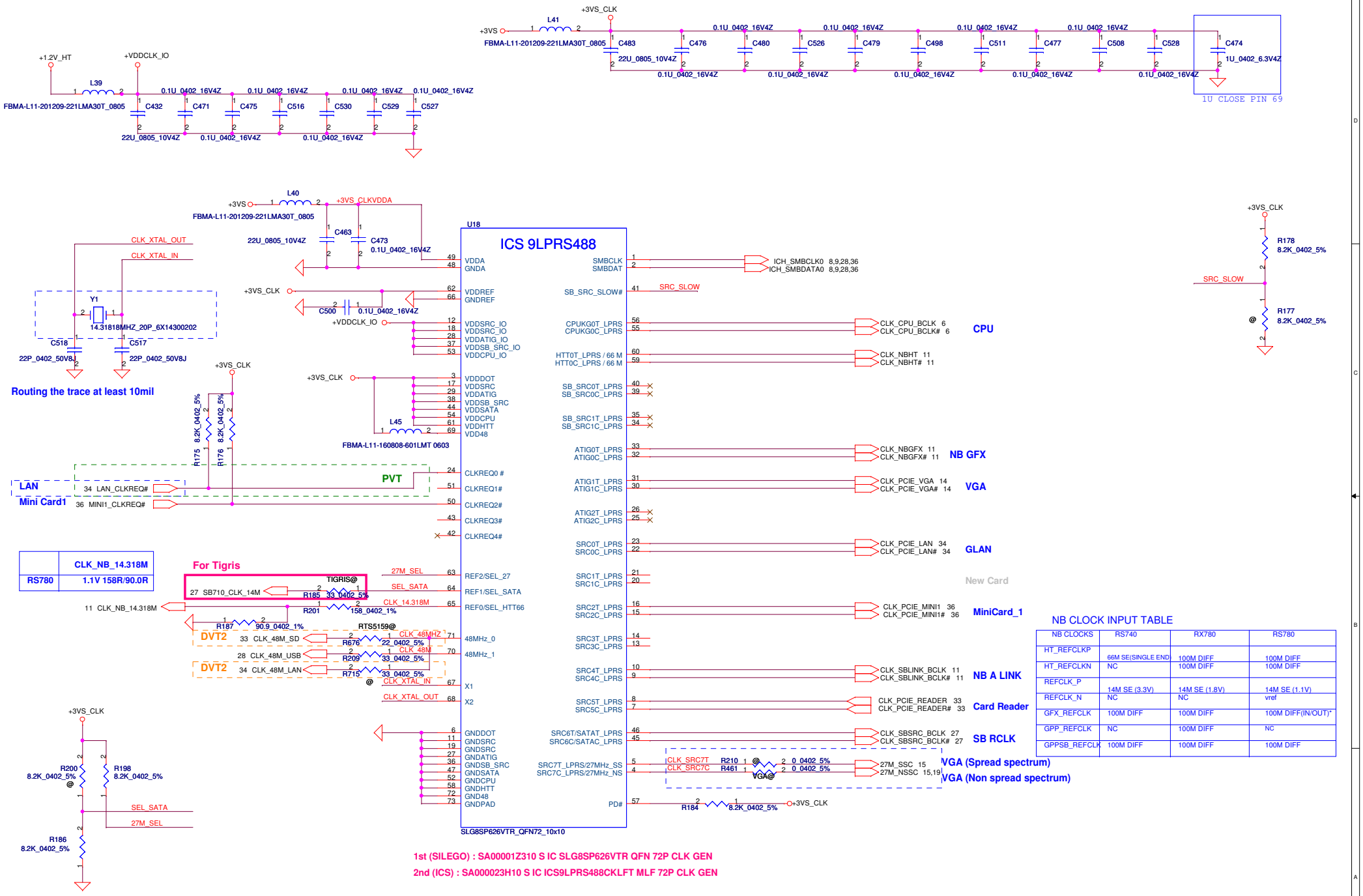

	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN

2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

* default

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

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Compal Electronics, Inc.

Title: Clock generator

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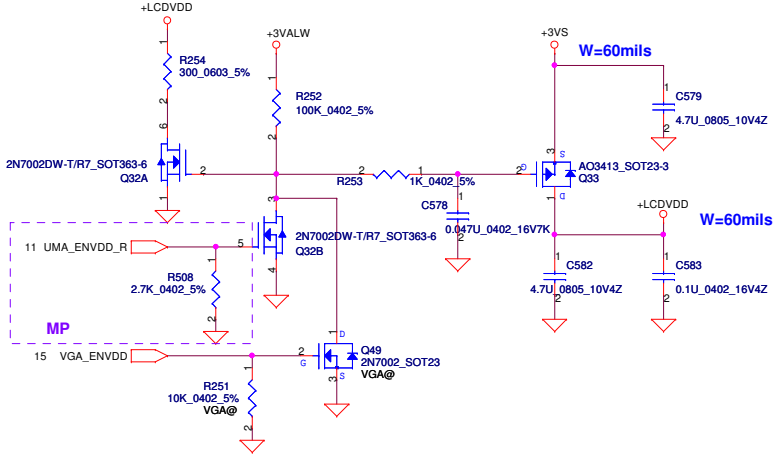
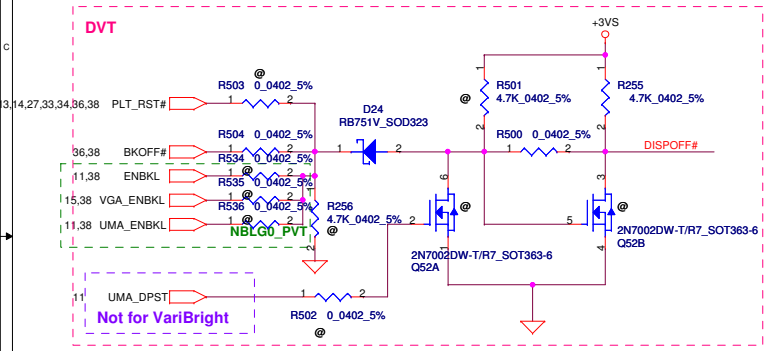
LCD POWER CIRCUIT



DVT



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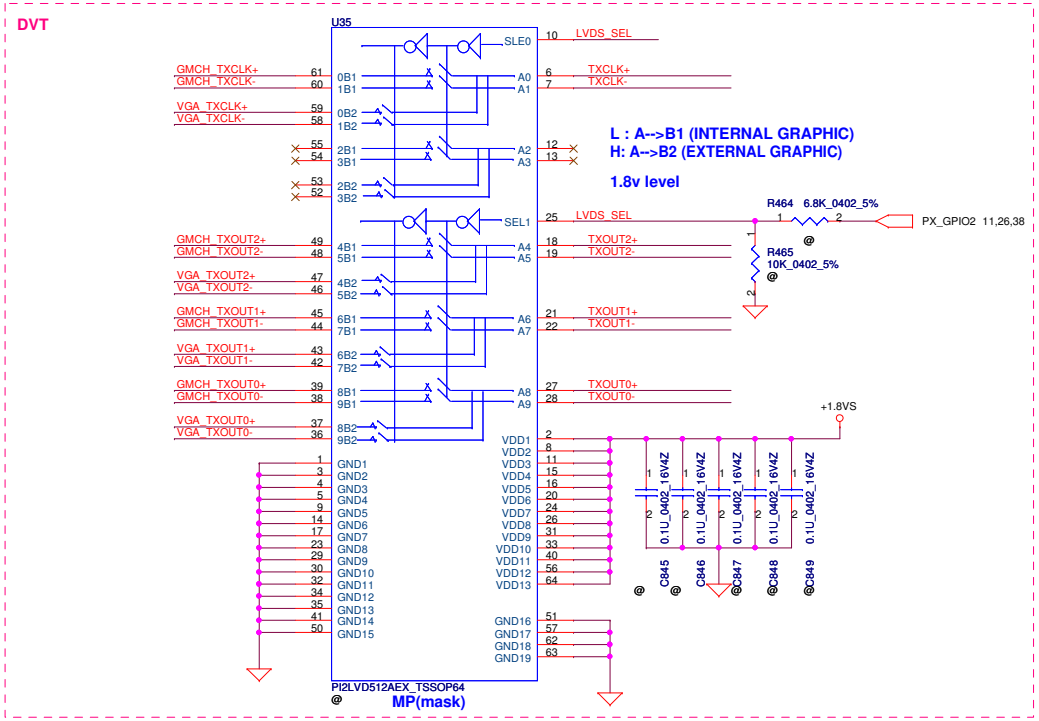
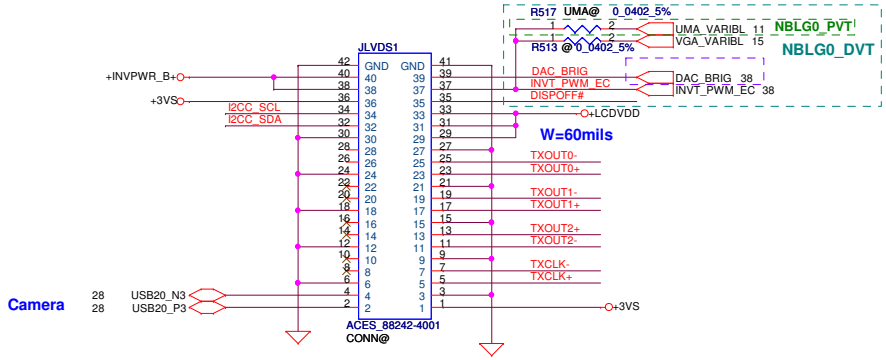
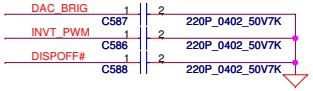


LCD/PANEL BD. Conn.





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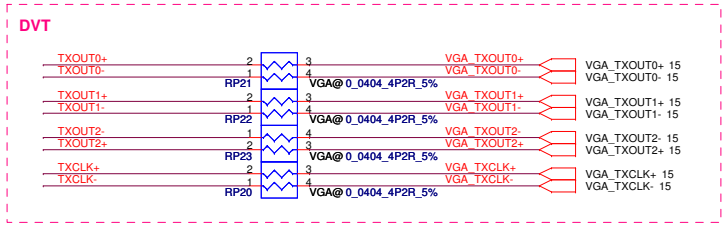

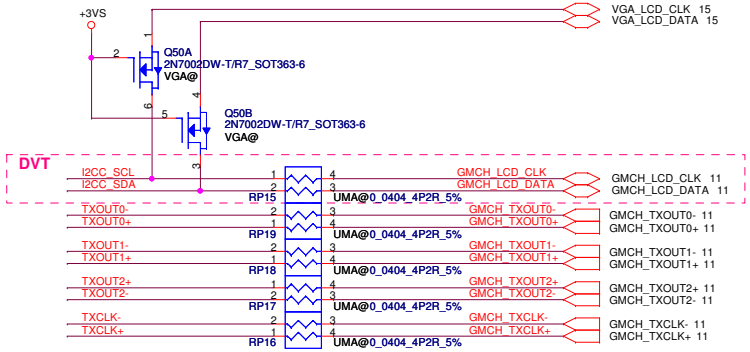

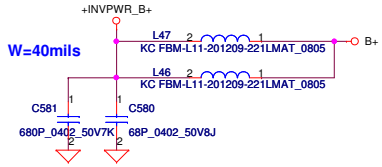

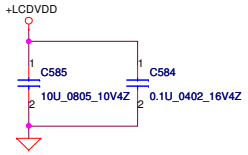

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Compal Electronics, Inc.

Title: LVDS Connector

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

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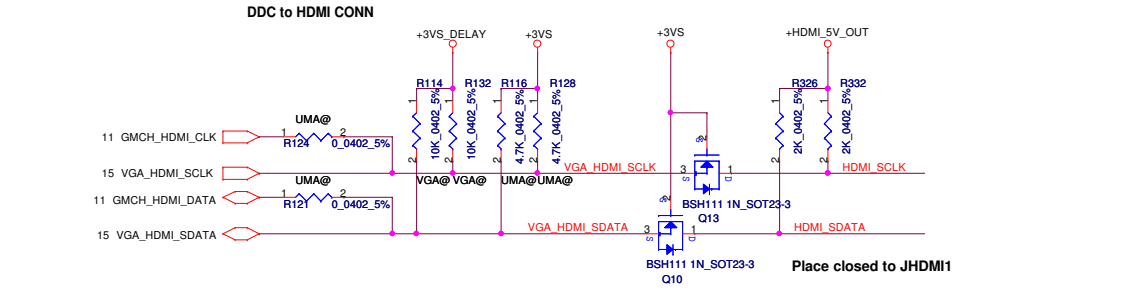

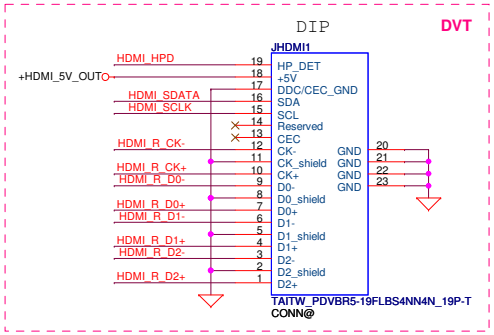

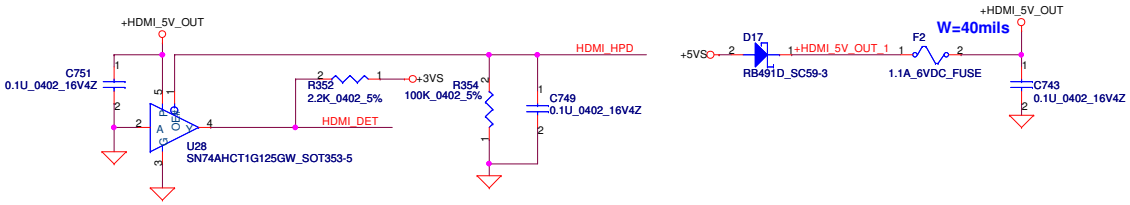

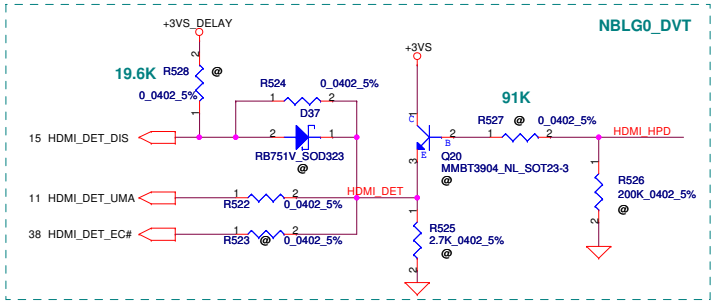

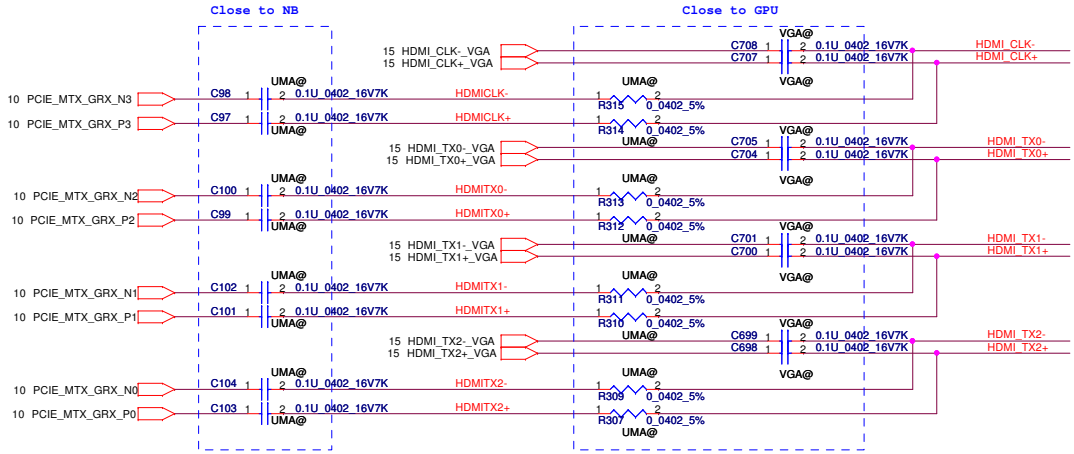

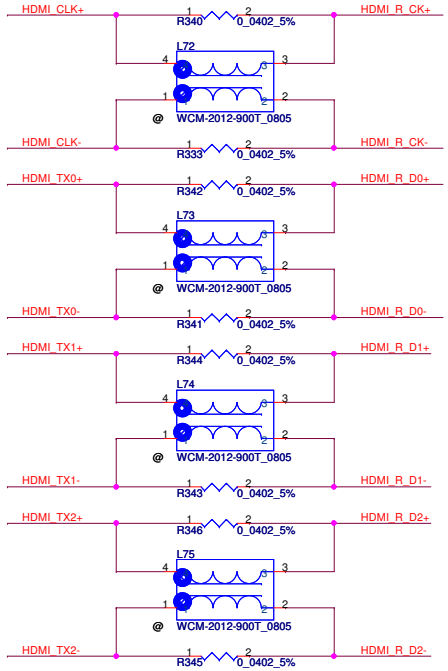

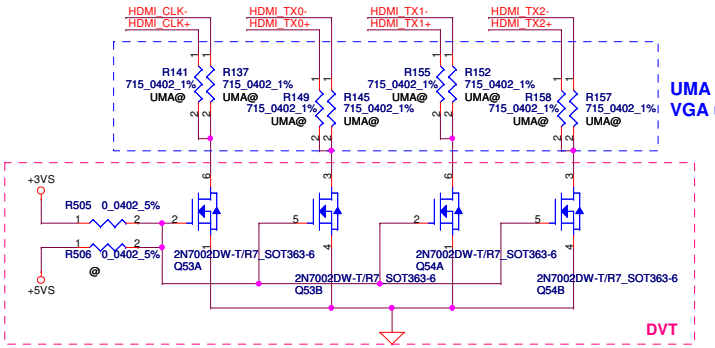

Update (For Puma / Tigris default value)

UMA use 715 ohm
VGA use 499 ohm

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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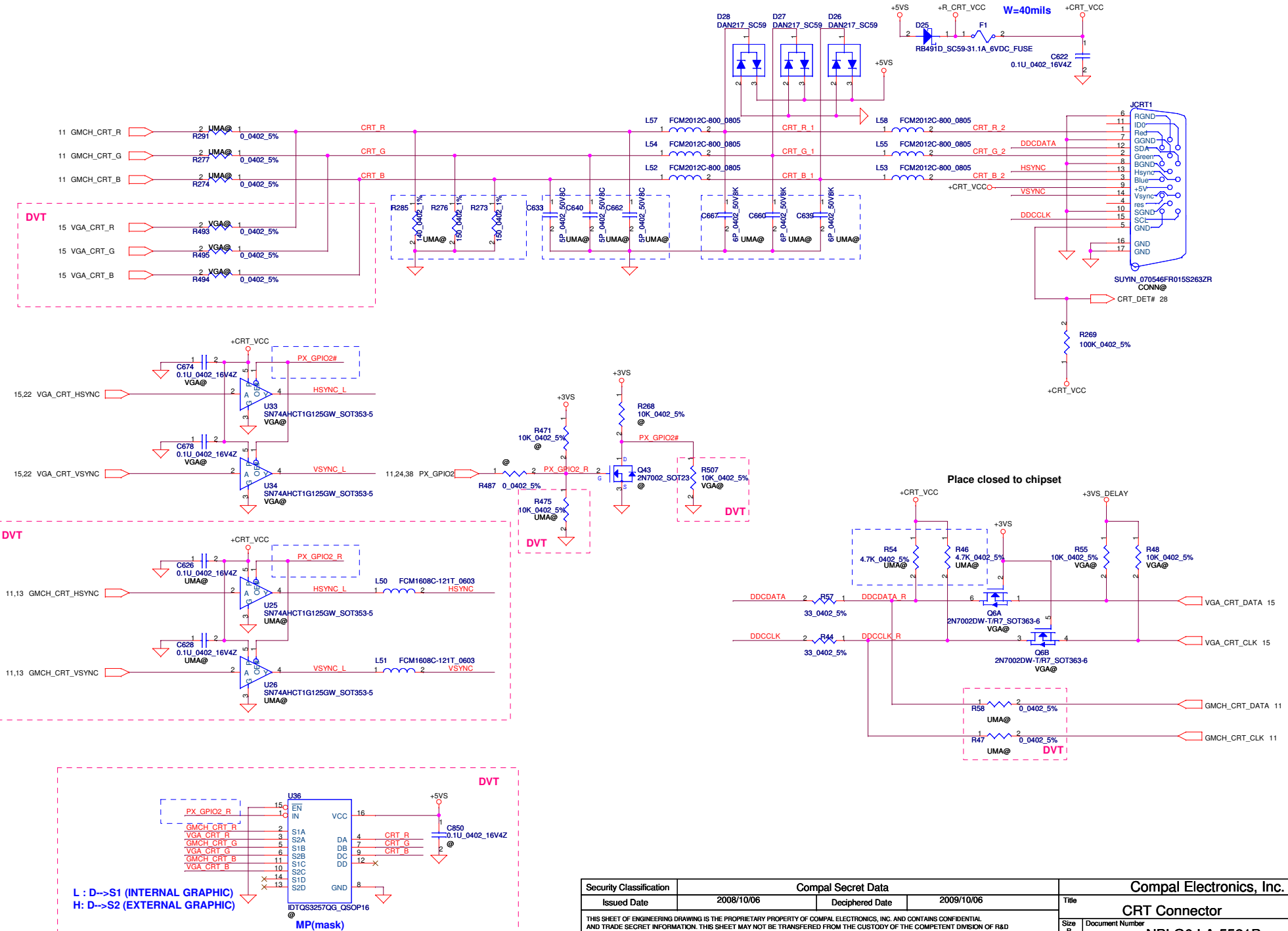
Compal Electronics, Inc.

Title: HDMI Connector

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 25 of 58

CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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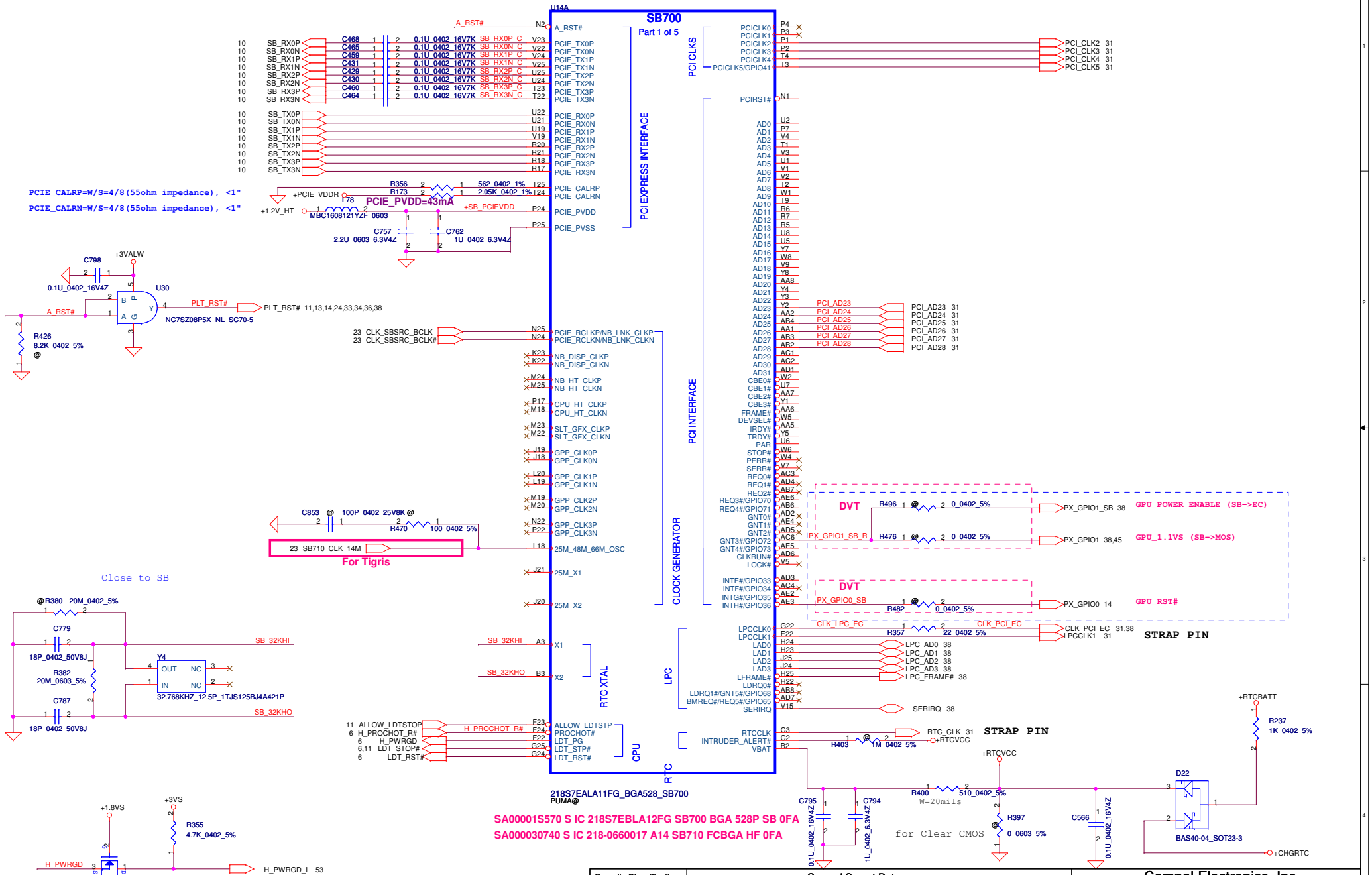
Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 26 of 58



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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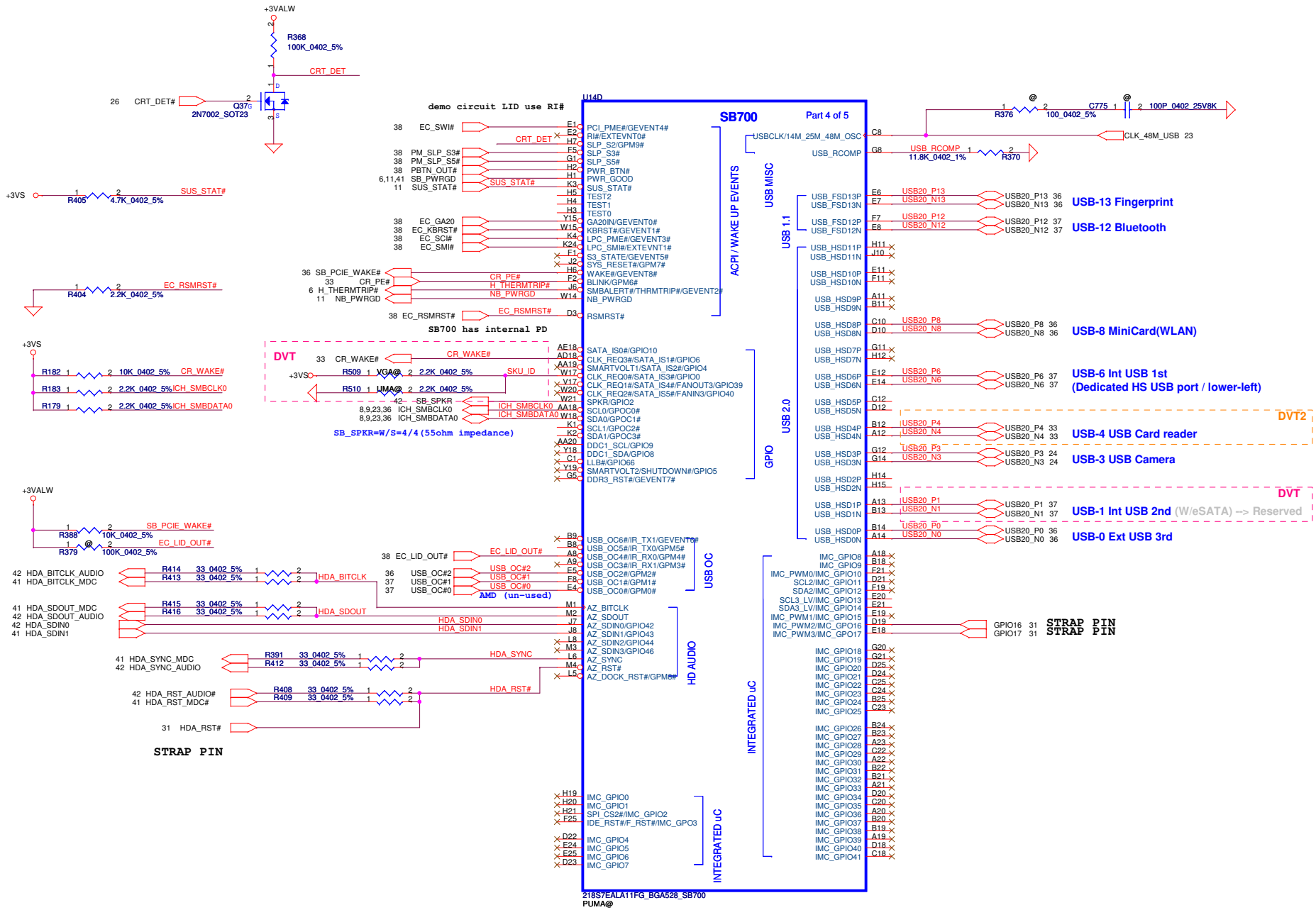
Compal Electronics, Inc.

Title: SB710-PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 27 of 58



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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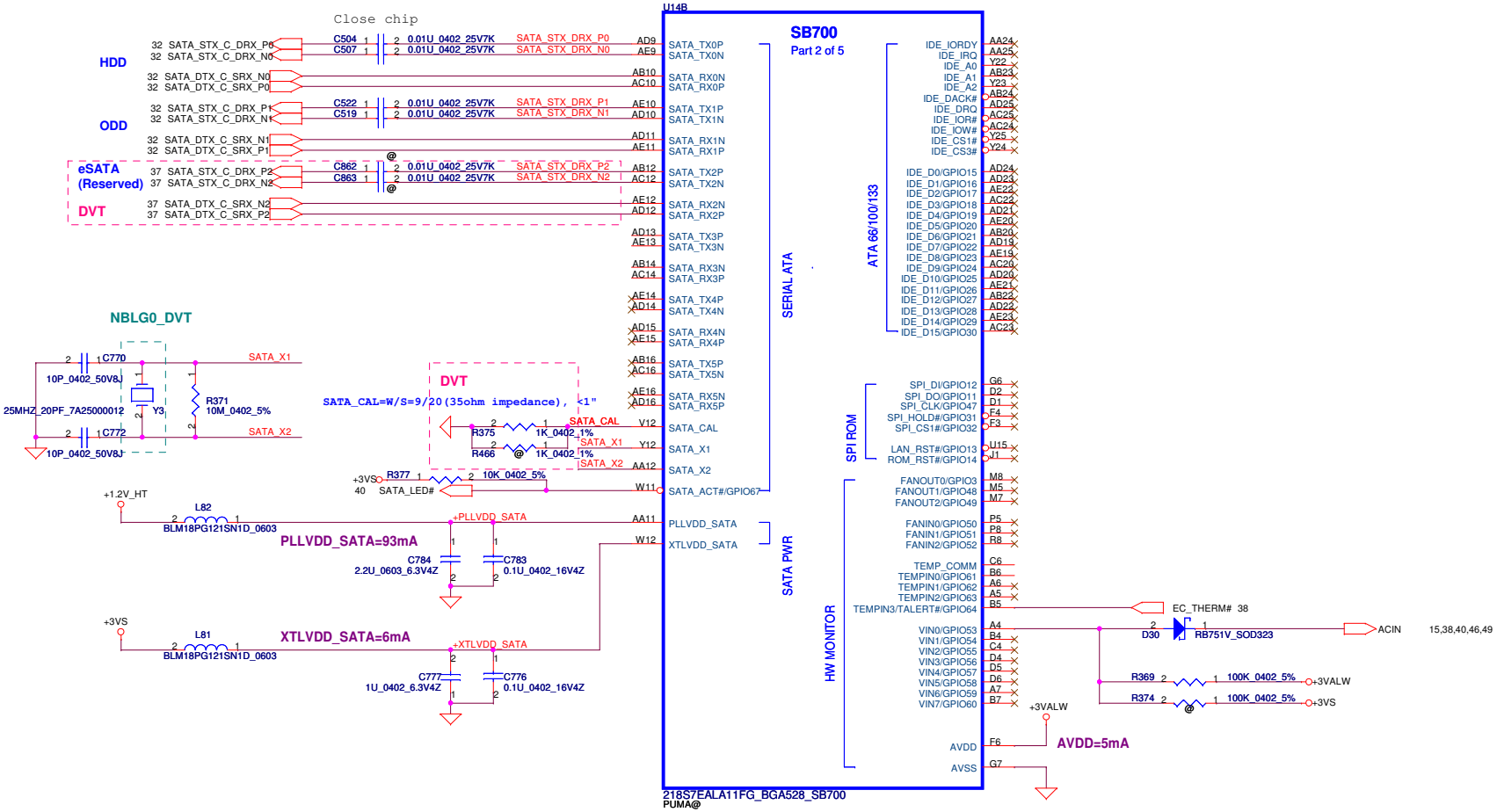
Compal Electronics, Inc.

Title: SB710 USB/HD audio

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 28 of 58



Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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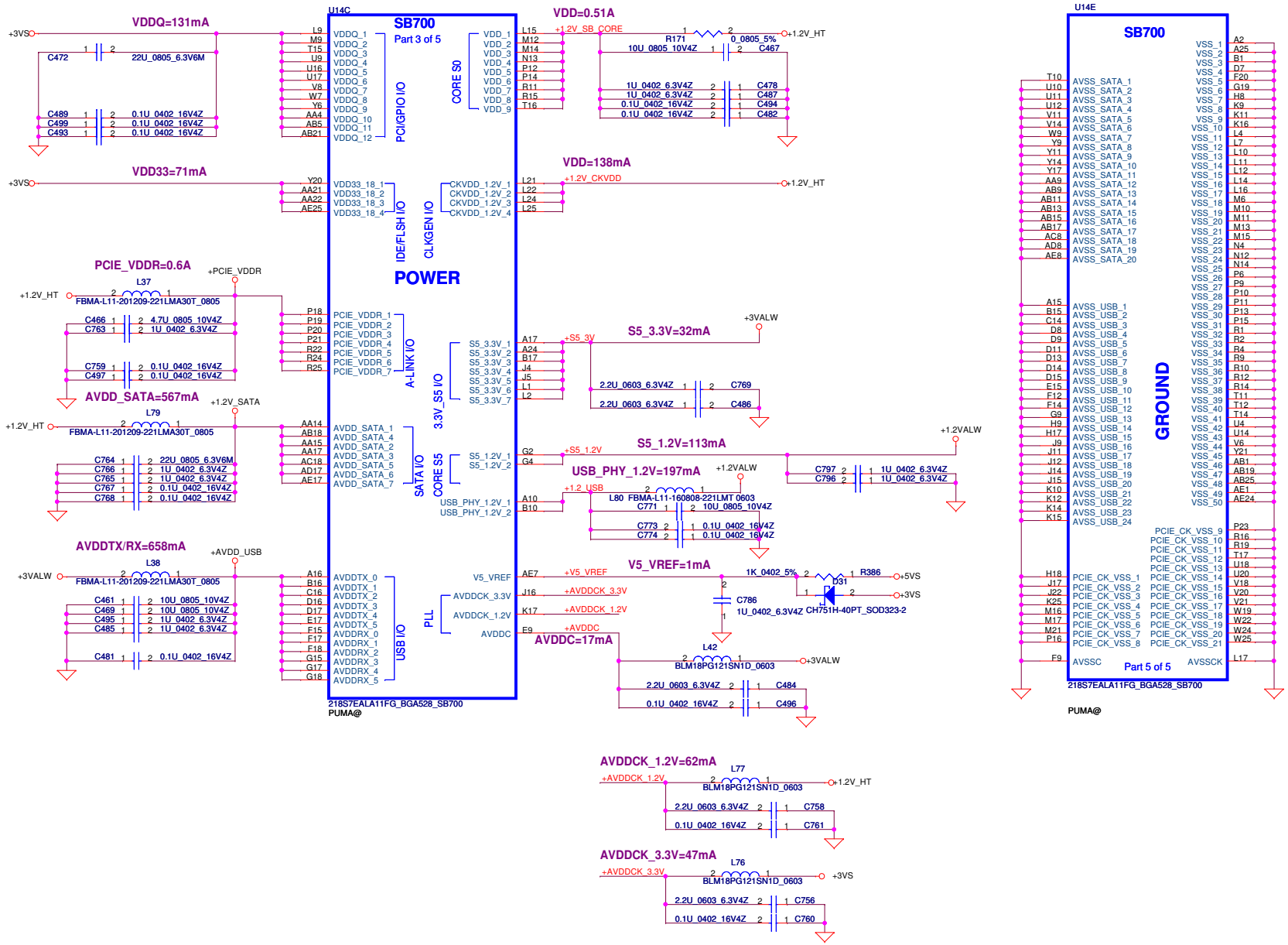
Compal Electronics, Inc.

Title: SB710 SATA/IDE/SPI

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 29 of 58



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: SB710 power/GND

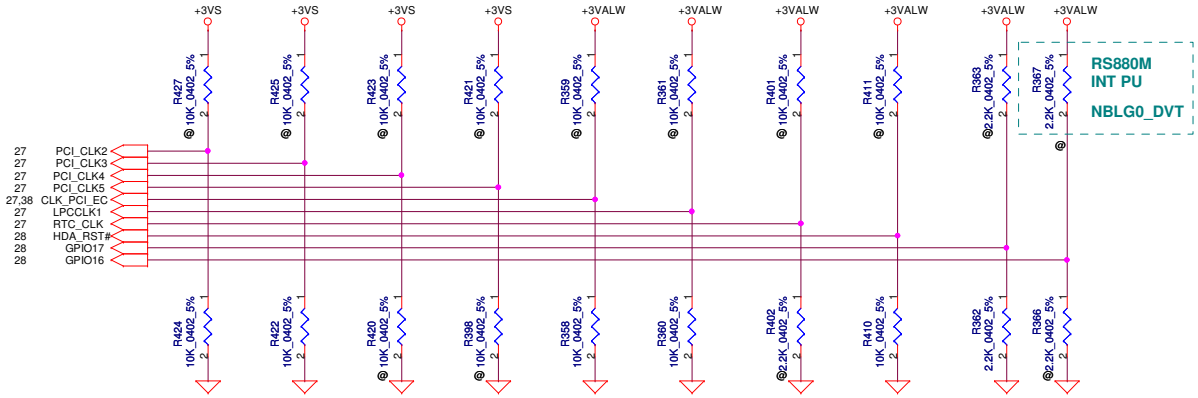
Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Sunday, April 12, 2009 | Sheet 30 of 58

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

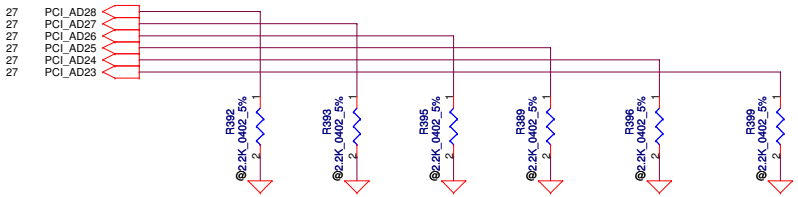
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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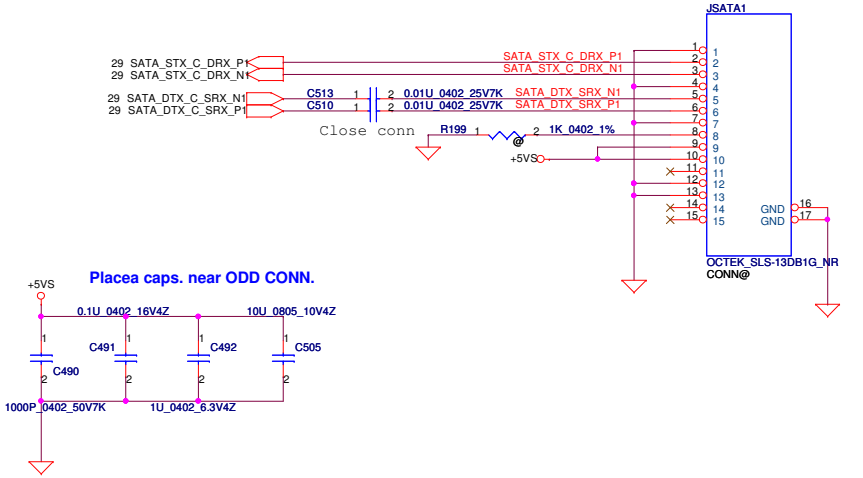
Compal Electronics, Inc.

Title: SB710 STRAPS

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

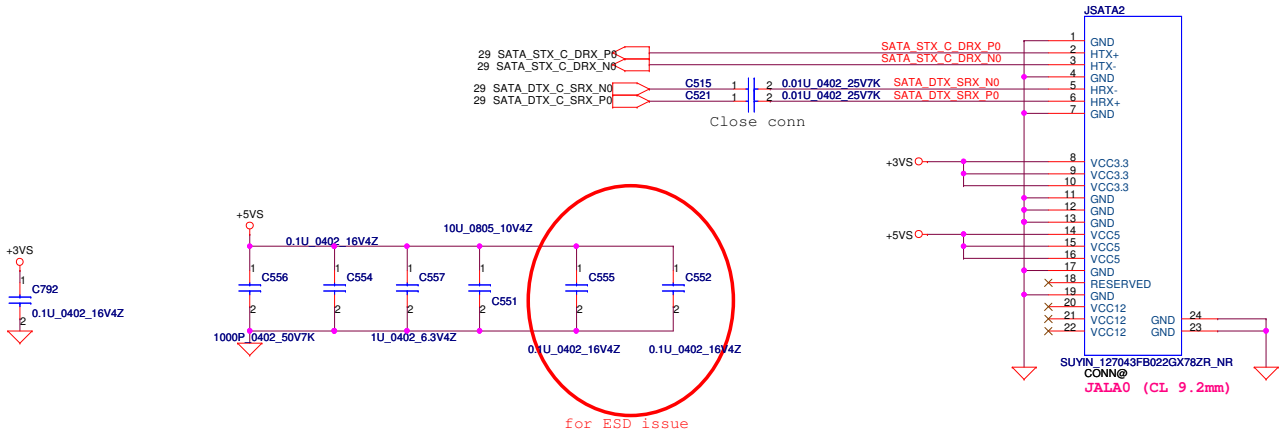
Date: Thursday, June 04, 2009 | Sheet 31 of 58

SATA ODD Conn.



Placea caps. near ODD CONN.

SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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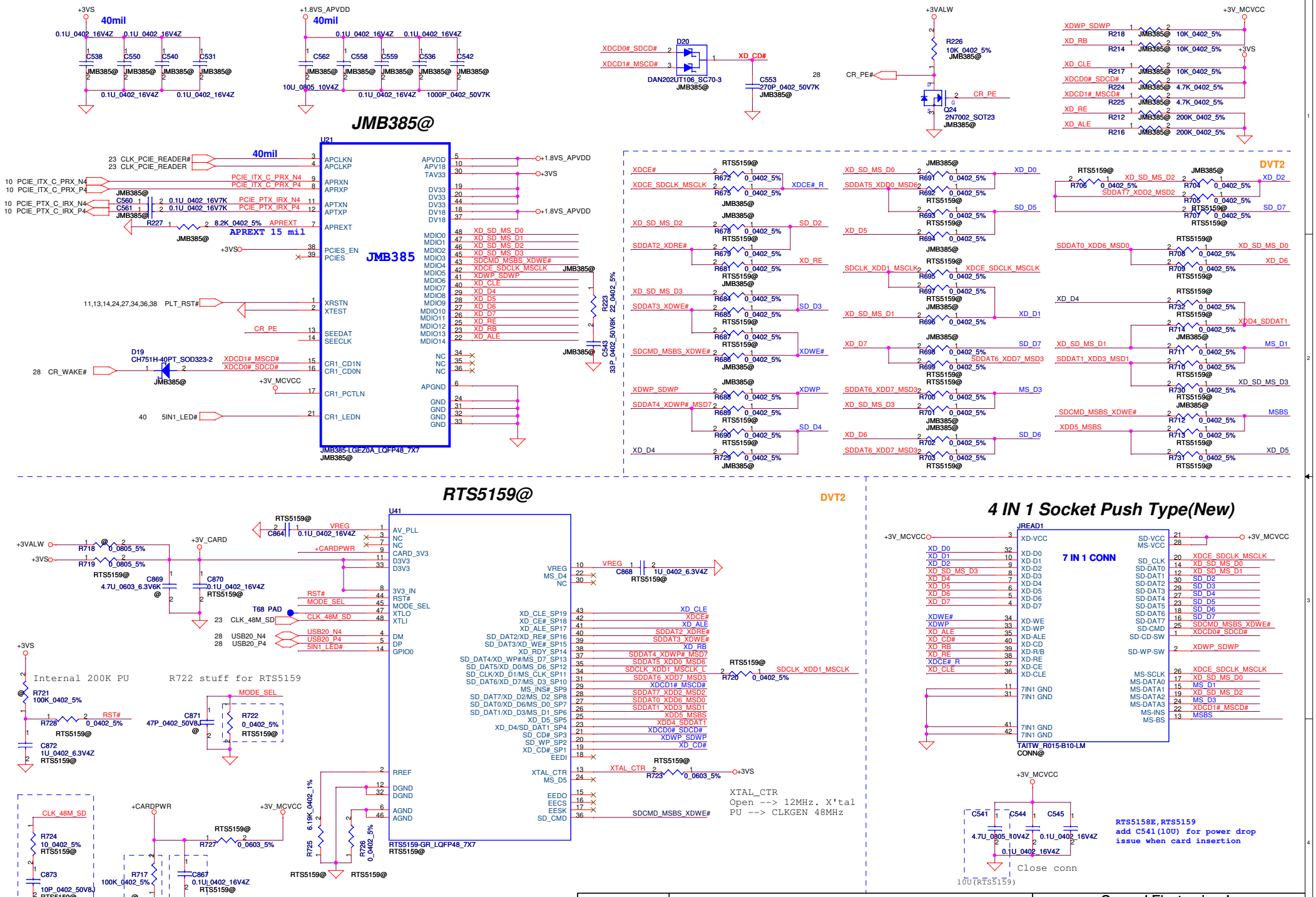
Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 32 of 58



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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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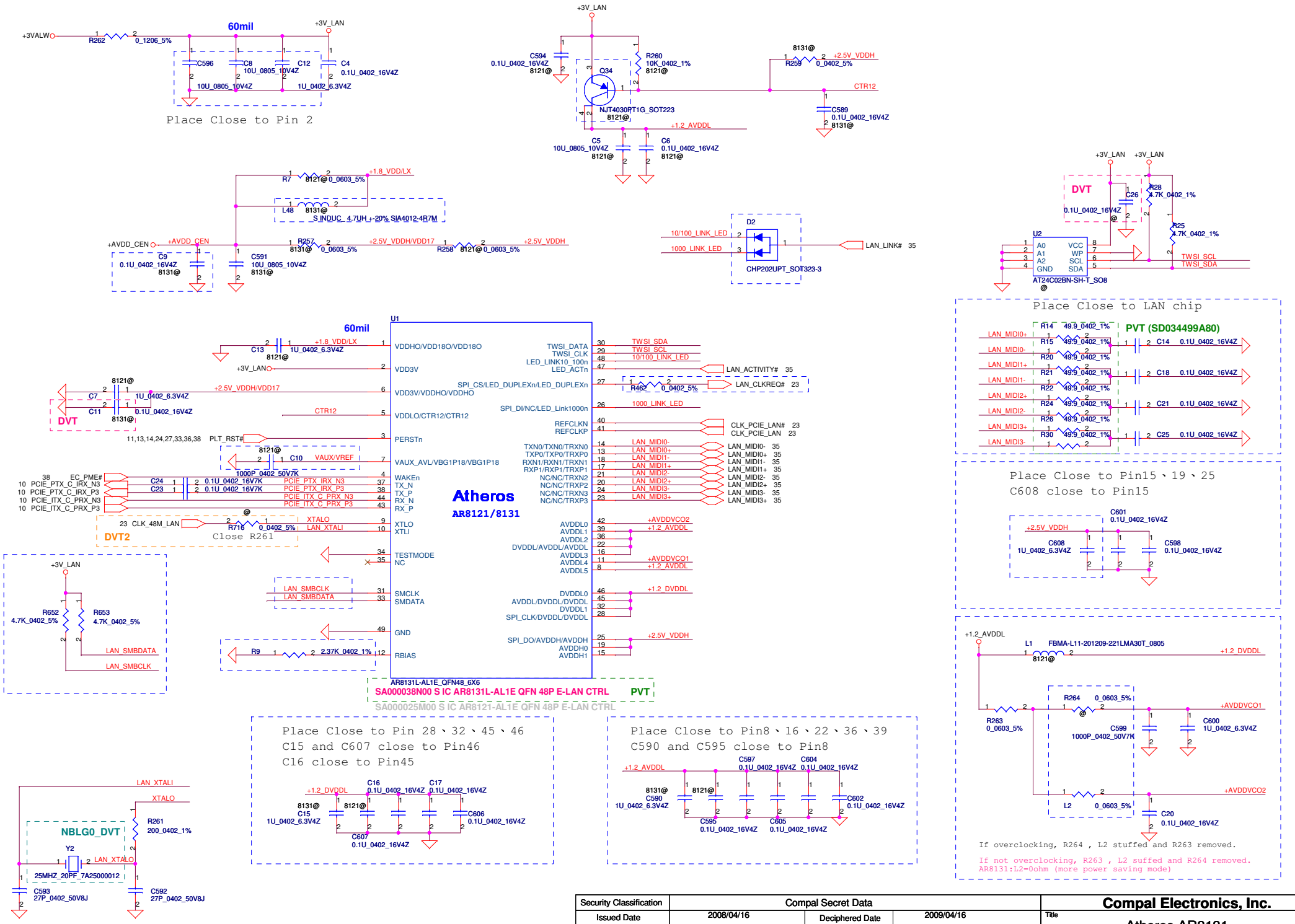
Compal Electronics, Inc.

Title: RTS5159 / (JMB385) card reader

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 33 of 58



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

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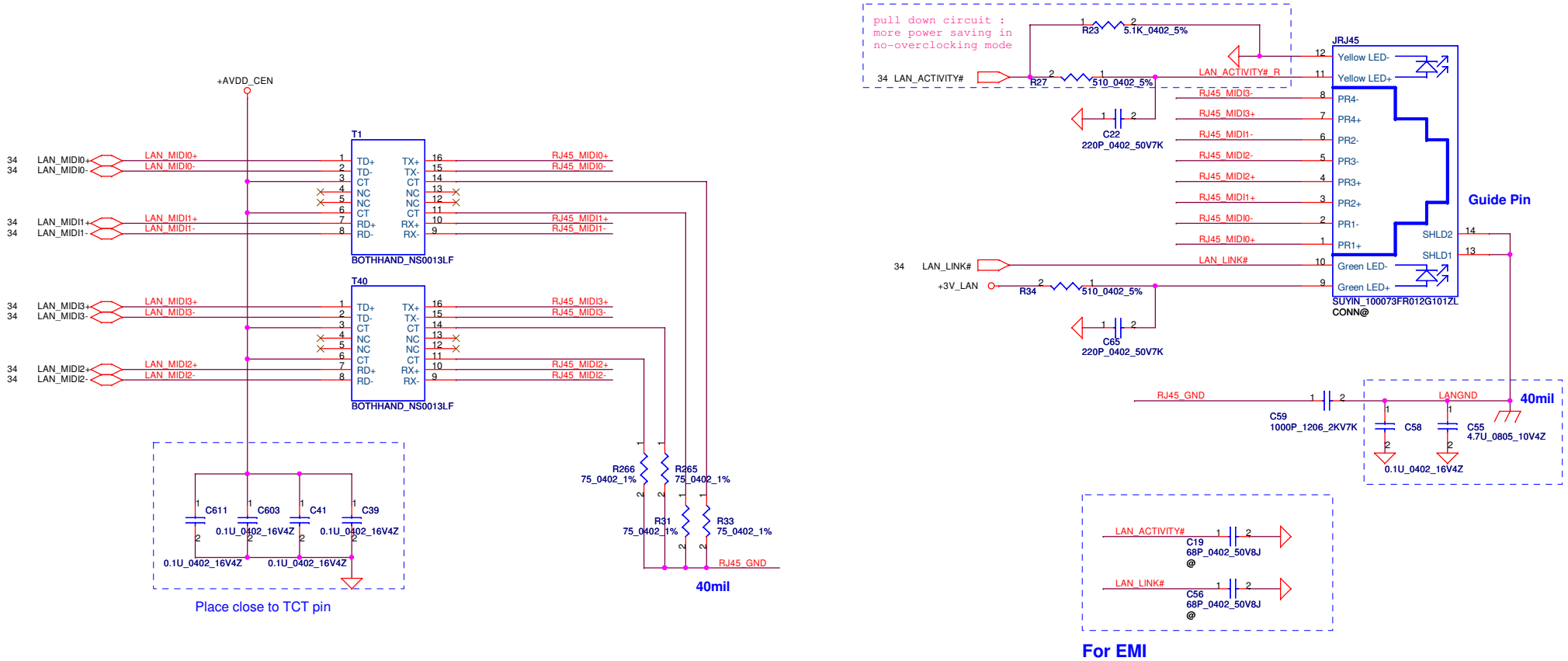
Compal Electronics, Inc.

Title: Atheros AR8131

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 34 of 58



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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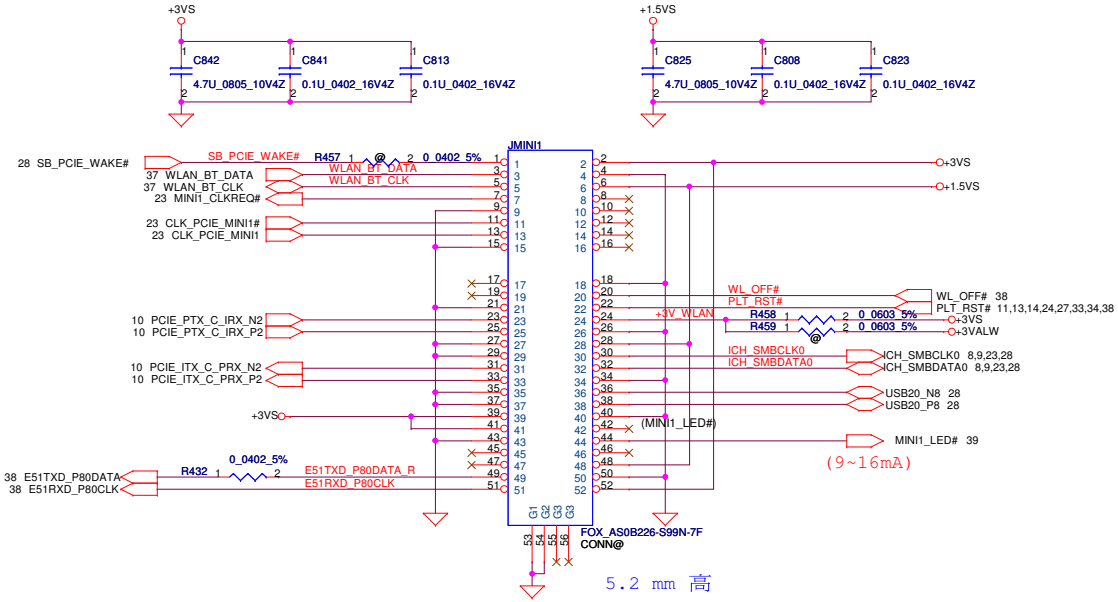
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

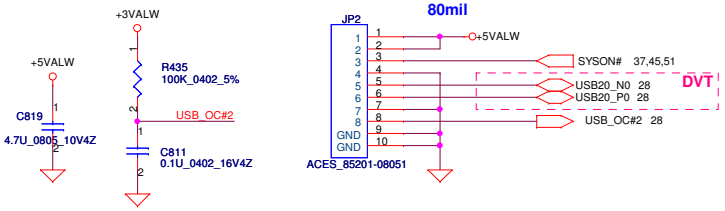
Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

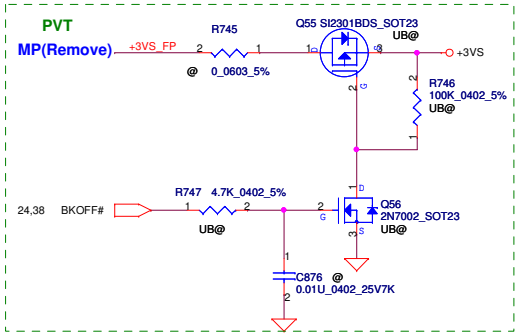
Date: Thursday, June 04, 2009 | Sheet 35 of 58

For Wireless LAN

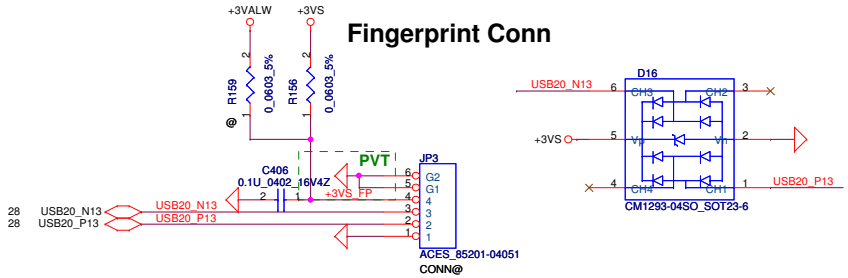


To USB/B Connector





Fingerprint Conn



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: MINI CARD (WLAN) / FP / Ext_USB

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

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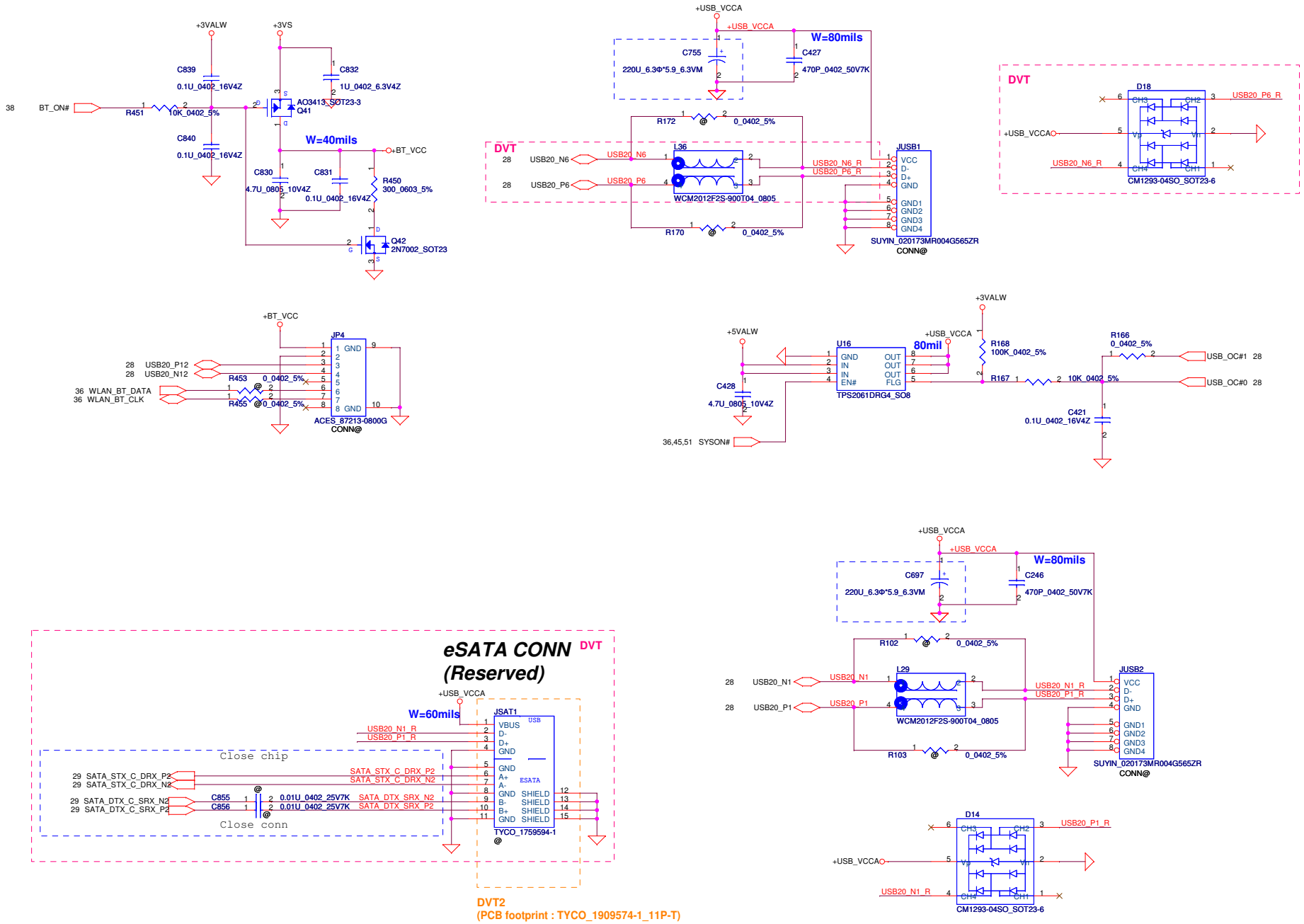
Bluetooth Conn.



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Compal Electronics, Inc.

Title: BlueTooth / Int USB x2 /eSATA

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

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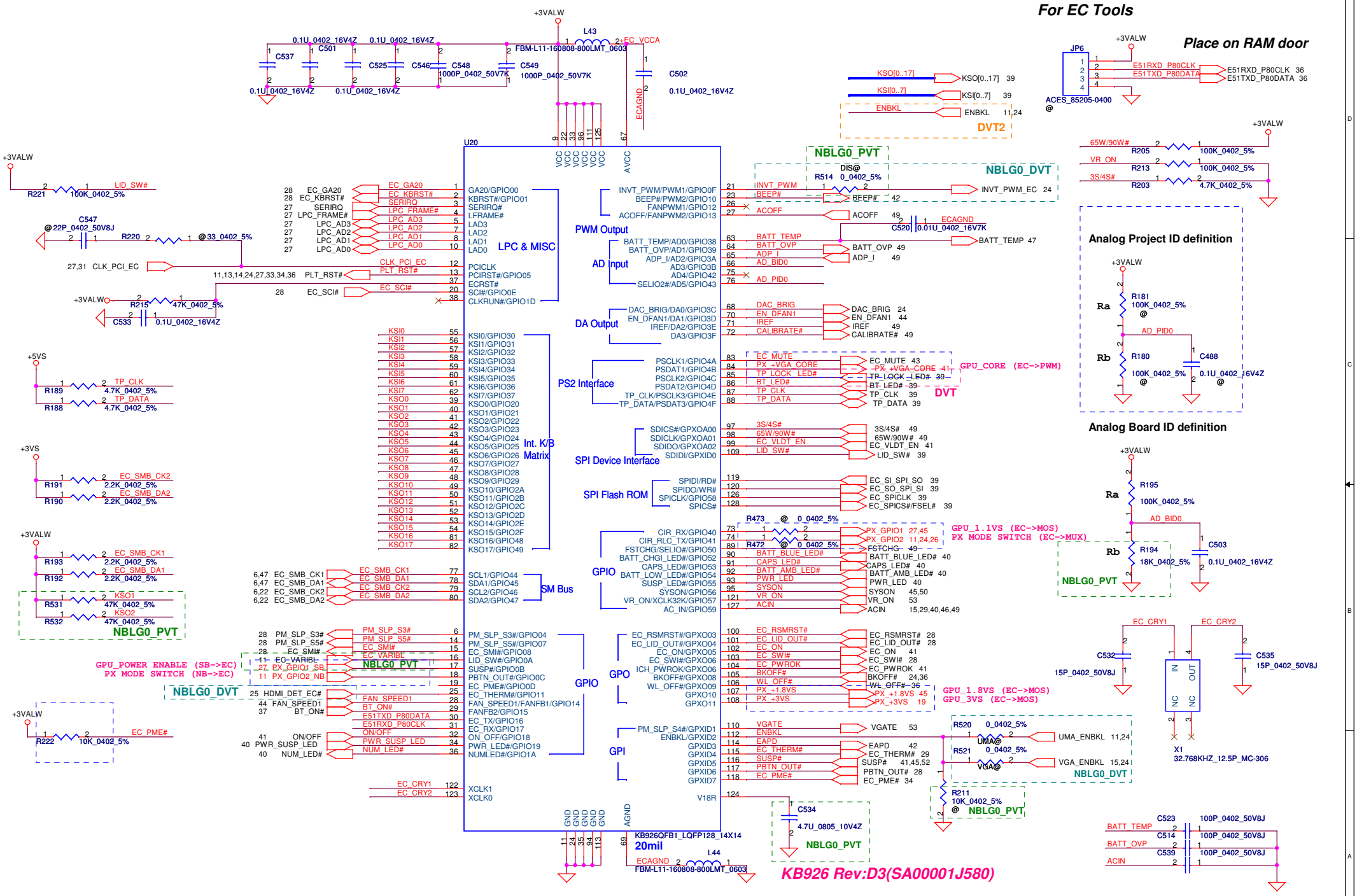

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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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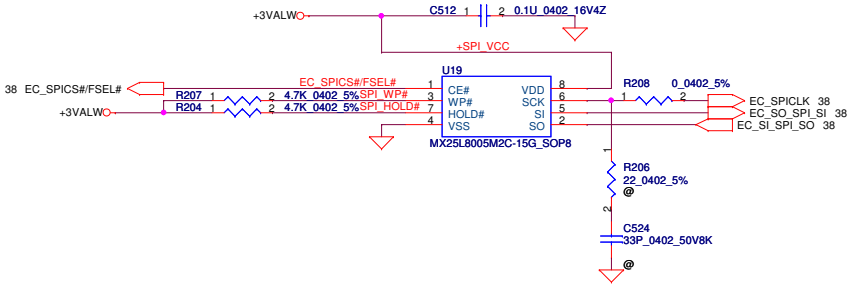
Compal Electronics, Inc.

Title: EC ENE KB926

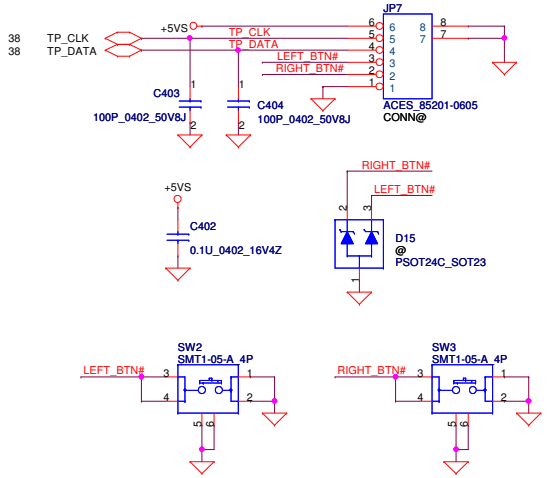
Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 38 of 58

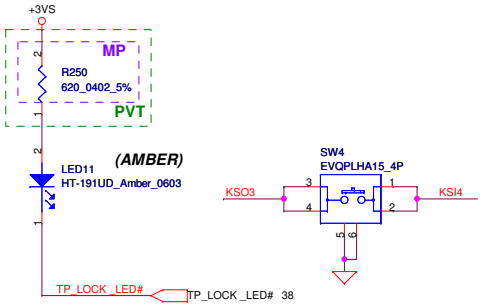
BIOS(SYS / EC / VGA)



To TP/B Conn.



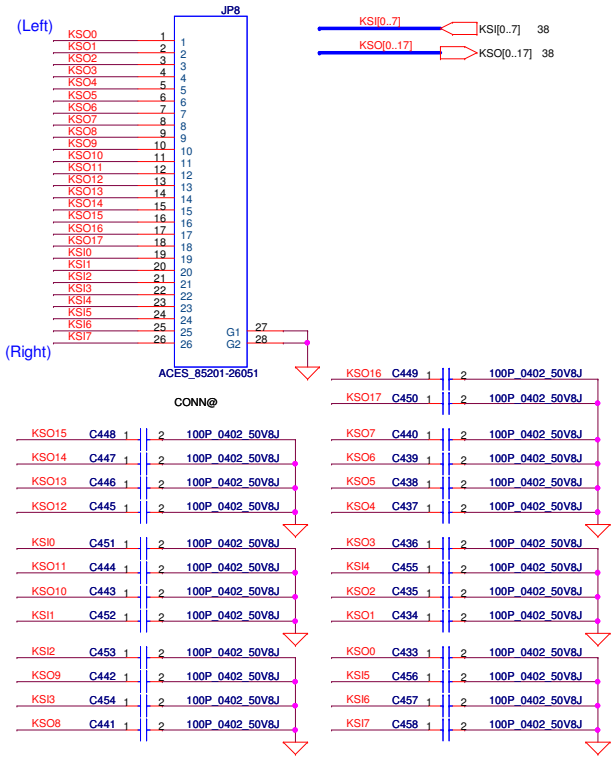
DVT



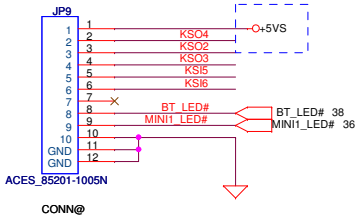
T/P lock button LED

T/P lock button

INT_KBD Conn.



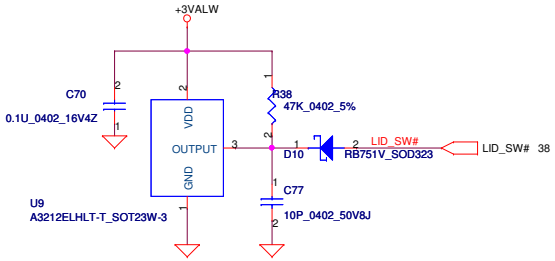
To FUN/B Conn (10PIN)



	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

Lid Switch

(Hall Effect Switch)



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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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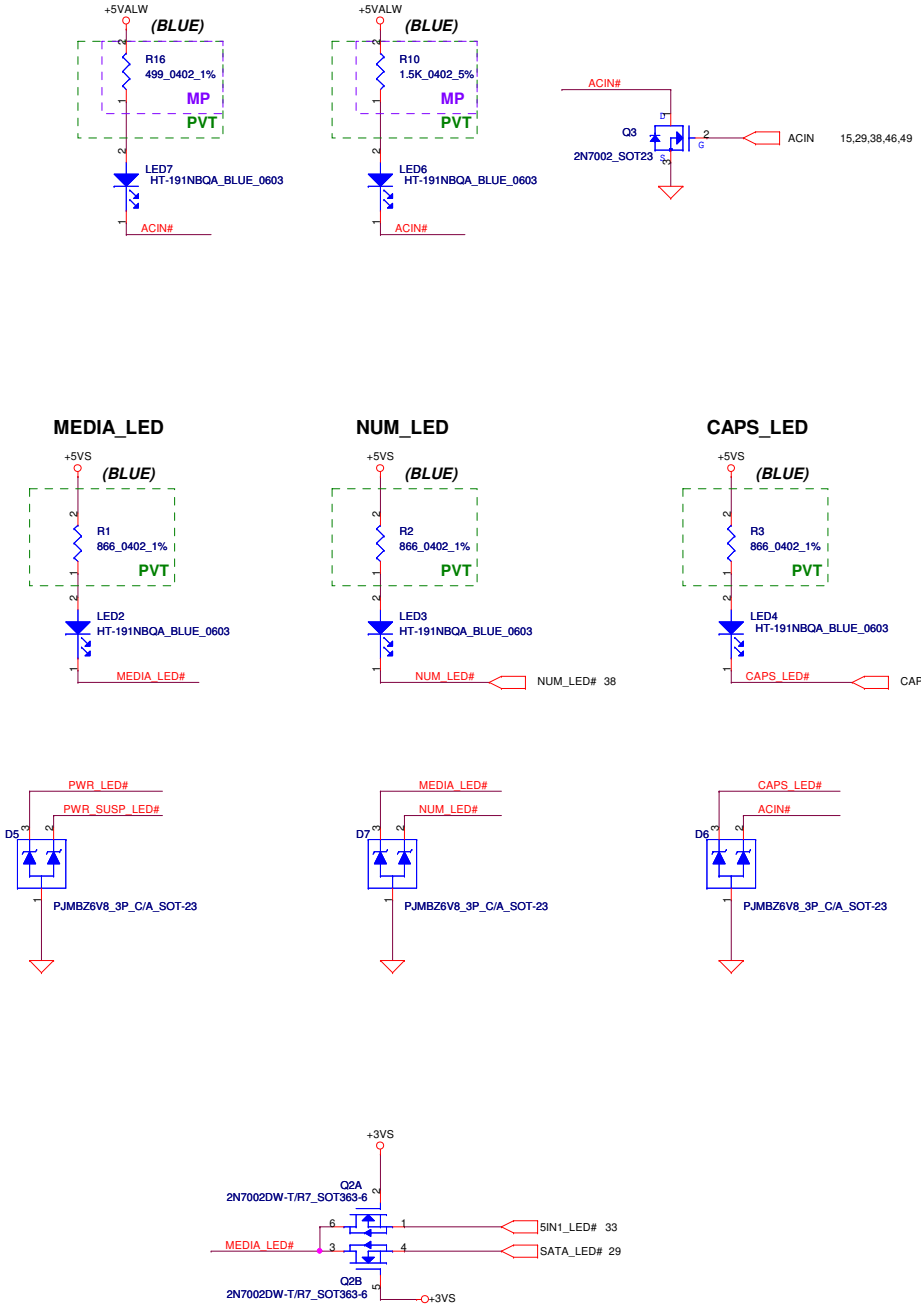
Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 39 of 58

Enlightener LED



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

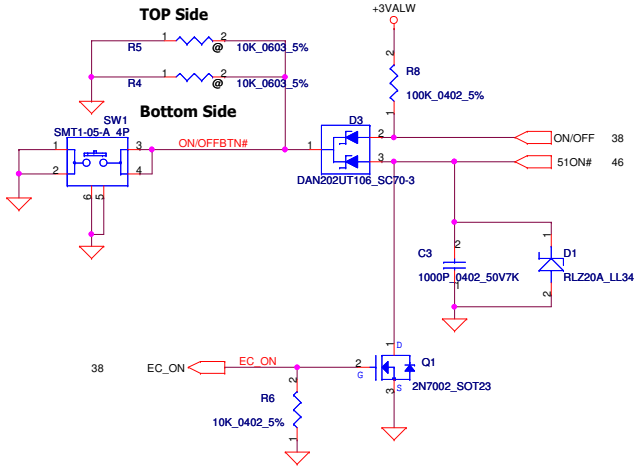
Title: LED

Size: Custom | Document Number: NBLG0 LA-5521P | Rev: 0.1

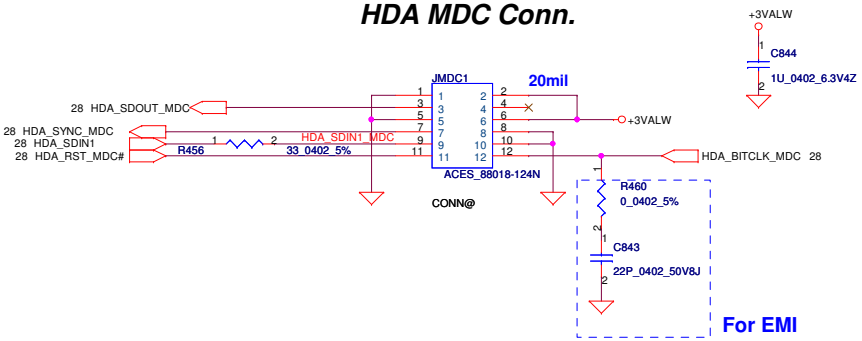
Date: Thursday, June 04, 2009 | Sheet 40 of 58

Power Button

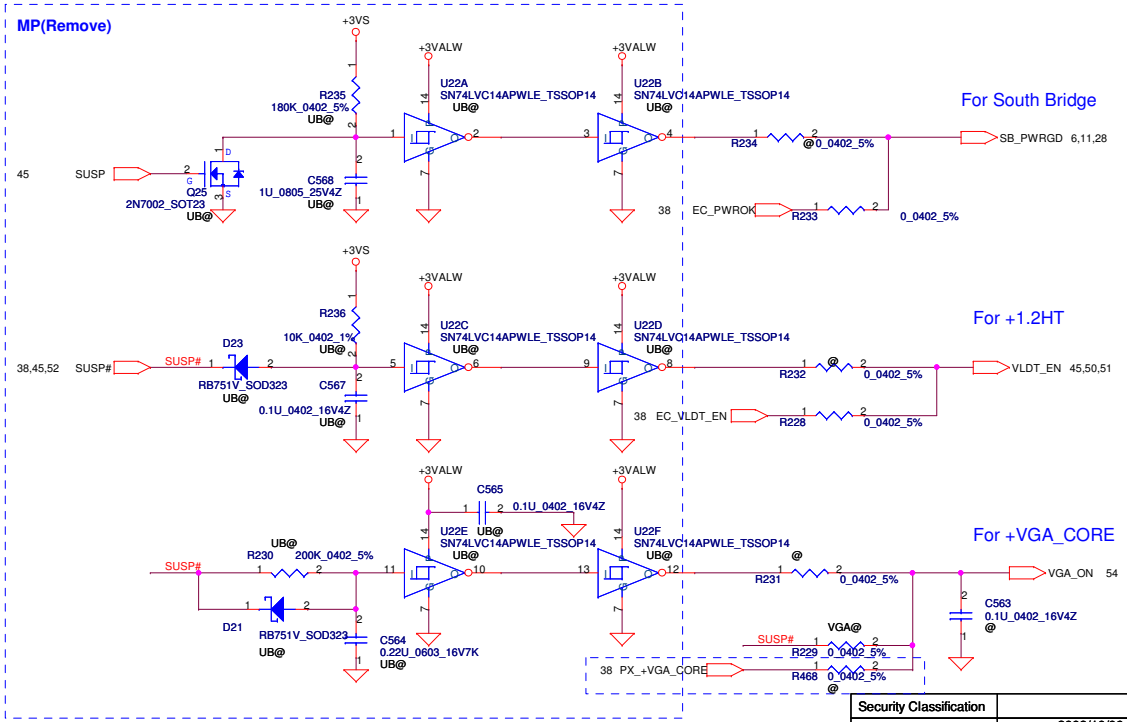
ON/OFF switch



HDA MDC Conn.



Power ON Circuit



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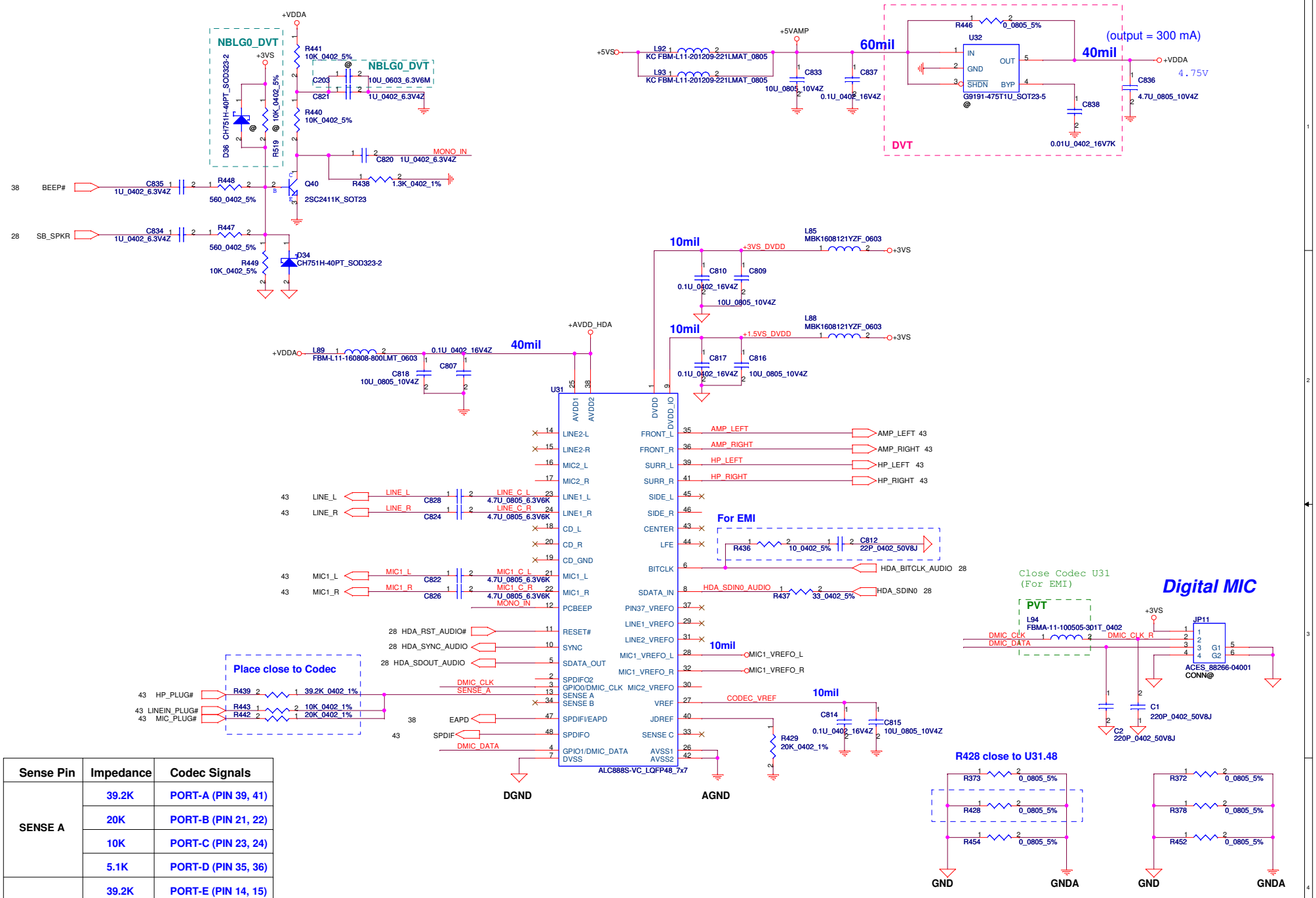
Compal Electronics, Inc.

Title: Power OK / MDC / CIR

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 41 of 58



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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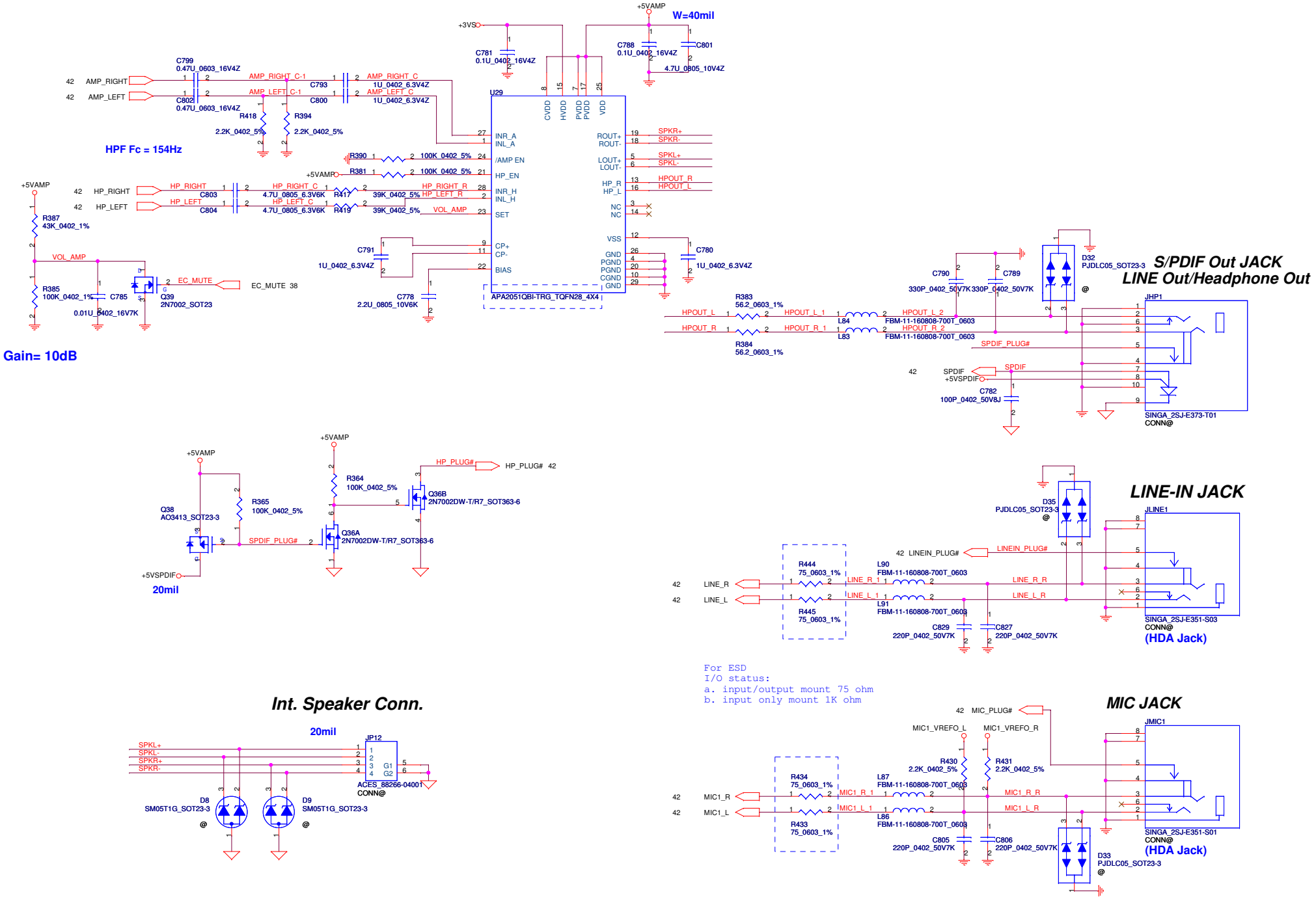
Compal Electronics, Inc.

Title: HD Audio Codec ALC888S-VC

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 42 of 58



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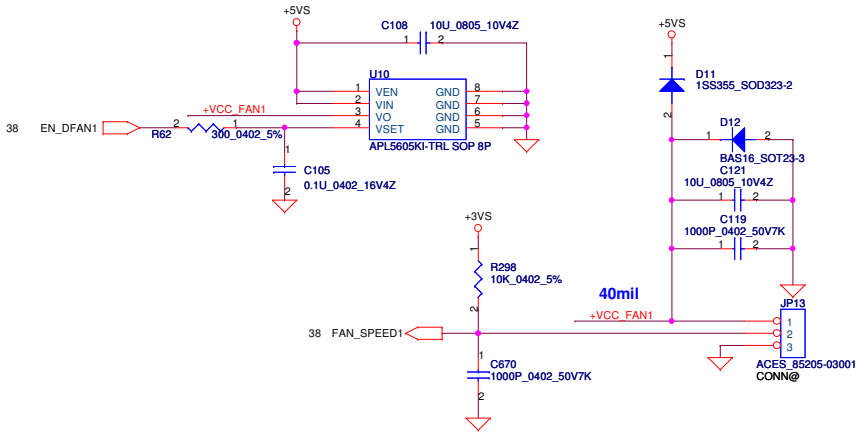
Compal Electronics, Inc.

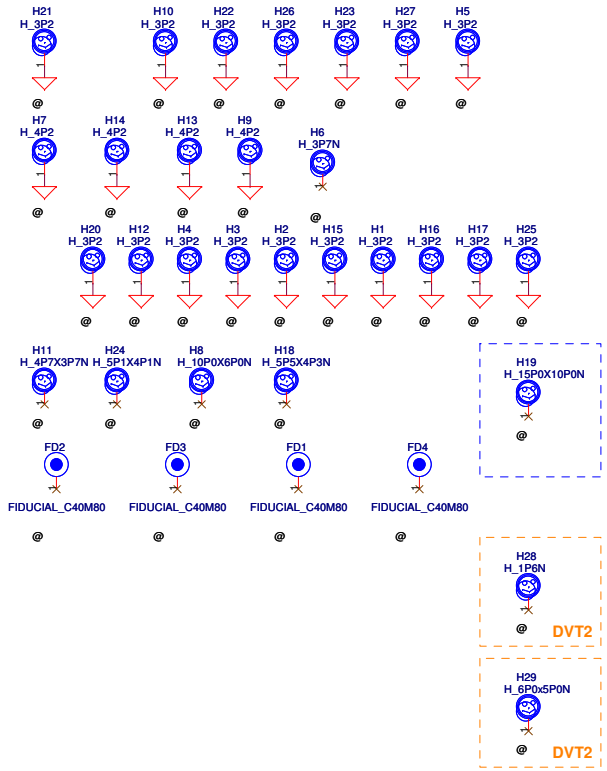
Title: Amplifier & Audio Jack

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 43 of 58

FAN1 Conn





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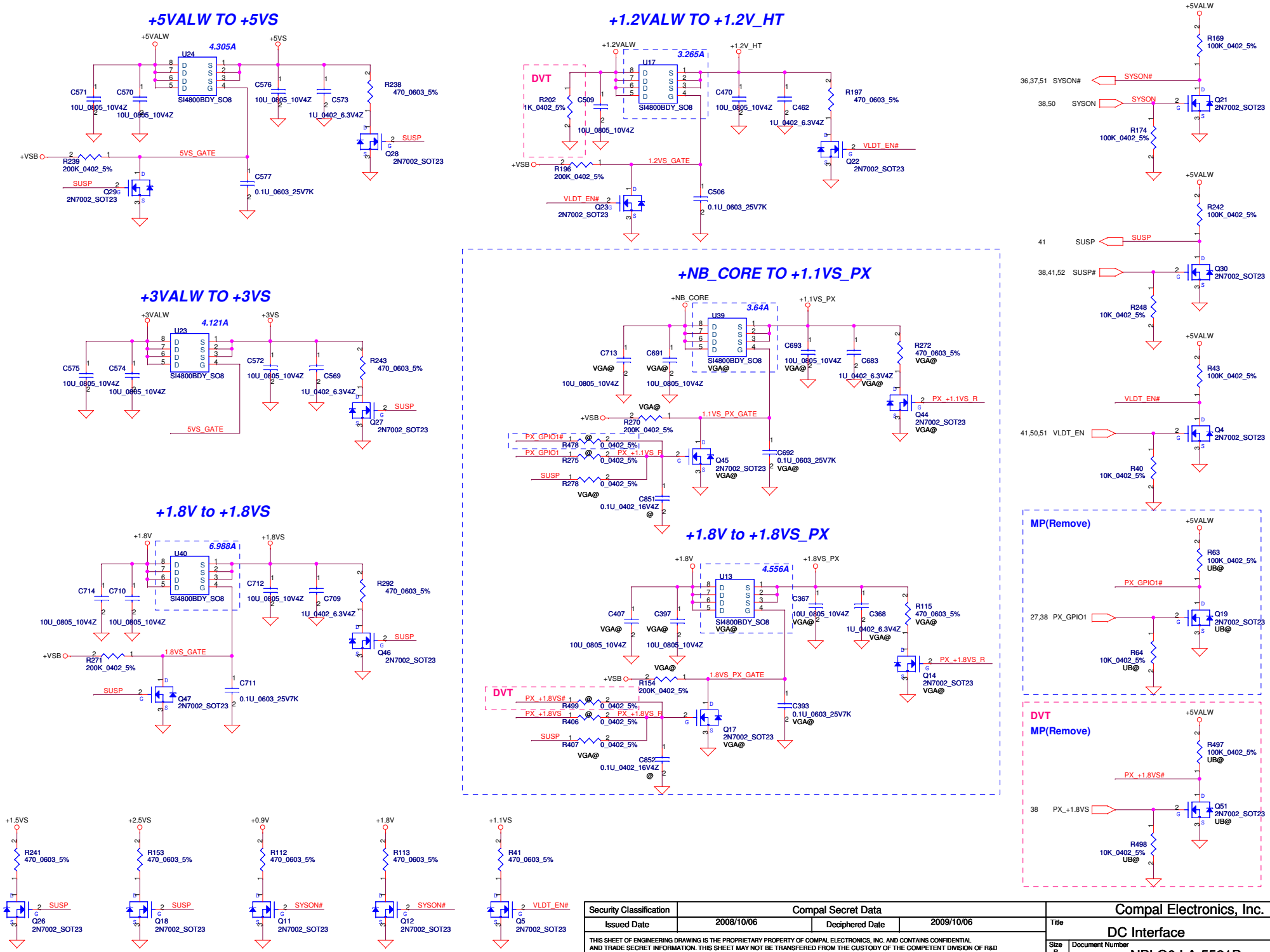
Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 44 of 58



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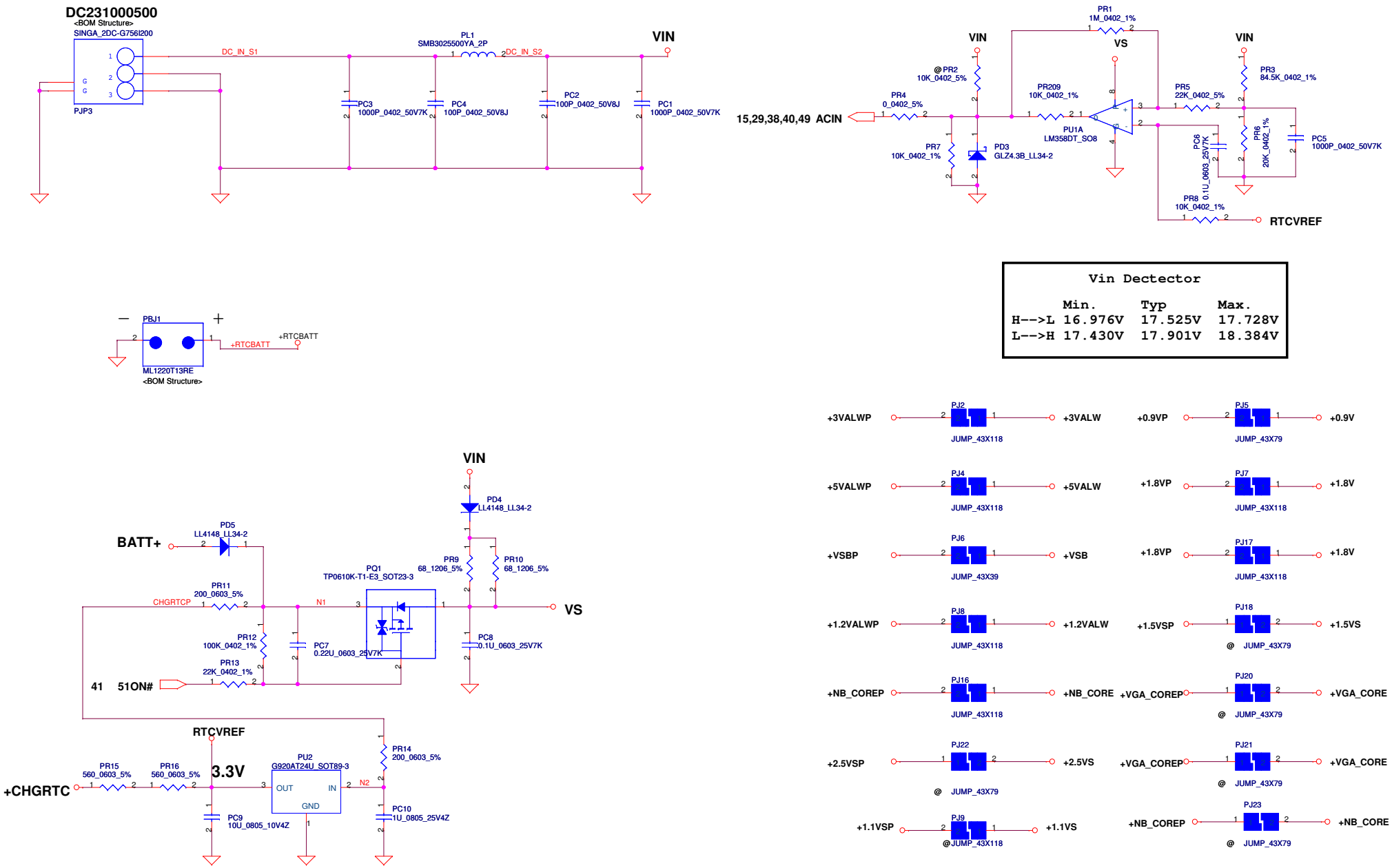
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: NBLG0 LA-5521P | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 45 of 58



Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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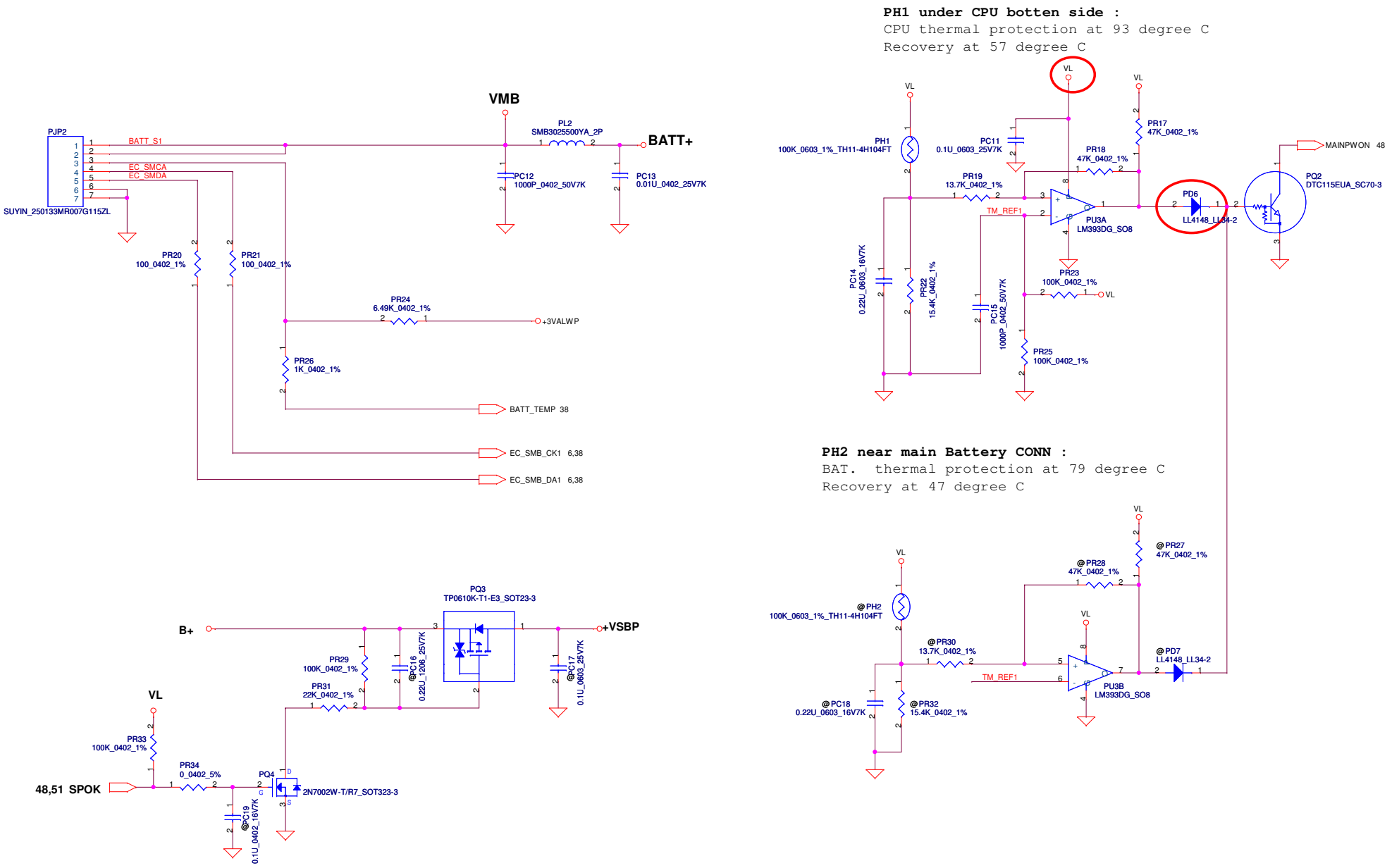
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 46 of 58



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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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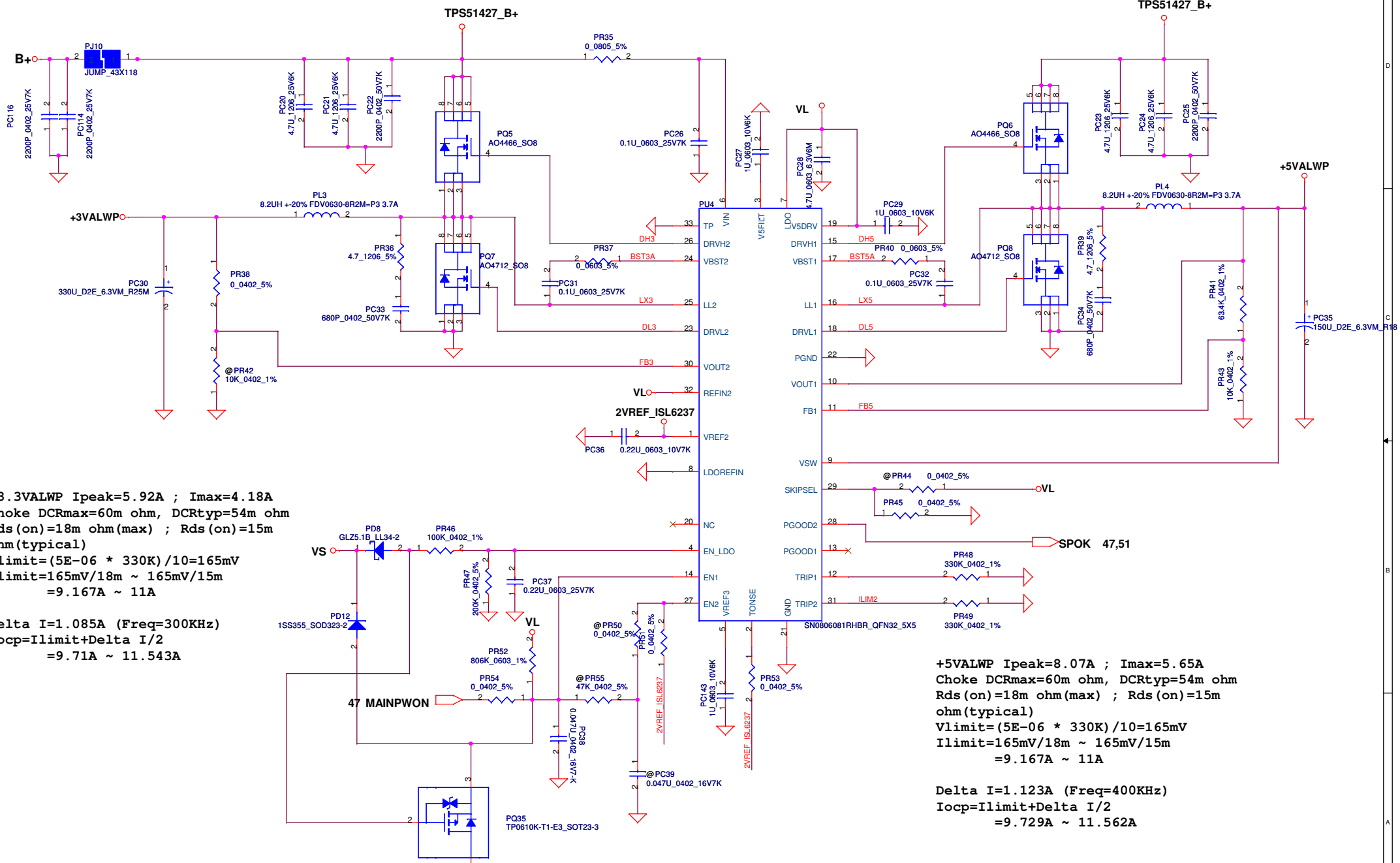
Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 47 of 58



+3.3VALWP Ipeak=5.92A ; Imax=4.18A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A

Delta I=1.085A (Freq=300KHz)
Iocp=Ilimit+Delta I/2
=9.71A ~ 11.543A

+5VALWP Ipeak=8.07A ; Imax=5.65A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A

Delta I=1.123A (Freq=400KHz)
Iocp=Ilimit+Delta I/2
=9.729A ~ 11.562A

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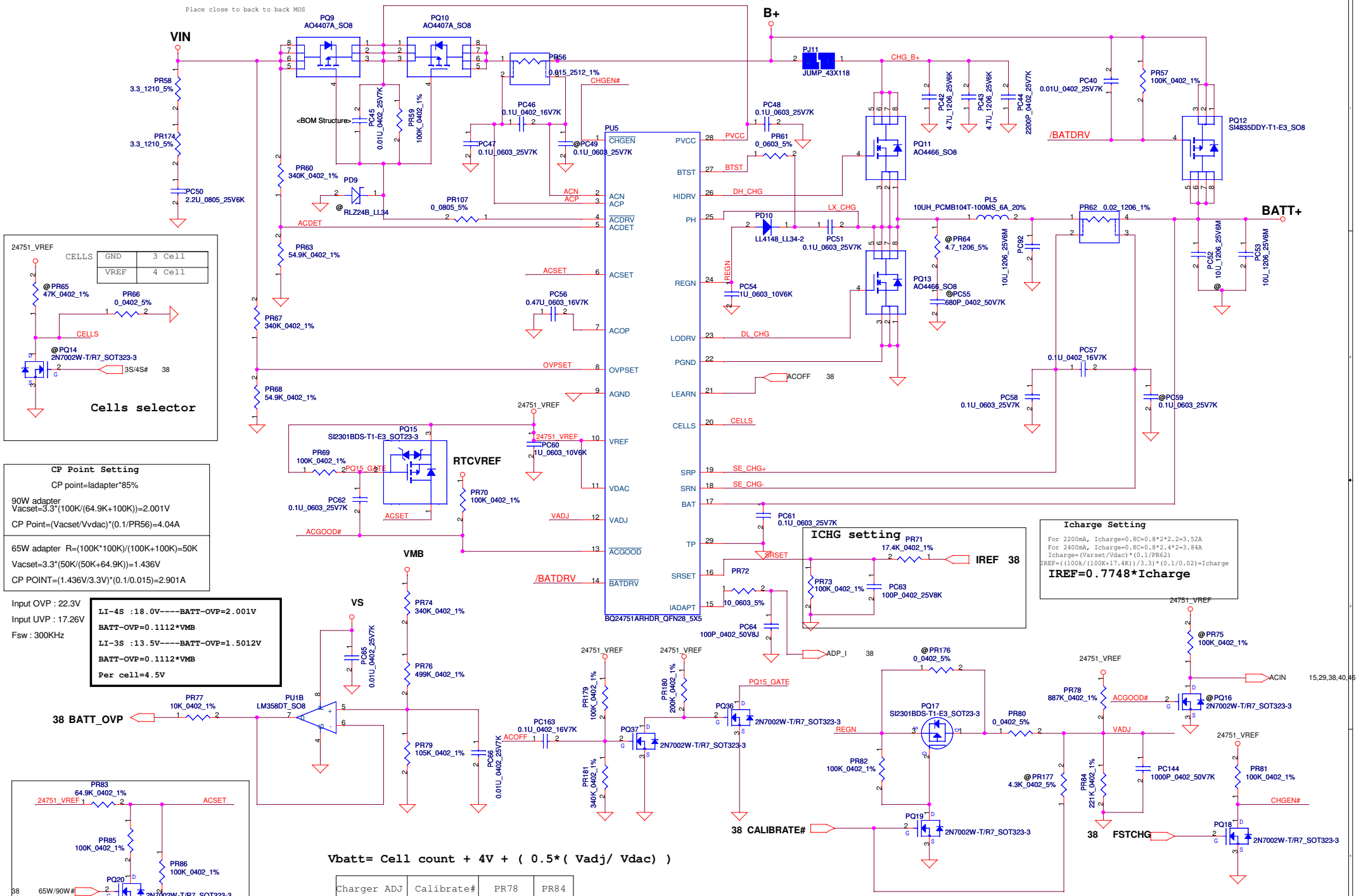
Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 48 of 58



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V(1.32)	H	@	@

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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NBLG0 | Rev: 0.1

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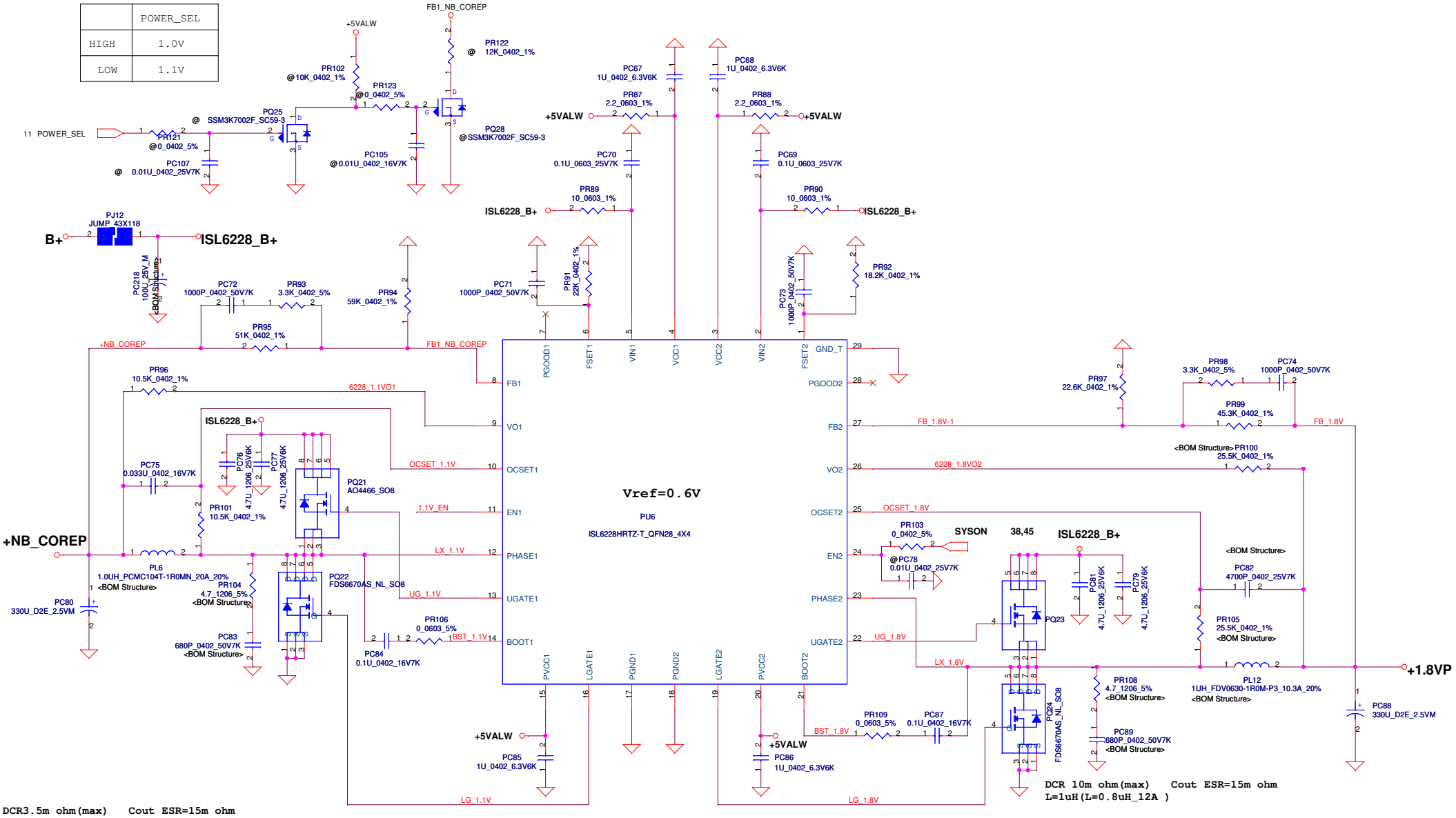
	POWER_SEL
HIGH	1.0V
LOW	1.1V



DCR3.5 ohm(max) Cout ESR=15m ohm

NB_CORE (1.1VSP) OCP Seting
Fsw=1/1.5E-10*22k =303K
Vo=Vref*((PR95+PR94)/PR94)
Ipeak=17.53A, Imax=12.27A
Iocp=17.53*1.2=21.04A
Delta I=3.838A
Iocp*DCR=(Rocset*9.5uA)=(21.04+1.92)*3.5m; Roset=8.44K
now chose Roset=10.5K
Csen=L/(DCR*Roset)=0.9uH/(3.5m*8.44k); Csen=0.031uF
now chose Csen=0.033uF
Iocp_min=(10.5K*9.5uA)/(3.5m ohm*1.3) =21.92A
Iocp_max=(10.5*10.5uA/(3.5m ohm)=28.86A

DCR 10m ohm(max) Cout ESR=15m ohm
L=1uH(L=0.8uH_12A)

1.8VP Ipeak=15.51A, Imax=10.86A
Fsw=1/1.5E-10*18.2k =366K
Vo=Vref*((PR97+PR99)/PR97)
Ipeak=15.51A, Imax=10.86A
Iocp=15.51*1.2=18.61A
Delta I=5.565A
Iocp*DCR=(Rocset*9.5uA)=(18.61+2.7825)*10m; Roset=22.5K
now chose Roset=25.5K
Csen=L/(DCR*Roset)=0.8uH/(10m*22.5k); Csen=3.56nF
now chose Csen=3300pF
Iocp_min=(25.5K*9.5uA)/(10m ohm*1.3) =18.63A
Iocp_max=(25.5*10.5uA/(10m ohm)=26.78A

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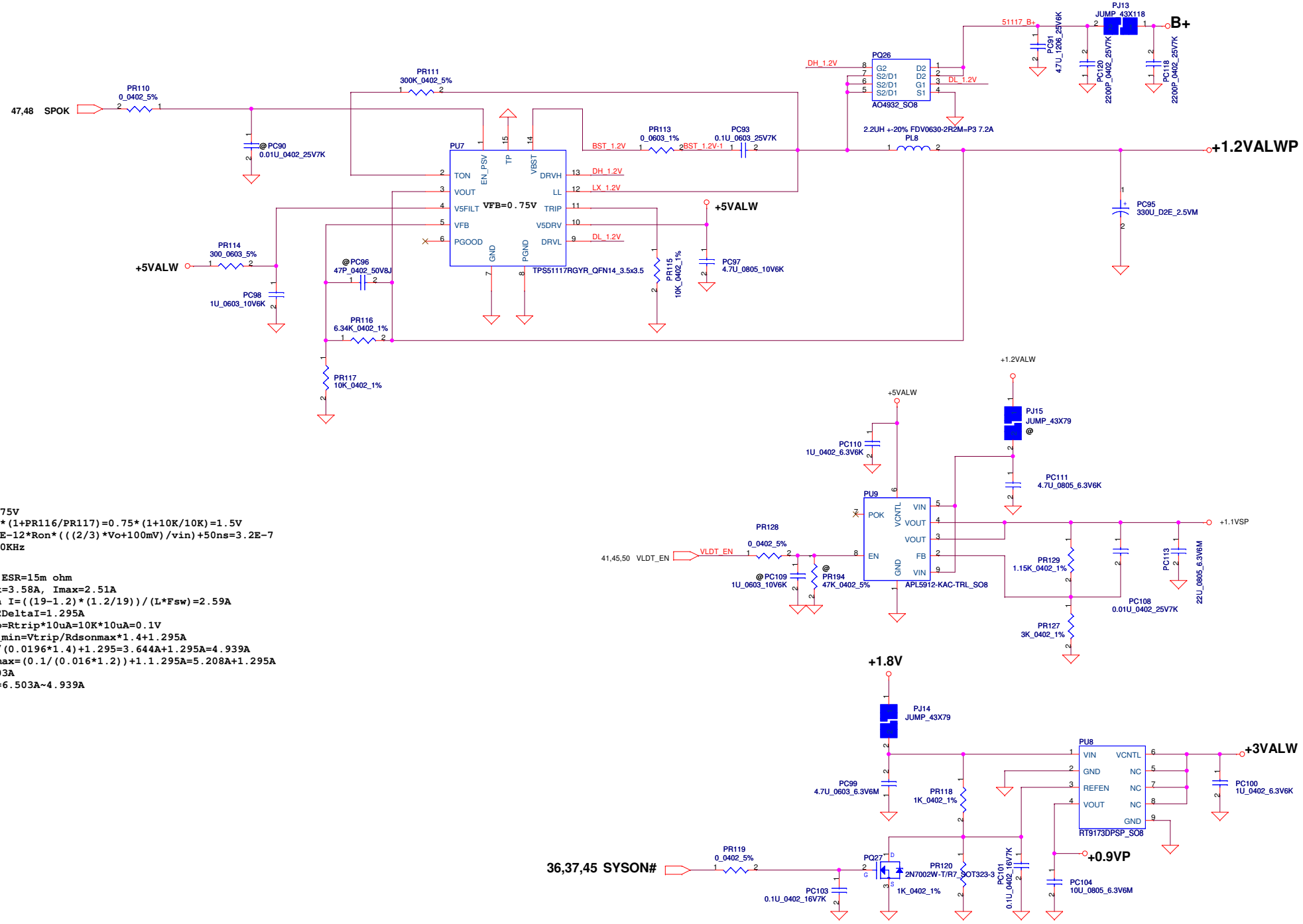
Compal Electronics, Inc.

Title: 1.8VP / 1.1VSP

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 50 of 58




```
VFB=0.75V
Vo=VFB*(1+PR116/PR117)=0.75*(1+10K/10K)=1.5V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/vin)+50ns=3.2E-7
Fsw=200KHz

 Cout ESR=15m ohm
 Ipeak=3.58A, Imax=2.51A
 Delta I=((19-1.2)*(1.2/19))/(L*Fsw)=2.59A
 =>1/2DeltaI=1.295A
 Vtrip=Rtrip*10uA=10K*10uA=0.1V
 Iocp_min=Vtrip/Rdsonmax*1.4+1.295A
 =0.1/(0.0196*1.4)+1.295=3.644A+1.295A=4.939A
 Iocpmax=(0.1/(0.016*1.2))+1.1.295A=5.208A+1.295A
 =6.503A
 Iocp=6.503A~4.939A
```

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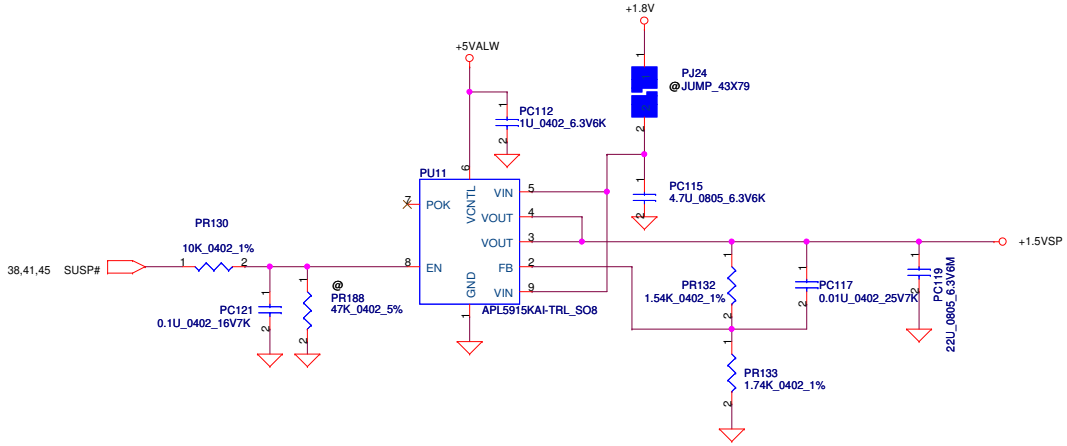
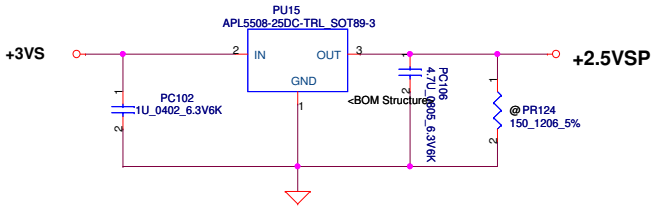
Compal Electronics, Inc.

Title: +1.2VALWP/+0.9VP/1.1VSP

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 51 of 58





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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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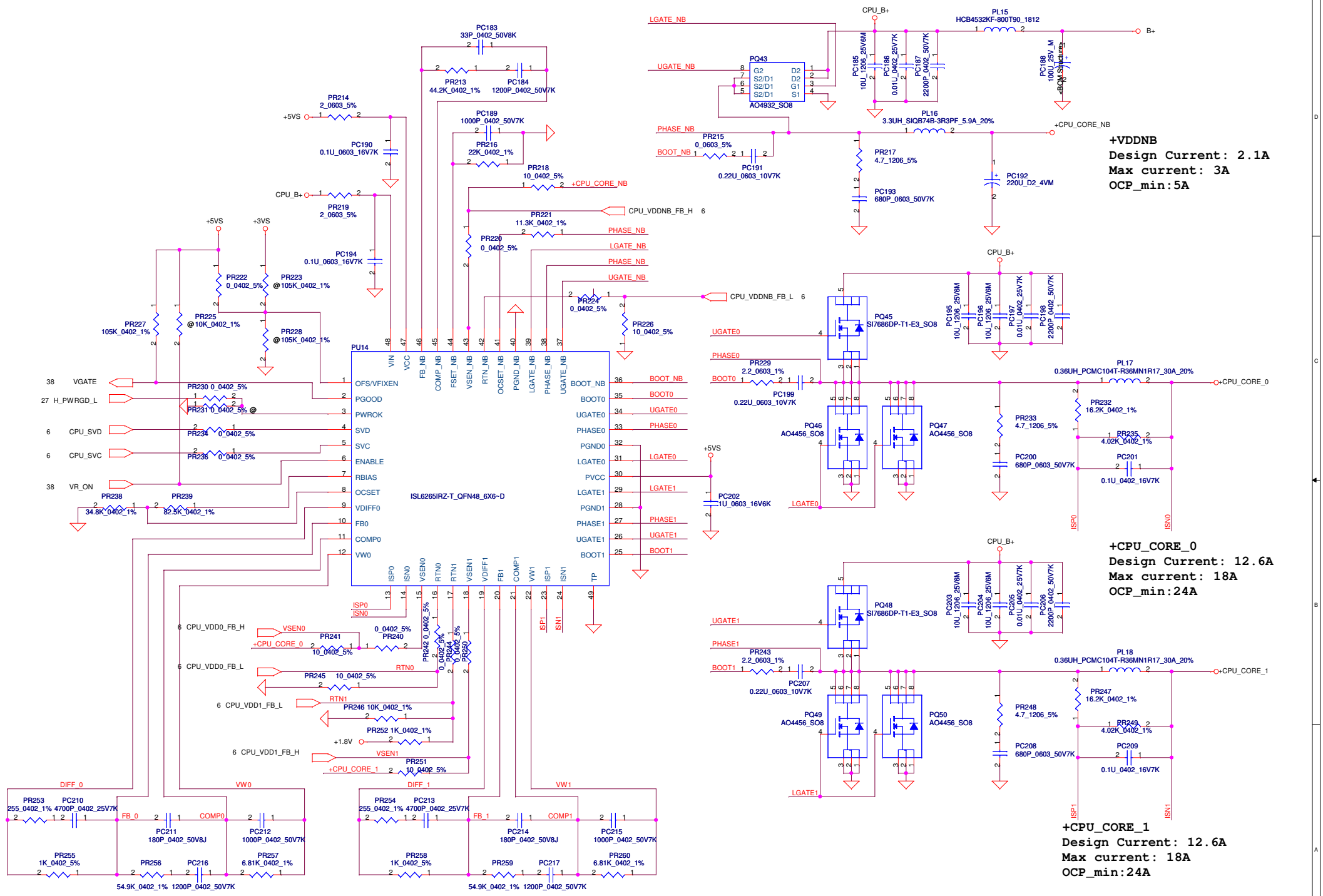
Compal Electronics, Inc.

Title: +2.5VSP/+1.5VSP

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 52 of 58



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Issued Date	2008/04/16	Deciphered Date	2009/04/16

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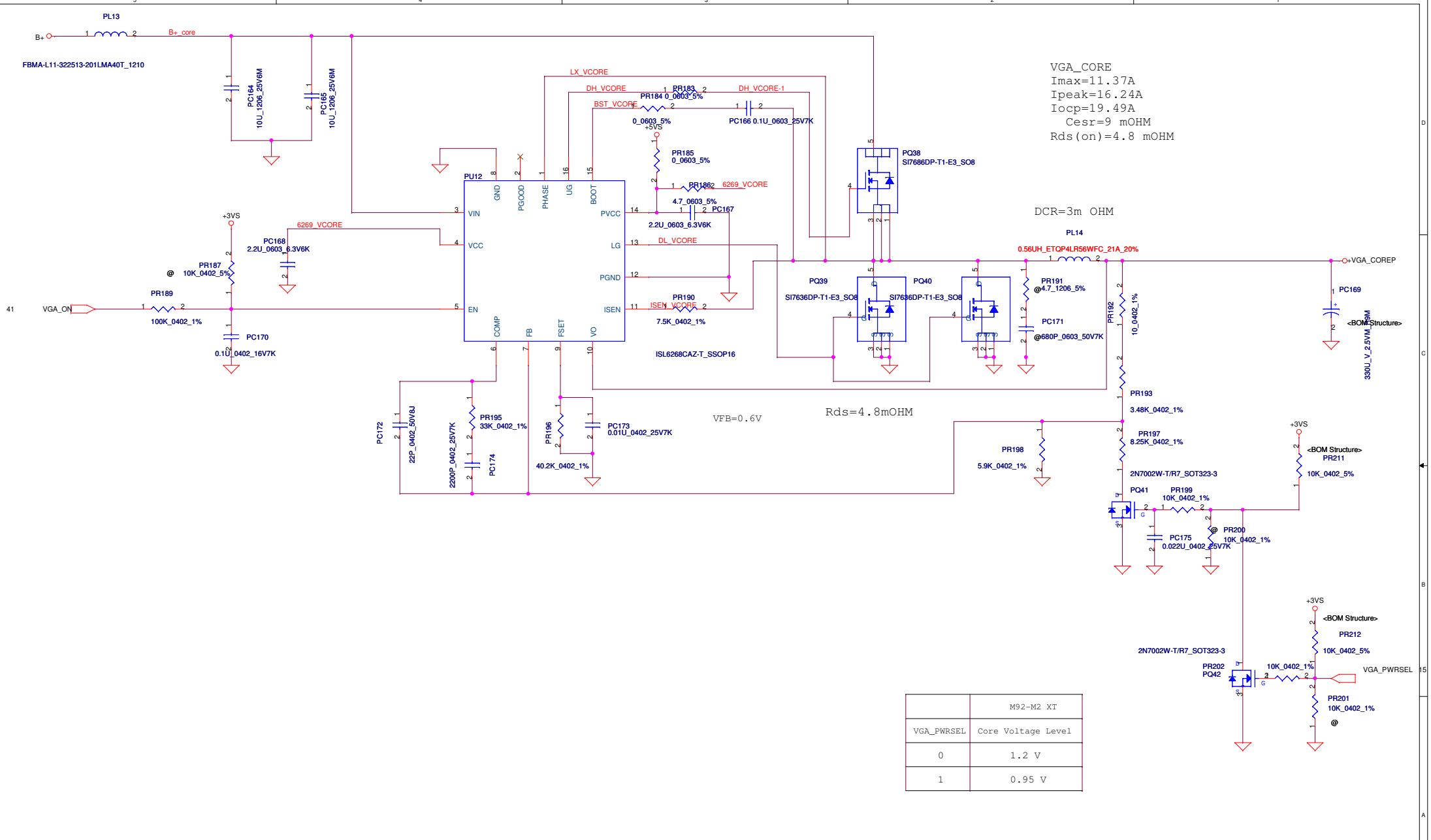
Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number: NBLG0 | Rev: 1.0

Date: Thursday, June 04, 2009 | Sheet 53 of 58



	M92-M2 XT
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V

Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2008/12/18

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Title: **VGA_CORE**

Size: Custom | Document Number: NBLG0 | Rev: 0.1

Date: Thursday, June 04, 2009 | Sheet 54 of 58

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT_KBLG0
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT_KBLG0
3	ADD snubber	EMI requestmrnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT_KBLG0
4	ADD snubber	EMI requestmrnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT_KBLG0
5	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT_KBLG0
6	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT_KBLG0
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT_KBLG0
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT_KBLG0
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT_KBLG0
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to o.1 uF	2009/01/04	DVT_KBLG0
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT_KBLG0
12	Add Diode at back to back gate pin	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	Add PD9 zener diode 24V 1/2W	2009/04/09	DVT_NBLG0
13	Add resistance at back to back gate pin	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	Add PR107 150 ohm, size is 0805	2009/04/09	DVT_NBLG0
14	change capacitance value at PVCC	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	change value from 0.1uF to 1uF	2009/04/09	DVT_NBLG0
15	reserve capacitance at source to gate of back to back	prevent spike voltage (To prevent PVCC and /ACDRV related pin EOS when ACOP, LEARN function test)	0.1	49	reserve PC45 0.01uF at source to gate of back to back	2009/04/09	DVT_NBLG0
16	reserve resistance at CPU_VDD1_FB_L	for tigris design change, and add 1.8V net at PR252 pin2	0.1	53	reserve PR252 that it value is 1K(0402,1%) at CPU_VDD1_FB_L	2009/04/09	DVT_NBLG0
17	change resistance value at CPU_VDD1_FB_L	for tigris design change	0.1	53	change PR246's value to 10K(0402,1%)	2009/04/09	DVT_NBLG0
18							
19							
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor	Reserved EC SMBUS1 due to +3VS leakege when S3 entry with SMBUS2
	P.8	Add C174/C175/C176 (0.1u_0402)	EMI request
	P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@	BOM error
	P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)	UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0
	P.11	Reserve R490(0ohm_0402)	NA
	P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@	For DIS +1.1VS power source from fixed +NB_CORE
	P.22	Remove VRAM Samsung(Q-die) & Qimonda type	Customer request
	P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@	Separately as DIS sku only & UMA sku only
	P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@	For DIS sku only
	P.24	Reserve Q52/R501/R502/R503	Reserve for UMA sku white screen flash when boot issue check
	P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)	DFX request
	P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506	NA (Just no need to modify)
	P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@	Separately as DIS sku only & UMA sku only
	P.27	Add R496 with @ & R476/R482 with @	NA
	P.28	Add R509 with VGA@ & R510 with UMA@	Reserve SKU ID for SW even SW check device ID instead currently
	P.29	Reserve C862/C863/C855/C856	Reserve eSATA function for future request
	P.37	Change JUSB1 as SB700 USB port6	Dedicated HS port on lower-left position
	P.38	Change U20 as KB926 D3 version (SA00001J580)	NA
	P.38	D41 with VGA@ & D42 with UMA@	Separately as DIS sku only & UMA sku only
	P.38	U20.85 defined as TP_LOCK _LED# feature	LED control simultaneously with Tutch-Pad locked function
	P.38	Change R194 as 8.2kohm_0402	Change board ID as 1 (PCB revision : 0.2)

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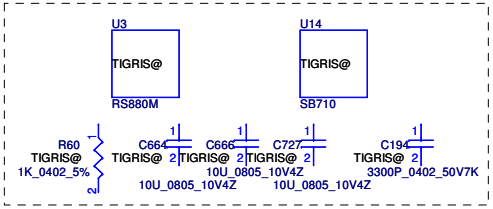
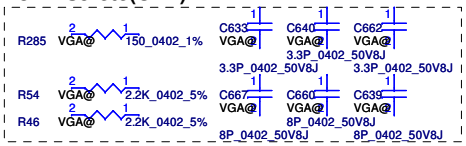
PHASE	PAGE	MODIFICATION LIST	PURPOSE
	P.39	Add R250/LED11/SW4	Add T/P lock button & T/P lock button LED
	P.45	Reserve R499 , R497/R498/Q51	NA
	P.45	Stuff R202	+1.2VALW leakege 640mv pulse when AC insertion & then might cause OVP
	P.34	C26 with @ & C11 as SE070104Z80	NA
	P.42	Stuff R446(0ohm_0805) & un-stuff U32(Audio LDO)	NA
DVT2	P.6	Remove CPU side-band(internal) temp sensor function	NA
	P.11/38	Add U49/C857/R744 (Reserve U48) & D42 with @, remove D42	NA
	P.23/34	Add R676 for CLK_48M_SD , reserve R715 / R716 for CLK_48M_LAN	NA
	P.24	Add R508(2.7K_0402) for ENVDD of UMA sku	NA
	P.28	SB700 USB port 4 for Realtek RTS5159 card reader	NA
	P.33	Add(co-layout) Realtek RTS5159 card reader	NA
	P.37	Change JSAT1 PCB footprint as TYCO_1909574-1_11P-T	NA
	P.38	R194 change as 18K_0402	Change board ID as 2 (PCB revision : 0.3)
	P.40	LED1 / 5 / 8 / 9 /10 PCB footprint change as LED_HT-297DQ-GQ_4P	For DFX
	P.44	Add H28 & H29	For thermal
PVT	P.11	Add R511 with @ & U50	For LCD white screen flash when coldboot issue
	P.11	Add C874 / C875 (1u_0402)	For CRT(acer lab) flicker
	P.11/38	C857 / U49 with @ , R744 / D42 with UMA@	NA
	P.42	Add L94(SM010027780) close to audio codec	For EMI
	P.40	Modify LED 1 / 5 / 8 from dual Blue/Amber LED as single Blue LED	Follow acer spec
	P.39/40	Modify R12/R13/R17/R16 (300->220ohm) , modify R1/R2/R3 (1.2K->866ohm) , modify R10 (300->715ohm) , modify R245/R247 (4.99K->750ohm) , modify R244/R246 (4.99K->866ohm) , modify R250 (1.2K->5.1K)	For LED brightness test
	P.23	Change LAN_CLKREQ# from U18.51 to U18.24 output	NA
	NA	Change test pad (execpt T8/T13/T15/T17/T18/T24/T28 /T29/T33/T45/T46/T48/T50/T56/T57/T12) from TPC12 to TPC24	
	P.36	Reserve Q55 / Q56 / R745 / R746 / R747 / C876 to turn off power of finger printer	
	P.38	R194 change as 18K_0402 for change board ID as 3 (PCB revision : 0.4)	
MP		Search for MP font	

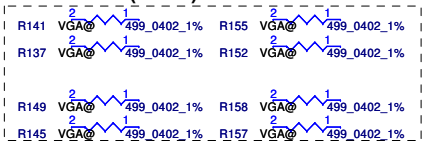
For TIGRIS



For Discrete(CRT)



For Discrete(HDMI)



PCB

PCB 047 LA-5521P REV0 M/B

LA5521MB Rev0 : DA80000FI00

LA5521MB Rev1 : DA80000FI10

LA5521MB with Sub/B Rev1:TBD

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PHASE	PAGE	MODIFICATION LIST	PURPOSE
NBLG0_DVT	P.11	Reserve R515 / R516 / R517 & add R514	Reserve for UMA(RS880M) LCD varibright feature
	P.14	Change dual diode as single diode x 2	NA
	P.14	Reserve U37 / C859	Reserve for AMD cross display feature
	P.15	Reserve R518 / R513	Reserve for DIS(M92) LCD varibright feature
	P.18	Add R512 / Q57 / Q58 / R219 / C858 & reserve L64	For DIS(M92) backbias power saving feature
	P.22	Reserve R529 / R530	NA
	P.25	Add R522 / R524 & reserve R523 / R525 / R526 / R527 / R528 / D37 / Q20	NA
	P.29 P.34	Change Y2 / Y3 part from SJ125P0M200(25MHz_20PF_+/-25PPM , 8.0x 4.5x1.5mm) as SJ100003300(25MHz_20PF_+/-30PPM , 5.0x3.2x1.2mm)	For cost down
	P.42	Reserve R519 / D36 / C203	NA
	P.31	R367 with @	RS880M internal PU already
	P.18	M92 decoupling power cap with @ (C355,C389,C237,C333,C202,C312, C313,C263,C264,C265,C343,C286,C247,C337,C353,C267)	NA

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