

Compal Confidential

KAV10 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

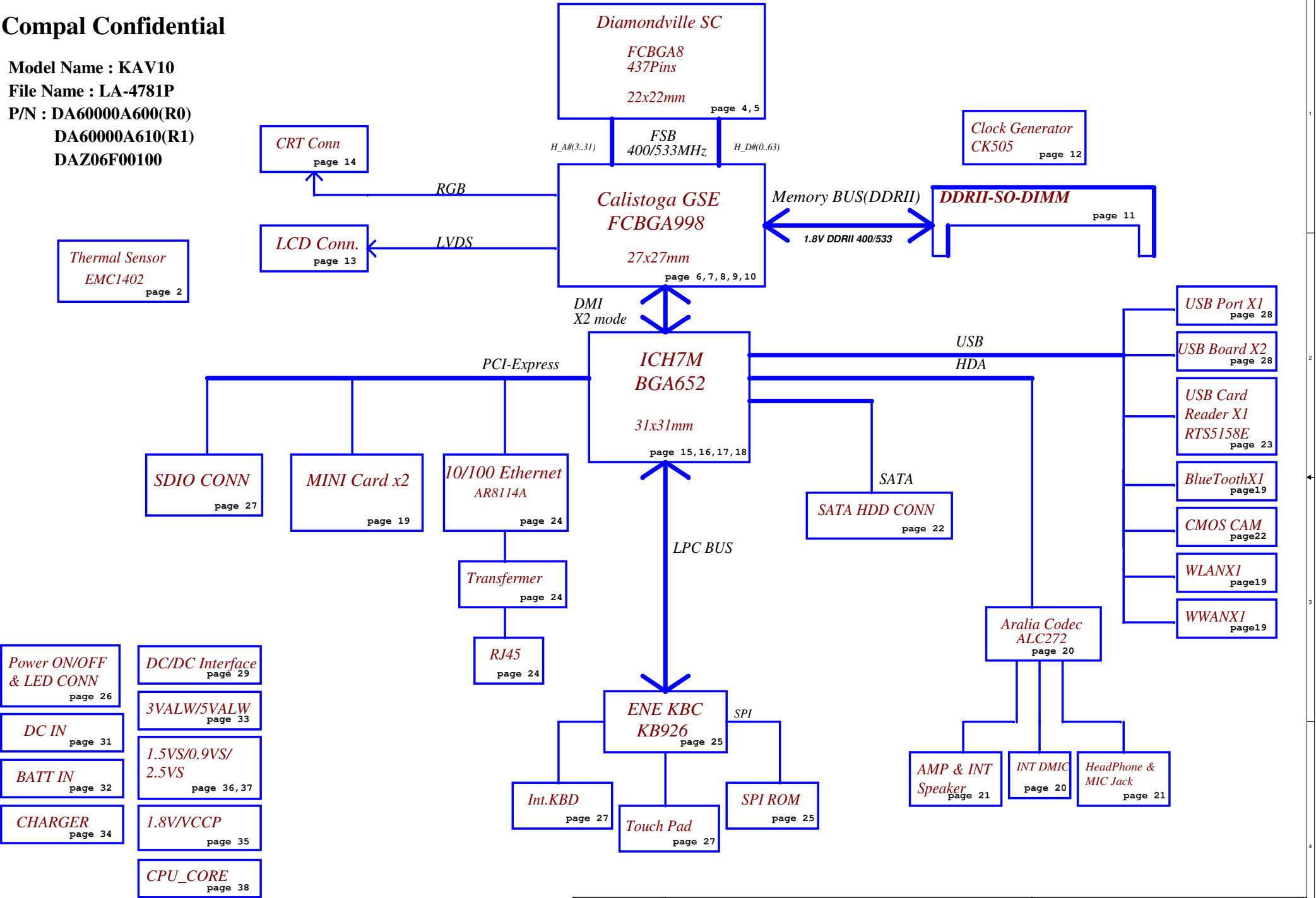
2008-12-30

REV: 1.0

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Model Name : KAV10
File Name : LA-4781P
P/N : DA60000A600(R0)
DA60000A610(R1)
DAZ06F00100



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

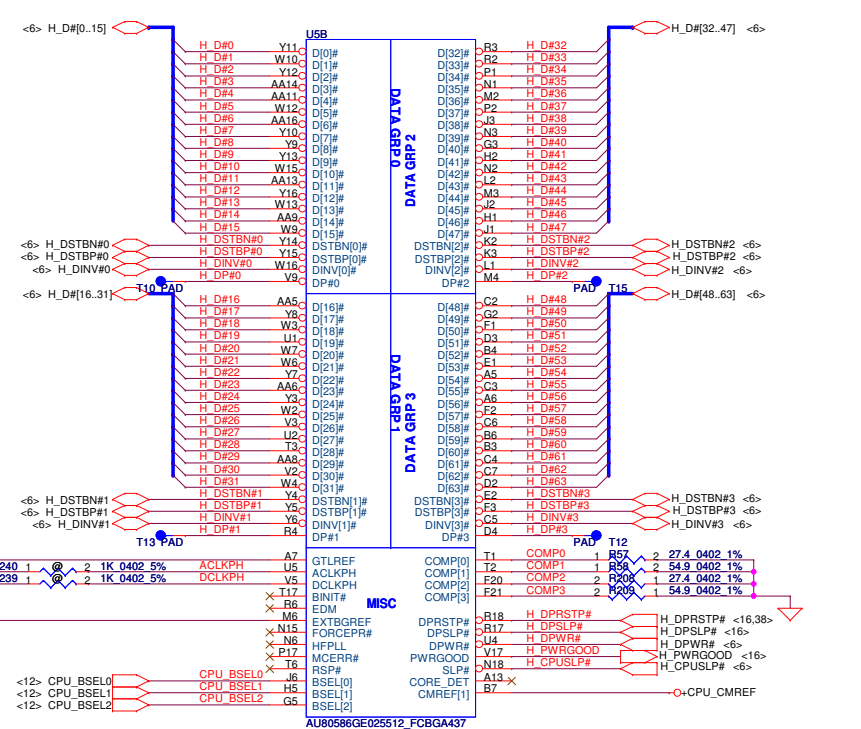
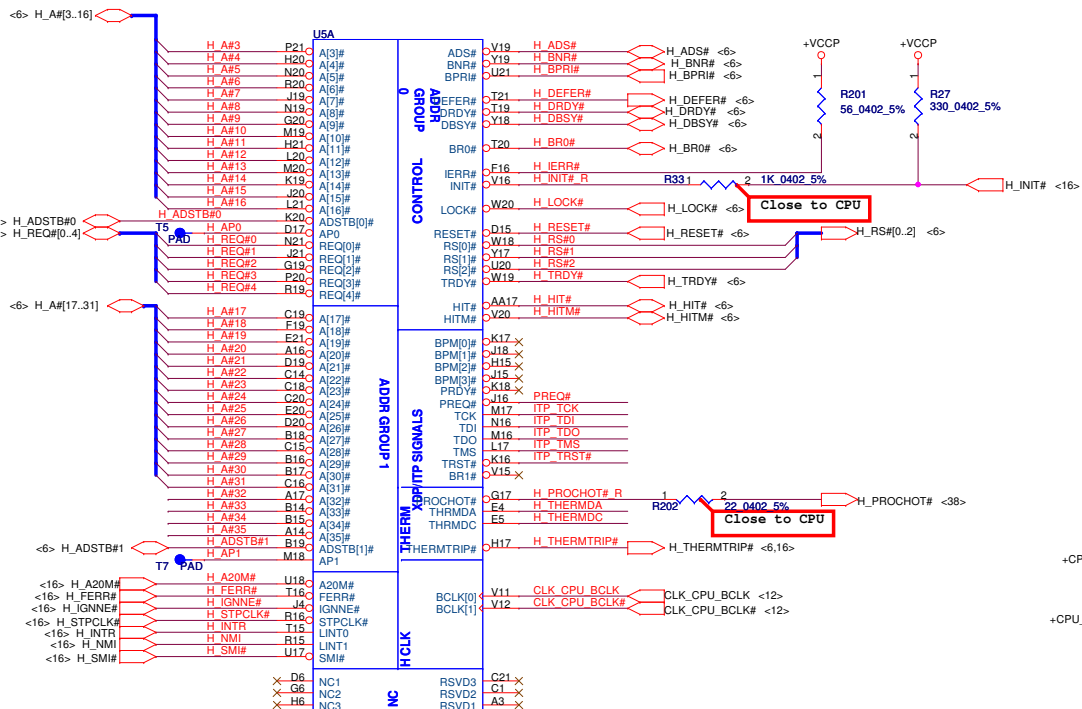
Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

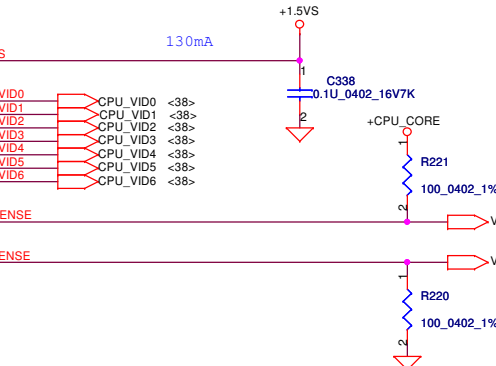
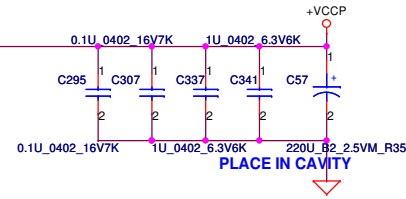
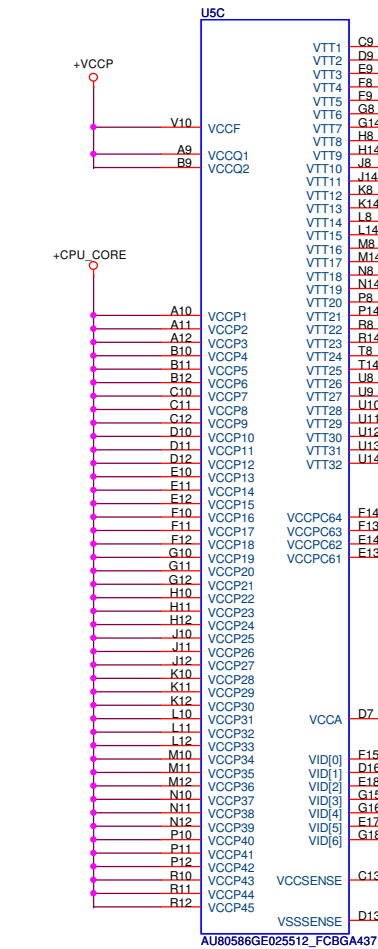
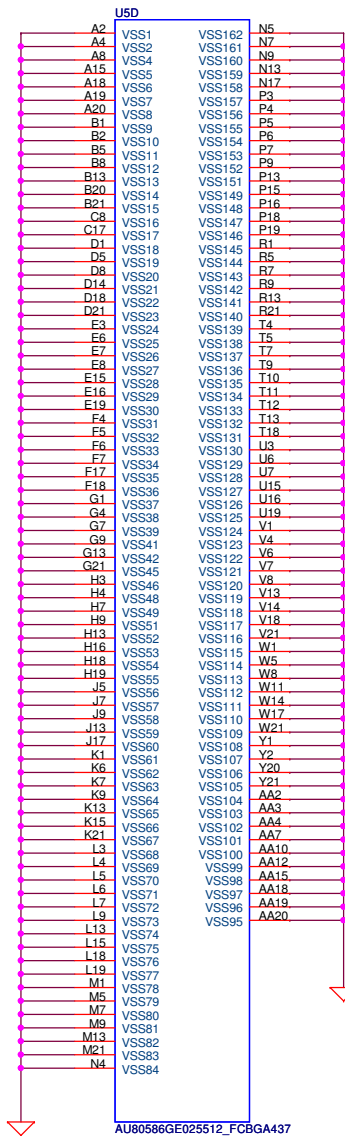
EC SM Bus2 address

Device	Address
EMC1402	1001 100X b

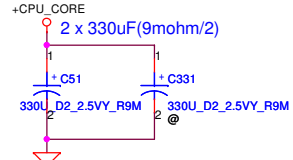
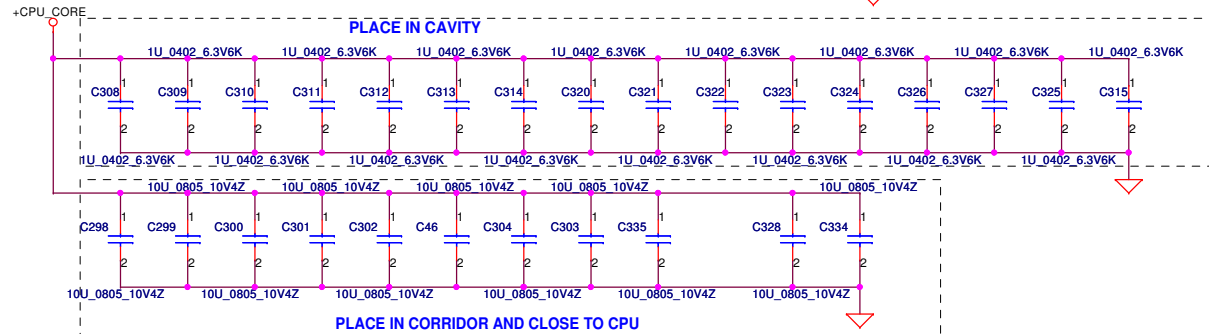
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

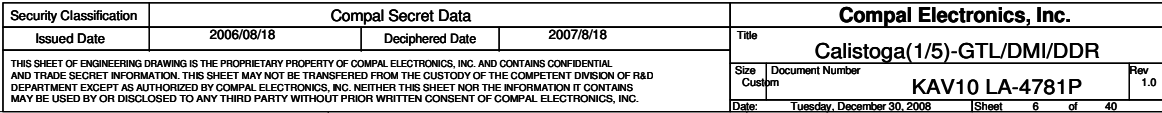


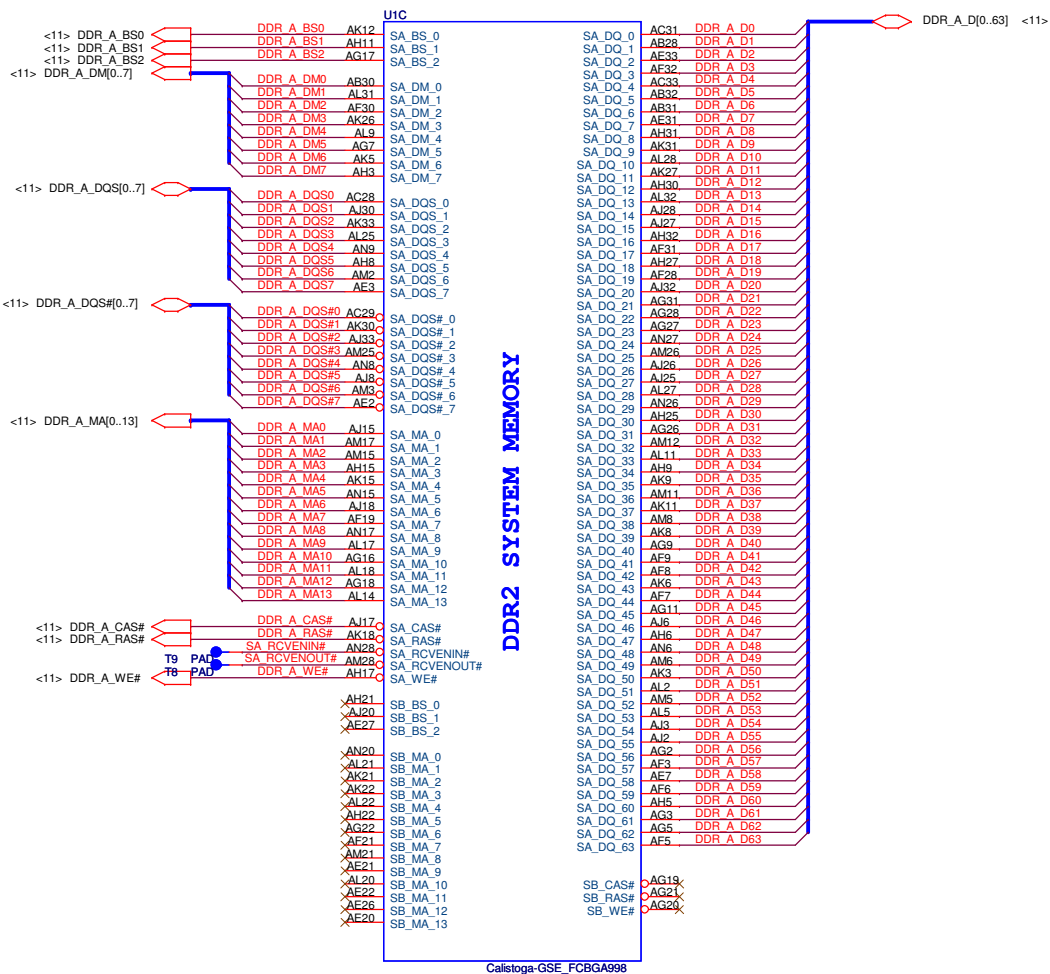


Length match within 25 mils
The trace space 7 mils,
 $Z_0=27.4\text{ohm}$

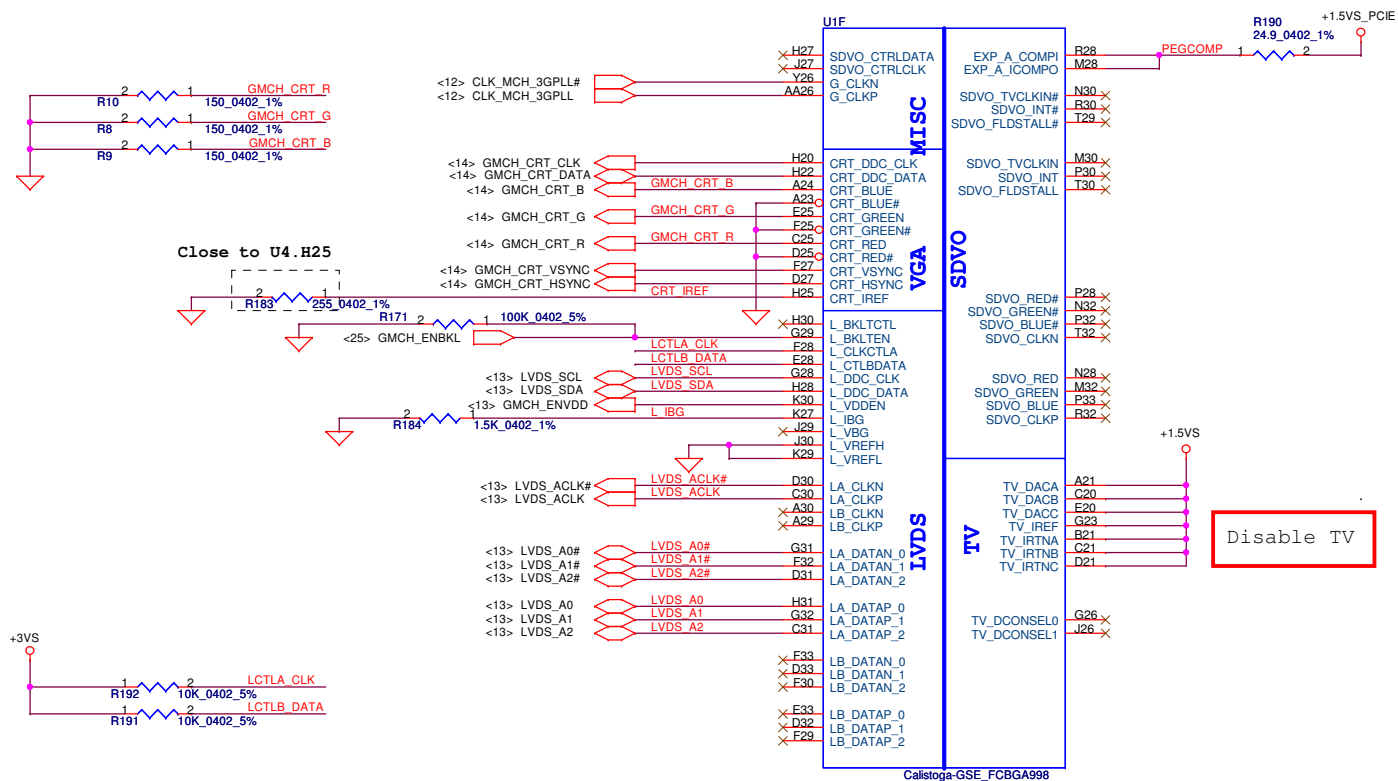


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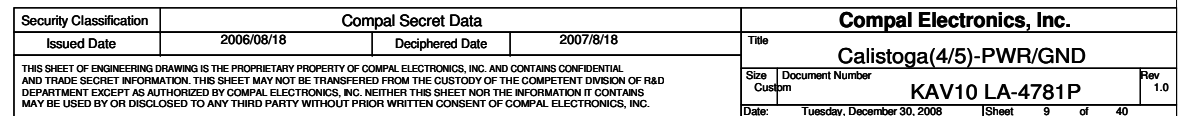




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				Custom			
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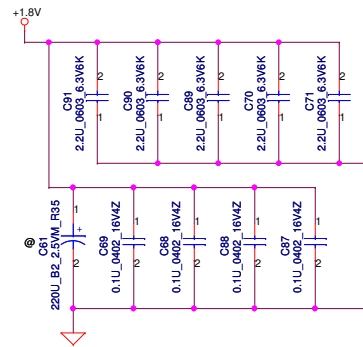


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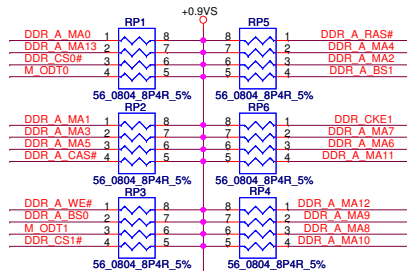
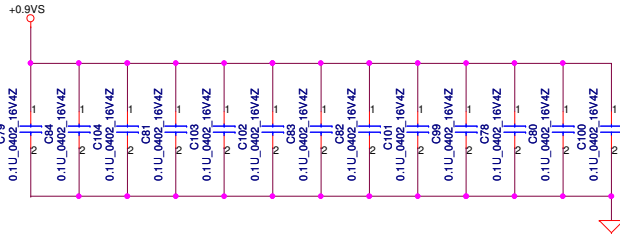


<7> DDR_A_DQS#[0..7]
 <7> DDR_A_D[0..63]
 <7> DDR_A_DM[0..7]
 <7> DDR_A_DQS[0..7]
 <7> DDR_A_MA[0..13]

Layout Note:
Place near JDIM1



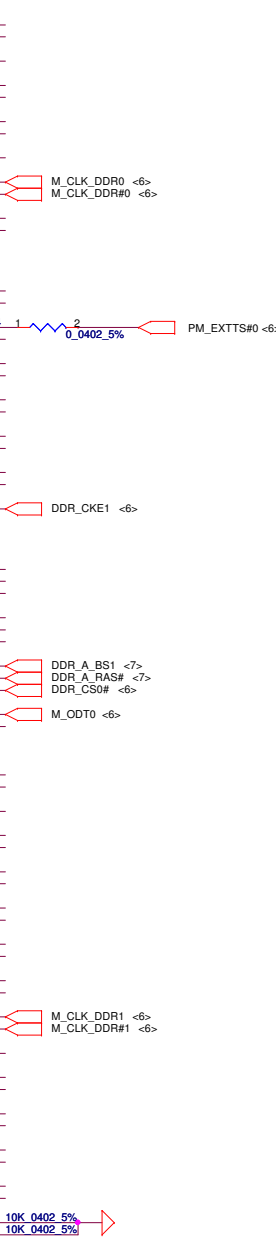
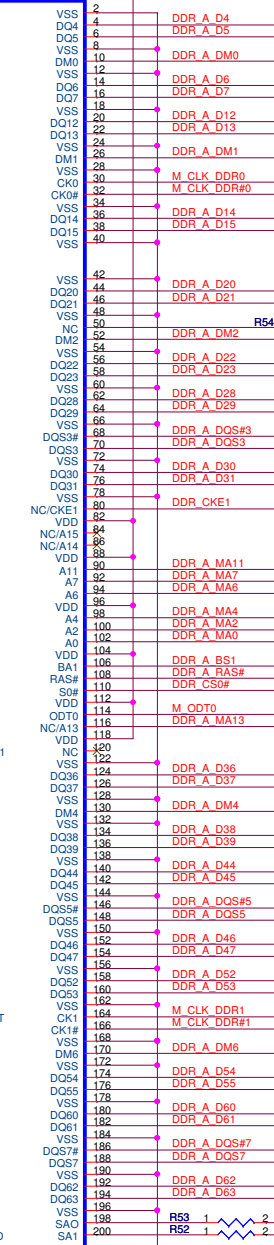
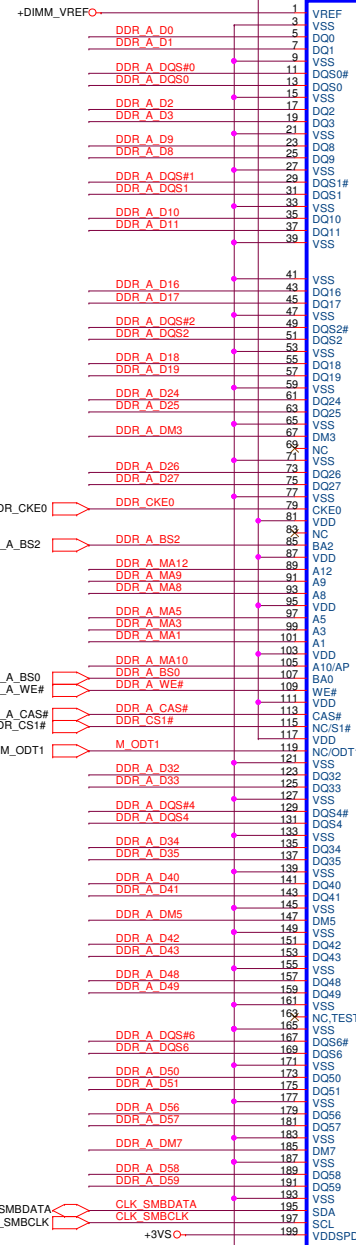
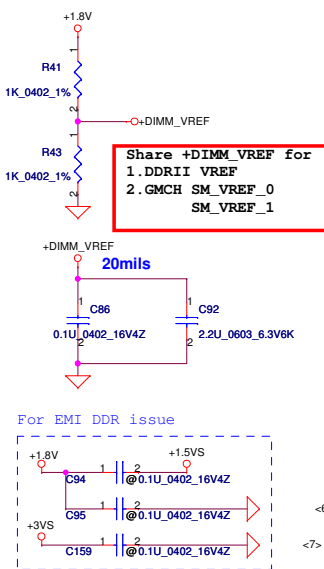
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely DIMMA, all trace length < 750 mil



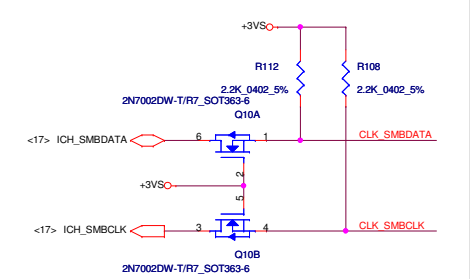
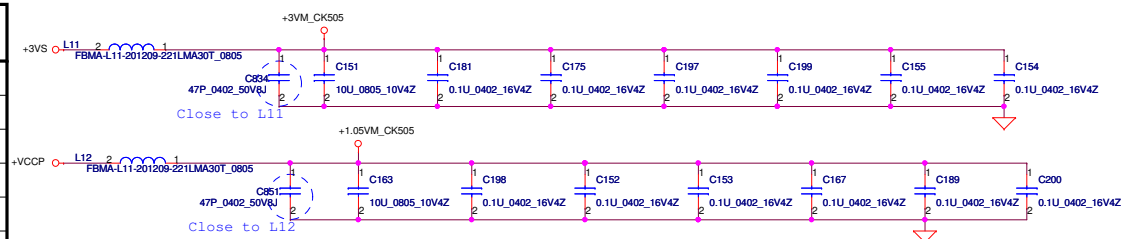
Layout Note:
Place these resistor closely DIMMA, all trace length Max=1.3"



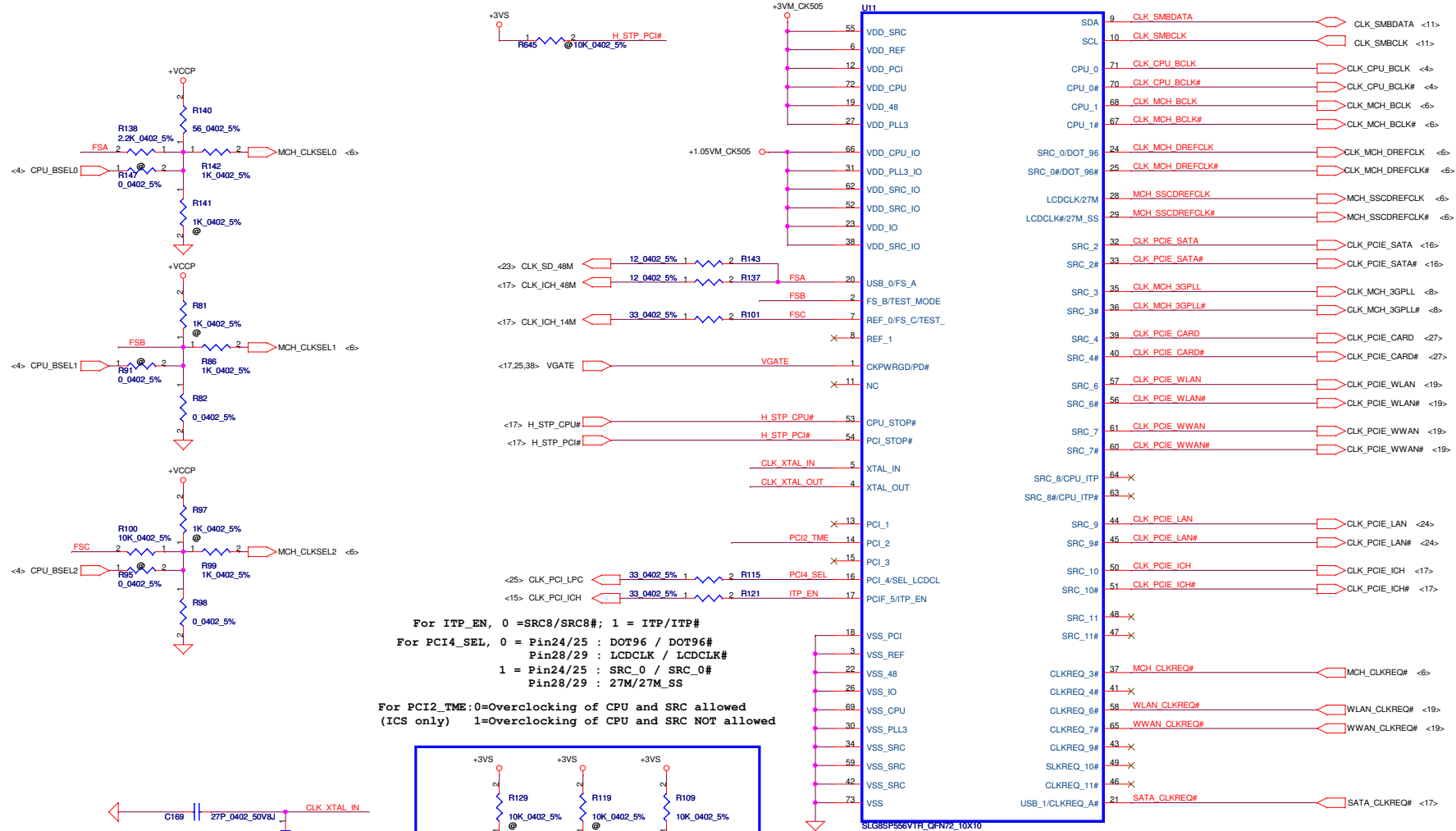
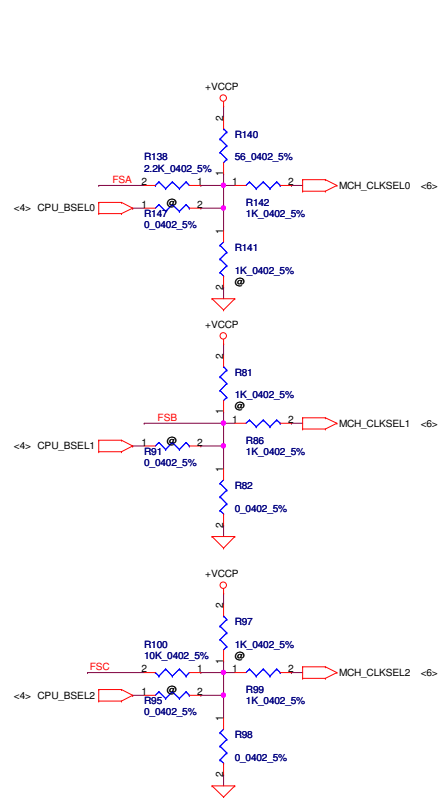
DIMMA

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)



Routing the trace at least 10mil

SRC PORT LIST

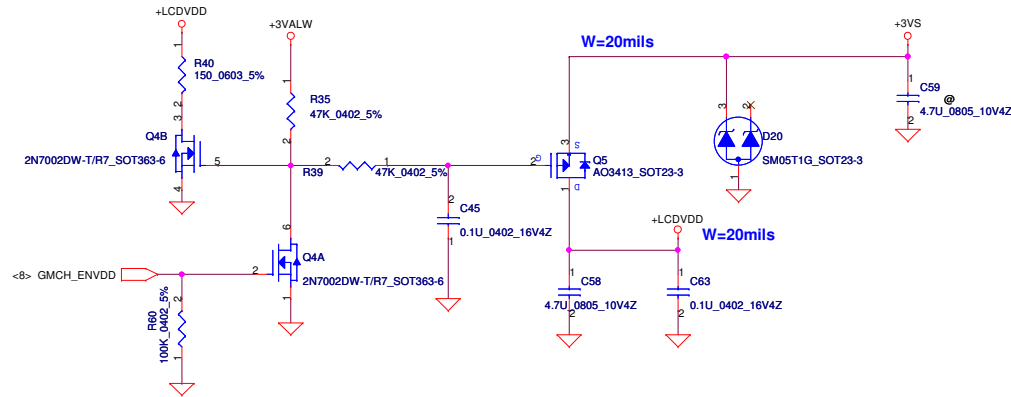
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	SATA_HDD
SRC3	MCH_3GPLL
SRC4	PCIE_CARDREADER
SRC6	PCIE_WLAN
SRC7	PCIE_WWAN
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	

REQ PORT LIST

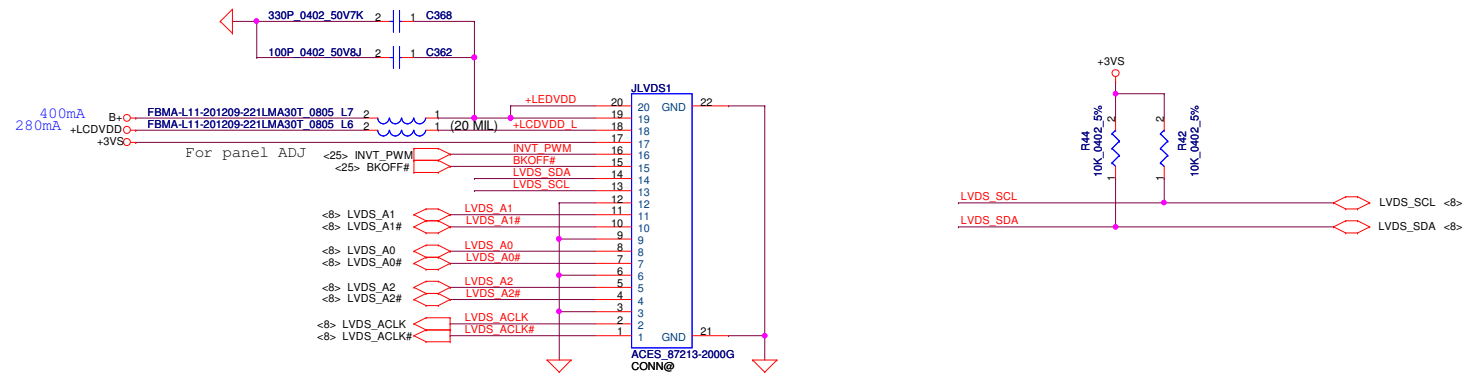
PORT	DEVICE
REQ_3#	MCH_3GPLL
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WWAN
REQ_9#	
REQ_10#	
REQ_11#	
REQ_A#	SATA

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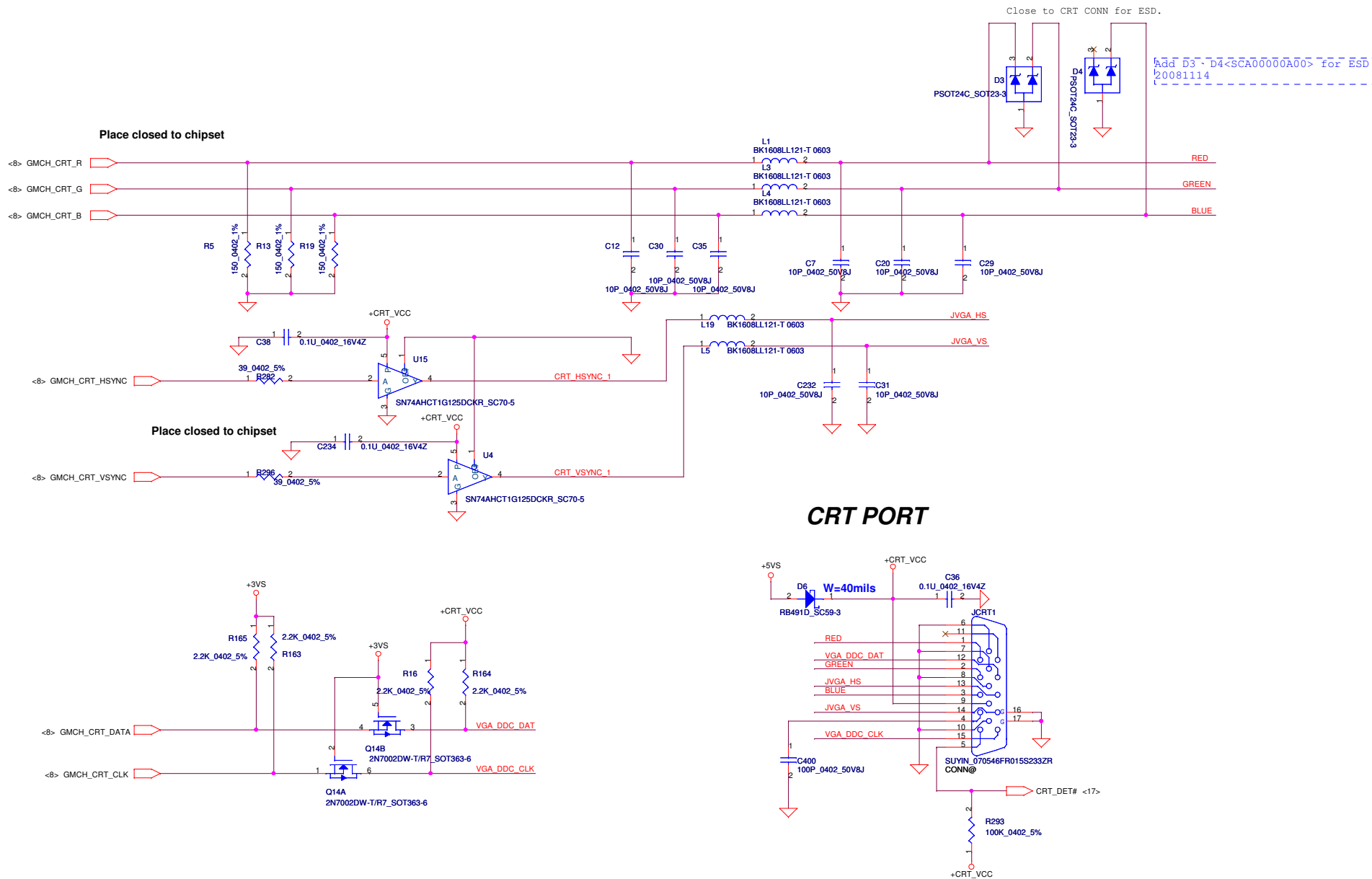
LCD POWER CIRCUIT



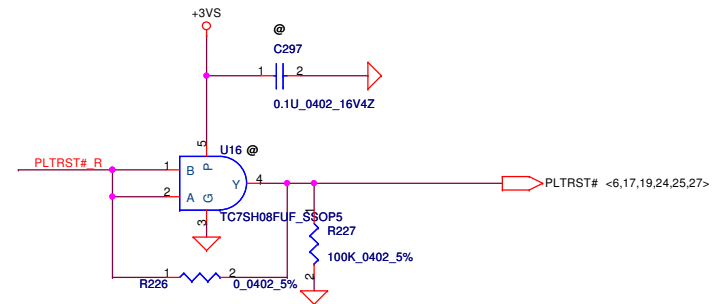
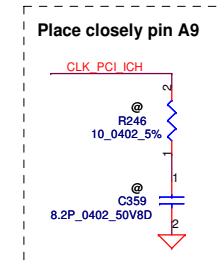
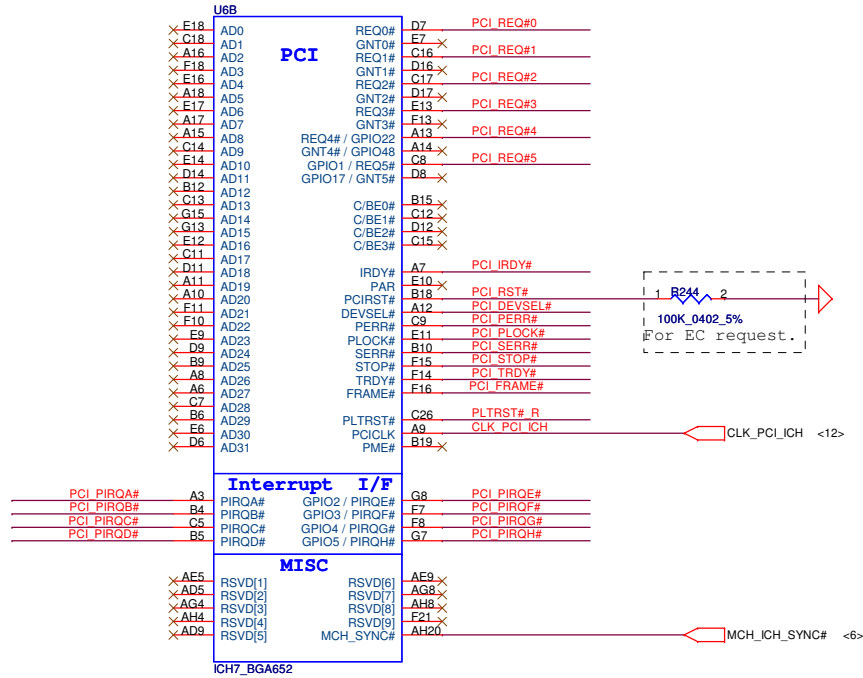
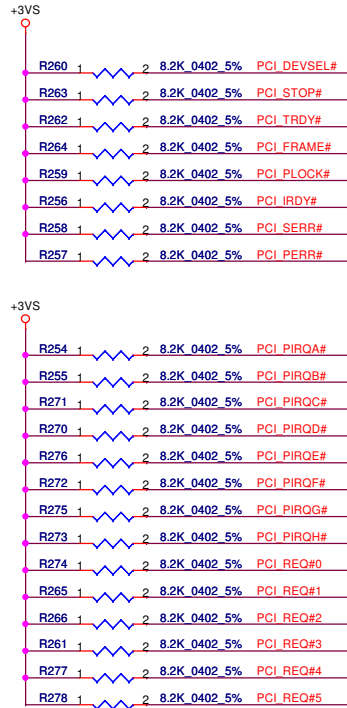
LCD/PANEL BD. Conn.



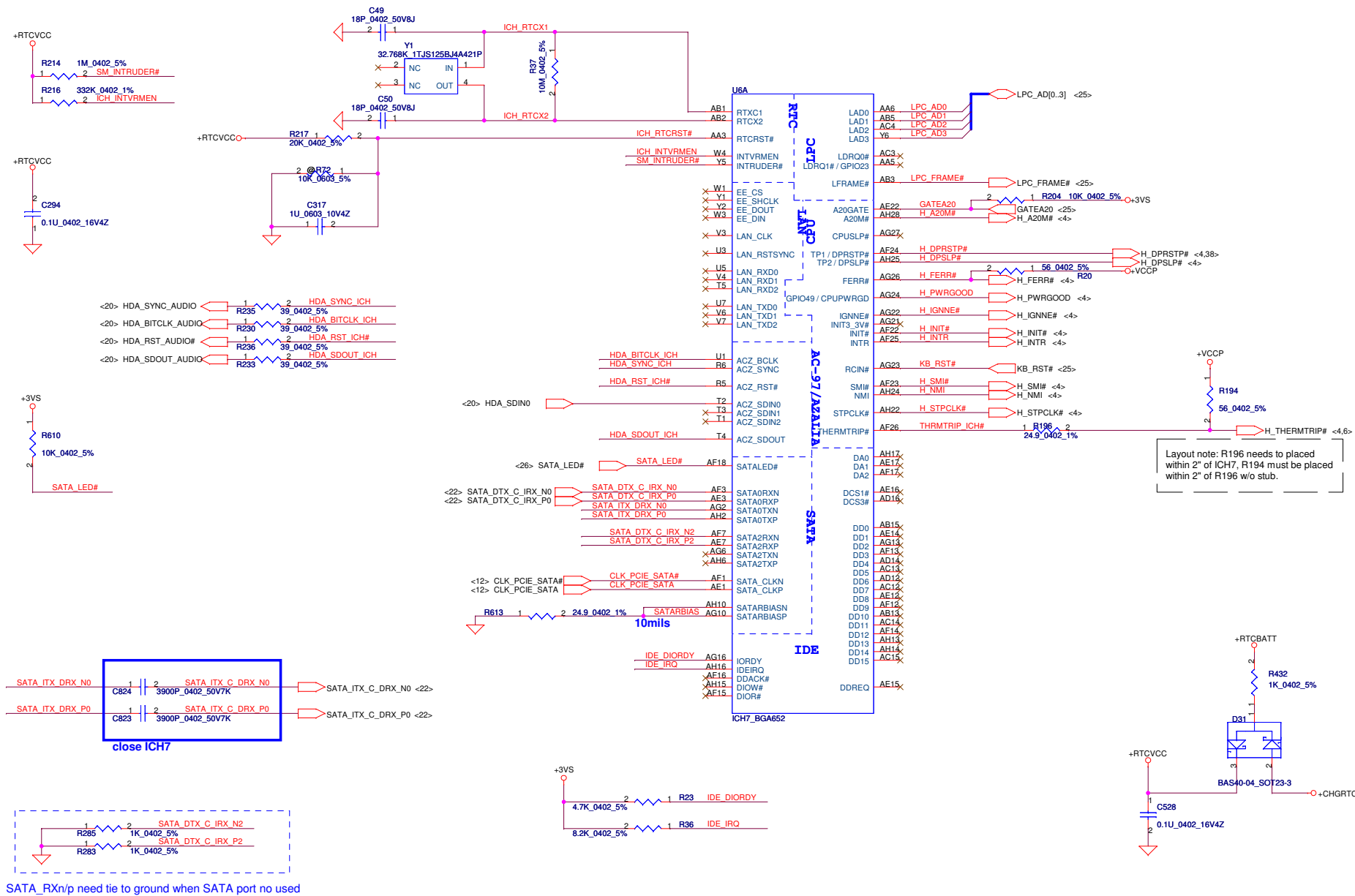
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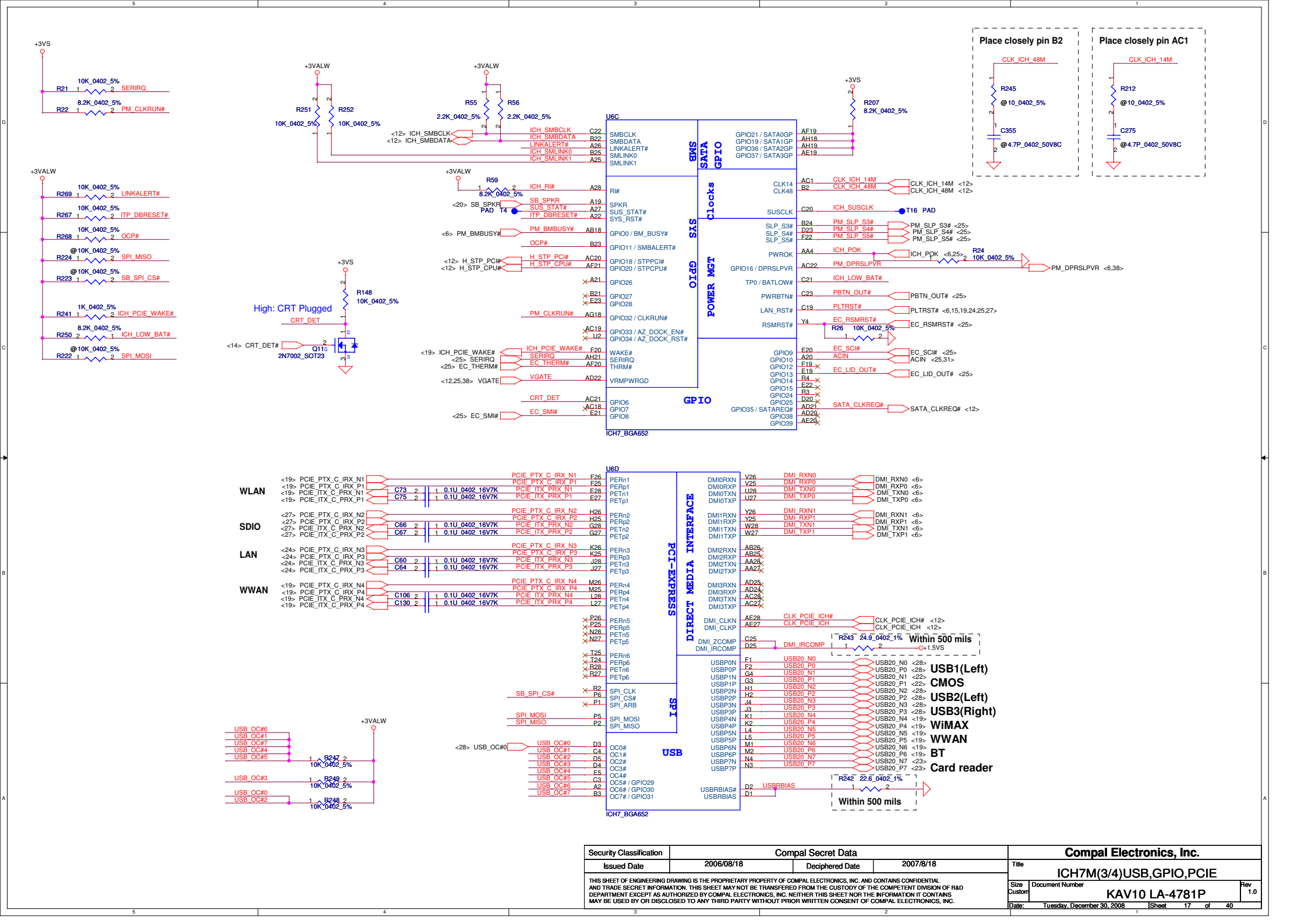
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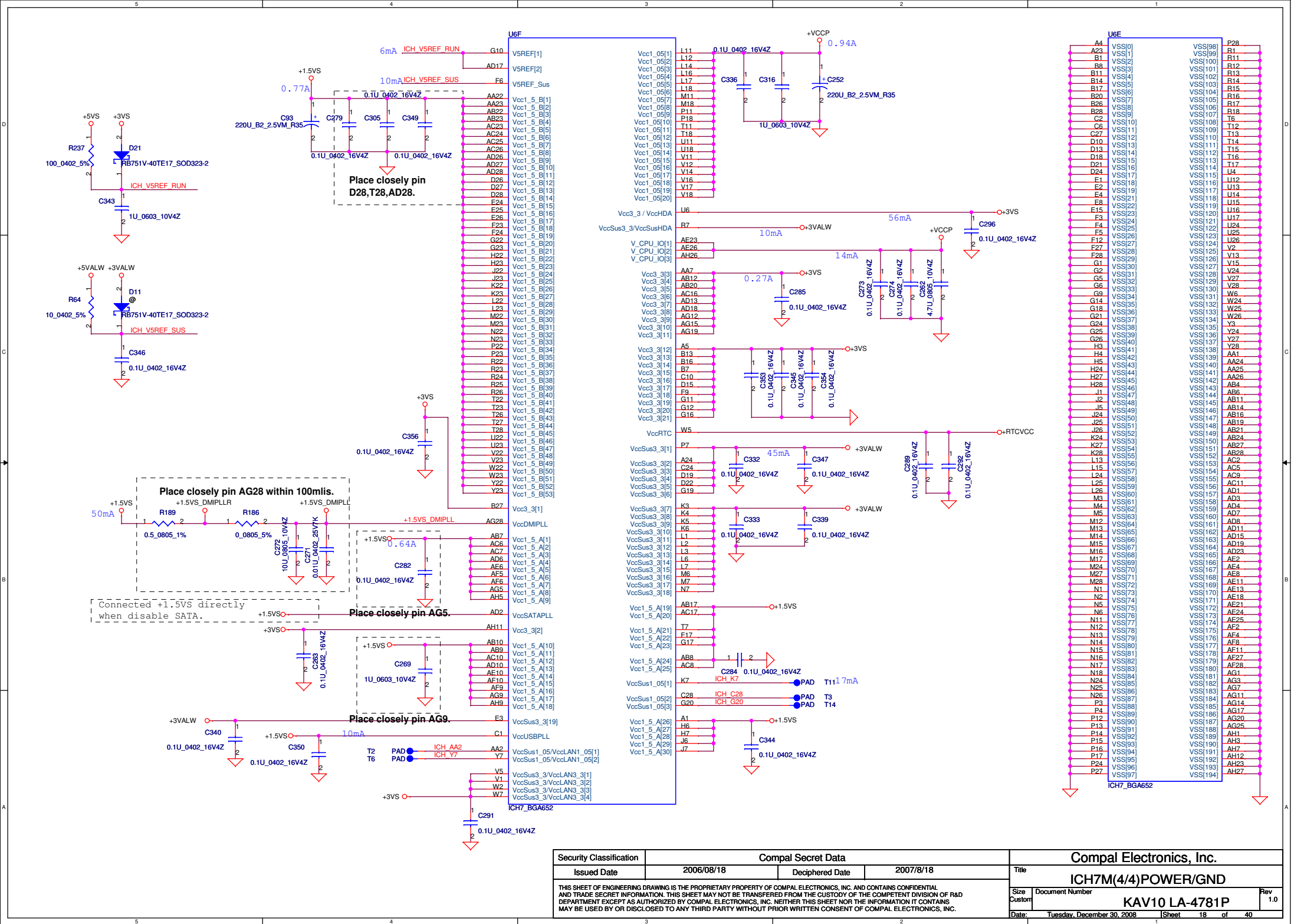


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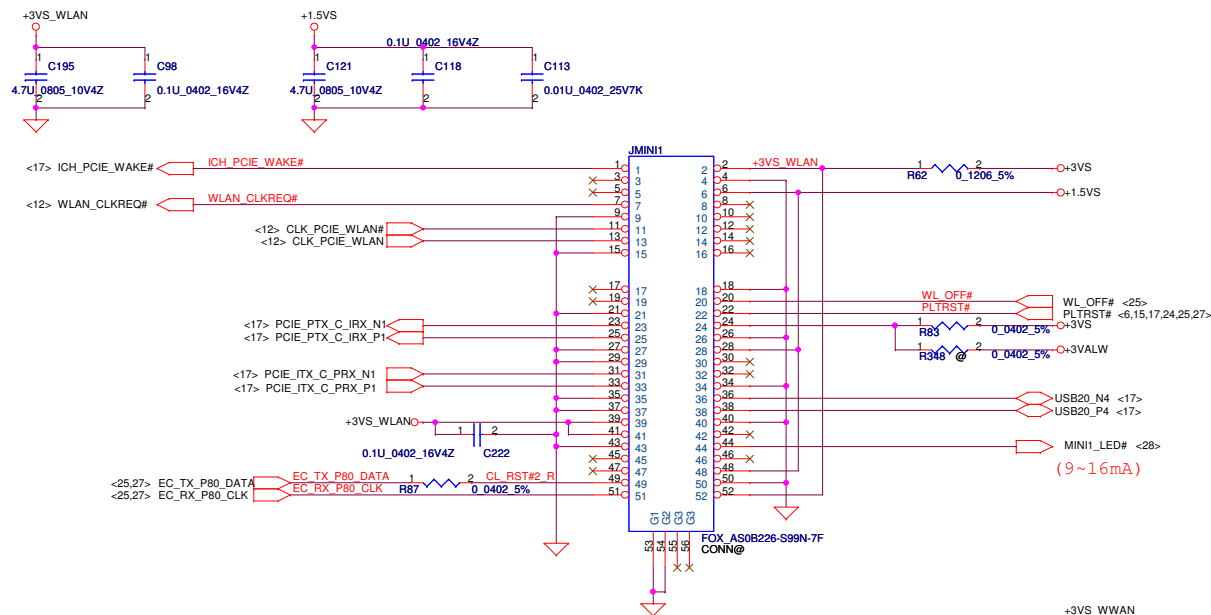


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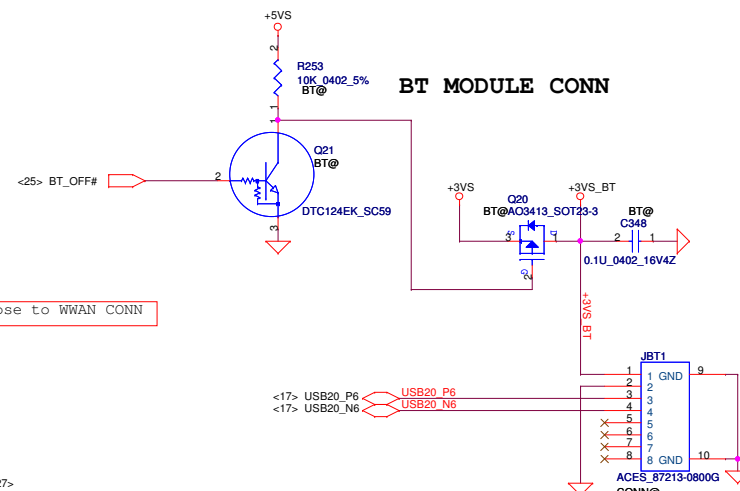
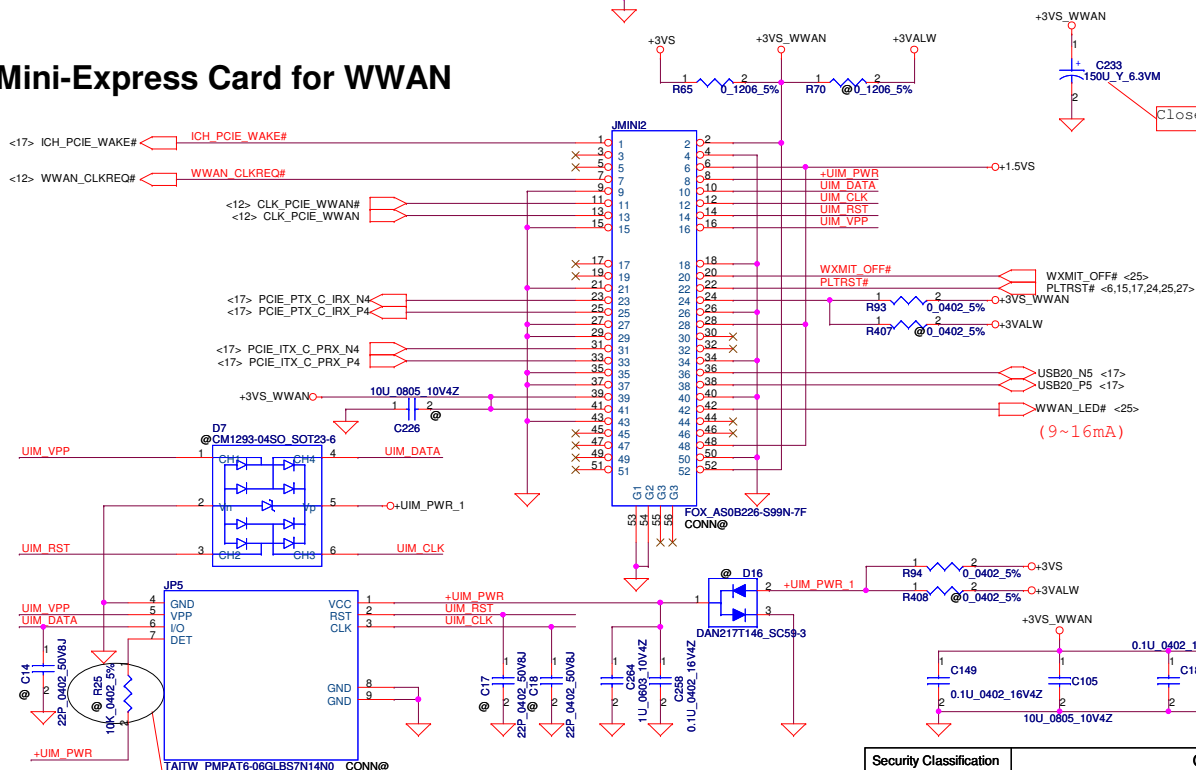




Mini-Express Card for WLAN

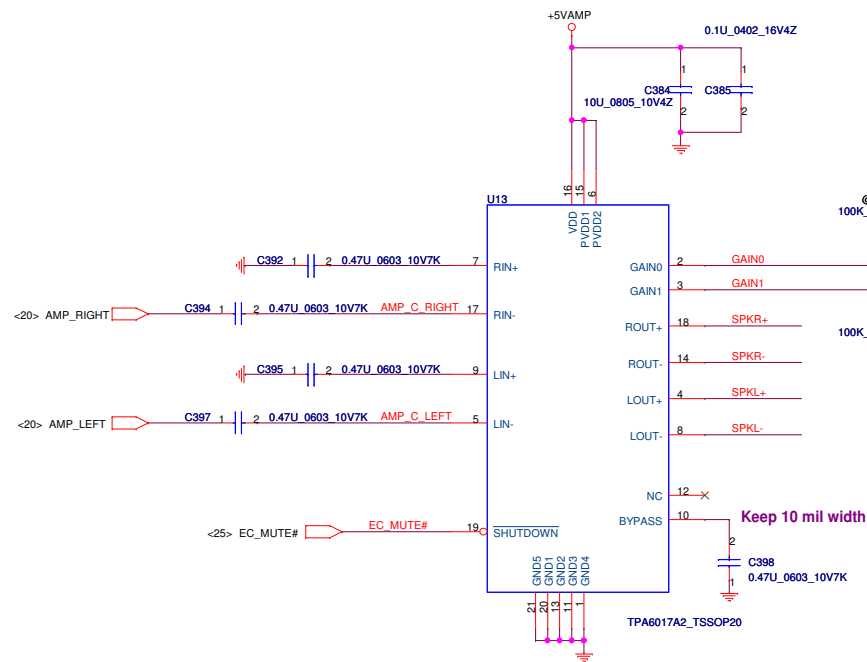


Mini-Express Card for WWAN

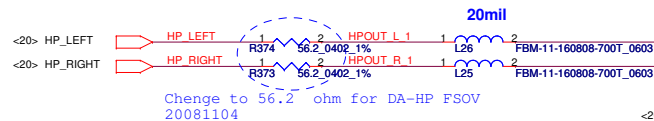


Reserve for SIM card does not meet rise time and pull-up is needed.

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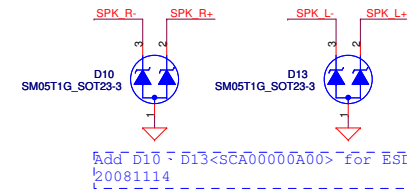
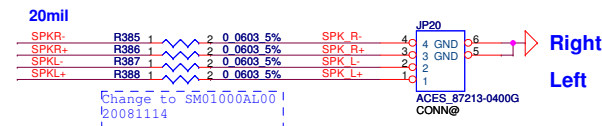


20081029 Update to 6dB

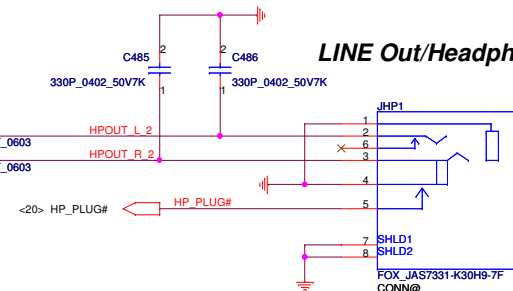


Change to 56.2 ohm for DA-HP FSOV
20081104

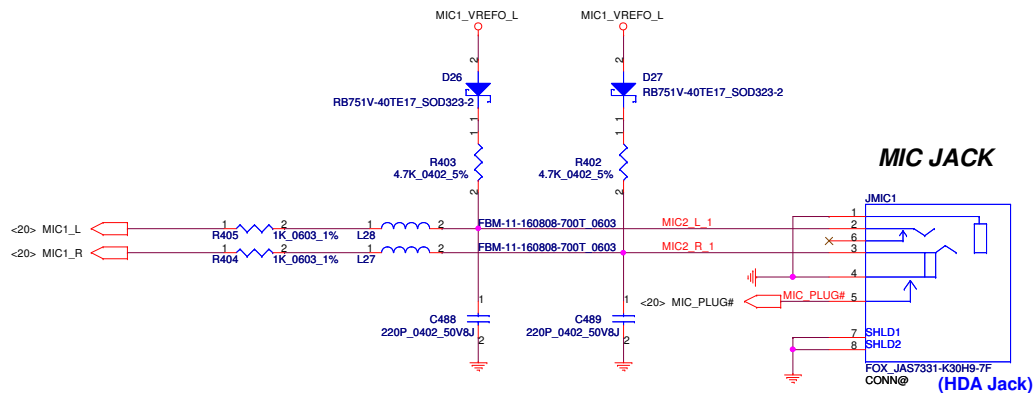
Int. Speaker Conn.



LINE Out/Headphone Out

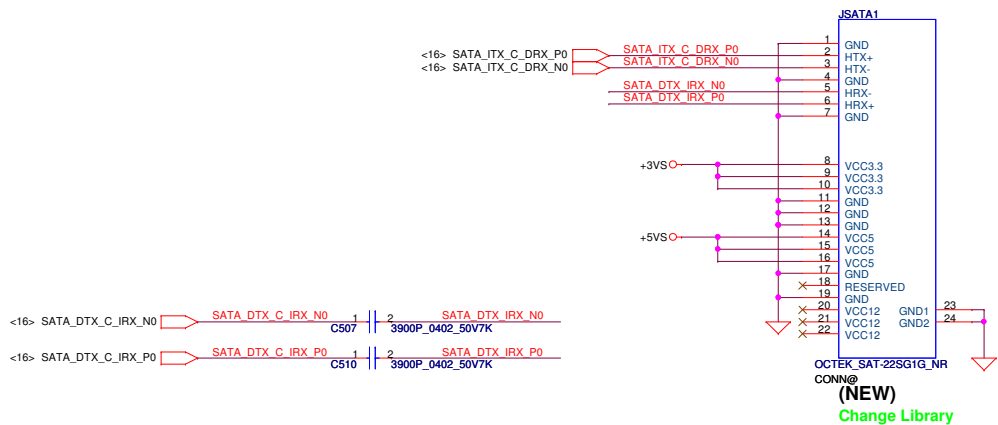


Change to 56.2 ohm for DA-HP FSOV
20081104

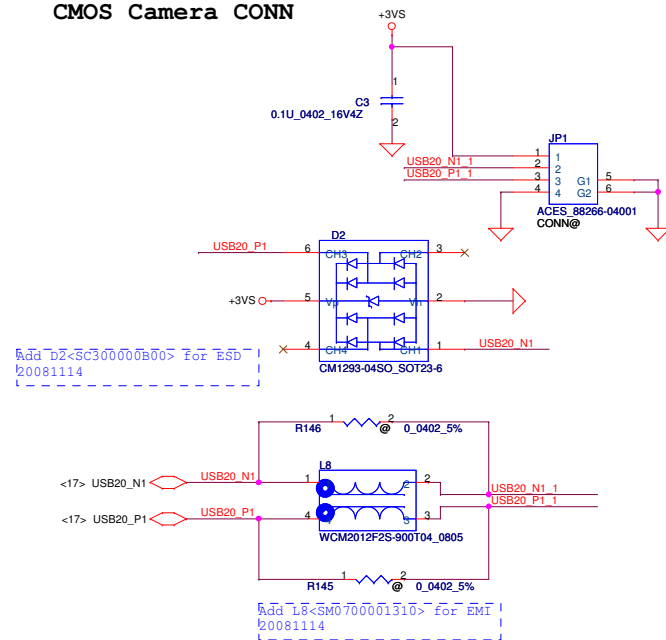


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Deciphered Date				2007/8/18				Amplifier & Audio Jack			
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Size B				Document Number				KAV10 LA-4781P			
Rev 1.0				Date				Tuesday, December 30, 2008			
Sheet				21				of 40			

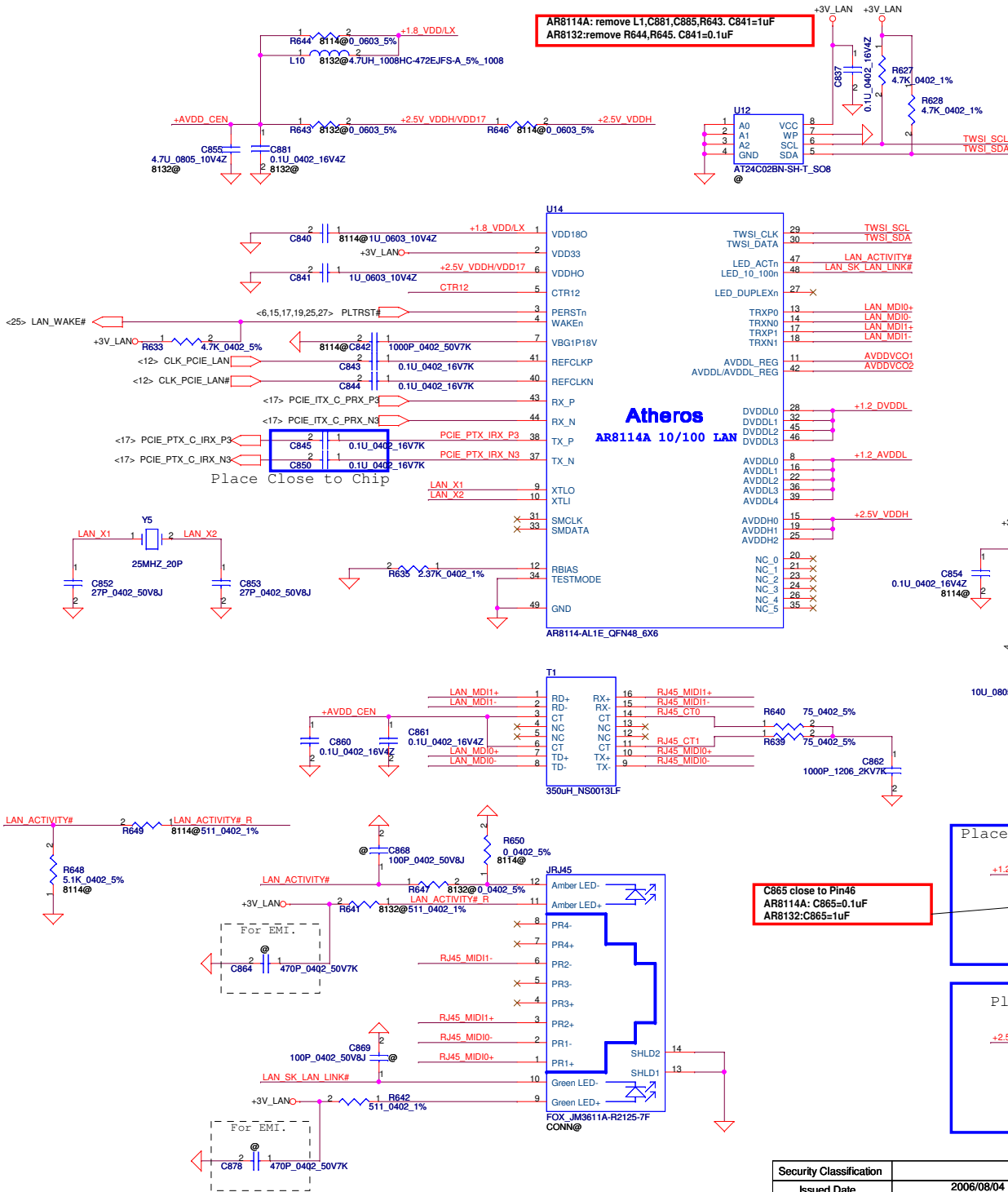
SATA HDD Conn.



CMOS Camera CONN

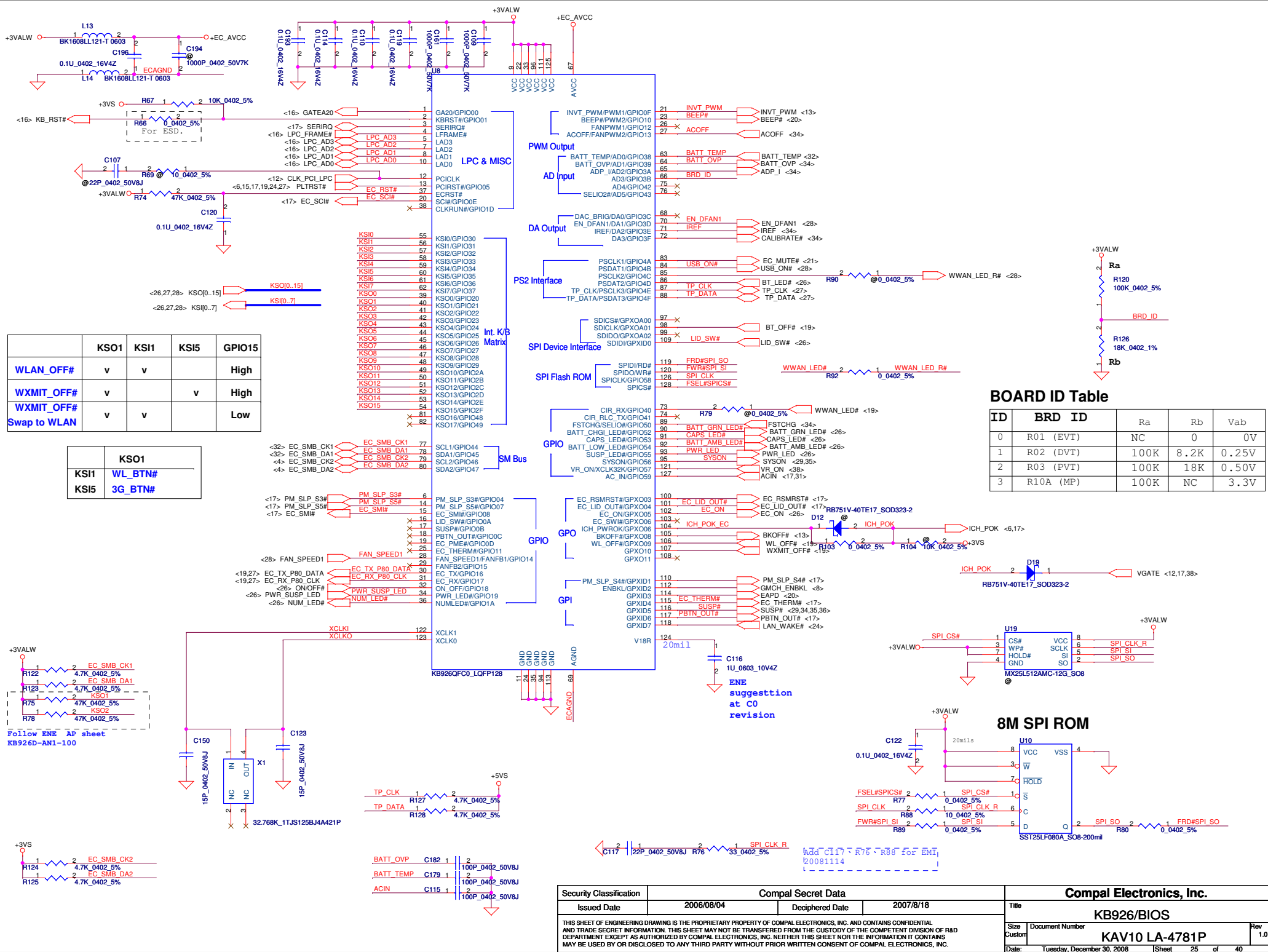


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						Size B		Document Number		Rev 1.0	
								KAV10 LA-4781P			
						Date:		Tuesday, December 30, 2008		Sheet 22 of 40	



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Deciphered Date				2007/8/18				KAV10 LA-4781P			
Title				Rev 1.0				Date: Tuesday, December 30, 2008			
Size				Document Number				Sheet 24 of 40			
Customer				Rev 1.0							

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ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

TOP Side

R73 @10K_0603_5%
R96 @10K_0603_5%
R347 100K_0402_5%
R3 10K_0402_5%

Bottom Side

D14 DAN202U_SC70
D1 RLZ20A_LL34
Q1 2N7002_SOT23

ON/OFFBTN#
ON/OFF#
51ON#
EC_ON
EC

Diagram illustrating the Pin 1 connection for the ACES 85201-0605 component. The component is connected to a 6-pin connector (JP2) with the following connections:

- Pin 1: +5V5
- Pin 2: +5VALW
- Pin 3: ON/OFFBTN#
- Pin 4: PWR_LED
- Pin 5: PWR_SUSP_LED
- Pin 6: Ground

Additional connections shown on the left:

- <25> PWR_LED is connected to Pin 3, Pin 4, and Pin 5.
- <25> PWR_SUSP_LED is connected to Pin 4 and Pin 5.

Component: ACES 85201-0605
CONN@

LED

3+VS

R195
@10K_0402_5%

<23> 5IN1_LED#

<16> SATA_LED#

SATA_LED#

MEDIA_LED#

+3VS

Q45A
2N7002DW-T/R7_SOT363-6

Q45B
2N7002DW-T/R7_SOT363-6

+3VS

Q3
2N7002_SOT23

<27> SDIO_LED#

SDIO_LED#

MEDIA_LED#

SDIO@

+3VS

LED2

R284 1.2K_0402_5%

+5VALW

R286 330_0402_5%

+5VALW

BATT_AMB_LED#

BATT_AMB_LED# <25>

BATT_GRN_LED#

BATT_GRN_LED# <25>

HT-297DQ-GO_AMB-YG

Compal Footprint

3 4
1 2

LID Switch

The schematic diagram shows the LID Switch circuit. It includes a +3VALW input, a 47K resistor (R71), a 0.1uF capacitor (C112), a 10pF capacitor (C11), and an A3212ELHLT-T_SOT23W-3 component (U9). The output of the component is connected to the LID_SW# pin of the A3212ELHLT-T_SOT23W-3 component.

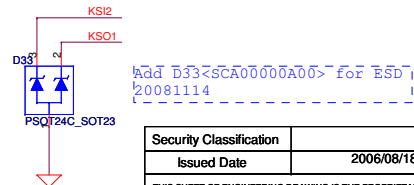
+5V
 (BLUE)
 R518
 1.5K 0402_1%
 BT@
 LED4
 HT-191NBQA_BLUE_0603
 BT@
 HARVATEK
 BT_LED#

The schematic diagram shows the internal wiring of the LED6 component. A +5VS power source is connected to a 1K_0402_5% resistor (R4). The other end of the resistor is connected to the anode of the LED6 (HT-191UYG-DT YEL/GRN_0603). The cathode of the LED6 is connected to a signal line labeled CAPS_LED#. The signal line is also connected to a component labeled CAPS_LED#.

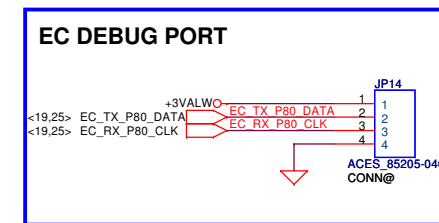
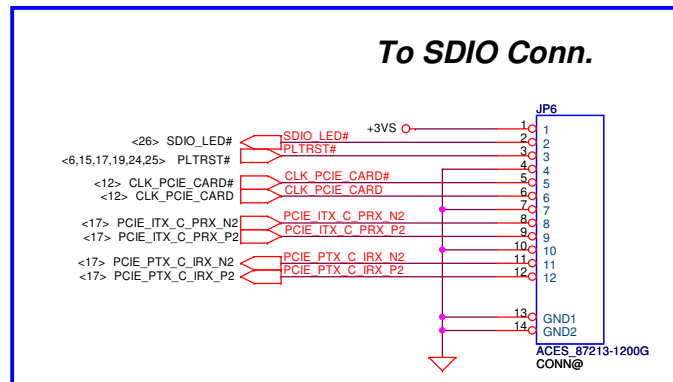
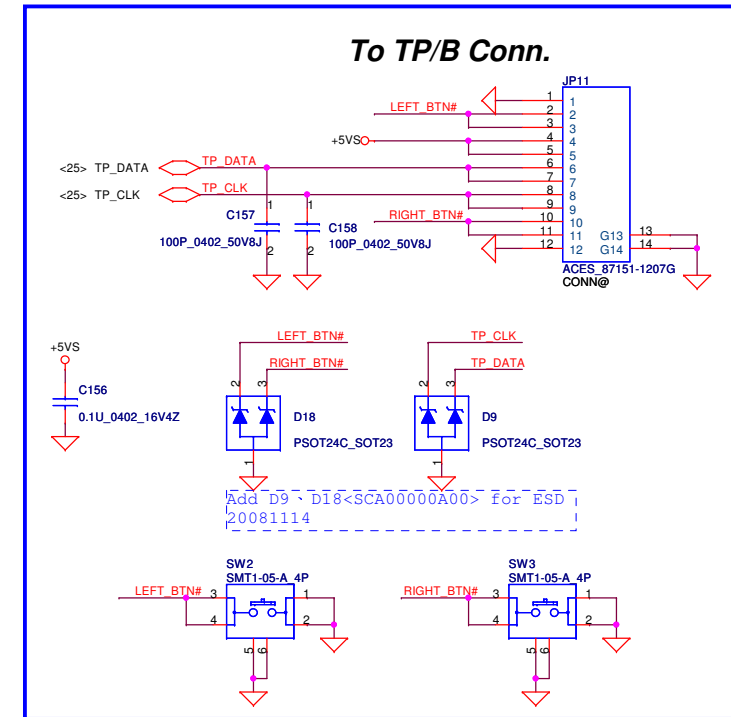
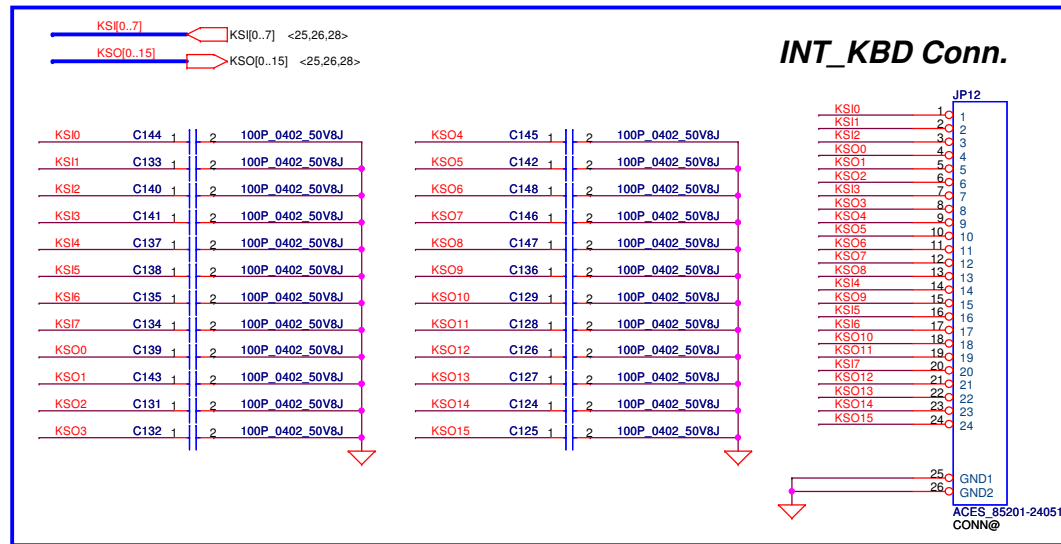
Bluetooth Button

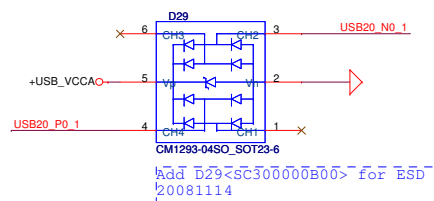
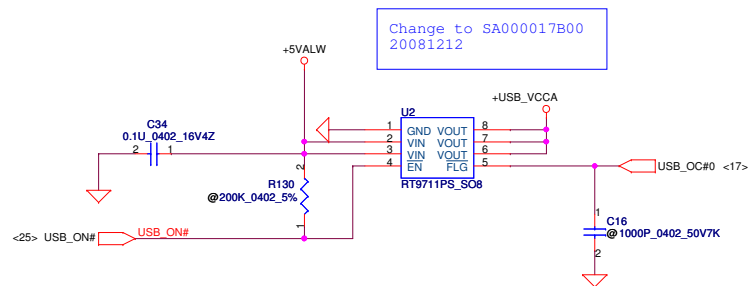
The diagram shows a circuit for a Bluetooth button. A blue switch labeled SW4 is connected to a module labeled BT@SMT1-05-A_4P. The module has four pins: 3 (KSO1), 4 (KSI2), 1 (KSI2), and 2 (KSO1). The module is connected to a red triangle symbol representing a Bluetooth signal. The module is labeled BT@SMT1-05-A_4P.

	KSO1
KSI2	BT_BTN#

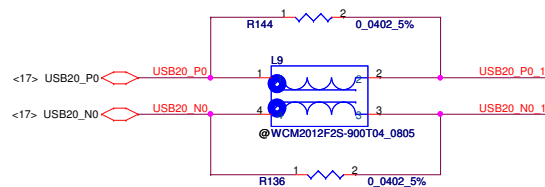
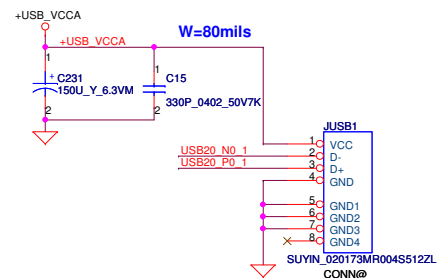


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				LID SW/LED/CMOS			
				Size	Document Number		Rev
				KAV10 LA-4781P			1.0
				Date:	Tuesday, December 30, 2008		Sheet





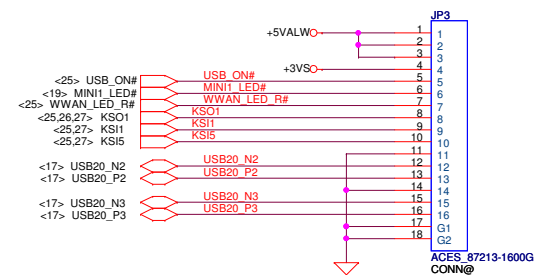
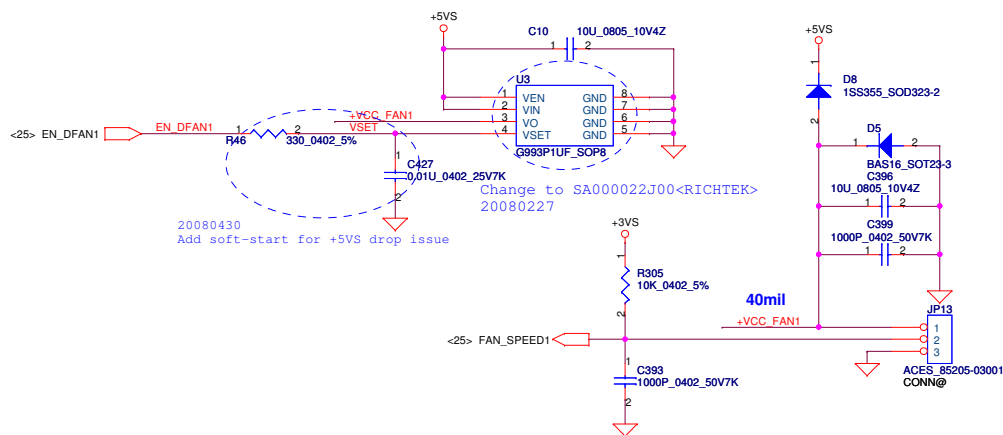
USB CONN. 1



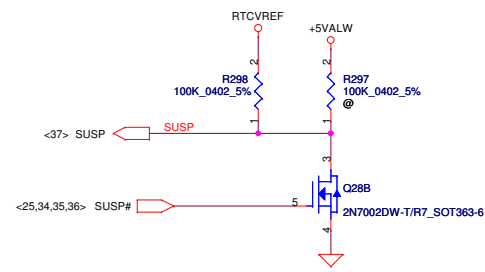
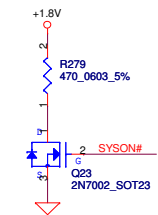
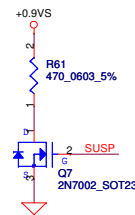
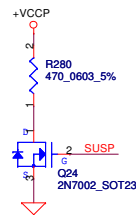
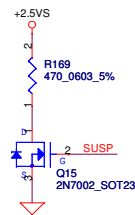
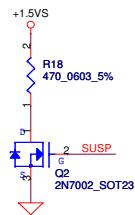
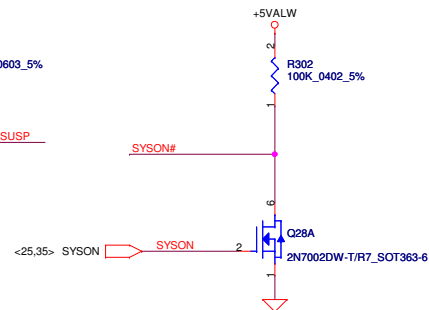
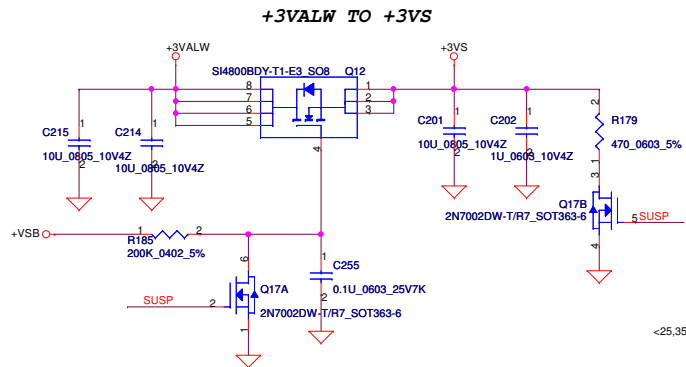
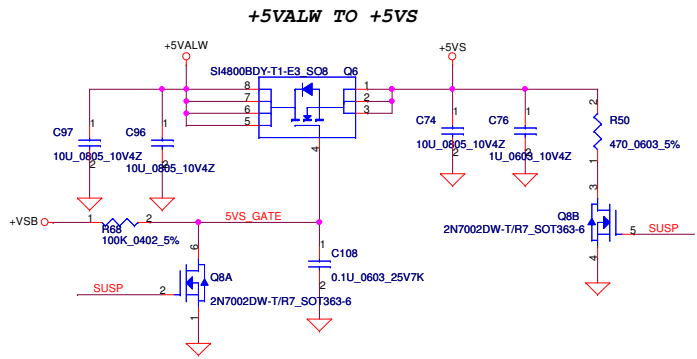
To USB/B Conn.

	KSO1
KS11	WL_BTN#
KS15	3G_BTN#

FAN1 Conn

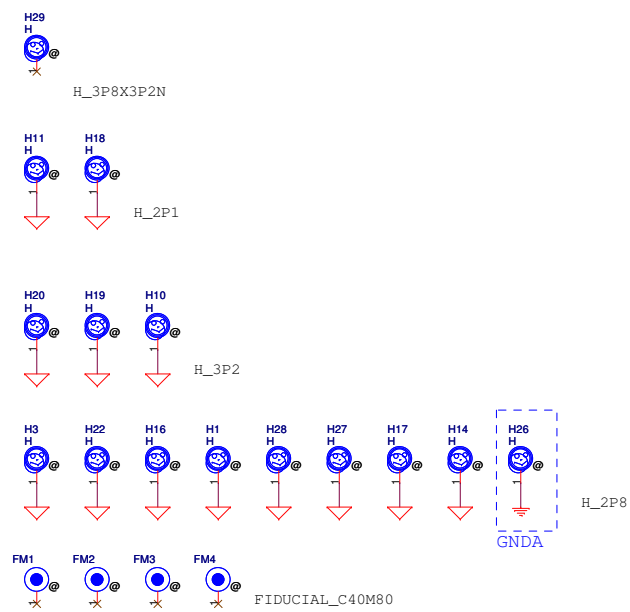


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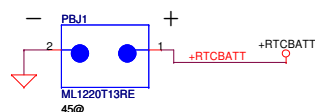
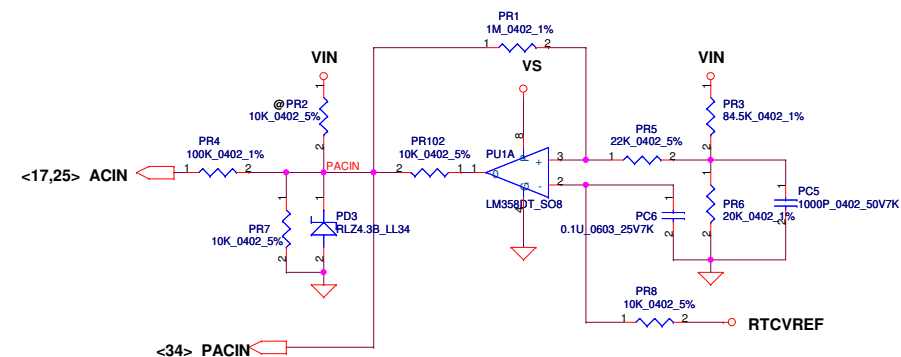


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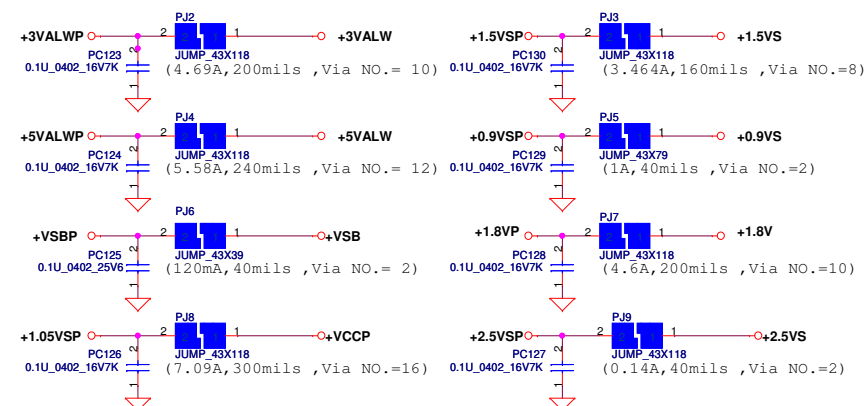
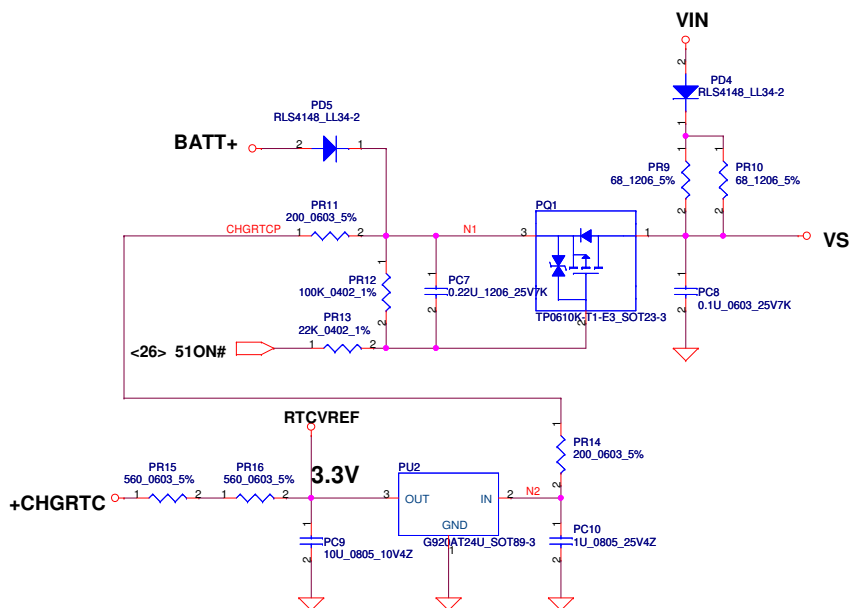
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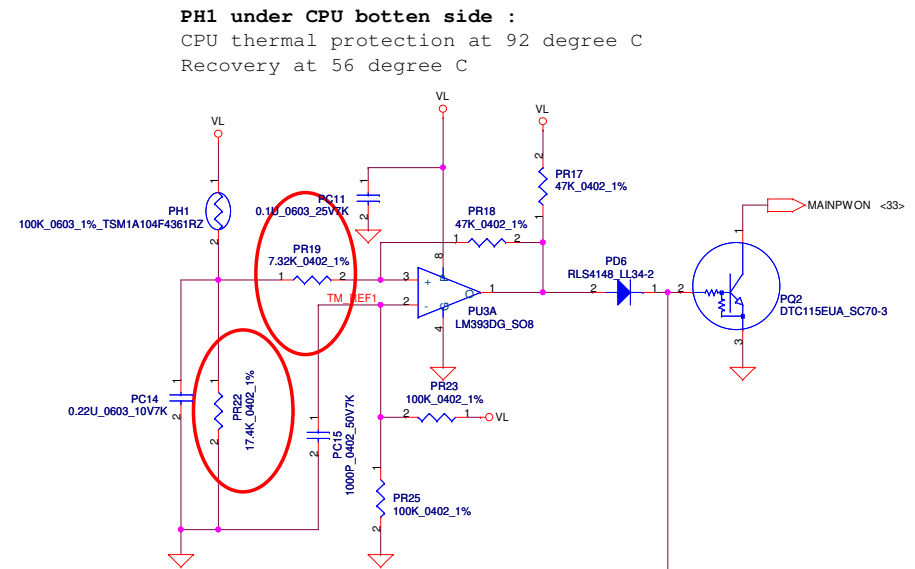
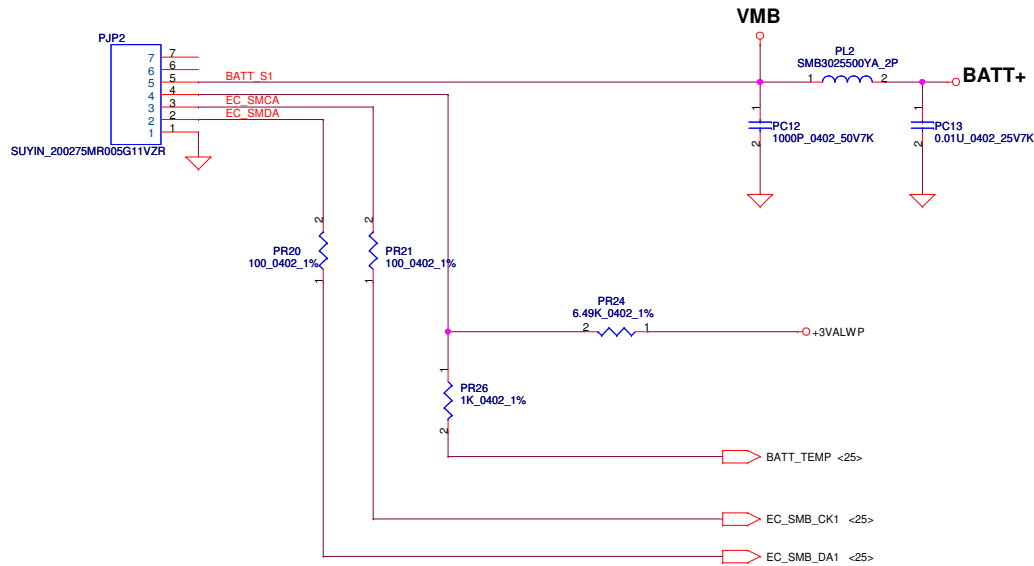
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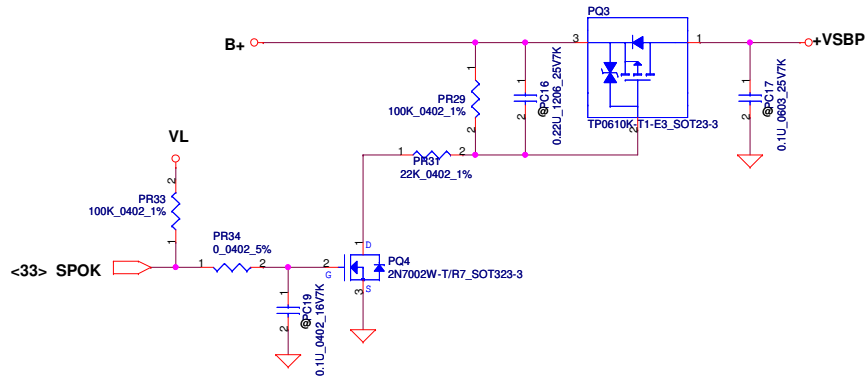
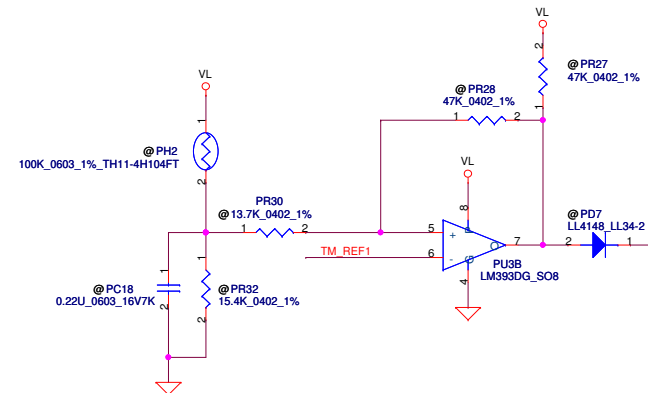
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



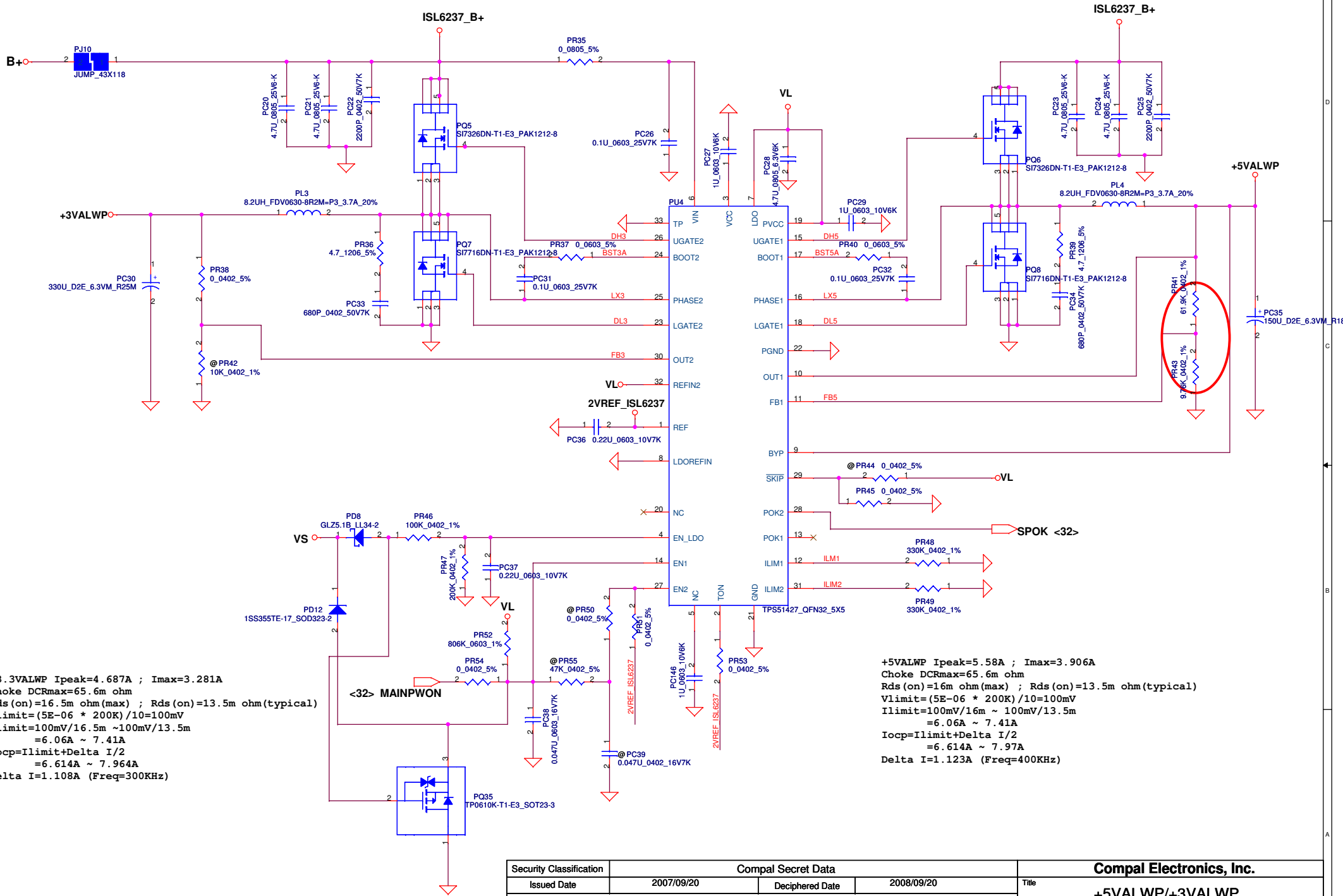
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PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



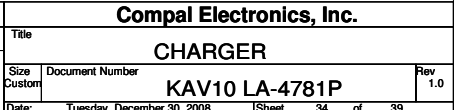
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				KAV10 LA-4781P	Rev
				Custom	1.0
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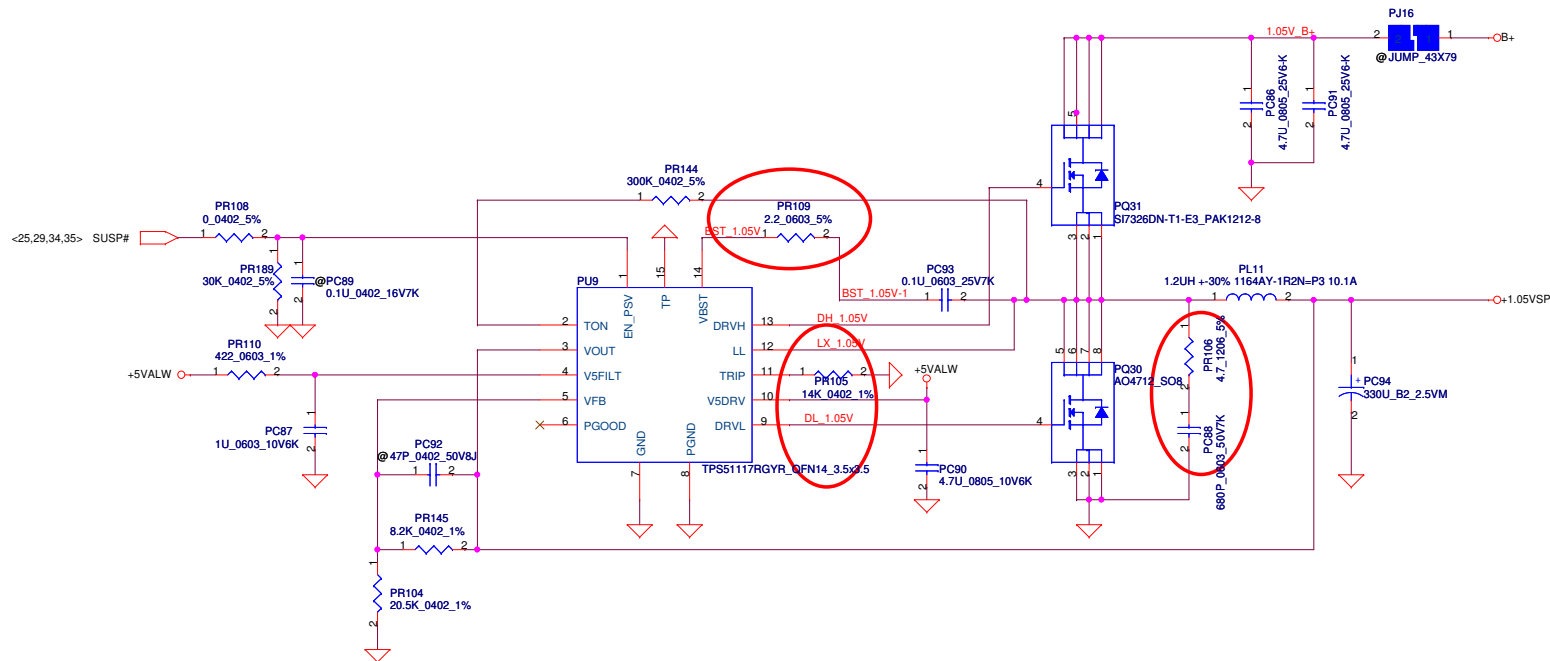


+3.3VALWP Ipeak=4.687A ; Imax=3.281A
Choke DCRmax=65.6m ohm
Rds(on)=16.5m ohm(max) ; Rds(on)=13.5m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/16.5m ~ 100mV/13.5m
=6.06A ~ 7.41A
Iocp=Ilimit+Delta I/2
=6.614A ~ 7.964A
Delta I=1.108A (Freq=300KHz)

+5VALWP Ipeak=5.58A ; Imax=3.906A
Choke DCRmax=65.6m ohm
Rds(on)=16m ohm(max) ; Rds(on)=13.5m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/16m ~ 100mV/13.5m
=6.06A ~ 7.41A
Iocp=Ilimit+Delta I/2
=6.614A ~ 7.97A
Delta I=1.123A (Freq=400KHz)

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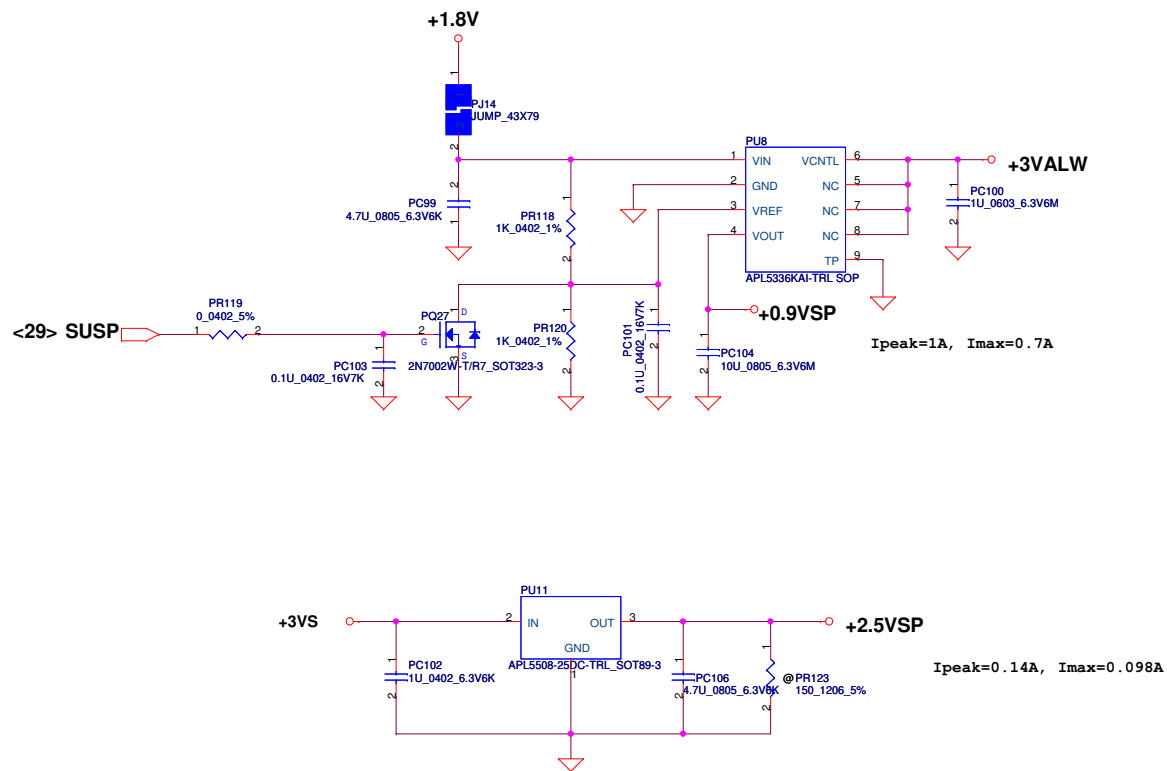




<Vo=1.05V> VFB=0.75V
 $V_o = V_{FB} * (1 + PR145 / PR104) = 0.75 * (1 + 8.2K / 20.5K) = 1.05V$
 $F_{sw} = 261KHz$

$C_{out} ESR = 15m\ ohm$ $R_{dson(max)} = 16.5m$ $R_{dson(typical)} = 13.5m$
 $I_{peak} = 7.09A$ $I_{max} = 4.963A$ $I_{ocp} = 8.51A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (1.5u * 261K) = 2.53A$
 $\Rightarrow 1/2 \Delta I = 1.265A$
 $V_{trip} = R_{trip} * I_{ocp} = 14K * 10uA = 0.14V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax} * 1.2) + 1.265$
 $= 0.14 / (0.0165 * 1.2) + 1.265 = 8.34A$
 $I_{ocpmax} = (0.14 / (0.0135 * 1.2)) + 1.265 = 9.91A$
 $I_{ocp} = 8.34A \sim 9.91A$

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify CPU_CORE VR_TT# circuit	circuit error	0.1	38	Cahnge PR128 to SD028680A80 (S RES 1/16W 68 +-5% 0402)	08/10/27	DVT
2	Diode modify	BOM error	0.1	31	Cahnge PD3 to SC4LZ43B0T4 (S ZEN DIO RLZ4.3B (LL-34))	08/10/27	DVT
3	Diode modify	BOM error	0.1	31	Cahnge PD4 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
4	Diode modify	BOM error	0.1	31	Cahnge PD5 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
5	Diode modify	BOM error	0.1	32	Cahnge PD6 to SC11N414880 (S DIO RLS4148 LL34)	08/10/27	DVT
6	Add 3/5V,charger,1.8/1.5V snubber	For ESD solution	0.1	33	Add PR36 PR39 PR57 PR147 PR148 to SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	08/10/27	DVT
7	Add CPU snubber	For ESD solution	0.1	33	Add PC33 PC34 PC40 PC122 PC95 to SE074681K80 (S CER CAP 680P 50V K X7R 0402)	08/10/27	DVT
8	Add CPU_CORE input capacitance	For ESD solution	0.1	38	Add PR126 to SD011680B80 (S RES 1/4W 6.8 +-5% 1206)	08/10/27	DVT
9	Add CPU_CORE input capacitance	For ESD solution	0.1	31	Add PC111 to SE024681J80 (S CER CAP 680P 50V J NPO 0603)	08/10/27	DVT
10	Modify 1.05V LMOS	cost down	0.1	31	Add PC133 SE042104K80 (S CER CAP .1U 25V K X7R 0603)	08/10/27	DVT
11	Modify 1.05V choke	cost down	0.1	31	Add PC132 SE074222K80 (S CER CAP 2200P 50V K X7R 0402)	08/10/27	DVT
12	Modify charger input capacitance size	BOM error	0.1	31	Add PC123 PC124 PC126 PC127 PC128 PC129 PC130 to SE076104K80 (S CER CAP .1U 16V K X7R 0402)	08/10/27	DVT
13	Modify charger VADJ circuit	circuit error	0.1	31	Add PC125 to SE072104K80 (S CER CAP 0.1U 25V K Y5V 0402)	08/10/27	DVT
14	Modify DIODE BOM (remove ROHN)	BOM error	0.1	31	change PQ30 to SB00000AJ00 (S TR AO4712 1N S08)	08/10/27	DVT
15	Modify ACIN circuit	EVI issue solution	0.1	31	change PL11 to SH00000FQ00 (S COIL 1.2UH +-30% 1164AY-1R2N=P3 10.1A)	08/10/27	DVT
16	Modify 3/5V circuit	Modify 5V voltage for HW request	0.1	31	change PC42 PC43 to SE142475K80 (S CER CAP 4.7U 25V K X5R 1206 H1.6)	08/10/29	DVT
17	Modify 1.8Vcircuit	Modify 1.8V voltage for HW request	0.1	35			
18	Modify 1.05V circuit	add snubber for SED 3G solution	0.1	36			
19	Modify 1.05V circuit	add boost for 1.05v issue	0.1	36			
20							
21							
22							
23							

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
				PIR (PWR)	
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- <8/25>
1. Update Power SCH
<8/26>
1. Update Power SCH
2. Change
 D7 SC300000D00 to SC300000000
3.Change
 C49、C50 SE071180K80 to SE071180J80
<8/27>
1. Updata Power SCH
2. Modify
 RJ45 temp footprint FOX_JM3611A-R4122-7F_12P-T
<8/28>
1. Updata Power SCH
<9/1>
1. Updata Screw
<9/5>
1. SWAP USB20_1 Signal.
<9/10>
1. Remove Mini card pin55、pin56 的GND。
2. Change JREAD1.42、H26 to GNDA。
<9/12>
1. Swap 3G ESD pin neme。
<9/15>
1. Update Audio Jack footprint
2. Chcnge R641、R642 300ohm to 511ohm for Arthros。
3. Update L footprint。
<9/16>
1. Update POWER SCH.
<9/17>
1. Update POWER SCH.
2. ADD R380、R383 for ESD.
<9/18>
1. Update ATHEROS 10/100 LAN <AR8132/AR8114>
<9/24>
1. Change C870 0.1u to 1u.
<9/26>
1. R88 change to 0ohm.

<10/21>
1.Remove C389 for Audio can't detect issue on page 16
2.Add KSO1/KSO2 PU +3VALW on page25
3.Add R205 for schematic mistake on page 04
4.Change EC RST to PLTRST on page 25
5.Add J8 to cost down Audio LDO on page 20
6.Add R72 to reserve +3VALW for 3G on page 19
7.Reserve C238 for CRTDAC on page 10
8.Add R87 for Debug card on page 19
9.Change C108/C255 to 0.1uF for random hang issue
10.Change JP3 pin assignment on page 28
<10/21>
1. Update Power SCH
<10/29>
1. Audio AMP 10dB update to 6dB
<11/3>
1. Update Power SCH
<11/4>
1. Change R373、R374 to 56.2 ohm for DA-HP FSOV
2. Add C834、C851 for 3G noise
3. Change KB926 C1 to D2
4. Card reader RT5158E change to RT5159-GR
<11/5>
1. Swap D7 pin define
<11/10>
1. EC add R79、R90、R92 for SMS wakeup。

<11/28>
1. Reserve C40、C46、C47、C233
2. R617 change to 0ohm for RTS5159
3. R68 200K change to 100K for sequence
4. Remove C47
5. Add D30 for LVDS
6. Add C55 0.1U
7. U2 Change to SA000017B00
 -because RT9715 Can't protect

<12/30>
1. Update power MP SCH