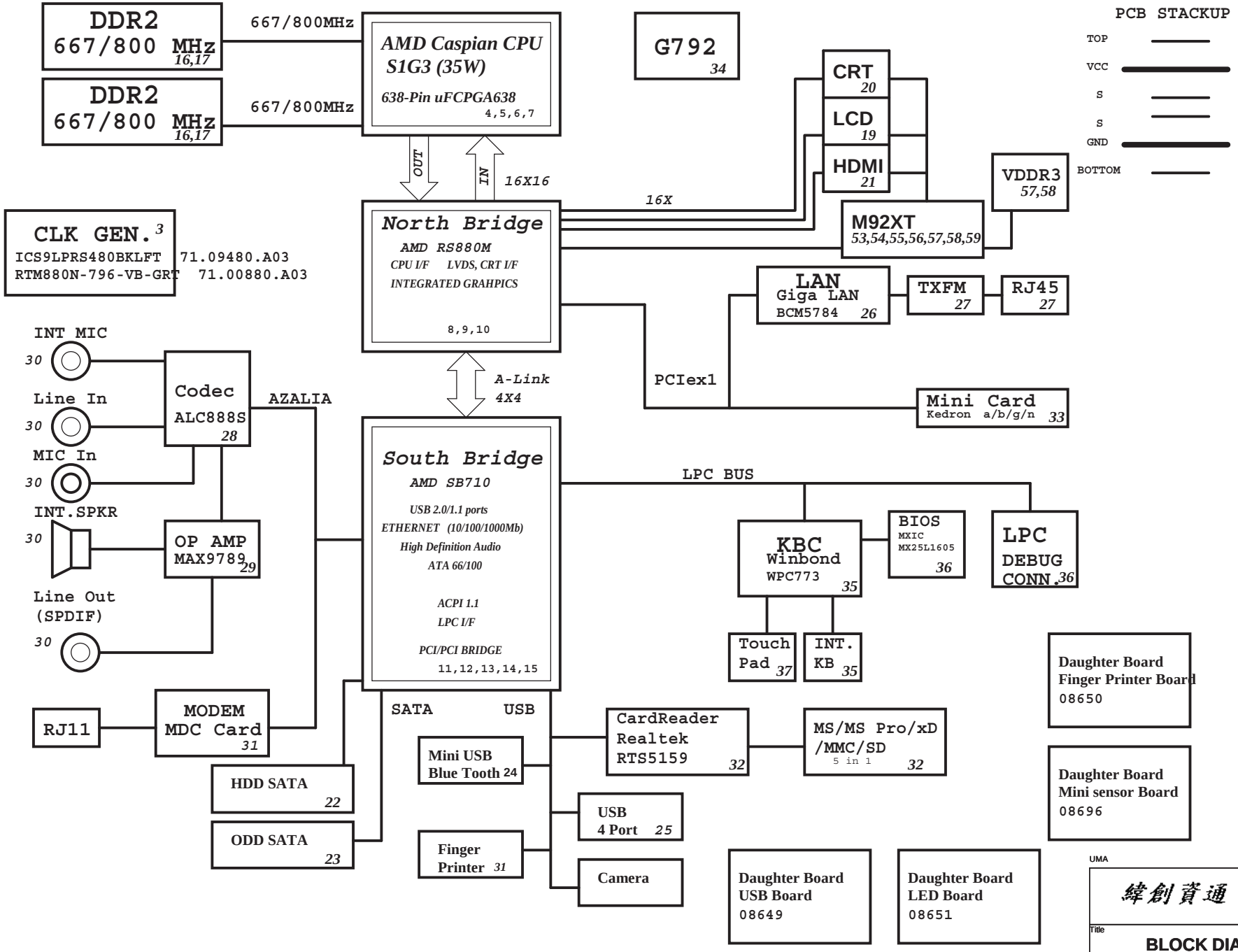
JV71-TR Block Diagram

Project code: 91.4FP01.001
PCB P/N : 48.4FP02.0SB
REVISION : 09243-SB



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49

5V_S5	1D1V_M92

RT9161 49

3D3V_S0	2D5V_S0 (200mA)

G957 49

3D3V_S0	1D5V_S0 (1A)

G9161 49

3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 1 of 61

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV71-TR	SA

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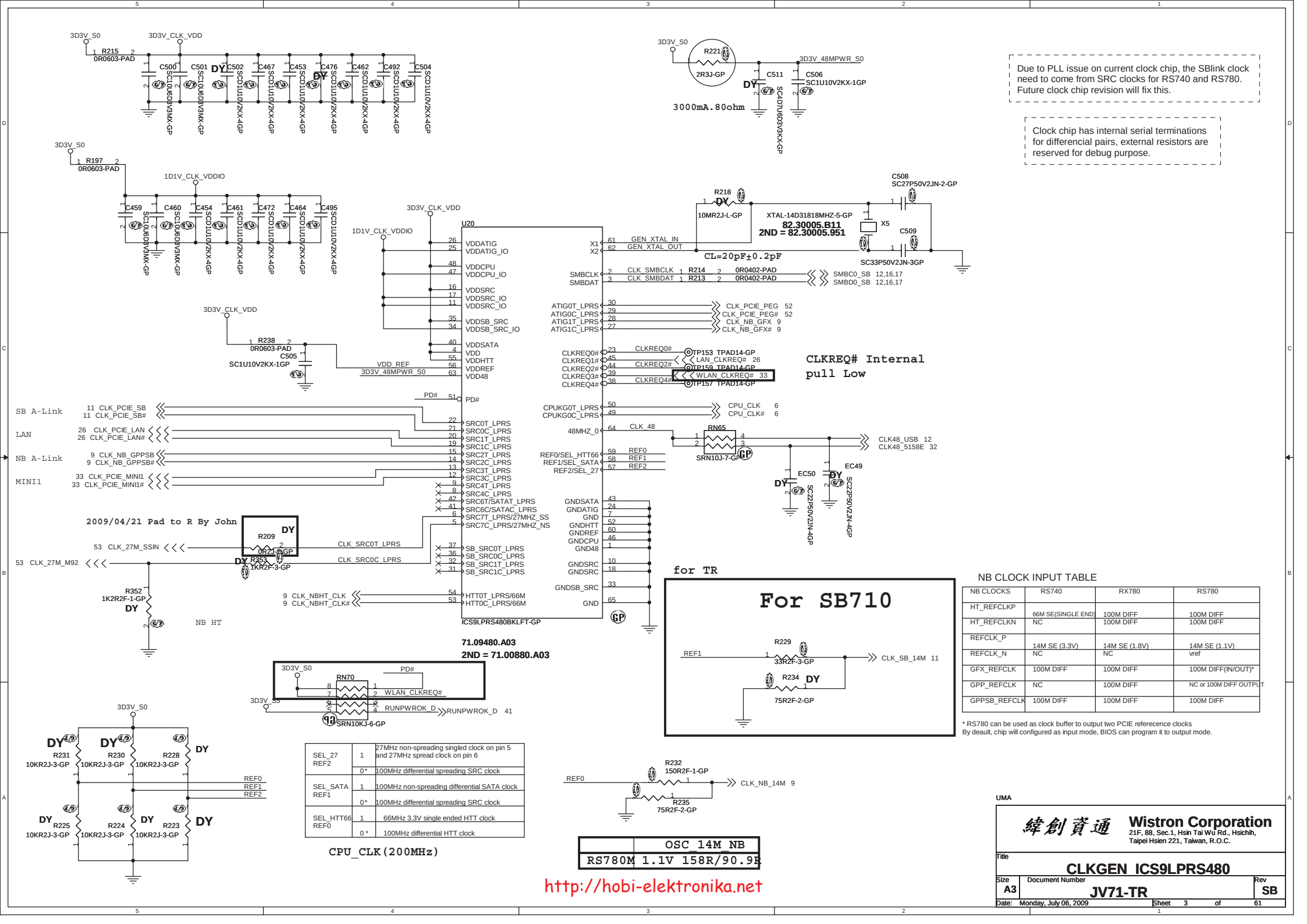

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

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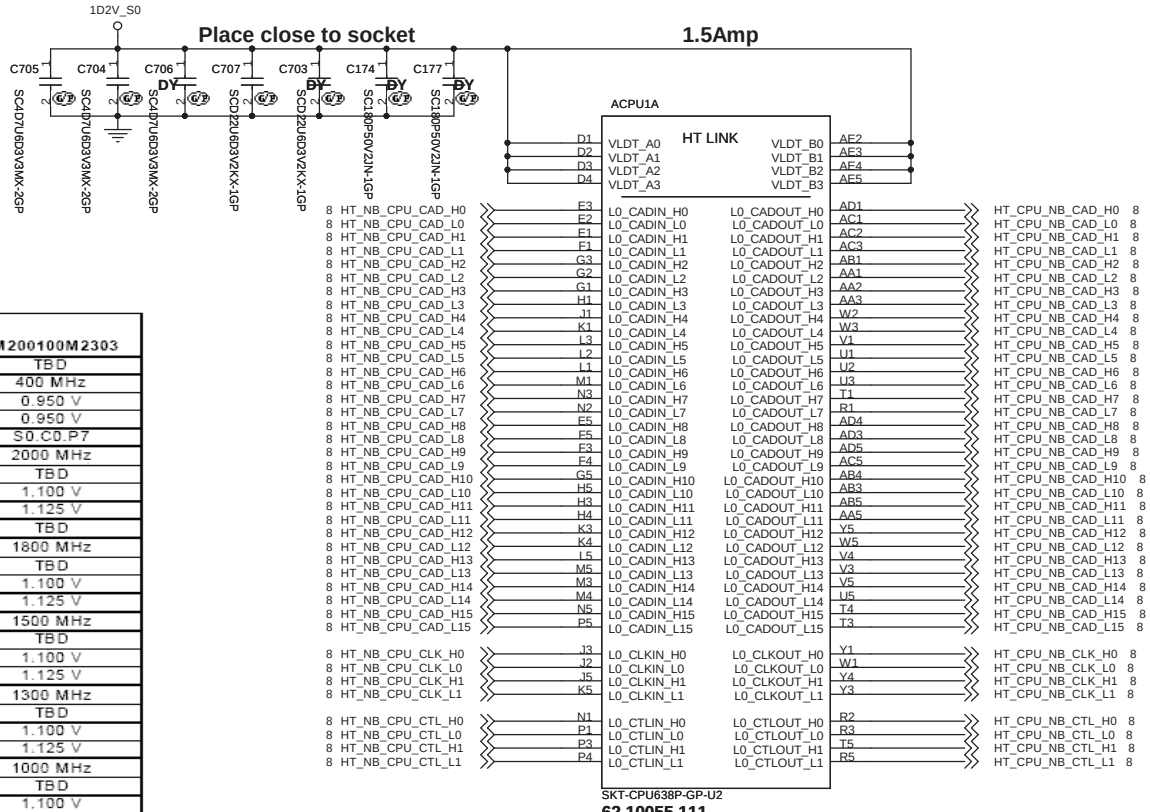
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 3 of 61



SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

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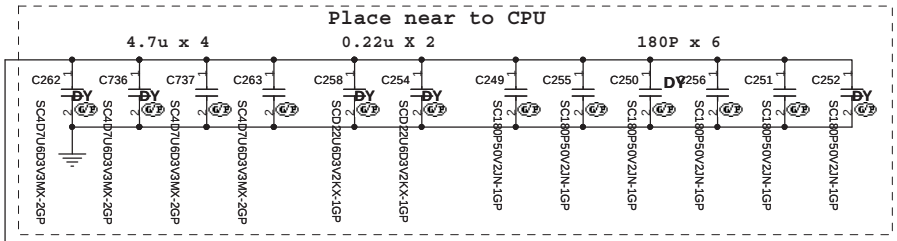
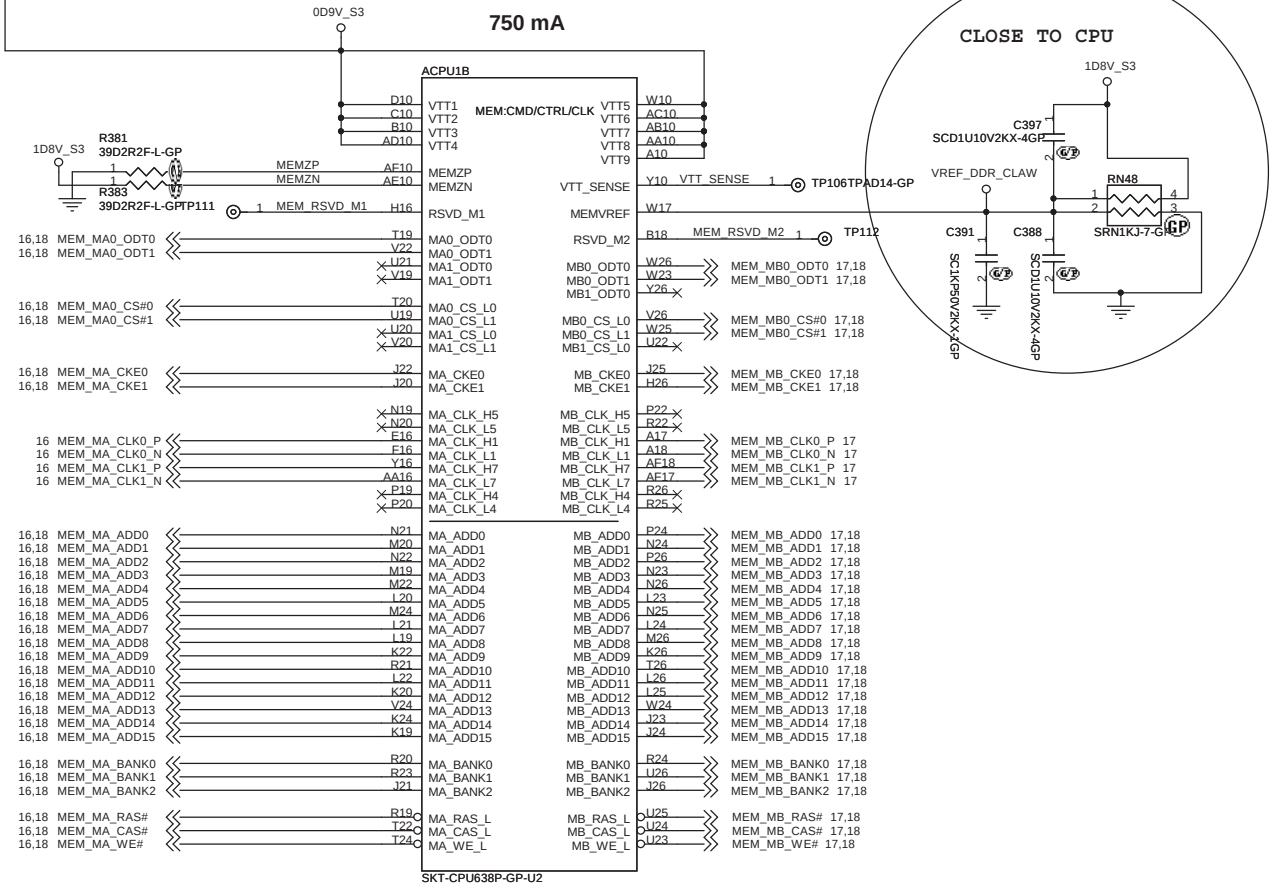
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

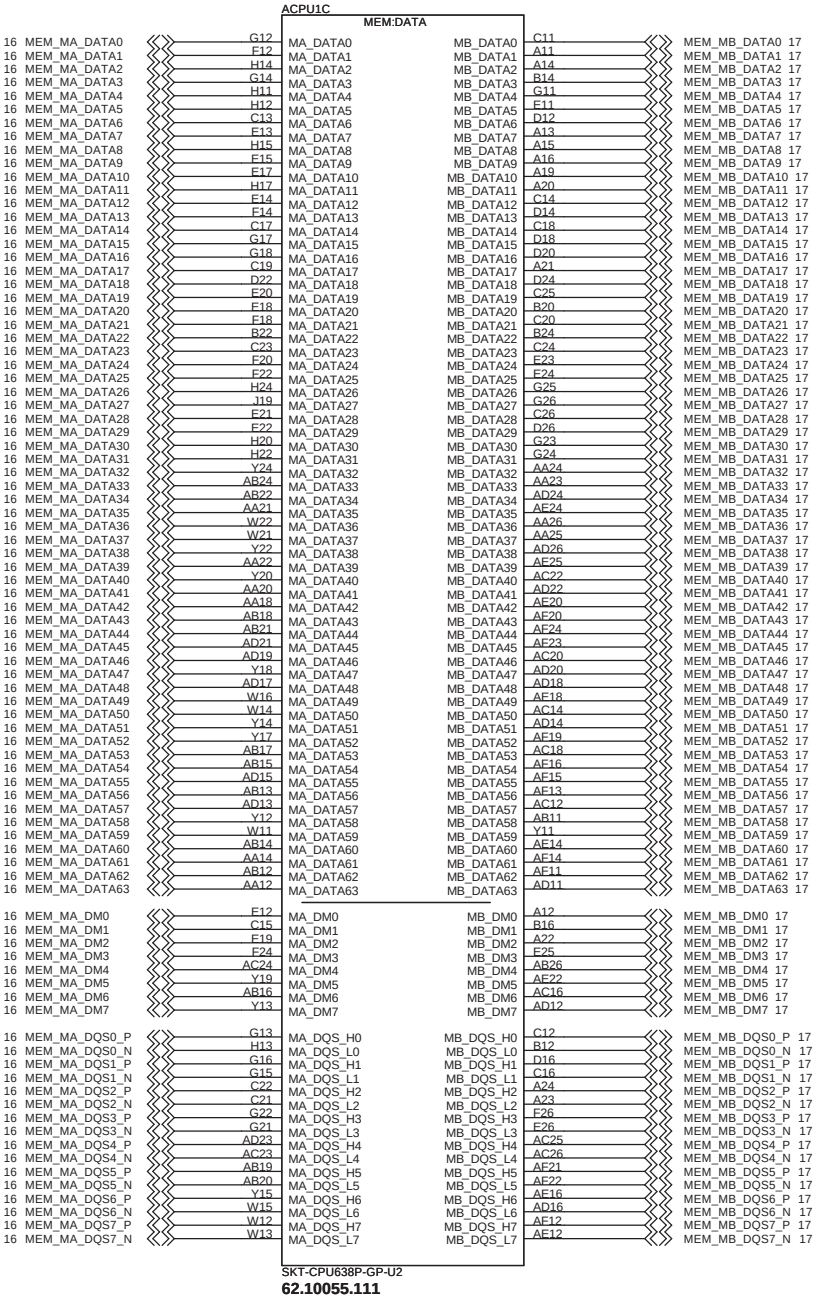
Title: CPU HT LINK I/F (1/4)

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 4 of 61







UMA

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Title	CPU_DDR_(2/4)	
Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 5 of 61	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

Cloce To CPU

For HDT DBG

for TR

for TR

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Near CPU PIN

84.T3904.C11
2ND = 84.03904.L06

62.10055.111

CPU exceeds to 125℃

HDT Connectors

UMA

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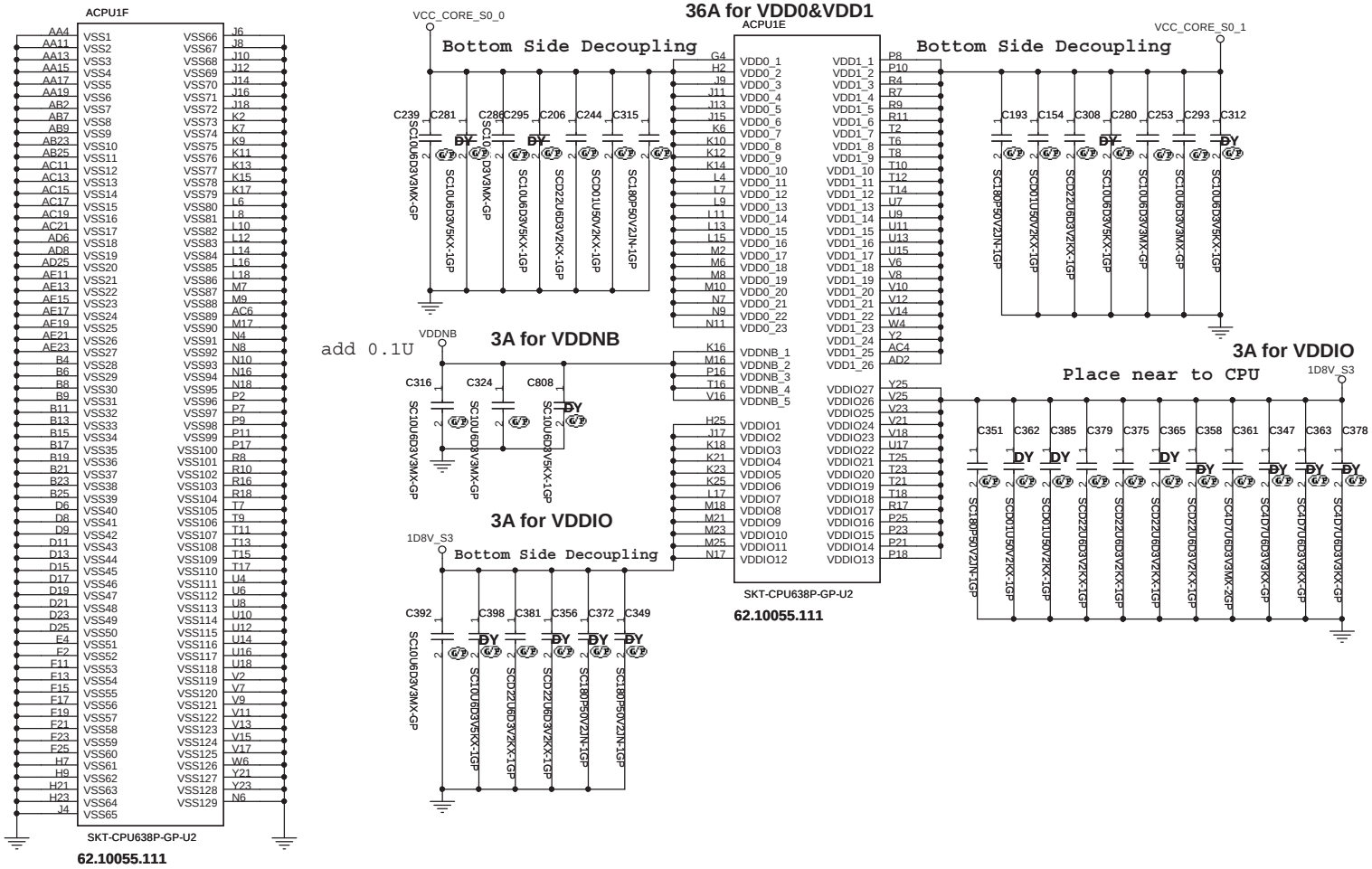
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 6 of 61



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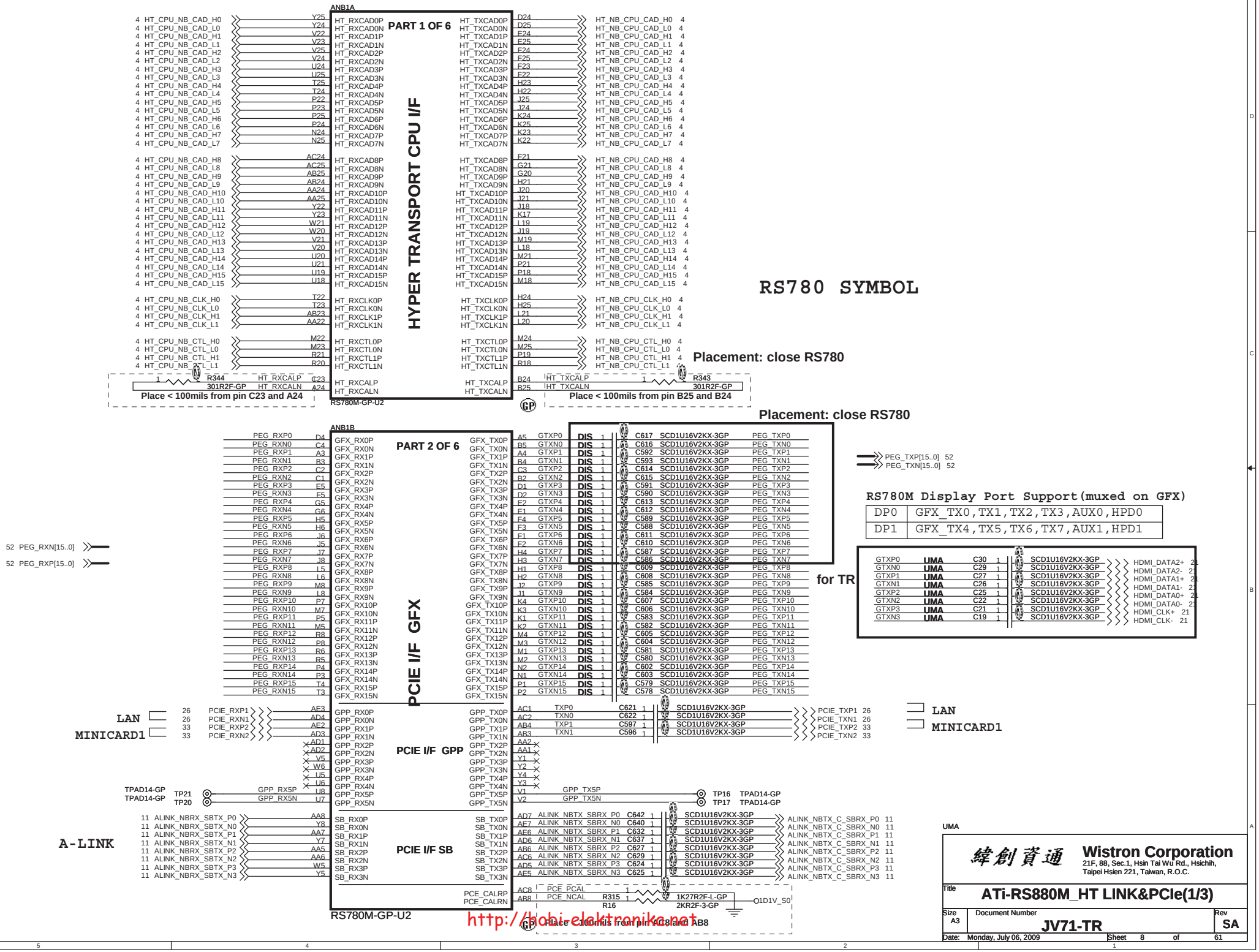
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size A3	Document Number JV71-TR	Rev SA
Date: Monday, July 06, 2009	Sheet 7 of 61	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
RS780 SYMBOL
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
for TR
LAN
MINICARD1
A-LINK
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size A3
Document Number
JV71-TR
Rev SA
Date: Monday, July 06, 2009
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Reserve for EMI 0408

NB_PWRGD — DY EC962 SC1KP50V2KX-1GP

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)

*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

*1 :Disable 0 : Enable

SUS_STAT#

Selects Loading of STRAPS From EEPROM

*1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

3D3V_S0 — L3 220ohm 100mA SBK160808T-221Y-N-GP — 68.00119.111 — 3D3V_S0_AVDD — C70 SCD1U10V2KX-4GP DY — C71 SC1U10V2KX-1GP

3D3V_S0 — R563 3K3R2J-3-GP — R562 3K3R2J-3-GP — GMCH_VSYNC — GMCH_HSYNC

6 LDT_RST#_CPU — R21 0R2J-2-GP DY — 11,26,35 PLT_RST1# — R17 0R2J-2-GP — SYSREST# — C37 SC220P50V2KX-3GP

1D8V_S0 — R41 0R0603-PAD — 1D8V_S0_AVDDDI — C88 SC1U10V2KX-1GP — C89 SCD1U10V2KX-4GP — 68.00119.111

1D8V_S0 — 220ohm 200mA — R43 SBK160808T-221Y-N-GP — C80 SC1U10V2KX-1GP — C99 SCD1U10V2KX-4GP — 1D8V_S0_AVDDQ

TC2 ST100U6D3VBM-5GP DY — 77.C1071.081

Close to NB ball

GMCH_BLUE — R36 150R2F-1-GP

GMCH_GREEN — R37 150R2F-1-GP

GMCH_RED — R38 140R2F-GP

2009/04/22 R609 Change to 1K By John

1D8V_S0 — for TR — R609 1KR2F-3-GP

6 LDT_STP#_CPU — R14 0R0402-PAD — NB_LDT_STOP#

6 ALLOW_LDTSTOP — R24 0R2J-2-GP DY — NB_ALLOW_LDTSTOP

for TR

1D8V_S0 — 220ohm 200mA — L4 2R3J-GP — 2009/05/26 SB Change

1D1V_S0 — L33 SBK160808T-221Y-N-GP — 220ohm 200mA — 68.00119.111 — 1D1V_S0_PLLVDD — C644 SC1U10V2KX-1GP — C643 SCD1U10V2KX-4GP DY

80.10715.L04
2ND = 77.C1071.081
3RD = 77.21071.09L

TC1 ST100U6D3VBM-1GP — C82 SC47U6D3V5MX-1GP DY — C78 SC1U10V2KX-1GP — C77 SCD1U10V2KX-4GP DY

ENABLE External CLK GEN

1D1V_S0 — RN11 SRN1KJ-7-GP

1D8V_S0 — L5 SBK160808T-221Y-N-GP — 220ohm 200mA — 68.00119.111 — VDDA18HTPLL — C86 SC1U10V2KX-1GP DY — C97 SCD1U10V2KX-4GP

1D8V_S0 — L1 SBK160808T-221Y-N-GP — 220ohm 200mA — 68.00119.111 — VDDA18PCIEPLL — C41 SC1U10V2KX-1GP DY — C42 SCD1U10V2KX-4GP

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.1V	1.0V

ANB1C

RS780M-GP-U2

PART 3 OF 6

CRT/TVOUT

AVDD1 F12
AVDD2 F12
AVDDDI F14
AVSSDI G15
AVDDQ H15
AVSSQ H14
1D8V_S0_AVDDQ

C_Pr E17
Y F17
COMP_Pb F15

20 GMCH_RED — RED G18
20 GMCH_GREEN — REDb G17 — GREEN E18 — GREENb F18 — BLUE F19 — BLUEb F19
20 GMCH_BLUE

20 GMCH_HSYNC — DAC_HSYNC A11
20 GMCH_VSYNC — DAC_VSYNC B11
20 GMCH_DDCCLK — DAC_SCL F8
20 GMCH_DDCDATA — DAC_SDA F8

R33 715R2F-GP — DAC_RSET G14

PLL PWR LVTM

PLLVDD A12
PLLVDD18 D14
PLLVSS B12
1D8V_S0_PLVDD18

VDDA18HTPLL H17
VDDA18HTPLL

VDDA18PCIEPLL D7
VDDA18PCIEPLL1 E7
VDDA18PCIEPLL2

SYSRESET# D8
POWERGOOD A10
LDTSTOP# C10
ALLOW_LDTSTOP C12
12,41 NB_PWRGD — NB_PWRGD
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

CLOCKs PM

HT_REFCLKP C25
HT_REFCLKN C24
3 CLK_NBHT_CLK
3 CLK_NBHT_CLK#

REFCLK_P/OSCIN E11
REFCLK_N F11
3 CLK_NB_14M — NB_REFCLK_N

GFX_REFCLKP T2
GFX_REFCLKN T1
3 CLK_NB_GFX — CLK_NB_GFX
3 CLK_NB_GFX# — CLK_NB_GFX#

GPP_REFCLKP U1
GPP_REFCLKN U2
TPAD14-GP TP180 — CLK_NBGPP_CLK
TPAD14-GP TP181 — CLK_NBGPP_CLK#

GPPSB_REFCLKP V4
GPPSB_REFCLKN V3
3 CLK_NB_GPPSB
3 CLK_NB_GPPSB#

MIS.

I2C_CLK B9
I2C_DATA A9
DDC_CLK0/AUX0P
DDC_DATA0/AUX0N
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
19 CLK_DDC_EDID
19 DAT_DDC_EDID
TPAD14-GP TP188 — DDC_DATA0/AUX0N B8
TPAD14-GP TP239 — DDC_CLK0/AUX0P A8
21 GMCH_HDMI_CLK — GMCH_HDMI_CLK B7
21 GMCH_HDMI_DATA — GMCH_HDMI_DATA A7
DDC_DATA0/AUX0N
DDC_CLK0/AUX0P

STRP_DATA B10
RESERVED G11
AUX_CAL C8
RS780_AUX_CAL — R294 150R2F-1-GP

TXOUT_L0P A22 — GMCH_TXAOUT0+ 19
TXOUT_L0N B22 — GMCH_TXAOUT0- 19
TXOUT_L1P A21 — GMCH_TXAOUT1+ 19
TXOUT_L1N B21 — GMCH_TXAOUT1- 19
TXOUT_L2P B20 — GMCH_TXAOUT2+ 19
TXOUT_L2N A20 — GMCH_TXAOUT2- 19
TXOUT_L3P A19
TXOUT_L3N B19

TXOUT_U0P B18 — GMCH_TXBOUT0+ 19
TXOUT_U0N A18 — GMCH_TXBOUT0- 19
TXOUT_U1P A17 — GMCH_TXBOUT1+ 19
TXOUT_U1N B17 — GMCH_TXBOUT1- 19
TXOUT_U2P D20 — GMCH_TXBOUT2+ 19
TXOUT_U2N D21 — GMCH_TXBOUT2- 19
TXOUT_U3P D18
TXOUT_U3N D19

TXCLK_LP B16 — GMCH_TXACLK+ 19
TXCLK_LN A16 — GMCH_TXACLK- 19
TXCLK_UP D16 — GMCH_TXBCLK+ 19
TXCLK_UN D17 — GMCH_TXBCLK- 19

1D8V_S0 — L34 SBK160808T-221Y-N-GP — 68.00119.111

VDDLTP18 A13 — 1D8V_S0_VDDLP18
VSSLTP18 B13
C649 SC1U10V2KX-1GP DY — C648 SCD1U10V2KX-4GP

VDDLT18_1 A15
VDDLT18_2 B15
VDDLT33_1 A14
VDDLT33_2 B14
1D8V_S0_VDDLT18 — L35 PBY201209T-221Y-N-GP — 68.00206.121

VSSLT1 C14
VSSLT2 D15
VSSLT3 C16
VSSLT4 C18
VSSLT5 C20
VSSLT6 F20
VSSLT7 C22
C652 — C653 SCD1U10V2KX-4GP DY
SC4D7U6D3V3MX-2GP

LVDS_DIGON E9
LVDS_BLON E7 — GMCH_BL_ON
LVDS_ENA_BL G12 — LVDS_ENA_BL — TP26 TPAD14-GP
GMCH_LCDVDD_ON 19
GMCH_BL_ON 35

RN10 — UMA — SRN4K7J-10-GP

TMDS_HPD D9
HPD D10 — NB_DVI_HPD — HDMI_DETECT# 21 — TP24 TPAD14-GP

SUS_STAT# D12 — SUS_STAT# — R29 10KR2J-3-GP — 3D3V_S0

THERMALDIODE_P AE8 — RS780_DXP3_1 — TP23 TPAD14-GP
THERMALDIODE_N AD8 — RS780_DXN3_1 — TP22 TPAD14-GP

TESTMODE D13 — TESTMODE_NB — R347 1K8R2F-GP

RS780 SYMBOL

3D3V_S0 — R19 2K2R2J-2-GP DY — STRP_DATA

35,53 BLON_IN — RN64
19,53 BRIGHTNESS_AMD — SRN0J-10-GP-U — LVDS_ENA_BL — GMCH_BL_ON
UMA

for TR

UMA

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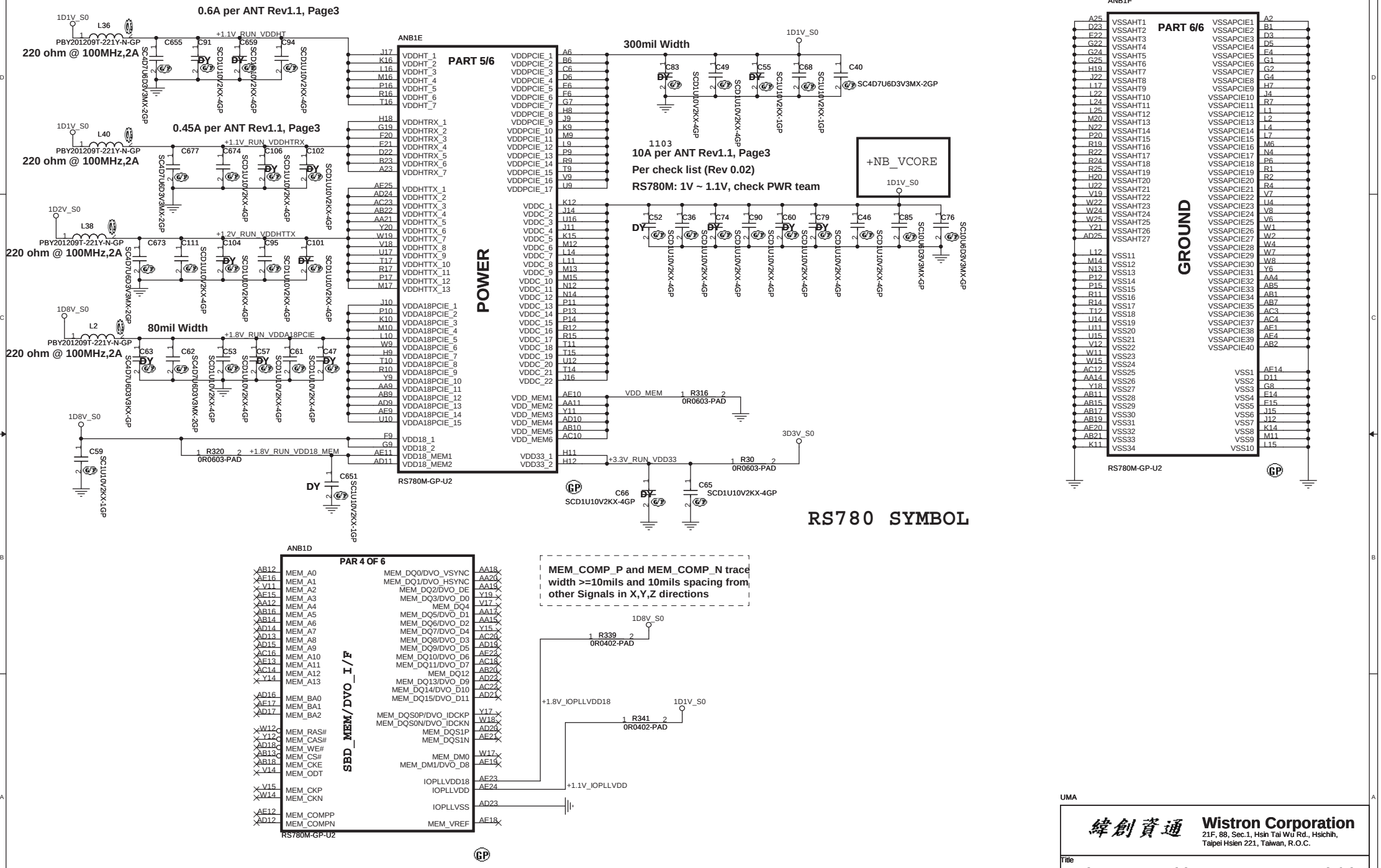
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M LVDS&CRT (2/3)

Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 9 of 61



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-RS880M_Side Port&PWR&GND(3/3)**

Size	Document Number	Rev
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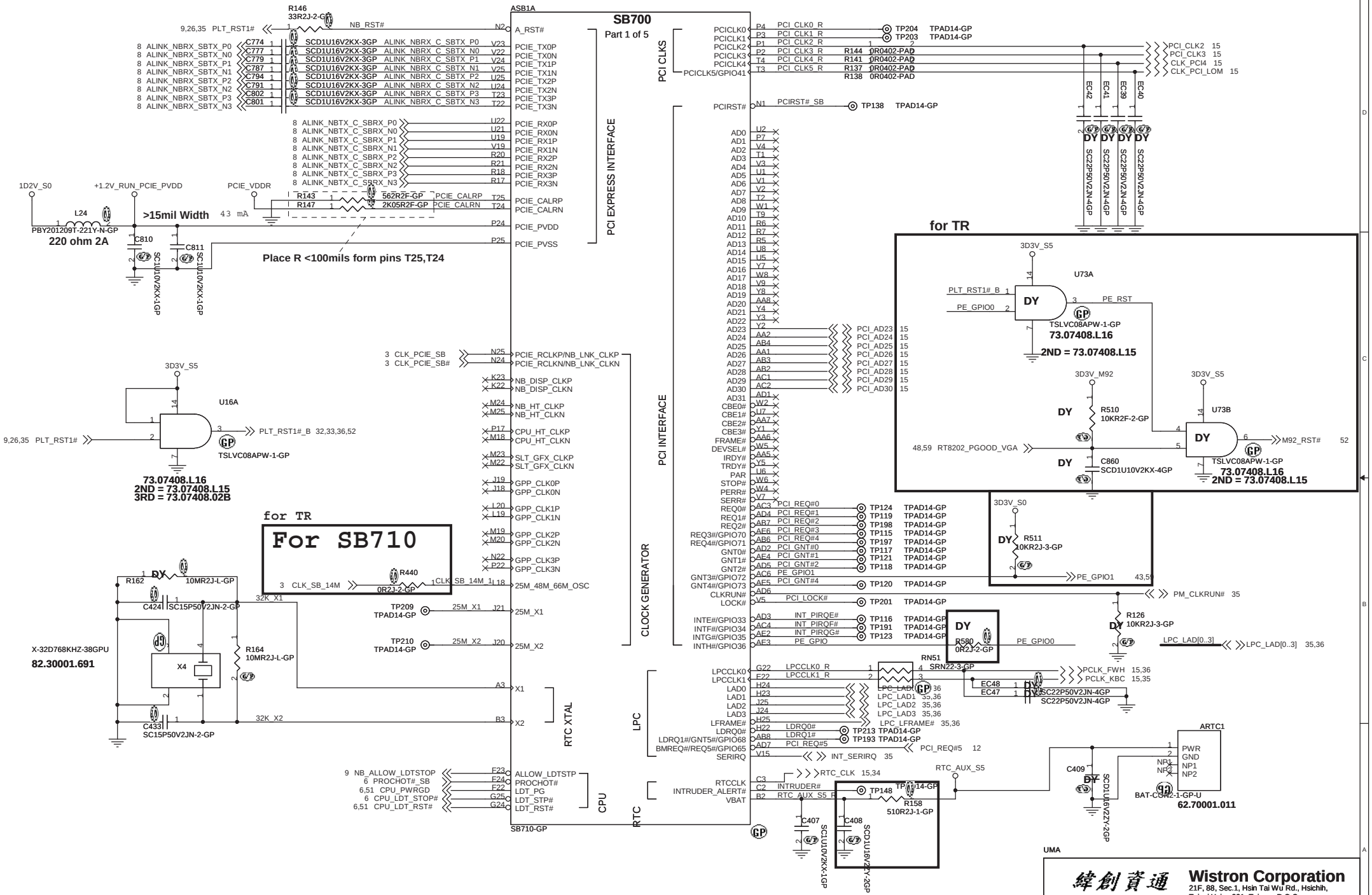
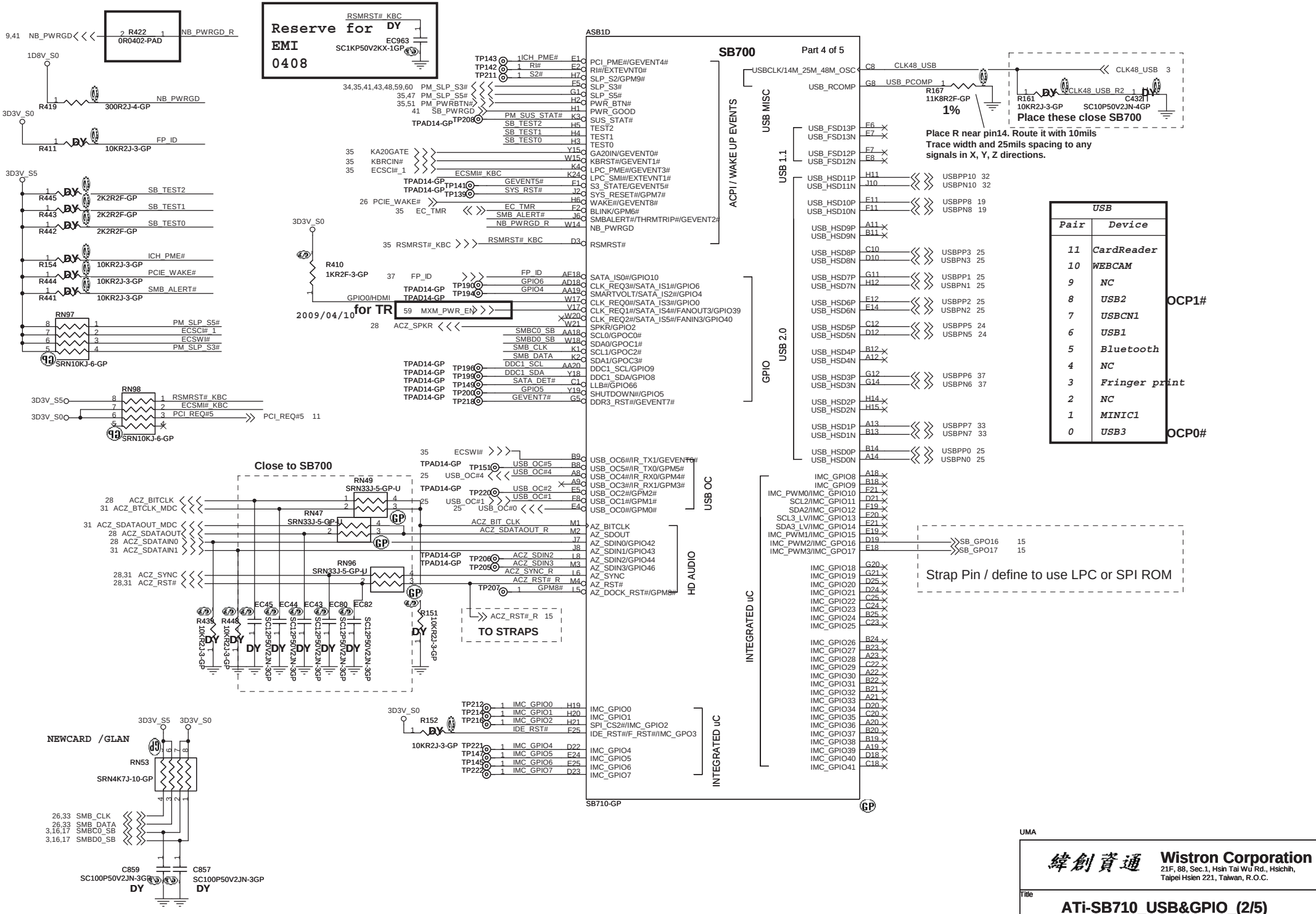
Date: Monday, July 06, 2009 Sheet 10 of 61


SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB710-GP
for TR
For SB710
for TR
>15mil Width
Place R <100mils form pins T25,T24
220 ohm 2A
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
82.30001.691
62.70001.011
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB710 PCIE&PCI (1/5)
JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 11 of 61
http://hobi-elektronika.net



PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD

SATA ODD

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

HW MONITOR

SATA PWR

SB710-GP

Very Close to SB700

XTAL-25MHZ-96GP
82.30020.791
2ND = 82.30020.851

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

2009/04/09 ALL DY

Layout connect to Cap then GND

UMA

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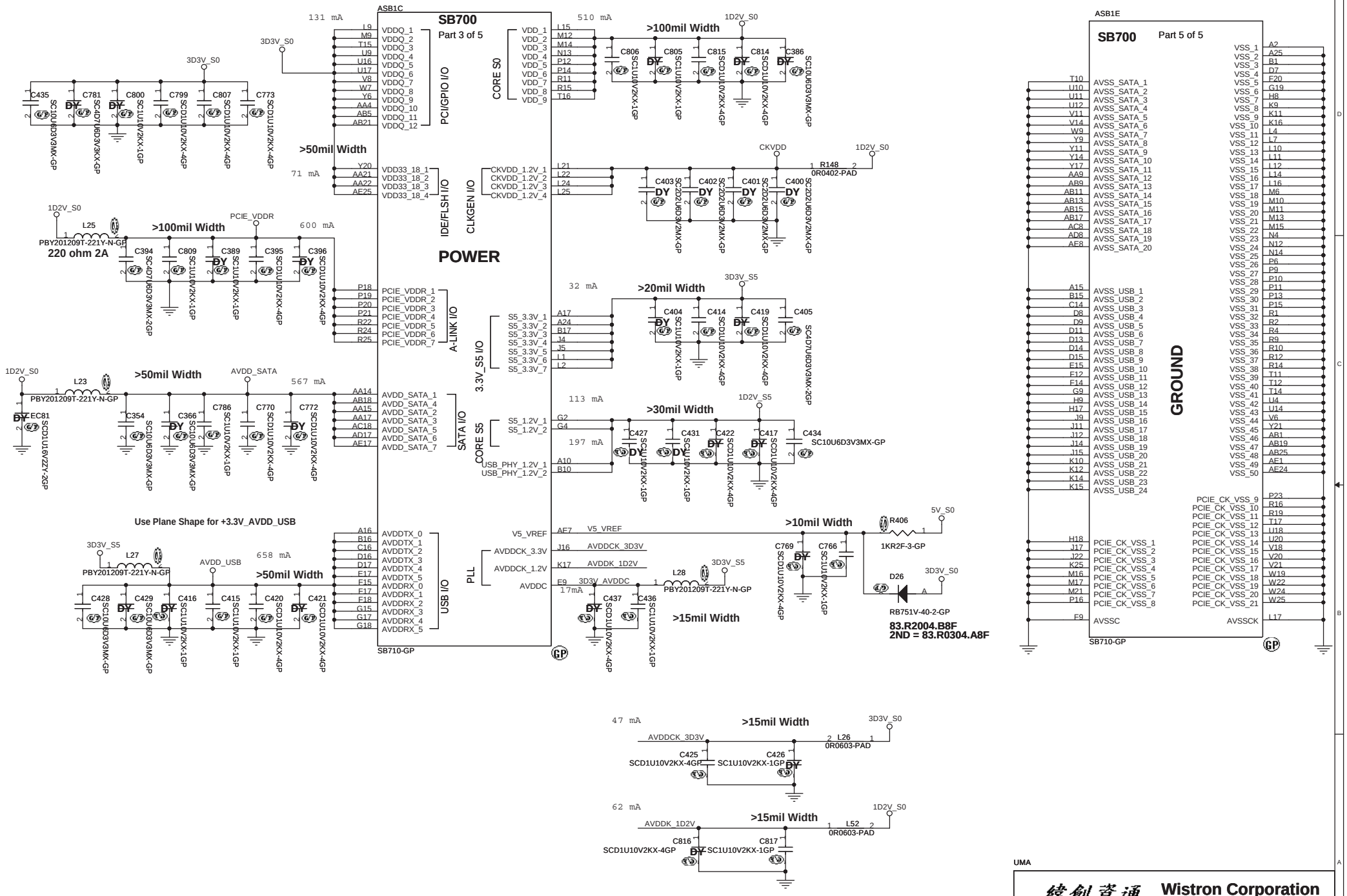
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 SATA-IDE (3/5)

Size: A3 | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 13 of 61



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 POWER&GND (4/5)

Size	Document Number	Rev
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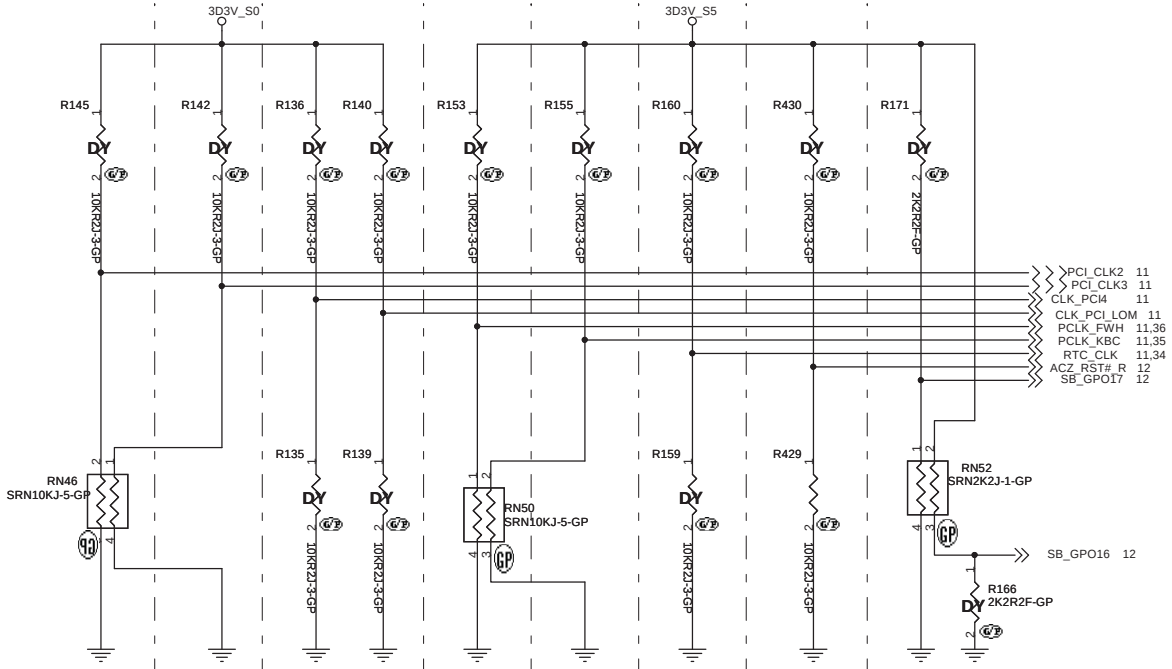
REQUIRED STRAPS

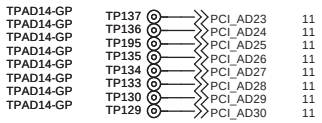
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved
								H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT
								L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

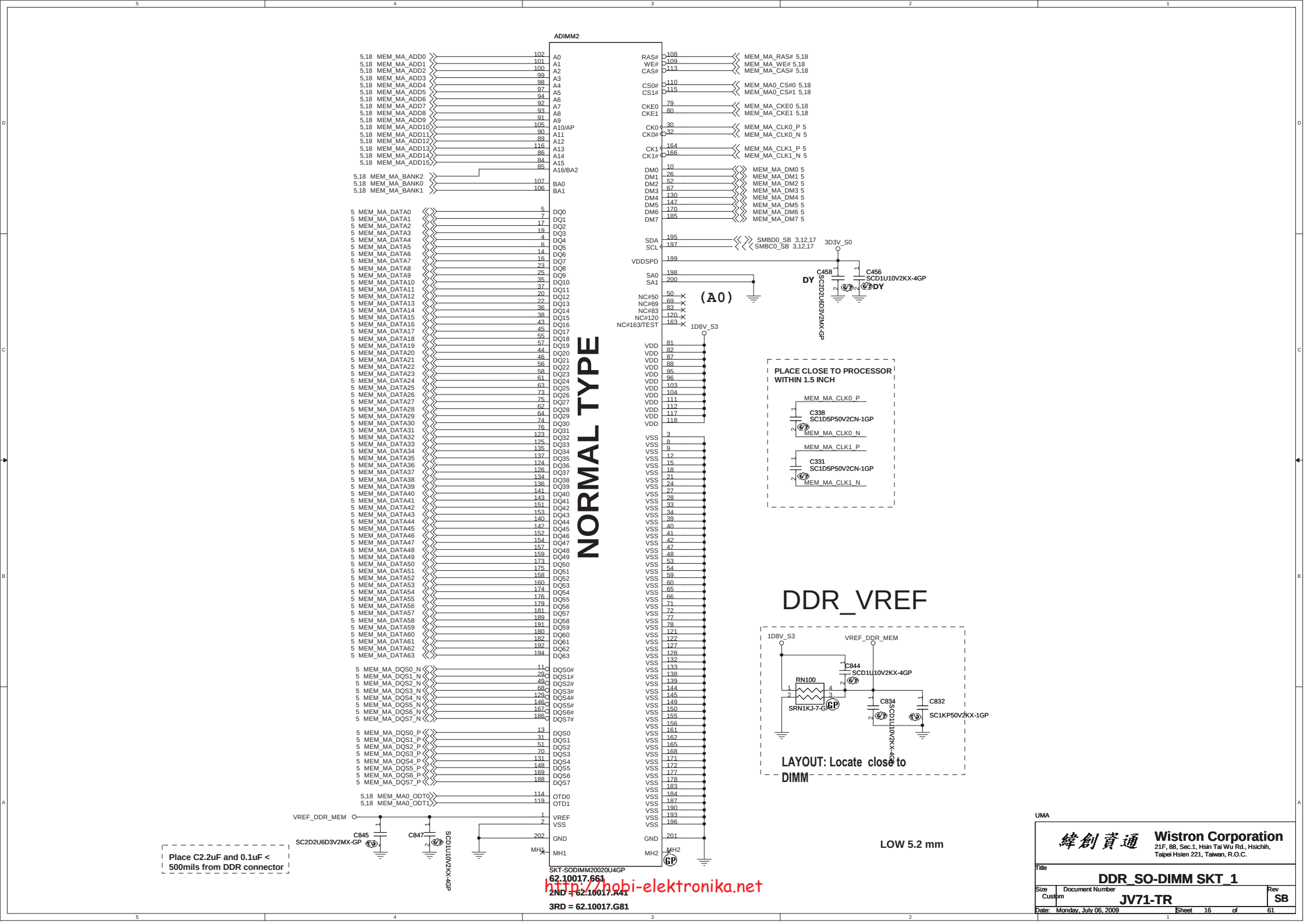
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

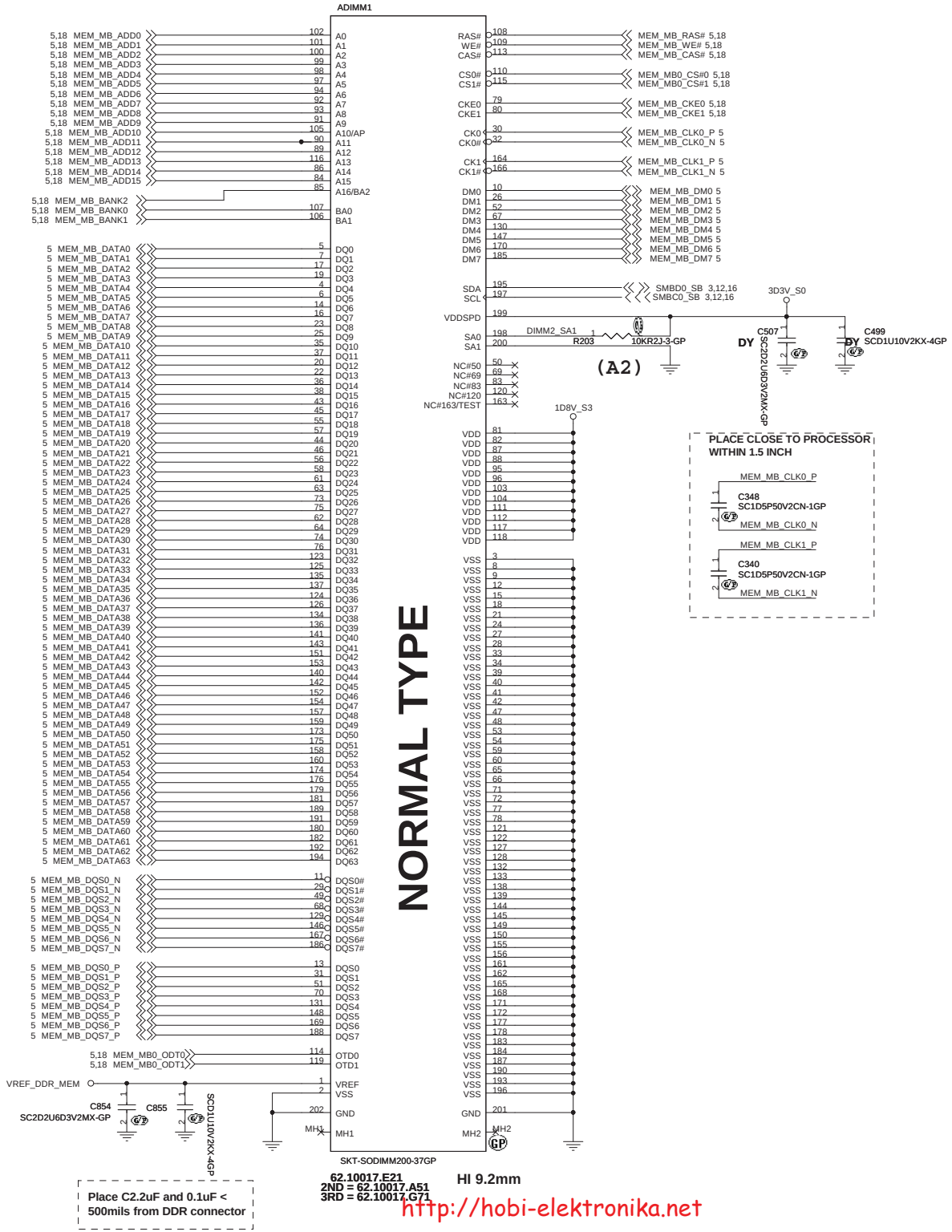
Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 15 of 61



UMA

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR_SO-DIMM SKT_1
Size: Custom	Document Number: JV71-TR
Rev: SB	
Date: Monday, July 06, 2009	Sheet 16 of 61



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

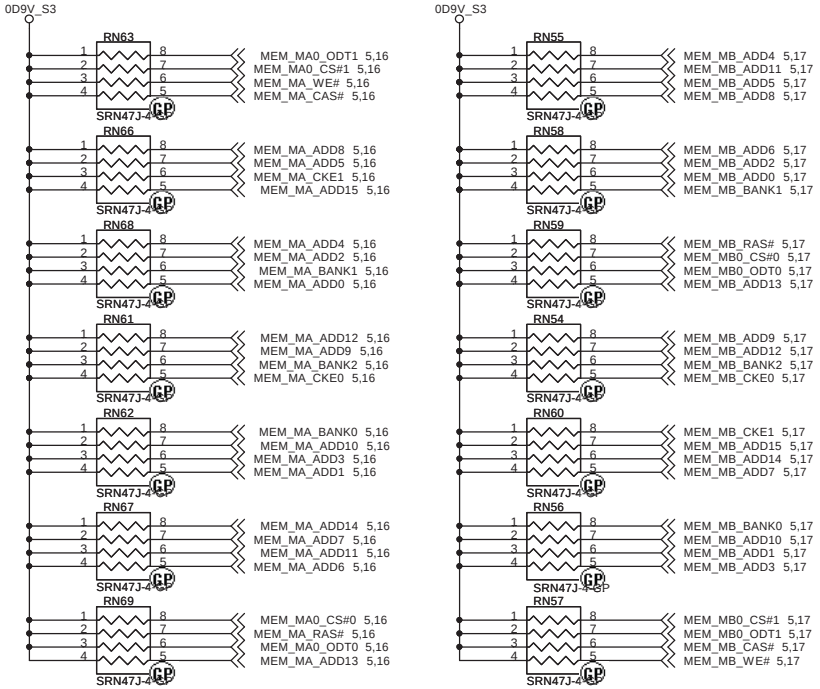
Title: DDR SO-DIMM SKT 2

Size: Custom | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 17 of 61

PARALLEL TERMINATION

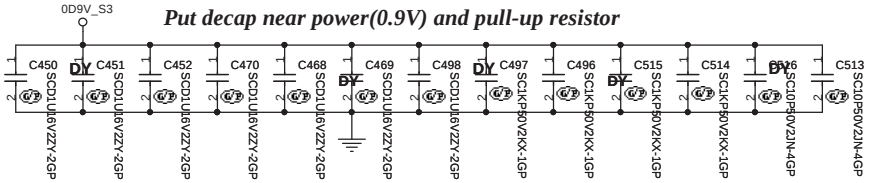
Put decap near power(0.9V) and pull-up resistor



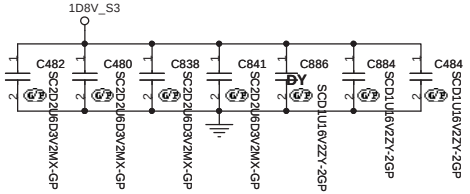
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

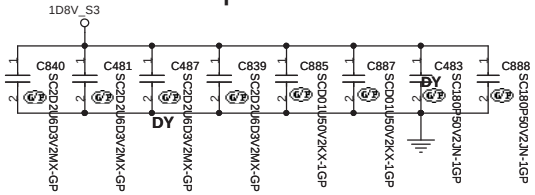


Place these Caps near DM1



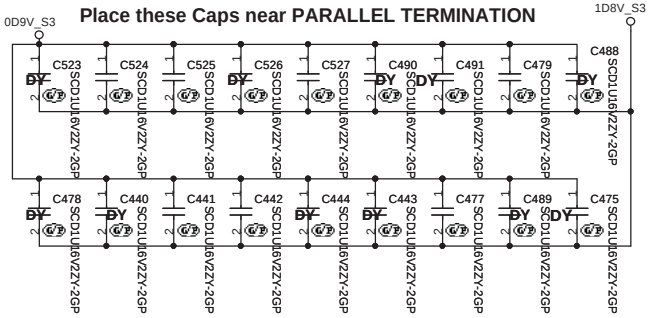
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



UMA

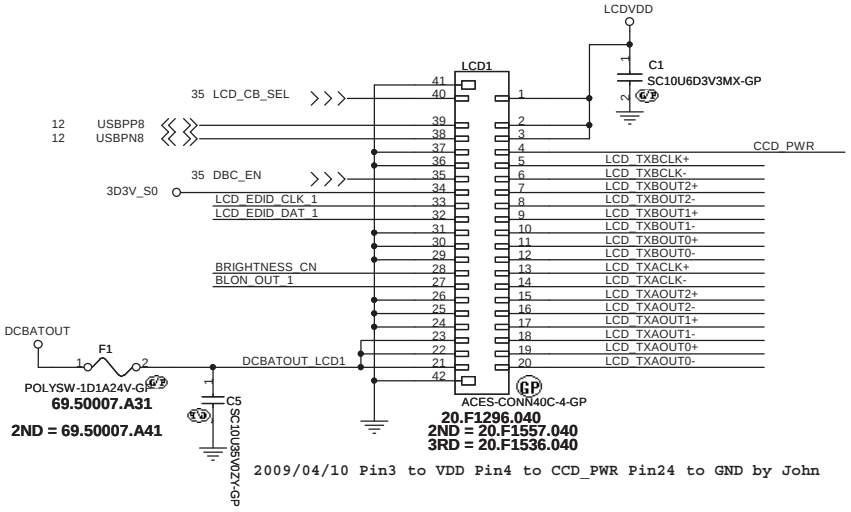
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DAMPING & TERMINATION**

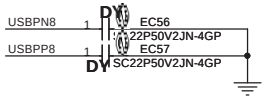
Size	Document Number	Rev
A3	JV71-TR	SB

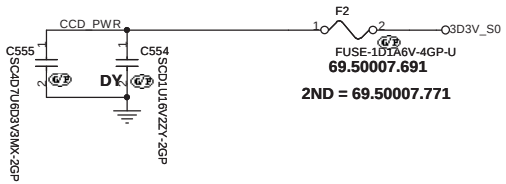
Date: Monday, July 06, 2009 Sheet 18 of 61

LCD/INVERTER/CCD CONN

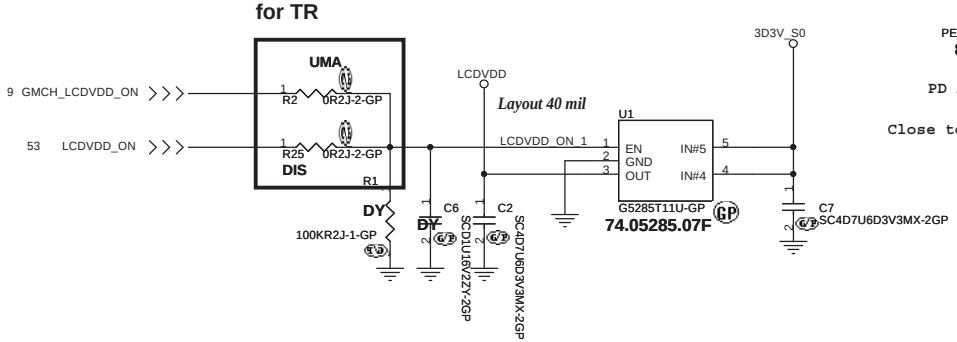


2009/04/10 Pin3 to VDD Pin4 to CCD_PWR Pin24 to GND by John

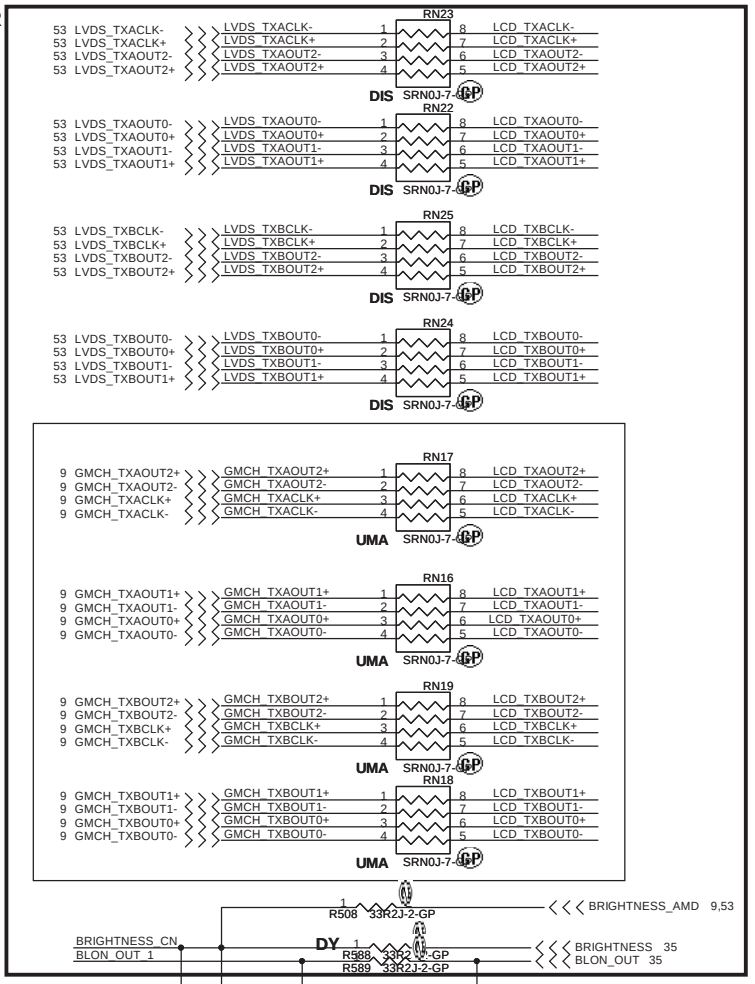


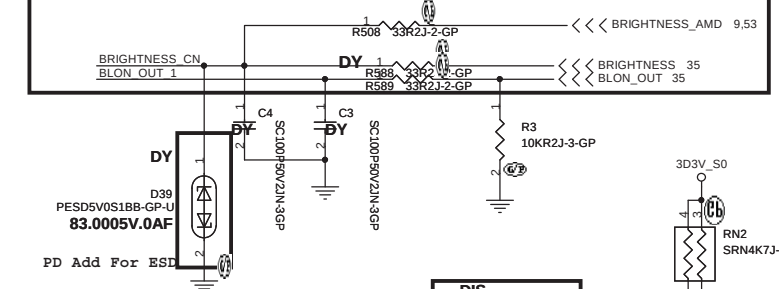


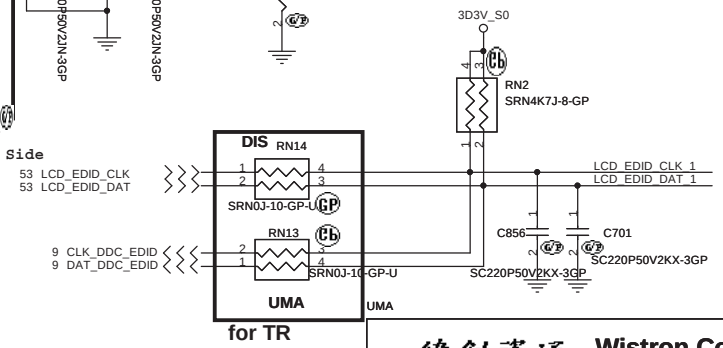
for TR



for TR







Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

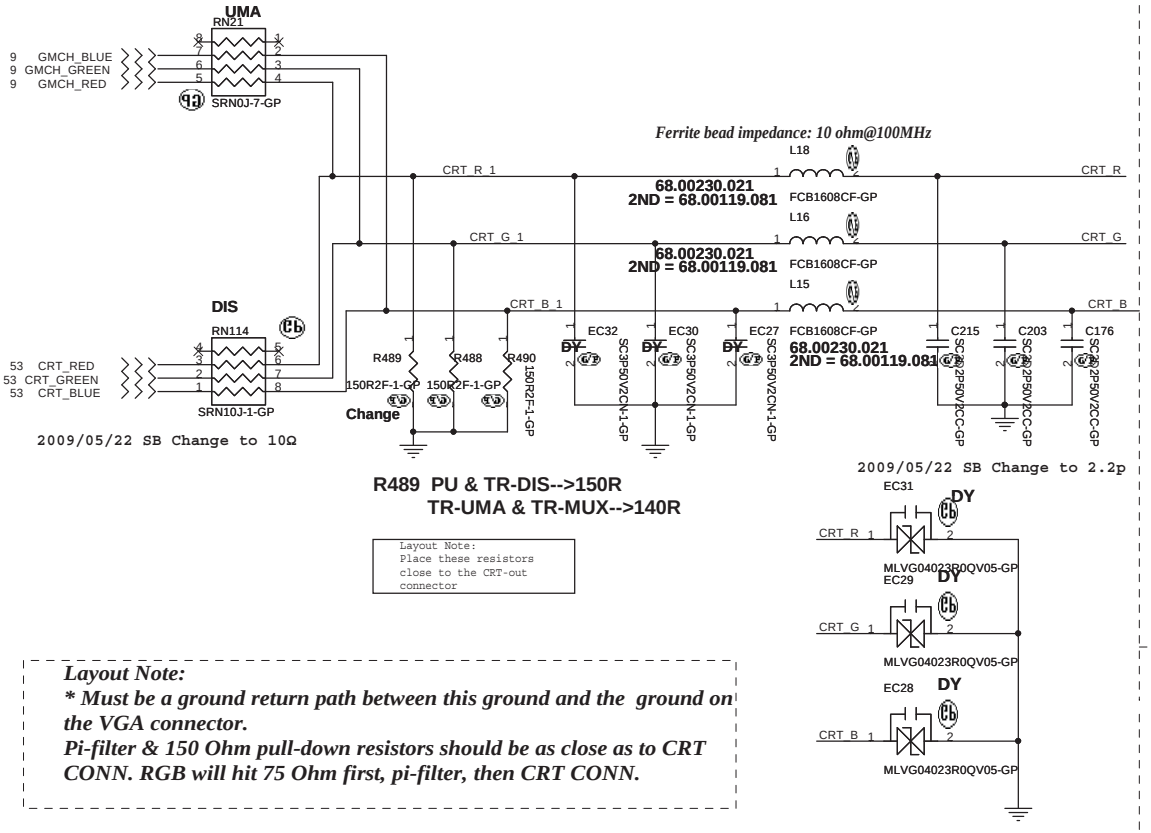
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

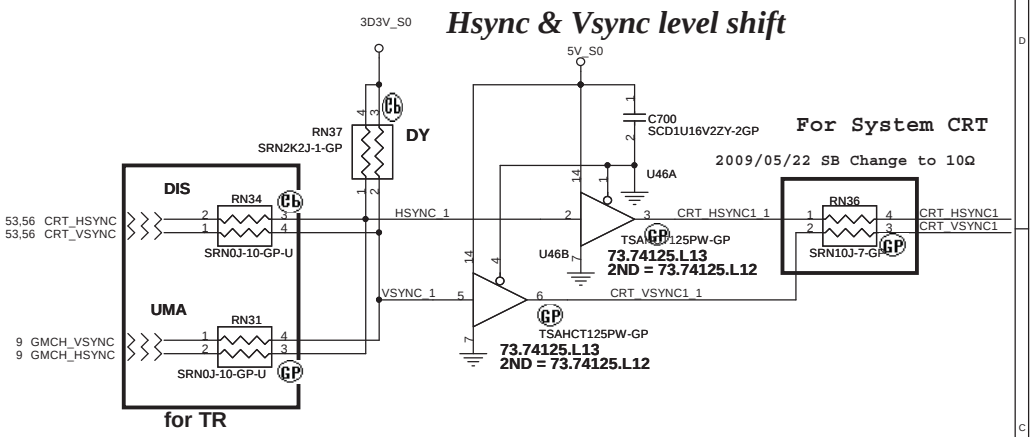
Title: LCD CONN

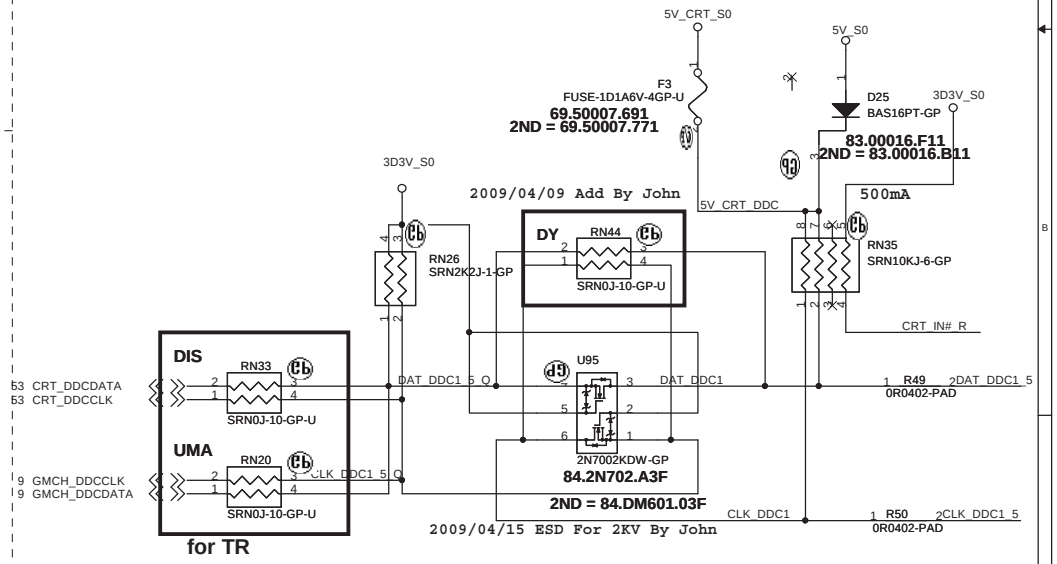
Size: A3 | Document Number: JV71-TR | Rev: -1

Date: Monday, July 06, 2009 | Sheet 19 of 61

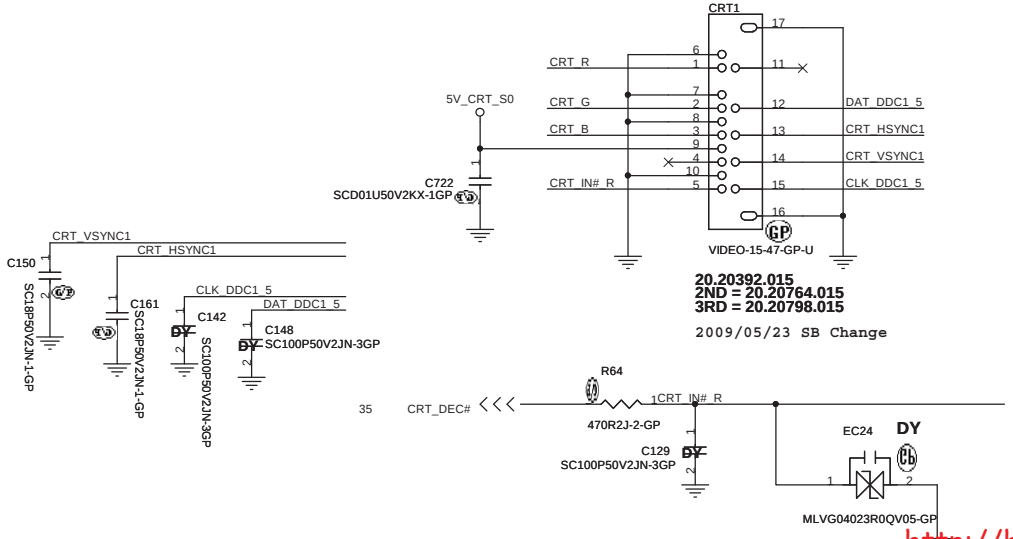


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





CRT I/F & CONNECTOR



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
	JV71-TR	SB

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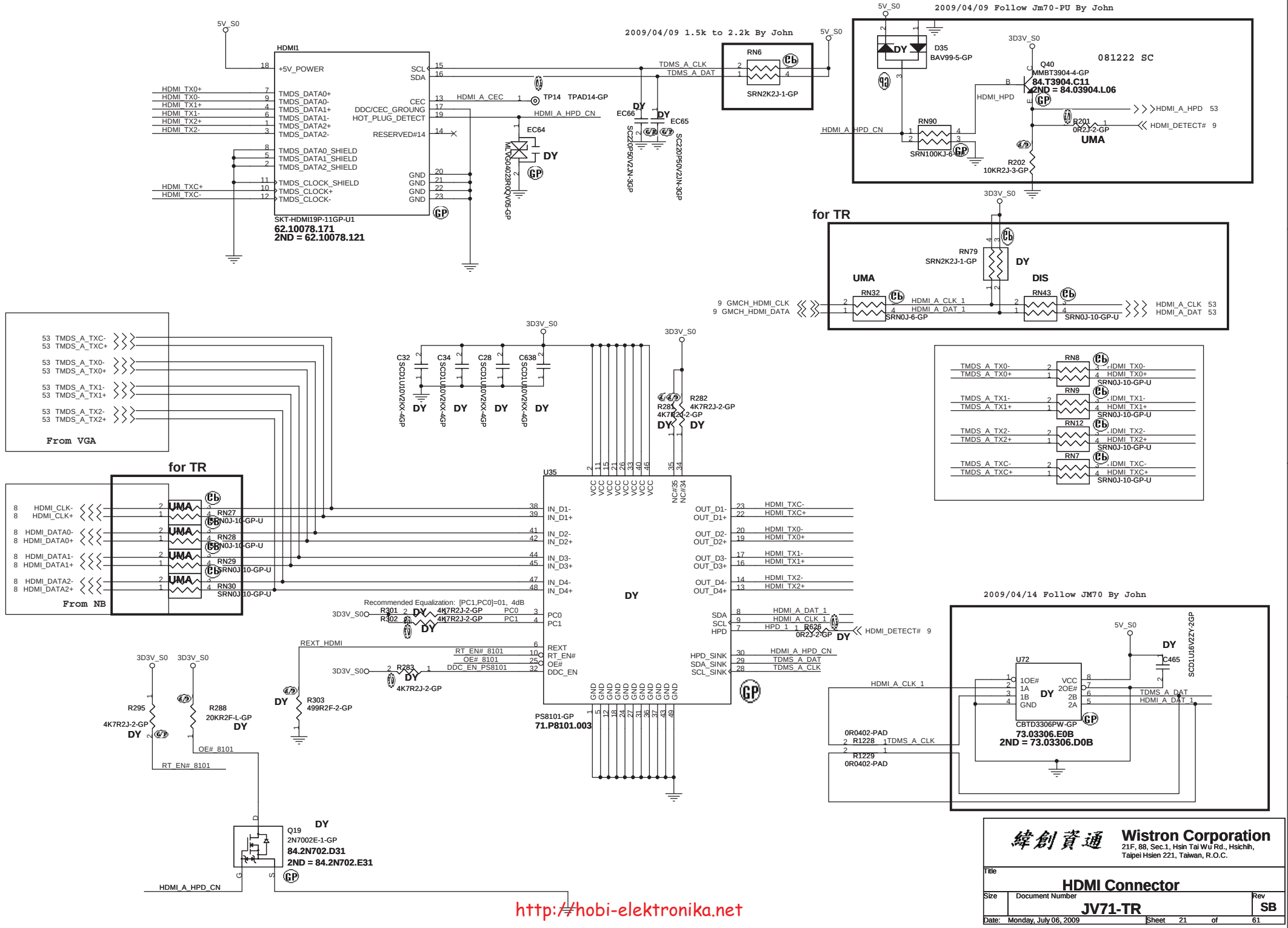
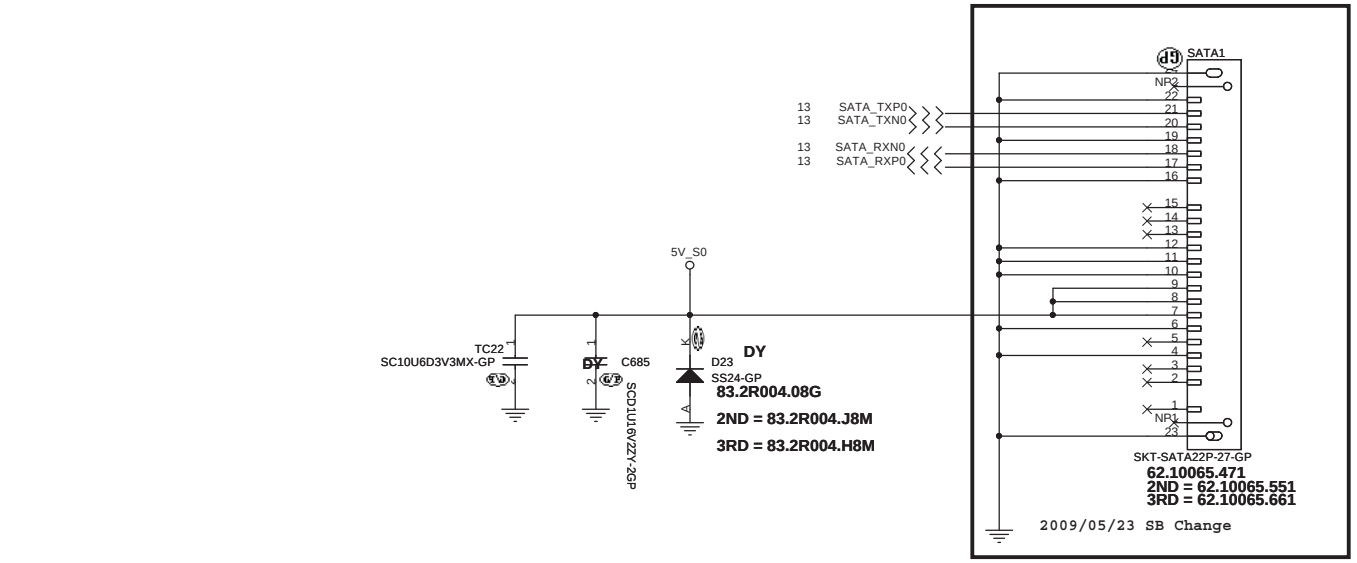
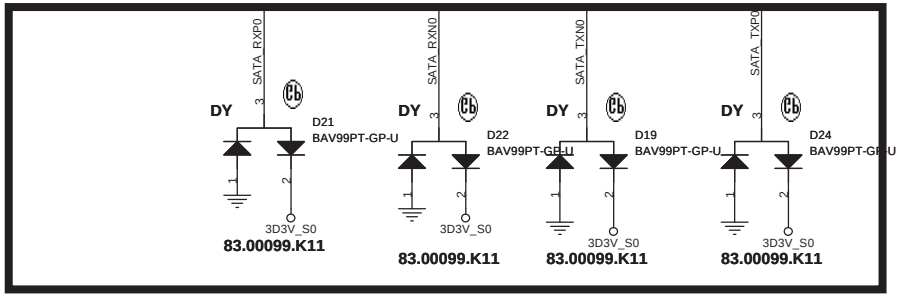


SATA Connector

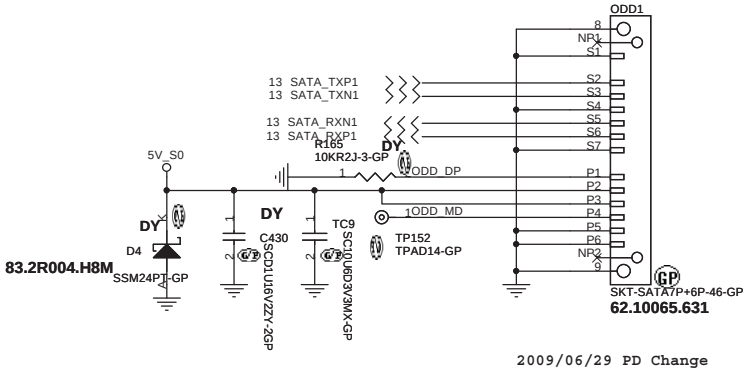


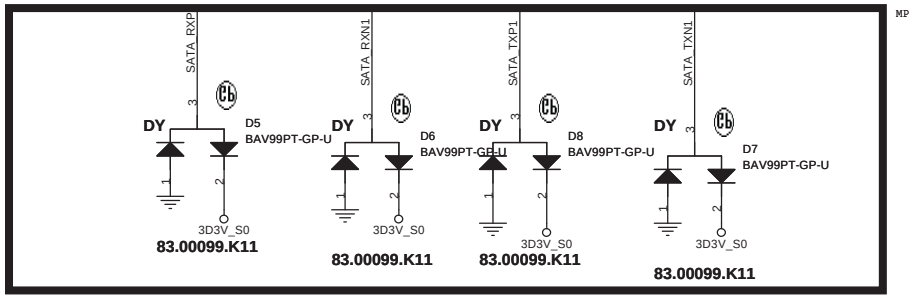


UMA

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HDD
Size	Document Number: JV71-TR
Rev	SB
Date: Monday, July 06, 2009	Sheet 22 of 61

SATA ODD Connector





UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

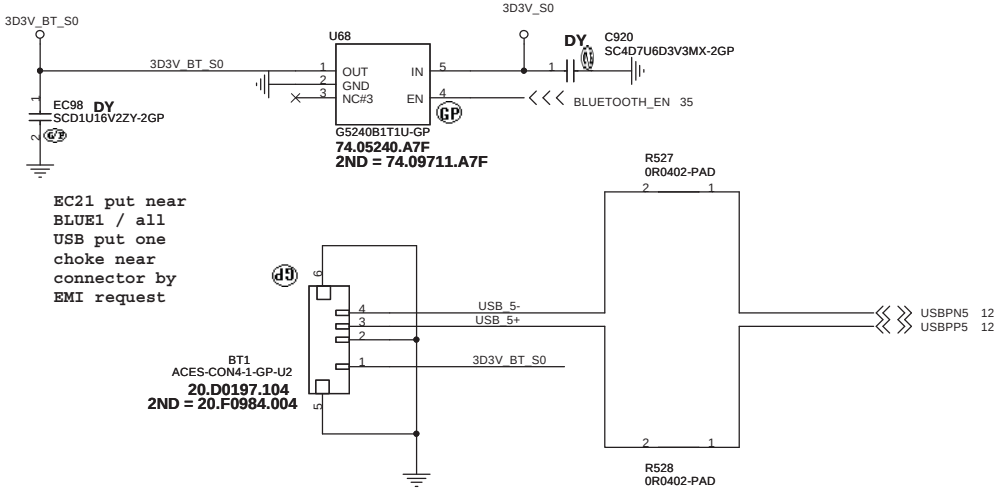
Title: ODD

Size | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 23 of 61

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BLUETOOTH		
Size	Document Number	Rev
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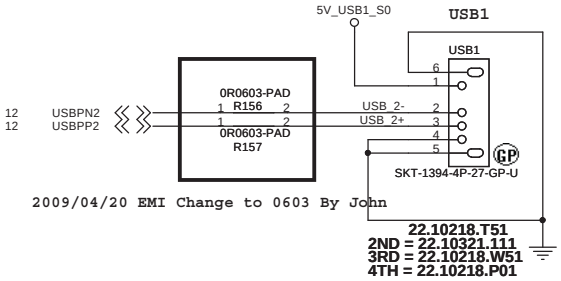
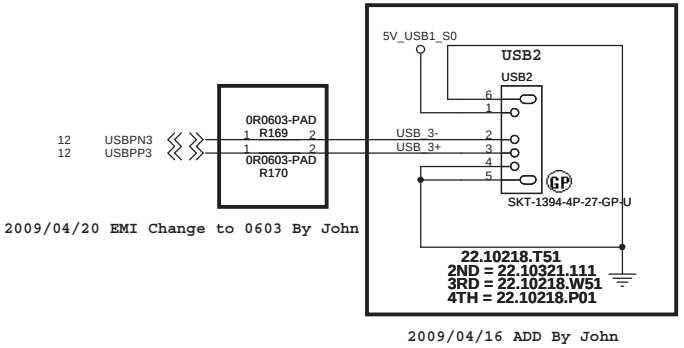
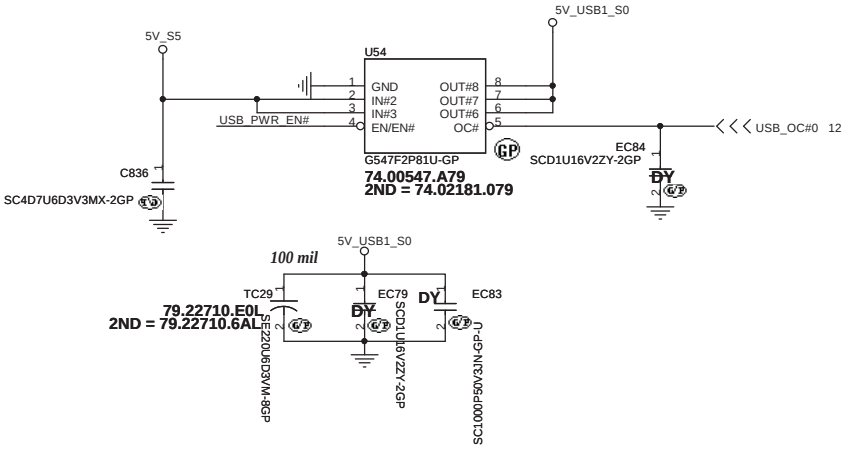
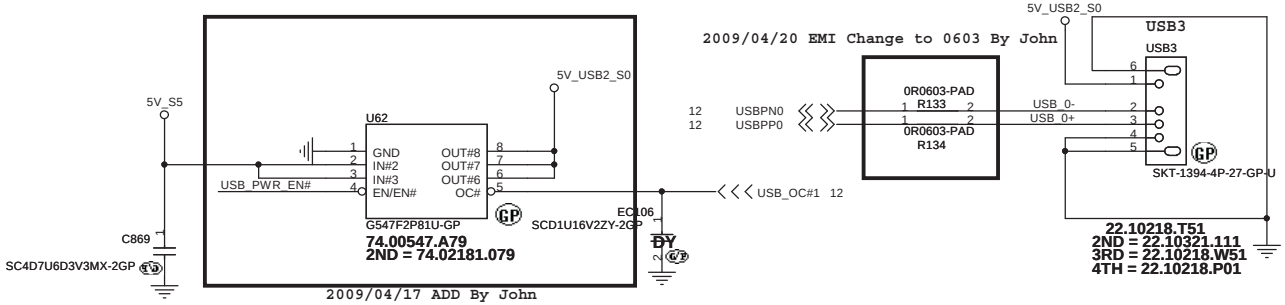
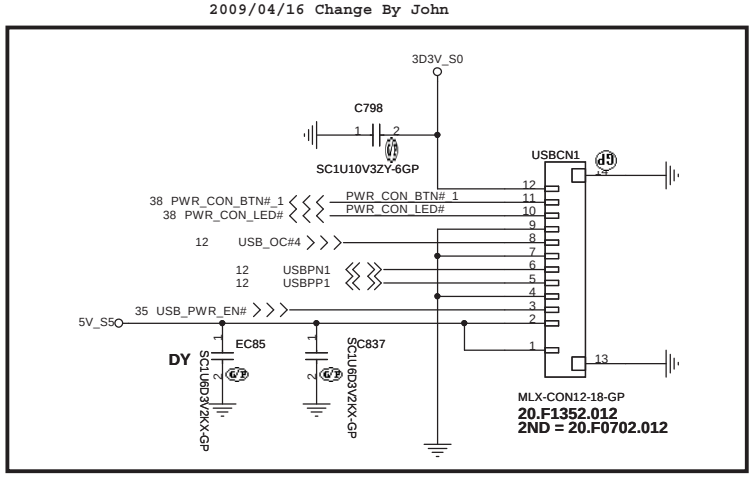
Date: Monday, July 06, 2009	Sheet 24 of 61	

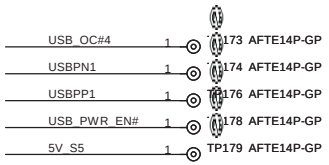


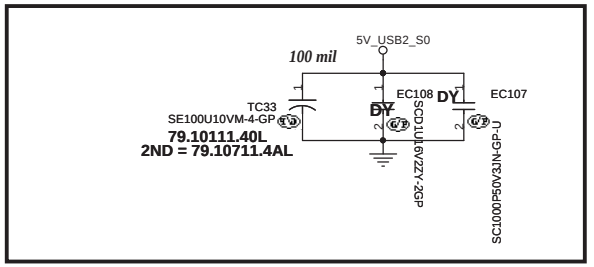








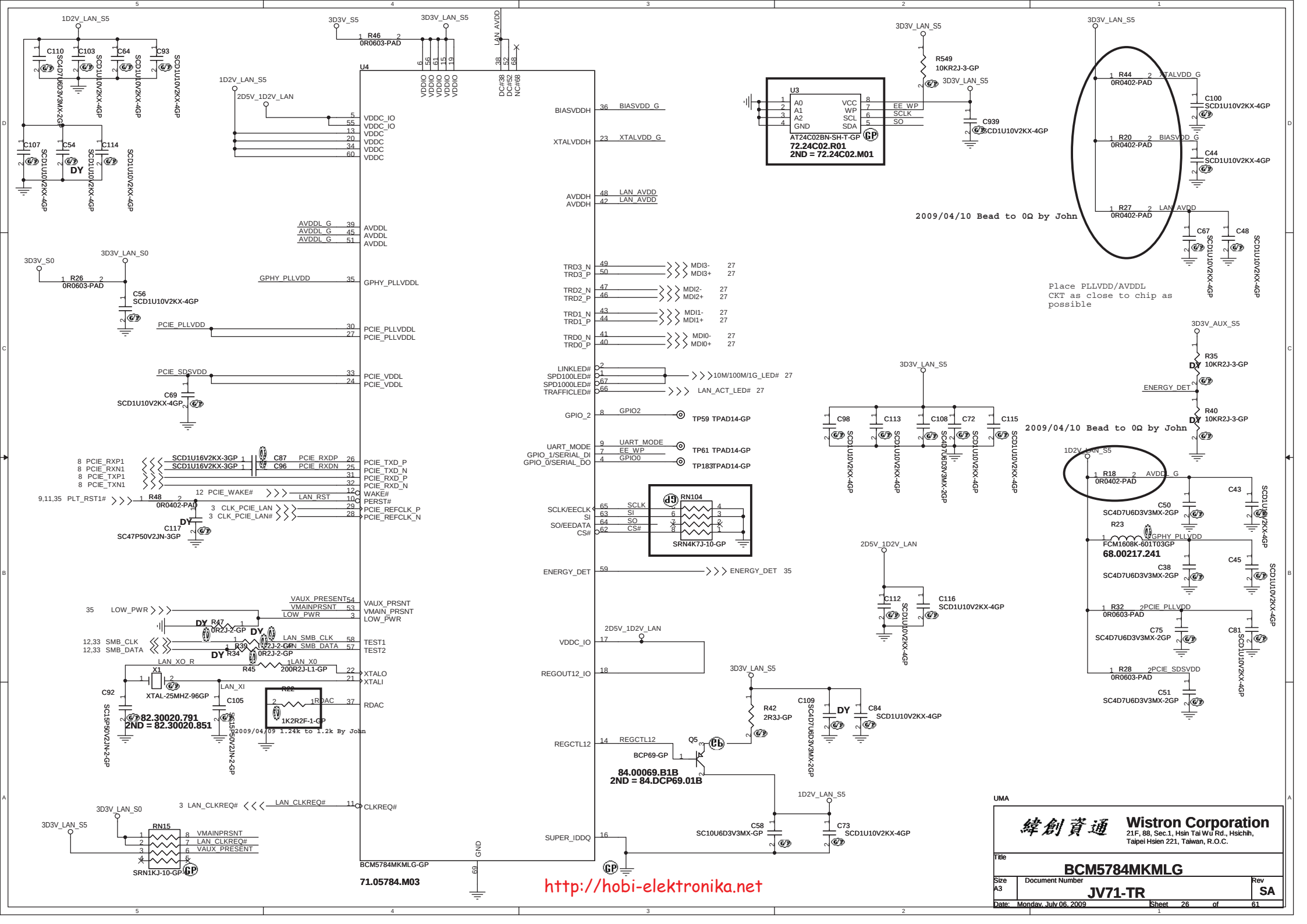




UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB		
Size	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 25 of 61	


U4
BCM5784MKMLG-GP
71.05784.M03
U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
2009/04/10 Bead to 0Ω by John
Place PLLVDD/AVDDL
CKT as close to chip as
possible
2009/04/10 Bead to 0Ω by John
82.30020.791
2ND = 82.30020.851
2009/04/09 1.24k to 1.2k By John
84.00069.B1B
2ND = 84.DCP69.01B
SRN4K7J-10-GP
SRN1KJ-10-GP
http://hobi-elektronika.net
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5784MKMLG
Size A3
Document Number JV71-TR
Rev SA
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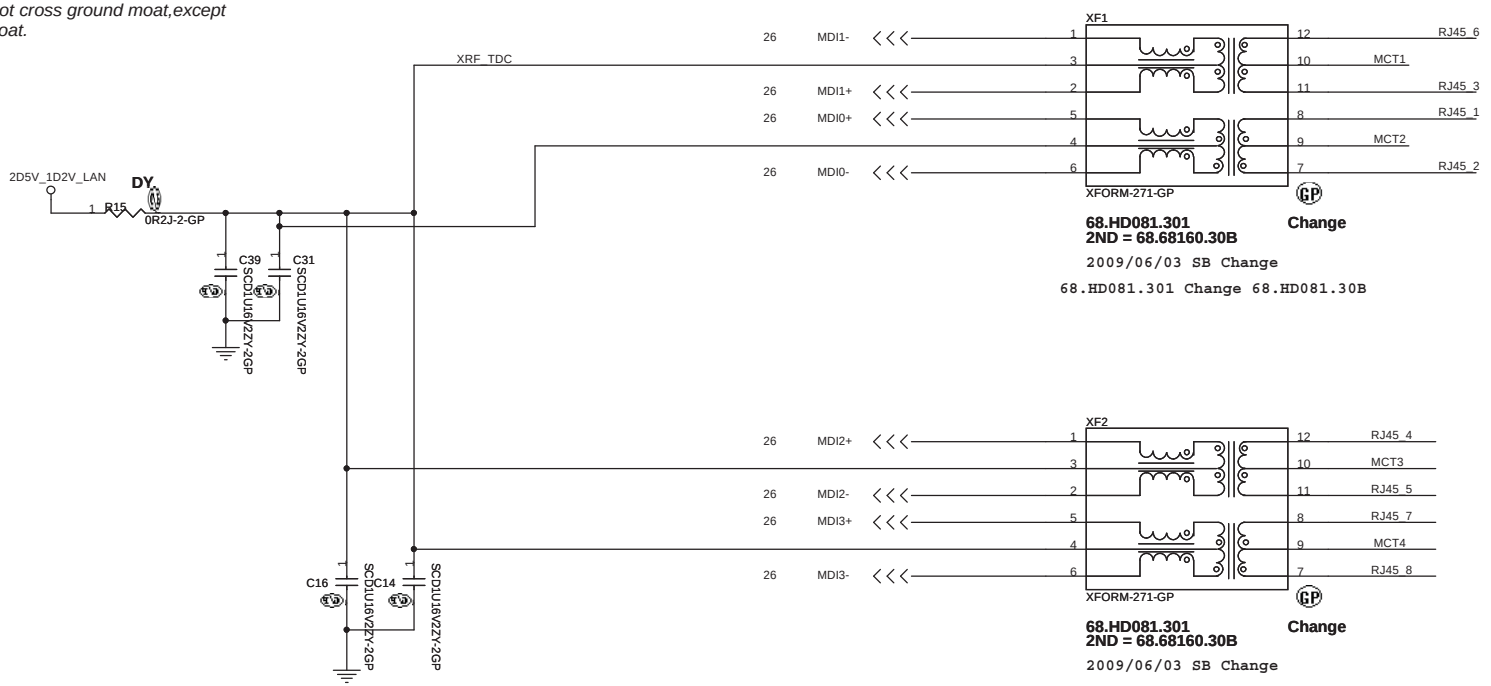
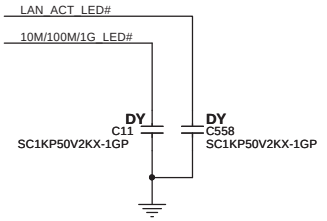
LAN Connector

GIGA Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

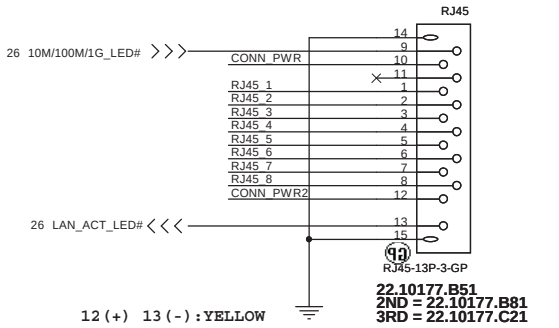




DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

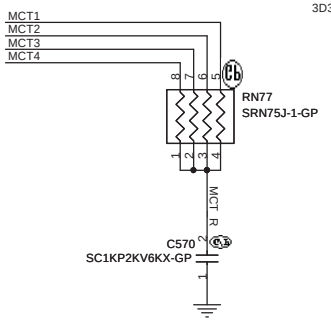
10(+) 9(-)::GREEN
10(+) 11(-):ORANGE

LAN Connector



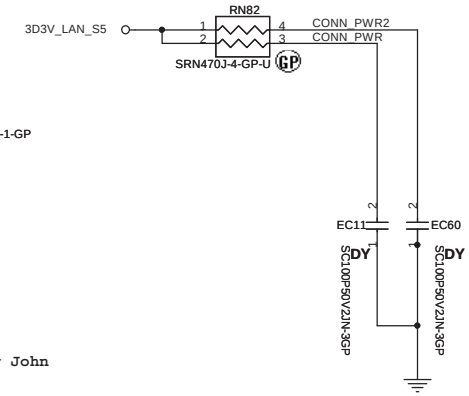
12(+) 13(-):YELLOW

2009/05/23 SB Change



2009/04/09 Follow JV70-PU By John

2009/04/09 Change 4P2R By John



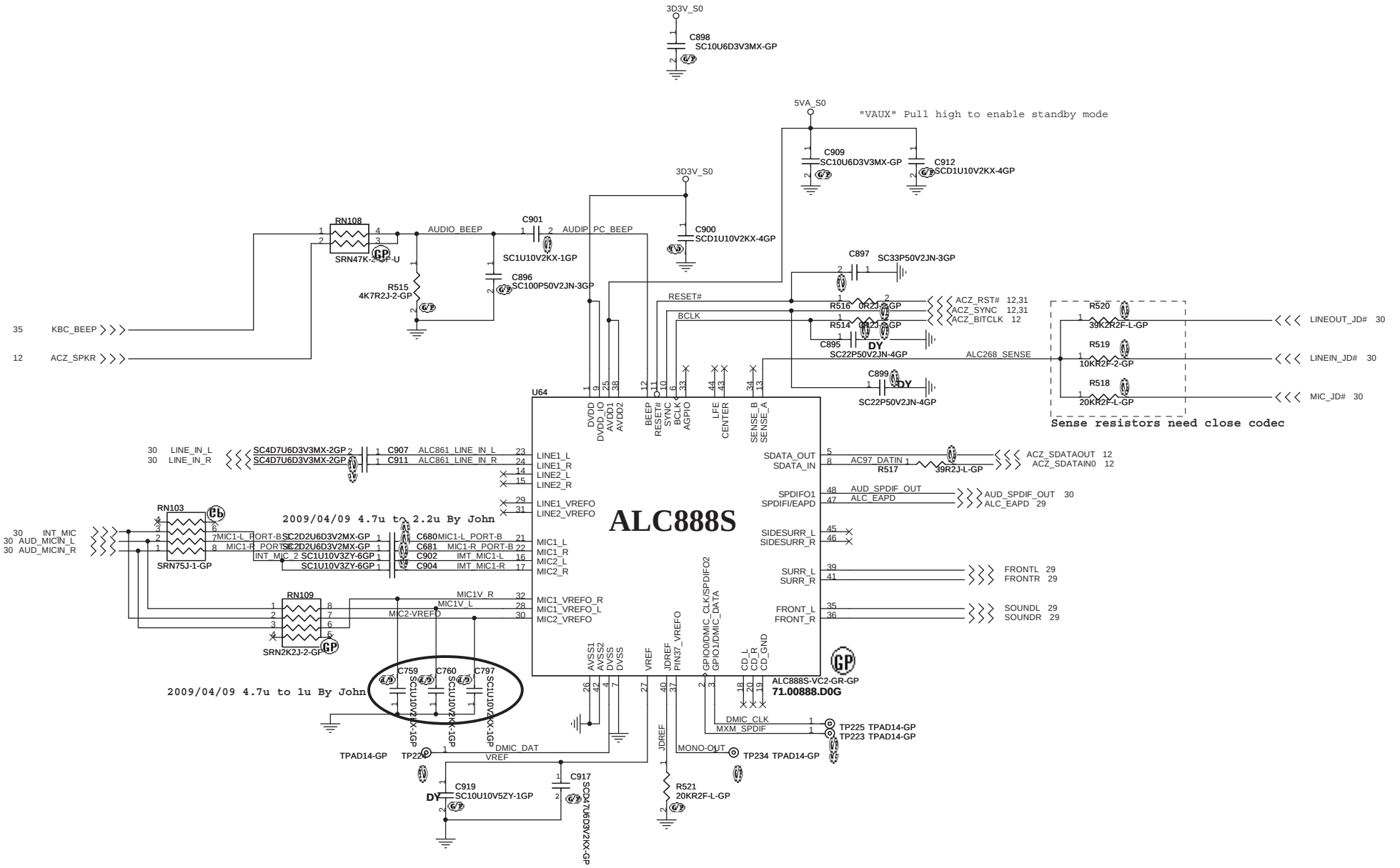
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

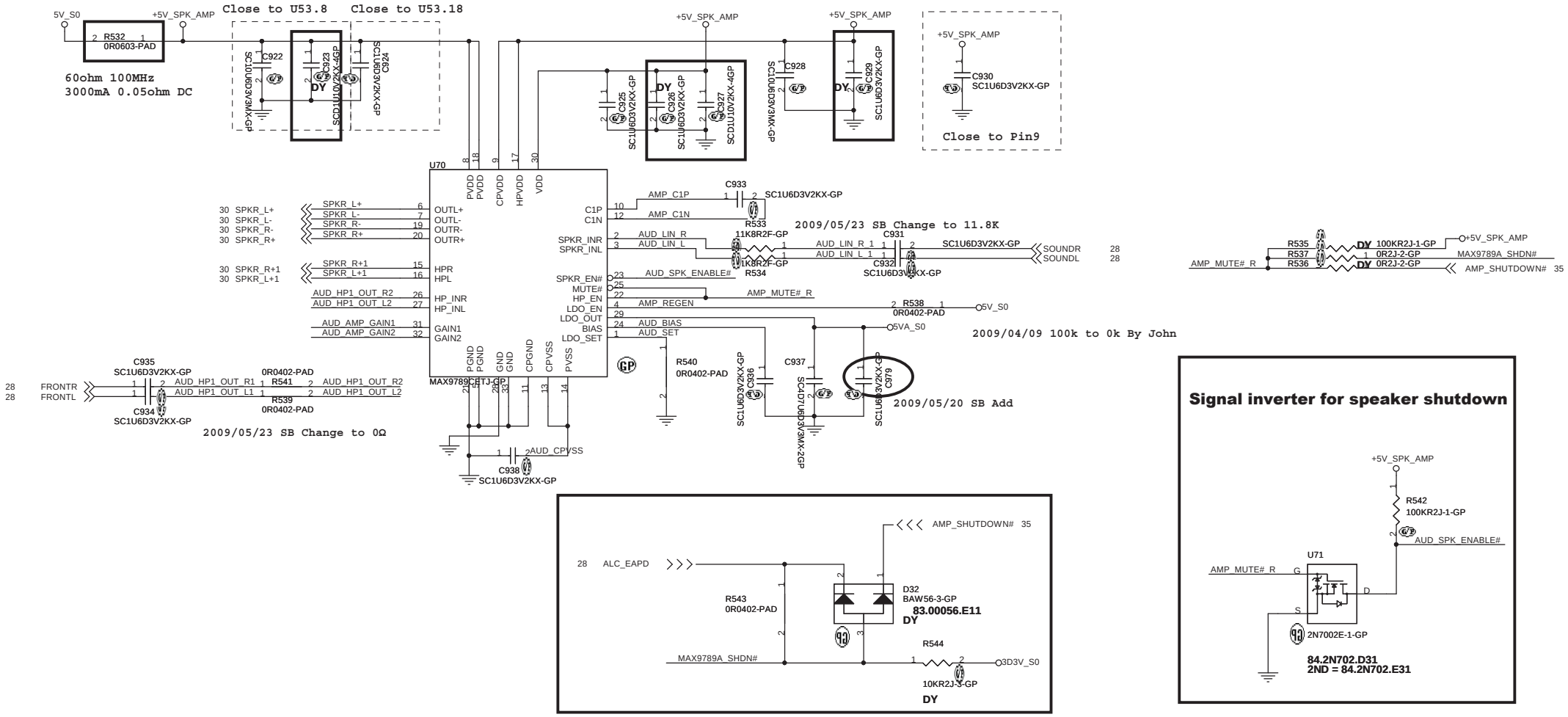
Size: A3 | Document Number: JV71-TR | Rev: SB

Date: Friday, July 10, 2009 | Sheet 27 of 61



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Azalia codec ALC888		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 28 of 61	


Close to U53.8
Close to U53.18
5V_S0
+5V_SPK_AMP
R532
0R0603-PAD
60ohm 100MHz
3000mA 0.05ohm DC
C922
C923
DY
C924
C925
C926
C927
C928
C929
C930
SC1U6D3V2KX-GP
Close to Pin9
U70
MAX9789CBTJ-GP
PVDD
CPVDD
HPVDD
VDD
PGND
GND
CPGND
CPVSS
PVSS
OUTL+
OUTL-
OUTR-
OUTR+
HPR
HPL
HP_INR
HP_INL
GAIN1
GAIN2
C1P
C1N
SPKR_INR
SPKR_INL
MUTE#
HP_EN
LDO_EN
LDO_OUT
BIAS
LDO_SET
SPKR_L+
SPKR_L-
SPKR_R-
SPKR_R+
SPKR_R+1
SPKR_L+1
AUD_HP1_OUT_R2
AUD_HP1_OUT_L2
AUD_AMP_GAIN1
AUD_AMP_GAIN2
AMP_C1P
AMP_C1N
AUD_LIN_R
AUD_LIN_L
AUD_SPK_ENABLE#
AMP_MUTE#_R
AMP_REGEN
AUD_BIAS
AUD_SET
AUD_CPVSS
C933
R533
11K8R2F-GP
R534
1K8R2F-GP
C931
C932
SOUNDR
SOUNDL
2009/05/23 SB Change to 11.8K
R535
R537
R536
100KR2J-1-GP
0R2J-2-GP
MAX9789A_SHDN#
AMP_SHUTDOWN#
R538
0R0402-PAD
5V_S0
5VA_S0
2009/04/09 100k to 0k By John
C935
C934
R541
R539
FRONTR
FRONTL
AUD_HP1_OUT_R1
AUD_HP1_OUT_L1
2009/05/23 SB Change to 0Ω
R540
C936
C937
C979
2009/05/20 SB Add
C938
Signal inverter for speaker shutdown
R542
100KR2J-1-GP
AUD_SPK_ENABLE#
U71
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
ALC_EAPD
R543
D32
BAW56-3-GP
83.00056.E11
R544
10KR2J-3-GP
3D3V_S0
GAIN SETTING
R545
100KR2J-1-GP
R546
100KR2J-1-GP
R547
100KR2J-1-GP
R548
100KR2J-1-GP
GAIN1
GAIN2
GAIN
0
6dB
10dB
15.6dB
21.6dB
http://hobi-elektronika.net
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
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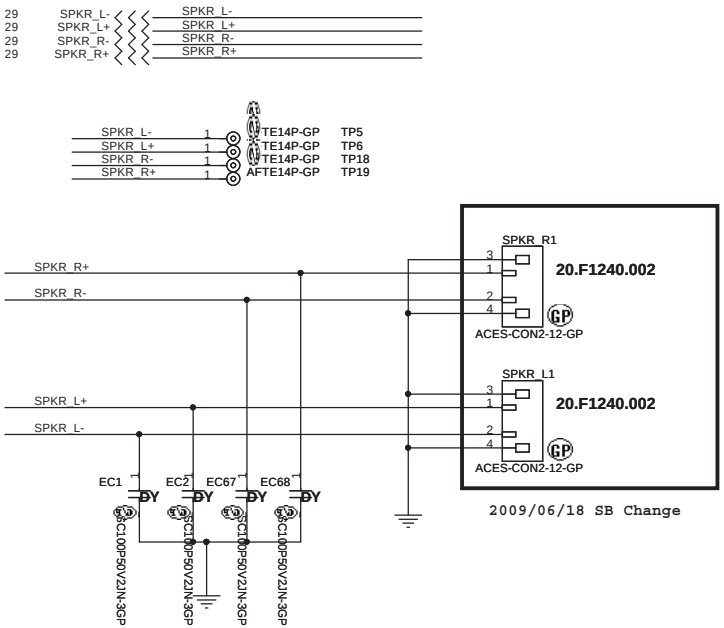
Internal Speaker



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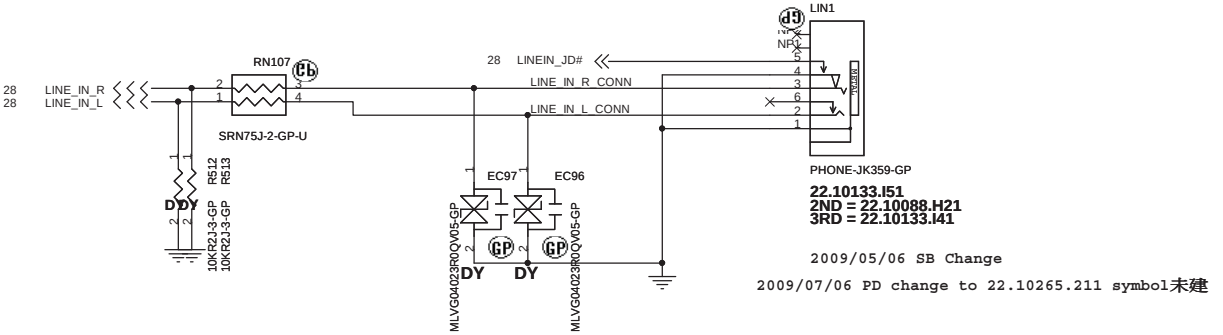
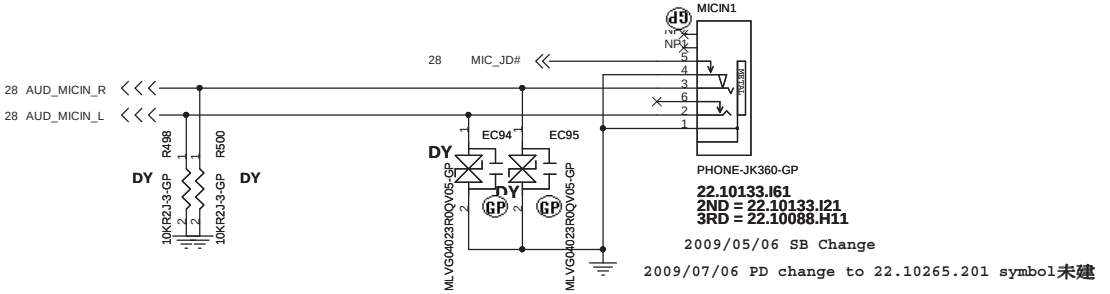


MIC IN



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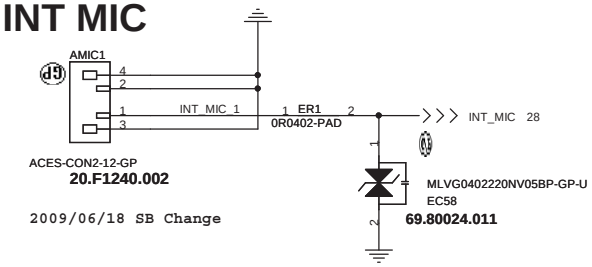

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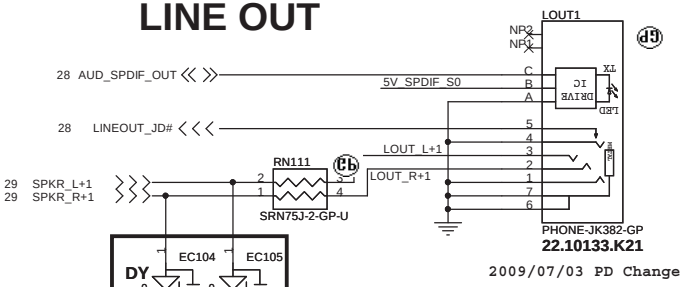

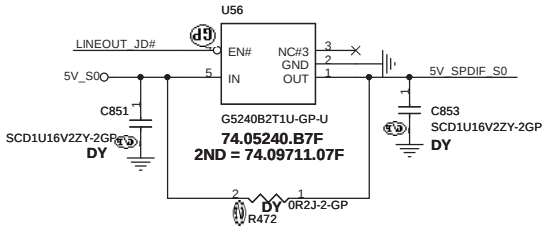

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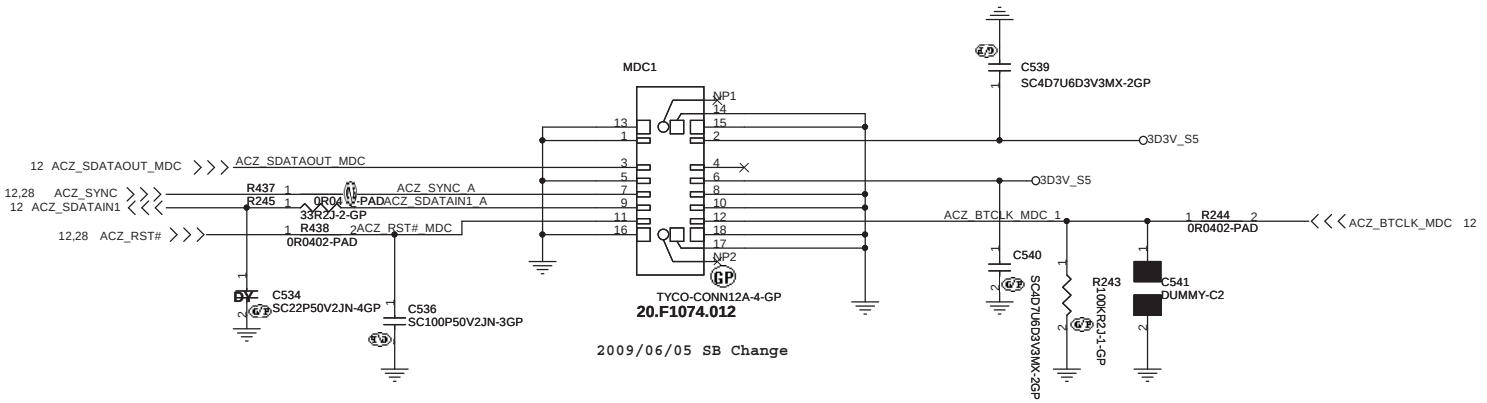
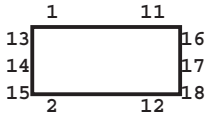
MDC 1.5 CONN





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MDC		
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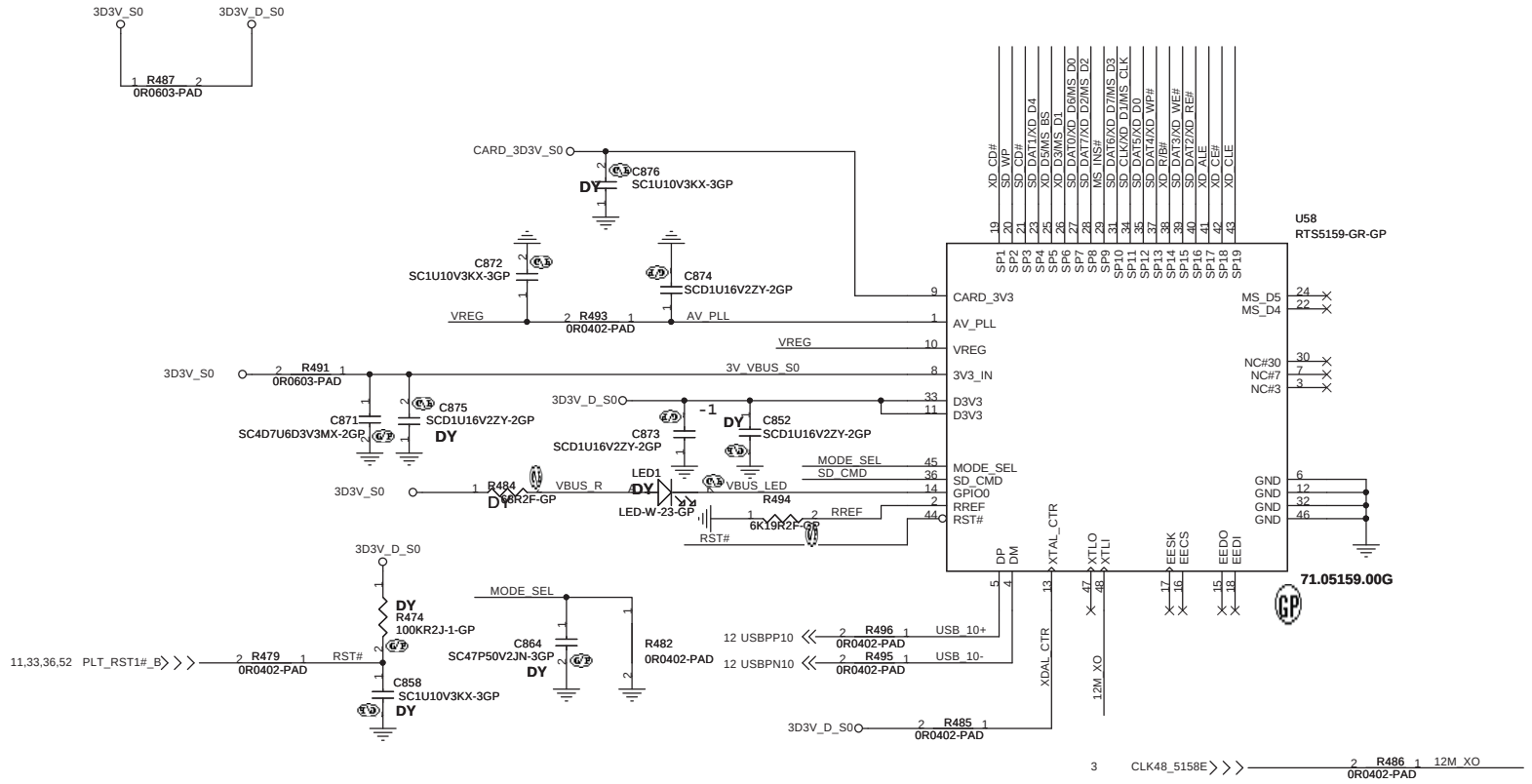
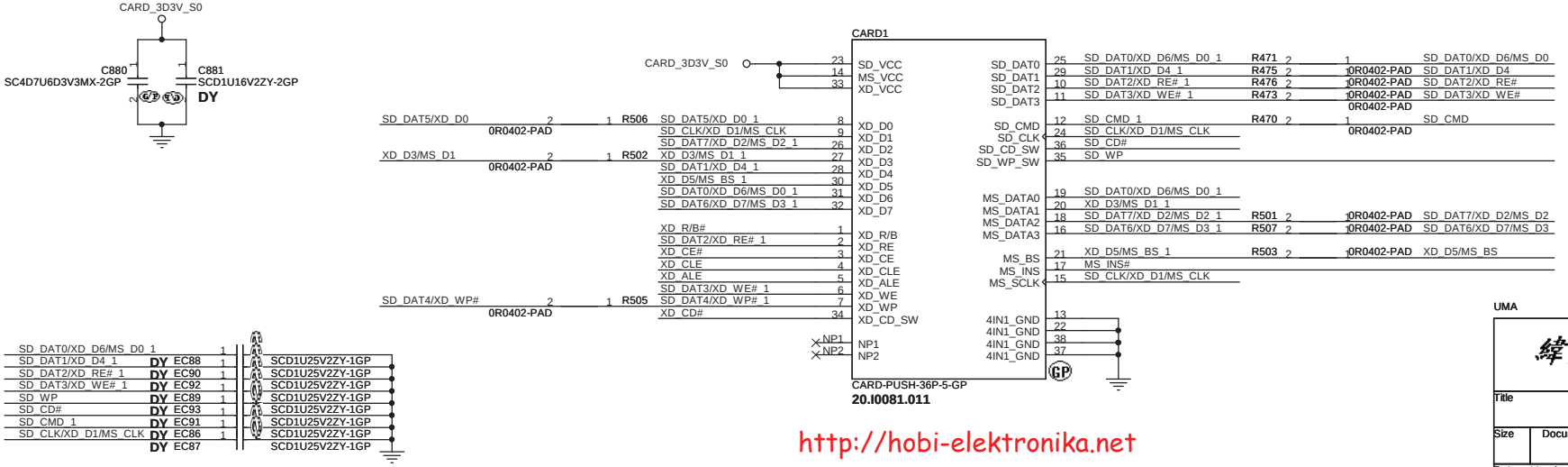


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



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Title	**CARDREADER- RTS5159**
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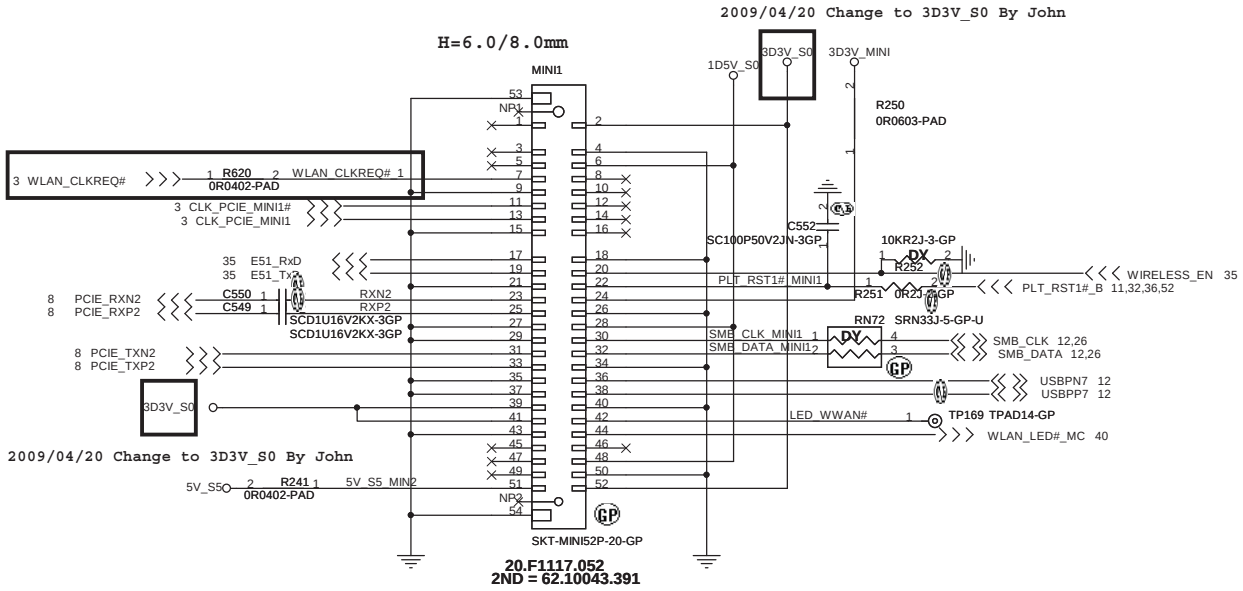
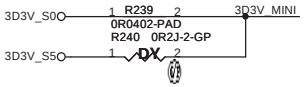
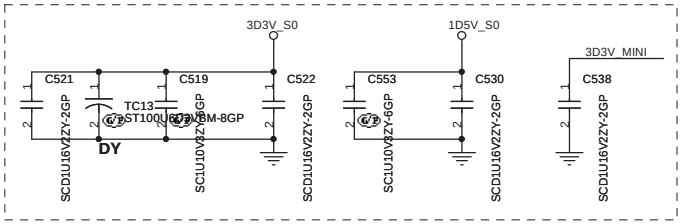
Mini Card Connector(WLAN)





Place near MINI1



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Taipei Hsien 221, Taiwan, R.O.C.

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MINI CARD		
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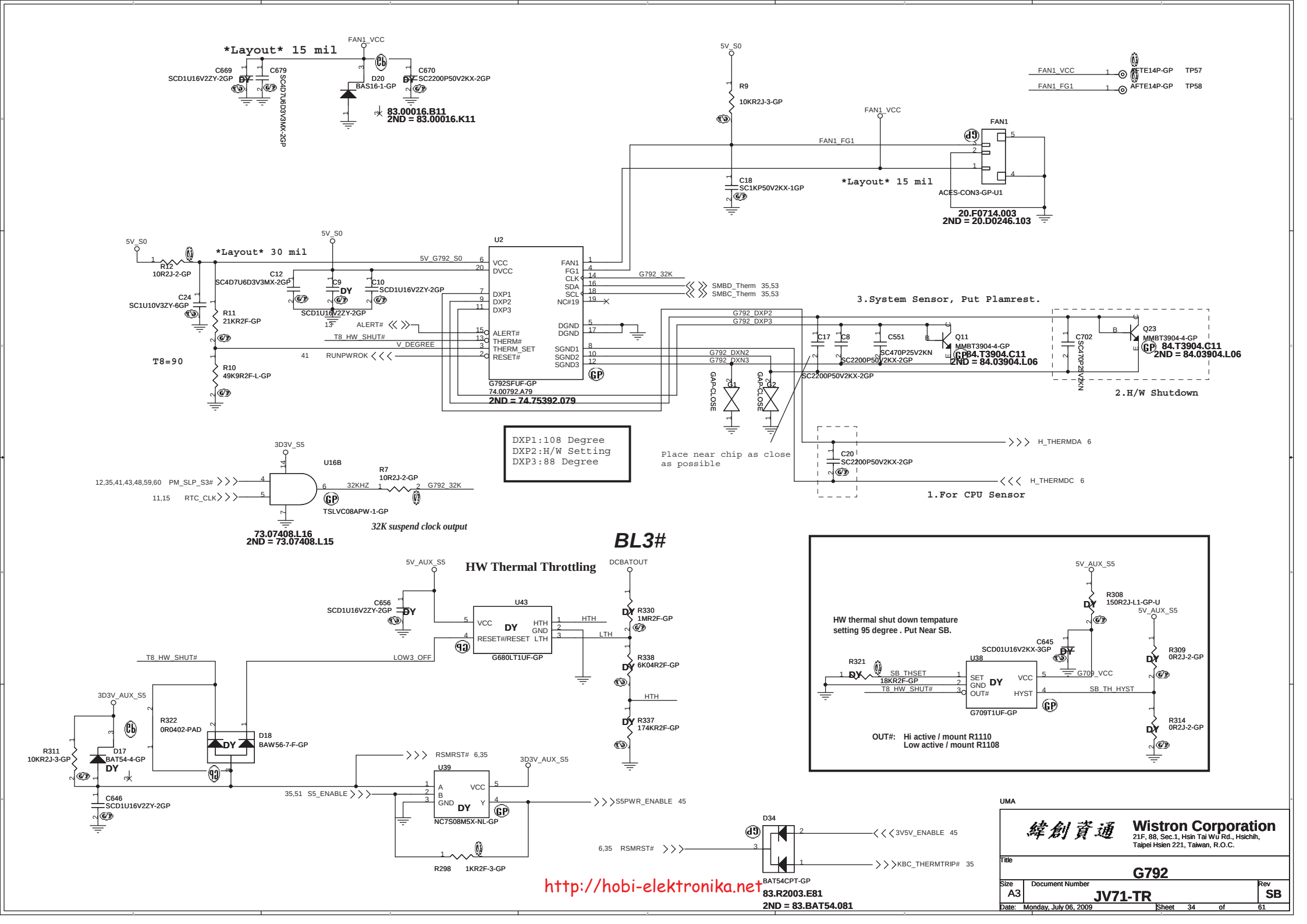

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Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

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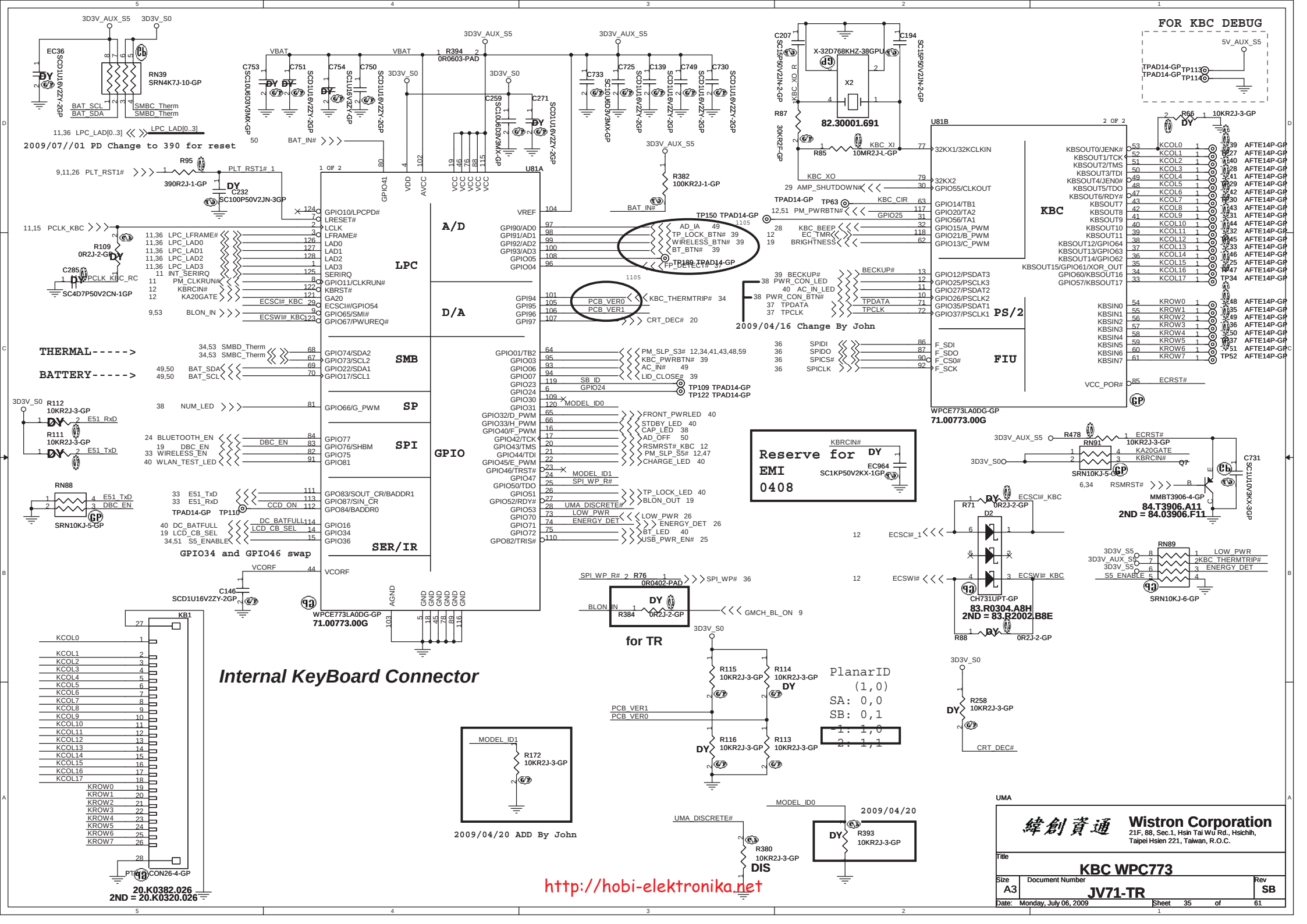
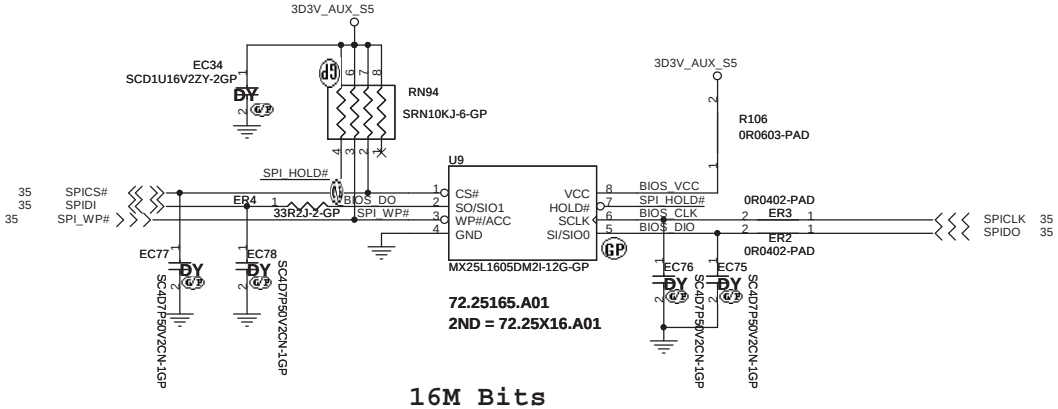
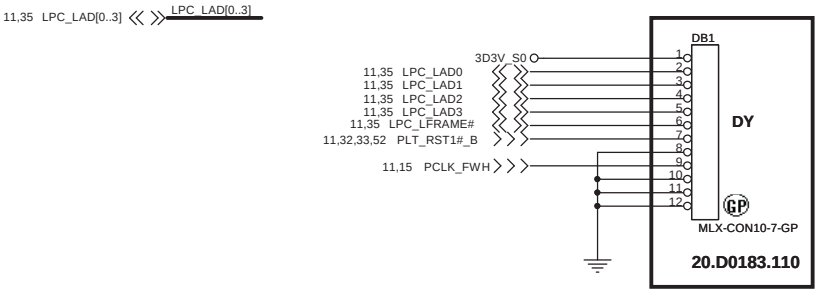

FOR KBC DEBUG
2009/07//01 PD Change to 390 for reset
2009/04/16 Change By John
THERMAL----->
BATTERY----->
GPIO34 and GPIO46 swap
Reserve for EMI 0408
for TR
PlanarID (1,0)
SA: 0,0
SB: 0,1
-1: 1,0
2: 1,1
2009/04/20 ADD By John
2009/04/20
Internal KeyBoard Connector
http://hobi-elektronika.net
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
Wistron Corporation
KBC WPC773
JV71-TR



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



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Title: BIOS

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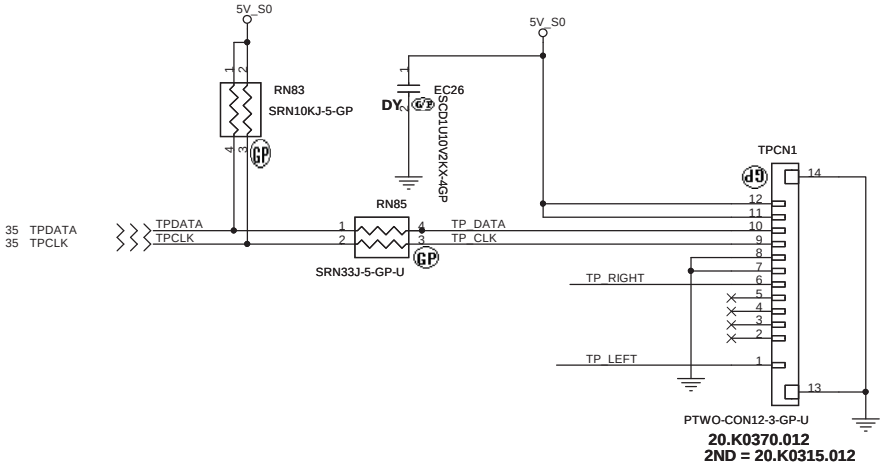
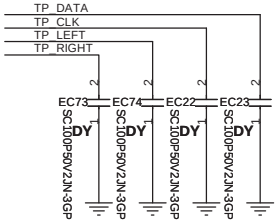
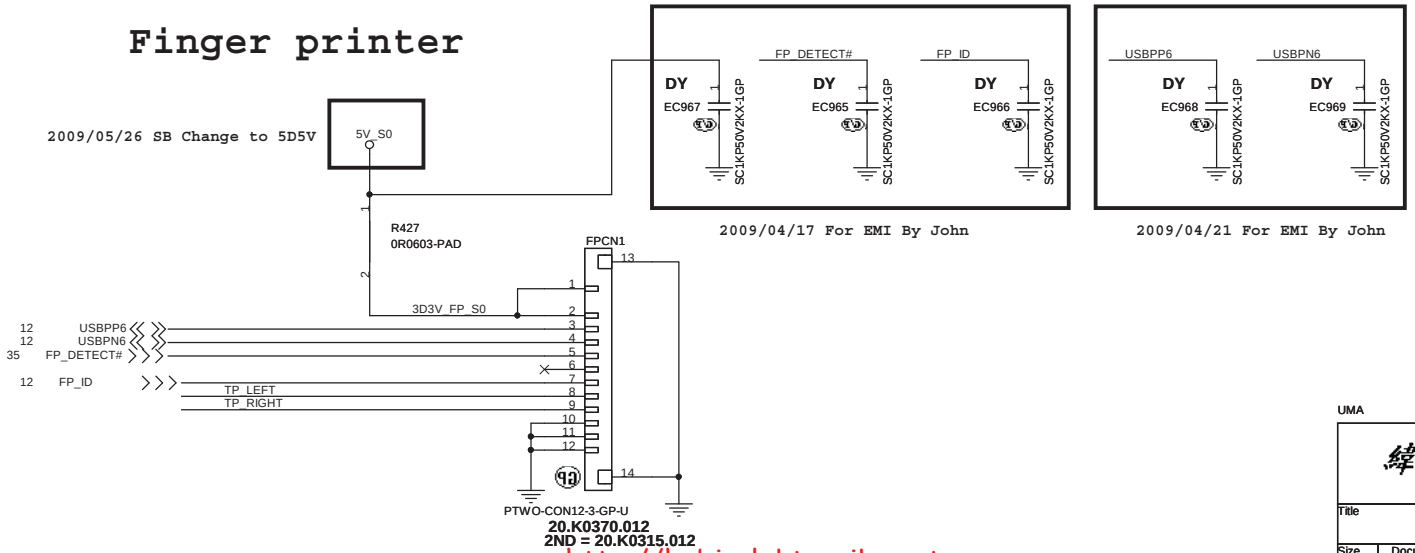
TOUCH PAD





Finger printer



UMA

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Title: **Touch PAD/Finger printer**

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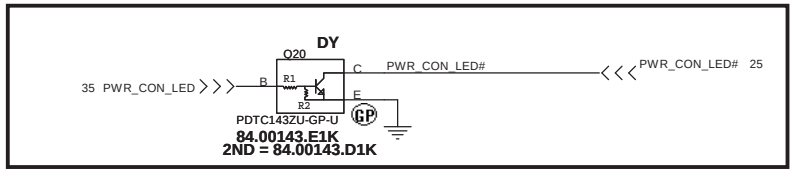
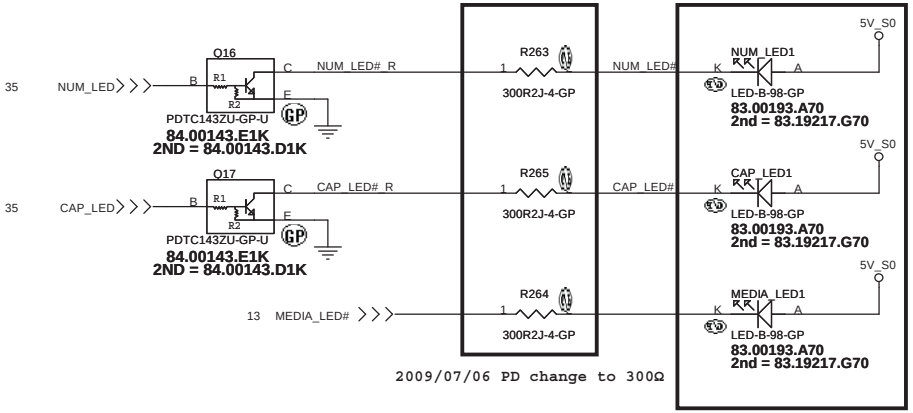
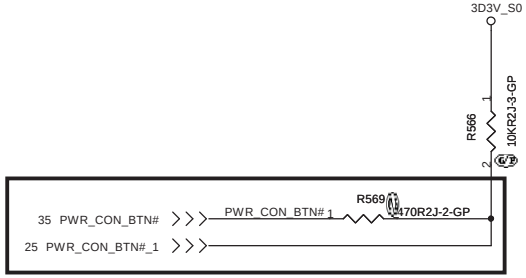
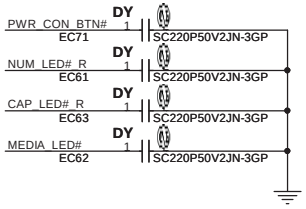
2009/04/16 Change By John







2009/04/16 Change By John



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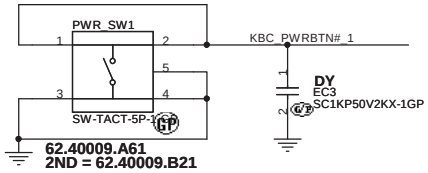
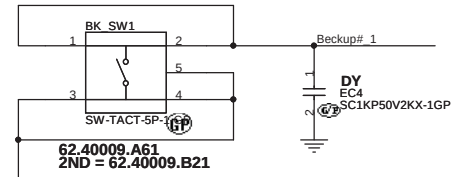
Cover Up Switch

Power Button



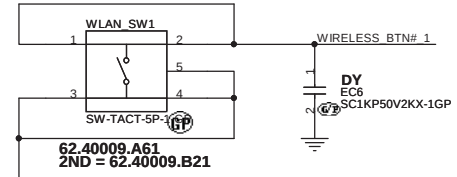
2009/05/23 SB Change

Beckup Button



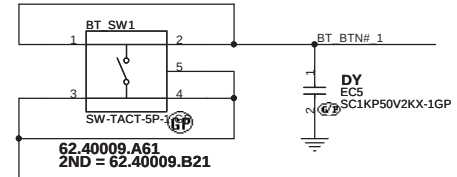
2009/05/23 SB Change

WIRELESS Button

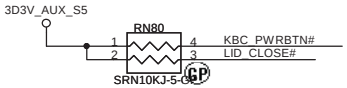


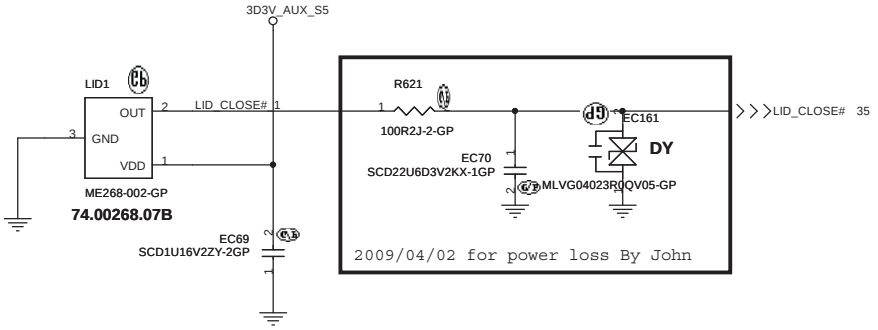
2009/05/23 SB Change

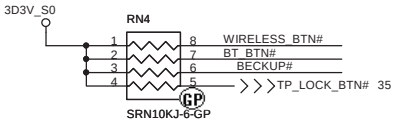
BT/3G Button

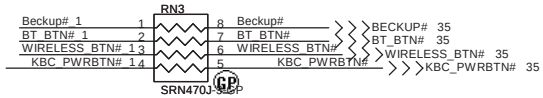


2009/05/23 SB Change

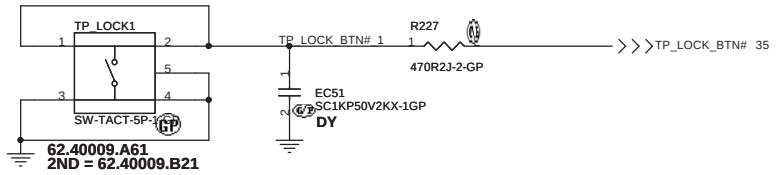








T/P lock Button



2009/05/23 SB Change

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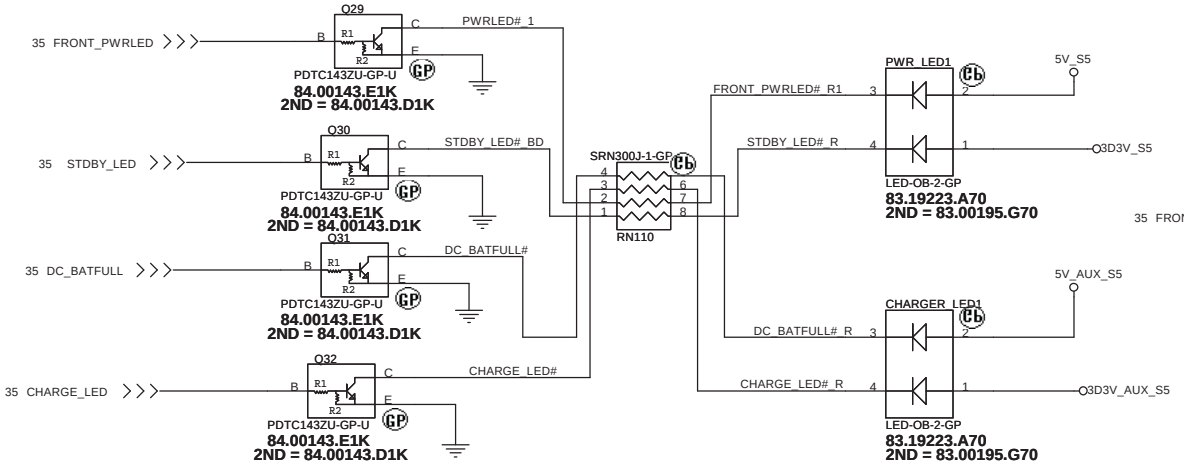

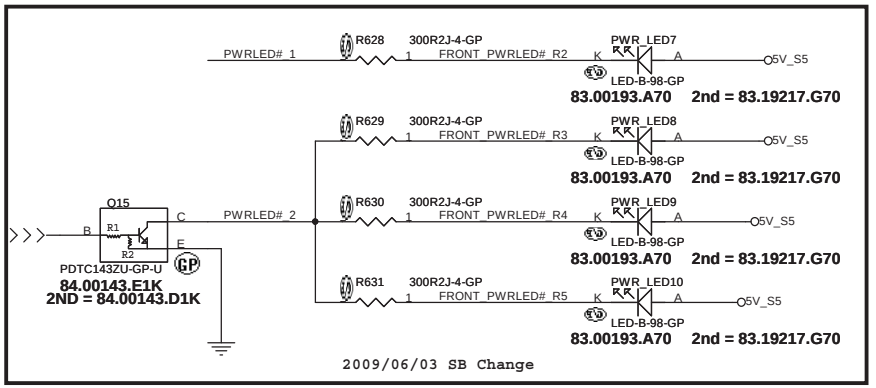

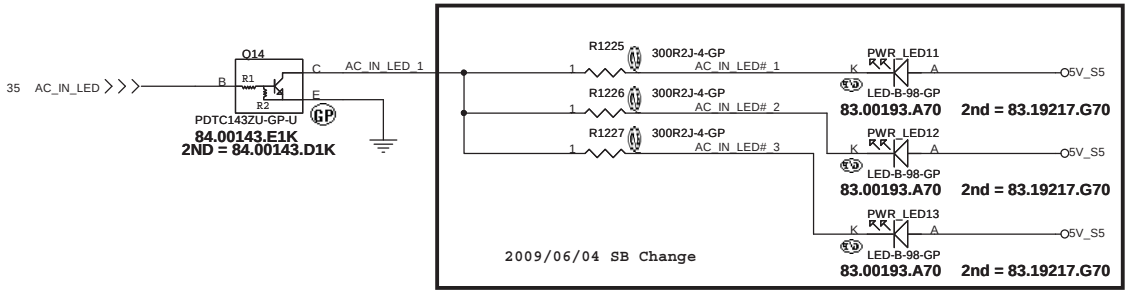

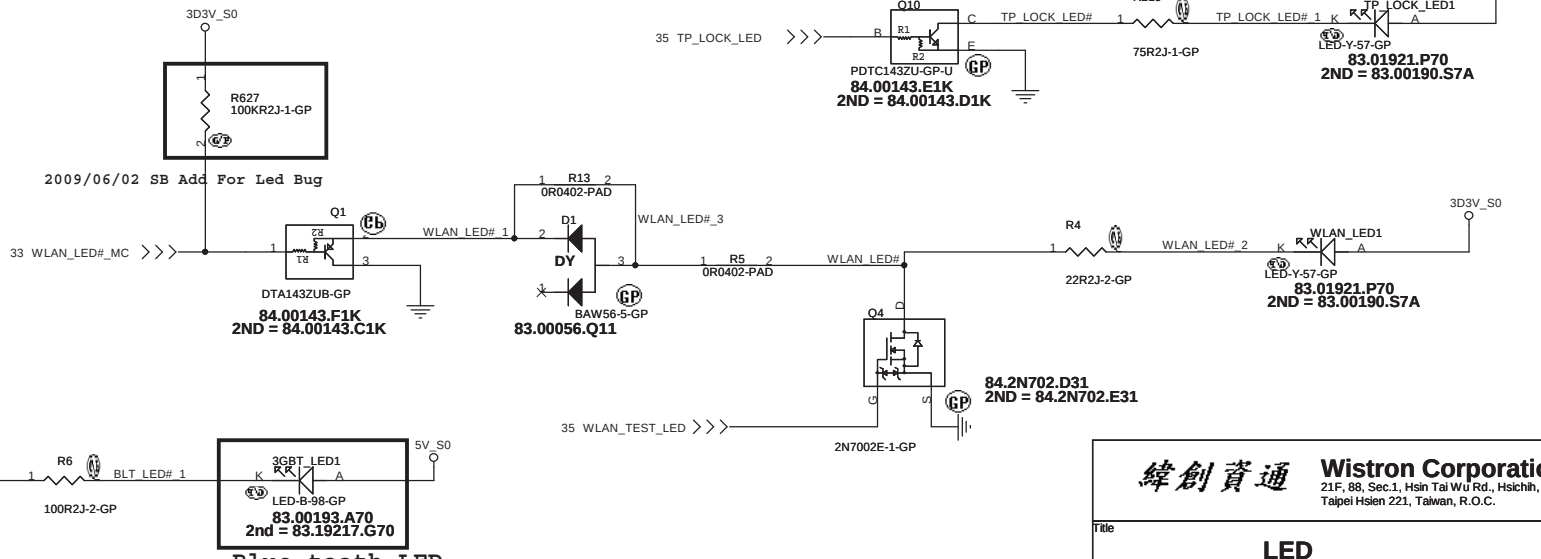

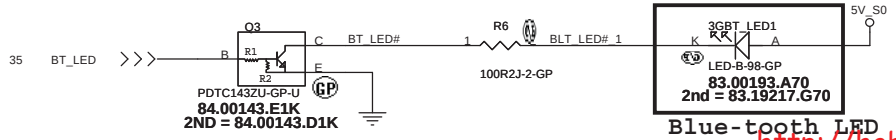

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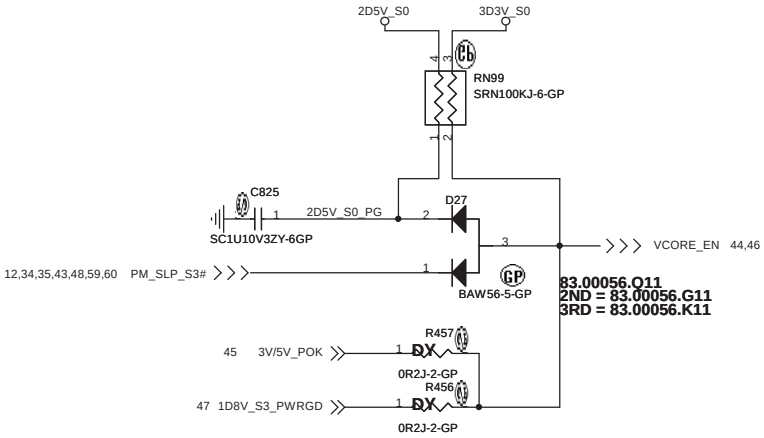
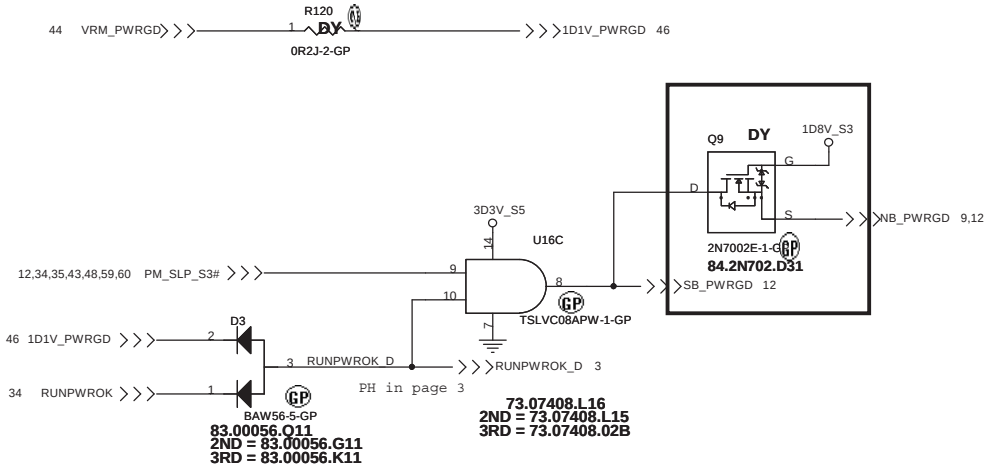


P/H @ 1D8V_S3 PAGE



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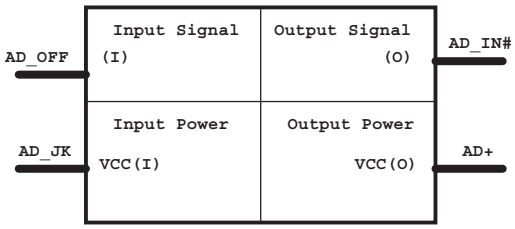
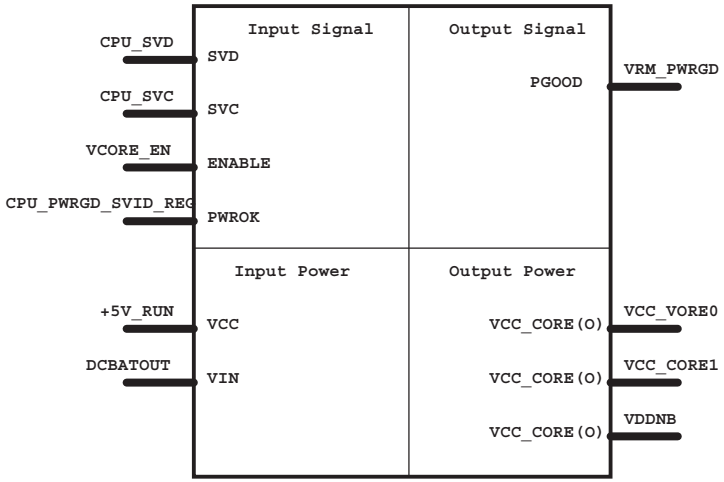
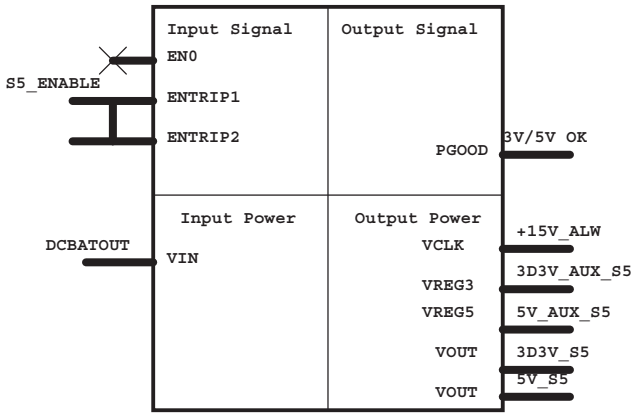
Adapter



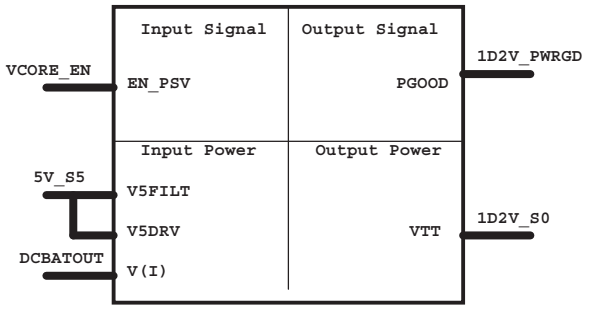
CPU_CORE
ISL6265HRTZ



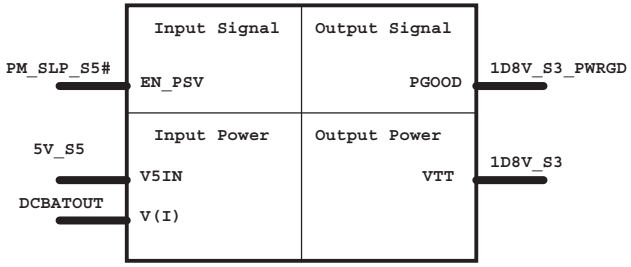
DCDC 5V/3D3V(RT8205A)



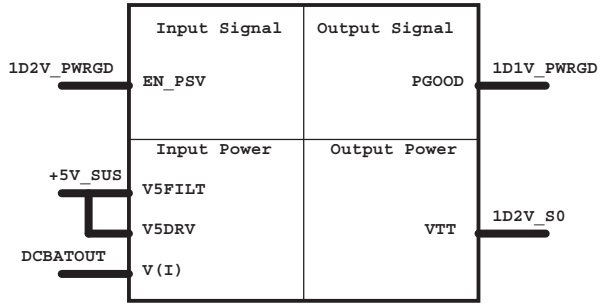
DCDC 1D2V(TPS51124)



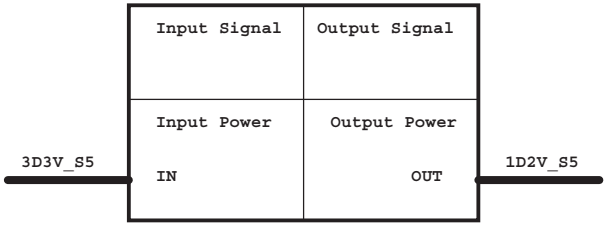
DCDC 1D8V(RT8209B)



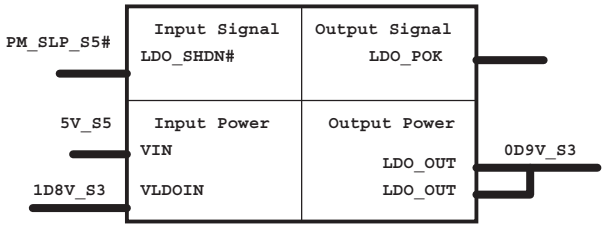
DCDC 1D1V(TPS51124)



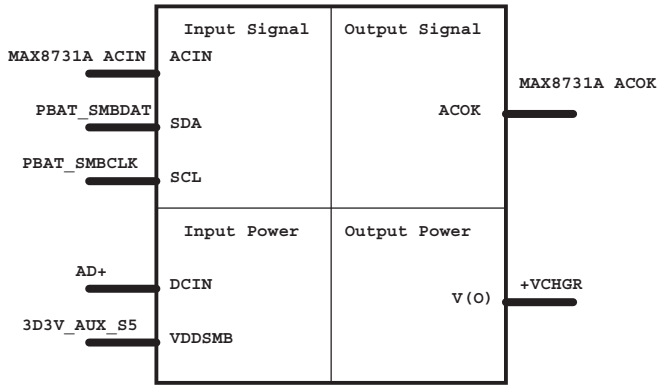
1D2V LDO G9161



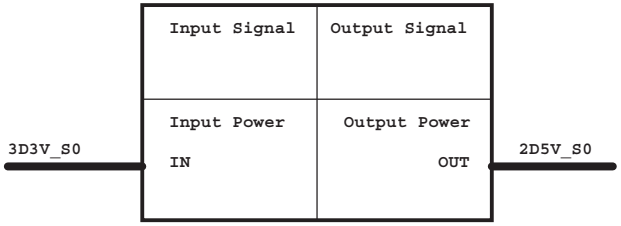
0D9V LDO RT9026



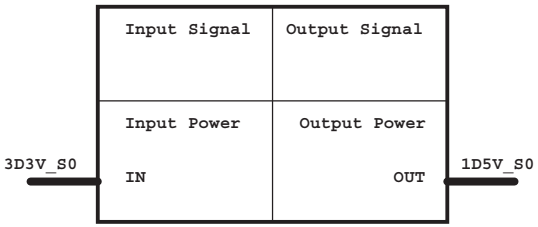
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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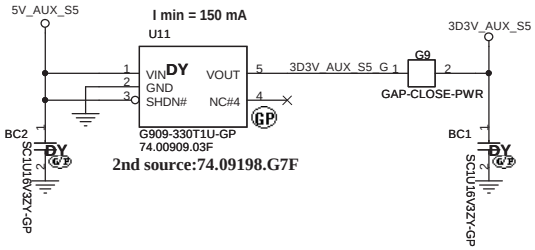
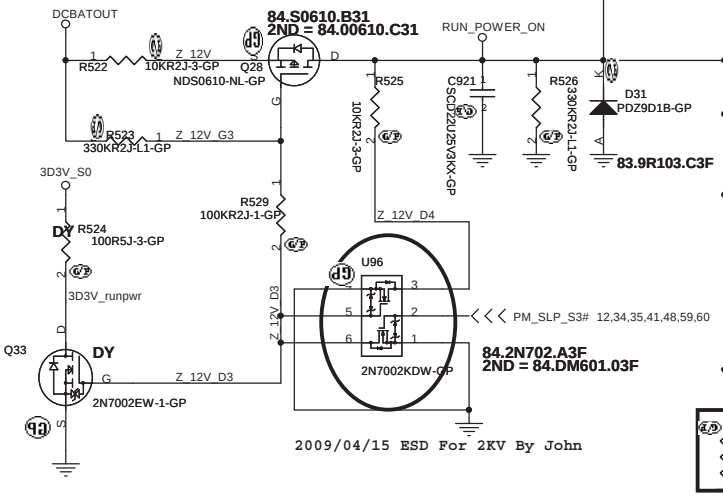
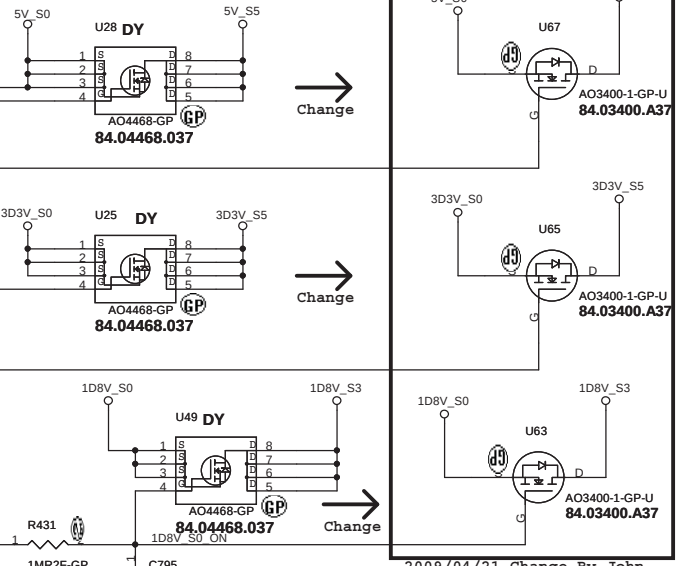
Aux Power 3D3V_AUX_S5



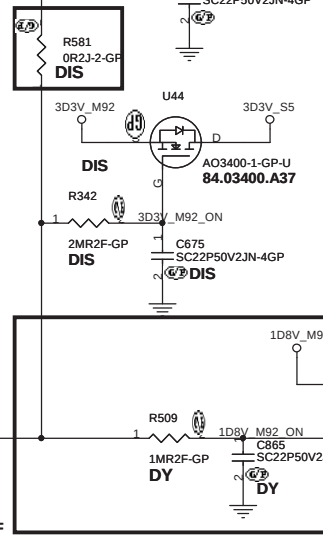
Run Power

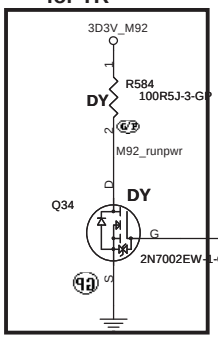


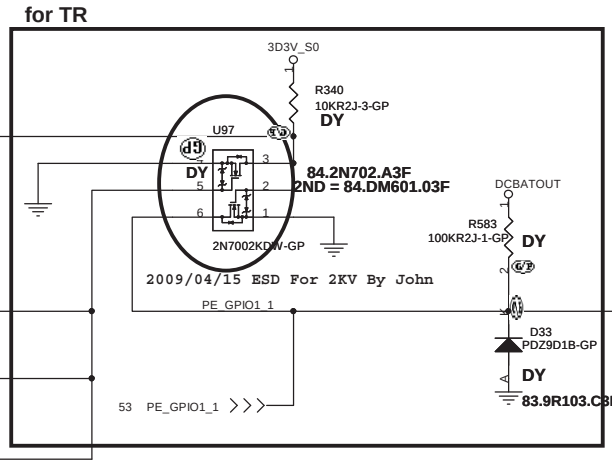
2009/04/15 ESD For 2KV By John



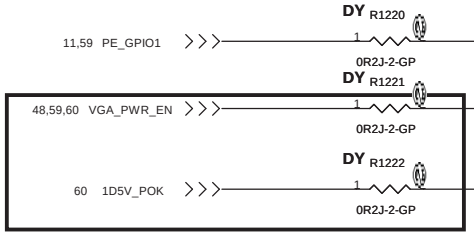
2009/04/21 Change By John



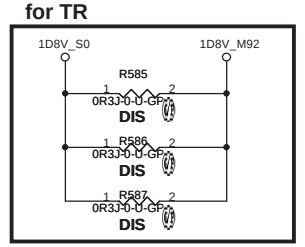




2009/04/15 ESD For 2KV By John



2009/04/21 ADD By John



R509,R342→10MΩ
C865→22pF
C675→1000pF
For VGA sequence issue

UMA

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Title: RUN AND AUX POWER

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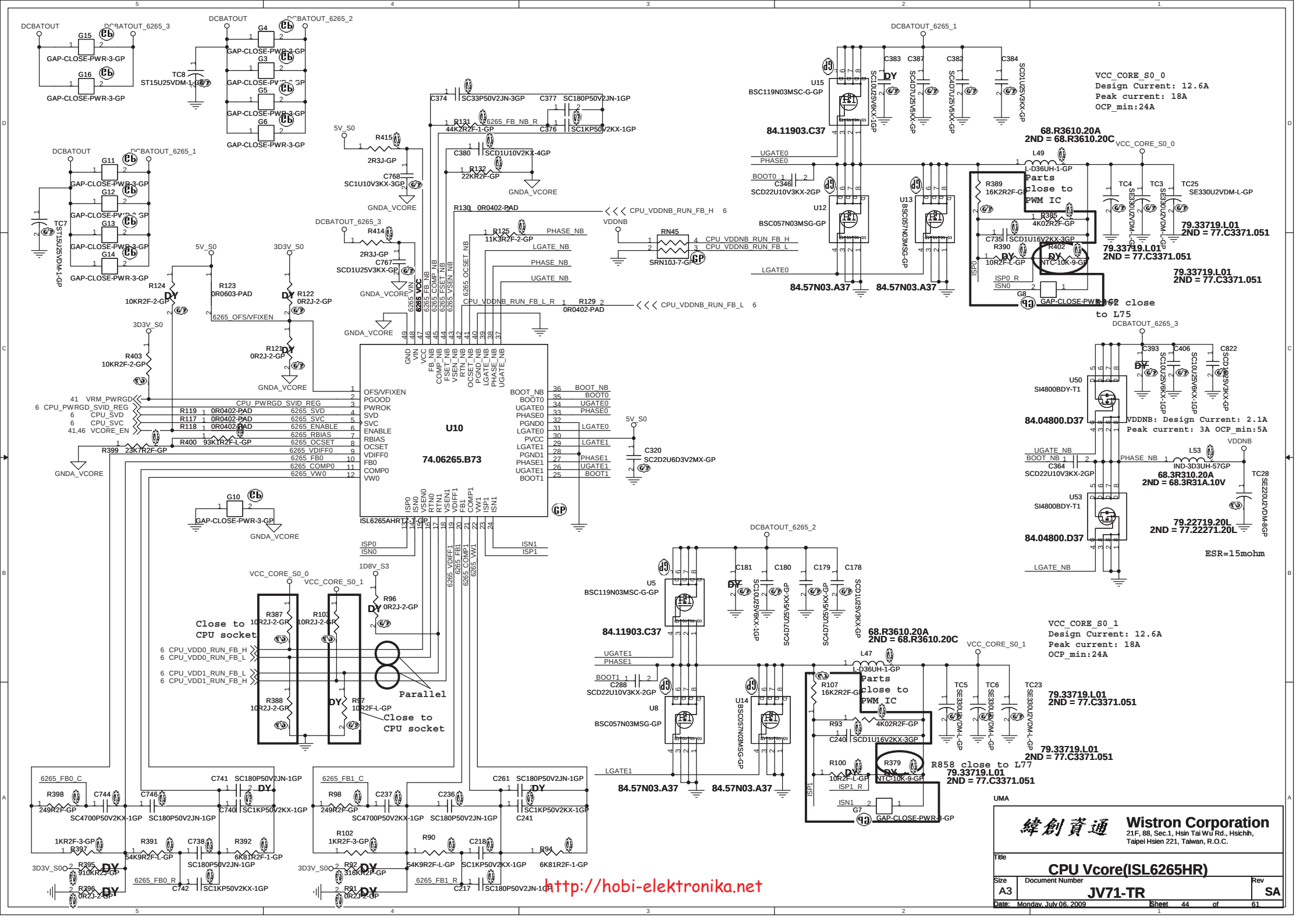
U10
74.06265.B73
ISL6265AHRTZ-T-GP
U15
BSC119N03MSC-G-GP
84.11903.C37
U12
BSC057N03MSG-GP
84.57N03.A37
U13
U50
SI4800BDY-T1
84.04800.D37
U53
U5
U8
U14
U49
U47
U48
U46
U45
U44
U43
U42
U41
U40
U39
U38
U37
U36
U35
U34
U33
U32
U31
U30
U29
U28
U27
U26
U25
U24
U23
U22
U21
U20
U19
U18
U17
U16
U15
U14
U13
U12
U11
U10
U9
U8
U7
U6
U5
U4
U3
U2
U1
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
68.R3610.20A
2ND = 68.R3610.20C
79.33719.L01
2ND = 77.C3371.051
79.22719.20L
2ND = 77.22271.20L
Parts close to PWM IC
R858 close to L77
R82 close to L75
Close to CPU socket
Parallel
68.R310.20A
2ND = 68.3R31A.10V
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV71-TR
SA
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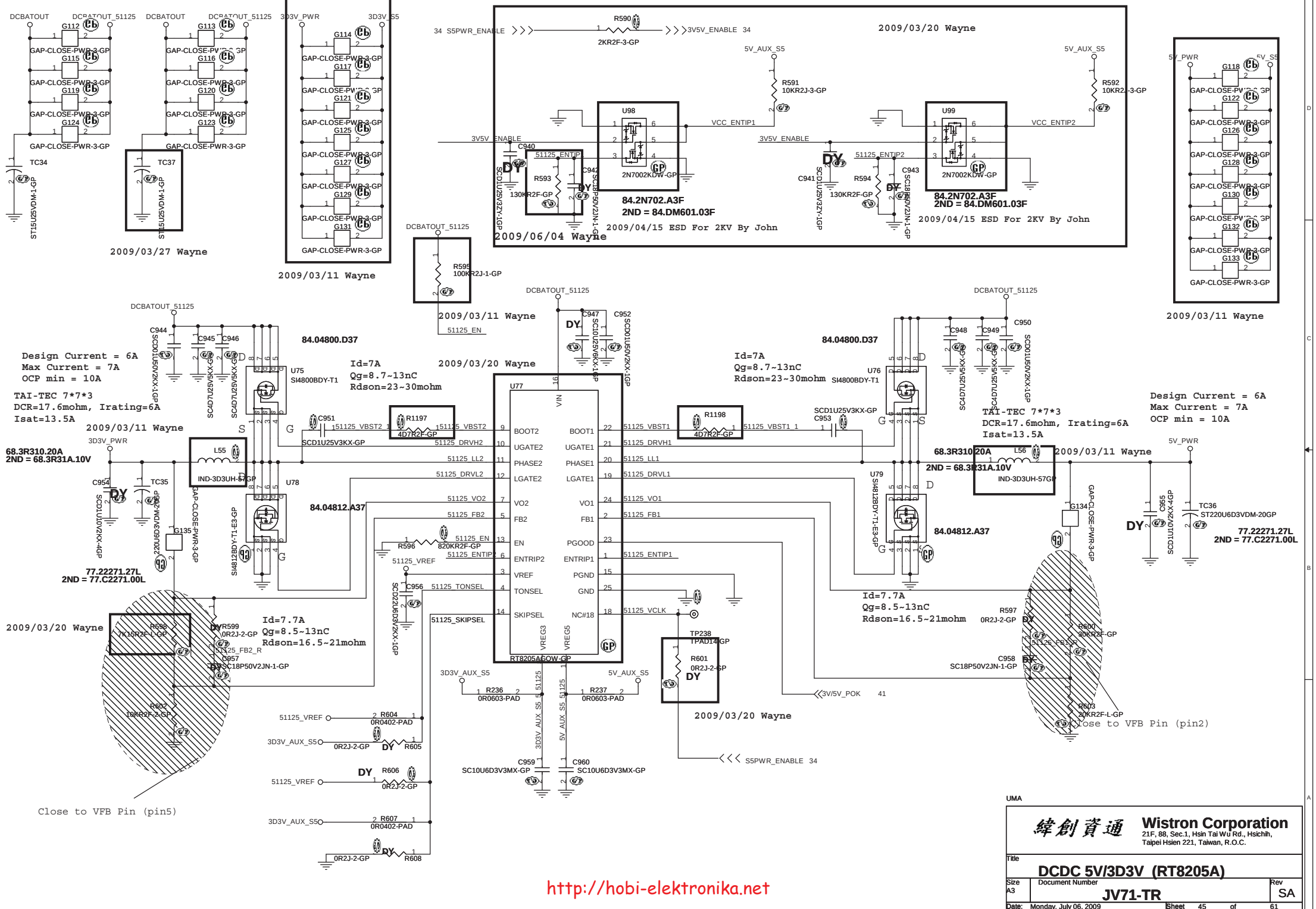
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
34 S5PWR_ENABLE
3V5V_ENABLE 34
R590 2KR2F-3-GP
R591 10KR2J-3-GP
R592 10KR2J-3-GP
U98
U99
VCC_ENTIP1
VCC_ENTIP2
3V5V_ENABLE
51125_ENTIP
51125_ENTIP2
C940
C941
C942
C943
R593 130KR2F-GP
R594 130KR2F-GP
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2009/04/15 ESD For 2KV By John
2009/06/04 Wayne
2009/03/20 Wayne
GAP-CLOSE-PWR-3-GP
TC34
TC37
ST15U25VDM-1-GP
2009/03/27 Wayne
2009/03/11 Wayne
R595 100KR2J-1-GP
51125_EN
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
84.04800.D37
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U75 SI4800BDY-T1
U76 SI4800BDY-T1
U77 RT8205AGQW-GP
U78 SI4812BDY-T1-E3-GP
U79 SI4812BDY-T1-E3-GP
L55 IND-3D3UH-57GP
L56 IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10V
84.04812.A37
77.22271.27L
2ND = 77.C2271.00L
ST220U6D3VDM-20GP
R596 820KR2F-GP
R597 0R2J-2-GP
R598 7K15R2F-L-GP
R599 0R2J-2-GP
R600 20KR2F-GP
R601 0R2J-2-GP
R602 10KR2F-2-GP
R603 20KR2F-L-GP
R604 0R0402-PAD
R605 0R2J-2-GP
R606 0R2J-2-GP
R607 0R0402-PAD
R608 0R2J-2-GP
R236 0R0603-PAD
R237 0R0603-PAD
TP238 TPAD14-GP
C956 SCD22U6D3V2KX-1GP
C957 SC18P50V2JN-1-GP
C958 SC18P50V2JN-1-GP
C959 SC10U6D3V3MX-GP
C960 SC10U6D3V3MX-GP
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
3V/5V_POK 41
S5PWR_ENABLE 34
http://hobi-elektronika.net
UMA
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
Size A3
Document Number
JV71-TR
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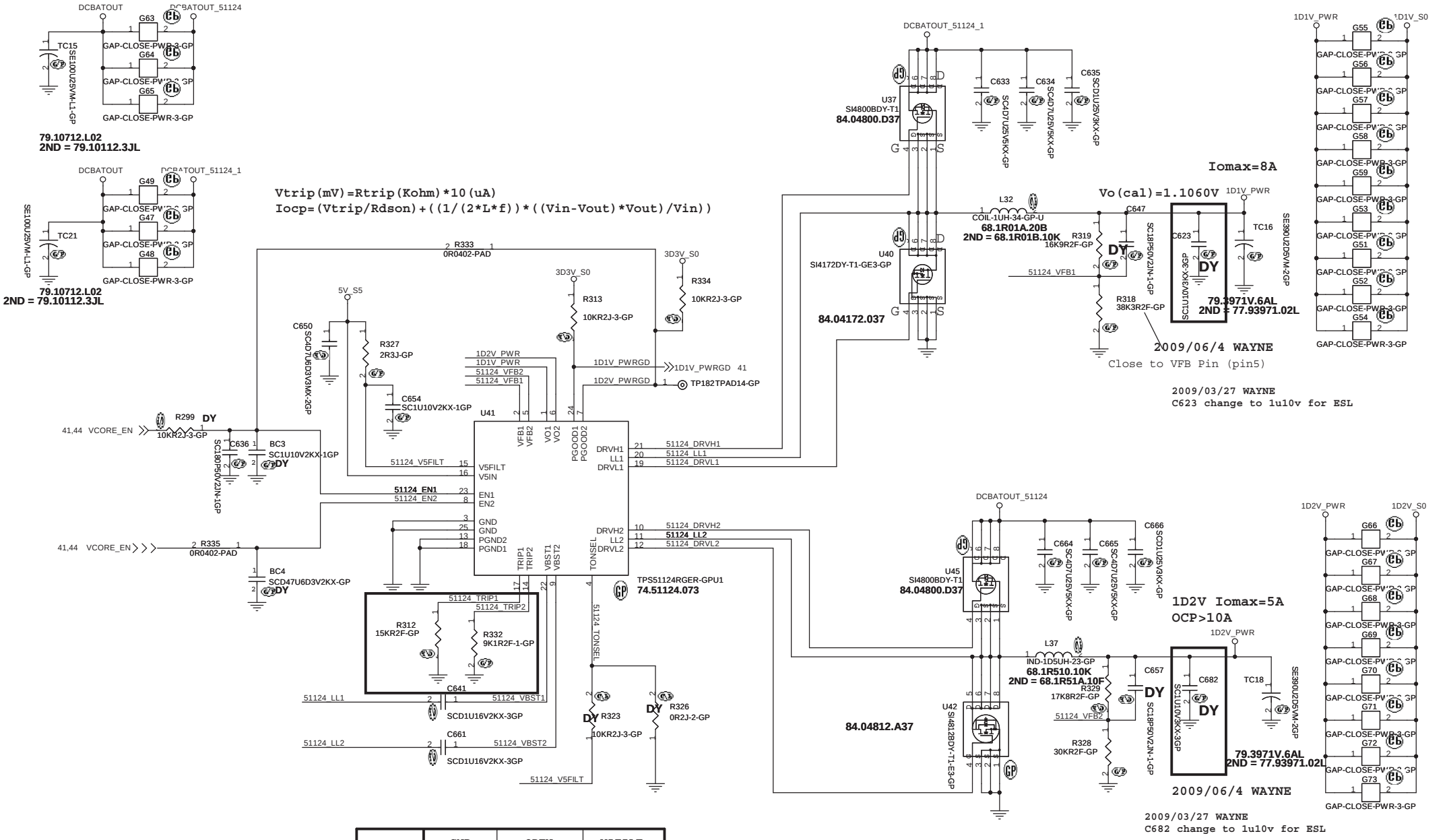

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

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Title: ***TPS51124_1D1V_1D2V***

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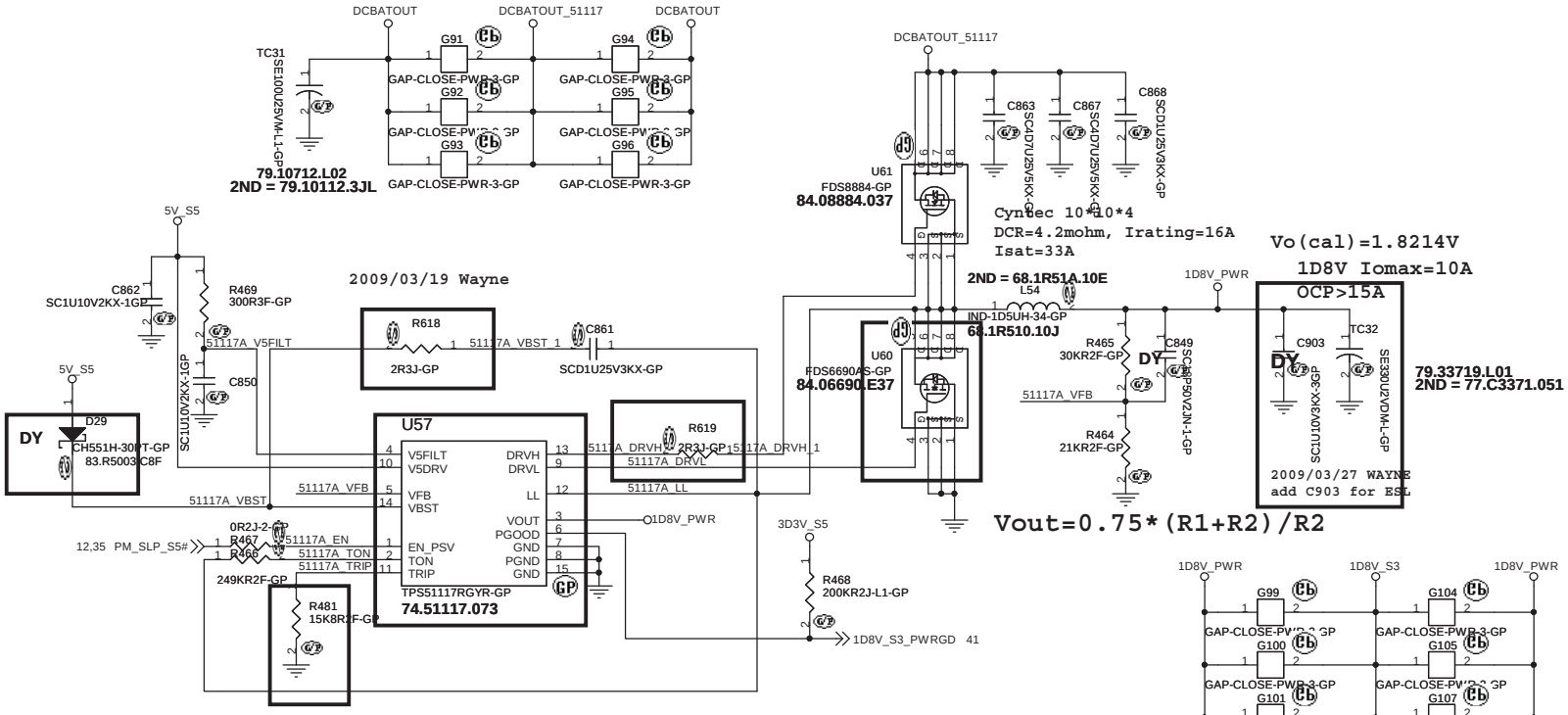
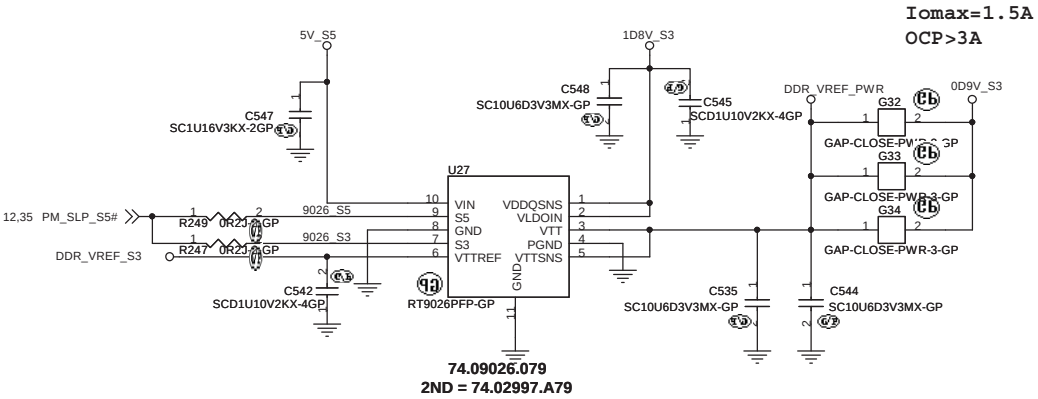


DDR_0.9V



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Title: DCDC_1D8V_APW7141/LDO 0D9V

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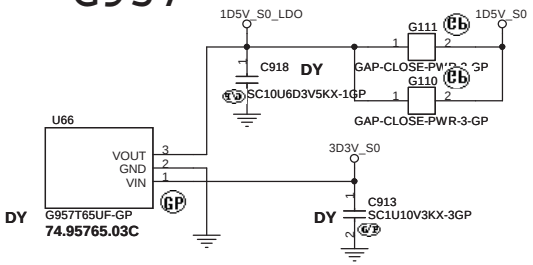
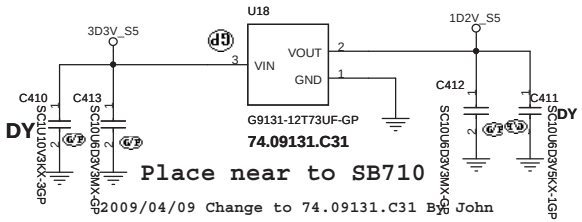
1D5V_S0
Iomax=1A

G957



For MINI Card.NEW Card power SW

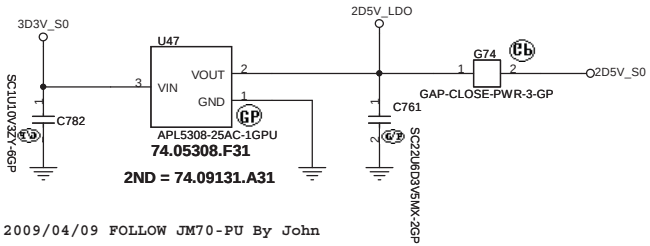
1D2V_S5
Iomax=400mA



Place near to SB710

2009/04/09 Change to 74.09131.C31 By John

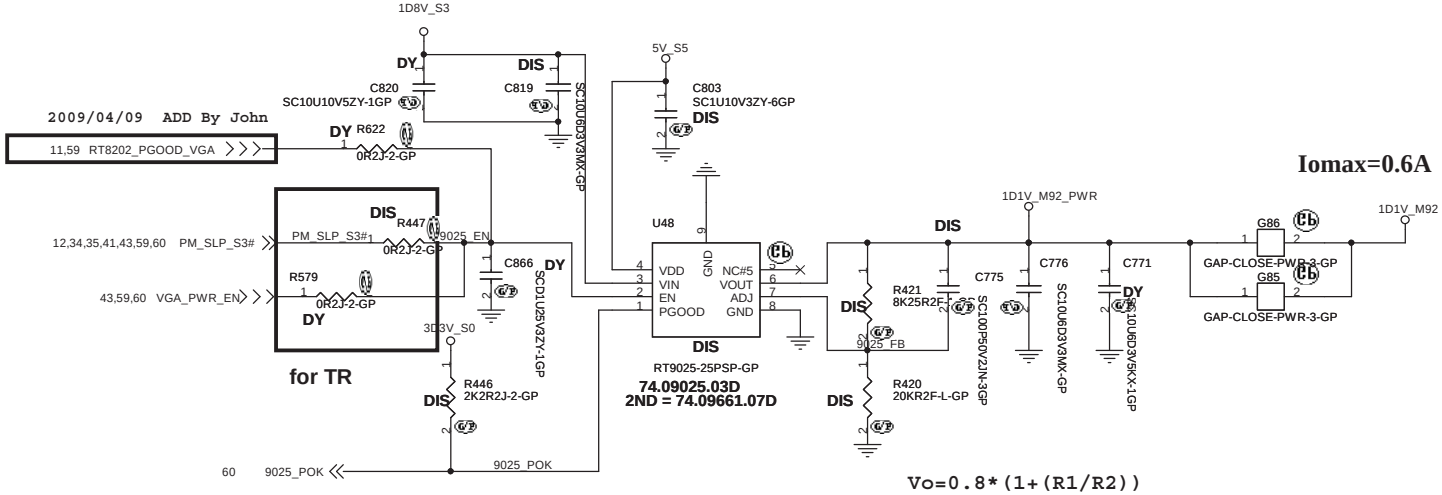
2D5V
Iomax=0.2A



2009/04/09 FOLLOW JM70-PU By John

Place near to CPU

Iomax=0.6A



Vo=0.8*(1+(R1/R2))

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	LDO 2D5V/1D5V/1D2V_S5/1D1V_M92	
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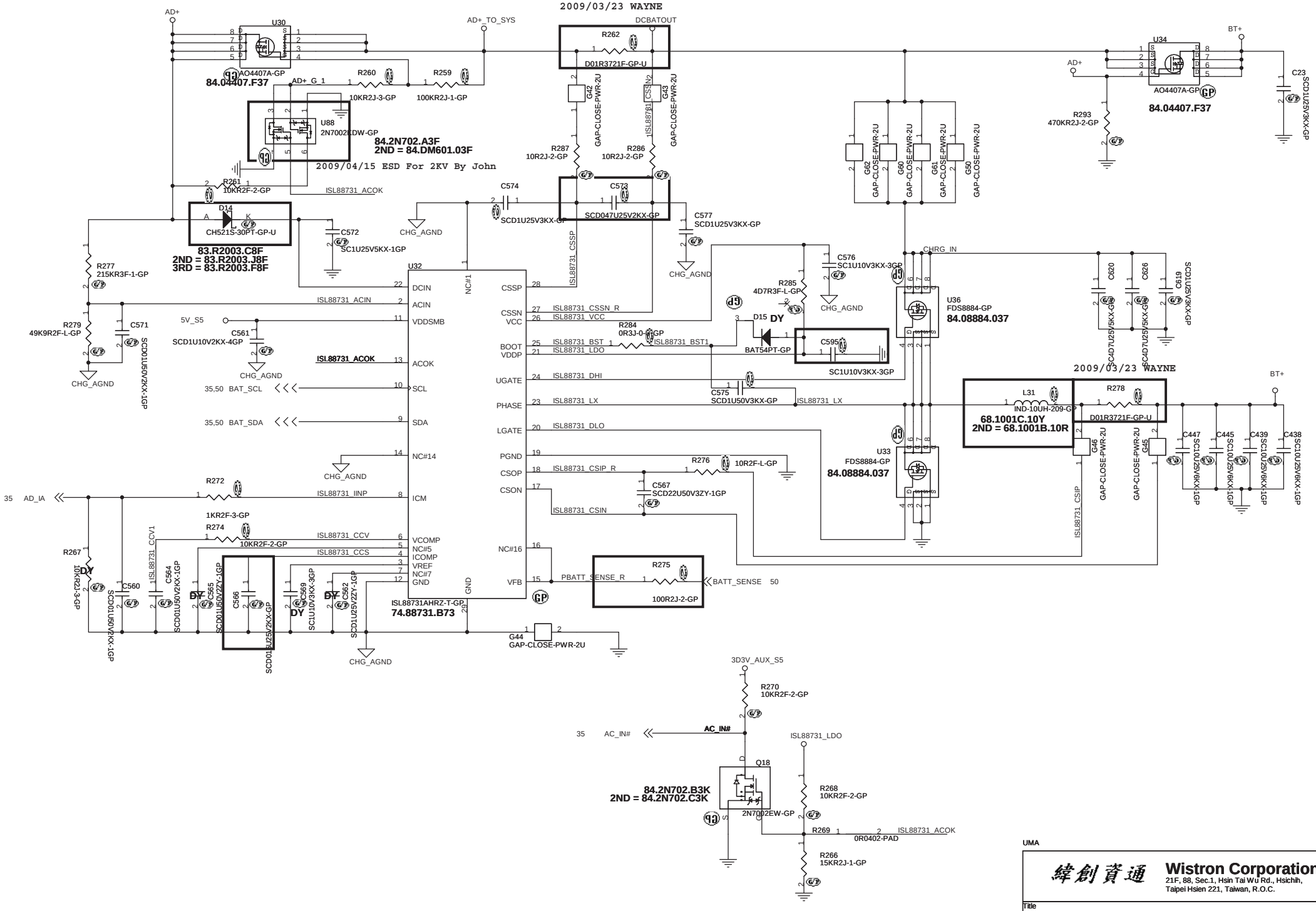
2009/03/23 WAYNE
AD+
AD+_TO_SYS
DCBATOUT
U30
AO4407A-GP
84.04407.F37
R260
10KR2J-3-GP
R259
100KR2J-1-GP
AD+_G_1
U88
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2009/04/15 ESD For 2KV By John
R261
10KR2F-2-GP
ISL88731_ACOK
D14
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
3RD = 83.R2003.F8F
C572
SC1U25V5KX-1GP
CHG_AGND
R262
D01R3721F-GP-U
G42 GAP-CLOSE-PWR-2U
G43 GAP-CLOSE-PWR-2U
ISL88731_CSSN_2
R287
10R2J-2-GP
R286
10R2J-2-GP
C574
SCD1U25V3KX-GP
C573
SCD047U25V2KX-GP
C577
SCD1U25V3KX-GP
ISL88731_CSSP
G62 GAP-CLOSE-PWR-2U
G60 GAP-CLOSE-PWR-2U
G61 GAP-CLOSE-PWR-2U
G50 GAP-CLOSE-PWR-2U
U34
AO4407A-GP
84.04407.F37
R293
470KR2J-2-GP
C23
SCD1U25V3KX-GP
BT+
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD01U50V2KX-1GP
C561
SCD1U10V2KX-4GP
5V_S5
ISL88731_ACIN
ISL88731_ACOK
35,50 BAT_SCL
35,50 BAT_SDA
U32
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST_1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
R284
0R3J-0-GP
ISL88731_BST1
D15 DY
BAT54PT-GP
C595
SC1U10V3KX-3GP
C575
SCD1U50V3KX-GP
R285
4D7R3F-L-GP
C576
SC1U10V3KX-3GP
CHRG_IN
U36
FDS8884-GP
84.08884.037
U33
FDS8884-GP
84.08884.037
C620
C626
C619
C4D7U25V5KX-GP
2009/03/23 WAYNE
L31
IND-10UH-209-GP
68.1001C.10Y
2ND = 68.1001B.10R
R278
D01R3721F-GP-U
G46 GAP-CLOSE-PWR-2U
G45 GAP-CLOSE-PWR-2U
C447
C445
C439
C438
SCD1U25V6KX-1GP
R276
10R2F-L-GP
C567
SCD22U50V3ZY-1GP
R275
100R2J-2-GP
PBATT_SENSE_R
BATT_SENSE
50
35 AD_IA
R272
1KR2F-3-GP
R274
10KR2F-2-GP
R267
100R2J-3-GP
DY
C560
C564
SCD01U50V2KX-1GP
C565
SCD01U50V2ZY-1GP
C566
SCD01U25V2KX-GP
C569
SC1U10V3KX-3GP
C562
SCD1U25V2ZY-1GP
G44 GAP-CLOSE-PWR-2U
3D3V_AUX_S5
R270
10KR2F-2-GP
35 AC_IN#
AC_IN#
Q18
84.2N702.B3K
2ND = 84.2N702.C3K
2N7002EW-GP
R268
10KR2F-2-GP
R269
0R0402-PAD
R266
15KR2J-1-GP
ISL88731_ACOK
http://hobi-elektronika.net
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
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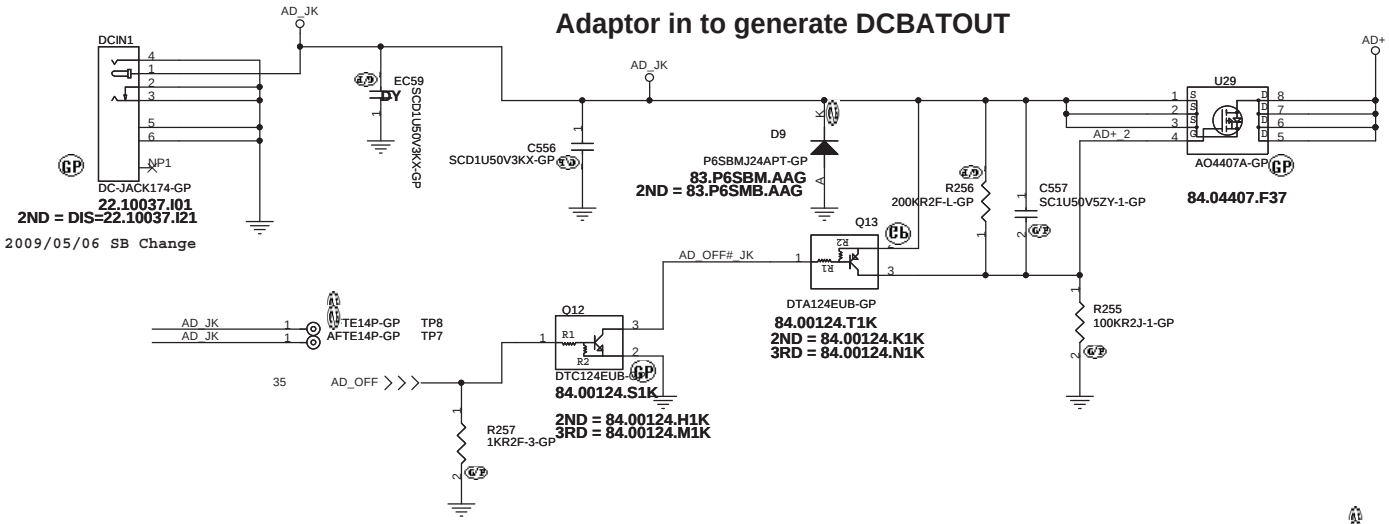
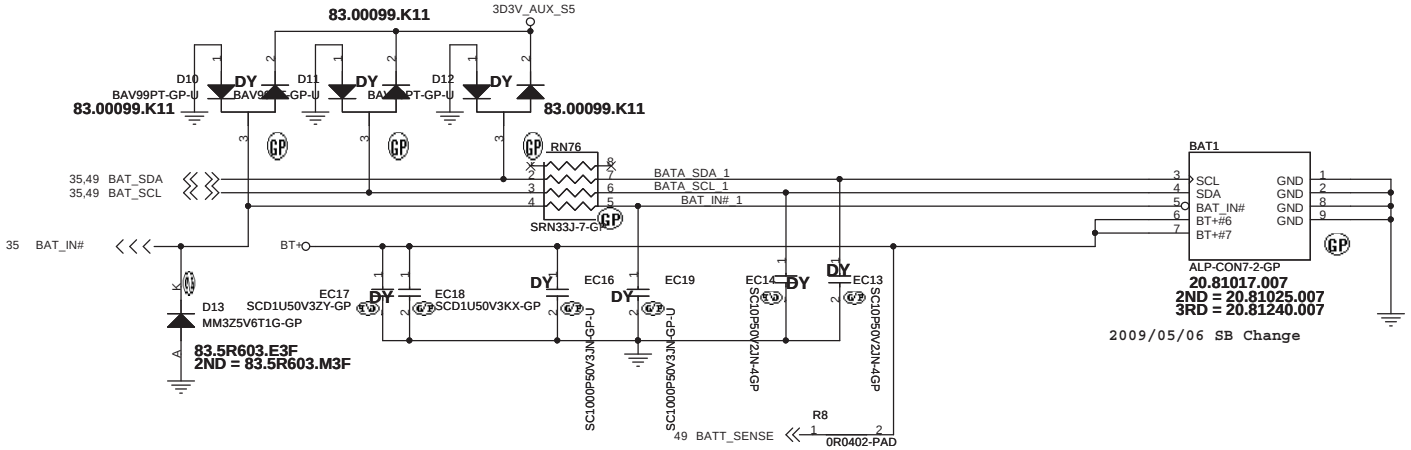
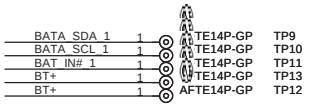
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title		
AD/BATT CONN		
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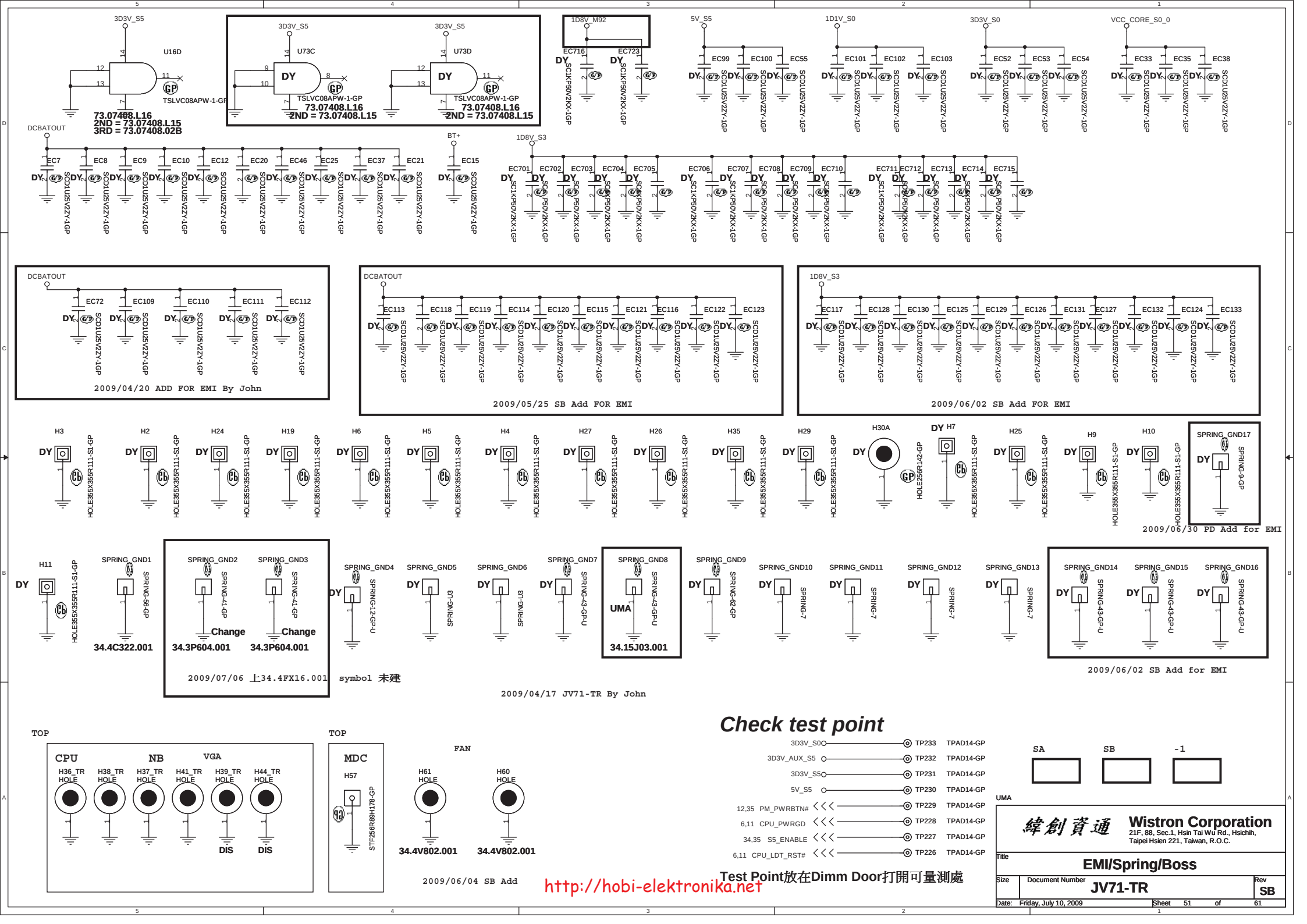
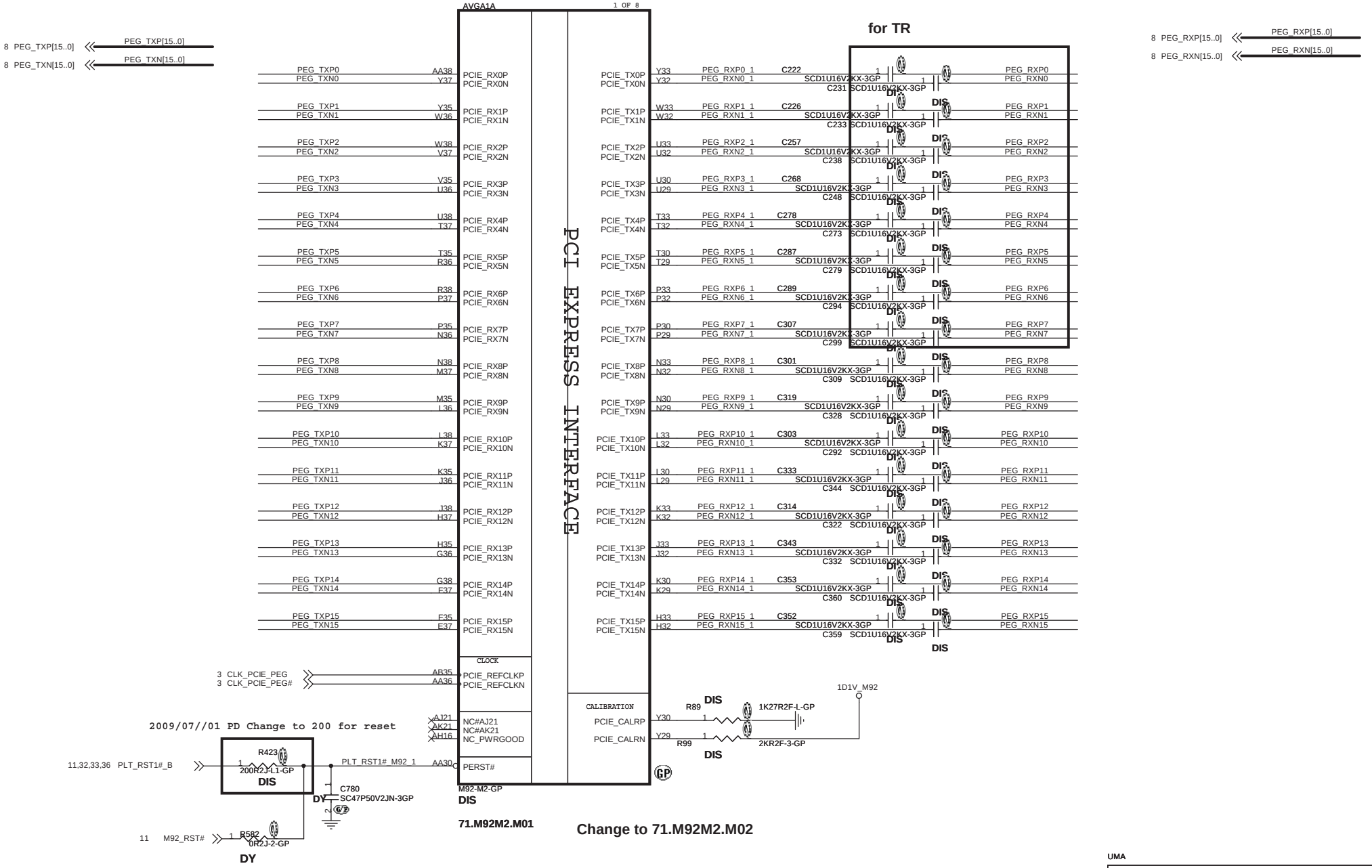
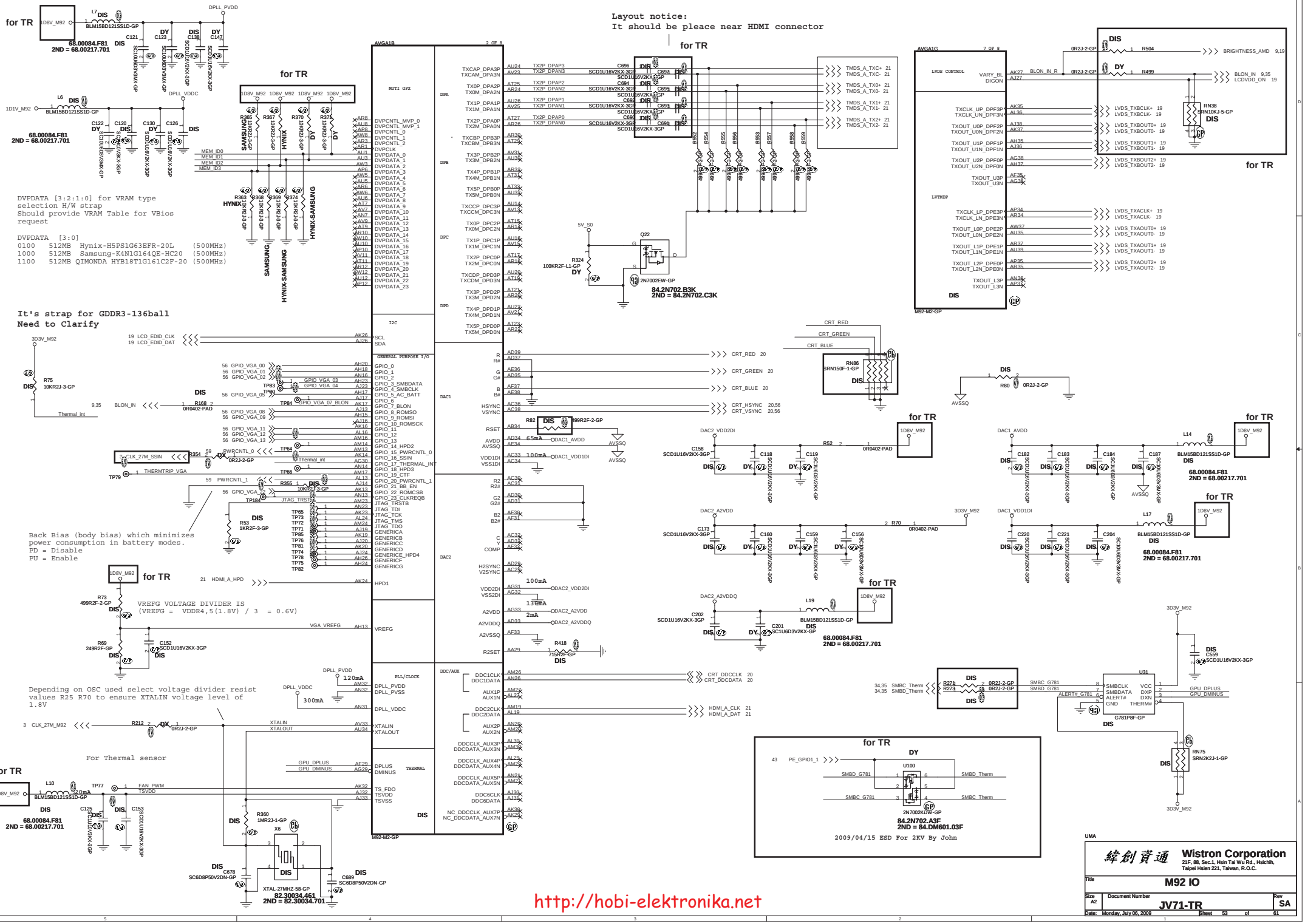
Date: Monday, July 06, 2009	Sheet 50 of 61	

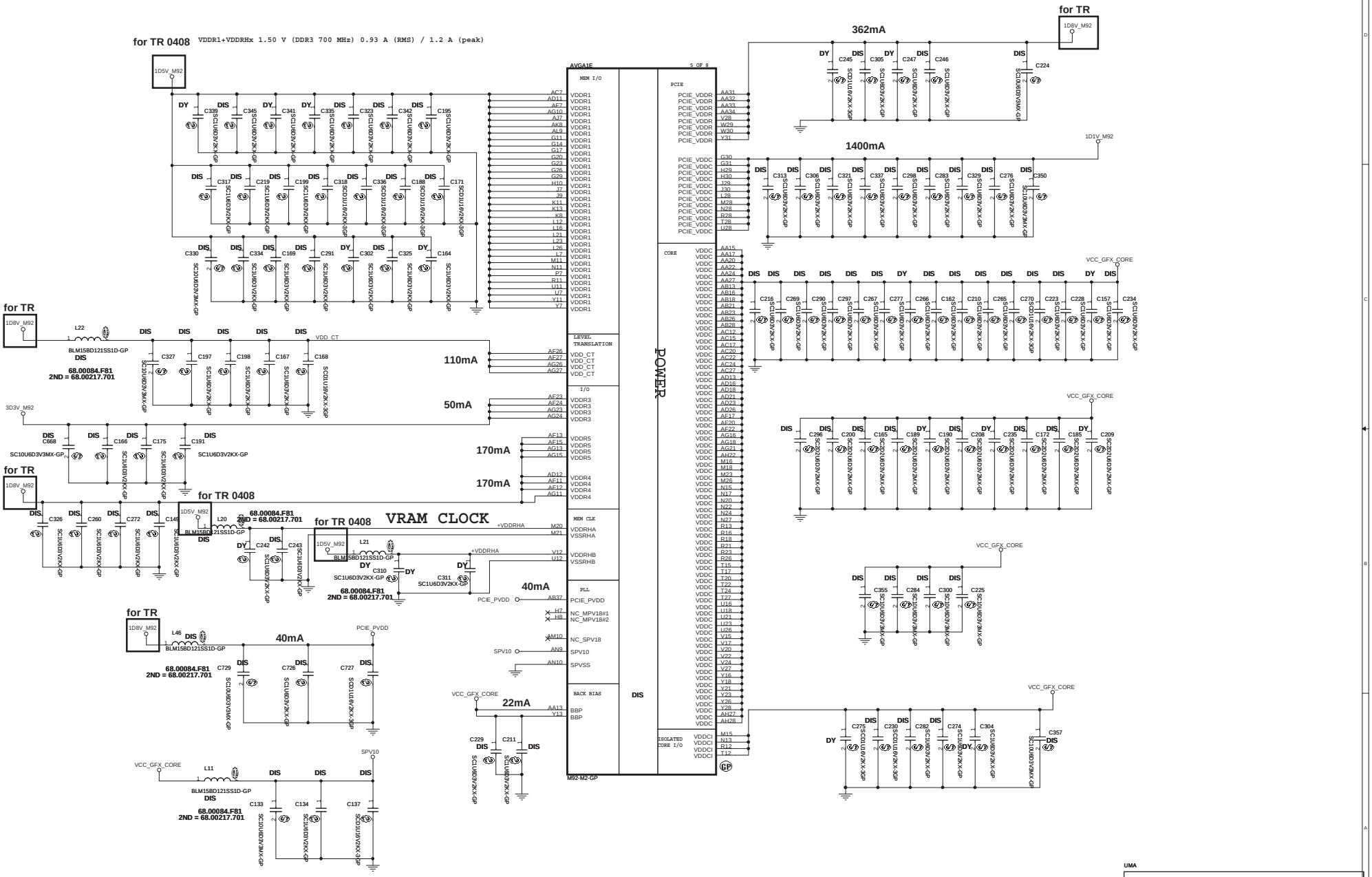

3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
U73C
U73D
1D8V_M92
EC716
EC723
SC1KP50V2KX-1GP
5V_S5
EC99
EC100
EC55
1D1V_S0
EC101
EC102
EC103
3D3V_S0
EC52
EC53
EC54
VCC_CORE_S0_0
EC33
EC35
EC38
SCD1U25V2ZY-1GP
DCBATOUT
EC7
EC8
EC9
EC10
EC12
EC20
EC46
EC25
EC37
EC21
BT+
EC15
1D8V_S3
EC701
EC702
EC703
EC704
EC705
EC706
EC707
EC708
EC709
EC710
EC711
EC712
EC713
EC714
EC715
SC1KP50V2KX-1GP
DCBATOUT
EC72
EC109
EC110
EC111
EC112
2009/04/20 ADD FOR EMI By John
DCBATOUT
EC113
EC118
EC119
EC114
EC120
EC115
EC121
EC116
EC122
EC123
2009/05/25 SB Add FOR EMI
1D8V_S3
EC117
EC128
EC130
EC125
EC129
EC126
EC131
EC127
EC132
EC124
EC133
2009/06/02 SB Add FOR EMI
H3
H2
H24
H19
H6
H5
H4
H27
H26
H35
H29
H30A
H7
H25
H9
H10
SPRING_GND17
SPRING-9-GP
HOLE355X355R111-S1-GP
HOLE256R142-GP
2009/06/30 PD Add for EMI
H11
SPRING_GND1
SPRING_GND2
SPRING_GND3
SPRING_GND4
SPRING_GND5
SPRING_GND6
SPRING_GND7
SPRING_GND8
SPRING_GND9
SPRING_GND10
SPRING_GND11
SPRING_GND12
SPRING_GND13
SPRING_GND14
SPRING_GND15
SPRING_GND16
SPRING-56-GP
SPRING-41-GP
SPRING-12-GP-U
SPRING-L3
SPRING-43-GP-U
SPRING-62-GP
SPRING-7
Change
34.4C322.001
34.3P604.001
34.3P604.001
UMA
34.15J03.001
2009/07/06 上34.4FX16.001 symbol 未建
2009/06/02 SB Add for EMI
2009/04/17 JV71-TR By John
TOP
CPU
NB
VGA
H36_TR HOLE
H38_TR HOLE
H37_TR HOLE
H41_TR HOLE
H39_TR HOLE
H44_TR HOLE
DIS
DIS
TOP
MDC
H57
STF256R89H178-GP
FAN
H61 HOLE
H60 HOLE
34.4V802.001
34.4V802.001
2009/06/04 SB Add
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,35 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
34,35 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
SA
SB
-1
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV71-TR
Rev
SB
Date: Friday, July 10, 2009
Sheet 51 of 61
http://hobi-elektronika.net



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 PCIE		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 52 of 61	


Layout notice:
It should be pleace near HDMI connector
for TR
DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
Depending on OSC used select voltage divider resist
values R25 R70 to ensure XTALIN voltage level of
1.8V
For Thermal sensor
84.2N702.B3K
2ND = 84.2N702.C3K
84.2N702.A3F
2ND = 84.DM601.03F
2009/04/15 ESD For 2KV By John
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
M92 IO
JV71-TR
Monday, July 06, 2009


for TR 0408
VDDR1+VDDRHx 1.50 V (DDR3 700 MHz) 0.93 A (RMS) / 1.2 A (peak)
for TR
362mA
1400mA
110mA
50mA
170mA
170mA
40mA
22mA
40mA
VRAM CLOCK
POWER
AVGA1E
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
ISOLATED CORE I/O
VCC_GFX_CORE
1D8V_M92
1D5V_M92
1D1V_M92
3D3V_M92
VDD_CT
+VDDRHA
+VDDRHB
PCIE_PVDD
SPV10
M92-M2-GP
http://hobi-elektronika.net
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Taipei Hsien 221, Taiwan, R.O.C.
UMA
M92 POWER
JV71-TR
SA
Monday, July 06, 2009
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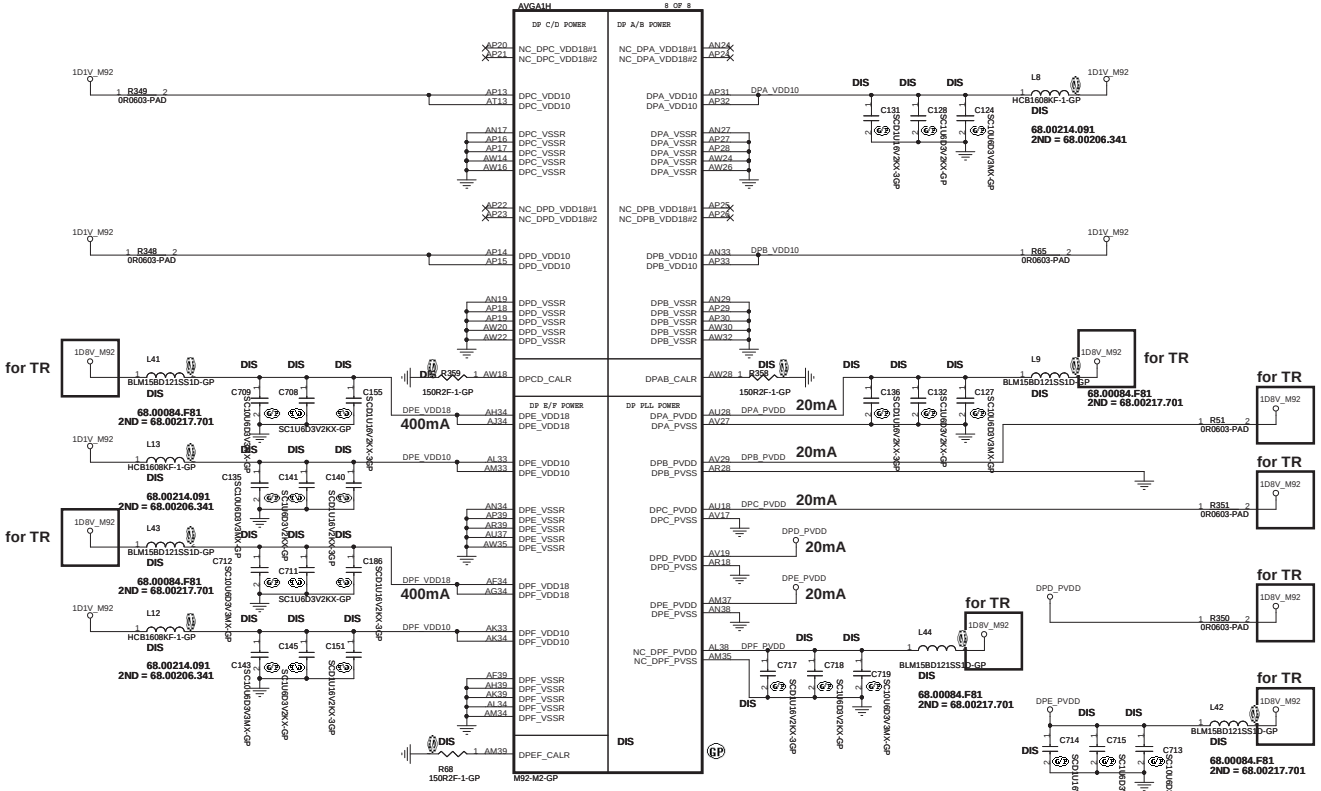

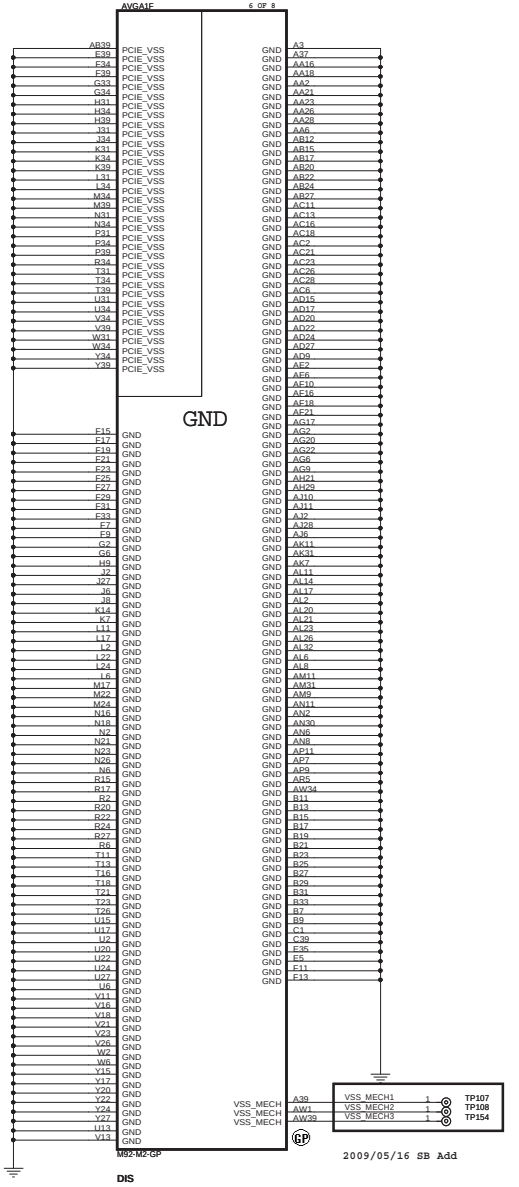

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DP POWER_GND**

Size	Document Number	Rev
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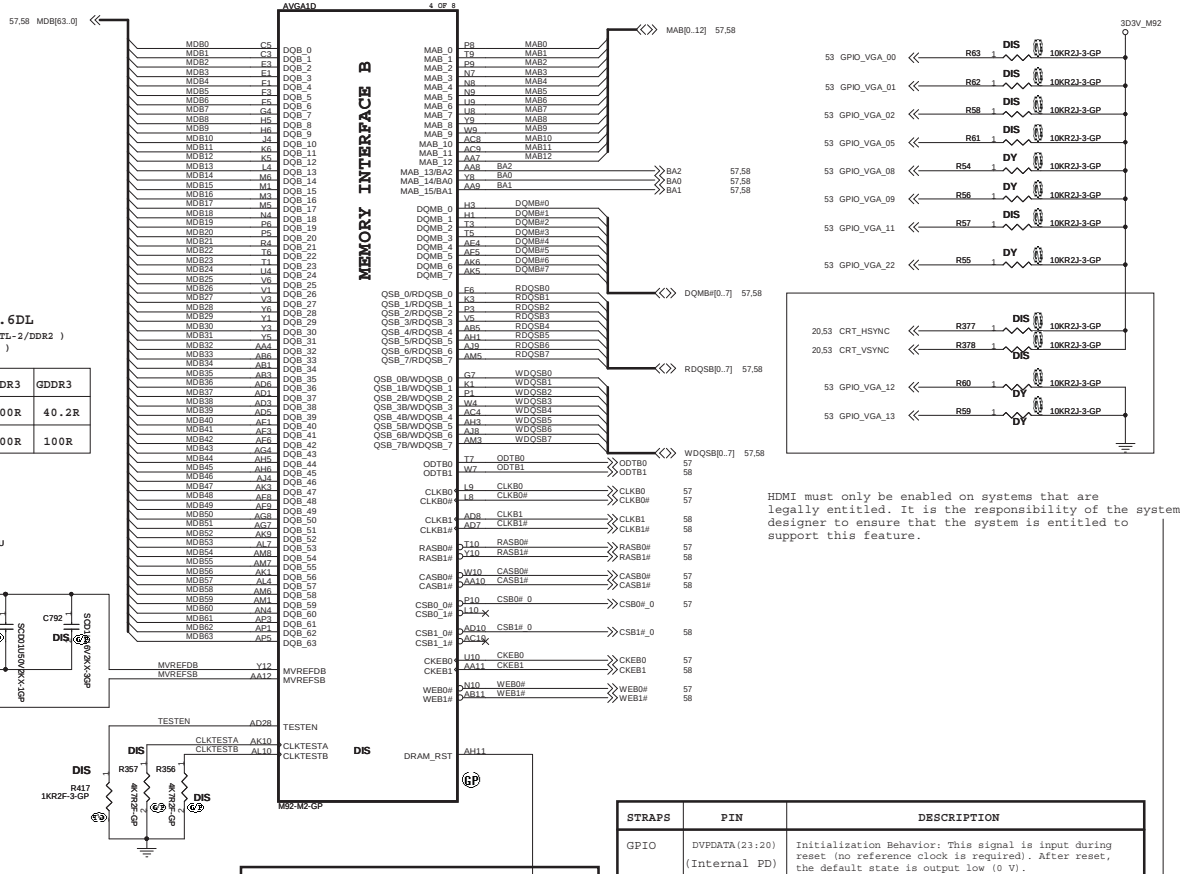
M92-M2 uses memory group B only



DIVIDER RESISTORS	DDR2	DDR3	GDDR3
MVREF TO 1.8V	100R	100R	40.2R
MVREF TO GND	100R	100R	100R

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x			
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

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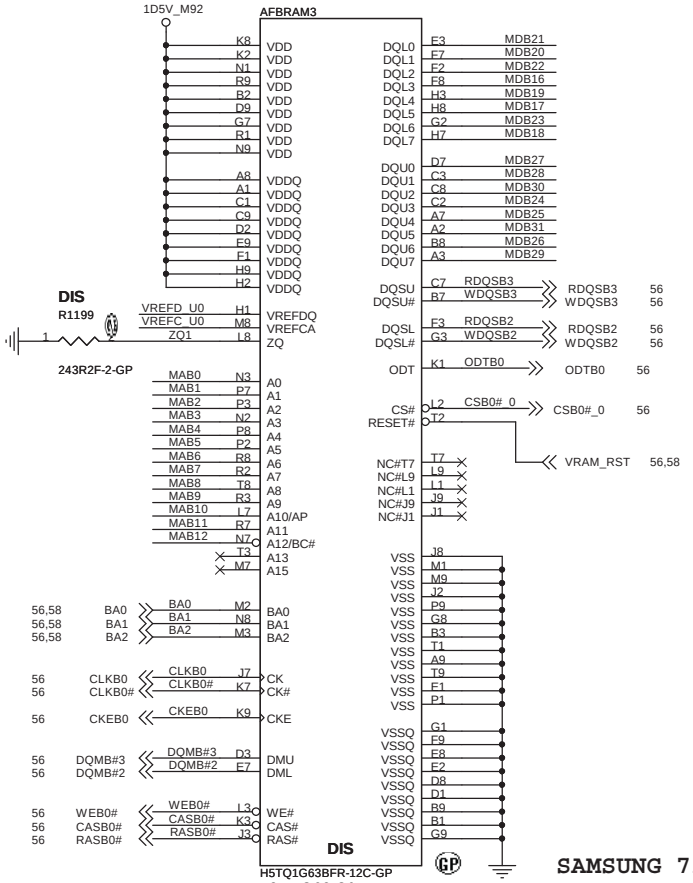
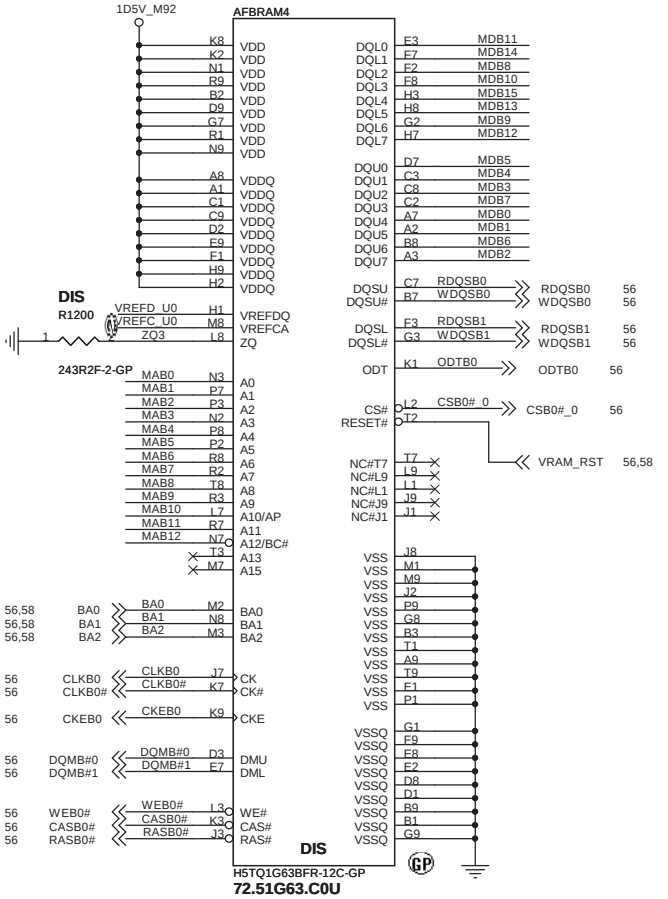
Title: Memory / Straps

Size: A2 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 56 of 61

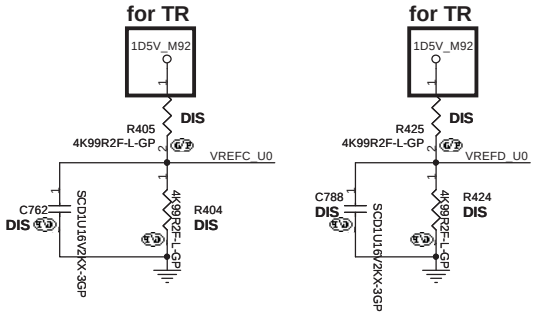
DDR3

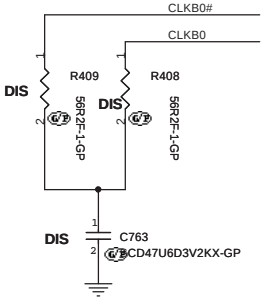


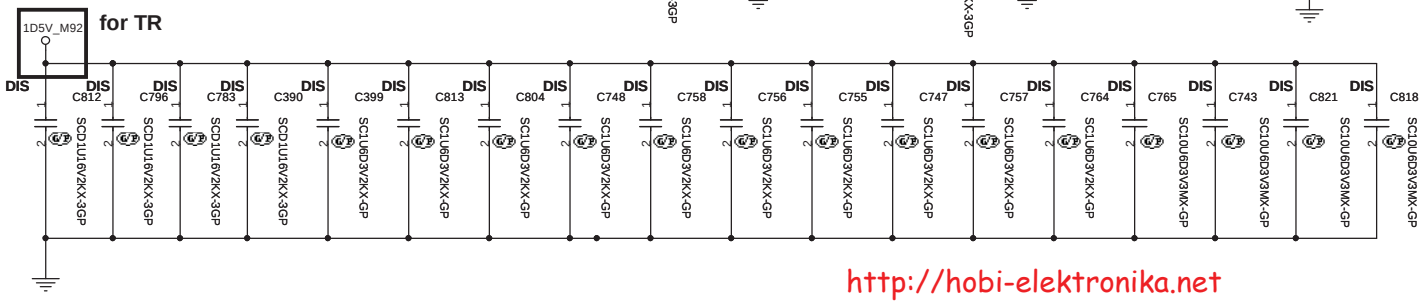


SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U

56,58 DQMB#[0..7]
56,58 RDQSB[0..7]
56,58 WDQSB[0..7]
56,58 MAB[0..12] MAB[0..12]
56,58 MDB[63..0] MDB[63..0]







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Title	DDR3 B0	
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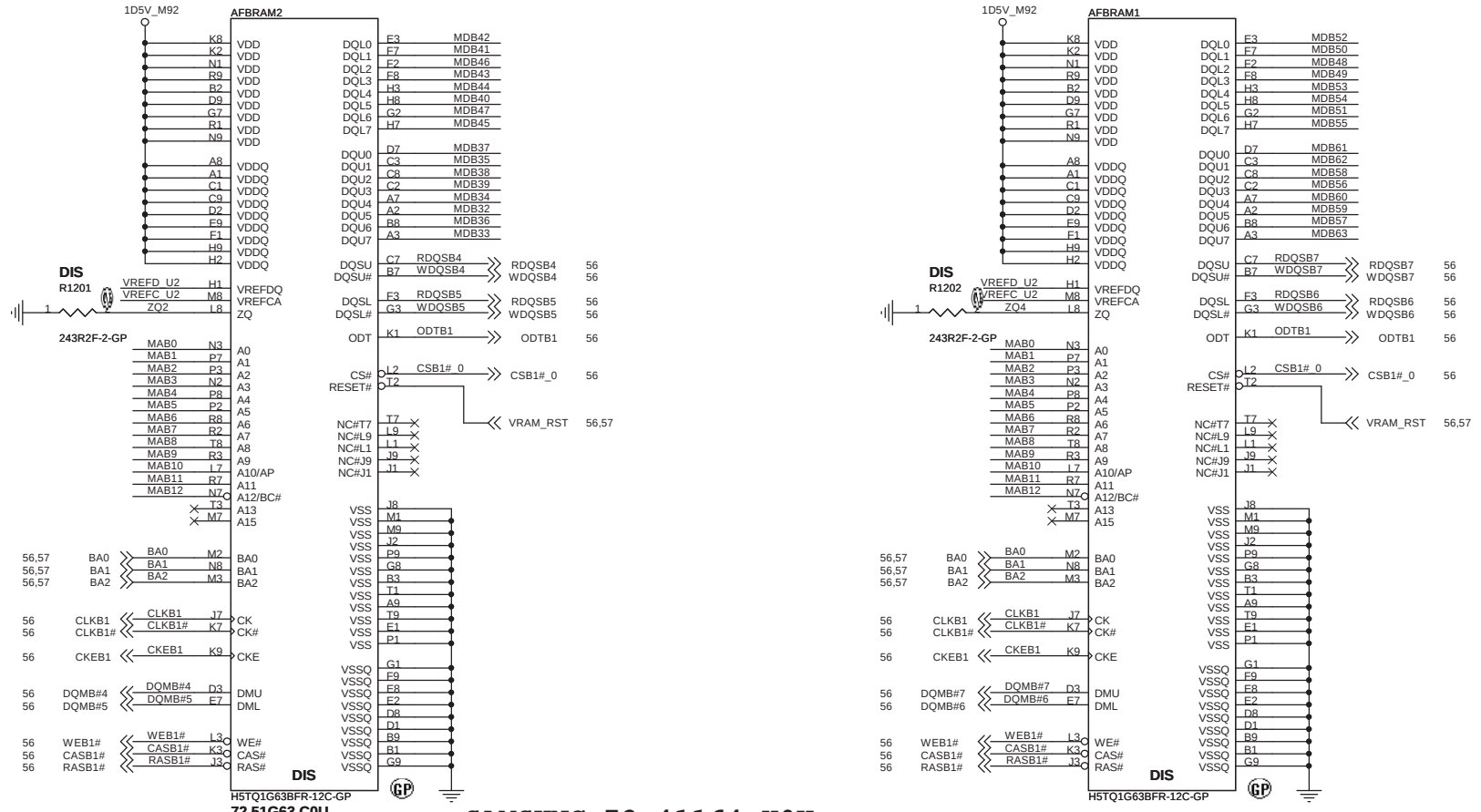
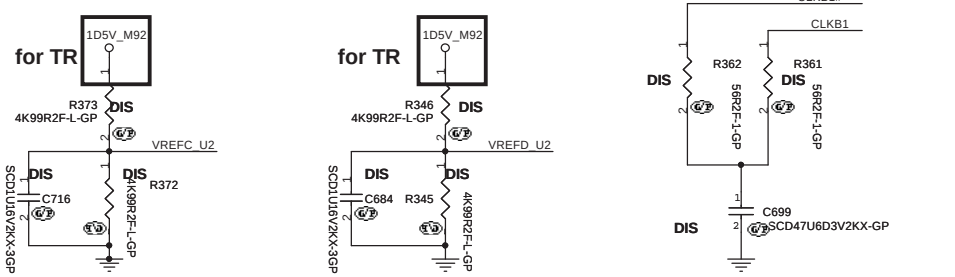
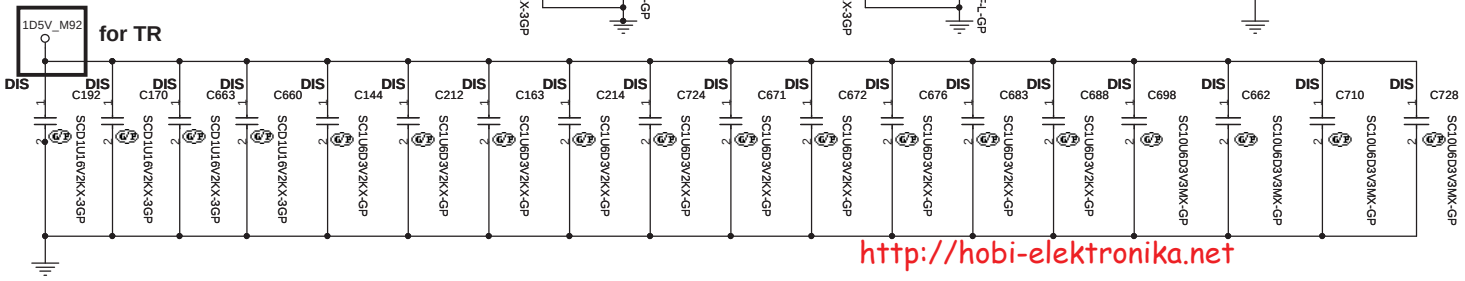


SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U

56,57 DQMB#[0..7]
56,57 RDQSB[0..7]
56,57 WDQSB[0..7]
56,57 MAB[0..12]
56,57 MDB[63..0]





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 DDR3 B1

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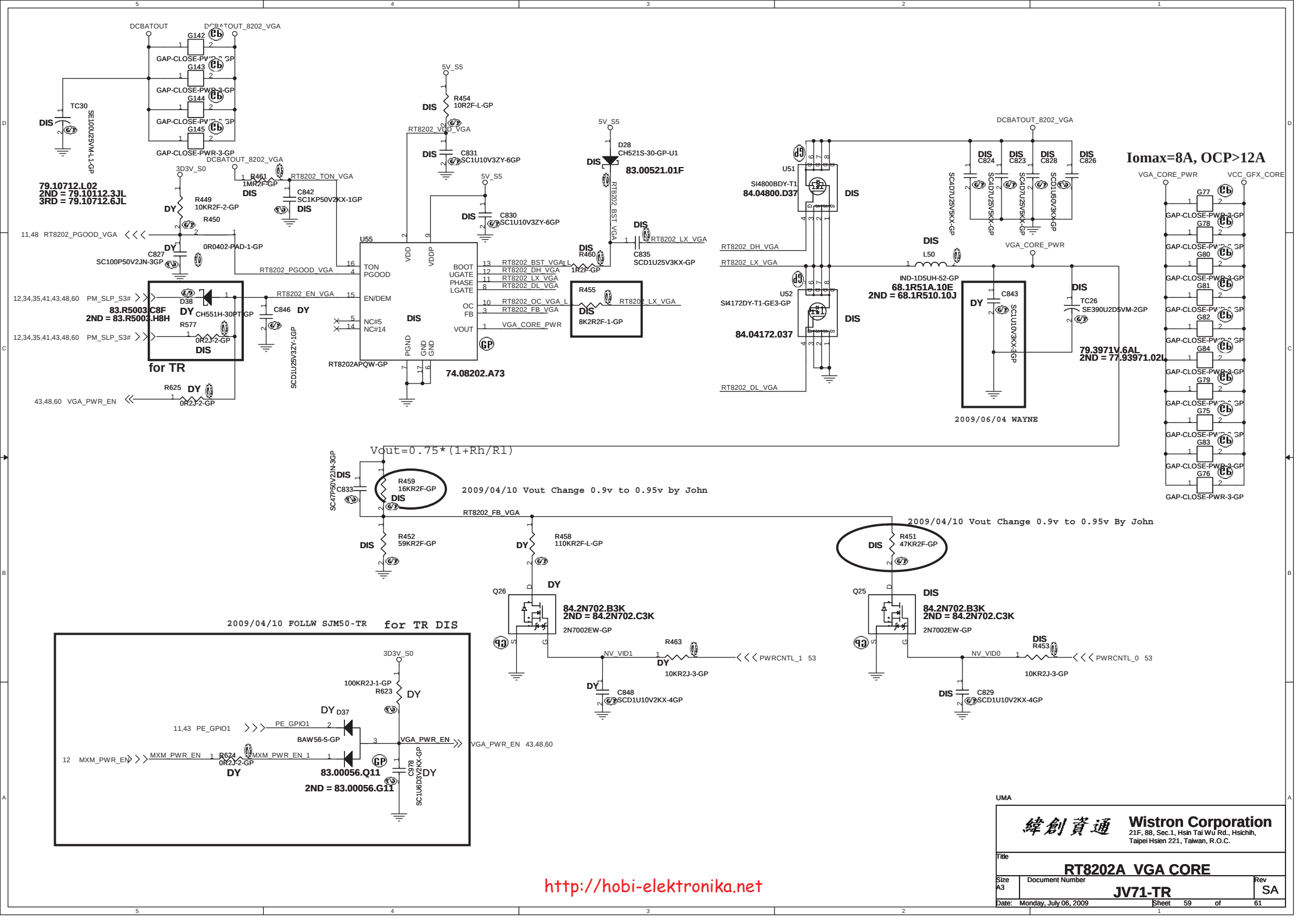

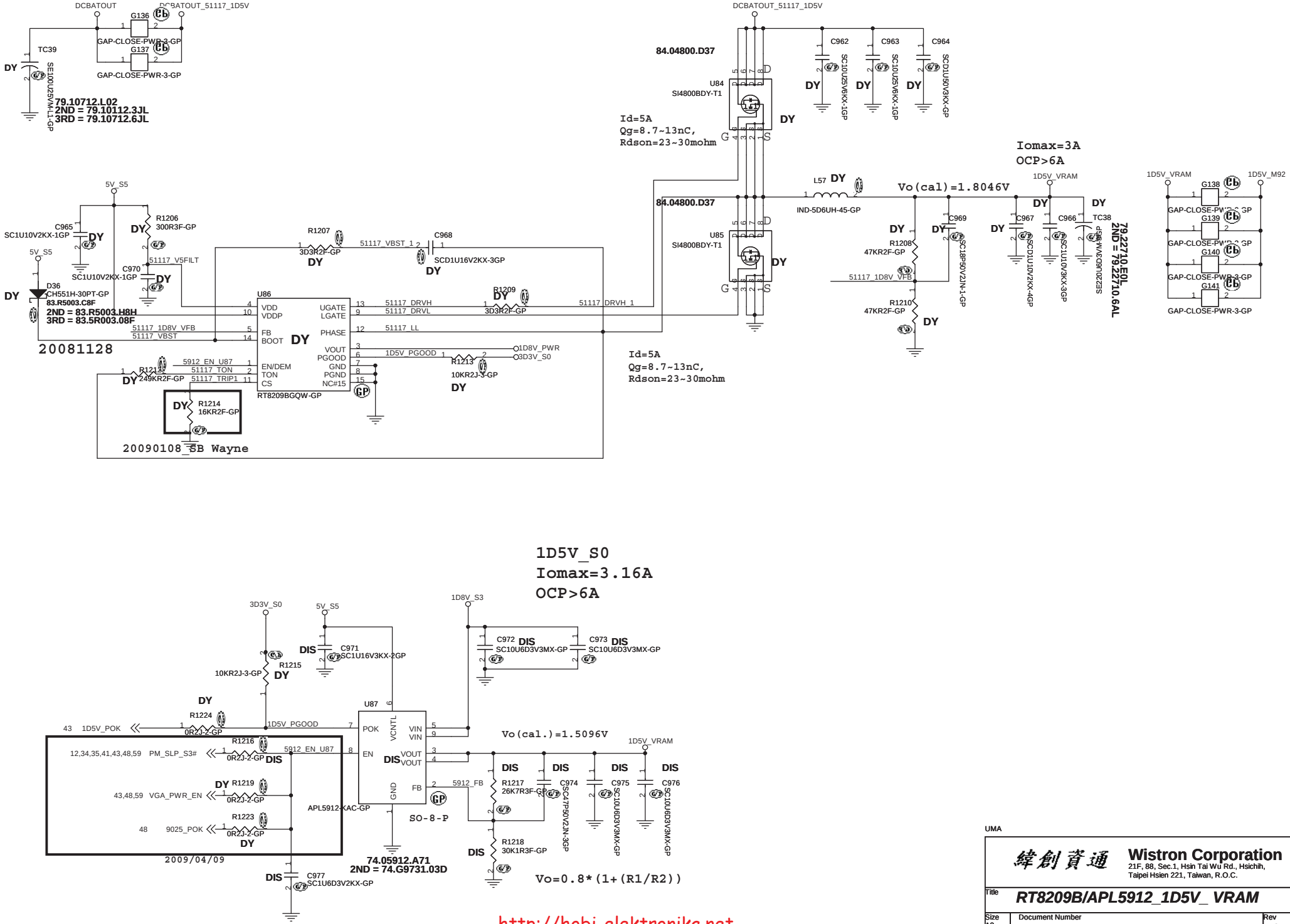

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Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209B/APL5912_1D5V_ VRAM	
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HISTORY**

Size	Document Number	Rev
A3	JV71-TR	SA

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