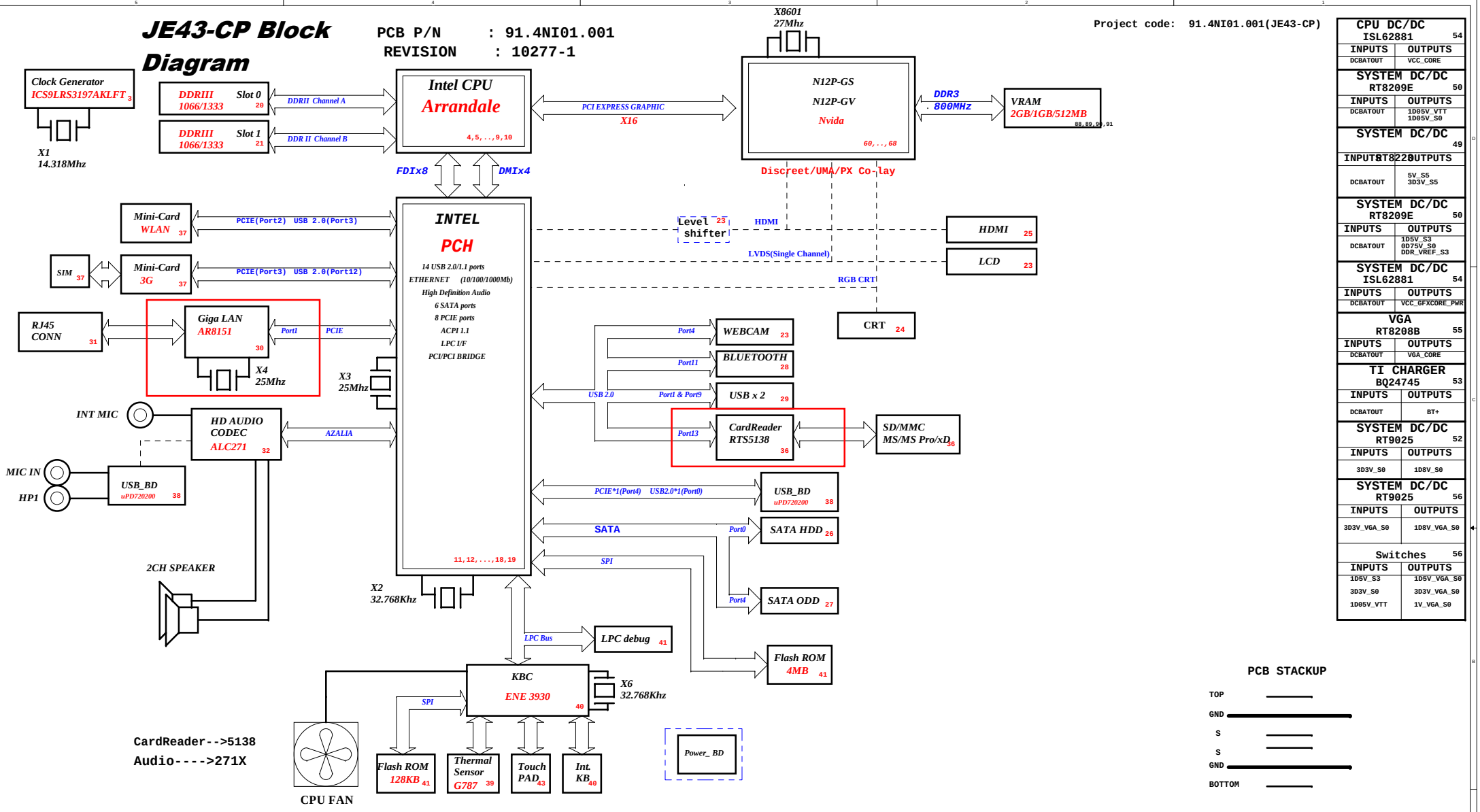
JE43-CP Block Diagram

PCB P/N : 91.4NI01.001
REVISION : 10277-1

Project code: 91.4NI01.001(JE43-CP)



CPU DC/DC ISL62881 54	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT8209E 50	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0

SYSTEM DC/DC 49	
INPUTS RT8220	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 50	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 54	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208B 55	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 53	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 52	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025 56	
INPUTS	OUTPUTS
3D3V_VGA_S0	1D8V_VGA_S0

Switches 56	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1V_VGA_S0

PCB STACKUP

TOP	
GND	
S	
S	
GND	
BOTTOM	

Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Block Diagram

Size	Document Number	Rev
A2	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 1 of 69

PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Hynix 1G 800M N11PGV SKU

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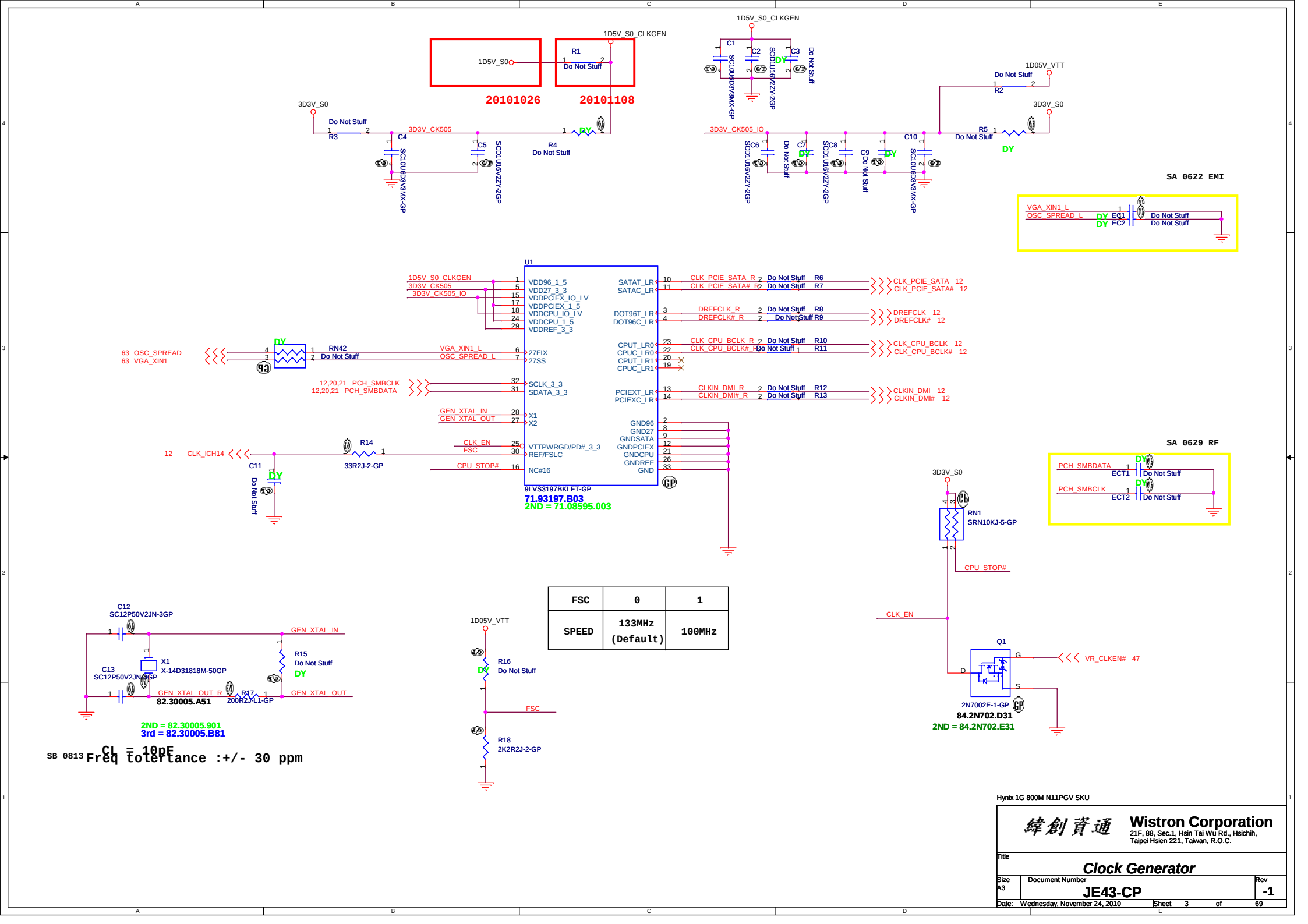
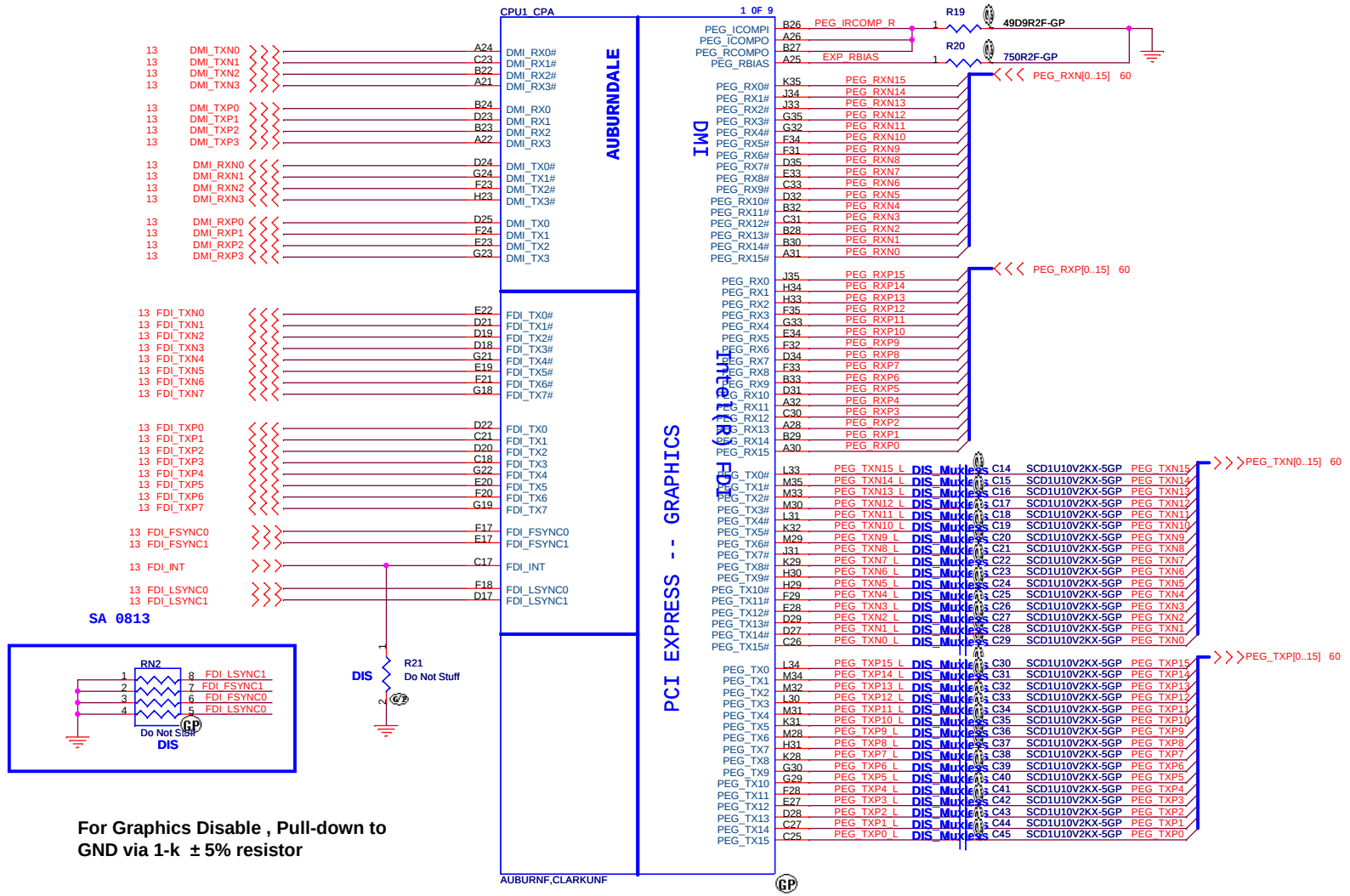
Title: Table of Content

Size: A3 | Document Number: JE43-CP | Rev: -1

Date: Wednesday, November 24, 2010 | Sheet 2 of 69


1D5V_S0_CLKGEN
1D5V_S0
R1
Do Not Stuff
20101026
20101108
3D3V_S0
Do Not Stuff
R3
3D3V_CK505
C4
SC10U6D3V3MX-GP
C5
SCD1U16V2ZY-2GP
R4
Do Not Stuff
DY
C1
C2
C3
Do Not Stuff
1D05V_VTT
R2
R5
3D3V_CK505_IO
C6
C7
C8
C9
C10
SA 0622 EMI
VGA_XIN1_L
OSC_SPREAD_L
EC1
EC2
U1
1D5V_S0_CLKGEN
3D3V_CK505
3D3V_CK505_IO
VDD96_1_5
VDD27_3_3
VDDPCIEX_IO_LV
VDDPCIEX_1_5
VDDCPU_IO_LV
VDDCPU_1_5
VDDREF_3_3
63 OSC_SPREAD
63 VGA_XIN1
RN42
27FIX
27SS
12,20,21 PCH_SMBCLK
12,20,21 PCH_SMBDATA
SCLK_3_3
SDATA_3_3
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
12 CLK_ICH14
R14
33R2J-2-GP
C11
CLK_EN
FSC
CPU_STOP#
VTTPWRGD/PD#_3_3
REF/FSLC
NC#16
9LVS3197BKLFT-GP
71.93197.B03
2ND = 71.08595.003
SATAT_LR
SATAC_LR
CLK_PCIE_SATA_R
CLK_PCIE_SATA# R
CLK_PCIE_SATA 12
CLK_PCIE_SATA# 12
DOT96T_LR
DOT96C_LR
DREFCLK_R
DREFCLK# R
DREFCLK 12
DREFCLK# 12
CPUT_LR0
CPUC_LR0
CPUT_LR1
CPUC_LR1
CLK_CPU_BCLK_R
CLK_CPU_BCLK# R
CLK_CPU_BCLK 12
CLK_CPU_BCLK# 12
PCIEXT_LR
PCIEXC_LR
CLKIN_DMI_R
CLKIN_DMI# R
CLKIN_DMI 12
CLKIN_DMI# 12
GND96
GND27
GNDSATA
GNDPCIEX
GNDPCPU
GNDREF
GND
SA 0629 RF
PCH_SMBDATA
PCH_SMBCLK
ECT1
ECT2
3D3V_S0
RN1
SRN10KJ-5-GP
CPU_STOP#
CLK_EN
Q1
VR_CLKEN# 47
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
C12
SC12P50V2JN-3GP
C13
SC12P50V2JN-3GP
X1
X-14D31818M-50GP
GEN_XTAL_IN
GEN_XTAL_OUT
GEN_XTAL_OUT_R
R15
R17
200R2J-L1-GP
82.30005.A51
2ND = 82.30005.901
3rd = 82.30005.B81
1D05V_VTT
R16
R18
2K2R2J-2-GP
FSC
FSC 0 1
SPEED 133MHz (Default) 100MHz
SB 0813
CL = 10pF
Freq tolerance :+/- 30 ppm
Hynix 1G 800M N11PGV SKU
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size A3
Document Number
JE43-CP
Rev -1
Date: Wednesday, November 24, 2010
Sheet 3 of 69



62.10055.321

3RD = 62.10055.341

4th = 62.10040.611

2ND = 62.10053.561

lab stuff 2nd,3rd and 4 th in BOM

Eng add 1st source(62.10040.611)

Eng do not stuff 4 th in BOM

becasue 4 th have been purge ,so stuff 1st in BOM

but CE said, 4th need stuff in PD if not any concern

0113 -1

Del 3rd 62.10055.341 and 4th 62.10055.321
3rd and 4th have been purged
CE will confrim SQM if it can add BOM
CE will release EC to add to BOM

Rynk 1C 800M N11PGV SKU

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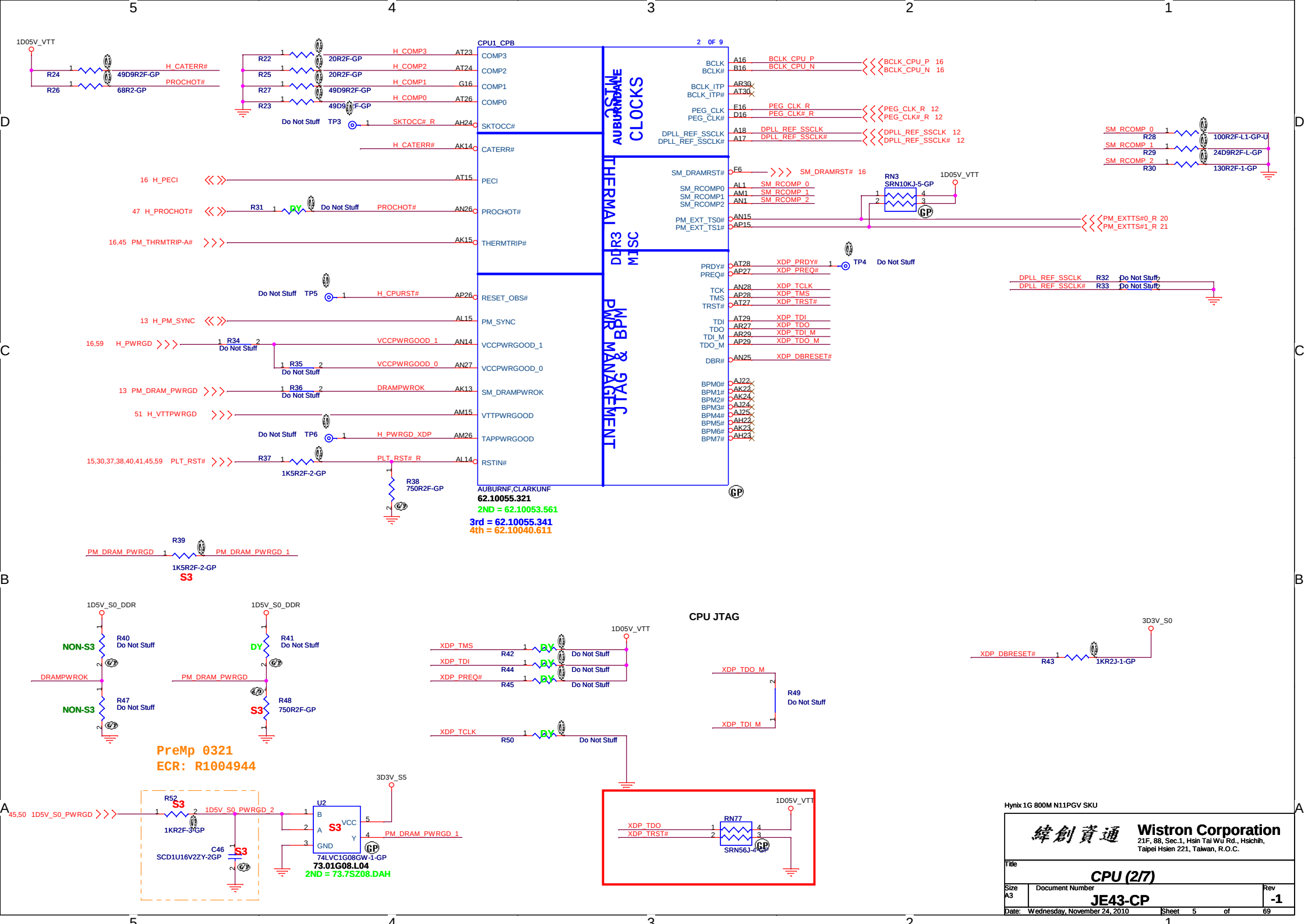
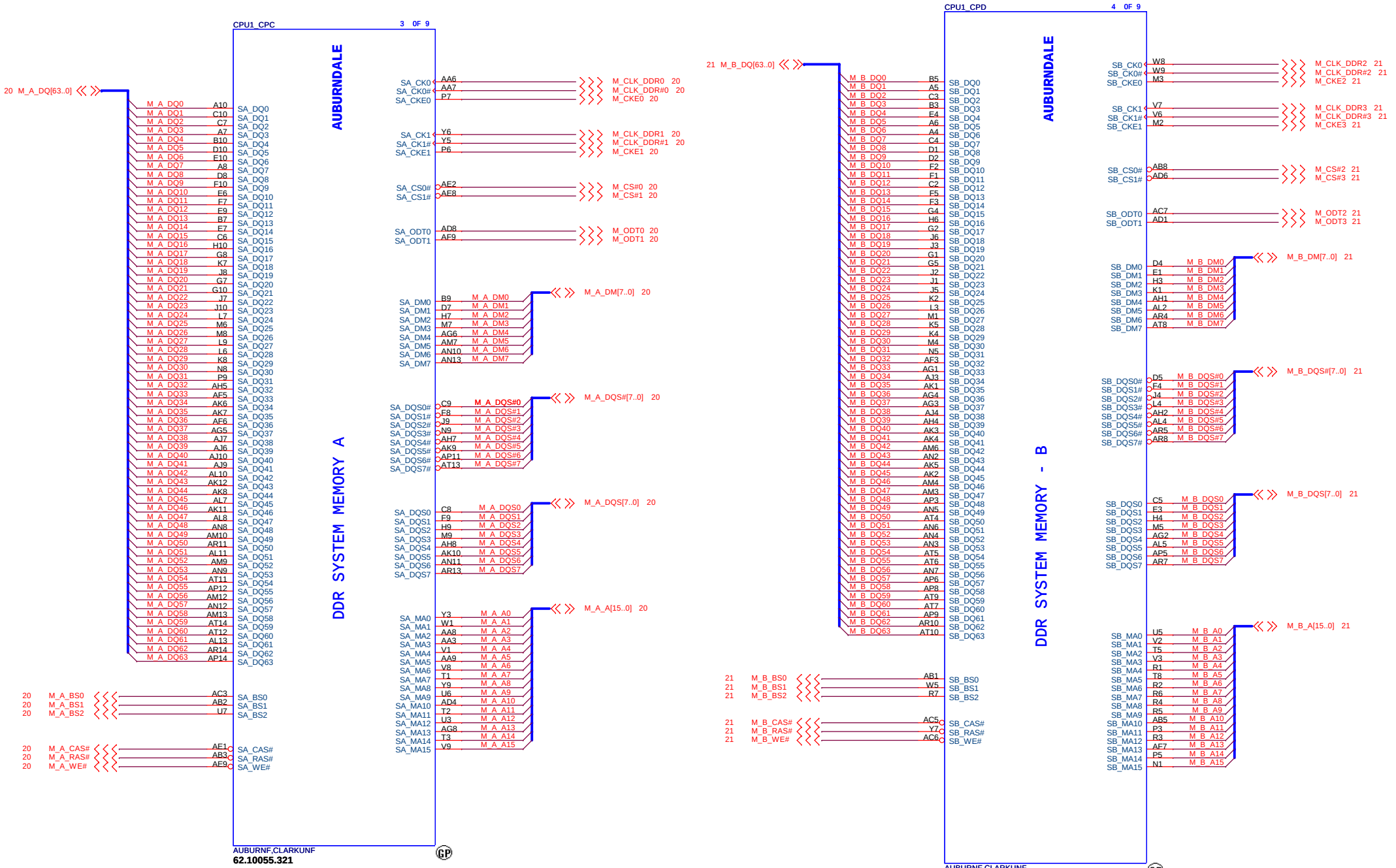
Title: CPU (1/7)		
Size: A3	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 4 of 69	


CPU1_CPB
2 OF 9
CLOCKS
THERMAL
MISC
PWR MANAGEMENT
JTAG
AUBURNDALE
DDR3
AUBURNF,CLARKUNF
62.10055.321
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611
CPU JTAG
PreMp 0321
ECR: R1004944
Hynix 1G 800M N11PGV SKU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (2/7)
JE43-CP
-1
Wednesday, November 24, 2010
Sheet 5 of 69



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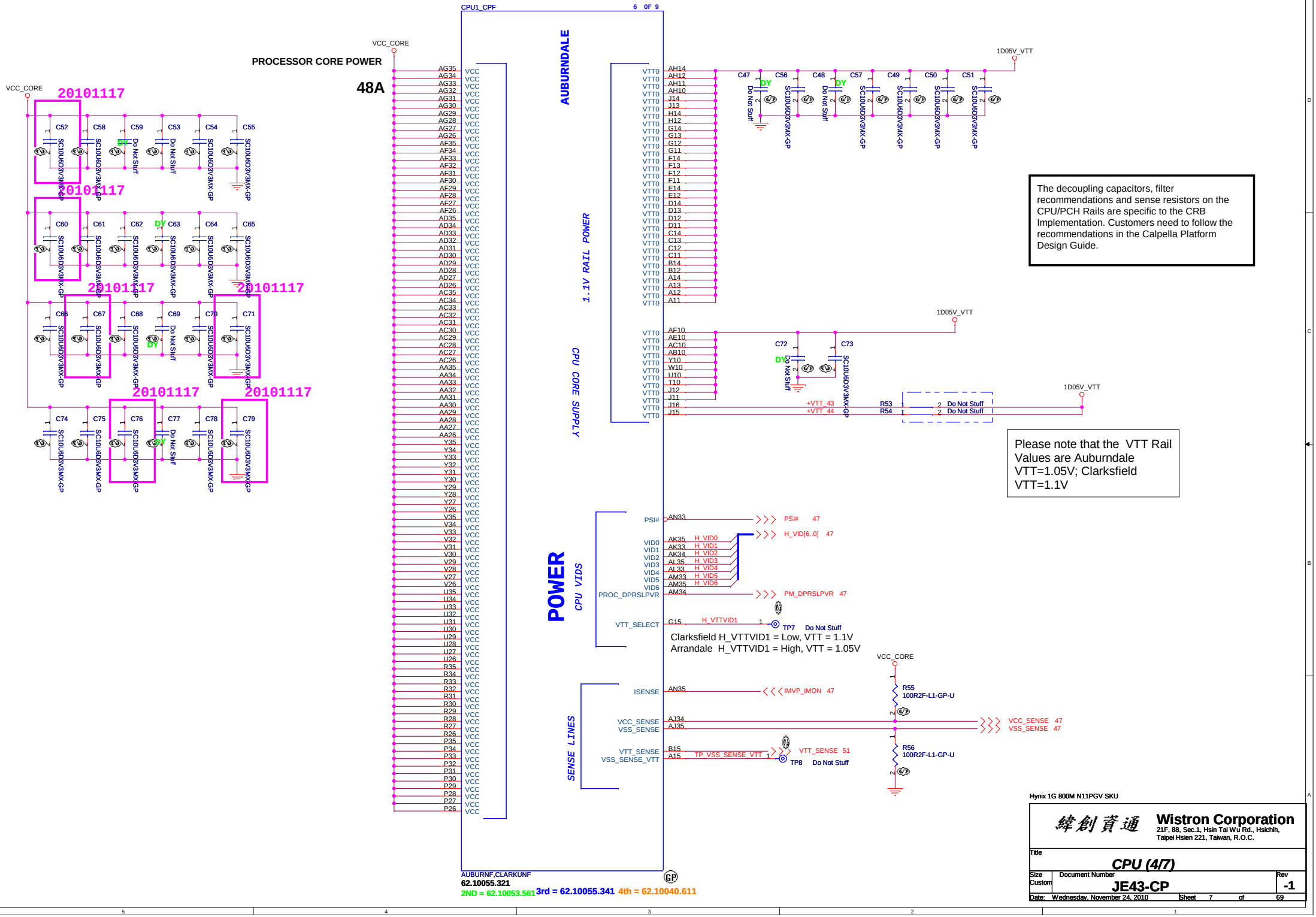
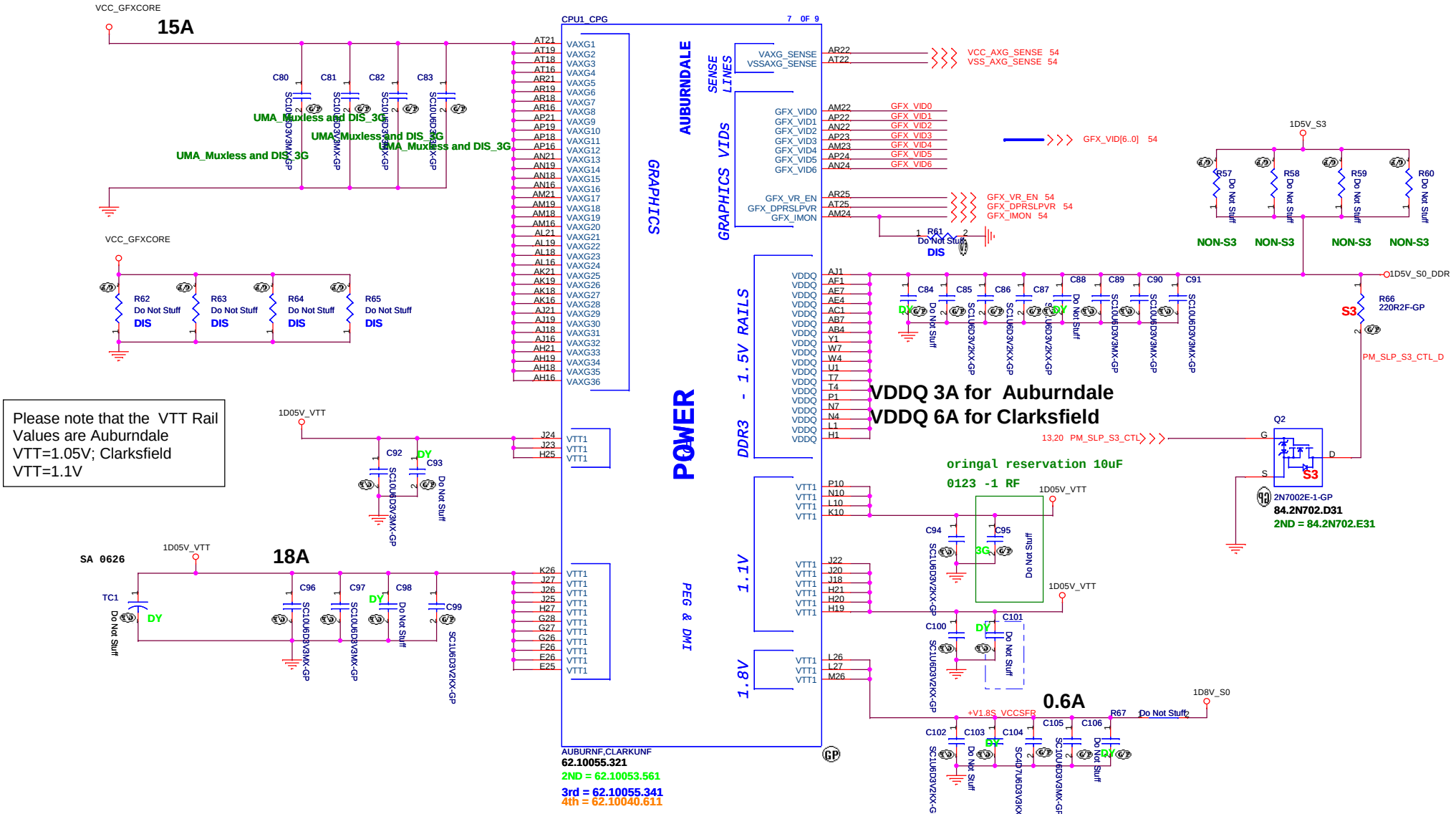
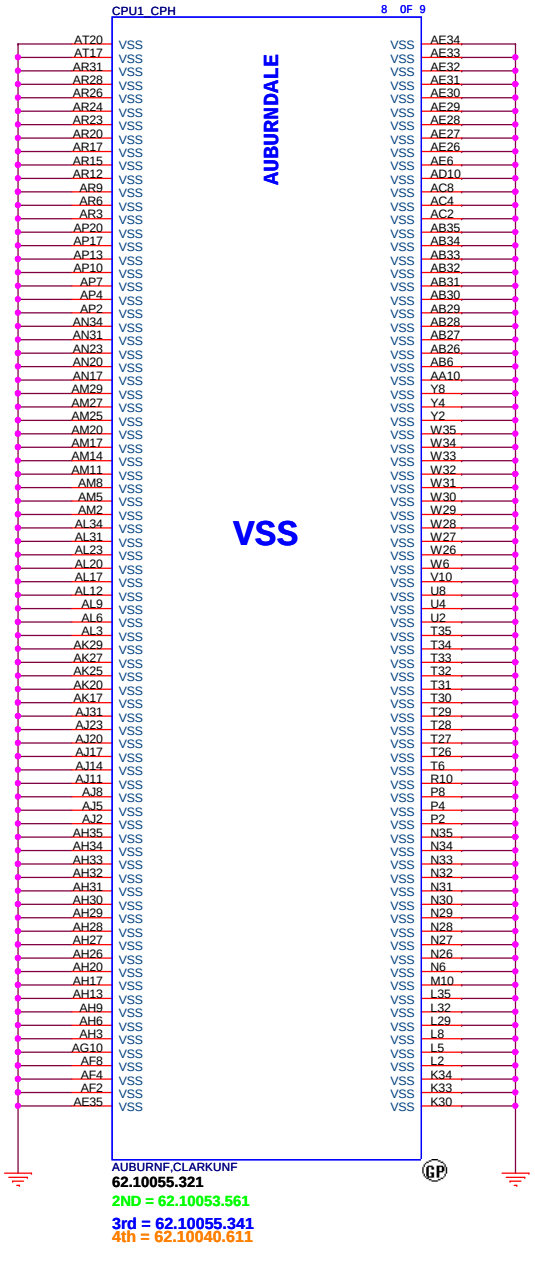
Title: CPU (3/7)

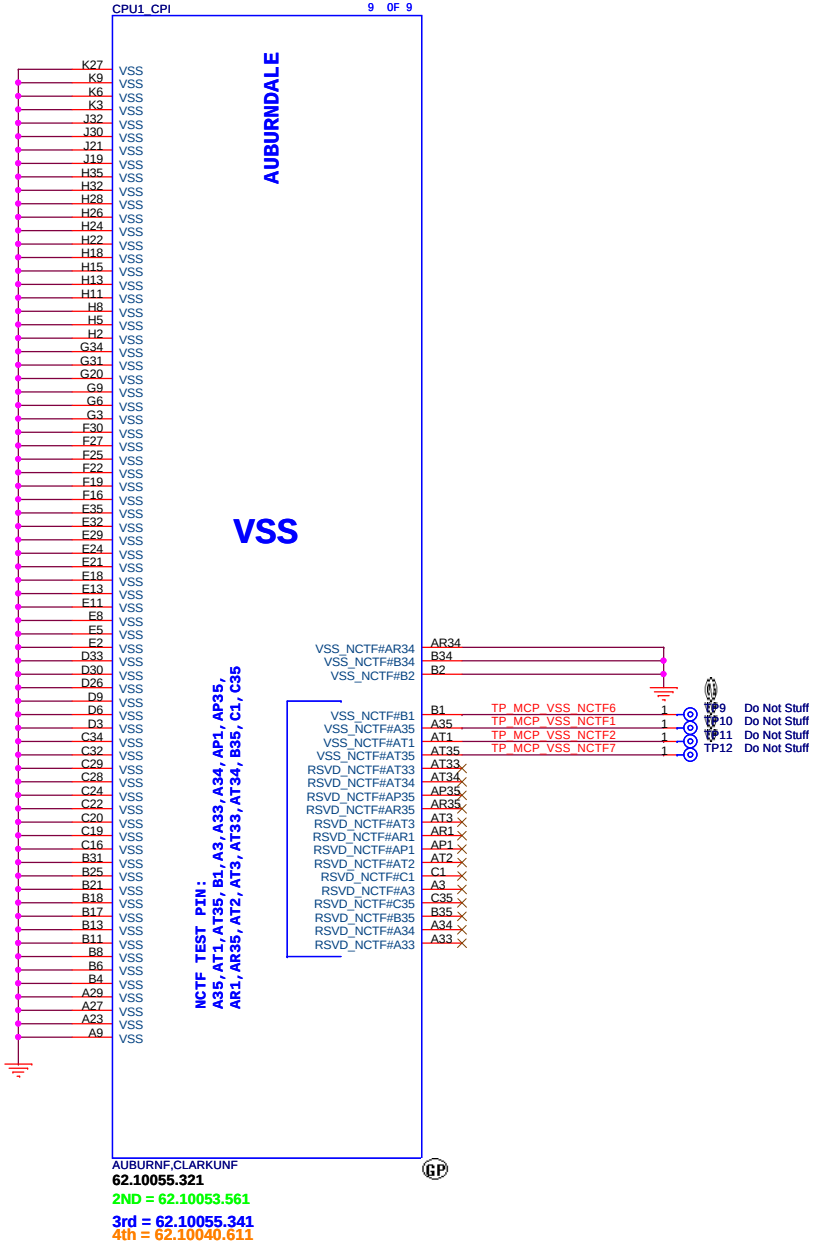
Size: A3 | Document Number: JE43-CP | Rev: -1

Date: Wednesday, November 24, 2010 | Sheet 6 of 69


PROCESSOR CORE POWER
48A
VCC_CORE
CPU1_CPF
6 0F 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
1D05V_VTT
20101117
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
POWER
CPU VIDS
PSI#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PROC_DPRSLPVR
VTT_SELECT
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
SENSE LINES
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
AUBURNF,CLARKUNF
62.10055.321
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611
Hynix 1G 800M N11PGV SKU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4/7)
Size Custom
Document Number
JE43-CP
Rev
-1
Date: Wednesday, November 24, 2010
Sheet 7 of 69


VCC_GFXCORE
15A
C80
C81
C82
C83
UMA_Muxless and DIS_3G
UMA_Muxless and DIS_3G
UMA_Muxless and DIS_3G
VCC_GFXCORE
R62 Do Not Stuff DIS
R63 Do Not Stuff DIS
R64 Do Not Stuff DIS
R65 Do Not Stuff DIS
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
1D05V_VTT
C92
C93
DY
Do Not Stuff
SA 0626
1D05V_VTT
18A
TC1
DY
Do Not Stuff
C96
C97
C98
C99
DY
Do Not Stuff
CPU1_CPG
7 0F 9
AUBURNDALE
GRAPHICS
POWER
DDR3 - 1.5V RAILS
1.1V
1.8V
PEG & DMI
SENSE LINES
GRAPHICS VIDs
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 54
VSS_AXG_SENSE 54
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6
GFX_VID[6..0] 54
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GFX_VR_EN 54
GFX_DPRSLPVR 54
GFX_IMON 54
R61 Do Not Stuff DIS
1D5V_S3
R57 Do Not Stuff
R58 Do Not Stuff
R59 Do Not Stuff
R60 Do Not Stuff
NON-S3
NON-S3
NON-S3
NON-S3
1D5V_S0_DDR
R66 220R2F-GP
S3
PM_SLP_S3_CTL_D
VDDQ 3A for Auburndale
VDDQ 6A for Clarksfield
13,20 PM_SLP_S3_CTL
Q2
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
oringal reservation 10uF
0123 -1 RF
1D05V_VTT
C84
C85
C86
C87
C88
C89
C90
C91
DY
3G
C94
C95
C100
C101
C102
C103
C104
C105
C106
0.6A
1D8V_S0
+V1.8S_VCCSFR
R67 Do Not Stuff
AUBURNF,CLARKUNF
62.10055.321
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611
Hynix 1G 800M N11PGV SKU
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (5/7)
Size A3
Document Number JE43-CP
Rev -1
Date: Wednesday, November 24, 2010
Sheet 8 of 69





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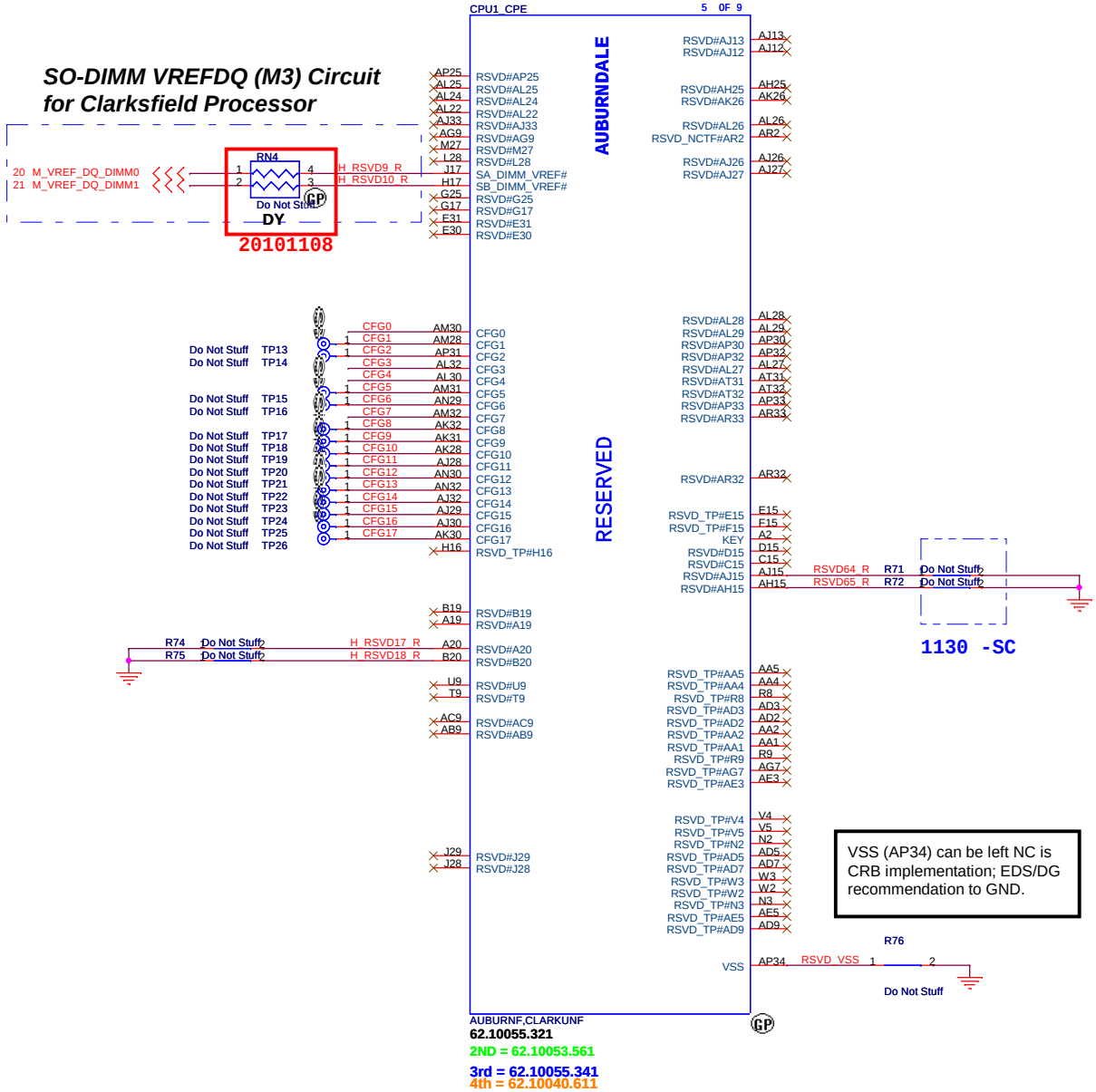
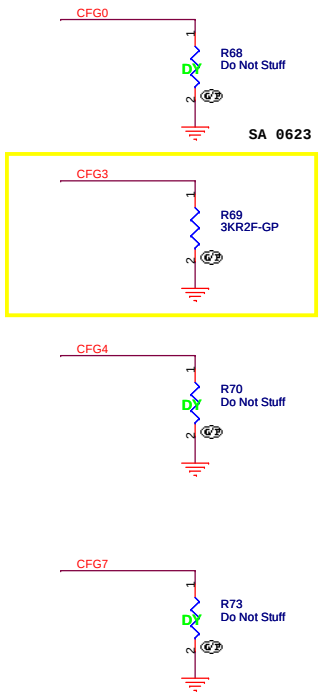
Title: **CPU (6/7)**

Size	Document Number	Rev
A3	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 9 of 69





Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

Hynix 1G 800M N11PGV SKU

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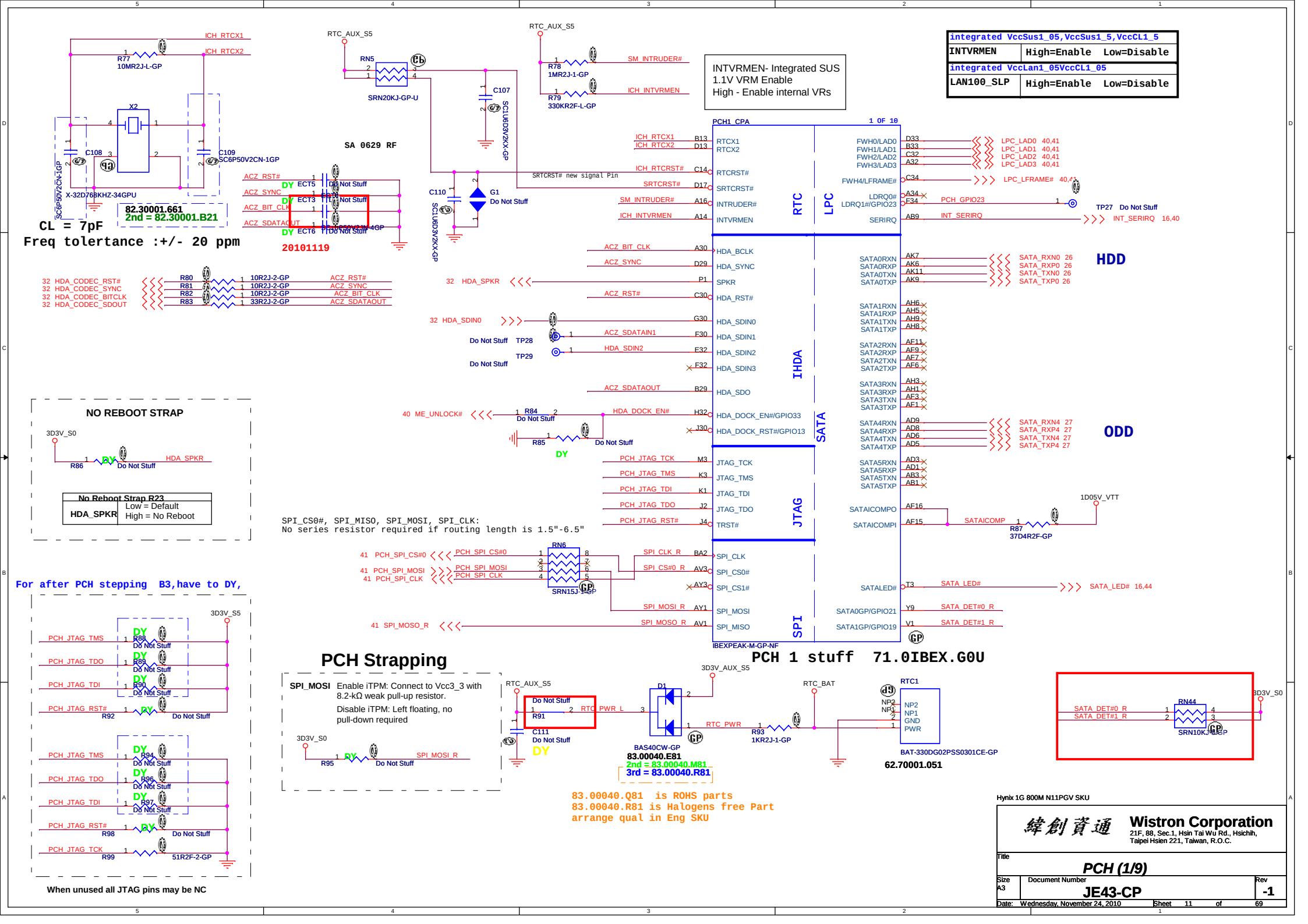
Title		
CPU (7/7)		
Size: A3	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 10 of 69	


integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1_CPA
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M-GP-NF
SA 0629 RF
CL = 7pF
Freq tolertance :+/- 20 ppm
82.30001.661
2nd = 82.30001.B21
20101119
X-32D768KHZ-34GPU
SRN20KJ-GP-U
SRTCRST# new signal Pin
HDD
ODD
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
SRN15J-GP
For after PCH stepping B3,have to DY,
When unused all JTAG pins may be NC
PCH Strapping
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
3rd = 83.00040.R81
BAT-330DG02PSS0301CE-GP
62.70001.051
PCH 1 stuff 71.0IBEX.G0U
83.00040.Q81 is ROHS parts
83.00040.R81 is Halogens free Part
arrange qual in Eng SKU
Hynix 1G 800M N11PGV SKU
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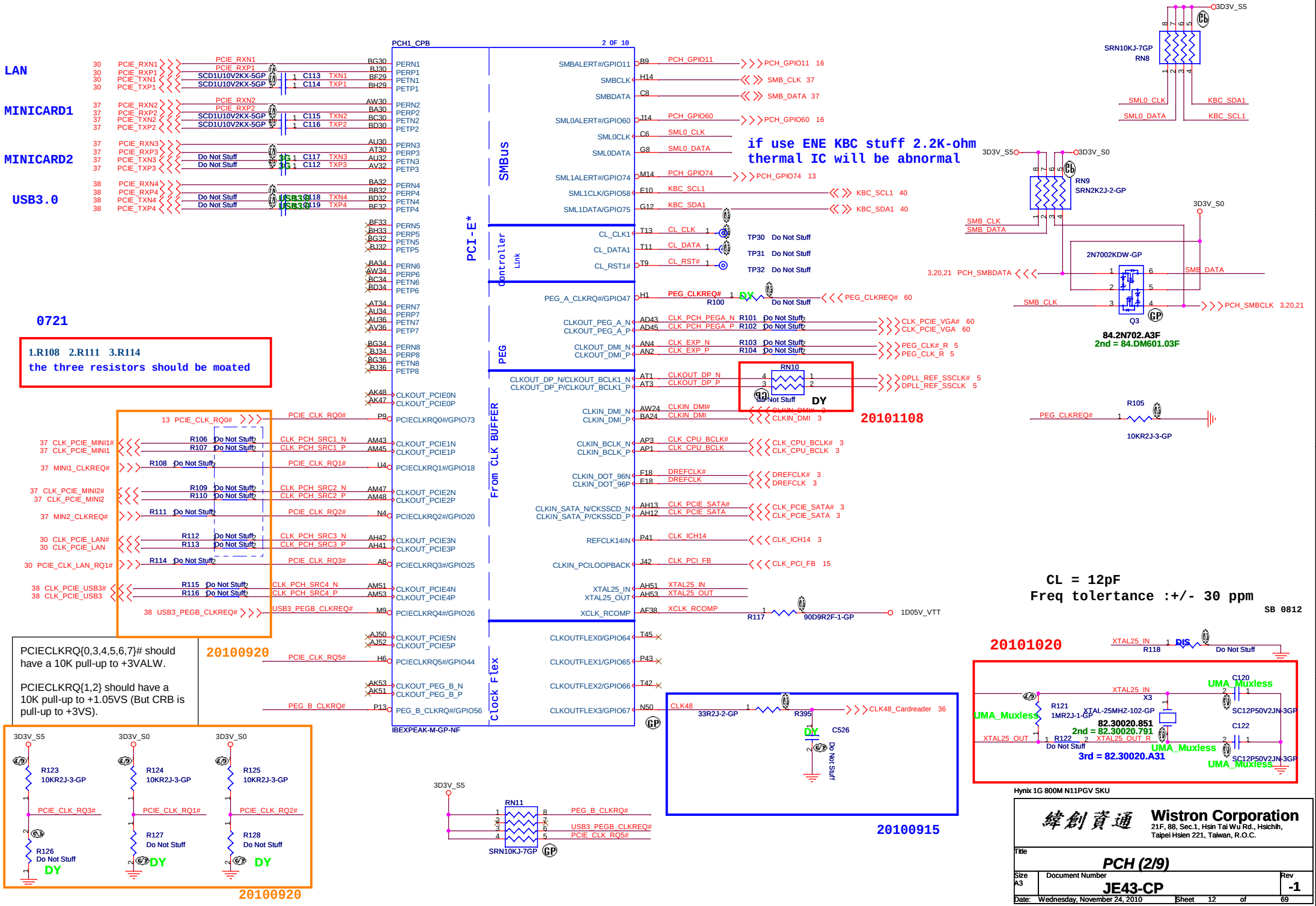
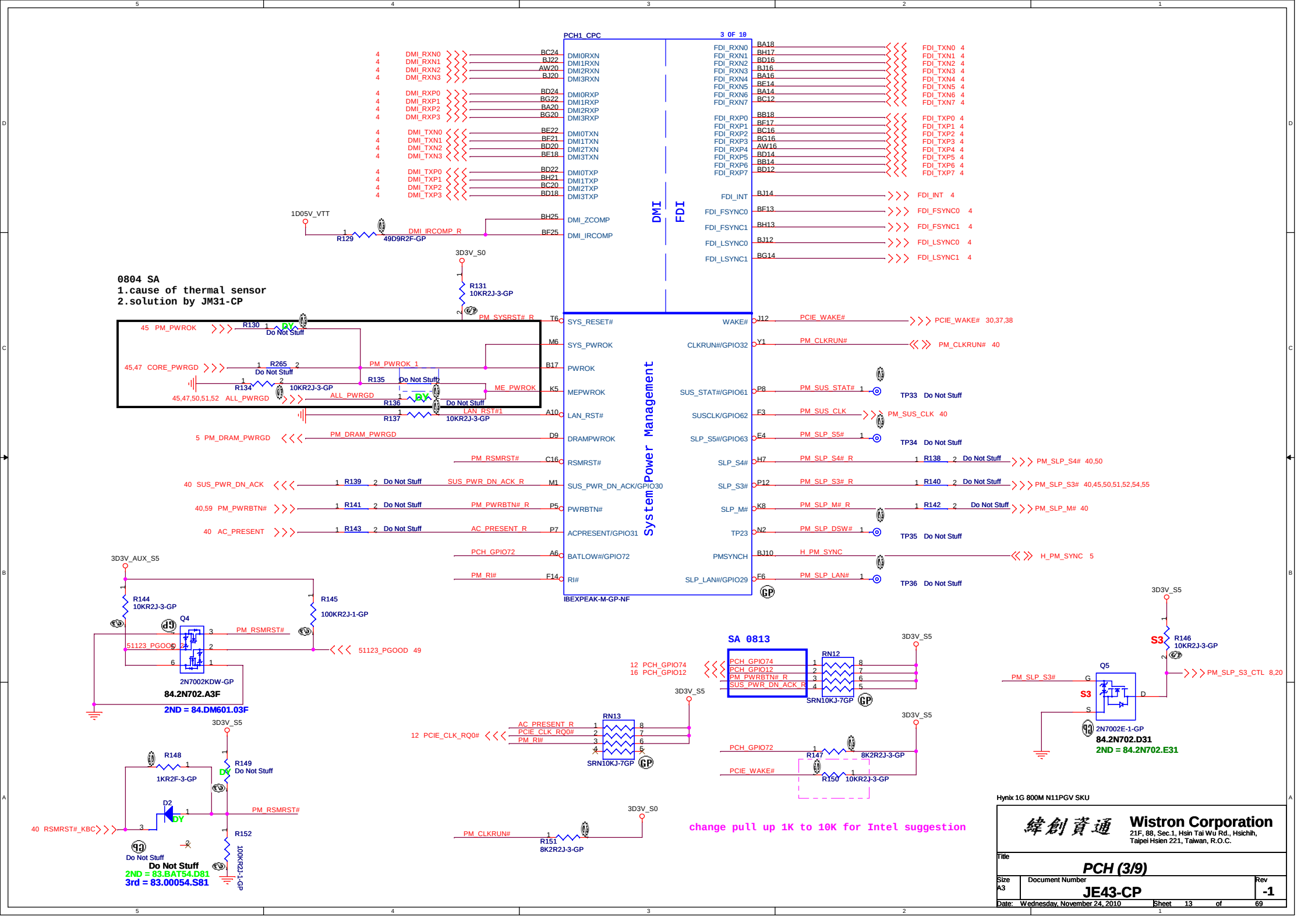
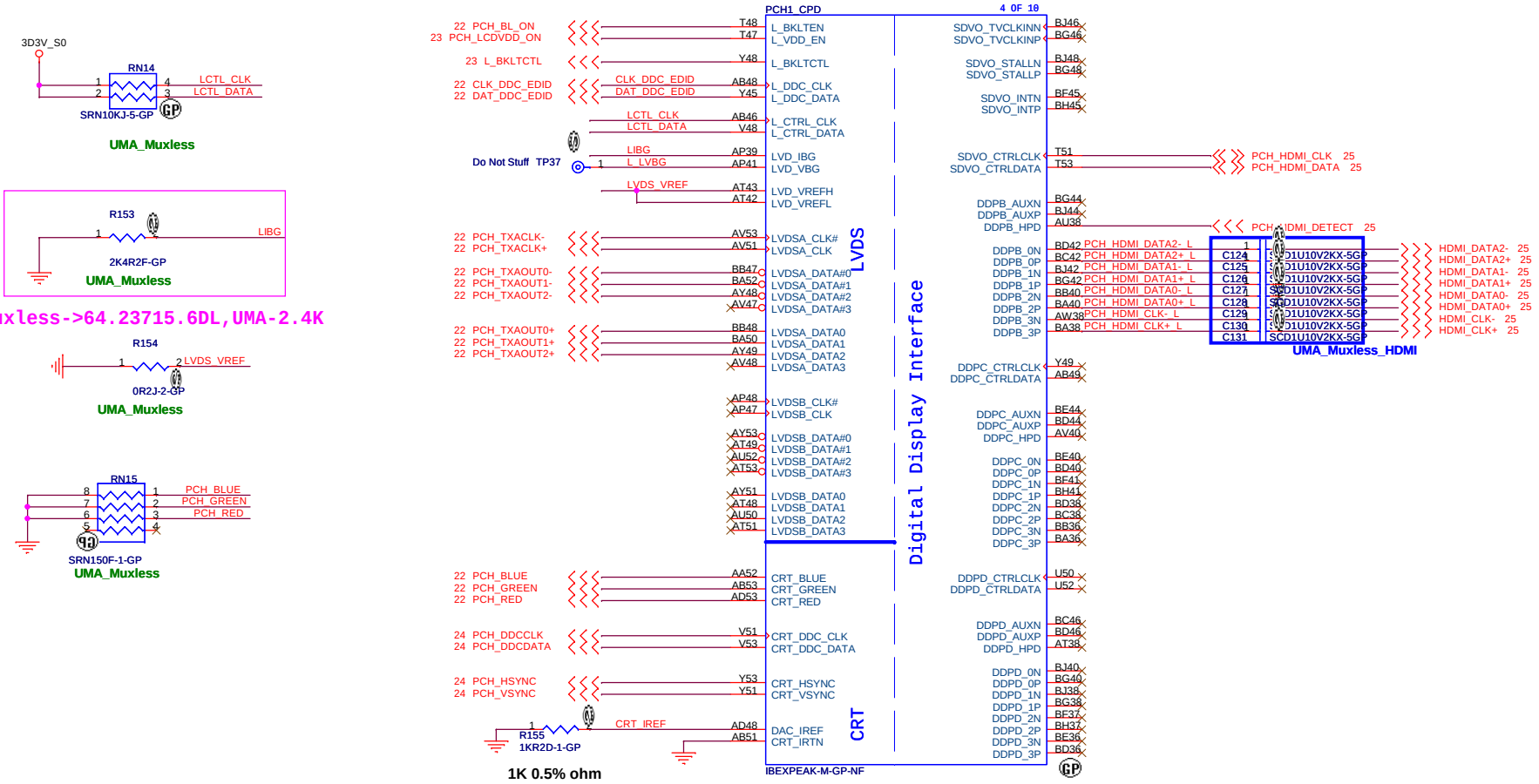
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (1/9)
Size A3
Document Number JE43-CP
Rev -1
Date: Wednesday, November 24, 2010
Sheet 11 of 69


LAN
MINICARD1
MINICARD2
USB3.0
PCH1_CPB
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
0721
1.R108 2.R111 3.R114
the three resistors should be moated
if use ENE KBC stuff 2.2K-ohm
thermal IC will be abnormal
20101108
20100920
20100915
20101020
CL = 12pF
Freq tolertance :+/- 30 ppm
SB 0812
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
Hynix 1G 800M N11PGV SKU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (2/9)
Size A3
Document Number
JE43-CP
Rev -1
Date: Wednesday, November 24, 2010
Sheet 12 of 69


PCH1_CPC
3 0F 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
0804 SA
1.cause of thermal sensor
2.solution by JM31-CP
SA 0813
change pull up 1K to 10K for Intel suggestion
Hynix 1G 800M N11PGV SKU
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
SRN10KJ-7GP
2ND = 83.BAT54.D81
3rd = 83.00054.S81
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (3/9)
JE43-CP
Wednesday, November 24, 2010



Hynix 1G 800M N11PGV SKU

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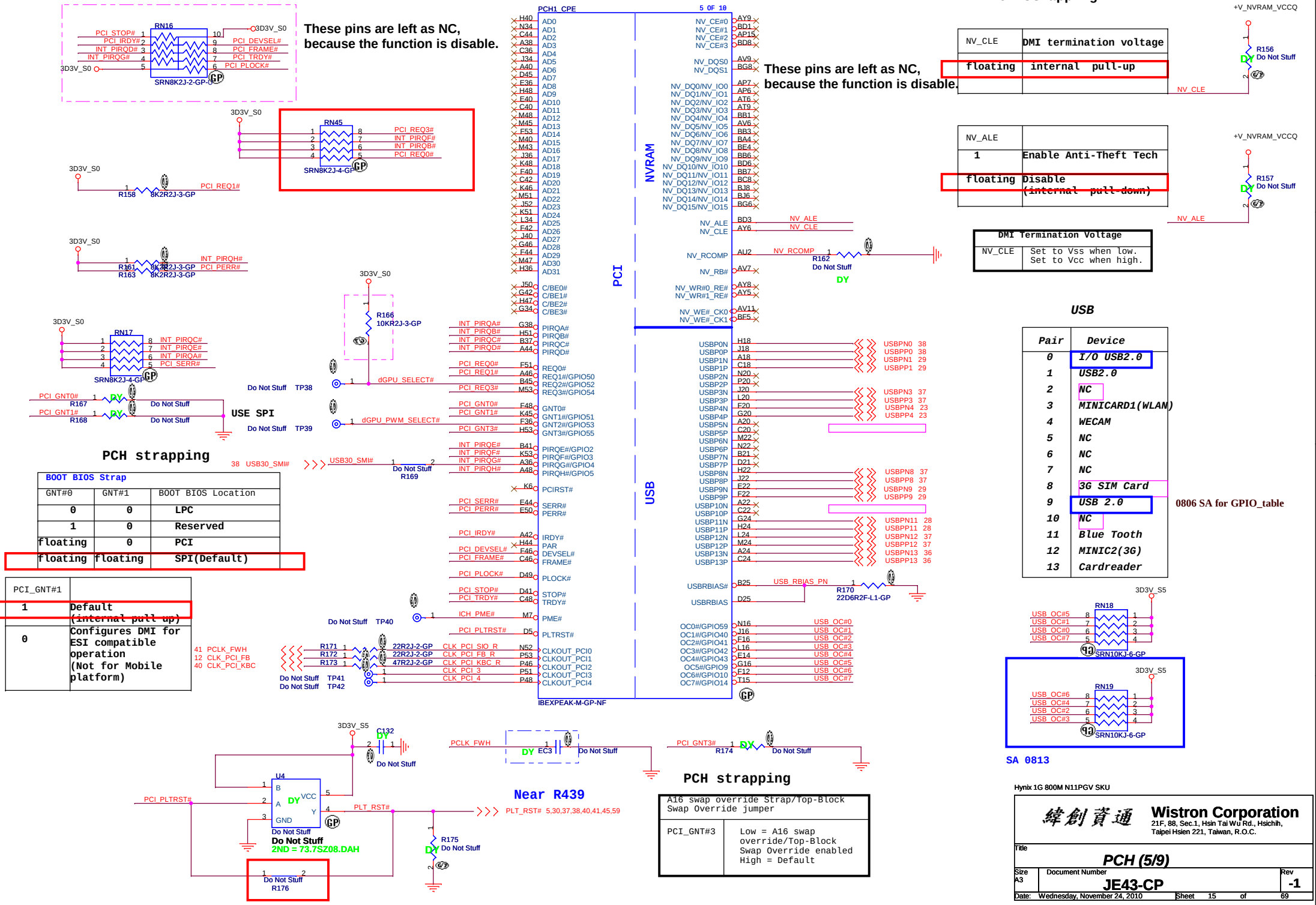
Title	PCH (4/9)	
Size A3	Document Number JE43-CP	Rev -1
Date: Wednesday, November 24, 2010	Sheet 14 of 69	



PCH strapping

NV_CLE	DMI termination voltage
floating	internal pull-up

NV_ALE	
1	Enable Anti-Theft Tech
floating	Disable (internal pull-down)

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

USB

Pair	Device
0	I/O USB2.0
1	USB2.0
2	NC
3	MINICARD1(WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB 2.0
10	NC
11	Blue Tooth
12	MINIC2(3G)
13	Cardreader

PCH strapping

BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI(Default)

PCI_GNT#1	
1	Default (internal pull up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title: PCH (5/9)
Size: A3 | Document Number: JE43-CP | Rev: -1
Date: Wednesday, November 24, 2010 | Sheet 15 of 69

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

PCH1_CPF
6 OF 10
IBEXPEAK-M-GP-NF

MISC
GPIO
CPU
NCTF
RSVD

PCH_GPIO0 Y3 BMBUSY#/GPIO0
EC_SMI# C38 TACH1/GPIO1
25 PX_HDMI# PX_HDMI# D37 TACH2/GPIO6
40 EC_SCI# EC_SCI# J32 TACH3/GPIO7
40 EC_SWI# EC_SWI# F10 GPIO8
13 PCH_GPIO12 PCH_GPIO12 K9 LAN_PHY_PWR_CTRL/GPIO12
PCH_GPIO15 T7 GPIO15
60 DGPU_HOLD_RST# DGPU_HOLD_RST# AA2 SATA4GP/GPIO16
55,56 DGPU_PWROK DGPU_PWROK F38 TACH0/GPIO17
PCH_GPIO22 Y7 SCLOCK/GPIO22
Do Not Stuff TP44 PCH_GPIO24 H10 GPIO24
Do Not Stuff TP45 PCH_GPIO27 AB12 GPIO27
Do Not Stuff TP54 PCH_GPIO28 V13 GPIO28
STP_PCI# M11 STP_PCI#/GPIO34
PCH_GPIO35 V6 SATACLKREQ#/GPIO35
56 DGPU_PWR_EN# DGPU_PWR_EN# AB7 SATA2GP/GPIO36
dGPU_PRSNT# AB13 SATA3GP/GPIO37
Do Not Stuff TP47 dGPU_EDID V3 SLOAD/GPIO38
PCH_GPIO39 P3 SDATAOUT0/GPIO39
PCH_GPIO45 H3 PCIECLKRQ6#/GPIO45
RST_GATE F1 PCIECLKRQ7#/GPIO46
PCH_GPIO48 AB6 SDATAOUT1/GPIO48
PSW_CLR# AA4 SATA5GP/GPIO49
PCH_GPIO57 F8 GPIO57

CLKOUT_PCIE6N AH45
CLKOUT_PCIE6P AH46
CLKOUT_PCIE7N AF48
CLKOUT_PCIE7P AF47
A20GATE U2 KA20GATE 40
CLKOUT_BCLK0_N/CLKOUT_PCIE8N AM3 BCLK_CPU_N_R
CLKOUT_BCLK0_P/CLKOUT_PCIE8P AM1 BCLK_CPU_P_R
PECI BG10 H_PECI 5
RCIN# T1 KBRCIN# 40
PROCPWRGD BE10 H_PWRGD 5,59
THRMTRIP# BD10 PCH_THERMTRIP_R
TP1 BA22
TP2 AW22
TP3 BB22
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AF13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB42
NC_4 AB41
NC_5 T39
INIT3_3V# P6 INIT3_3V#
TP24 C10

R564 Do Not Stuff
R585 Do Not Stuff
BCLK_CPU_N 5
BCLK_CPU_P 5
20101115
R177 56R2J-4-GP 1D05V_VTT
R178 Do Not Stuff DY
PM_THRMTRIP-A# 5,45
Placed Within 2" from PCH

RN21 SRN10KJ-7GP 3D3V_S5
12 PCH_GPIO11
12 PCH_GPIO60
PCH_GPIO28
PCH_GPIO45 R179 8K2R2J-3-GP
PCH_GPIO15 R180 1KR2J-1-GP

PSW_CLR# G2 Do Not Stuff

RN22 SRN10KJ-7GP 3D3V_S0
11,44 SATA_LED#
PCH_GPIO39
11,40 INT_SERIRQ
PSW_CLR#

RP1 SRN10KJ-L3-GP 3D3V_S0
STP_PCI#
PCH_GPIO0
dGPU_EDID
EC_SMI#
EC_SCI#
PX_HDMI#

Do Not Stuff TP48 TP49 PCH_TP95 PCH_TP96
Do Not Stuff TP50 PCH_TP97
Do Not Stuff TP51 PCH_TP98
Do Not Stuff TP52

NCTF TEST PIN:
A4,A49,A5,A50,A52,A53,B2,B53,BE1,
BE53,BF1,BF53,BH1,BH53,BJ1,BJ2,BJ4,
BJ49,BJ5,BJ50,BJ52,BJ53,D1,D53,E1,E53

1D5V_S3
R181 1KR2F-3-GP S3
DDR3_DRAMRST# 20,21
NON-S3
R182 Do Not Stuff
2ND = 84.2N702.E31
84.2N702.D31
2N7002E-1-GP
Q6
3D3V_S5
R183 10KR2F-2-GP S3
RST_GATE
C133 SCD047U25V2KX-GP
SM_DRAMRST# 5
R184 100KR2F-L1-GP
20100922

3D3V_S0
R269 UMA_512M Do Not Stuff
PCH_GPIO48
R270 1G_2G 10KR2J-3-GP
UMA/512M : HIGH
1G : LOW
R271 2G Do Not Stuff
PCH_GPIO35
R272 UMA_512M_1G 10KR2J-3-GP
2G : HIGH
UMA/1G/512M : LOW
Hynix 1G 800M N11PGV SKU

H: No SG function
L: SG Support
3D3V_S0
R186 Do Not Stuff
DIS_UMA
dGPU_PRSNT#
R190 10KR2J-3-GP
Muxless

3D3V_S5
UMA_Muxless
R187 10KR2J-3-GP
PCH_GPIO57
R191 Do Not Stuff
UMA_DISCRETE#
Optimus: HIGH
UMA: HIGH
DIS ONLY: LOW
DIS

20100921
3D3V_S0
UMA_800M
R266 10KR2J-3-GP
PCH_GPIO22
R268 Do Not Stuff
900M
VRAM Frequency
VRAM 800Mhz : PULL HIGH
VRAM 900Mhz : PULL LOW

3D3V_S0
R188 DY Do Not Stuff
DGPU_PWR_EN#
R192 10KR2J-3-GP

3D3V_S0
R189 DY Do Not Stuff
DGPU_HOLD_RST#
R193 10KR2J-3-GP

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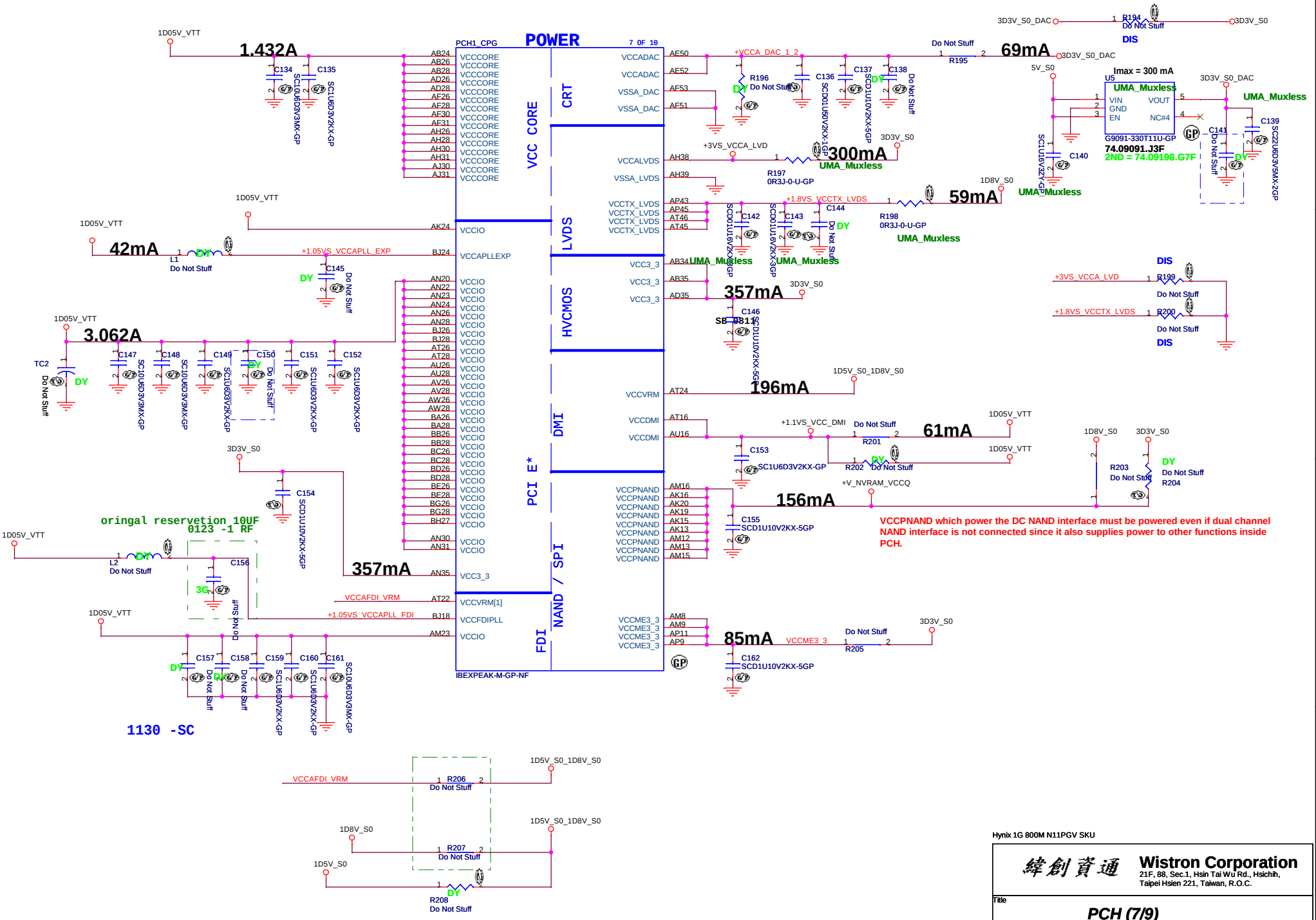
Title: PCH (6/9)
Size: A3
Document Number: JE43-CP
Rev: -1
Date: Wednesday, November 24, 2010
Sheet 16 of 69



Hynix 1G 800M N11PGV SKU

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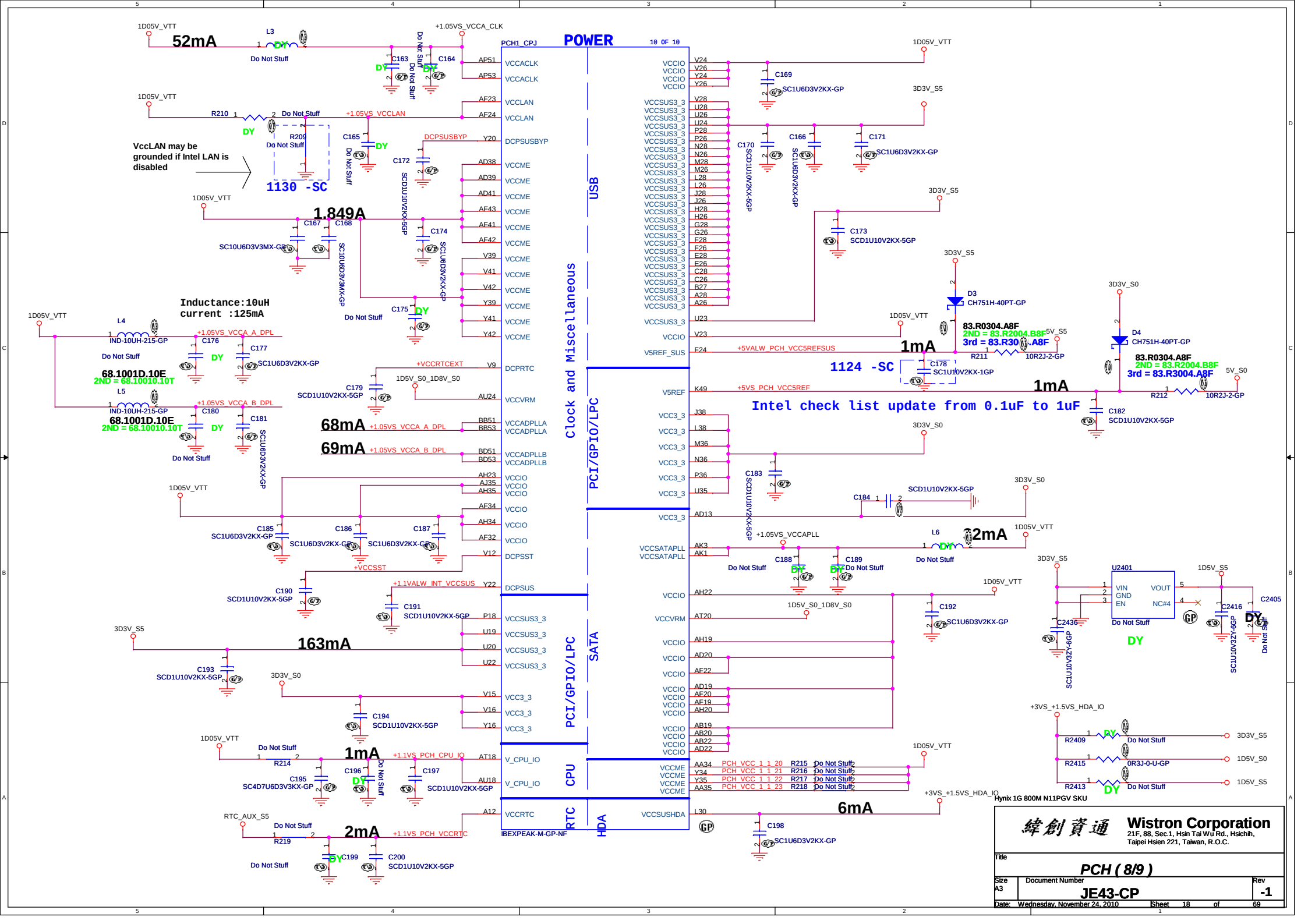
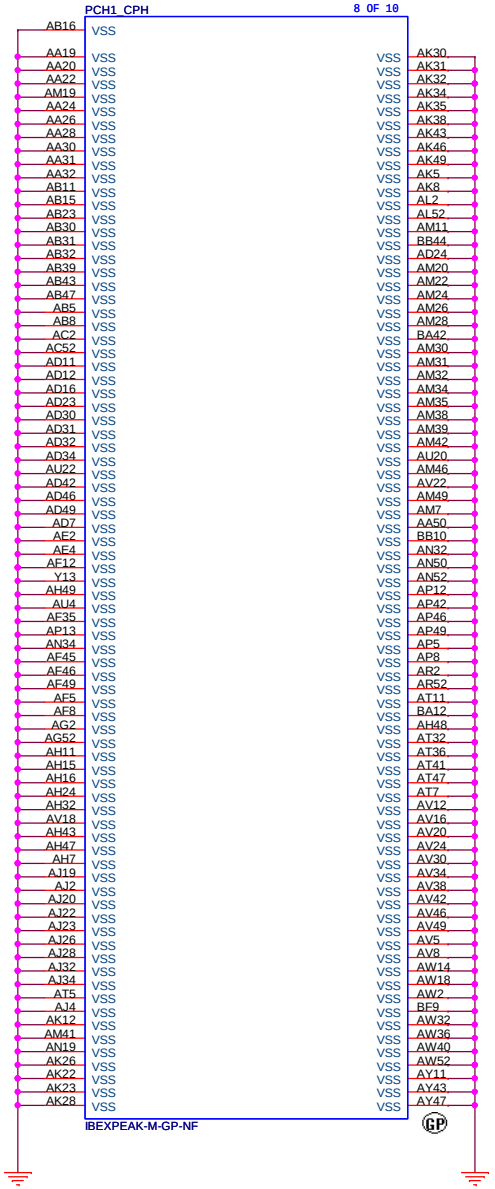
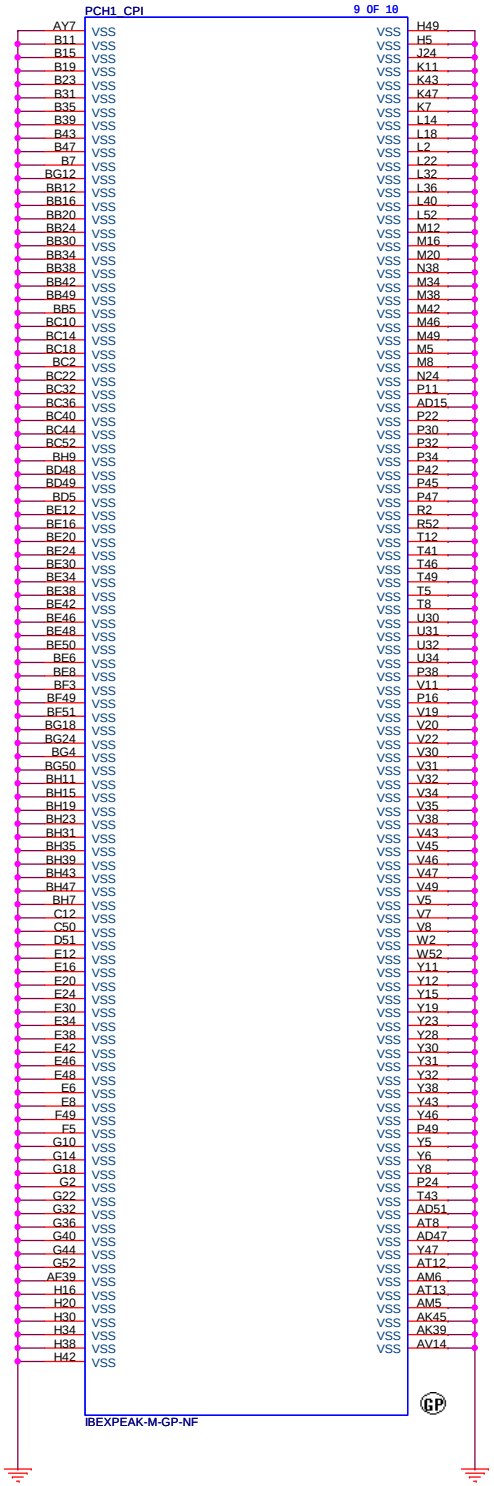
Title	PCH (7/9)	
Size A3	Document Number JE43-CP	Rev -1
Date: Wednesday, November 24, 2010	Sheet 17 of 69	


POWER
10 OF 10
PCH1_CPJ
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
52mA
1.849A
Inductance:10uH
current :125mA
68.1001D.10E
2ND = 68.10010.10T
68mA
69mA
163mA
1mA
2mA
6mA
1124 -SC
1130 -SC
VccLAN may be grounded if Intel LAN is disabled
Intel check list update from 0.1uF to 1uF
Hynix 1G 800M N11PGV SKU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
JE43-CP
Rev -1
Date: Wednesday, November 24, 2010
Sheet 18 of 69





Hynix 1G 800M N11PGV SKU

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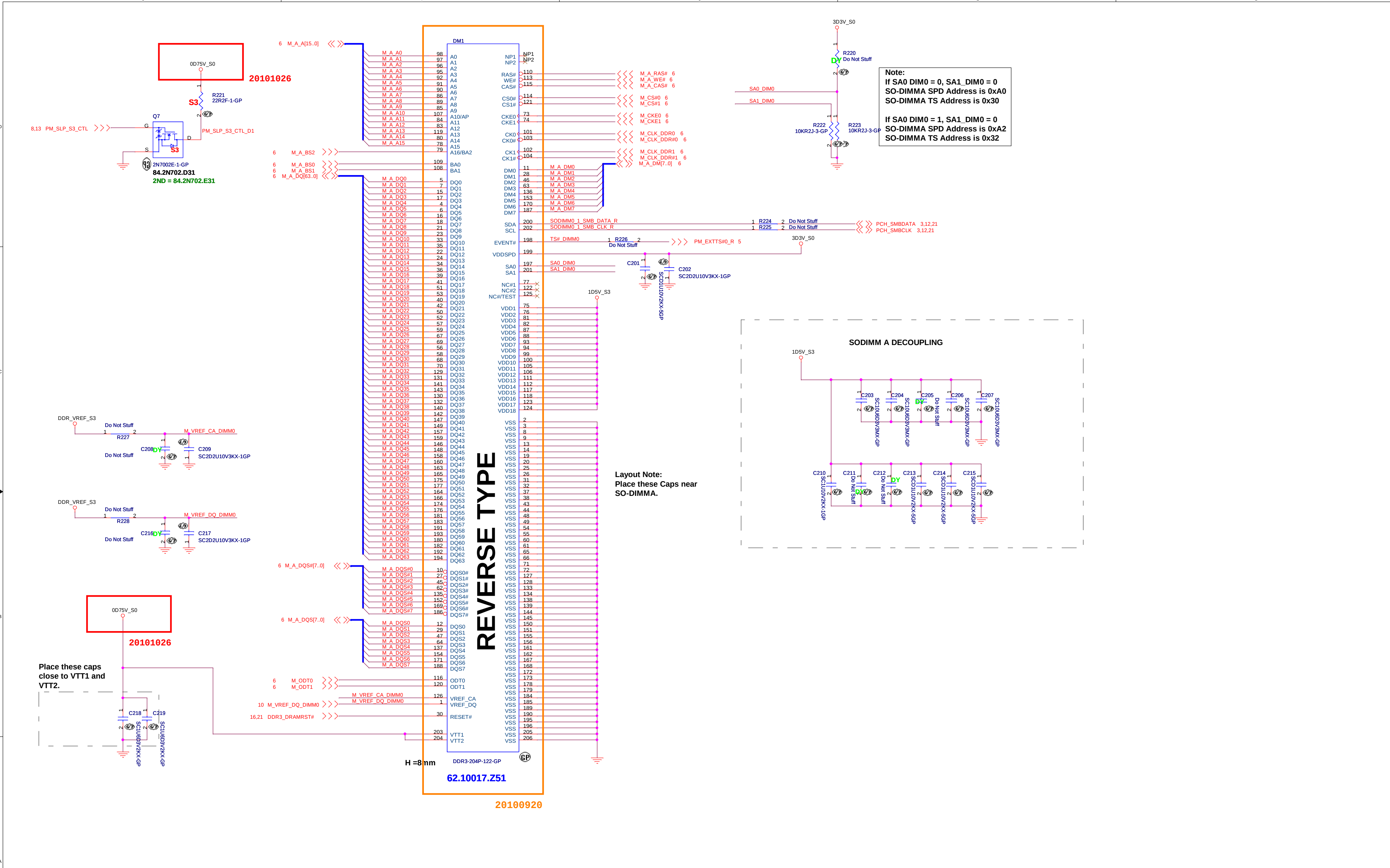
Title: ***PCH (9/9)***

Size	Document Number	Rev
A3	**JE43-CP**	-1

Date: Wednesday, November 24, 2010 Sheet 19 of 69



Hynix 1G 800M N11PGV SKU

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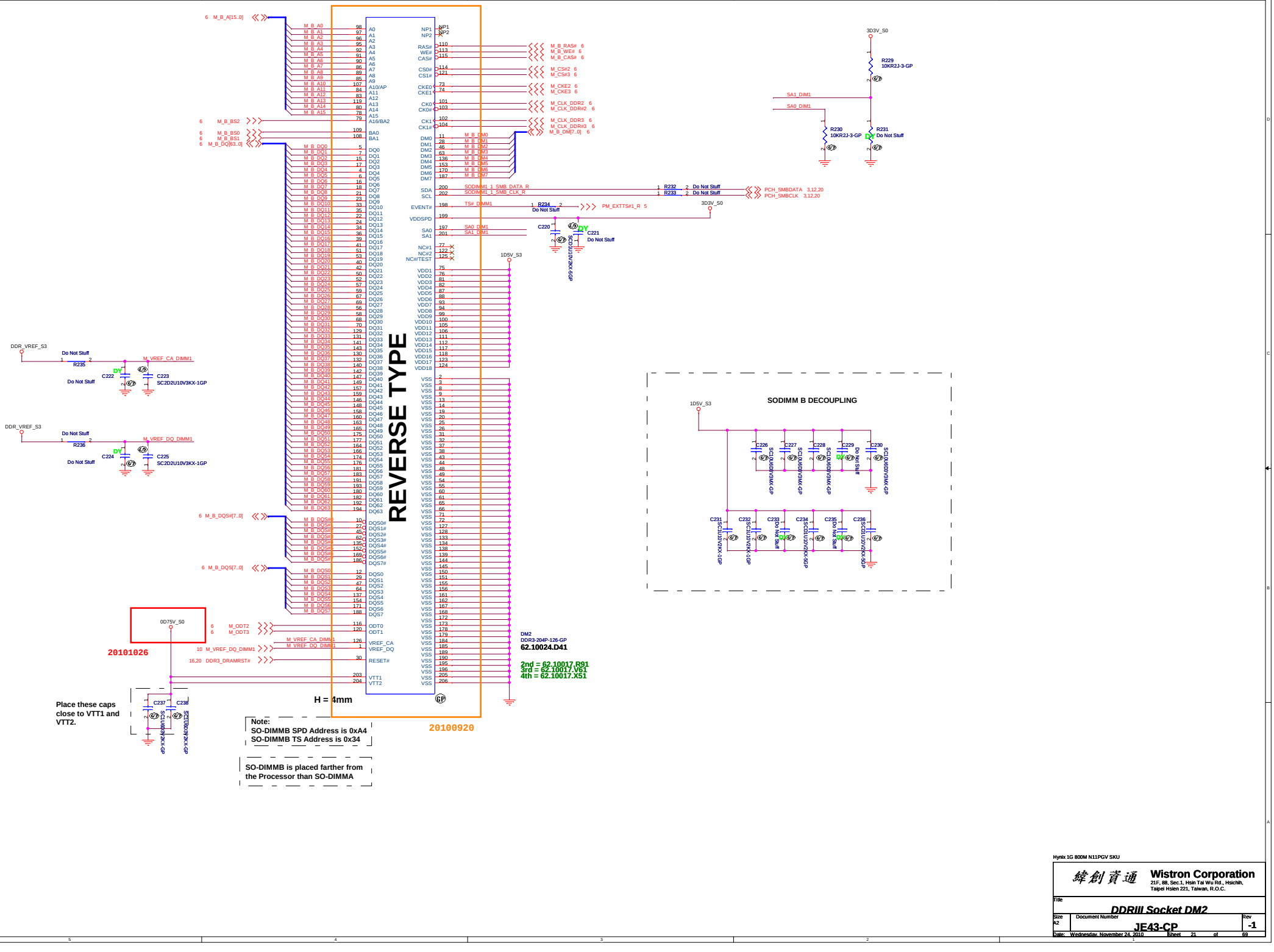
Title	DDRIII Socket DM1	
Size A2	Document Number JE43-CP	Rev -1
Date: Wednesday, November 24, 2010	Sheet 20 of 69	


REVERSE TYPE
H = 4mm
20100920
20101026
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
DM2
DDR3-204P-126-GP
62.10024.D41
2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51
Hynix 1G 800M N11PGV SKU
Wistron Corporation
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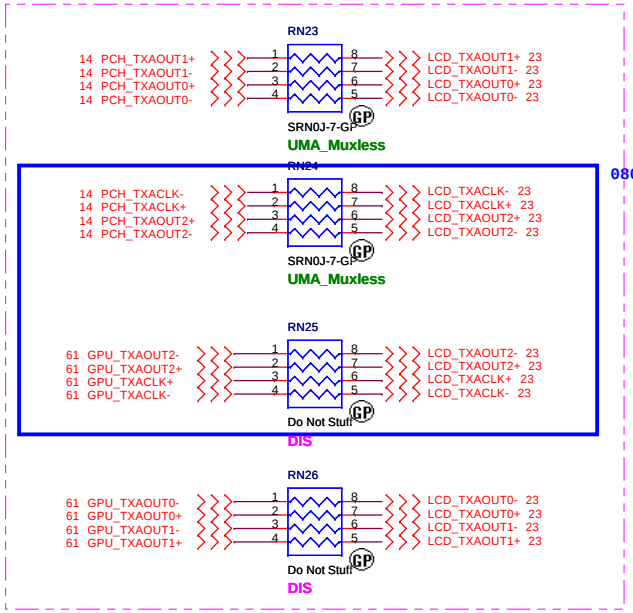
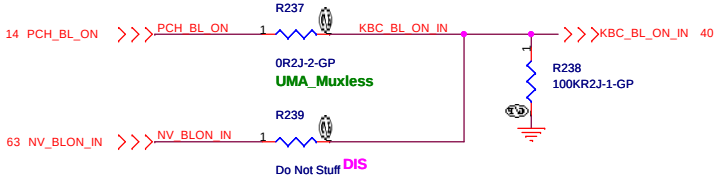
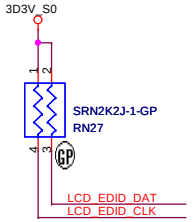
DDRIII Socket DM2
Size A2
Document Number JE43-CP
Rev -1
Date: Wednesday, November 24, 2010
Sheet 21 of 69

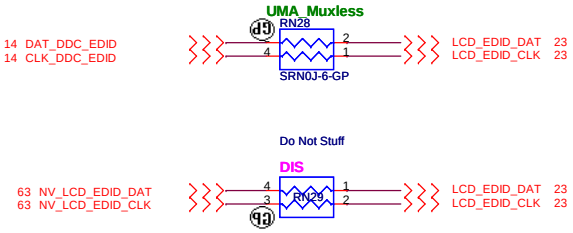
LCD



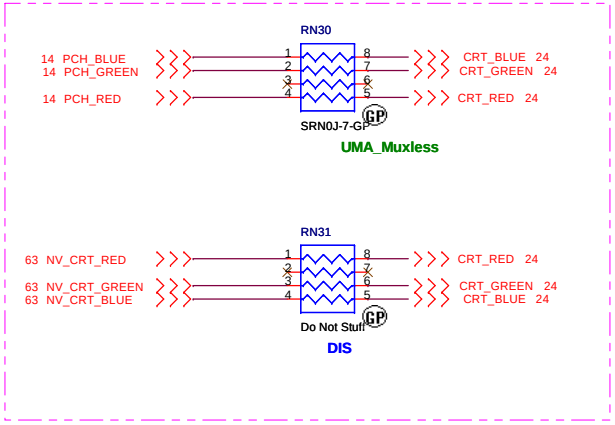
0807 SA CLK SWAP







CRT



Hynix 1G 800M N11PGV SKU

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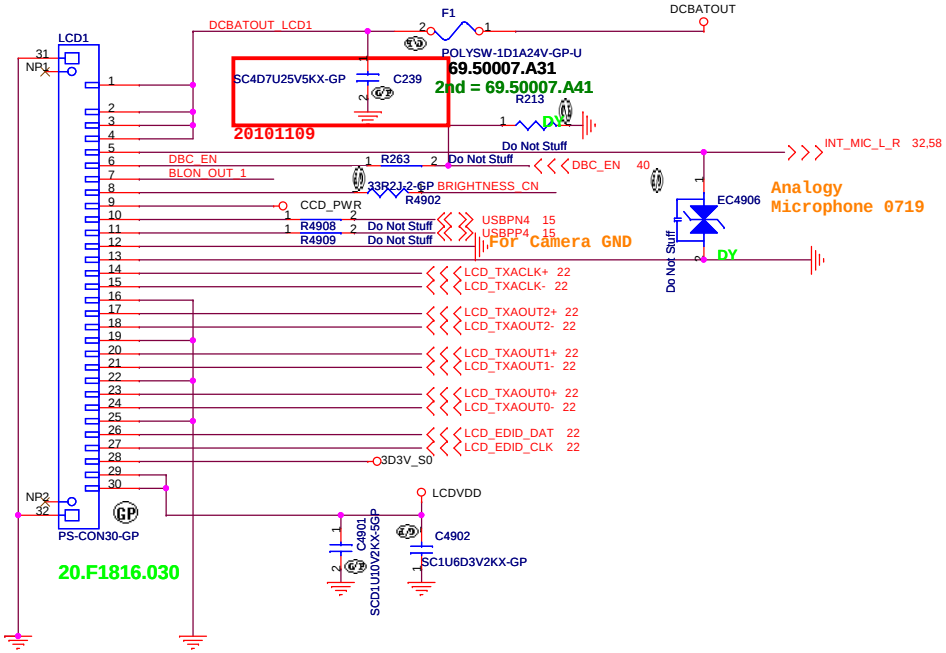
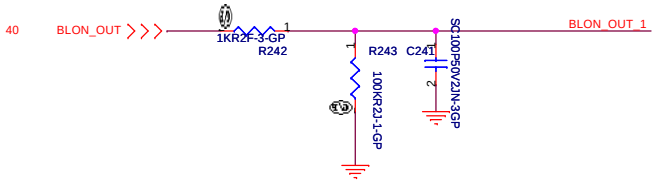
Title: LCD_CRT_SWITCHABLE

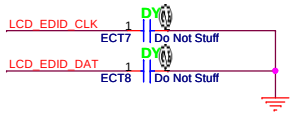
Size	Document Number	Rev
A3	JE43-CP	-1

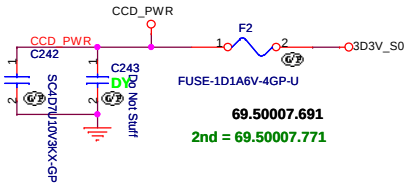
Date: Wednesday, November 24, 2010 Sheet 22 of 69

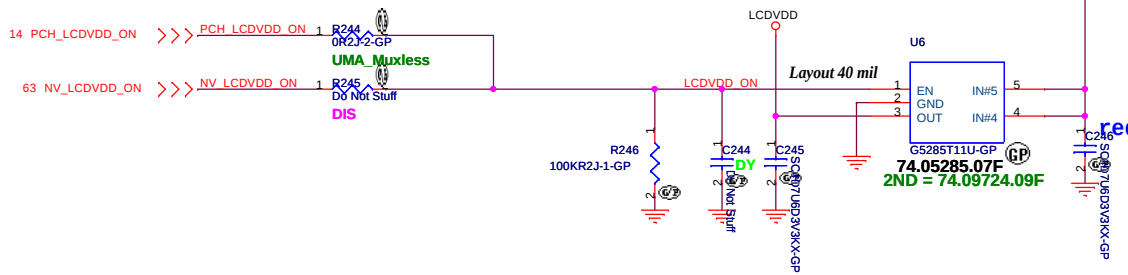
LCD/INVERTER/CCD CONN *LCD/CCD CONN*











PreMp 0312
ECR:R1003642

request by EMI Aaron

Hynix 1G 800M N11PGV SKU

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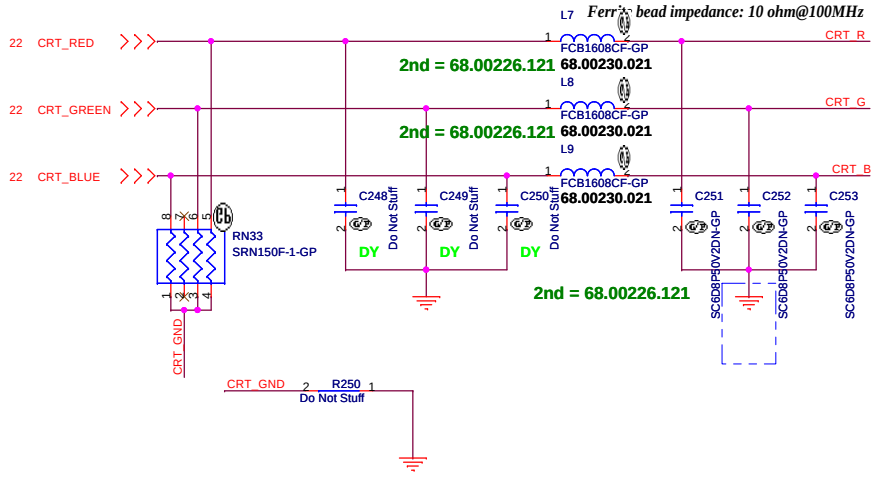
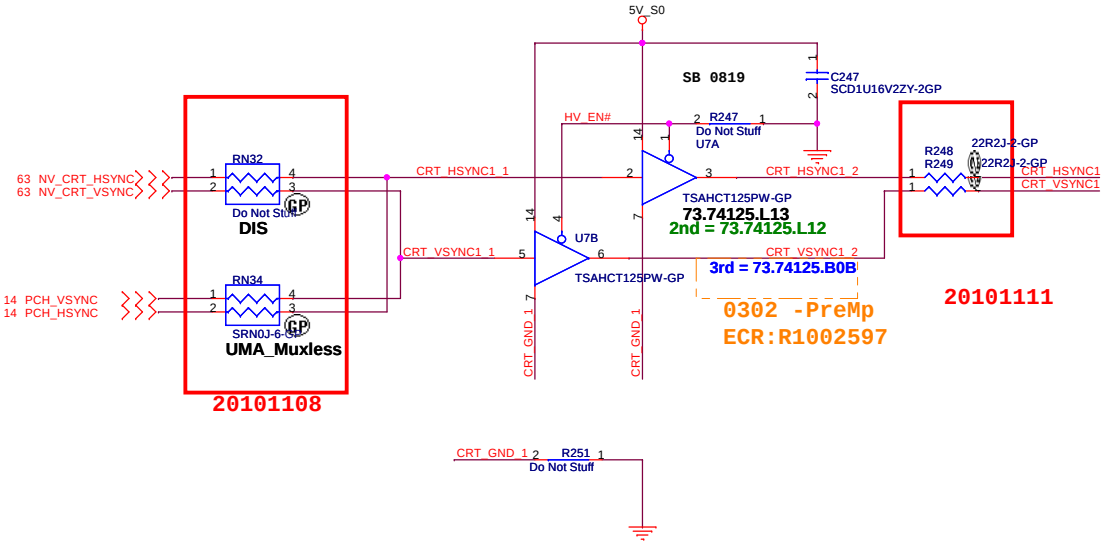
Taipei Hsien 221, Taiwan, R.O.C.

Title	*LCD CONN*	
Size	Document Number **JE43-CP**	Rev -1
Date: Wednesday, November 24, 2010	Sheet 23 of 69	

Layout Note:
Place these resistors close to the CRT-out connector

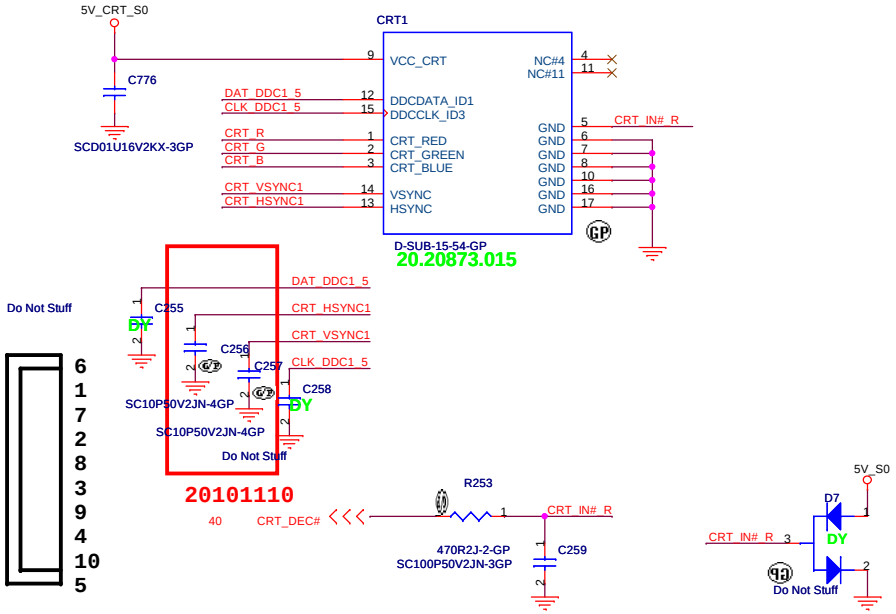


Hsync & Vsync level shift

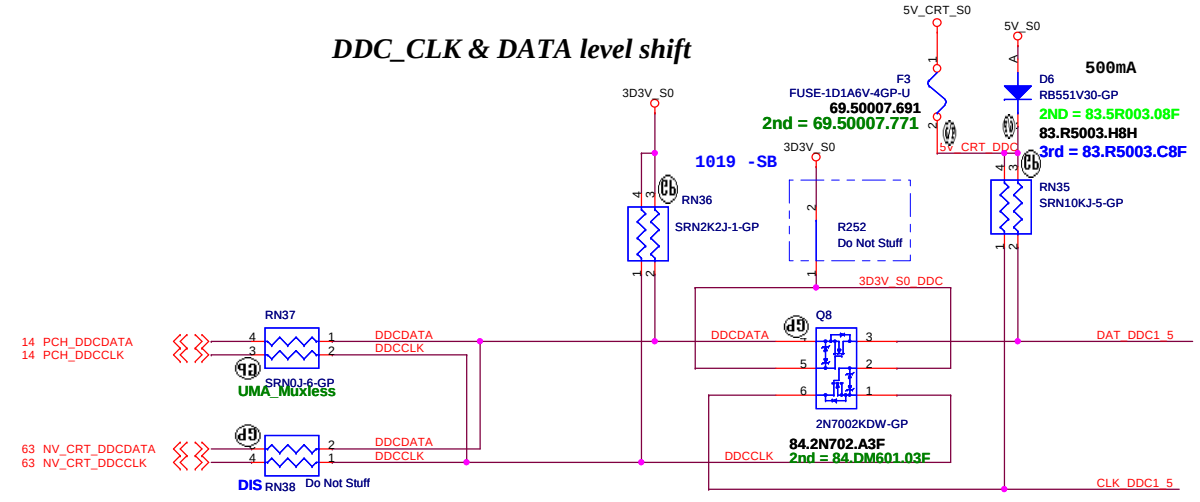


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



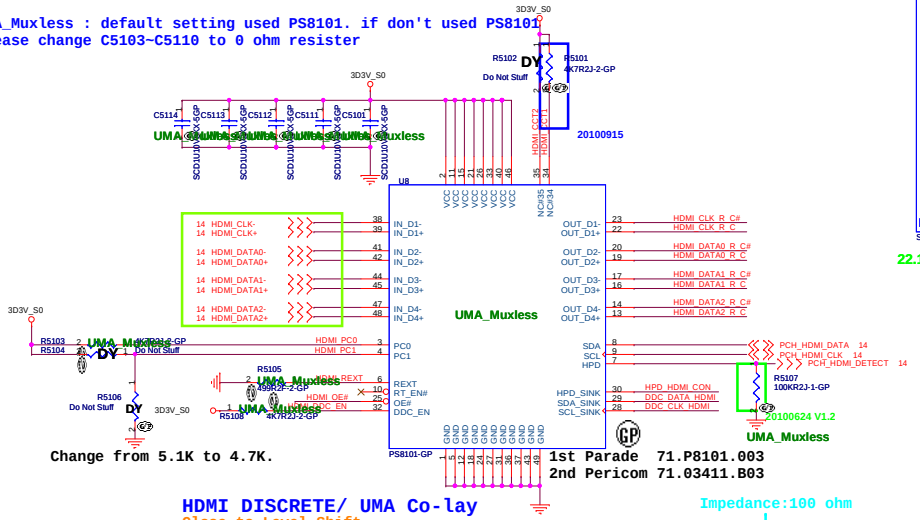
Hynix 1G 800M N11PGV SKU

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT CONN**	
Size	Document Number **JE43-CP**	Rev -1
Date: Wednesday, November 24, 2010	Sheet 24 of 69	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister



HDMI DISCRETE/ UMA Co-lay

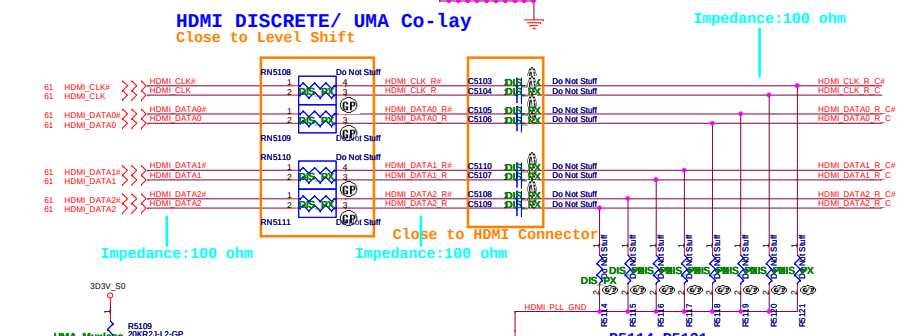
Close to Level Shift

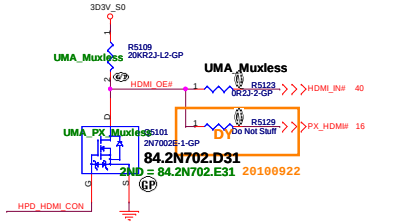
Impedance:100 ohm

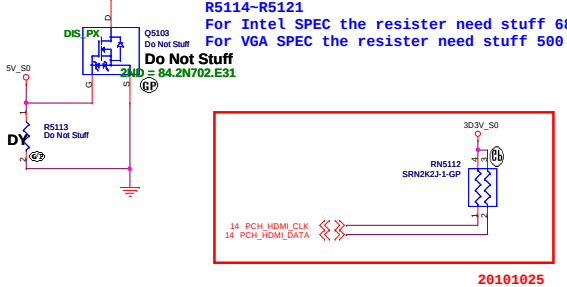
Impedance:100 ohm

Impedance:100 ohm

Close to HDMI Connector



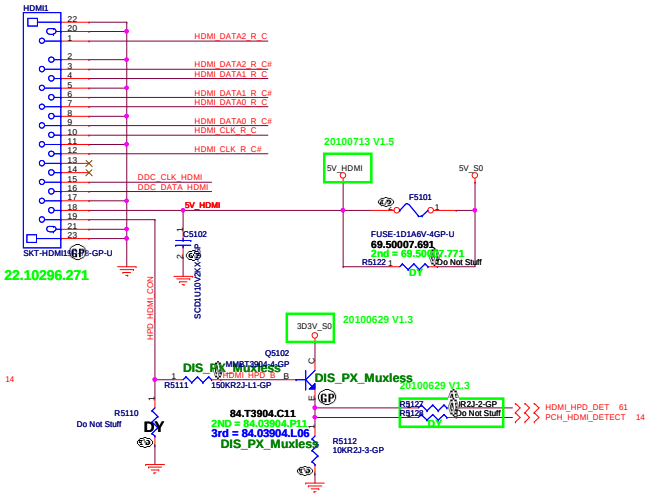




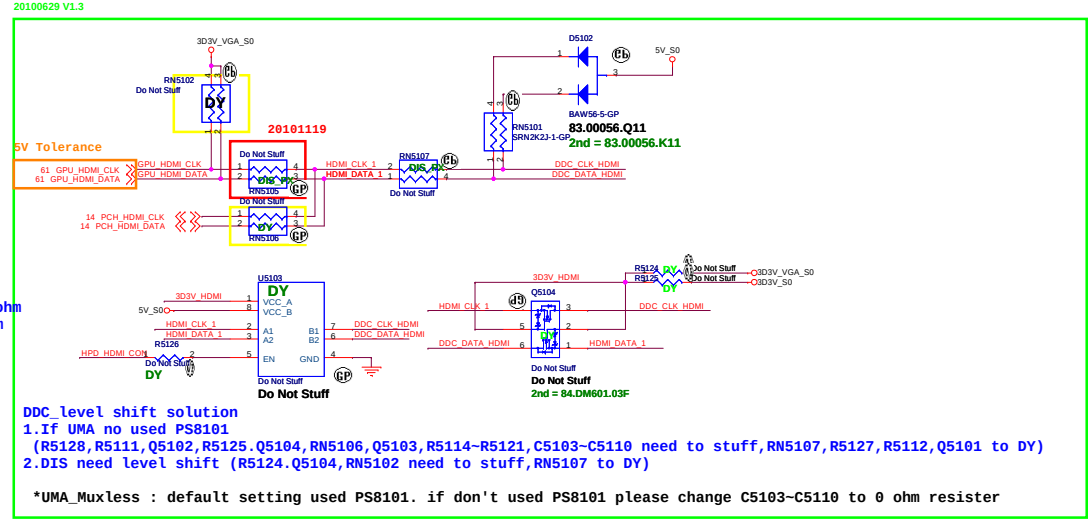
R5114~R5121
For Intel SPEC the resister need stuff 680 ohm
For VGA SPEC the resister need stuff 500 ohm

20101025

HDMI CONN



20100629 V1.3



DDC_level shift solution
1.If UMA no used PS8101
(R5128,R5111,Q5102,R5125.Q5104,RN5106,Q5103,R5114~R5121,C5103~C5110 need to stuff,RN5107,R5127,R5112,Q5101 to DY)
2.DIS need level shift (R5124.Q5104,RN5102 need to stuff,RN5107 to DY)

*UMA_Muxless : default setting used PS8101. if don't used PS8101 please change C5103~C5110 to 0 ohm resister

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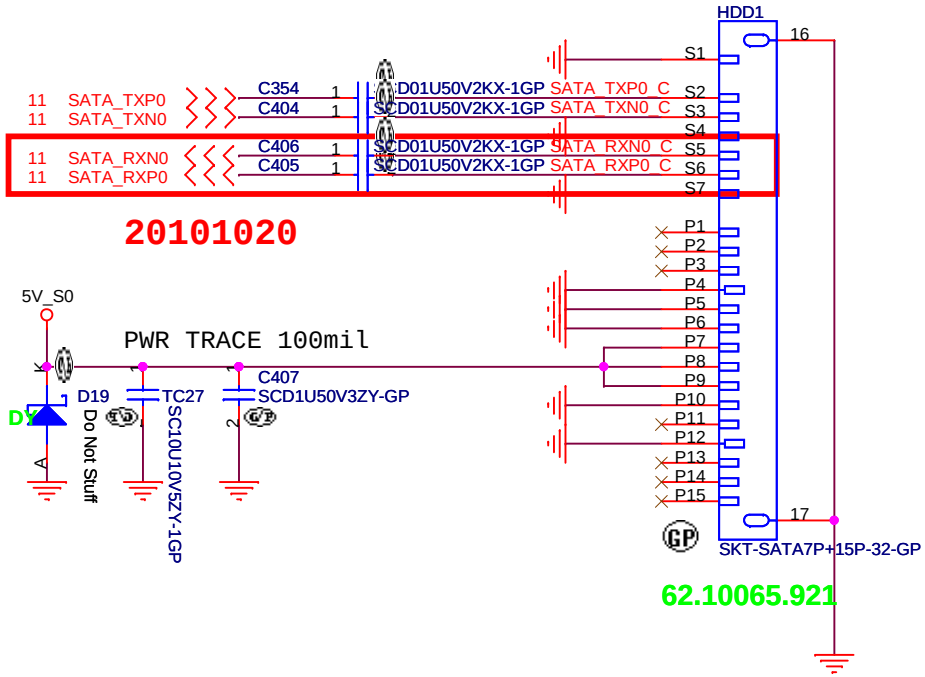
Title: HDMI CONN		
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 25 of 69	

SATA Connector



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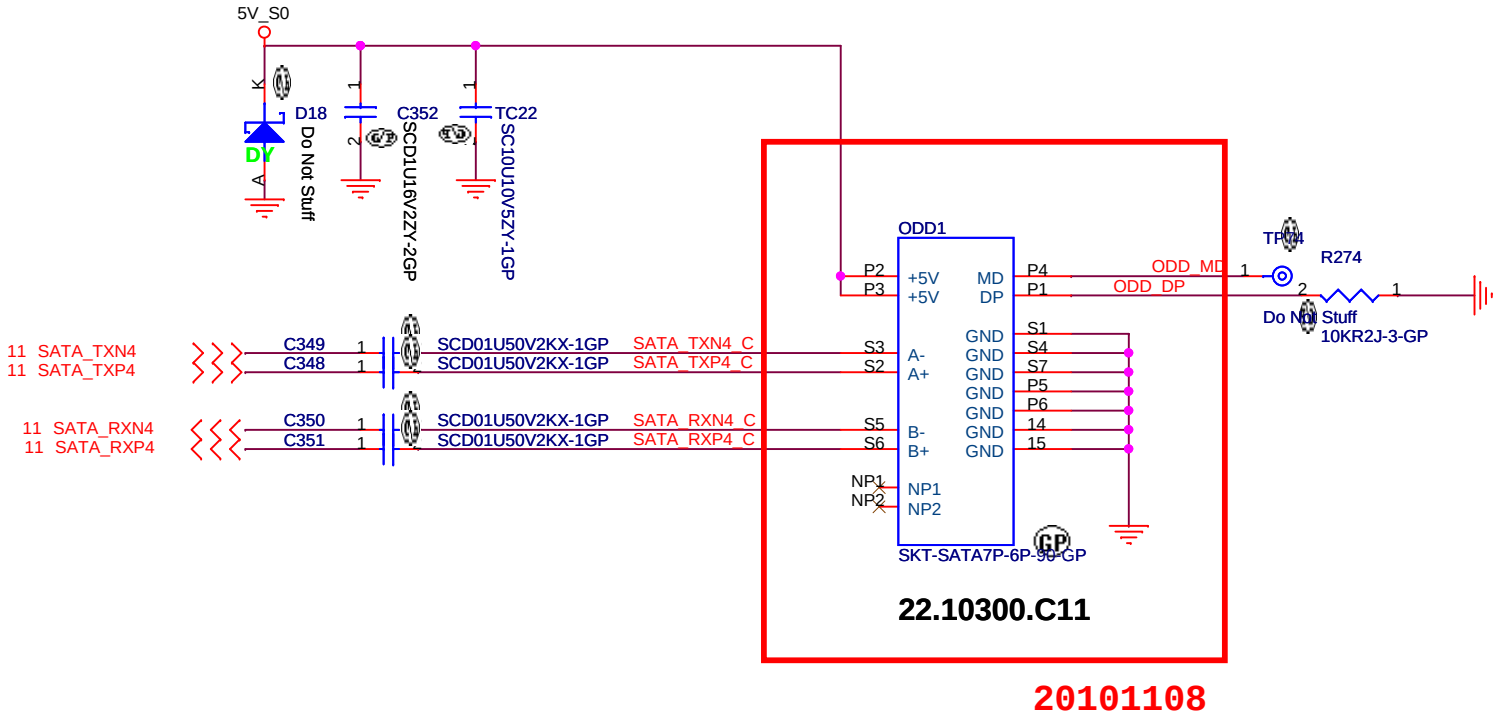
Title	HDD CONN	
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 26 of 69	

ODD Connector



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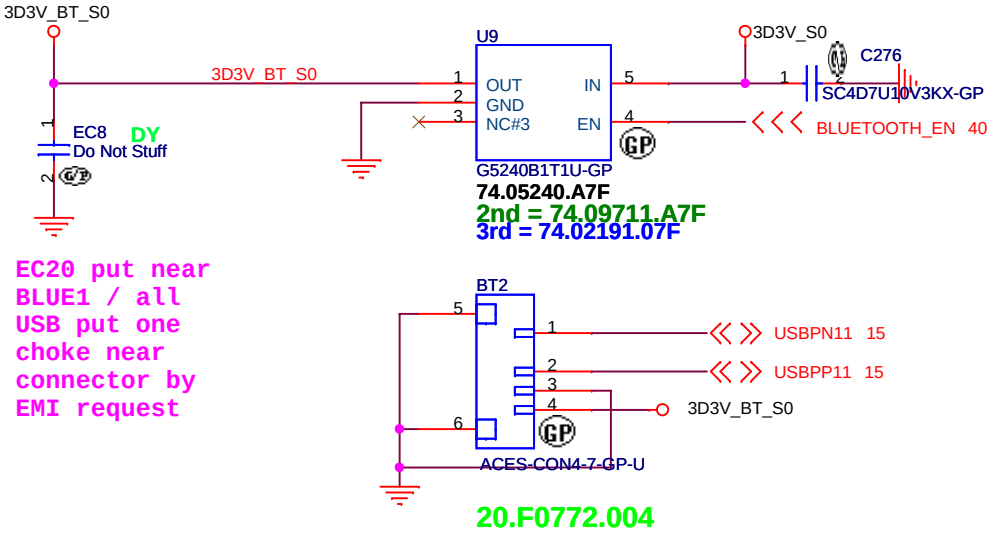
Title: ODD		
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 27 of 69	

BLUETOOTH MODULE



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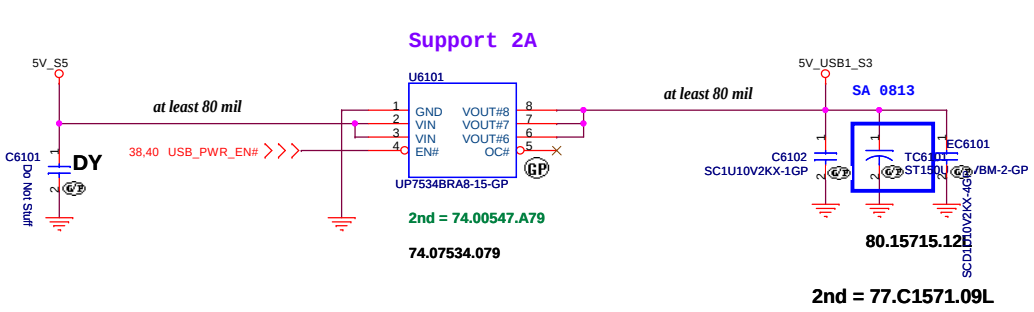
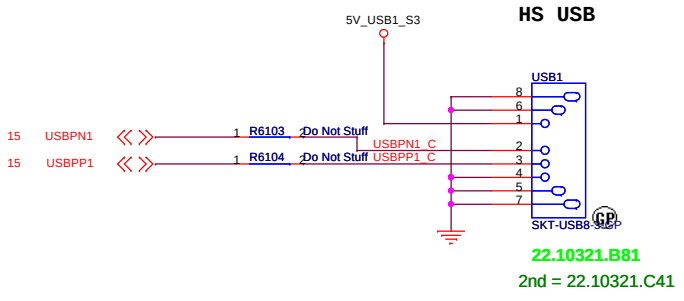
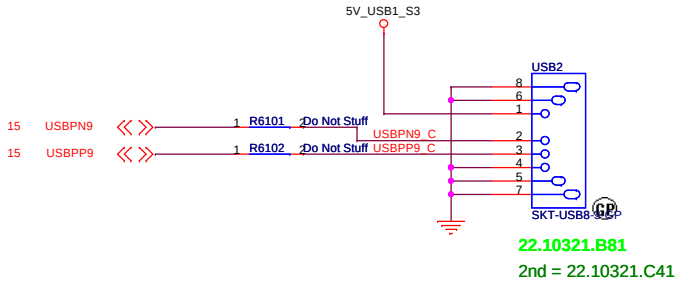
Title: BLUETOOTH CONN		
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 28 of 69	







Hynix 1G 800M N11PGV SKU

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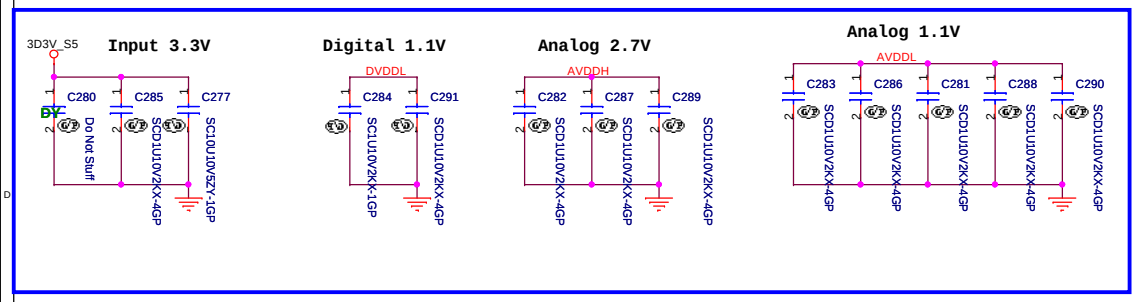
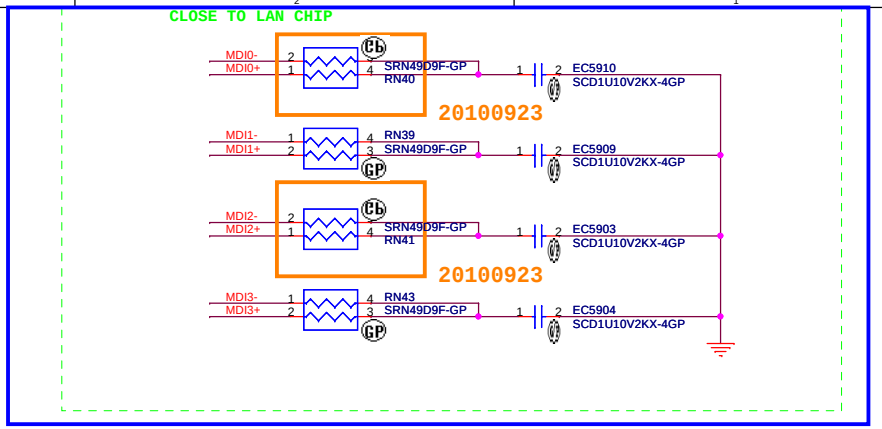
Title: *USB 2.0 CONN*		
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 29 of 69	



20100915



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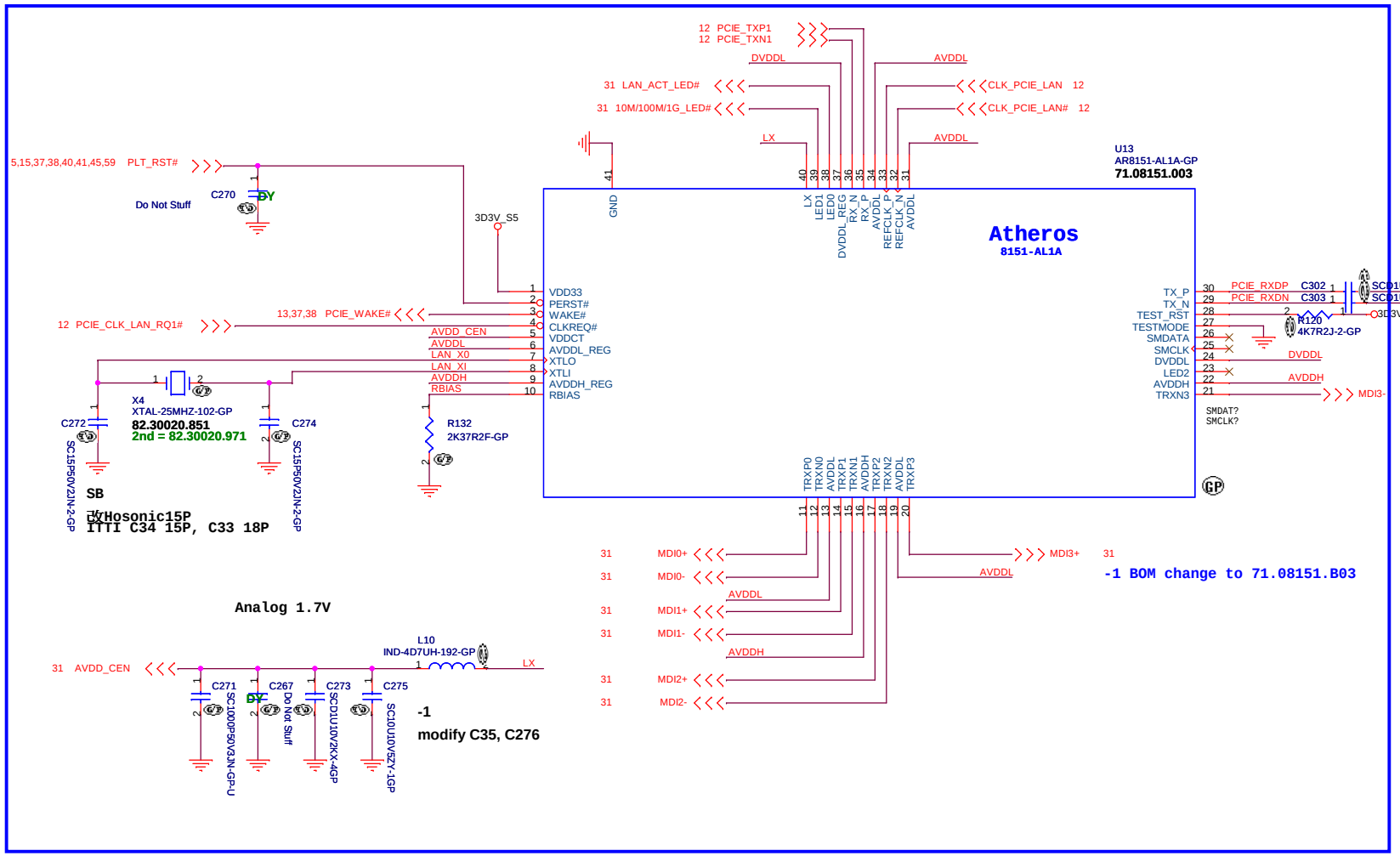

20100915

Hynix 1G 800M N11PGV SKU

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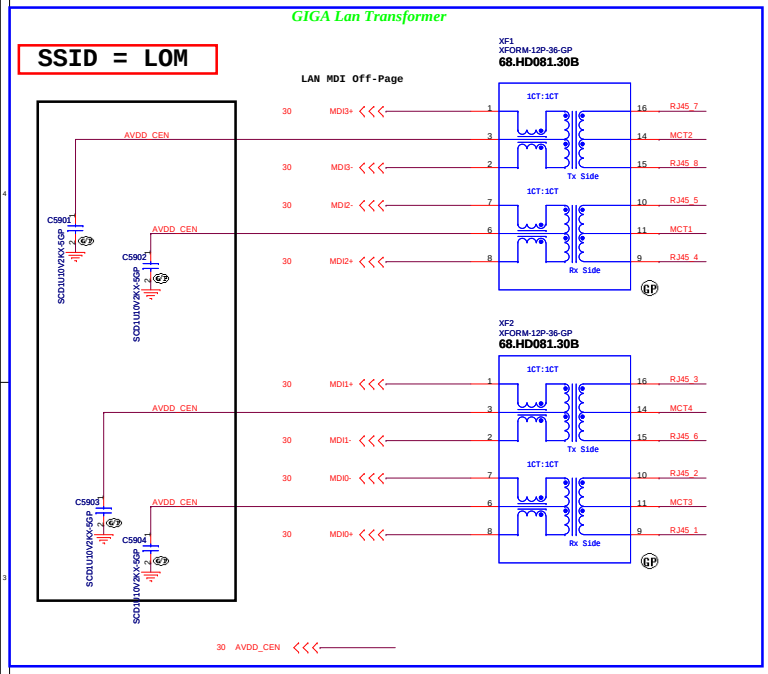
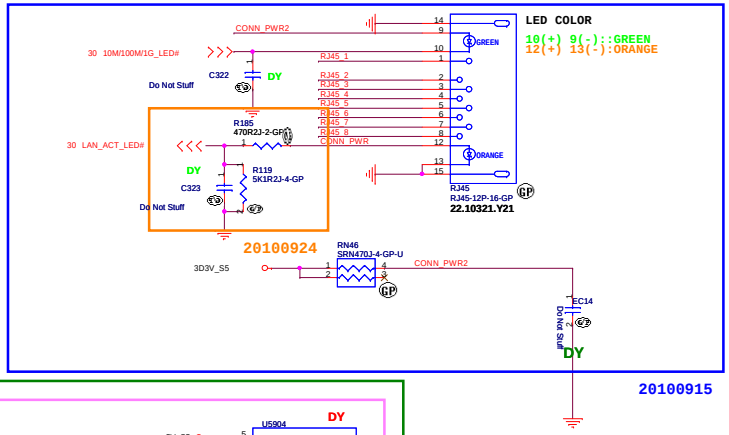
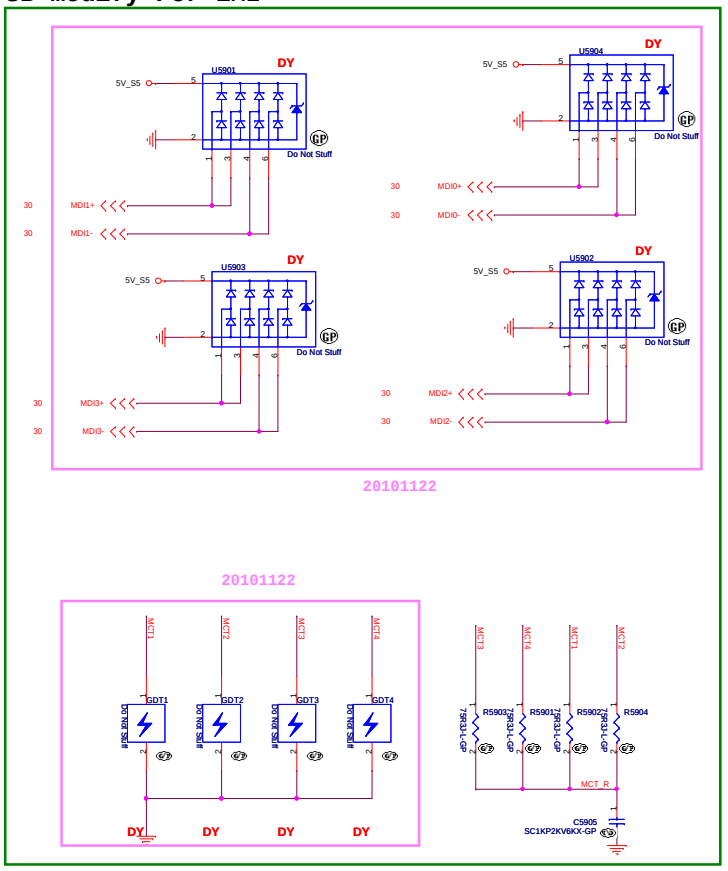
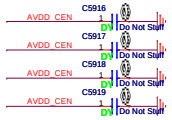
Title: *AR8151 chip*		
Size: A3	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 30 of 69	





SB modify For EMI





Hynix 1G 800M N11PGV SKU

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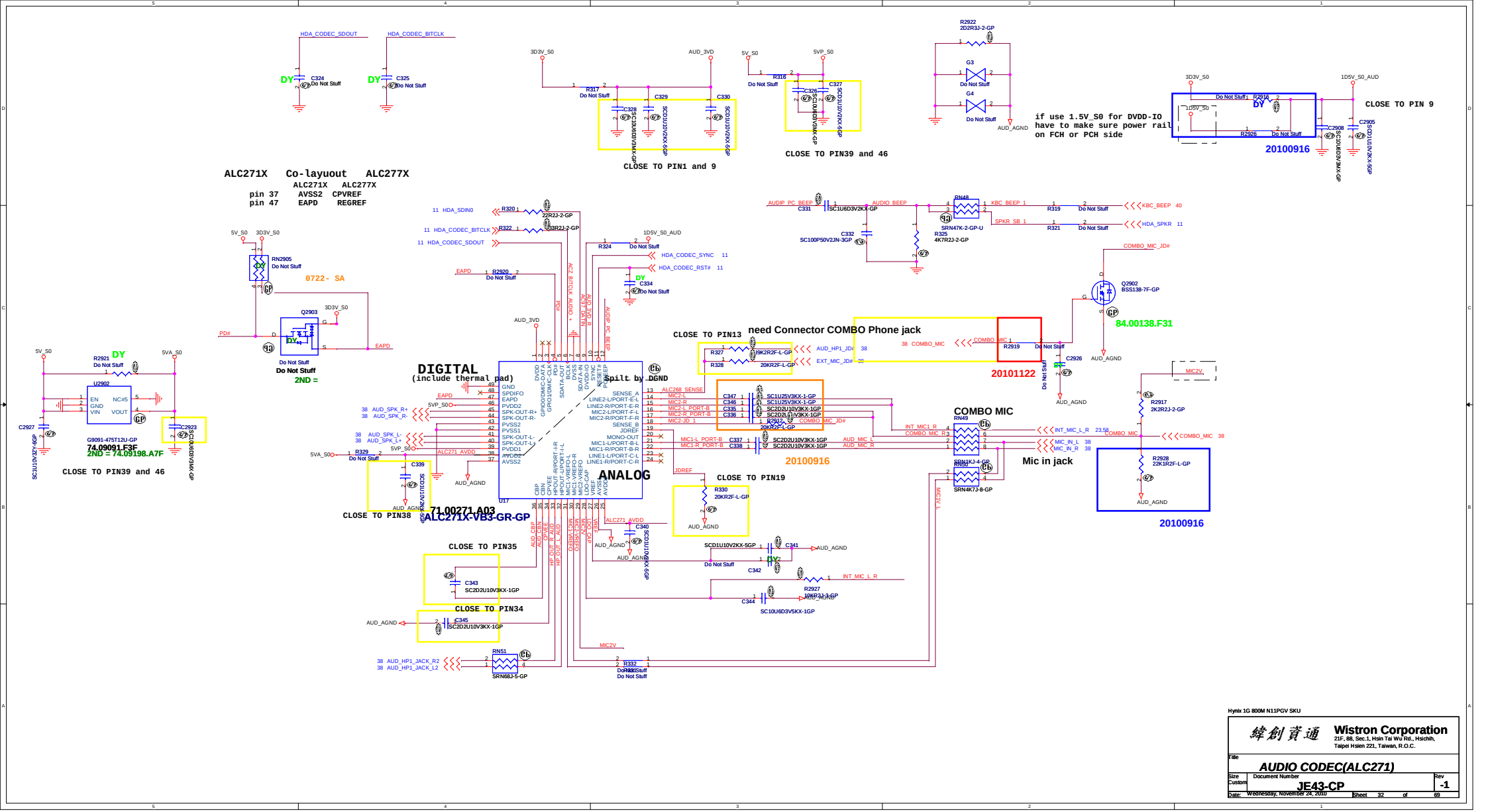
Title: **LAN CONN**

Size	Document Number	Rev
A2	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 31 of 69


ALC271X Co-layuout ALC277X
ALC271X ALC277X
pin 37 AVSS2 CPVREF
pin 47 EAPD REGREF
0722- SA
2ND =
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
74.09091.F3F
2ND = 74.09198.A7F
G9091-475T12U-GP
CLOSE TO PIN39 and 46
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
CLOSE TO PIN9
CLOSE TO PIN13
need Connector COMBO Phone jack
CLOSE TO PIN19
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
if use 1.5V_S0 for DVDD-IO have to make sure power rail on FCH or PCH side
20100916
20101122
84.00138.F31
COMBO MIC
Mic in jack
Hynix 1G 800M N11PGV SKU
Wistron Corporation
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AUDIO CODEC(ALC271)
JE43-CP
Wednesday, November 24, 2010

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Title	****	
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 33 of 69	

Hynix 1G 800M N11PGV SKU

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Title	****	
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 34 of 69	

Hynix 1G 800M N11PGV SKU

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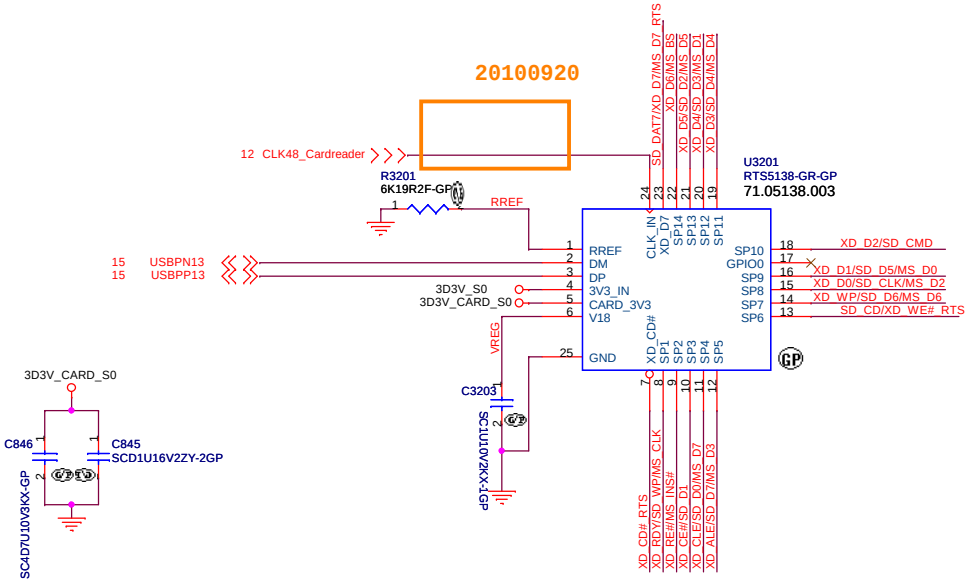
Title

RTS5138 (CARD READER)

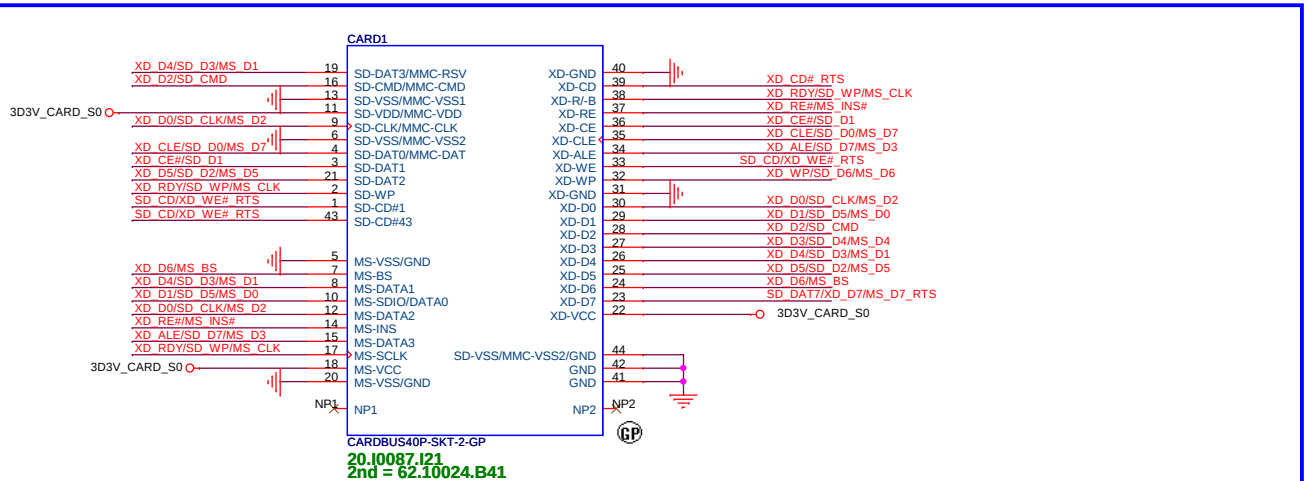
Size	Document Number	Rev
A3	**JE43-CP**	**-1**

Date: Wednesday, November 24, 2010 Sheet 35 of 69



20100915

4 IN1 CARD-READER (SD/MS/MS PRO/XD)



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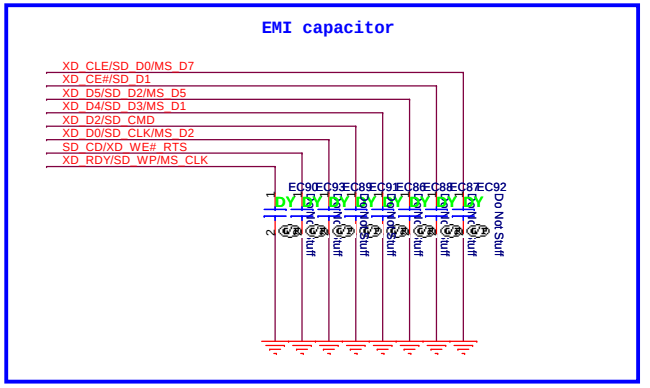

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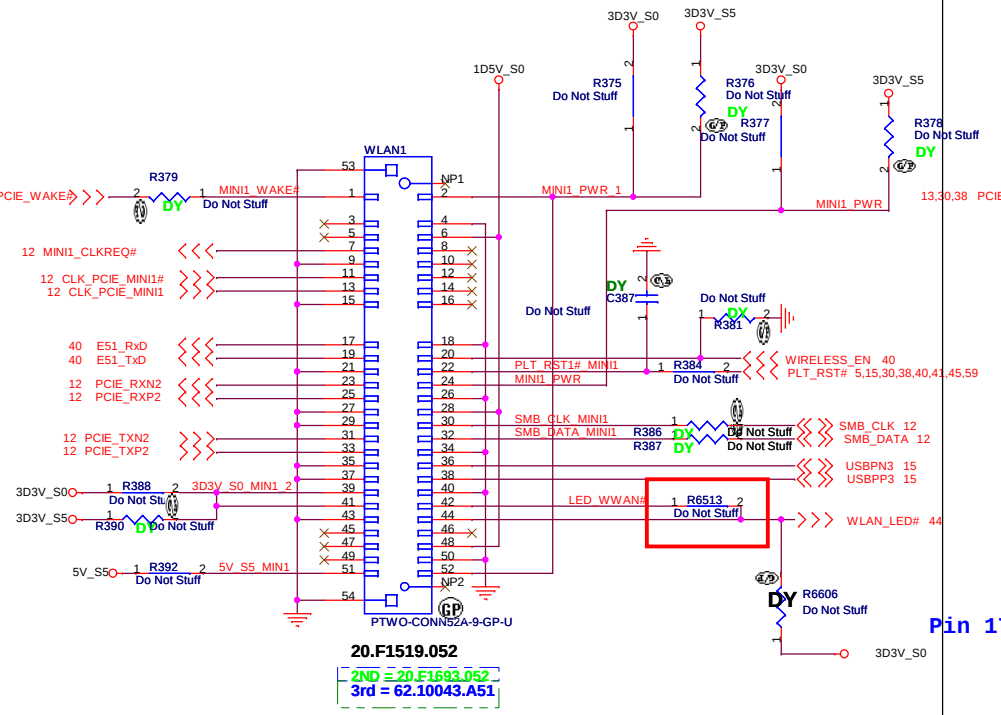
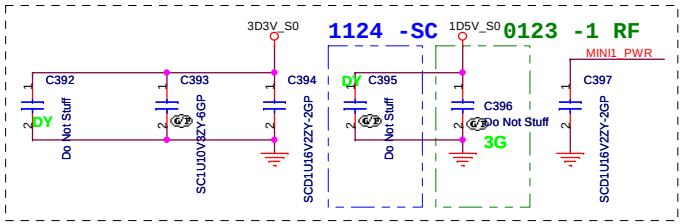
Title	Cardreader CONN	
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 36 of 69	

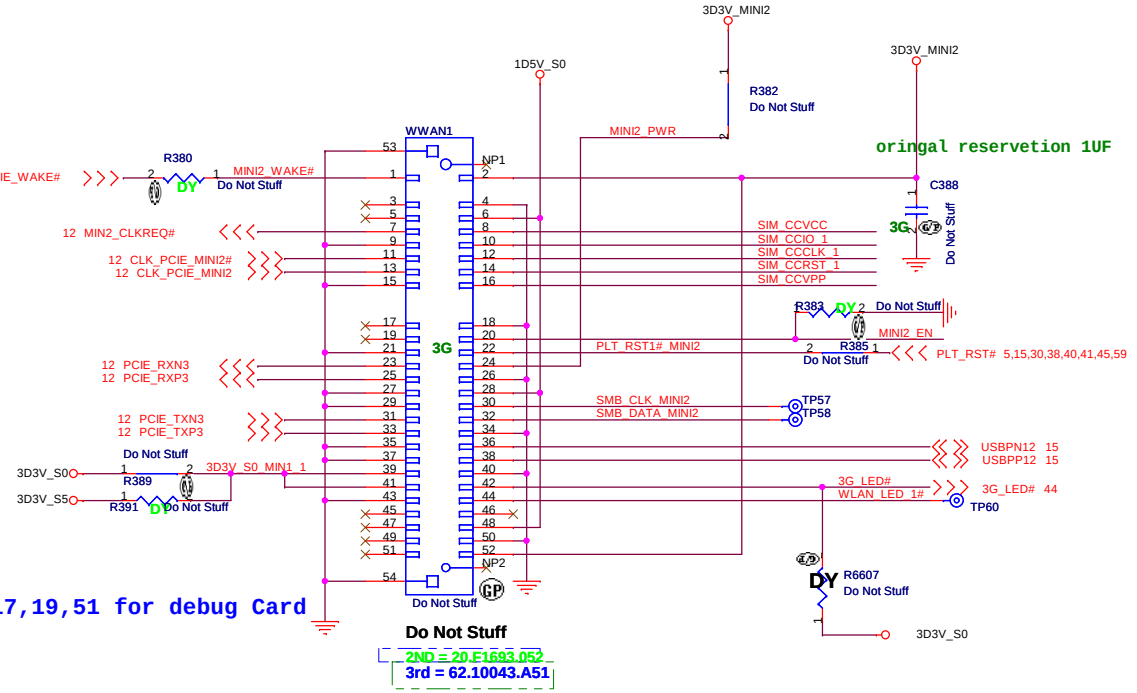
Mini Card Connector(WLAN)
Support debug-card

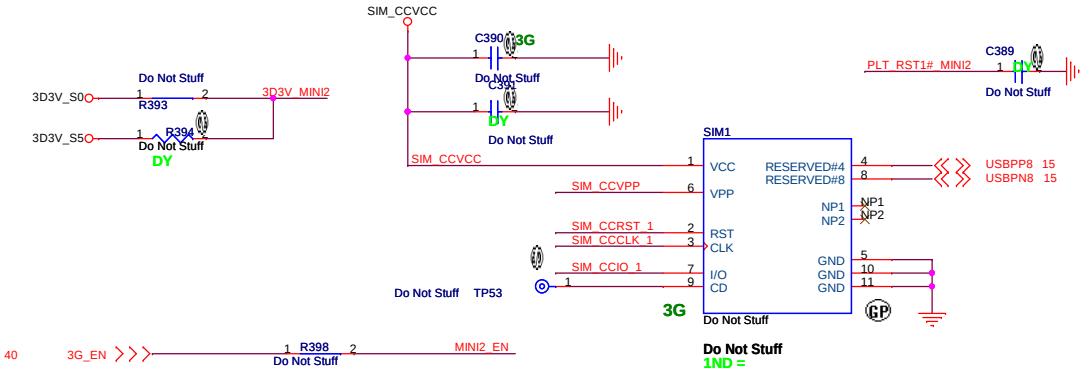


Place near MINI1

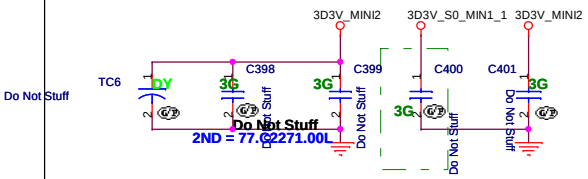


Mini Card Connector(Robson2 and 3G)





oringal reservetion 10UF



Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
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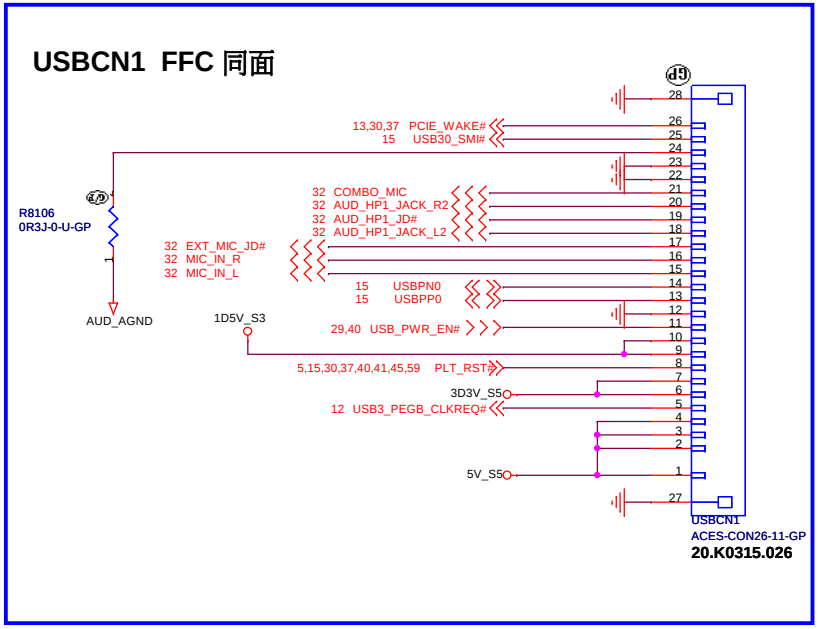
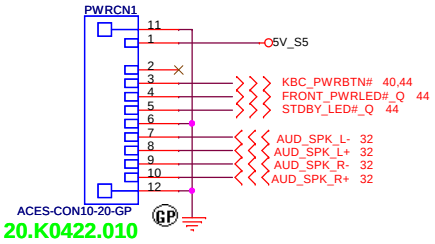
Title	MINI CARD	
Size A3	Document Number JE43-CP	Rev -1
Date: Wednesday, November 24, 2010	Sheet 37 of 69	

USBCN1 FFC 同面

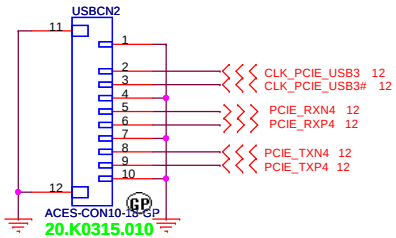


20100915

PWRCN1 FFC 異面



USBCN2 FFC 同面



Hynix 1G 800M N11PGV SKU

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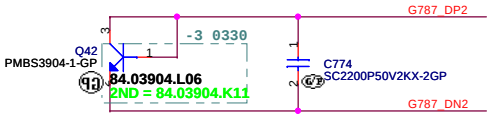
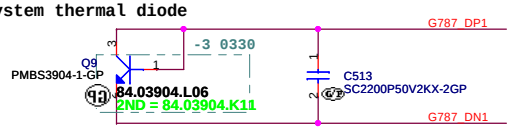
Title: I/O Board		
Size: A3	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 38 of 69	

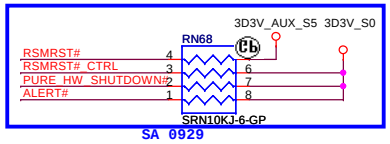
for T8 thermal diode

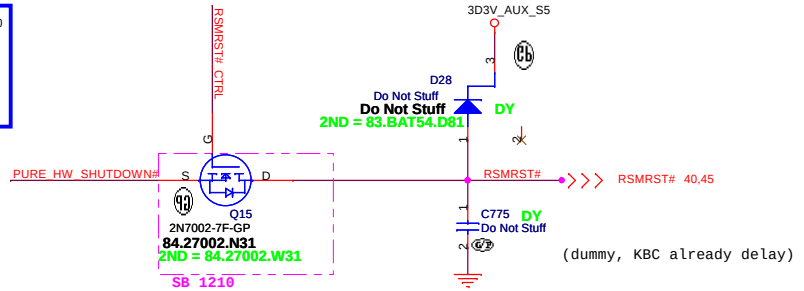


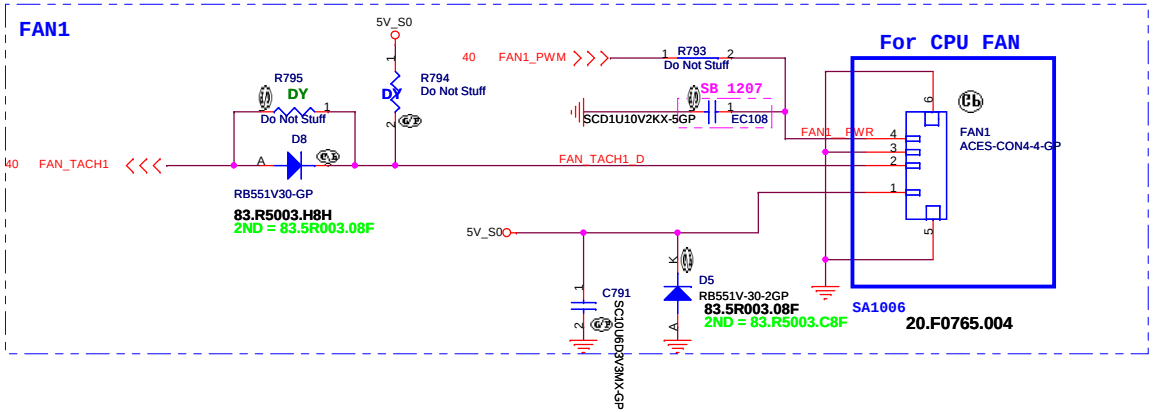
C82 & C561 CLOSE TO G787

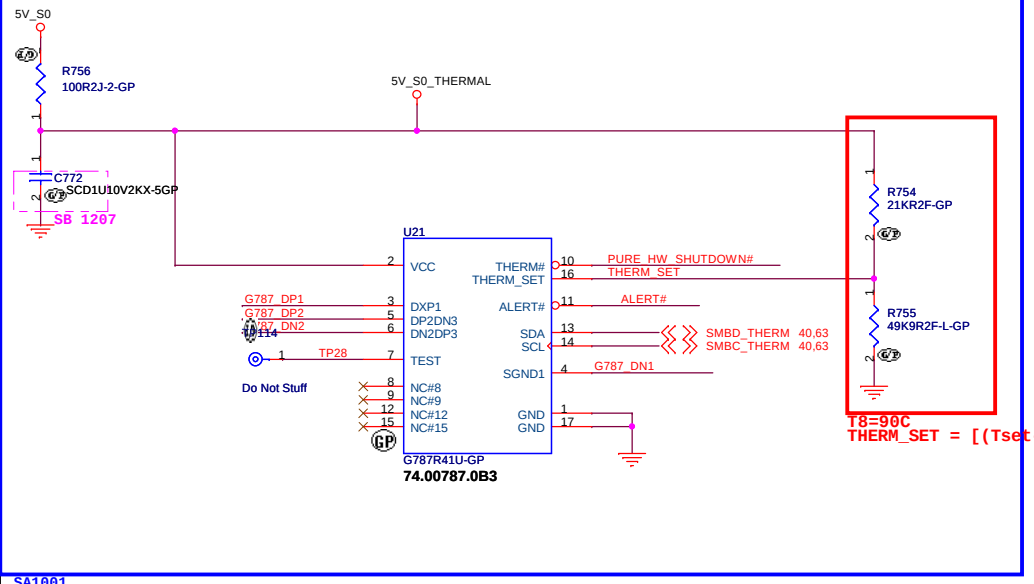
for system thermal diode











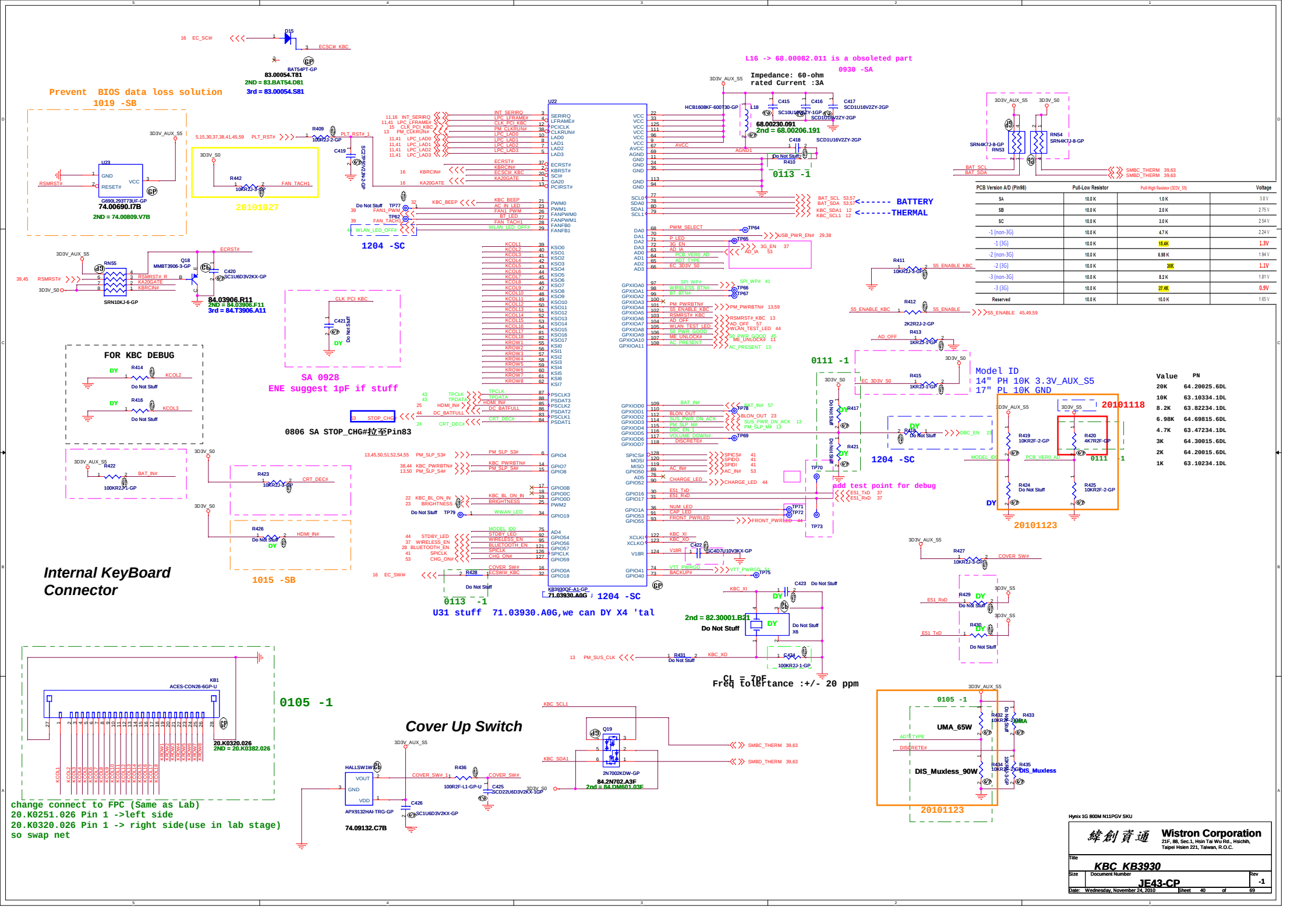
Hynix 1G 800M N11PGV SKU

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Connector***

Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 39 of 69



PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_S5)	Voltage
SA	10.0 K	1.0 K	3.0 V
SB	10.0 K	2.0 K	2.75 V
SC	10.0 K	3.0 K	2.54 V
-1 (non-3G)	10.0 K	4.7 K	2.24 V
-1 (3G)	10.0 K	15.4K	1.3V
-2 (non-3G)	10.0 K	6.98 K	1.94 V
-2 (3G)	10.0 K	20K	1.1V
-3 (non-3G)	10.0 K	8.2 K	1.81 V
-3 (3G)	10.0 K	27.4K	0.9V
Reserved	10.0 K	10.0 K	1.65 V

Value	PN
20K	64.20025.6DL
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

Hynix 1G 800M N11PGV SKU

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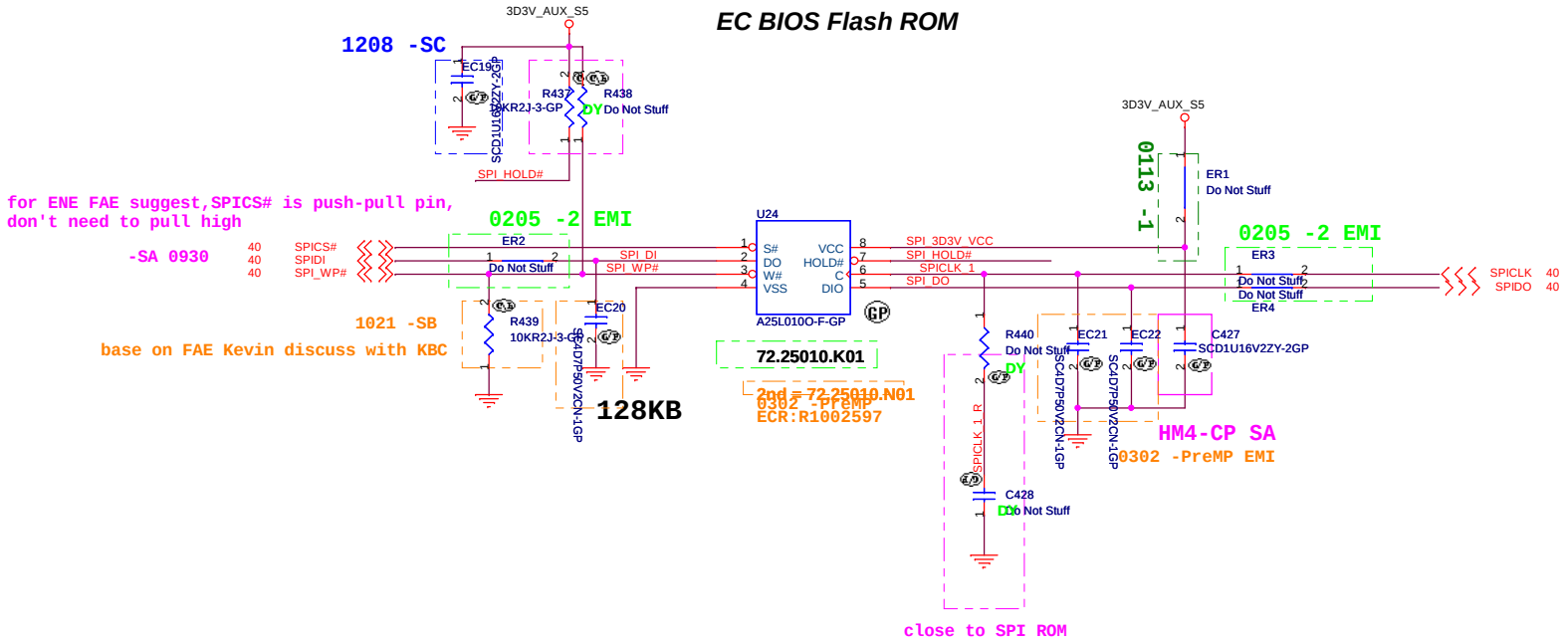
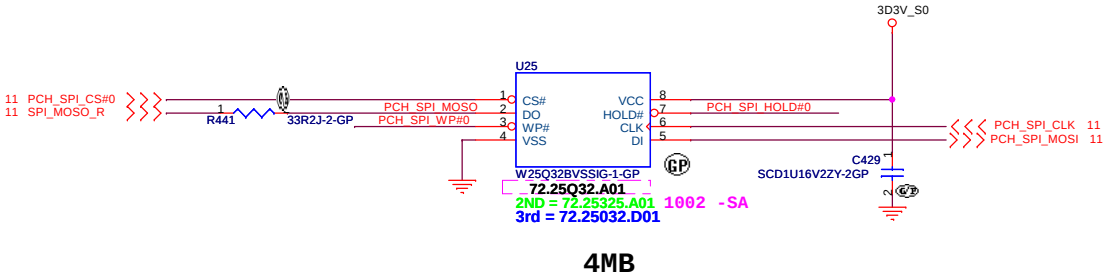
Title: KBC_KB3930
Size: Document Number: JE43-CP Rev: -1
Date: Wednesday, November 24, 2010 Sheet 40 of 69

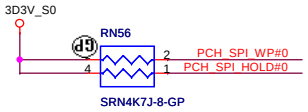
EC BIOS Flash ROM



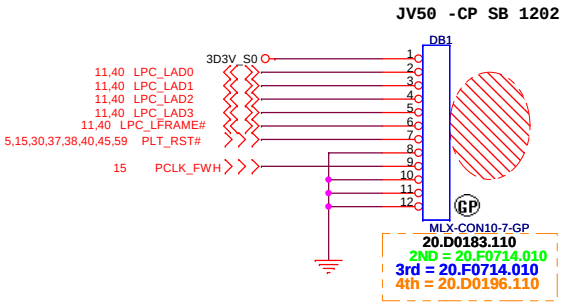
System BIOS Flash ROM



4MB



GOLDEN FINGER FOR DEBUG BOARD



Lab only stuff 4th source(20.D0196.110)
Eng and PD DY DB1

Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: BIOS
Size | Document Number: JE43-CP | Rev: -1
Date: Wednesday, November 24, 2010 | Sheet 41 of 69

Hynix 1G 800M N11PGV SKU

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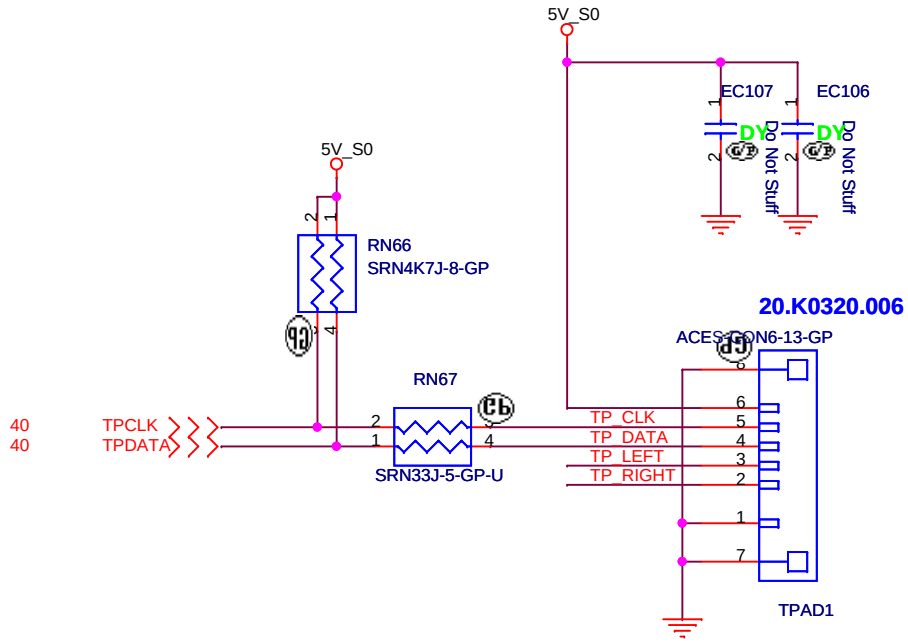
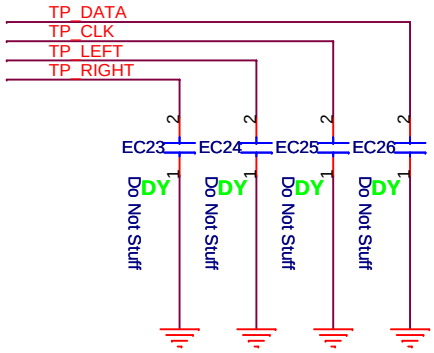
Taipei Hsien 221, Taiwan, R.O.C.

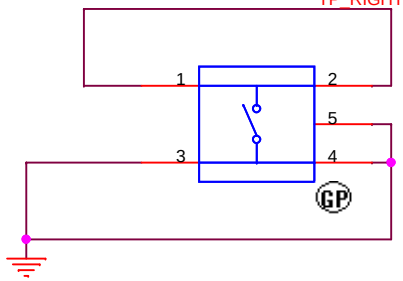
Title	****	
Size A3	Document Number **JE43-CP**	Rev **-1**
Date: Wednesday, November 24, 2010	Sheet 42 of 69	





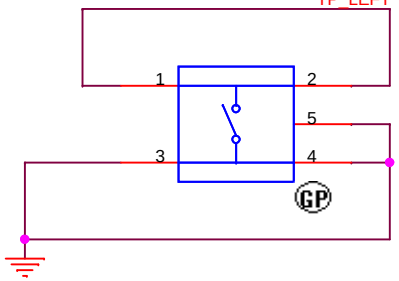
RIGHT

SW_R1
SW-TACT-5P-9-GP
62.40089.141
Change:62.40089.221
TP_RIGHT



LEFT

SW_L1
SW-TACT-5P-9-GP
62.40089.141
Change:62.40089.221
TP_LEFT



Hynix 1G 800M N11PGV SKU

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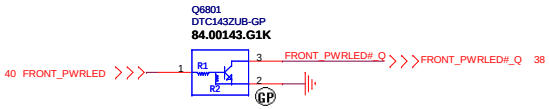
Taipei Hsien 221, Taiwan, R.O.C.

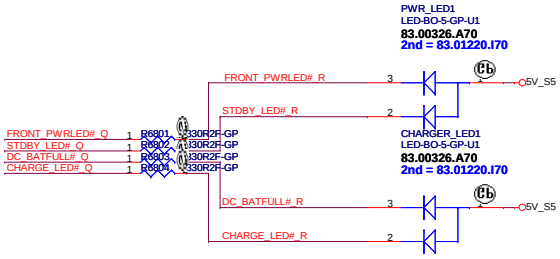
Title: *Touch PAD_FP CONN*

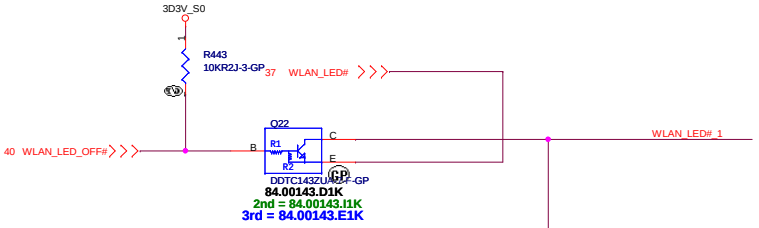
Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 43 of 69

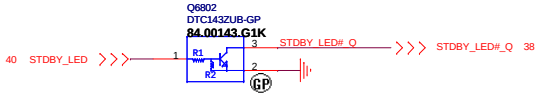
Power button LED

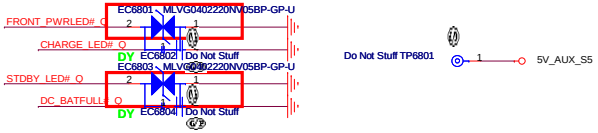




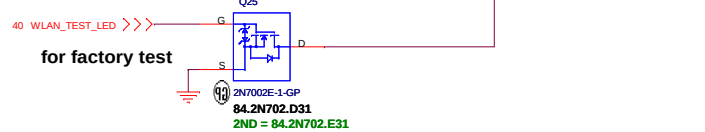


Power STDBY_LED



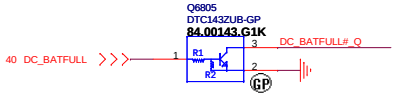


EC6801, EC6803, EC34 請幫忙上件 22p 5.5V 的
Varistor料號是 69.80024.011

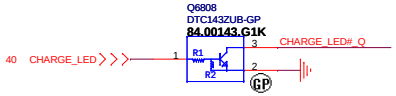


For 2010 Acer Project, WLAN and 3G LED control by KBC

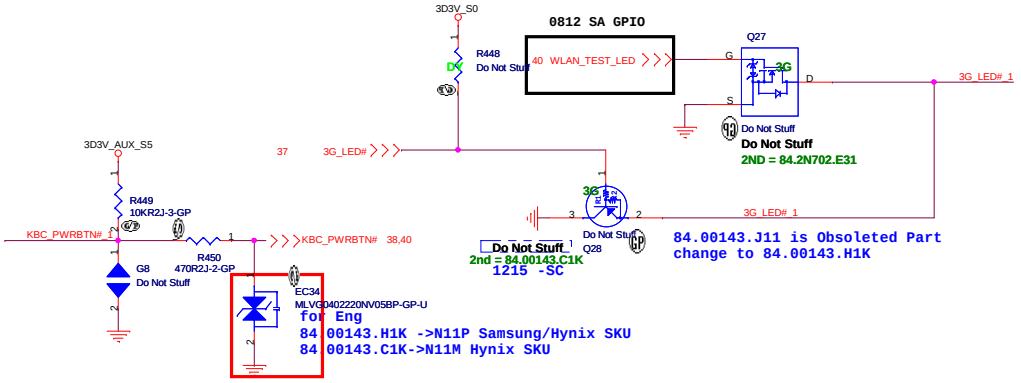
Battery LED2(DC_BATFULL)



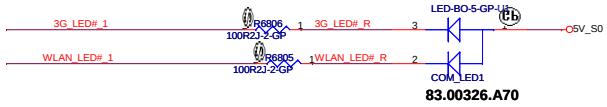
Battery LED1(CHARGE)



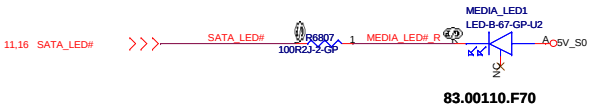
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net



84.00143.J11 is Obsoleted Part
change to 84.00143.H1K



SATA HDD LED



Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

Hynix 1G 800M N11PGV SKU

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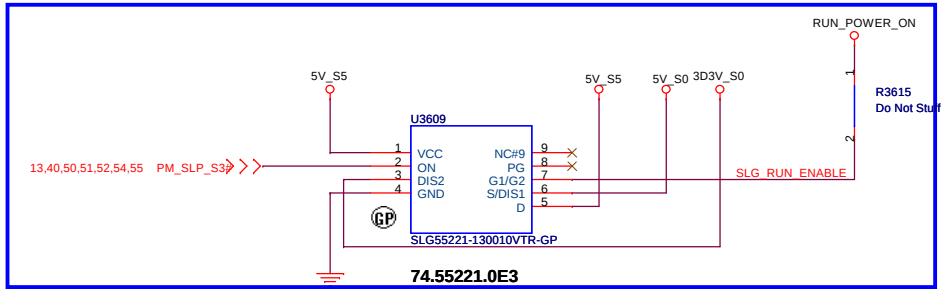
Title: LED&POWERBD CONN
Size: Document Number: JE43-CP Rev: -1
Date: Wednesday, November 24, 2010 Sheet 44 of 69

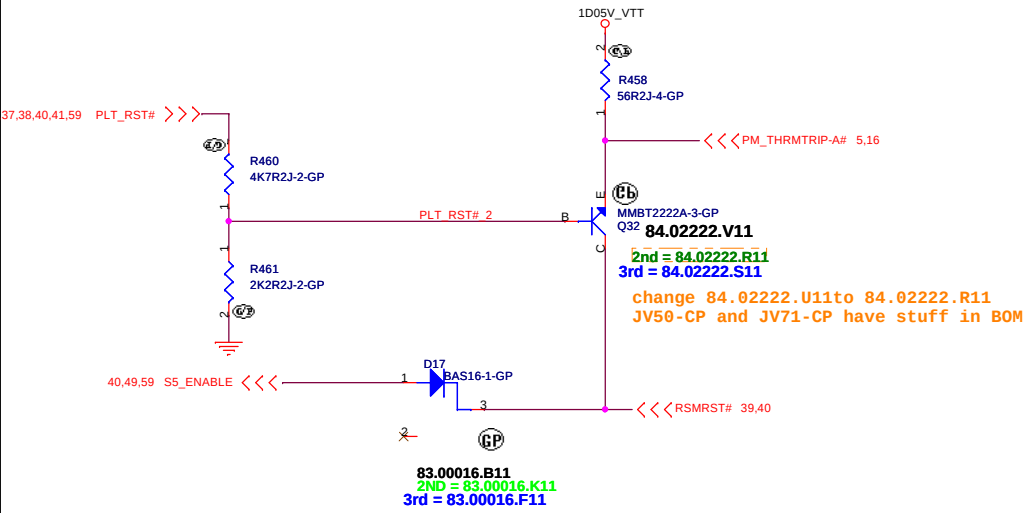
0804 SA Add Seligo Run Power SKT

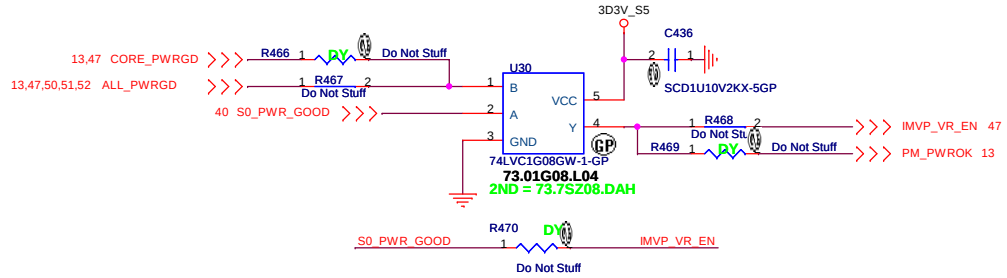


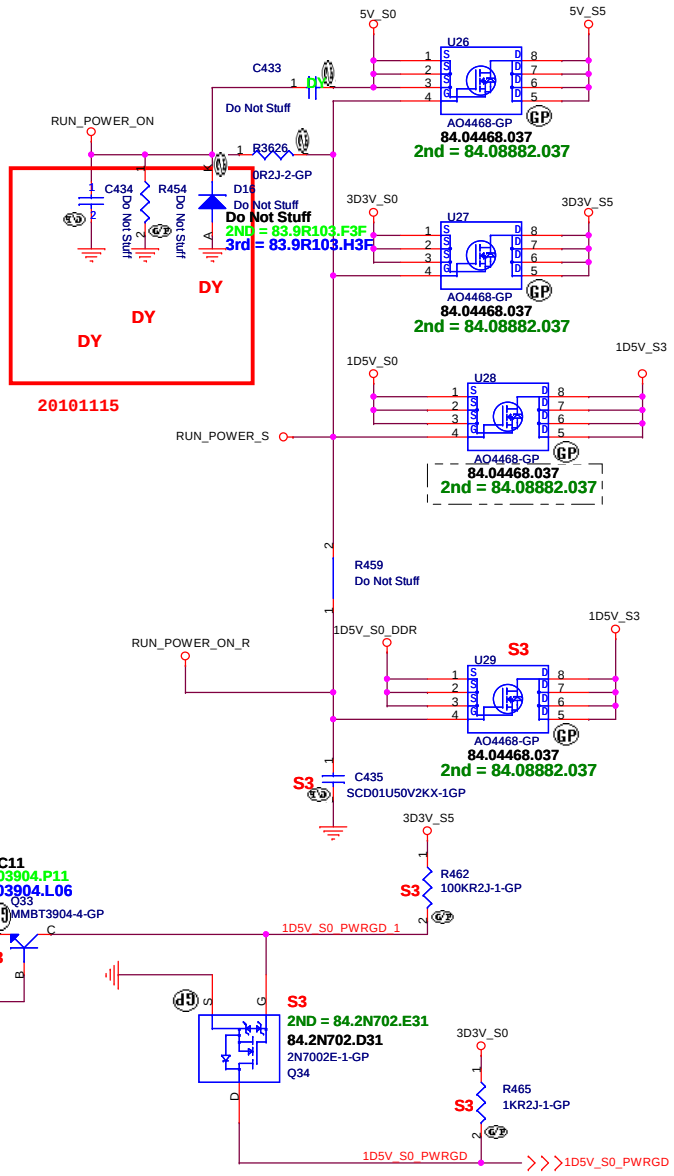
3D3V_AUX_S5

Del Aux Power schematic ,
it is not necessary for reservation

Run Power







PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

Hynix 1G 800M N11PGV SKU

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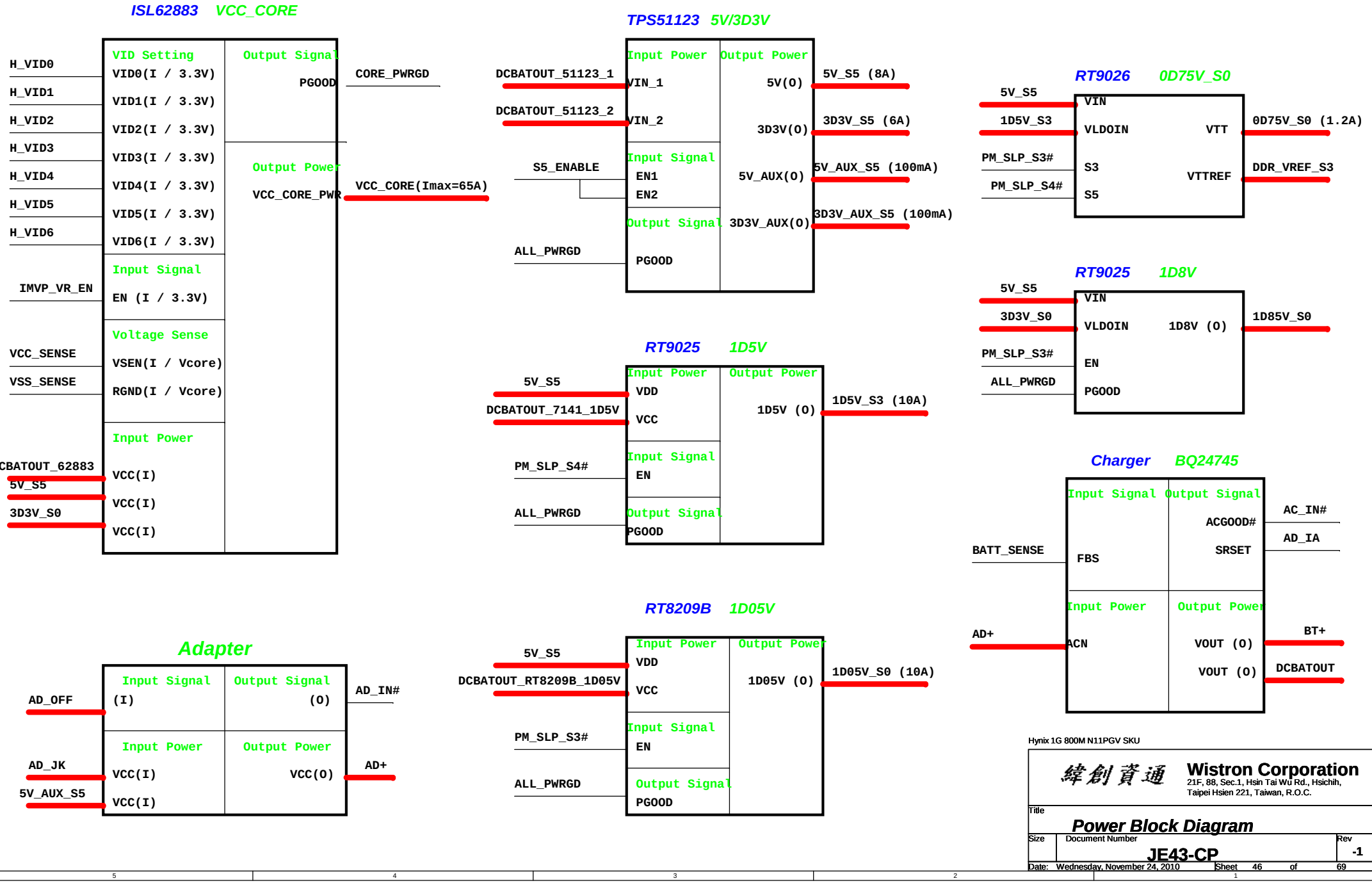
Title: ***RUN POWER and 3D3V_AUX_S5***

Size: | Document Number: **JE43-CP** | Rev: -1

Date: Wednesday, November 24, 2010 | Sheet 45 of 69



Hynix 1G 800M N11PGV SKU

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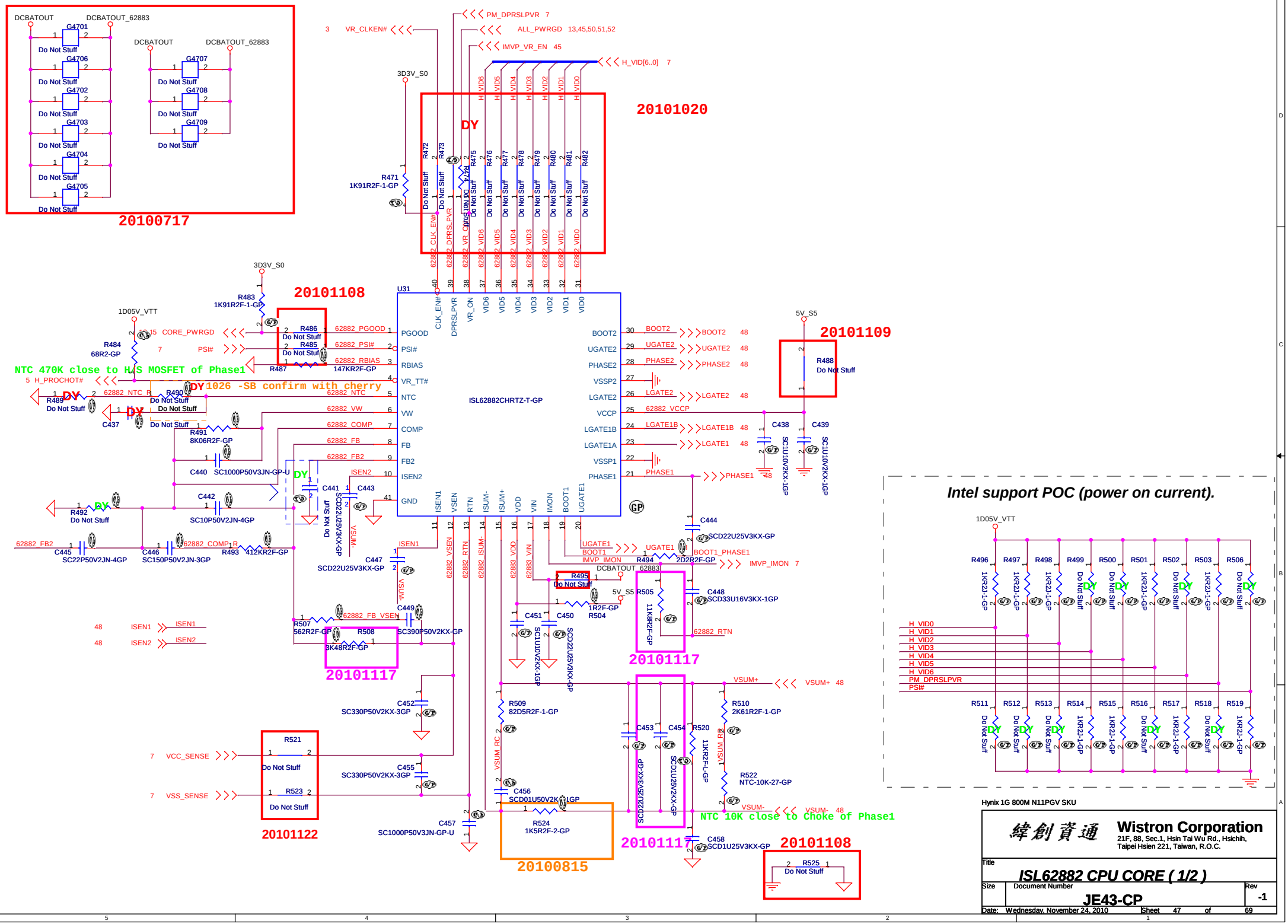
Title: Power Block Diagram

Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 46 of 69


DCBATOUT
DCBATOUT_62883
G4701
G4706
G4702
G4703
G4704
G4705
G4707
G4708
G4709
Do Not Stuff
20100717
PM_DPRSLPVR 7
ALL_PWRGD 13,45,50,51,52
IMVP_VR_EN 45
H_VID[6..0] 7
VR_CLKEN# 3
3D3V_S0
DY
20101020
R471 1K91R2F-1-GP
R472
R473
R475
R476
R477
R478
R479
R480
R481
R482
62882_CLK_EN#
62882_DPRSLPVR
62882_VR_ON
62882_VID6
62882_VID5
62882_VID4
62882_VID3
62882_VID2
62882_VID1
62882_VID0
U31
ISL62882CHRTZ-T-GP
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
20101108
1D05V_VTT
R483 1K91R2F-1-GP
R484 68R2-GP
R485 Do Not Stuff
R486 Do Not Stuff
R487 147KR2F-GP
R488 Do Not Stuff
R489 Do Not Stuff
R490 Do Not Stuff
R491 8K06R2F-GP
R492 Do Not Stuff
R493 412KR2F-GP
R494 2D2R2F-GP
R495 Do Not Stuff
R496 1KR2J-1-GP
R497 1KR2J-1-GP
R498 1KR2J-1-GP
R499 Do Not Stuff
R500 Do Not Stuff
R501 1KR2J-1-GP
R502 Do Not Stuff
R503 1KR2J-1-GP
R504 1R2F-GP
R505 11K8R2F-GP
R506 Do Not Stuff
R507 562R2F-GP
R508 3K48R2F-GP
R509 82D5R2F-1-GP
R510 2K61R2F-1-GP
R511 Do Not Stuff
R512 Do Not Stuff
R513 Do Not Stuff
R514 1KR2J-1-GP
R515 1KR2J-1-GP
R516 Do Not Stuff
R517 Do Not Stuff
R518 1KR2J-1-GP
R519 1KR2J-1-GP
R520 11KR2F-1-GP
R521 Do Not Stuff
R522 NTC-10K-27-GP
R523 Do Not Stuff
R524 1K5R2F-2-GP
R525 Do Not Stuff
C437 Do Not Stuff
C438 SC1U10V2KX-1GP
C439 SC1U10V2KX-1GP
C440 SC1000P50V3JN-GP-U
C441 SCD22U25V3KX-GP
C442 SC10P50V2JN-4GP
C443 SCD22U25V3KX-GP
C444 SCD22U25V3KX-GP
C445 SC22P50V2JN-4GP
C446 SC150P50V2JN-3GP
C447 SCD22U25V3KX-GP
C448 SCD33U16V3KX-1GP
C449 SC390P50V2KX-GP
C450 SCD22U25V3KX-GP
C451 SC1U10V2KX-1GP
C452 SC330P50V2KX-3GP
C453 SCD22U25V3KX-GP
C454 SCD1U25V3KX-GP
C455 SC330P50V2KX-3GP
C456 SCD01U50V2KX-1GP
C457 SC1000P50V3JN-GP-U
C458 SCD1U25V3KX-GP
20101117
20101122
20100815
20101108
20101109
5V_S5
1D05V_VTT
NTC 470K close to H/S MOSFET of Phase1
DY1026 -SB confirm with cherry
NTC 10K close to Choke of Phase1
CORE_PWRGD
PSI#
H_PROCHOT#
VCC_SENSE
VSS_SENSE
62882_PGOOD
62882_PSI#
62882_RBIAS
62882_NTC
62882_VW
62882_COMP
62882_FB
62882_FB2
62882_VCCP
62882_RTN
62882_FB_VSEN
62882_COMP_R
BOOT2
UGATE2
PHASE2
LGATE2
LGATE1B
LGATE1
PHASE1
BOOT1_PHASE1
IMVP_IMON
DCBATOUT_62883
VSUM+
VSUM-
VSUM_RC
VSUM_FB
ISEN1
ISEN2
Intel support POC (power on current).
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
Hynix 1G 800M N11PGV SKU
緯創資通
Wistron Corporation
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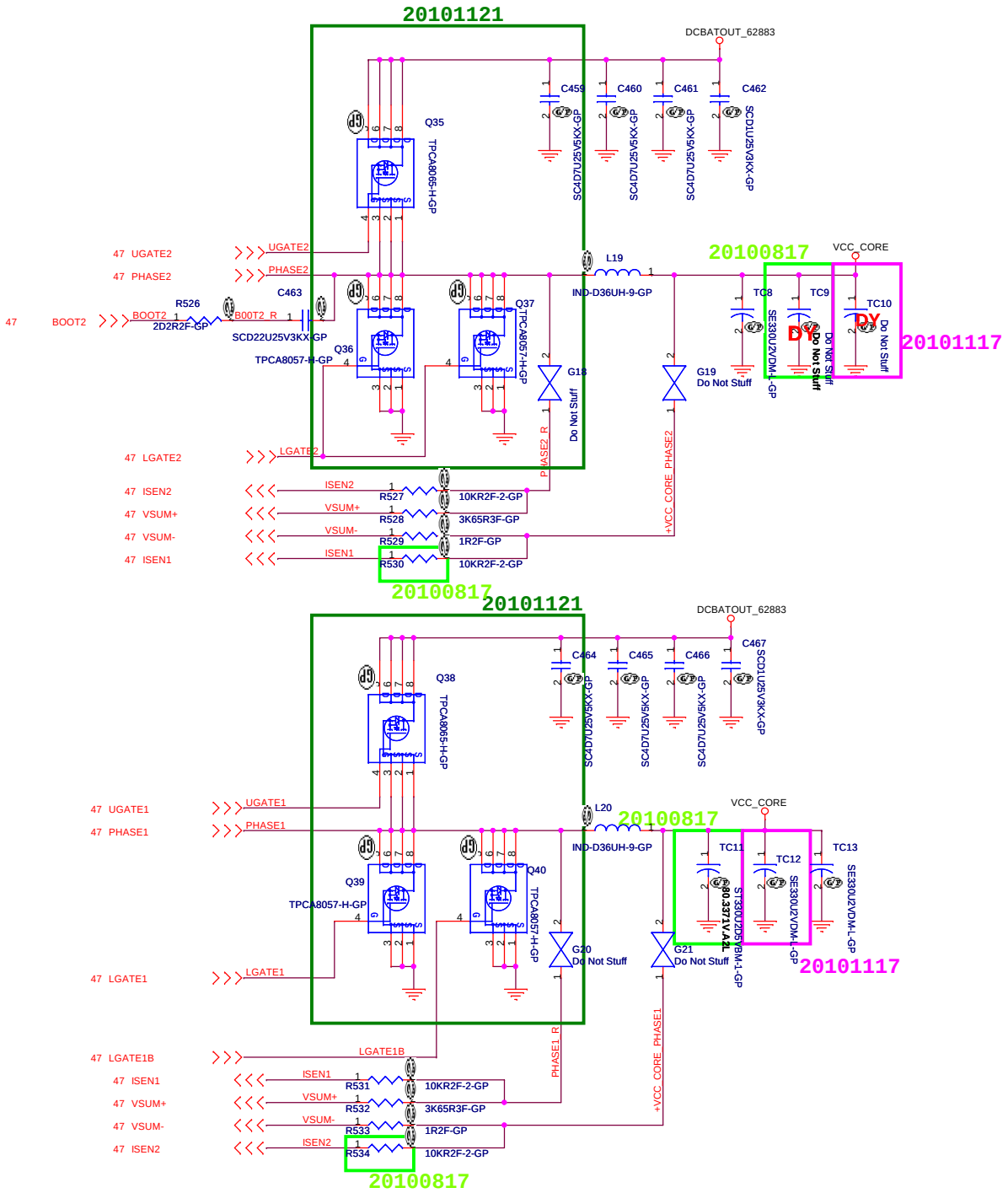
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
JE43-CP
Rev
-1
Date: Wednesday, November 24, 2010
Sheet 47 of 69



Vcc_core
Iomax=48A
OCP>72A

Hynix 1G 800M N11PGV SKU

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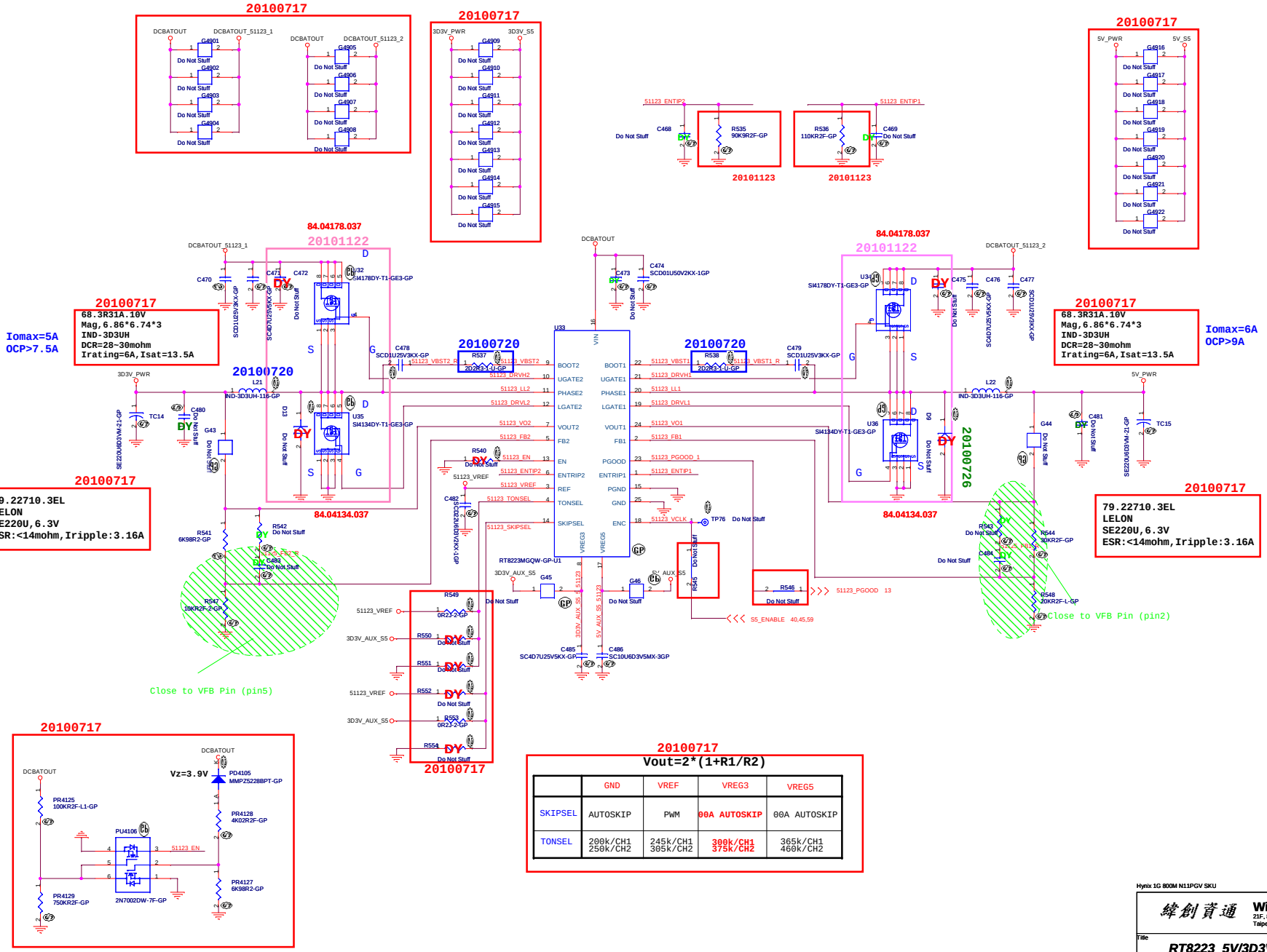
Title: ISL62882 CPU CORE (2/2)

Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 48 of 69



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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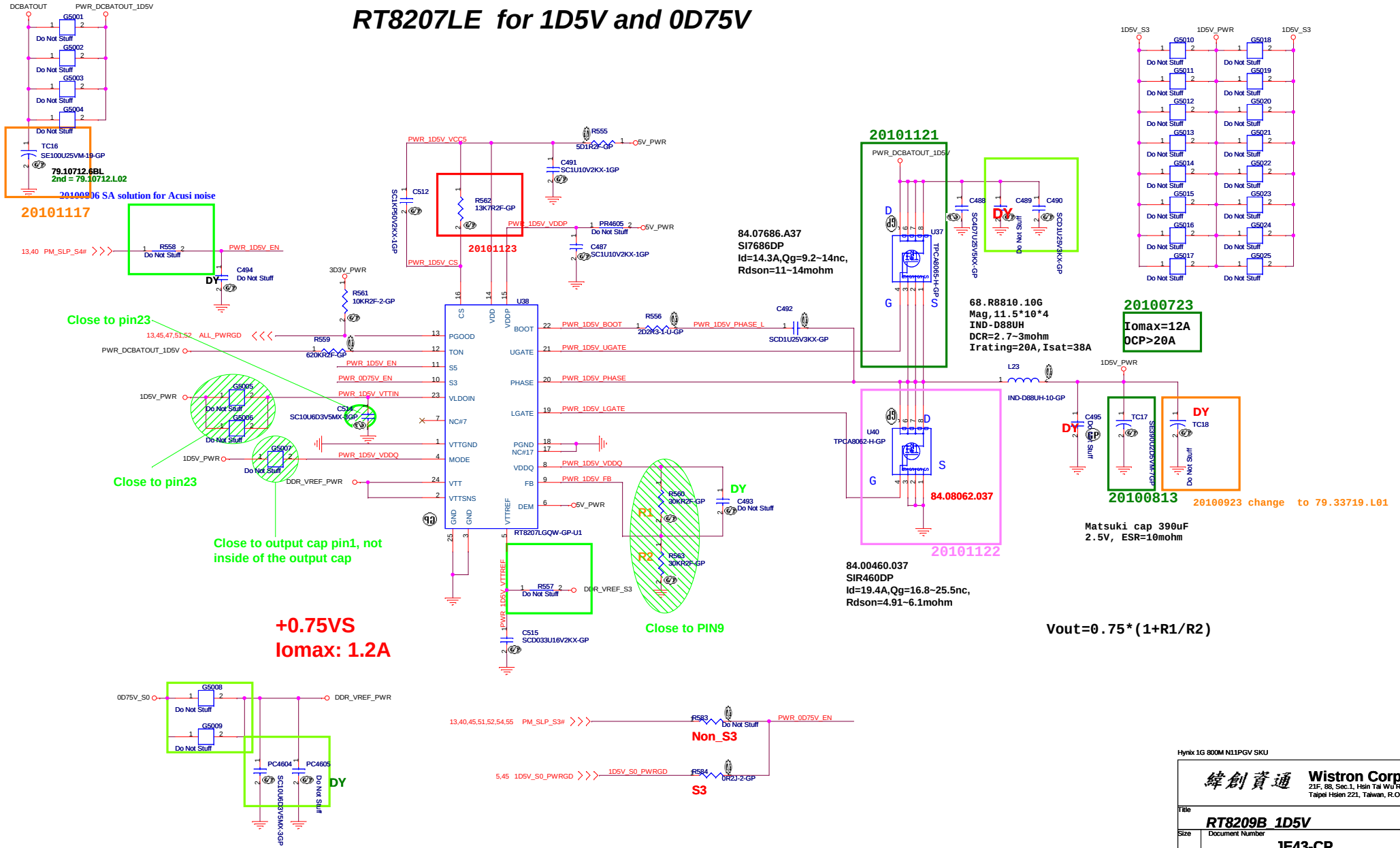
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223 5V/3D3V

Size: | Document Number: JE43-CP | Rev: -1

Date: Wednesday, November 24, 2010 | Sheet 49 of 69

RT8207LE for 1D5V and 0D75V



Hynix 1G 800M N11PGV SKU

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Title		
RT8209B 1D5V		
Size	Document Number	Rev
	JE43-CP	-1
Date: Wednesday, November 24, 2010	Sheet 50 of 69	

RT8209E for VCCP

20100717

DCBATOUT DCBATOUT_RT8209B_VCCP

G5101 Do Not Stuff
G5102 Do Not Stuff
G5103 Do Not Stuff
G5104 Do Not Stuff
G5105 Do Not Stuff
G5106 Do Not Stuff

20101121

DCBATOUT_RT8209B_VCCP

D41 TPCA8065-H-GP
C497 DY Do Not Stuff
C496 SC4D7U25V5KX-GP
C498 SC4D7U25V5KX-GP
C499 SCD1U25V3KX-GP

Iomax=22A
OCP>33A

Vout=0.75*(1+R1/R2)

5V_S5

C500 SC1U10V2KX-1GP
C503 SC1U10V2KX-1GP
R566 2D2R2F-GP
RT8209B_VCCP_V5FILT

R567 0R3J-0-U-GP
RT8209B_VCCP_LL_1
C501 SCD1U25V3KX-GP

R565 Do Not Stuff
RT8209B_VCCP_DRVH_R

L24 IND-D36UH-9-GP
Vout=1.0625(Cal)
+VCCP_PWR

U42 TPCA8062-H-GP
U43 TPCA8062-H-GP

C502 DY Do Not Stuff
TC19 SE330U2VDM-L-GP
TC20 SE330U2VDM-L-GP
R568 10KR2F-2-GP
R569 24KR2F-GP
RT8209B_VCCP_VFB

84.08062.037
84.08062.037

20100717
79.33719.L01
Panasonic
SE330U , 2V
ESR:9mohm,Iripple:3A

20100717

U44
VDD VDDP FB BOOT EN/DEM TON CS
UGATE LGATE PHASE VOUT PGOOD GND PGND NC#15
RT8209PGQW-GP

RT8209B_VCCP_DRVH
RT8209B_VCCP_DRVL
RT8209B_VCCP_LL
RT8209B_VCCP_VFB
VCCP_RUN ON
RT8209B_VCCP_TON
RT8209B_VCCP_TRIP
+VCCP_PWR
VTT_PWRGD
VTT_PWRGD 40

R570 Do Not Stuff
R571 DY Do Not Stuff
R572 200KR2F-L-GP
13,45,47,50,52 ALL_PWRGD
13,40,45,50,52,54,55 PM_SLP_S3#

R573 10K2R2F-GP

20101109
20101123
20101122

Freq=360KHz

becasue of 1.05V_S0 and 1.05V_VTT combin togther
use PM_SLP_S3# Enable 1.05V power

3D3V_S0
R575 10KR2J-3-GP
2N7002KDW-GP
VTT_PWRGD
C504 SCD1U10V2KX-5GP
Q41
H_VTTPWRGD_R
84.2N702.A3F
2nd = 84.DM601.03F
H_VTTPWRGD

3D3V_S5
R576 100KR2J-1-GP

1D05V_VTT
R577 1KR2J-1-GP
H_VTTPWRGD 5

RT8209B_VCCP_VFB
R574 DY Do Not Stuff
VTT_SENSE 7

20100717

+VCCP_PWR 1D05V_VTT

G5107 Do Not Stuff
G5108 Do Not Stuff
G5109 Do Not Stuff
G5110 Do Not Stuff
G5111 Do Not Stuff
G5112 Do Not Stuff
G5113 Do Not Stuff
G5114 Do Not Stuff
G5115 Do Not Stuff
G5116 Do Not Stuff
G5117 Do Not Stuff
G5118 Do Not Stuff
G5119 Do Not Stuff
G5120 Do Not Stuff
G5121 Do Not Stuff
G5122 Do Not Stuff
G5123 Do Not Stuff
G5124 Do Not Stuff
G5125 Do Not Stuff
G5126 Do Not Stuff

Hynix 1G 800M N11PGV SKU

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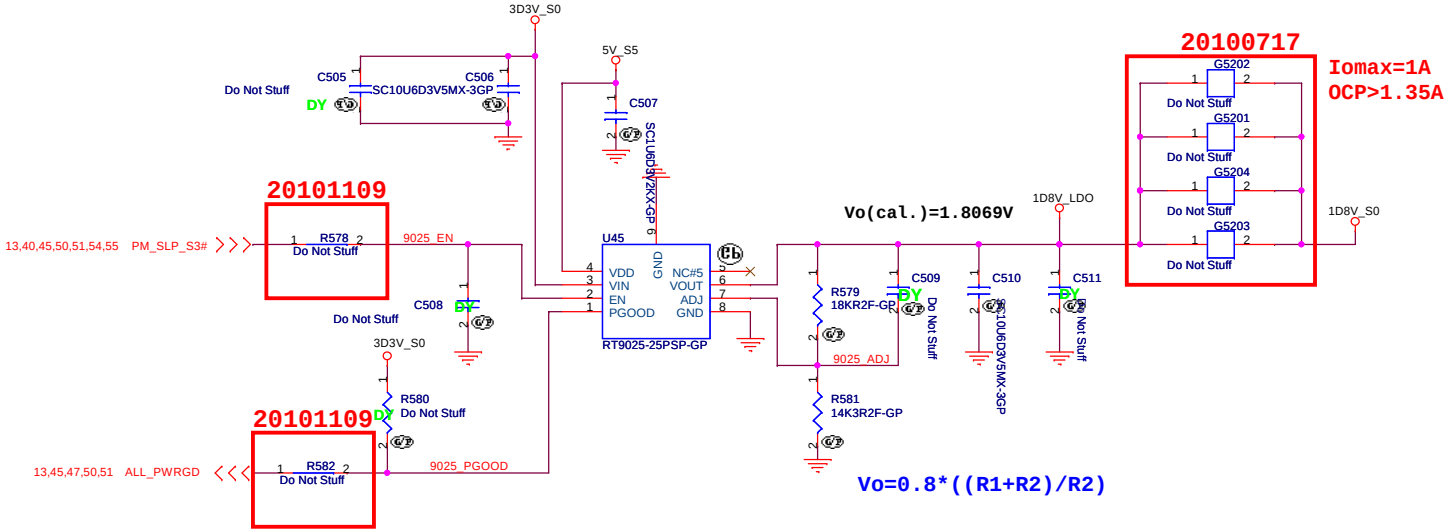
Title: RT8209B +VCCP
Size: Document Number: JE43-CP Rev: -1
Date: Wednesday, November 24, 2010 Sheet 51 of 69

RT9025 for 1D8V_S0

20090915



Hynix 1G 800M N11PGV SKU

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*RT9025_1D8V/RT9026_0D75*	
Size	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 52 of 69	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

ADD A 24V ZENAR

20100720

20100720

20100720

20100806

20101109

20101109

20100726

20100723

20100723

20101121

20101118

20100719

20100717

20100706 Wayne

84.P1403.B37

84.P1403.B37

83.00400.C1F
2nd = 83.1S400.B2F

83.R0203.08F
2nd = 83.1R003.I8F

83.SMF18.0AH

84.08884.A37
FDMC8884
Id=9A,Qg=5-9nc,
Rdson=22~30mohm

68.4R71C.10K
CYNTEC,6.87x6.47x3.0
L-4D7UH
DCR=37~40mohm
Irating=5.5A,Isat=10A

84.07692.A37
FDMC7692
Id=13.3A,Qg=10-20nc,
Rdson=9.5~11.5mohm

74.24745.073

84.2N702.A3F
2nd = 84.DM601.03F

STOP_CHG# to KBC

CHG_ON# to KBC

AC_IN# to KBC

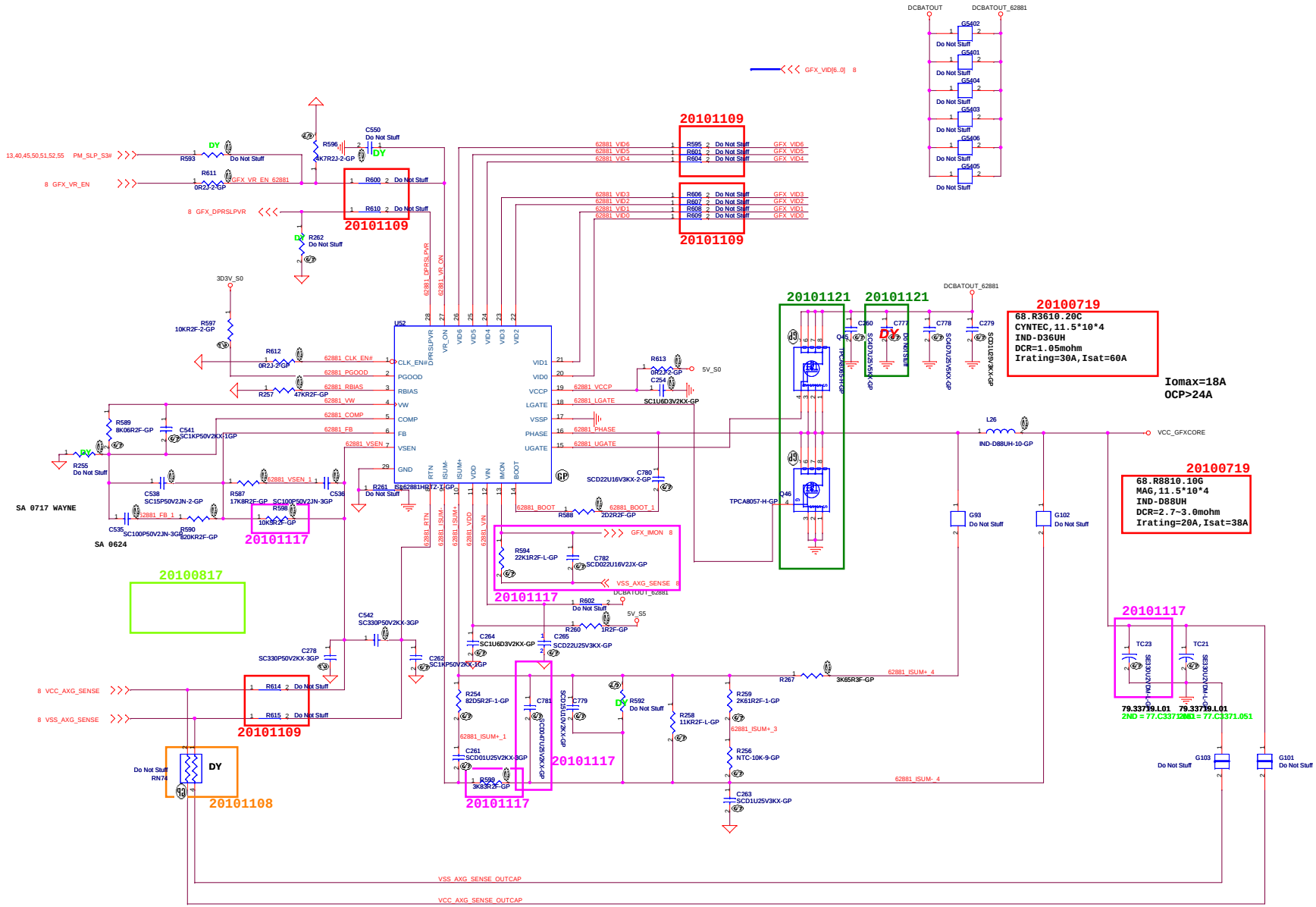
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: JE43-CP | Rev: -1

Date: Wednesday, November 24, 2010 | Sheet 53 of 69



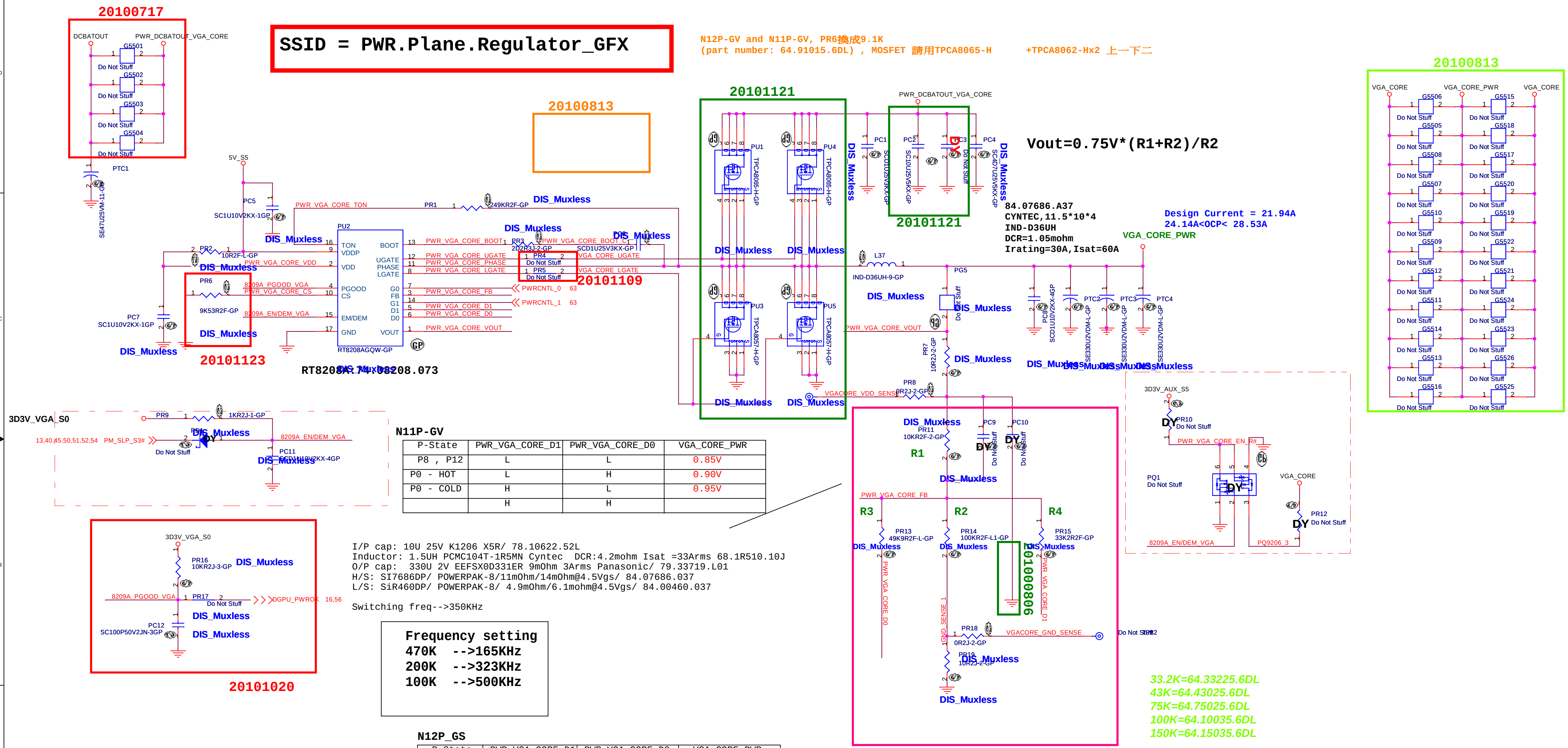
Hynix 1G 800M N11PGV SKU

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL62881_+VCC_GFXCORE**

Size	Document Number	Rev
A2	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 54 of 69



SSID = PWR.Plane.Regulator_GFX

N12P-GV and N11P-GV, PR6換成9.1K
(part number: 64.91015.6DL) , MOSFET 請用TPCA8065-H +TPCA8062-Hx2 上一下二

RT8208A:74.08208.073

N11P-GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	0.90V
P0 - COLD	H	L	0.95V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

N12P_GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.05V
	H	H	

N12P_GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.02V
	H	H	

N12P GS:PR11=10K,PR14=100K,PR13=49.9K,PR15=33.2K
N12P GV: PR11=10K,PR14=75K,PR13=49.9K,PR15=43K
N11P GV: PR11=10K,PR14=75K,PR13=150K,PR15=75K

Hynix 1G 800M N11PGV SKU

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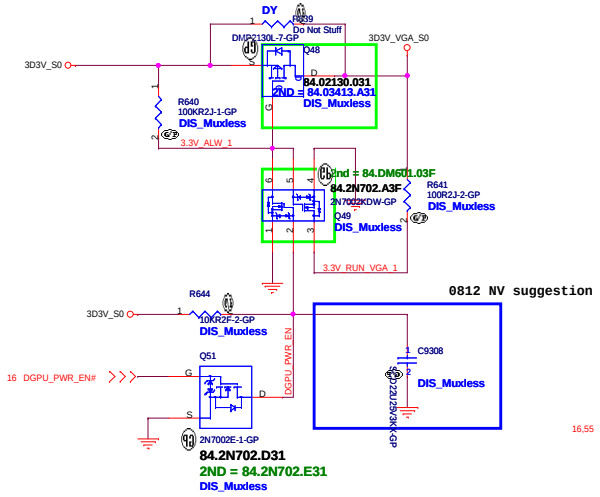
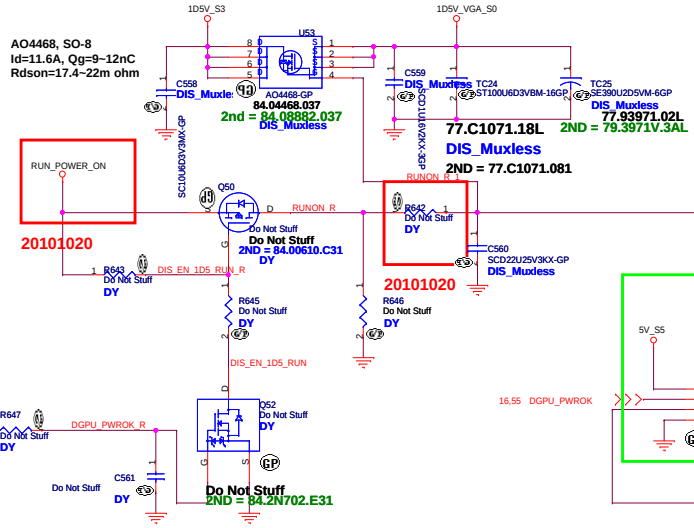
Title: RT8208B_+VGA_CORE
Size: Custom | Document Number: JE43-CP | Rev: -1
Date: Wednesday, November 24, 2010 | Sheet 55 of 69

+3VS to 3.3V_DELAY Transfer

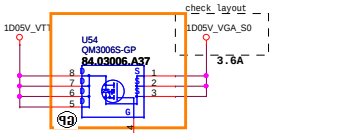
+3VS to 3.3V_DELAY Transfer

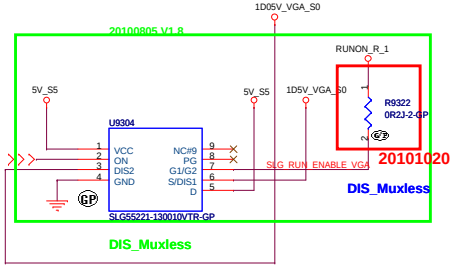


1D5V_VGA_S0



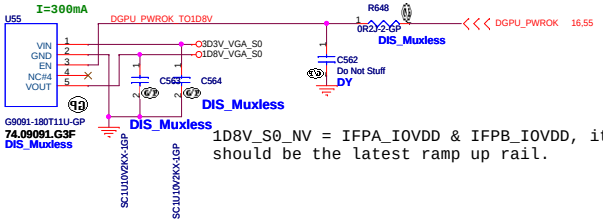
1.05V to 1.05V_VGA_S0 Transfer





RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
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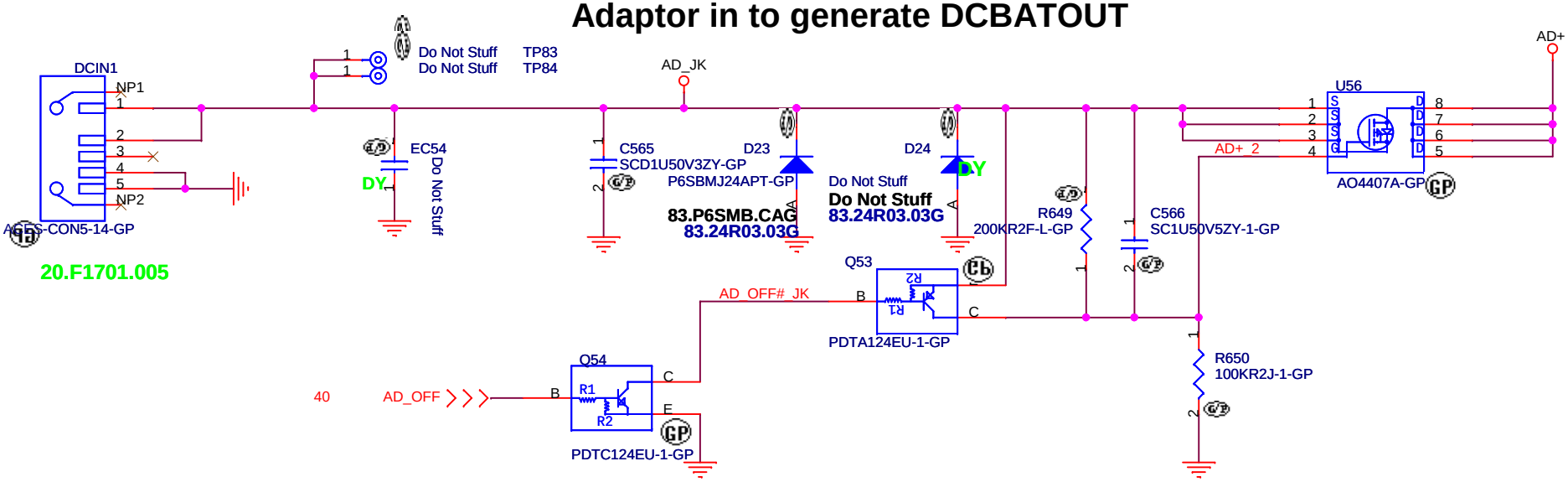
Title: DISCRETE VGA POWER

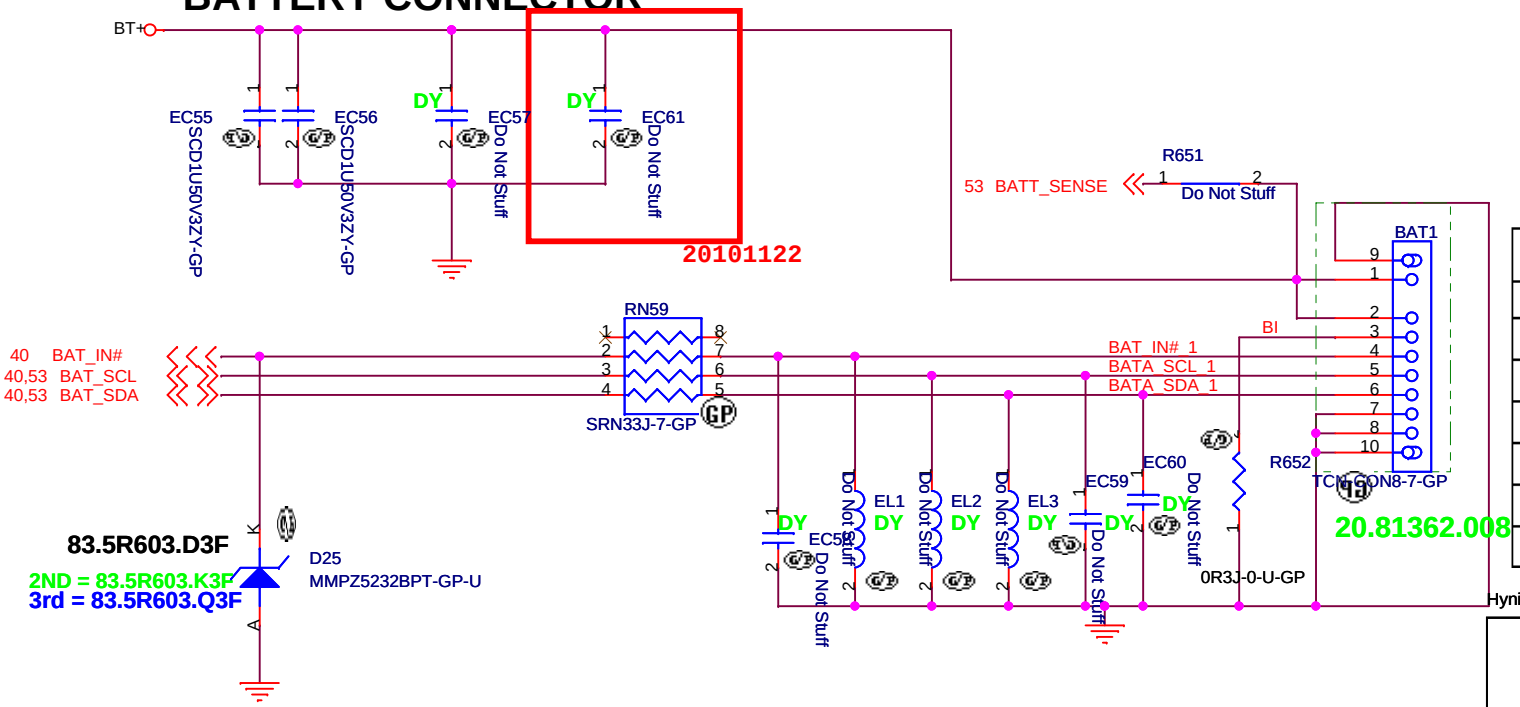
Size	Document Number	Rev
C	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 56 of 69

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

Hynix 1G 800M N11PGV SKU

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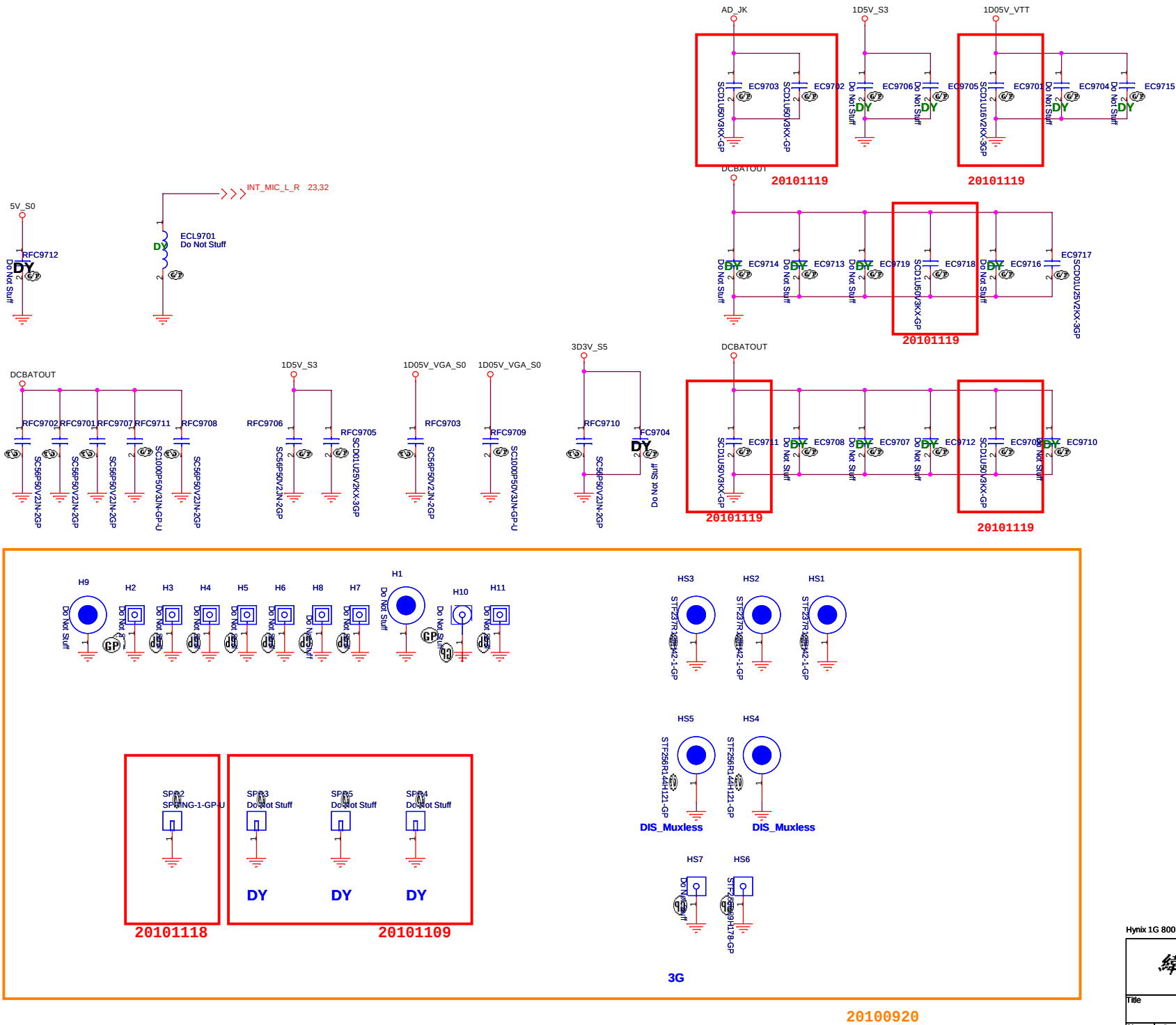
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 57 of 69



Hynix 1G 800M N11PGV SKU

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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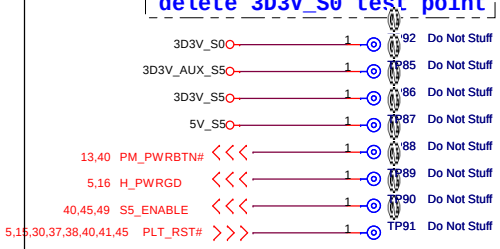
Title: ***EMI/Spring/Boss***

Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 58 of 69

Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

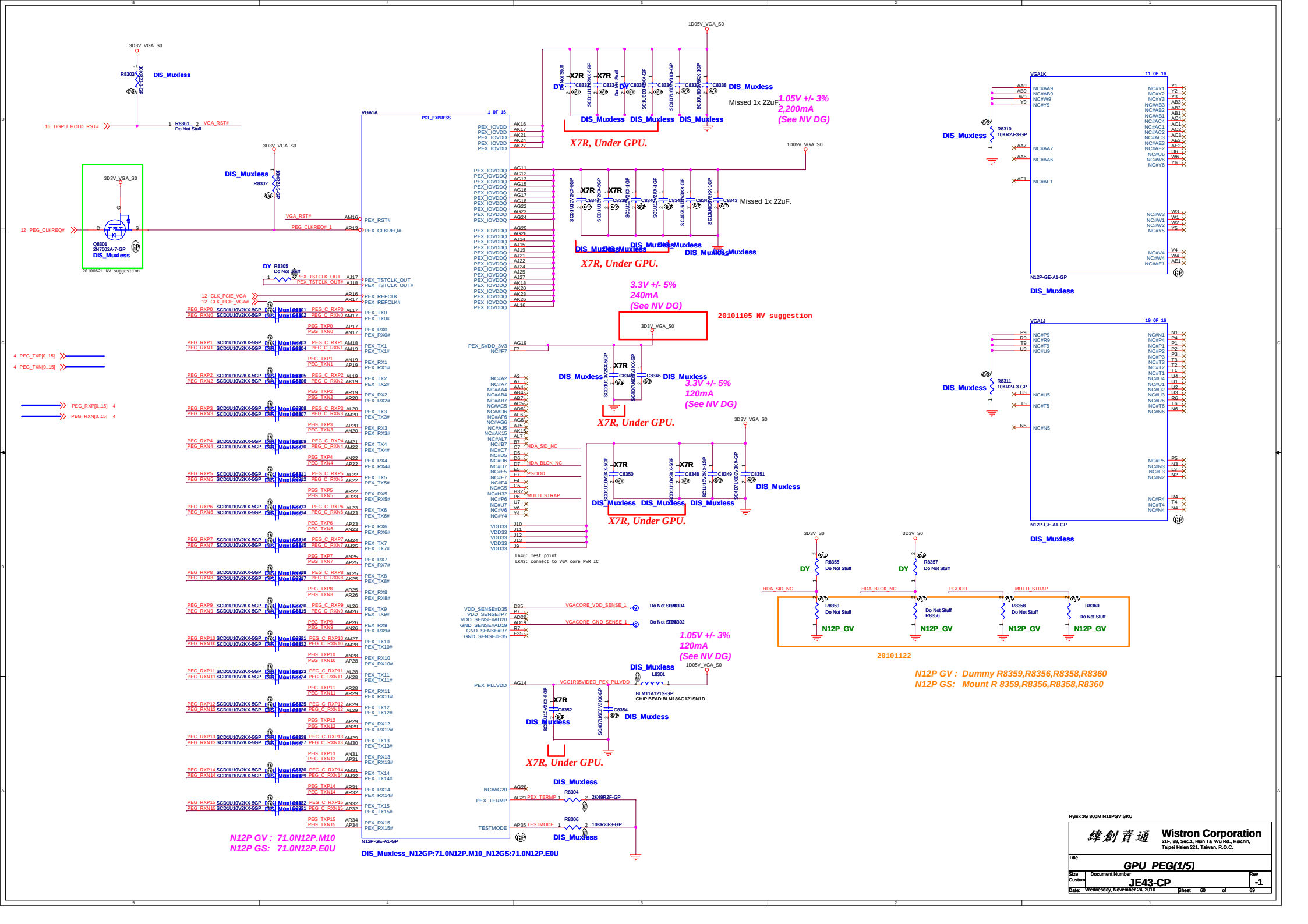
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AFTE_TP

Size | Document Number: JE43-CP | Rev: -1

Date: Wednesday, November 24, 2010 | Sheet 59 of 69



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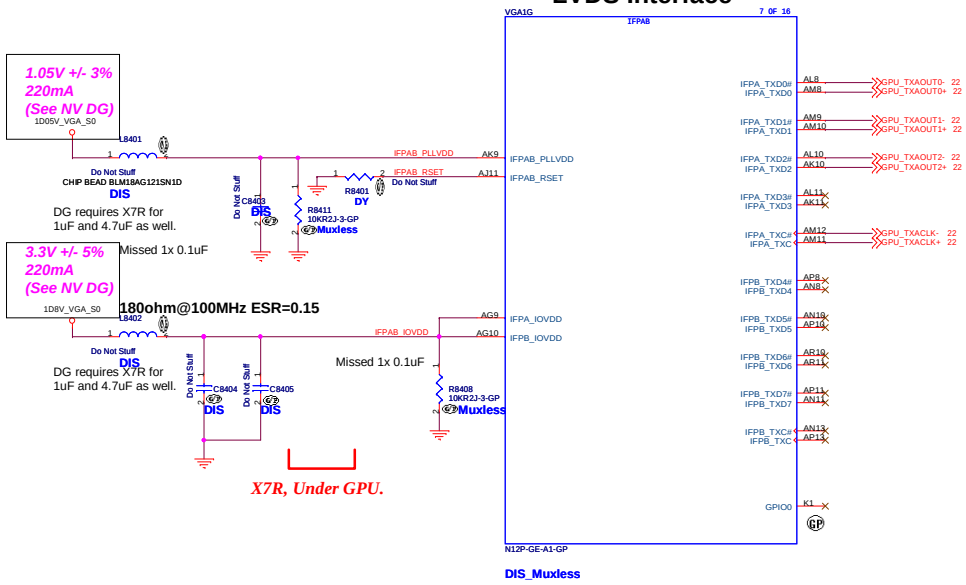
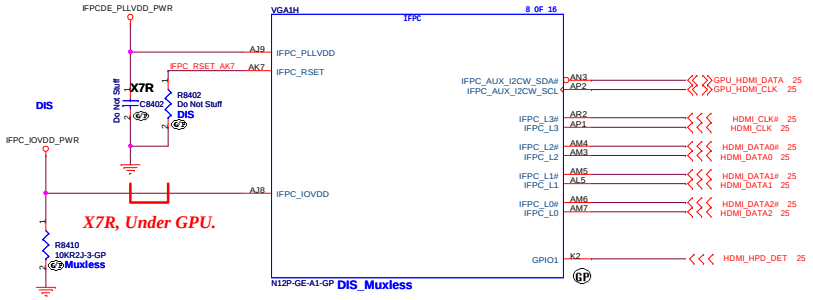
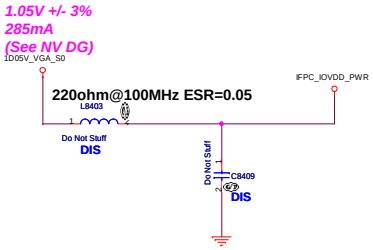
Title	GPU_PEG(1/5)		
Size: Custom	Document Number: JE43-CP		Rev: -1
Date: Wednesday, November 24, 2010	Sheet 60 of 69		

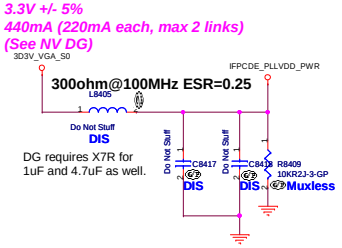
LVDS Interface

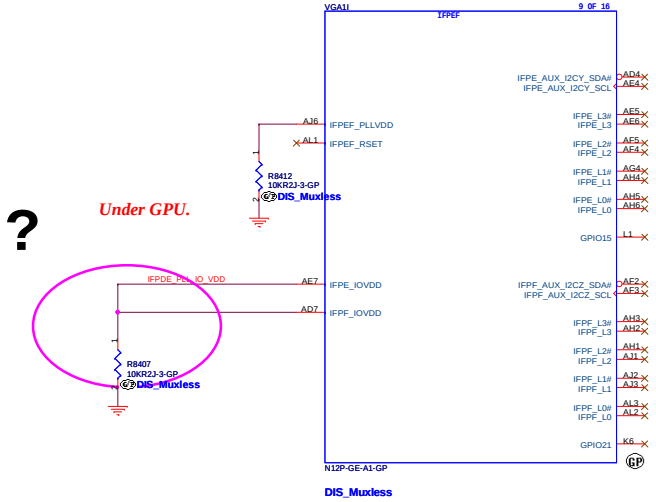


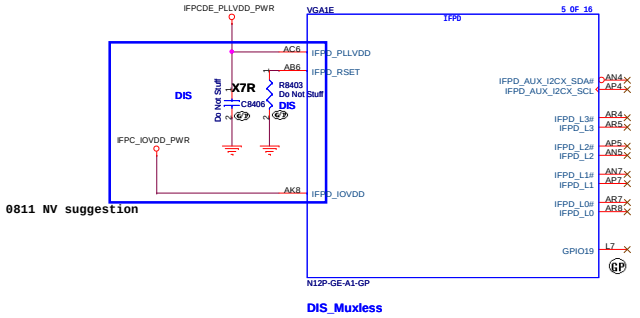
HDMI Interface











Hynix 1G 800M N11PGV SKU

緯創資通 **Wistron Corporation**
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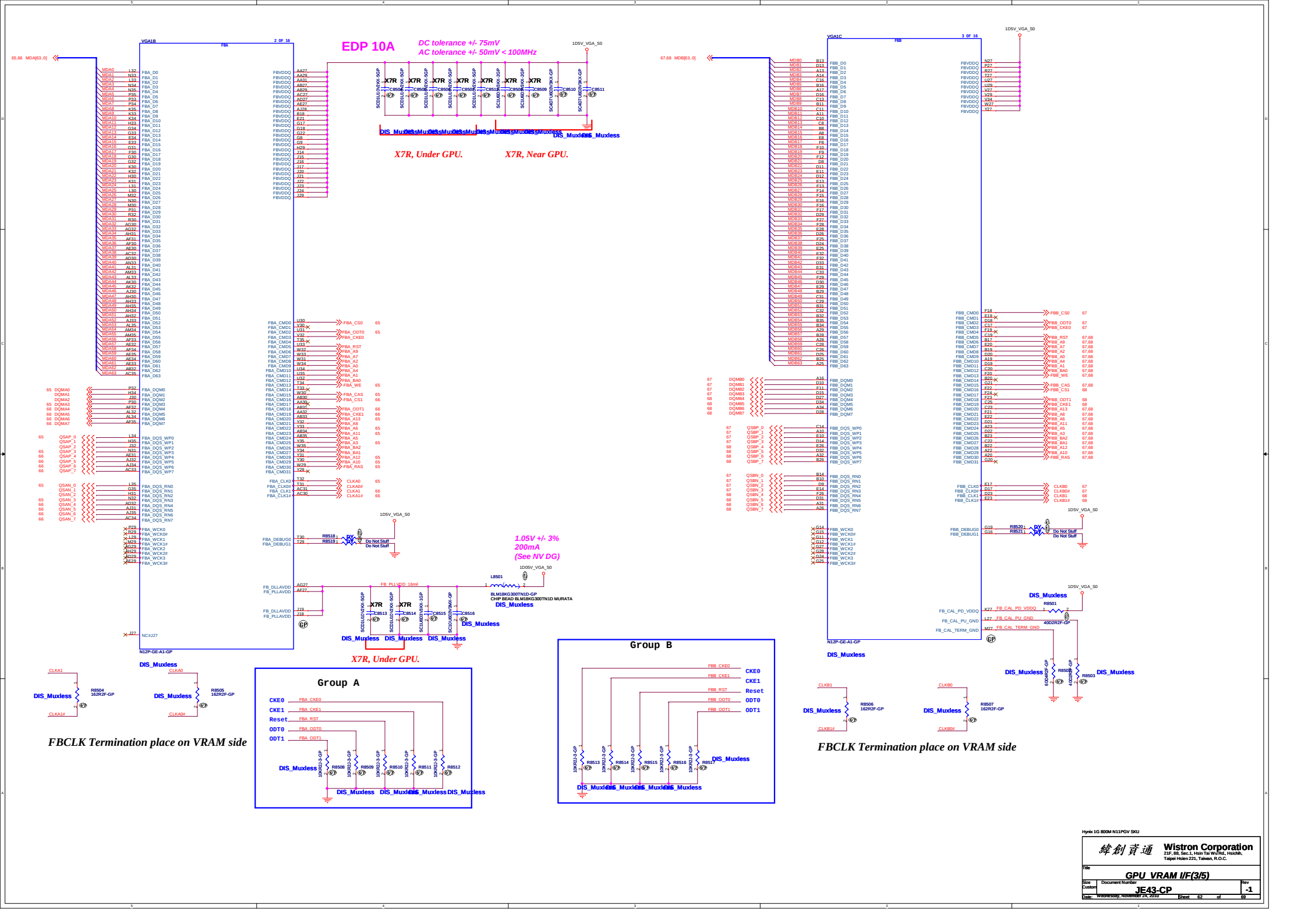
Taipei Hsien 221, Taiwan, R.O.C.

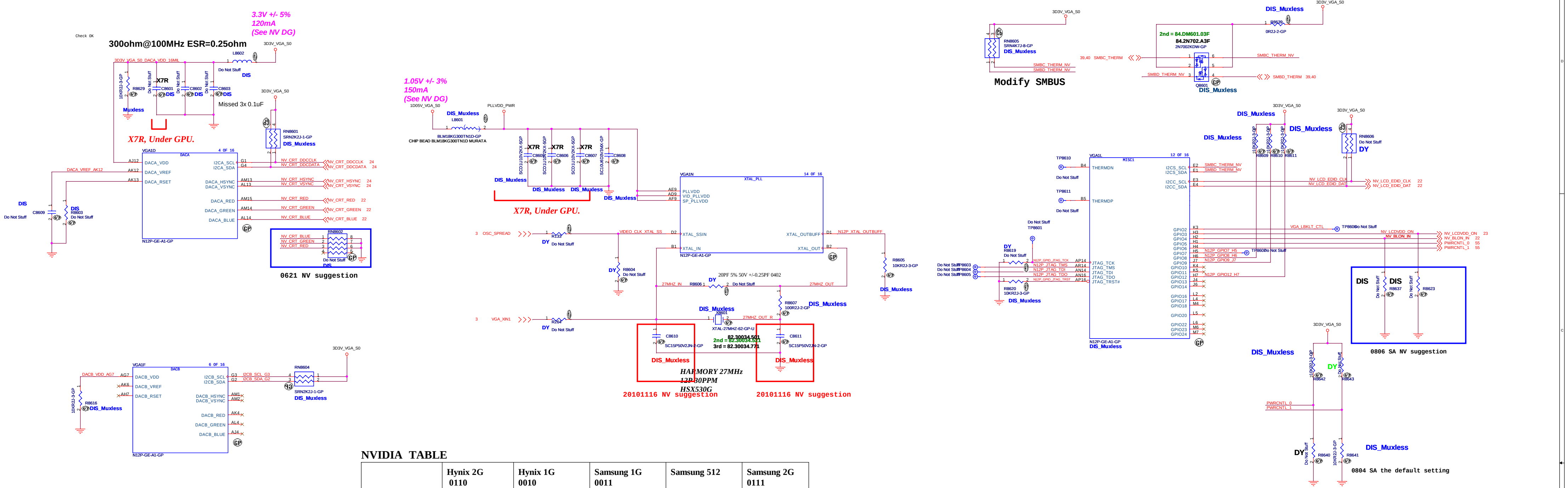
Title: **GPU DIGITAL OUT(2/5)**

Size	Document Number	Rev
Custom	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 61 of 69


EDP 10A
DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz
X7R, Under GPU.
X7R, Near GPU.
1.05V +/- 3%
200mA
(See NV DG)
X7R, Under GPU.
Group A
Group B
FBCLK Termination place on VRAM side
FBCLK Termination place on VRAM side
Wistron Corporation
GPU VRAM I/F(3/5)
JE43-CP

VGA Thermal sensor 787



NVIDIA TABLE

	Hynix 2G 0110 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
64Mx16 DDR3	Hynix	0x2	H5TQ1G63DFR-11C	900/800
	Samsung	0x3	K4W1G1646E-HC11	900
	Samsung	TBD	K4W1G1646G-BC11	900/800
	Hynix	0x0	H5TQ1G63BFR-12C	800
	Samsung	0x1	K4W1G1646E-HC12	800

```
GPU_ROM_SI   for 1Gbit       for 2Gbit       for 1Gbit       for 2Gbit
             Hynix VRAM      Hynix VRAM      Samsung VRAM    Samsung VRAM
             RAM_CFG[0]=0    RAM_CFG[0]=0    RAM_CFG[0]=1    RAM_CFG[0]=1
             RAM_CFG[1]=1    RAM_CFG[1]=1    RAM_CFG[1]=1    RAM_CFG[1]=1
             RAM_CFG[2]=0    RAM_CFG[2]=1    RAM_CFG[2]=0    RAM_CFG[2]=1
             RAM_CFG[3]=0    RAM_CFG[3]=0    RAM_CFG[3]=0    RAM_CFG[3]=0

GPU_ROM_SO        VGA_DEVICE    =1 (low bit)
                  SMB_ALT_ADDR  =0
                  FB_0_BAR_SIZE =0
                  XCLK_417      =0 (High bit)

GPU_ROM_SCLK   PEX_PLL_EN_TERM =0
               SLOT_CLK_CFG    =1
               SUB_VENDOR      =0
               PCI_DEVID[4]    =1   N11P Fermi QS 1
```

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

TABLE NVIDIA

71.0N12P.E0U 71.0N12P.A0U

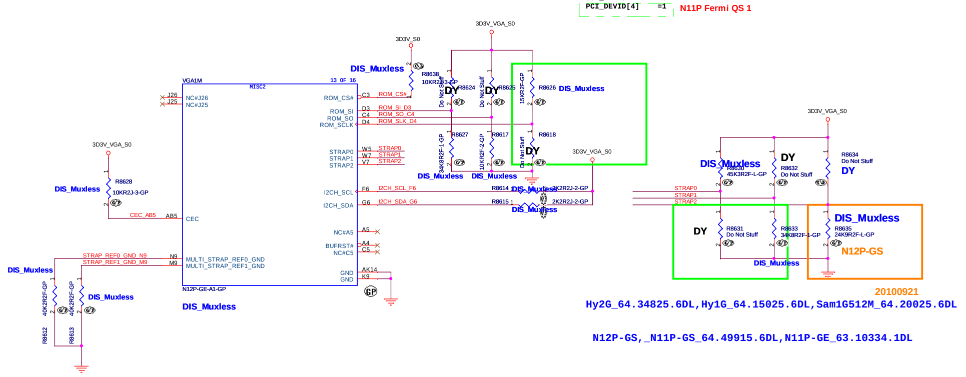
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GV DEV ID: 0x0DF5 (0101)
STRAP2 PU R8634	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

N12P-GS | N12P-GV | N11P-GE Pull Low | N11P-GS Pull Low | N12P-GE

```
STRAP0   USER[0]=1
         USER[1]=1
         USER[2]=1   USE 1111 (45K)
         USER[3]=1

STRAP1   3GIO_PADCFG[0]=0    0
         3GIO_PADCFG[1]=1    1
         3GIO_PADCFG[2]=1    1
         3GIO_PADCFG[3]=1    0   USE 0110 (35K)

STRAP2   PCI_DEVID[0]=1 N12P-GS   GF108-730-A1  0x0DF4 (0X4)  (0100)
         PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1  0x0DF7 (0X7)  (0111)
         PCI_DEVID[2]=0 N11P-GS Fermi  0x0DF0 (0000)
         PCI_DEVID[3]=0 N11P-GE Fermi  0x0DF1 (0001)
```



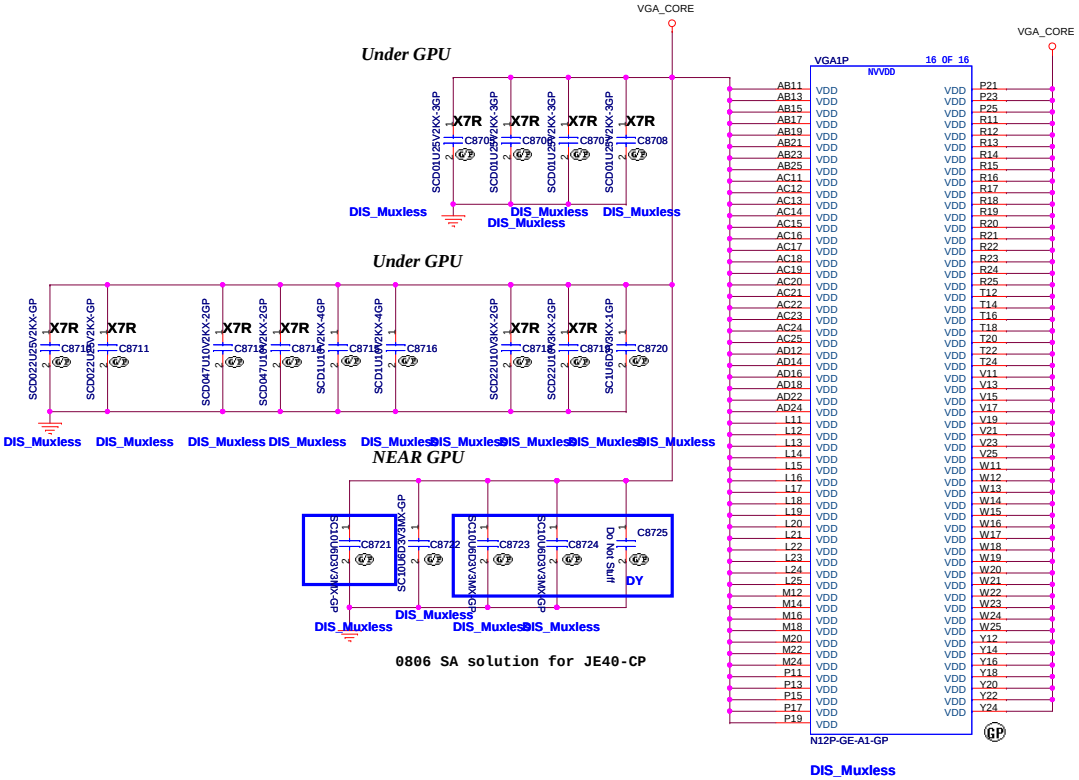
Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL

N12P-GS,_N11P-GS_64.49915.6DL,N11P-GE_63.10334.1DL

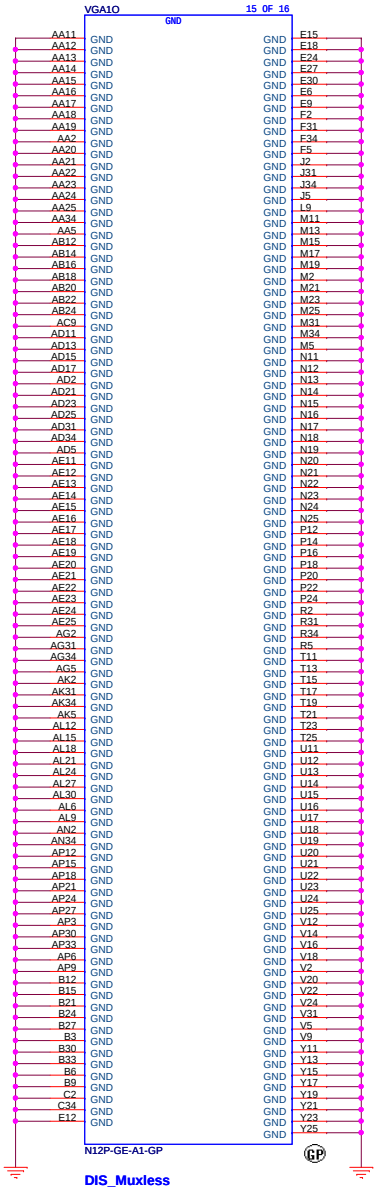
Hynix 1G 800M N11PGV SKU

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_GPIO/STRAP(4/5)
Size Custom / Document Number	JE43-CP / Rev -1
Date: Wednesday, November 24, 2010	Sheet 63 of 69

EDP 50A
(TDP 37W)



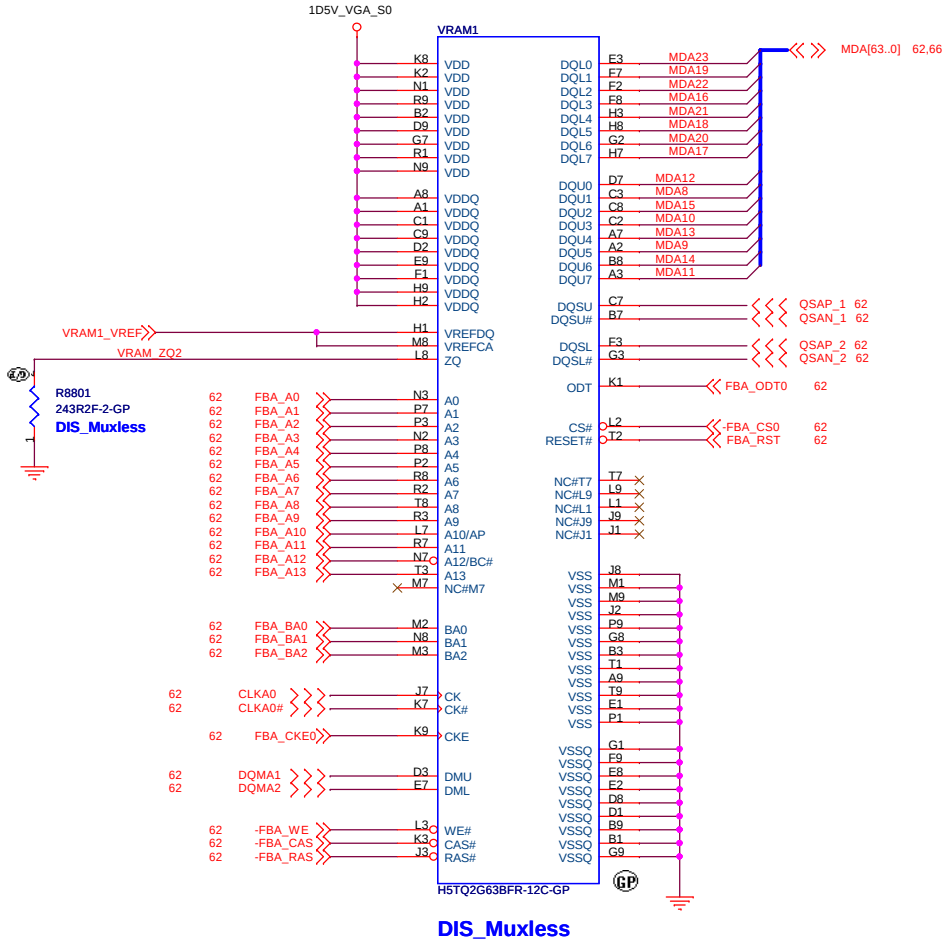
0806 SA solution for JE40-CP

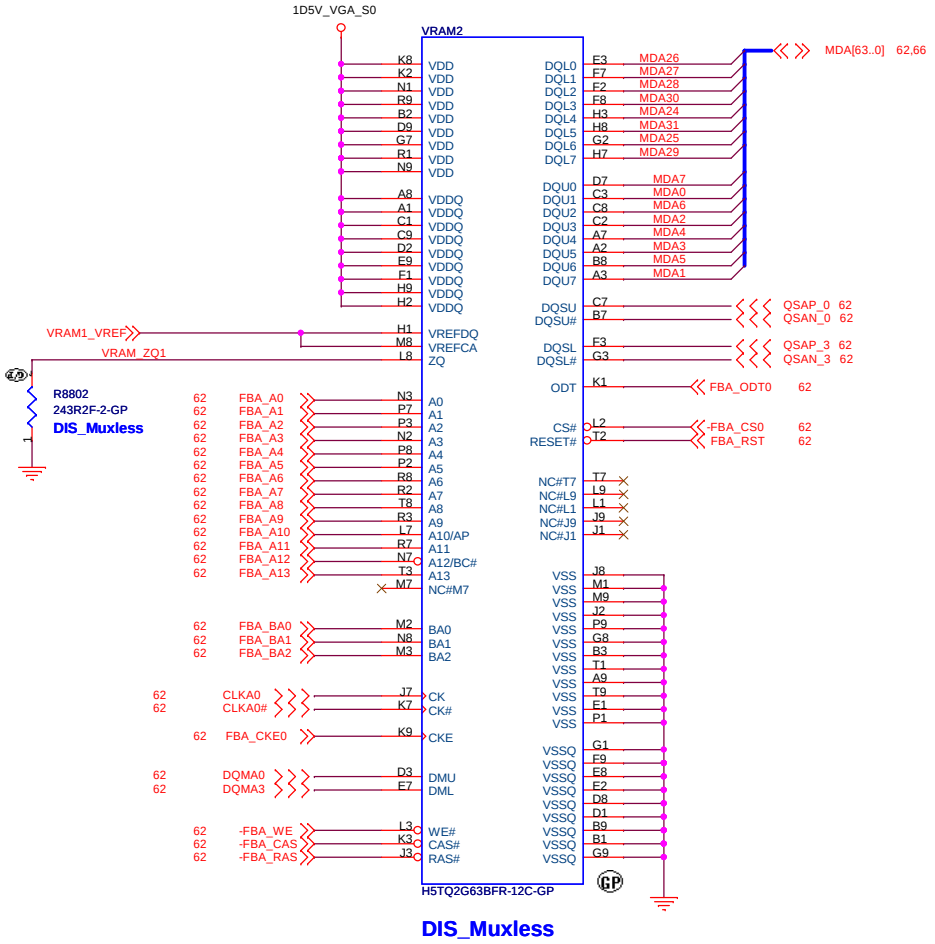


Hynix 1G 800M N11PGV SKU

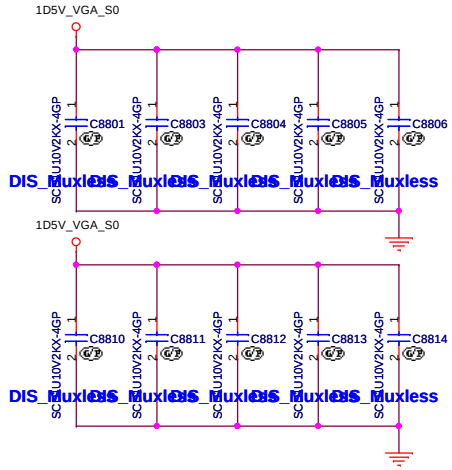
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

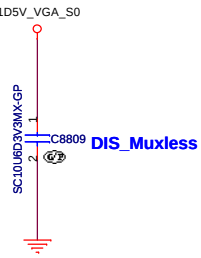
Title	GPU_DPPWR/GND(5/5)	
Size: Custom	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 64 of 69	

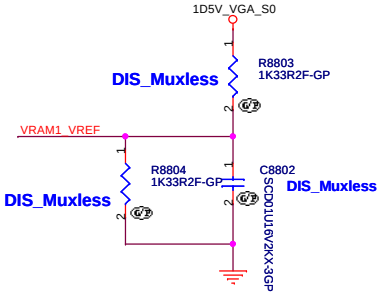


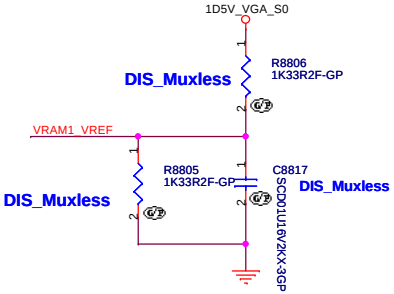


Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX4_VR.1GB0G.004,Sam512X4_VR.1GB0B.006



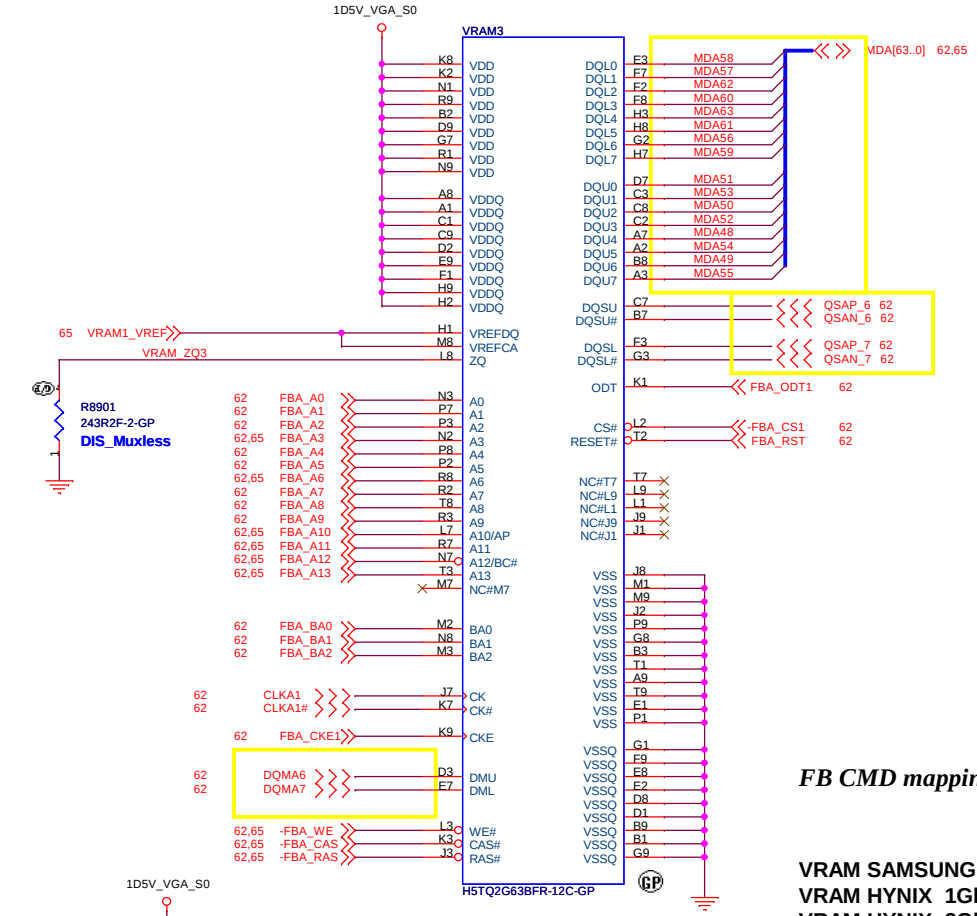


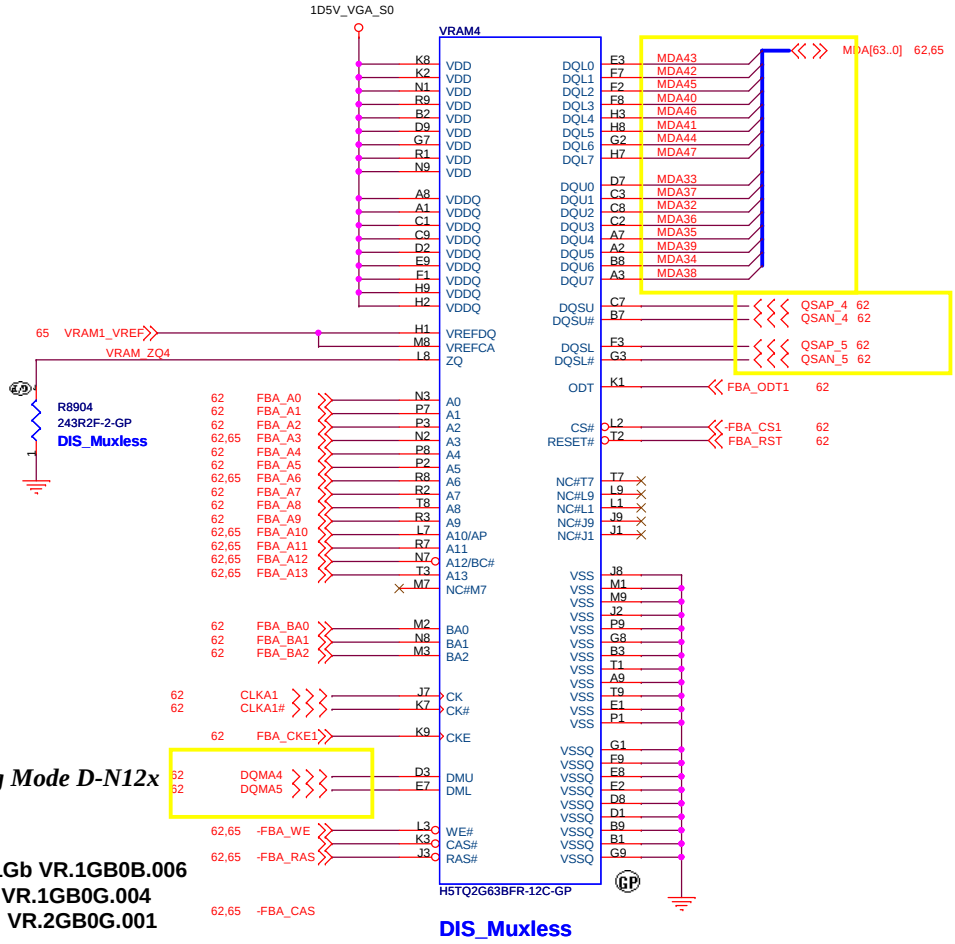




Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM1,2 (1/4)		
Size: A3	Document Number: JE43-CP	Rev: -1
Date: Wednesday, November 24, 2010	Sheet 65 of 69	

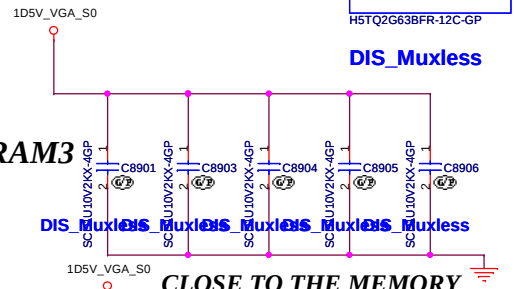




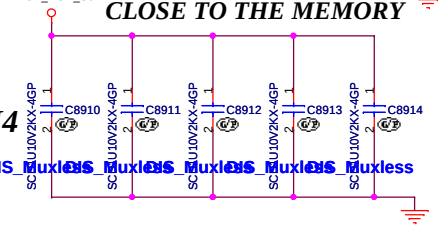
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb VR.1GB0G.004
VRAM HYNIX 2Gb VR.2GB0G.001

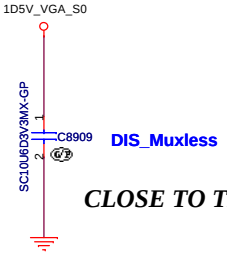
FOR VRAM3



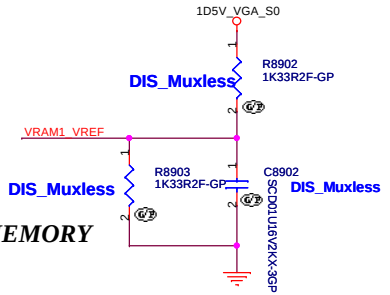
CLOSE TO THE MEMORY

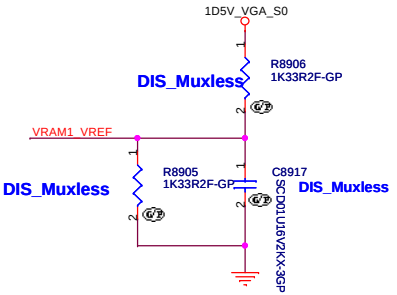


FOR VRAM4



CLOSE TO THE MEMORY





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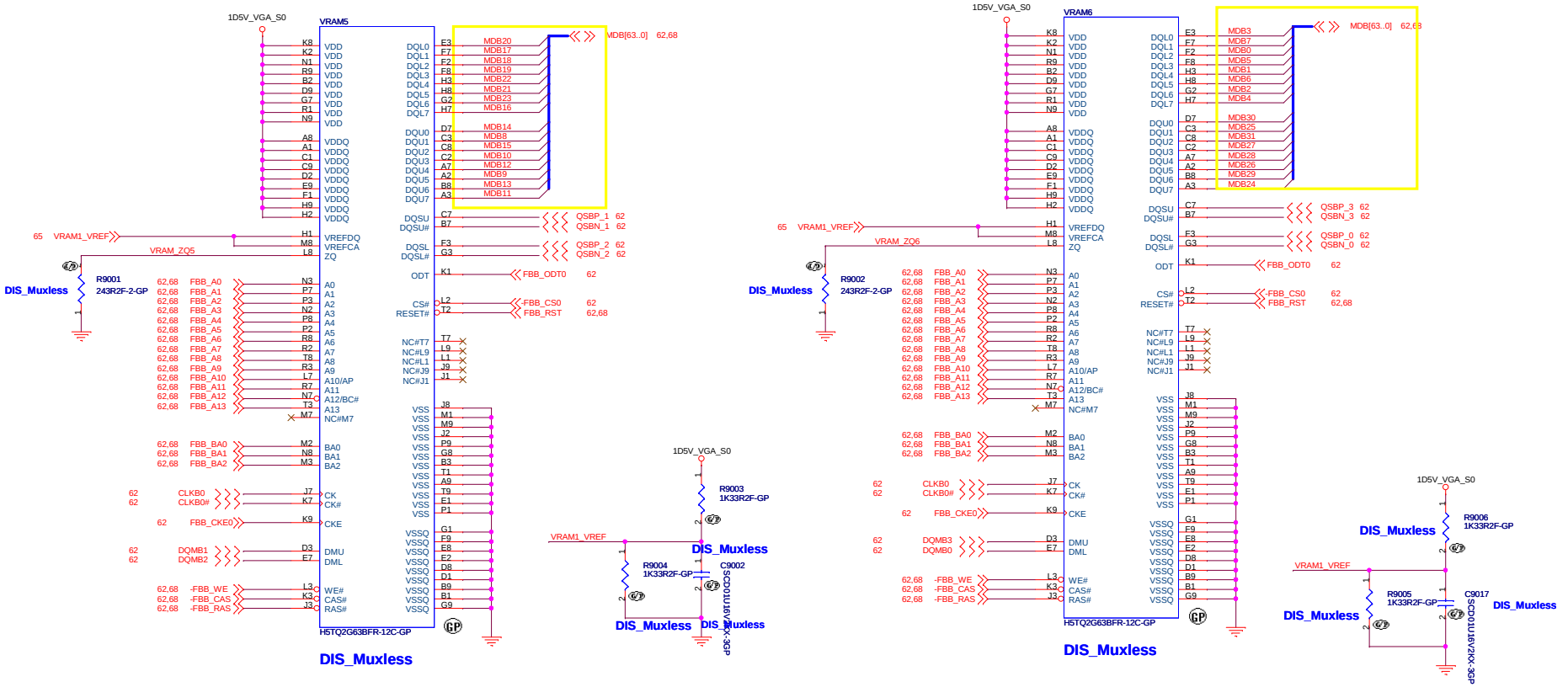
Title: **GPU-VRAM3,4 (2/4)**

Size	Document Number	Rev
A3	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 66 of 69



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb VR.1GB0G.004
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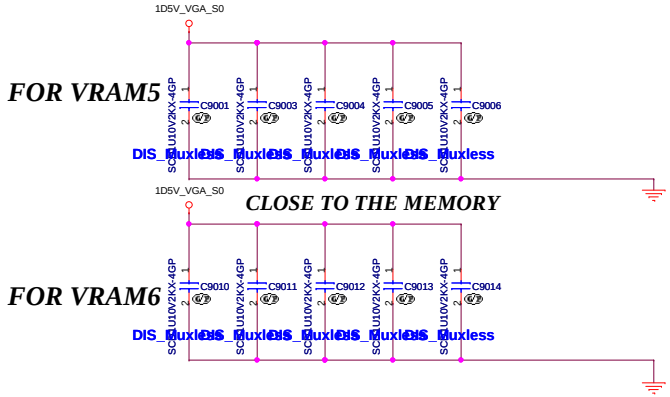
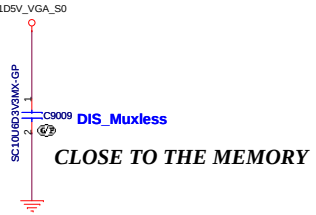


DG requires 4x0.1uF and 8x1.0uF per VRAM chip



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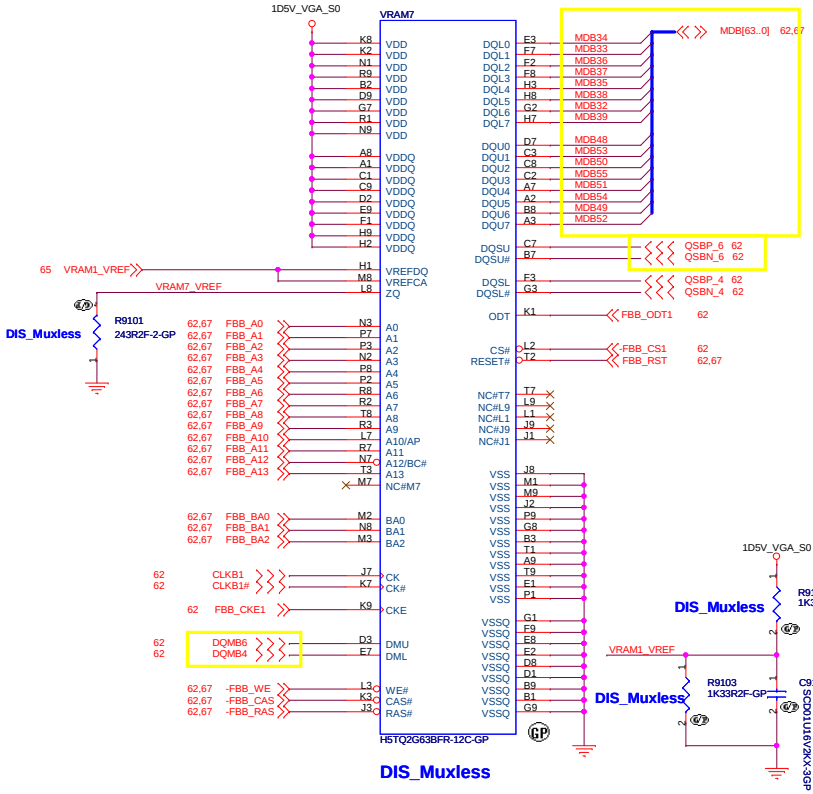
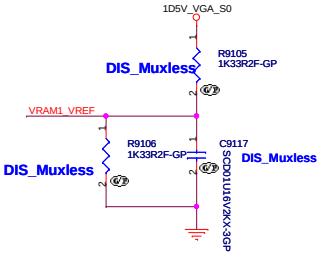
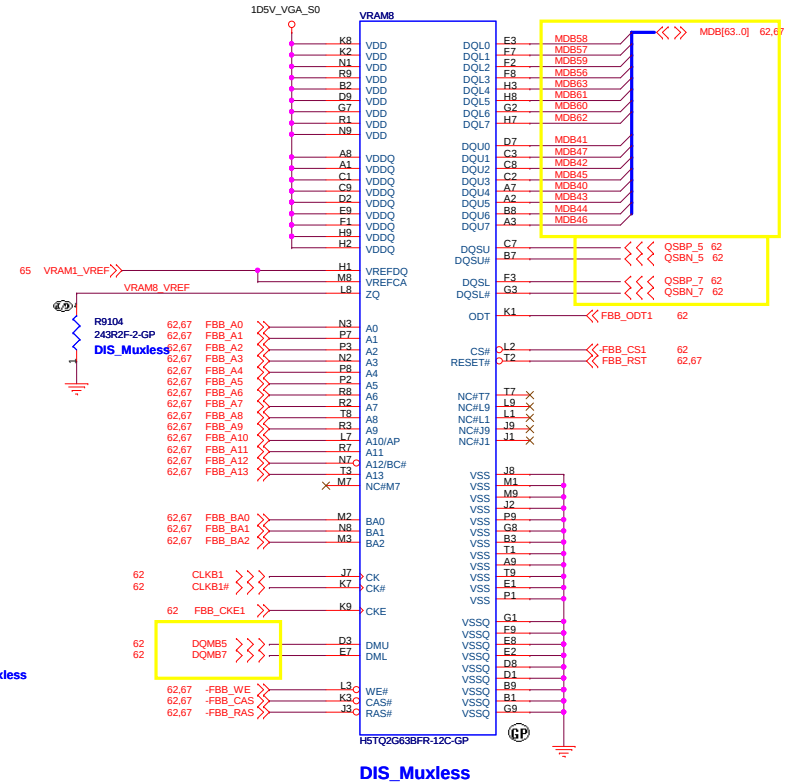
Title: GPU-VRAM5,6 (3/4)
Size: Custom | Document Number: JE43-CP | Rev: -1
Date: Wednesday, November 24, 2010 | Sheet 67 of 69

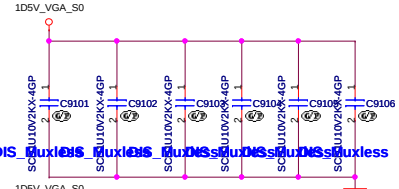






VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb VR.1GB0G.004
VRAM HYNIX 2Gb VR.2GB0G.001

FOR VRAM7



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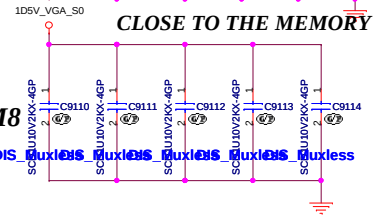
FOR VRAM8



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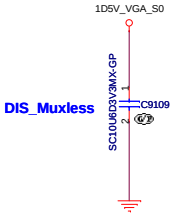

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Size	Document Number	Rev
Custom	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 68 of 69

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Title: ***Modify History***

Size	Document Number	Rev
	JE43-CP	-1

Date: Wednesday, November 24, 2010 Sheet 69 of 69